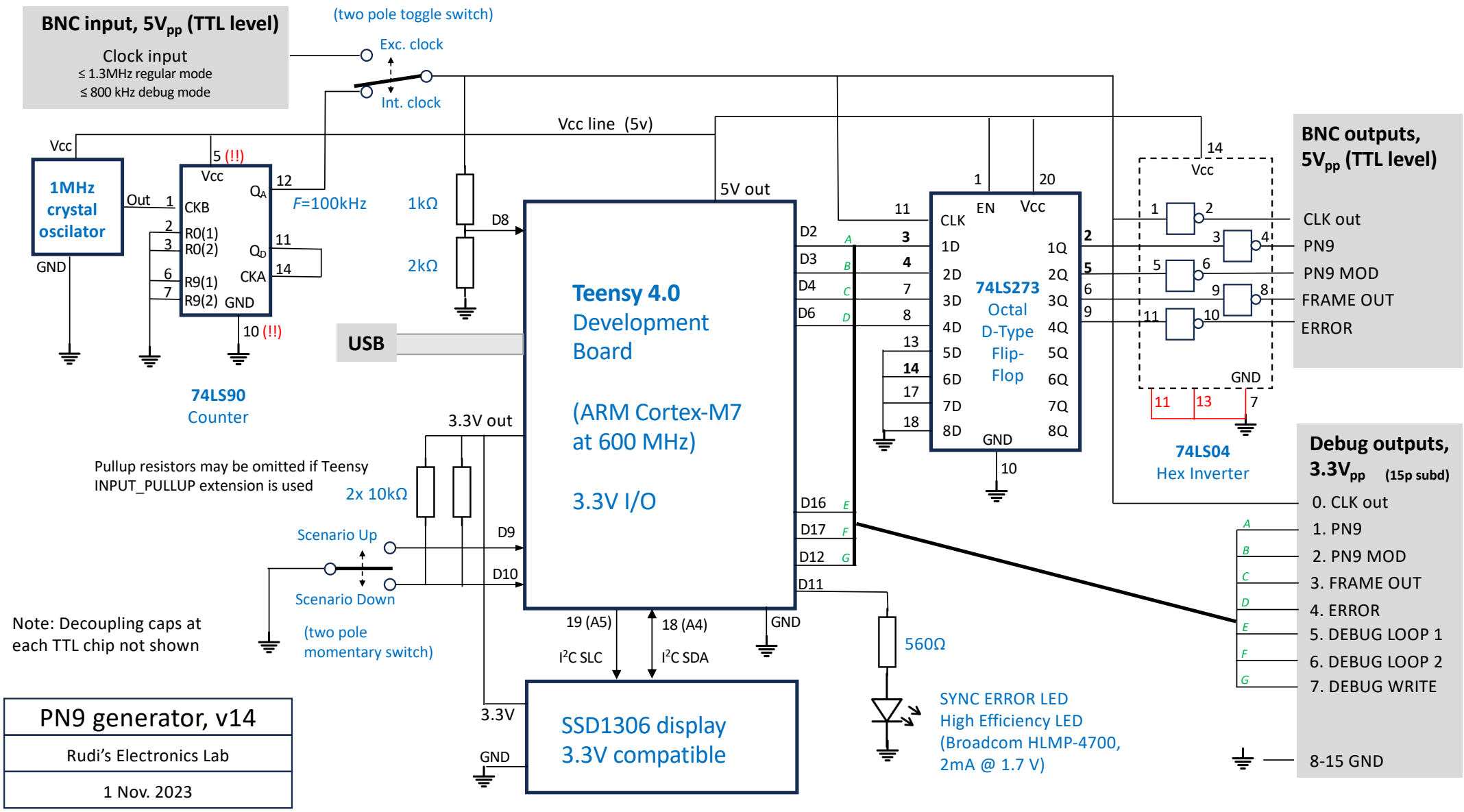
BNC input, 5Vpp (TTL level)
Clock input
≤ 1.3MHz regular mode
≤ 800 kHz debug mode
(two pole toggle switch)
Exc. clock
Int. clock
Vcc line (5v)
Vcc
1MHz crystal oscilator
Out
GND
5 (!!)
Vcc
CKB
R0(1)
R0(2)
R9(1)
R9(2)
GND
QA
QD
CKA
12
11
14
10 (!!)
74LS90
Counter
F=100kHz
1kΩ
2kΩ
D8
USB
5V out
Teensy 4.0
Development
Board
(ARM Cortex-M7
at 600 MHz)
3.3V I/O
D2
D3
D4
D6
D16
D17
D12
D11
19 (A5)
18 (A4)
GND
I2C SLC
I2C SDA
3.3V out
Pullup resistors may be omitted if Teensy
INPUT_PULLUP extension is used
2x 10kΩ
Scenario Up
Scenario Down
D9
D10
(two pole
momentary switch)
Note: Decoupling caps at
each TTL chip not shown
3.3V
GND
SSD1306 display
3.3V compatible
560Ω
SYNC ERROR LED
High Efficiency LED
(Broadcom HLMP-4700,
2mA @ 1.7 V)
CLK
EN
Vcc
1D
2D
3D
4D
5D
6D
7D
8D
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
74LS273
Octal
D-Type
Flip-
Flop
74LS04
Hex Inverter
BNC outputs,
5Vpp (TTL level)
CLK out
PN9
PN9 MOD
FRAME OUT
ERROR
Debug outputs,
3.3Vpp (15p subd)
0. CLK out
1. PN9
2. PN9 MOD
3. FRAME OUT
4. ERROR
5. DEBUG LOOP 1
6. DEBUG LOOP 2
7. DEBUG WRITE
8-15 GND
PN9 generator, v14
Rudi's Electronics Lab
1 Nov. 2023