EXION: Exploiting Inter- and Intra-Iteration Output Sparsity for Diffusion Models

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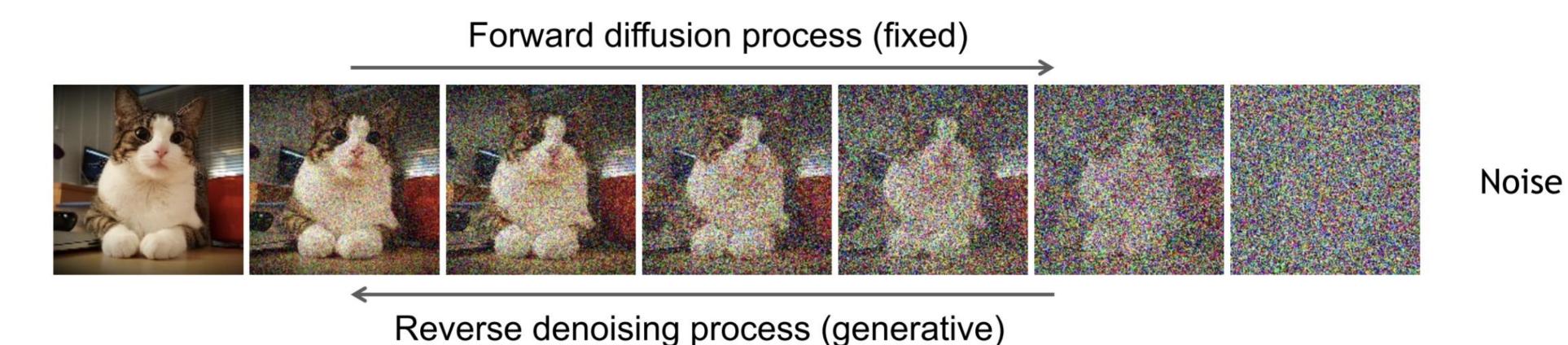
Preliminaries

Data

Denoising Diffusion Models: Learning to generate by denoising

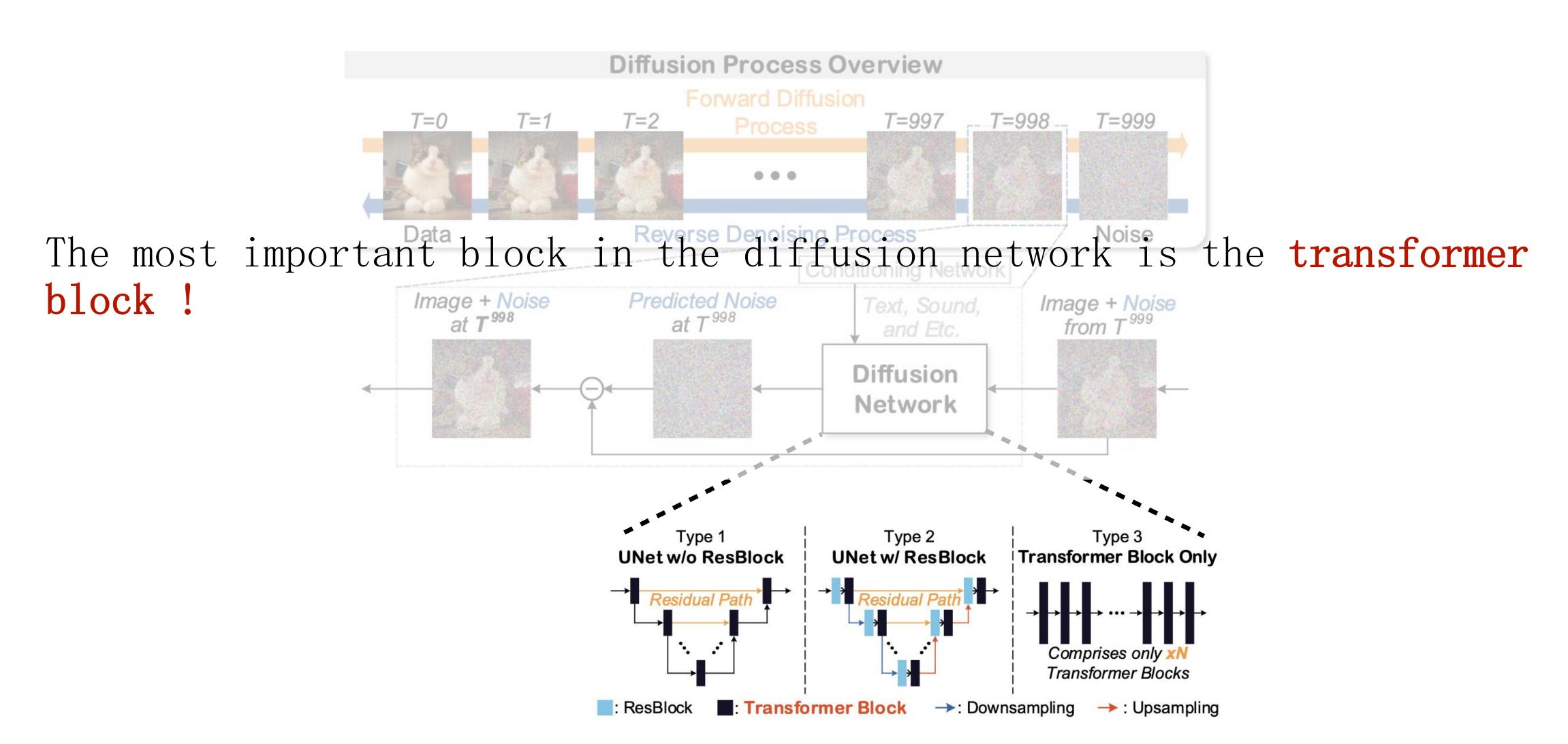
Denoising diffusion models consist of two processes:

- Forward diffusion process that gradually adds noise to input
- Reverse denoising process that learns to generate data by denoising



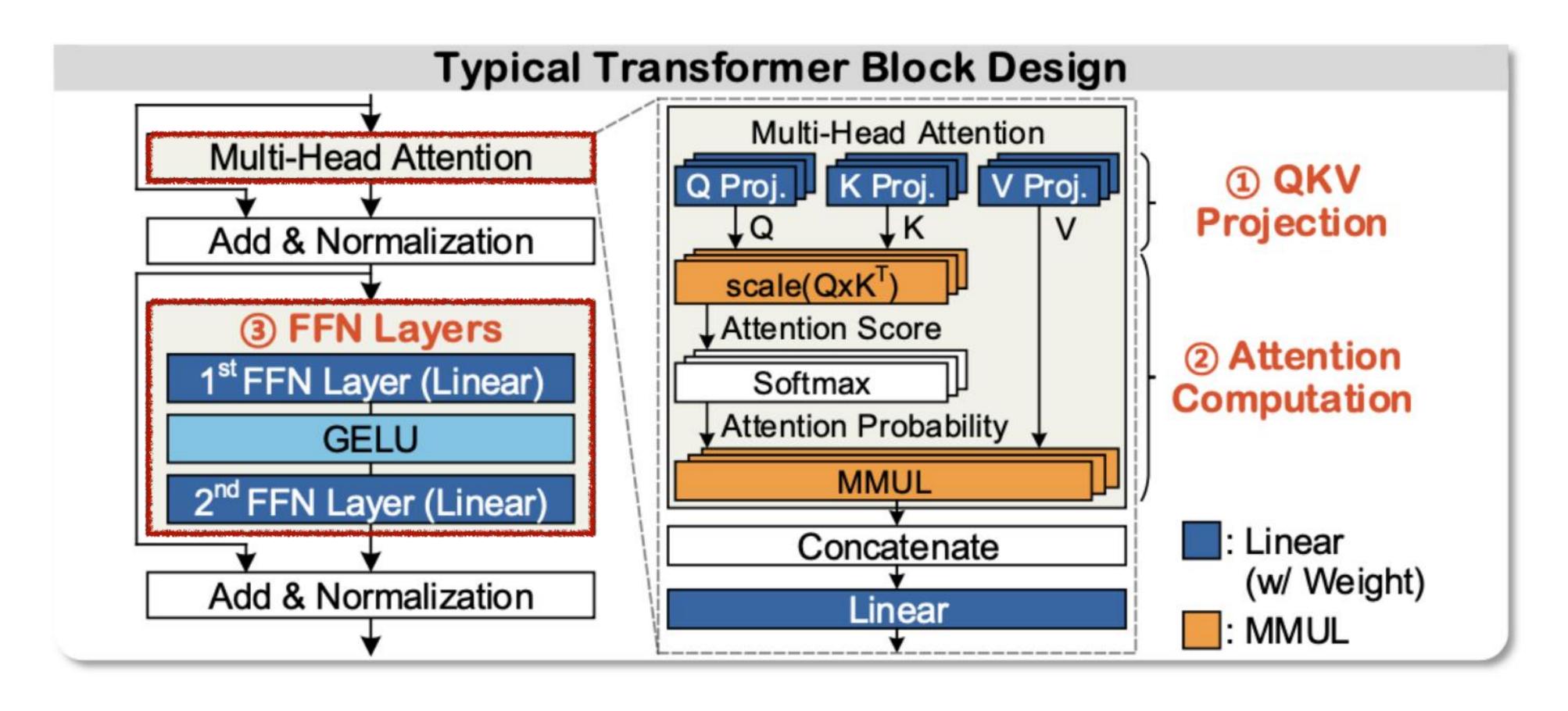
Preliminaries

Denoising Diffusion Models: Learning to generate by denoising



Preliminaries

Transformer Block Design



Problems

Better outputs come with higher energy consumption and longer latency: (Each generation requires numerous denoising iterations

- Each iteration evaluates numerous Transformer Blocks
- Each transformer block entails a large number of operations

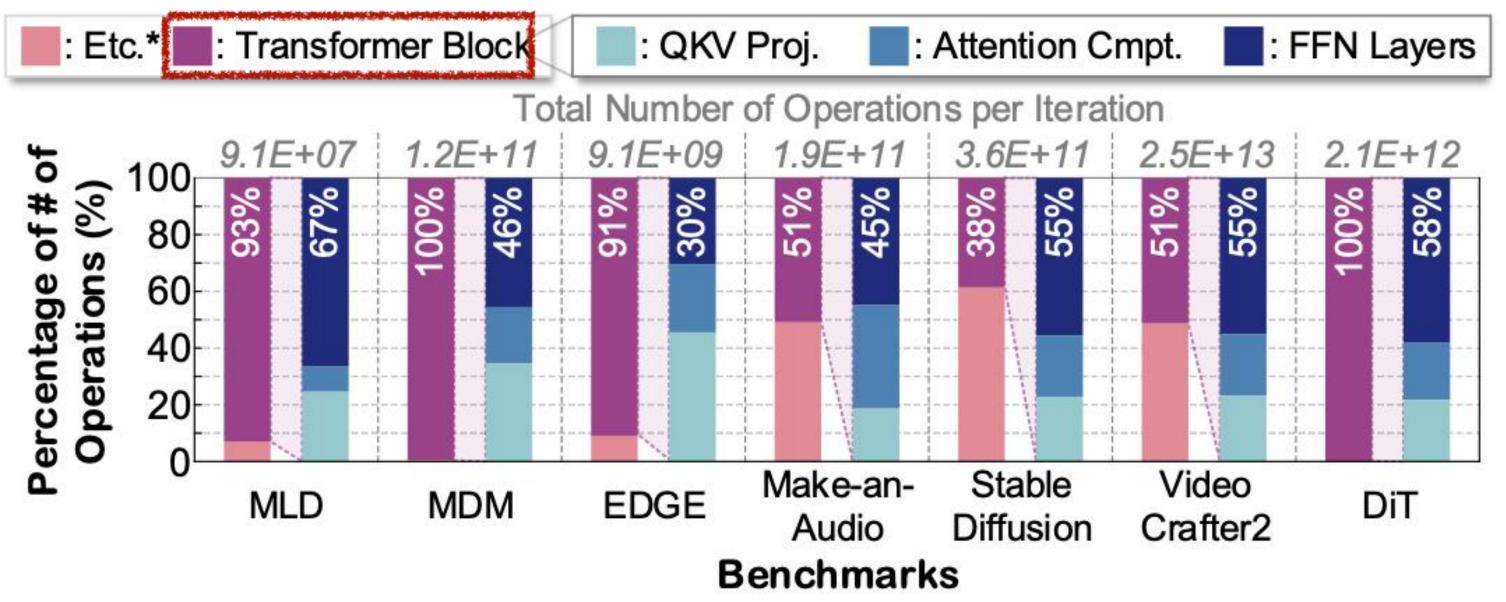
Metric	StyleGAN-XL	Stable Diffusion	
Energy (Joules)	~65.5 J	1546.7 J	X23.6 more energy
Latency (sec)	~1.2 s	11.8 s	X 9.8 slower

Experiment results on NVIDIA's RTX 6000 Ada

Problems

Better outputs come with higher energy consumption and longer latency: (

Fig. Number of Operations Breakdown



- *: Includes entire operations except transformer blocks
- the transformer block accounts for the highest ratio
- the FFN layers are generally the most compute-intensive

Overview

EXION: Exploiting Inter- and Intra-Iteration Output Sparsity for Diffusion Models

Key ideas: exploiting the unique <u>inter-</u> and <u>intra-</u>iteration <u>output sparsity</u>

Overview

EXION: Exploiting Inter- and Intra-Iteration Output Sparsity for Diffusion Models

Key ideas

1. Software optimizations

• FFN-Reuse across different iterations

• Sparse attention computation via eager prediction

2. ConMerge: data compaction mechanism

3. Specialized hardware architecture

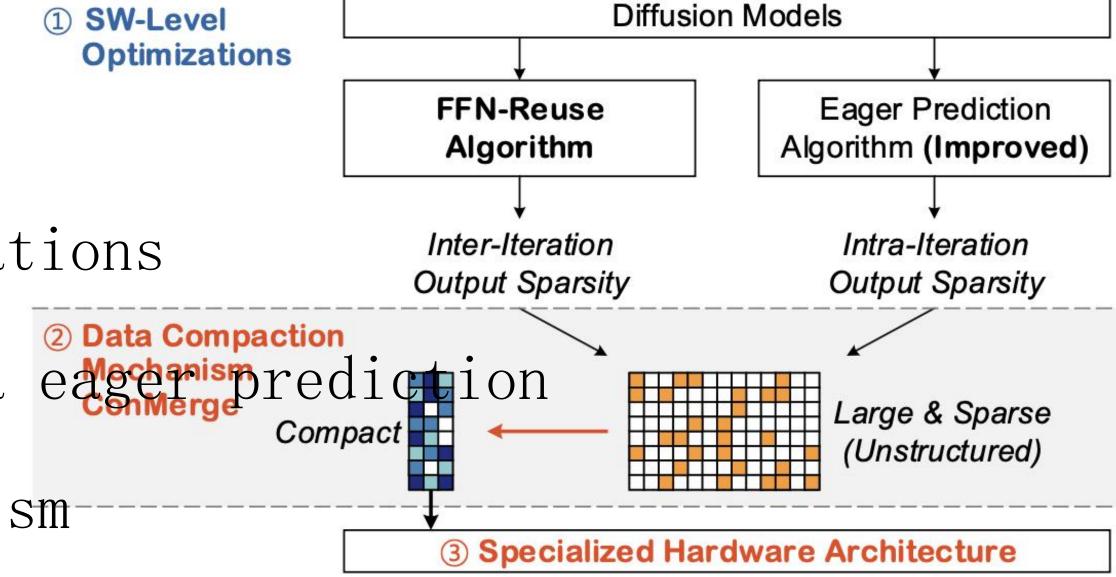
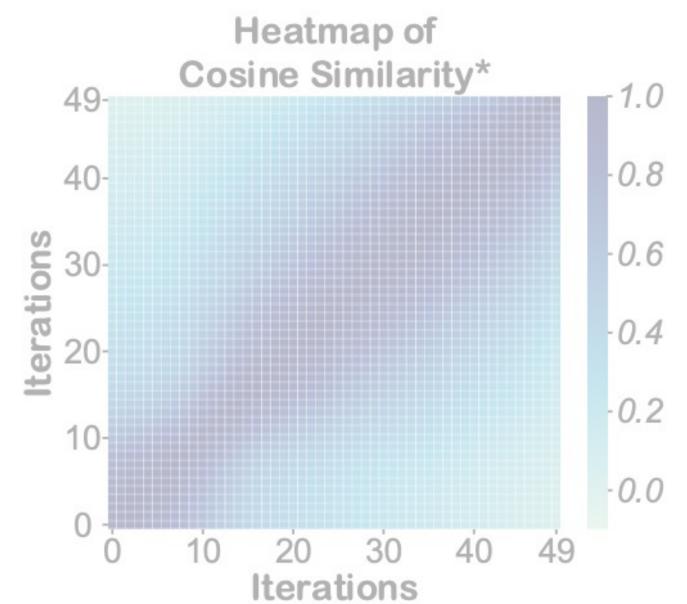


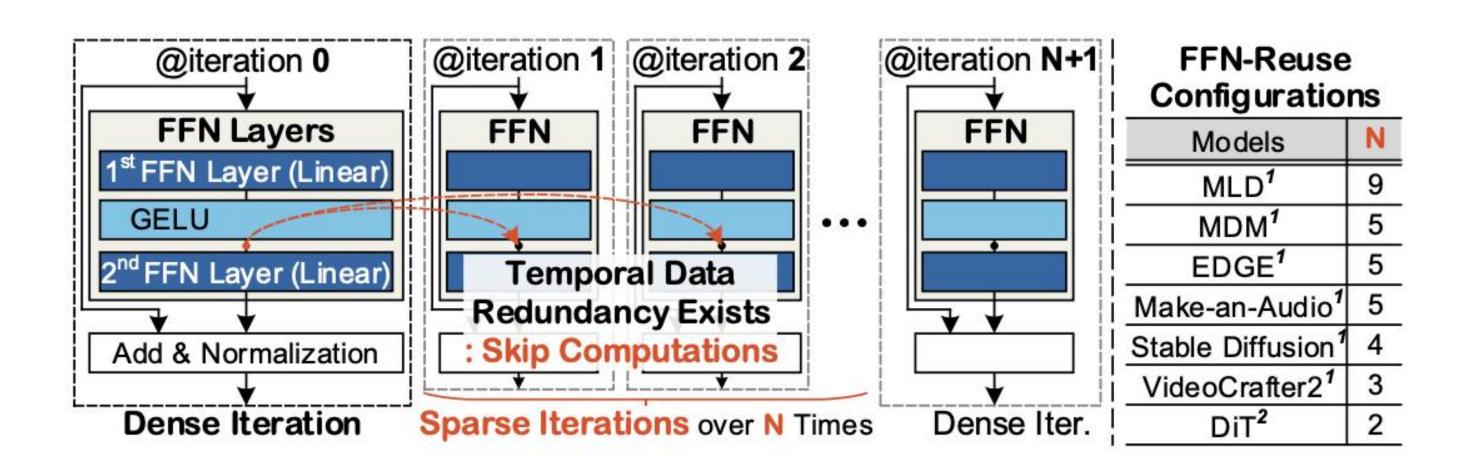
Fig. 1. Overview of EXION Accelerator

Software optimization 1. FFN-Reuse (inter iteration)

Observation: temporal data redundancy exists across different iterations in

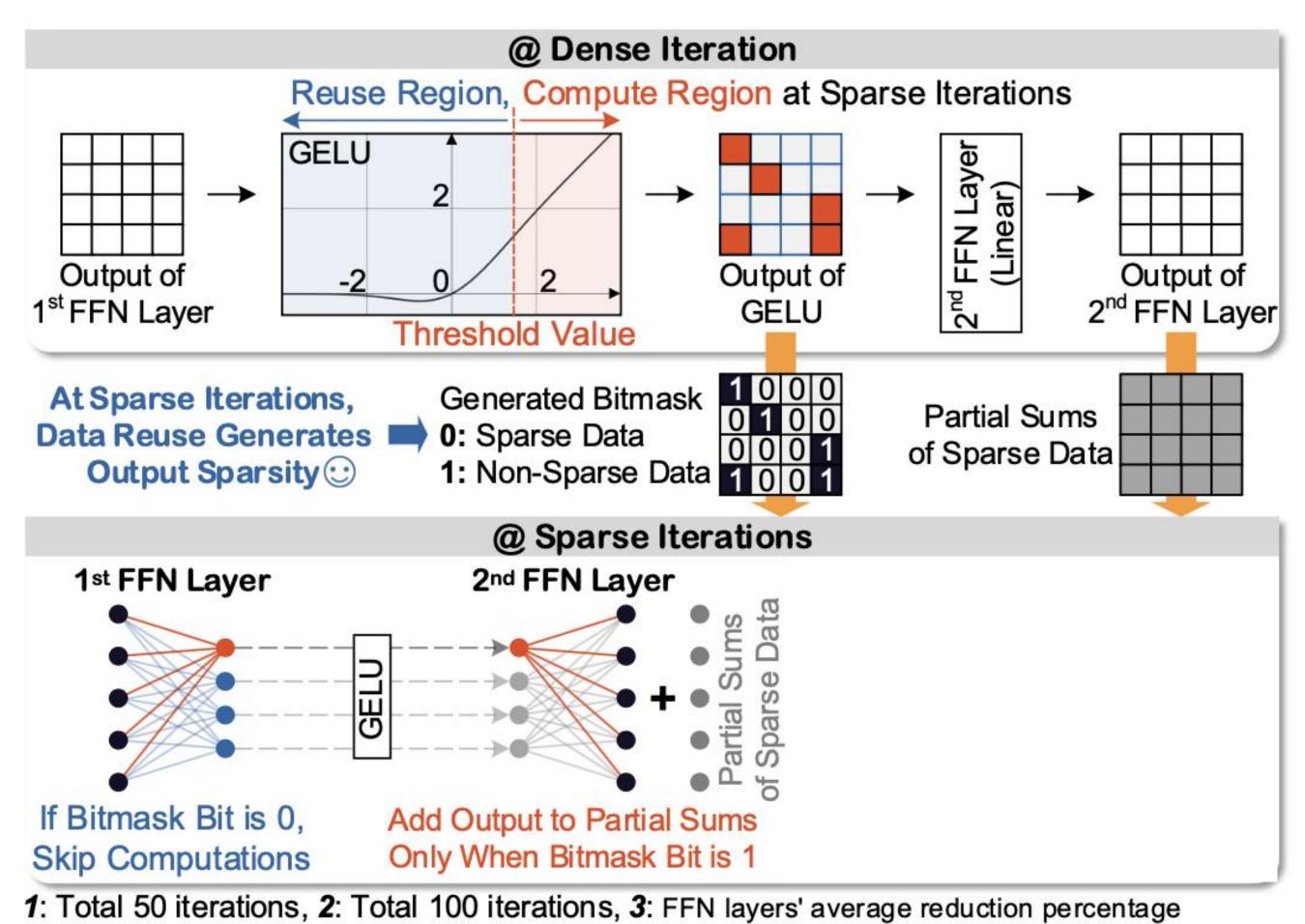


*: Cosine similarity of 2nd block's GELU output in FFN layers across different iterations in DiT model



Software optimization 1. FFN-Reuse (inter iteration)

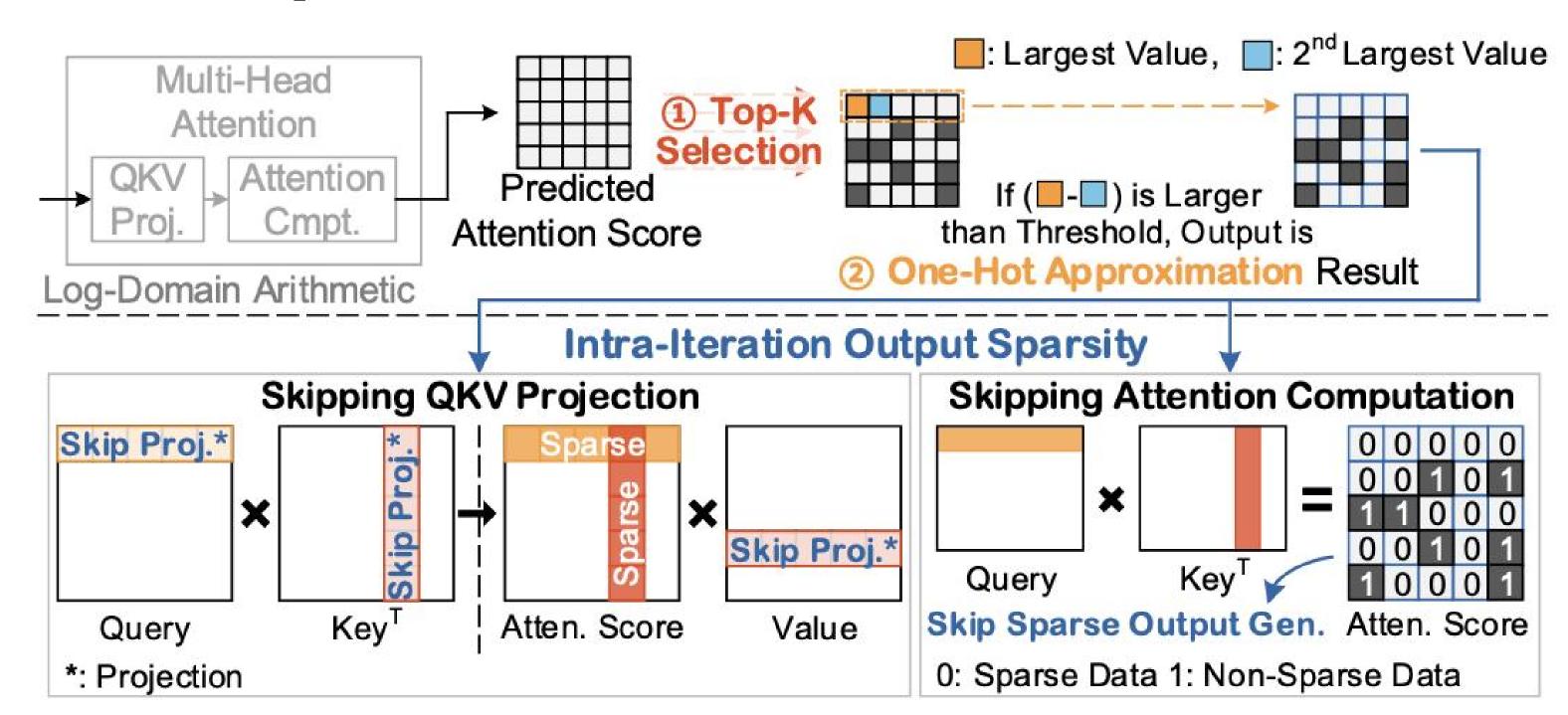
Fig: FFN-Reuse Algorithm for Inter-iteration Output Sparsity



Software optimization 2. Early Prediction (intra iteration)

Goal: predict attention score to skip unnecessary computations

- Skip QKV projection
- Skip attention computation (Q * K^T)



Software optimization 2. Early Prediction (intra iteration)

Question: how to estimate the attention early before the QKV generation?

FACT: FFN-Attention Co-optimized Transformer Architecture with Eager Correlation Prediction

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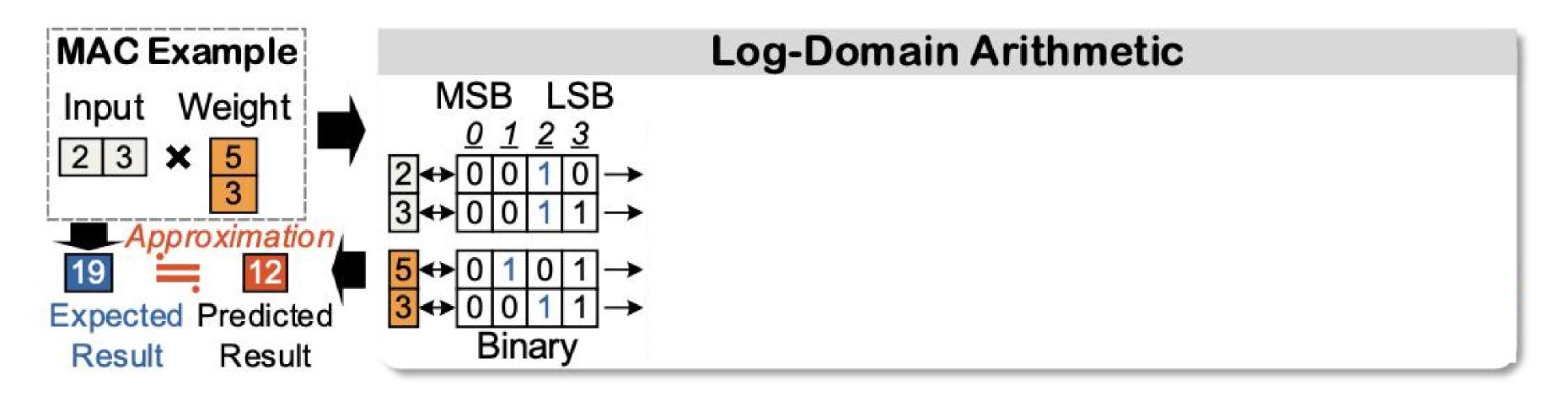
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Software optimization 2. Early Prediction (intra iteration)

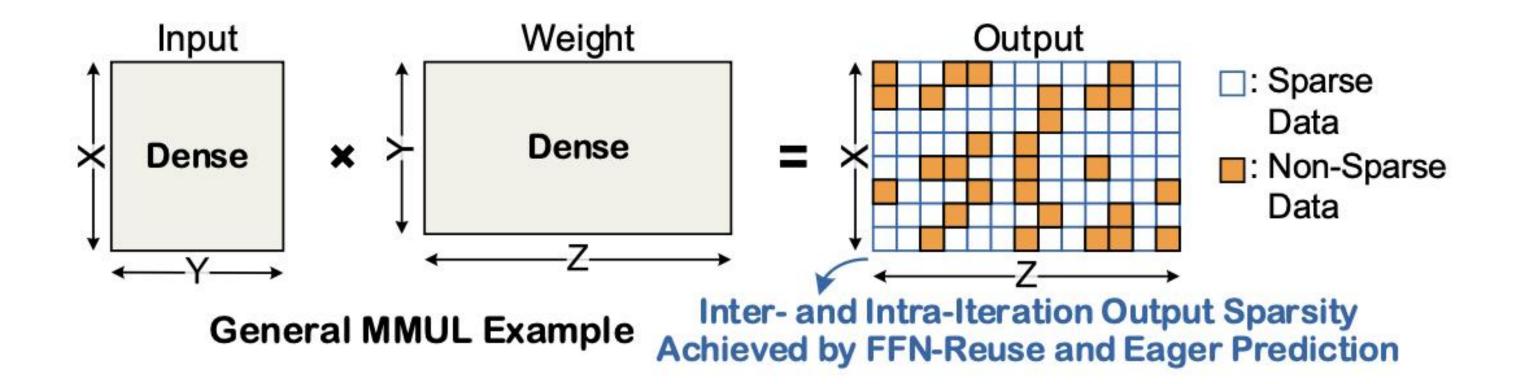
Key ideas: use a log-based multiplication-free prediction

- First transforms the data into log-domain by using a leading-one detector
- Then substitutes the costly multiplication with low-power shift-and-add op



Ps: an INT-type number α can be decomposed as: $\alpha = Sign \times 2^{(W-LO-1)} \times M$ the multiplication of two INT-type numbers: $\alpha \times \beta = XOR(Sign_{\alpha}, Sign_{\beta})$ $\times 2^{(W_{\alpha} + W_{\beta} - (LO_{\alpha} + LO_{\beta}) - 2)} \times (M_{\alpha} \times M_{\beta})$

Inter- and Intra-Iteration Output Sparsity



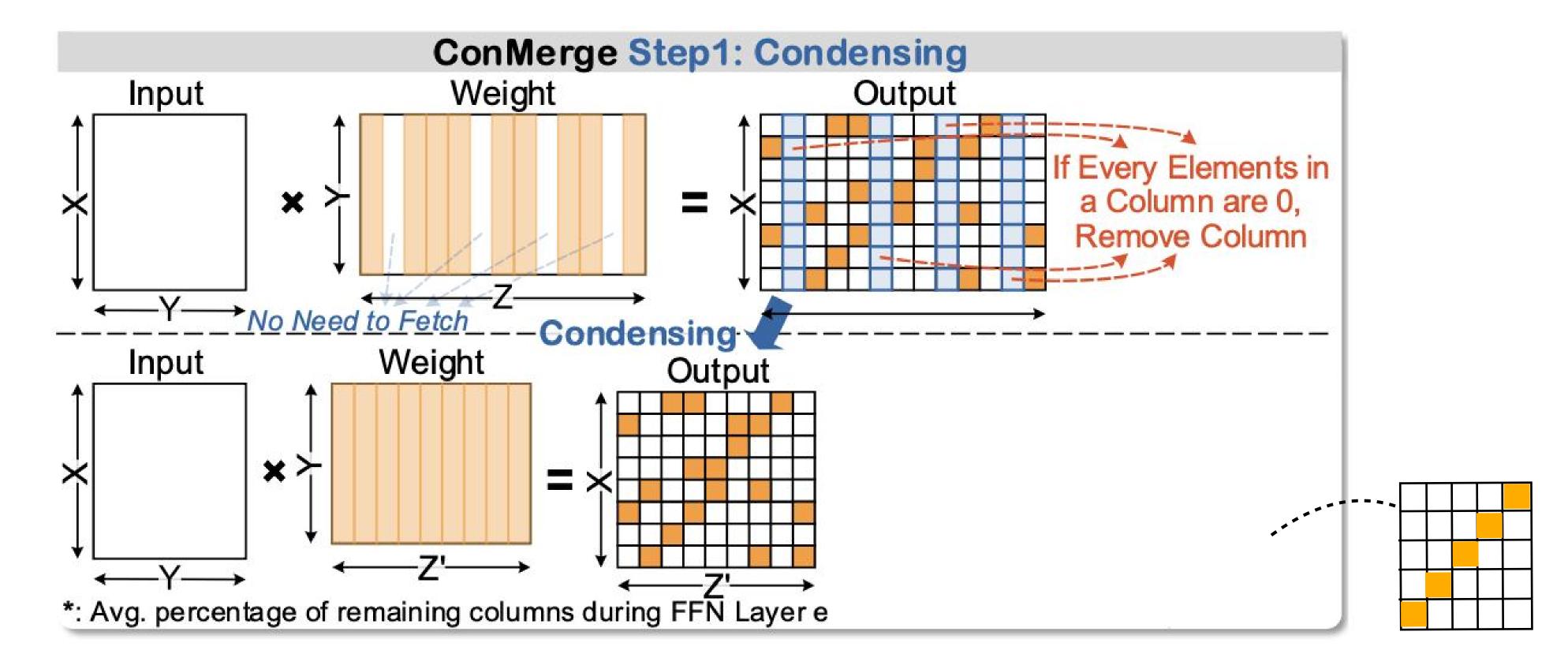
Problem: Conventional HW, such as GPUs, cannot utilize it to reduce energy

ConMerge: data compaction mechanism

Goal: to condense and merge large&sparse matrices into small&compact forms

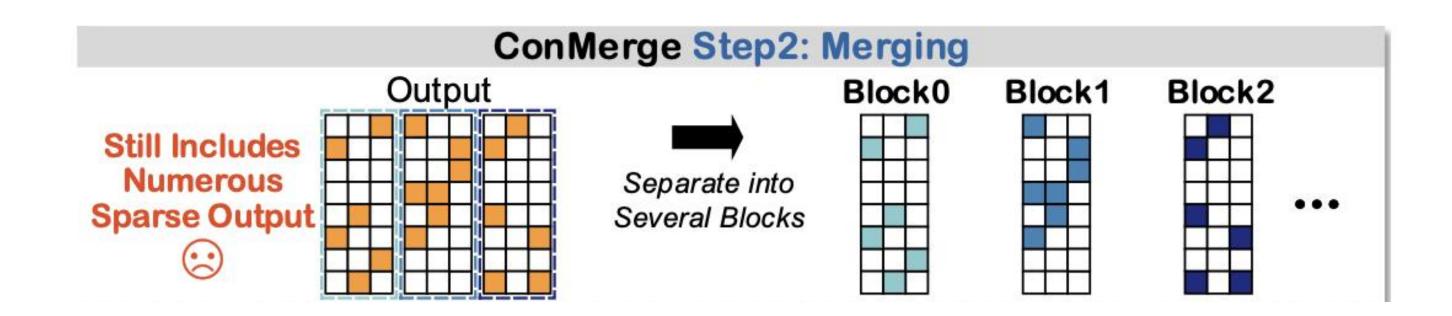
ConMerge: data compaction mechanism

condense

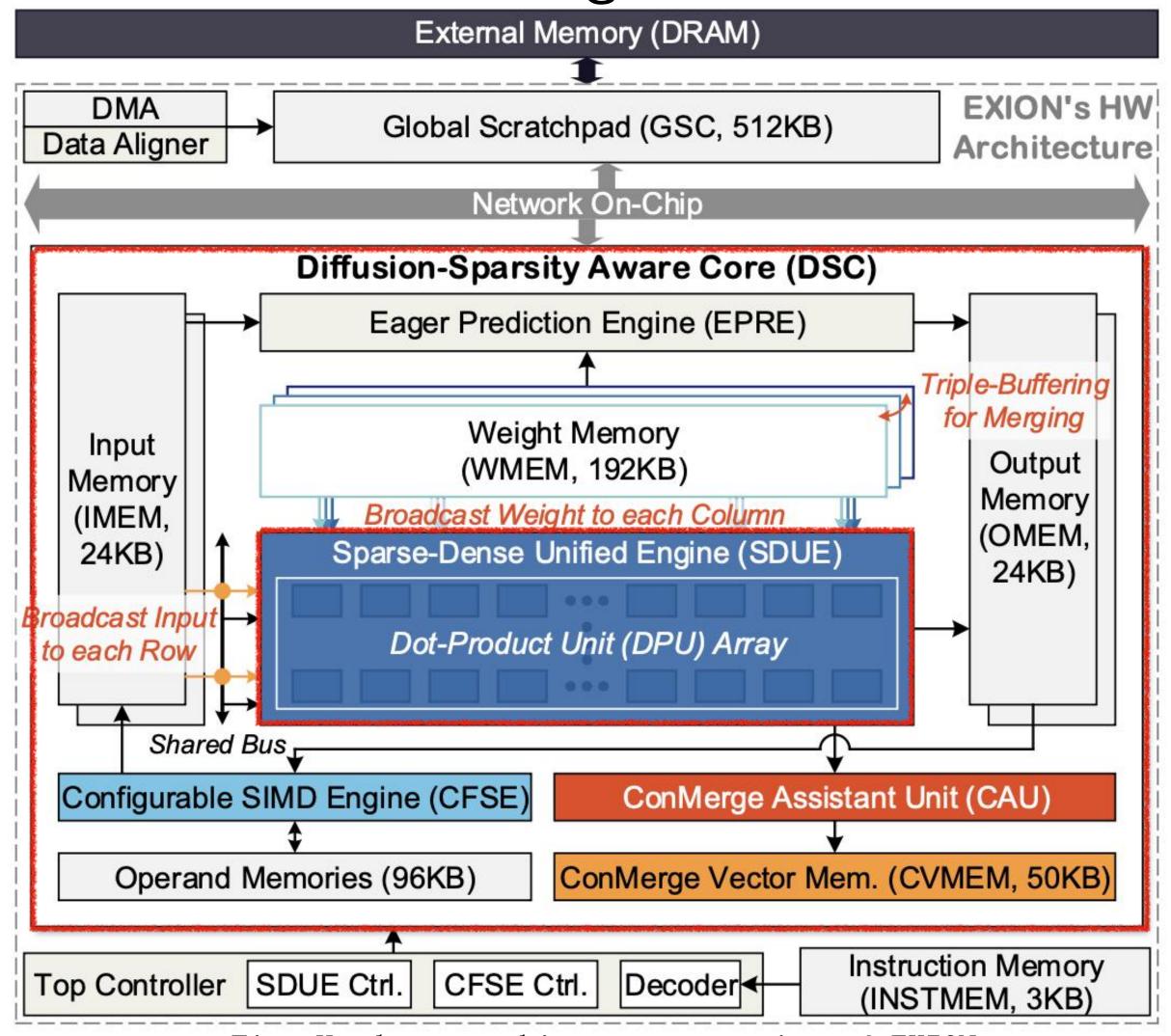


ConMerge: data compaction mechanism

• merge



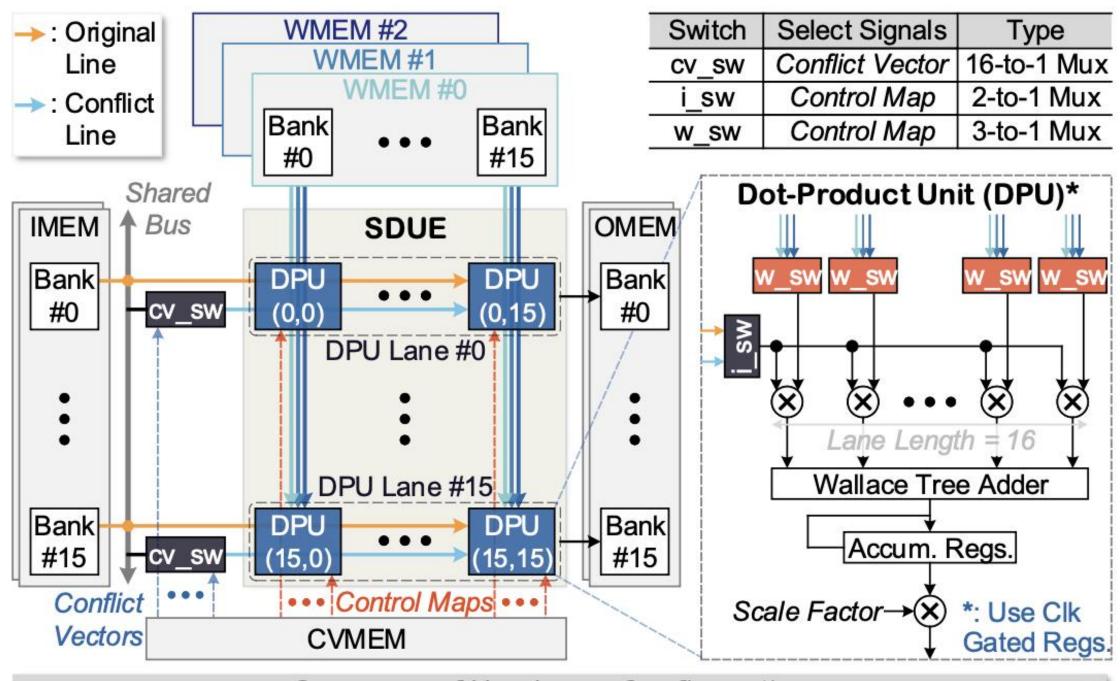
Hardware co-design: Overview



DSC: run the diffusion model's dense and sparse iterations

Fig: Hardware architecture overview of EXION

Hardware co-design: Sparse-Dense Unified Engine (SDUE)



Summary of Hardware Configurations								
Toy HW Model (Figure 8-9) EXION Configuration								
	SDUE SDUE							
DPU	# of Rows	8		DPU	# of F	Rows	16	
Array	# of Columns	3		Array	# of Co	lumns	16	
	Memory* Memory*							
# 0.5	IMEM	8		ш ос	5KB per Bank)			
# of Banks	WMEM	3		# of Banks	WMEM 16 (12KB per Bank)			
Daliks	OMEM	8		Daliks	OMEM	16 (1.	5KB per Bank)	
*: Configuration of a single memory between/among double/triple-buffered memories								

cv switch: conflict vector switch

i_sw: input switch

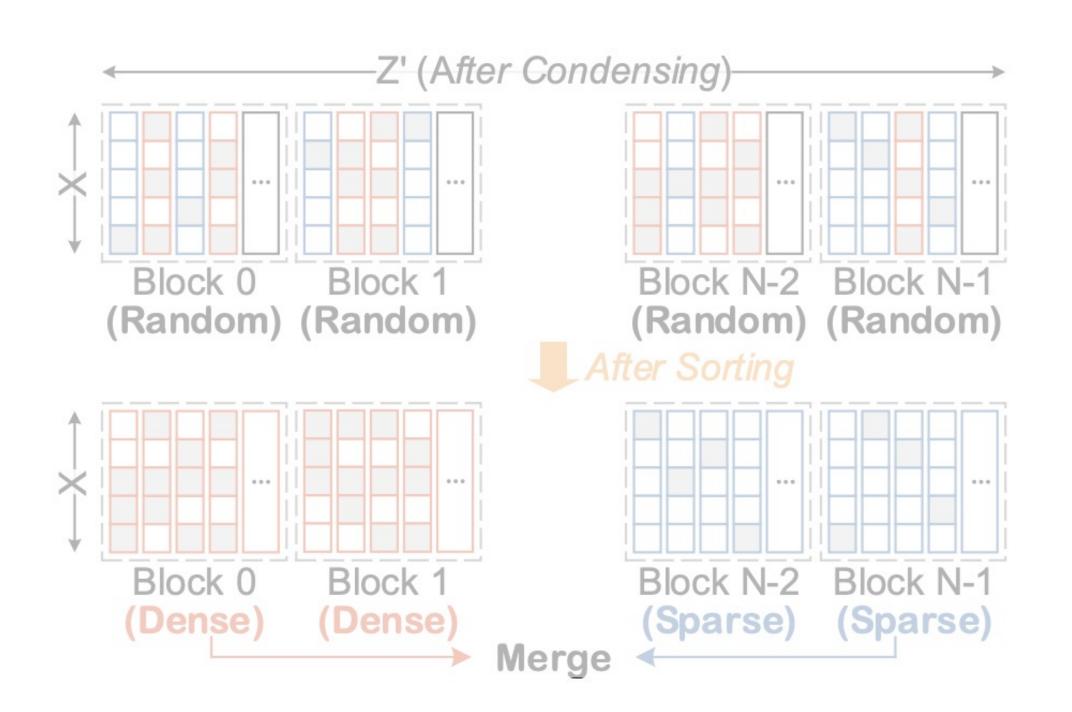
w_sw: weight switch

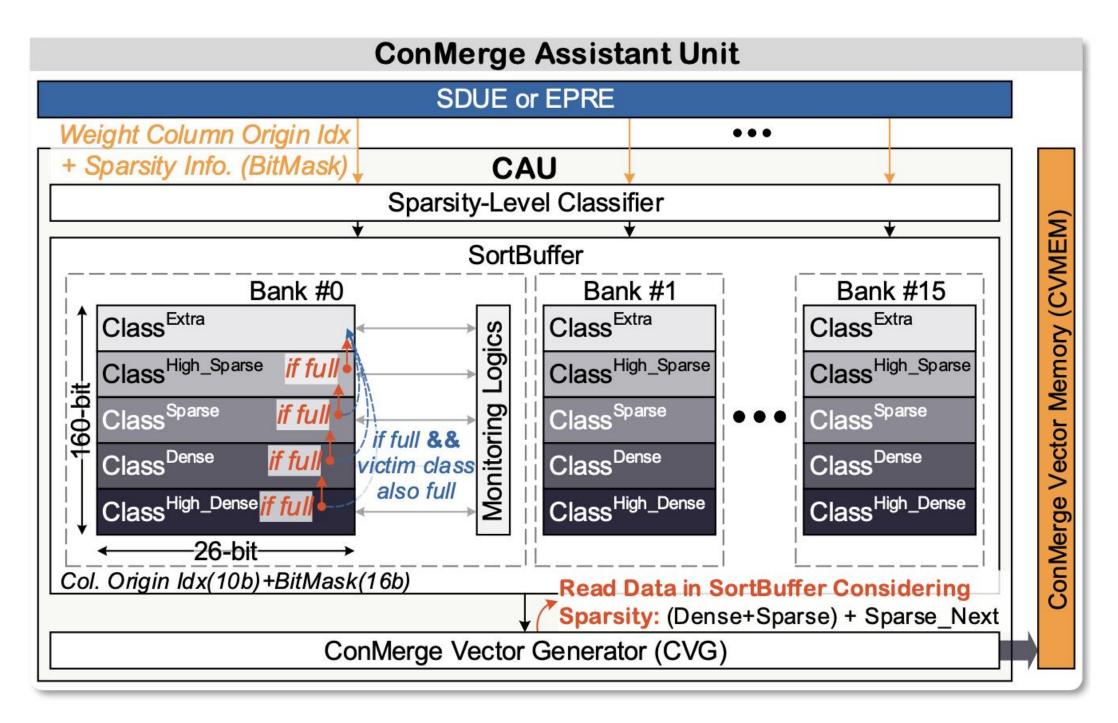
SDUE can compute:

- the normal dense output matrix
- and also the ConMerged block

Hardware co-design: ConMerge Assistant Unit (CAU)

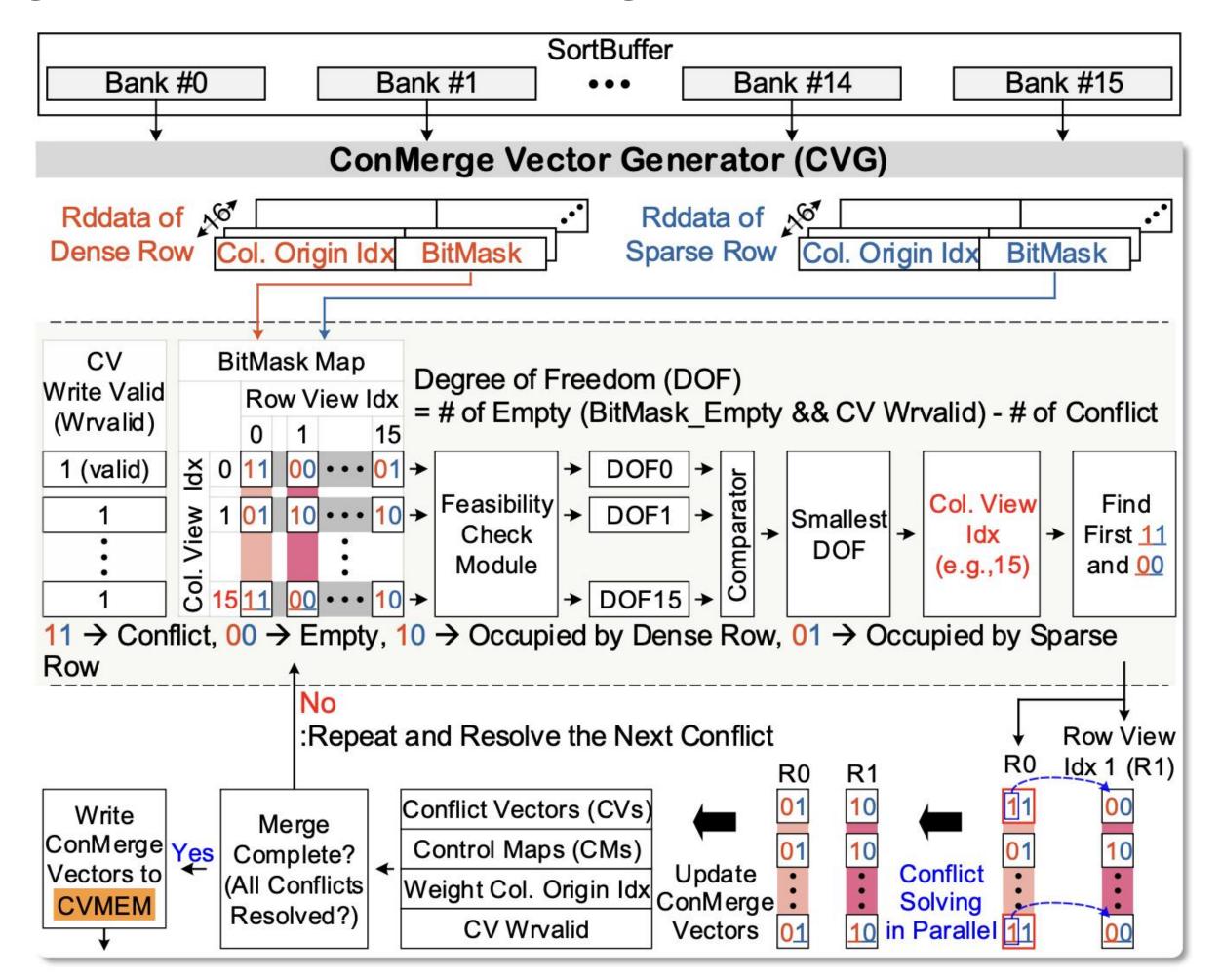
• Sorting strategies for fast merging





Hardware co-design: ConMerge Assistant Unit (CAU)

• Detailed Merging Process in ConMerge Vector Generator



Experimental setup

• Workloads selected: seven different diffusion models

```
text-to-motion (MLD and MDM)
music-to-motion (EDGE)

text-to-image (Stable Diffusion)

class-to-image (DiT)

text-to-audio (Make-an-Audio)

text-to-video (VideoCrafter2)
```

• Hardware specifications of GPUs

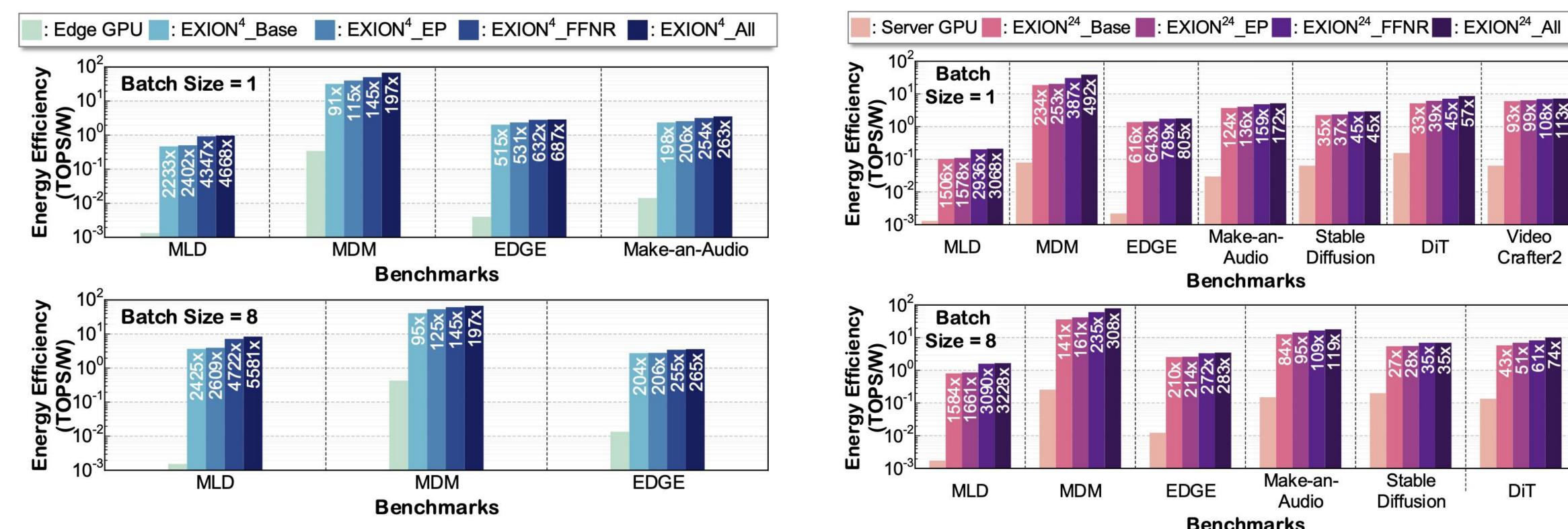
	Edge GPU	Server GPU
	NVIDIA Jetson Orin Nano	NVIDIA RTX 6000 Ada
Throughput	40.0 TOPS	91.1 TFLOPS ¹
Memory Bandwidth	68 GB/s	960 GB/s
Power Consumption	-15W	-300W

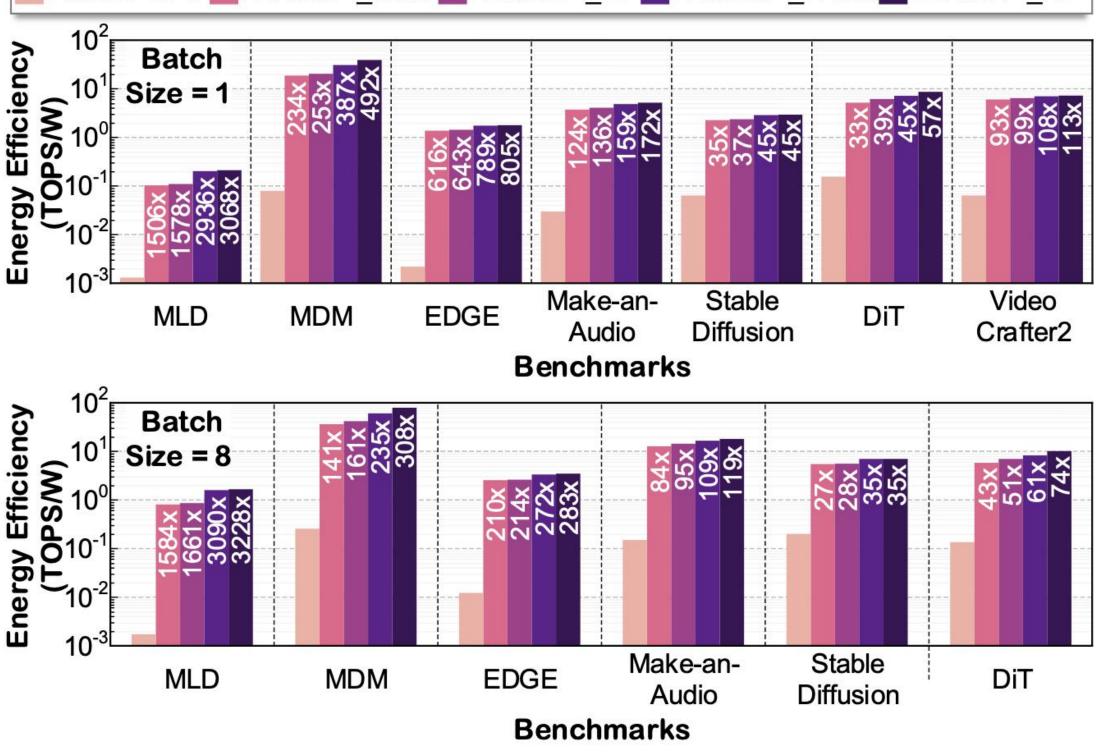
Accuracy Evaluation

	Models		MLD	M	DM	El	DGE	Make-a	n-Audio	Stab	le Diffu	sion		DiT		Vid	eoCraf	ter2
	Task	Text	t-to-Motion	Text-to	o-Motion	Music-	to-Motion	Text-to	o-Audio	Te	xt-to-lma	to-Image Generation		Image Generation		Te	Text-to-Video	
	Dataset	Hun	manML3D	Huma	nML3D	AIS	ST++	Audio	oCaps	C	OCO 20	14	ImageNet 2012		2012 ECTV			
To	tal Iterations		50	,	50		50	5	50		50		100		50			
20						Output :	Sparsity A	chieved	by EXIO	N's Soft	ware-L	evel Optii	mization	S				
FFN-	Inter-Iter. Sparsity	ter-Iter. Sparsity 95% 95%		5%	95% 97%		7%	97%		1	80%			70%				
Reuse	N ¹		9		5		5		5		4			2			3	
EP ²	Intra-Iter. Sparsity (q_th³, k⁴)	(q_th=	30% =0.3, k=0.7)		5% 3, k=0.05)		50% 0.9, k=0.5)		0% 7, k=0.2)	20% (q_th=0.8, k=0.8)		95% (q_th=0.15, k=0.05)		50% (q_th=2, k=0.5)		0.5)		
	*							Accu	racy Eval	luation N	/letric							
Appli	ed Methods	FID (↓) w/ GT⁵	R-Precision (†)	FID (↓) w/ GT⁵	PSNR w/ Vanil. ⁶ (↑)	PFC (↓)	Beat Align Score (↑)		PSNR w/ Vanil. ⁶ (↑)		IS (↑)	PSNR w/ Vanil. ⁶ (↑)		IS (↑)	PSNR w/ Vanil. ⁶ (↑)	VQA _A(↑)	IS (↑)	PSNR w/ Vanil. ⁶ (↑)
Vanil	a Model	0.393	0.754	0.406	-	1.352	0.218	4.618	-	26.63	33.11	- 1	10.63	265.73	-	59.68	17.06	-
FFN-	Reuse	0.401	0.752	0.467	19.22	1.389	0.214	4.932	27.14	26.05	33.04	18.20	14.42	265.73	15.99	58.92	16.83	28.25
FFN-	Reuse+EP²	0.410	0.745	0.968	17.84	2.241	0.195	4.975	26.09		-	14.06	-		14.60		-	27.86
FFN-F	Reuse+EP ² +Quant. ⁷	0.410	0.744	1.080	17.67	2.411	0.193	5.131	25.72	-	18=05	13.94	-	10 05	14.57	-		27.56

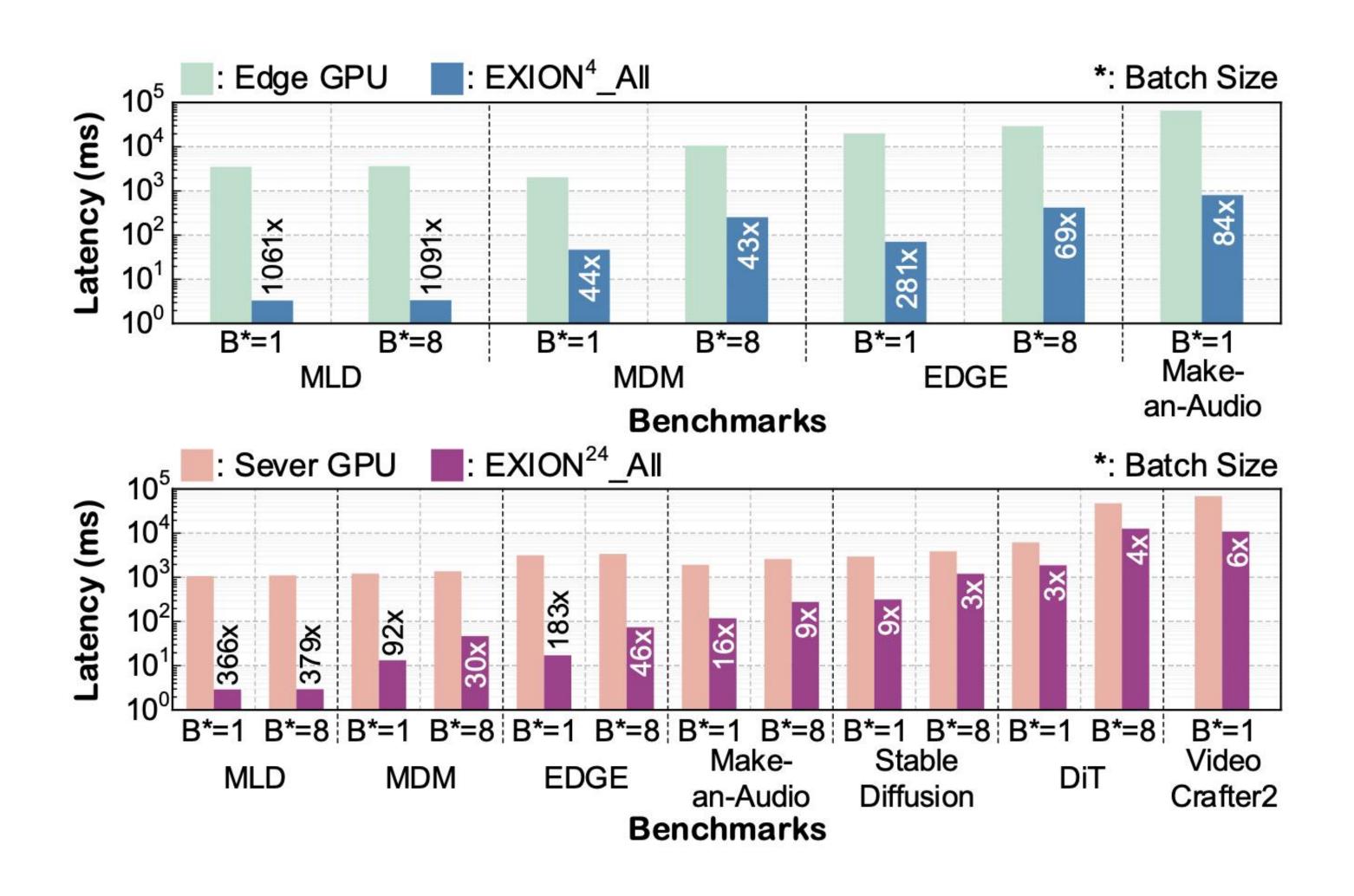
^{1: #} of sparse iterations between two dense iterations, 2: EP w/ TS LOD, 3: Threshold for the difference between the largest value and the 2nd largest value, 4: Top-k selection ratio (i.e., k=0.5 selects 50% of the data), 5: Ground truth, 6: Compute PSNR compared to the vanilla model, 7: After post-training quantization (INT mixed precision, 12b for SDUE/EPRE and 16/32b for CFSE)

Performance Evaluation: Energy efficiency





Performance Evaluation: Latency



Thanks!

Q&A

Previous Solutions

Software-based approaches

Reduce the large number of iterations (inference steps), e.g. distillation; Cache and reuse block results;

• Problems: harms accuracy; some of them even require retraining

Hardware accelerators

In each iteration: optimizing QKV projection and attention computation

• Problems: no significantly energy&latency reduce of the overall diffusion