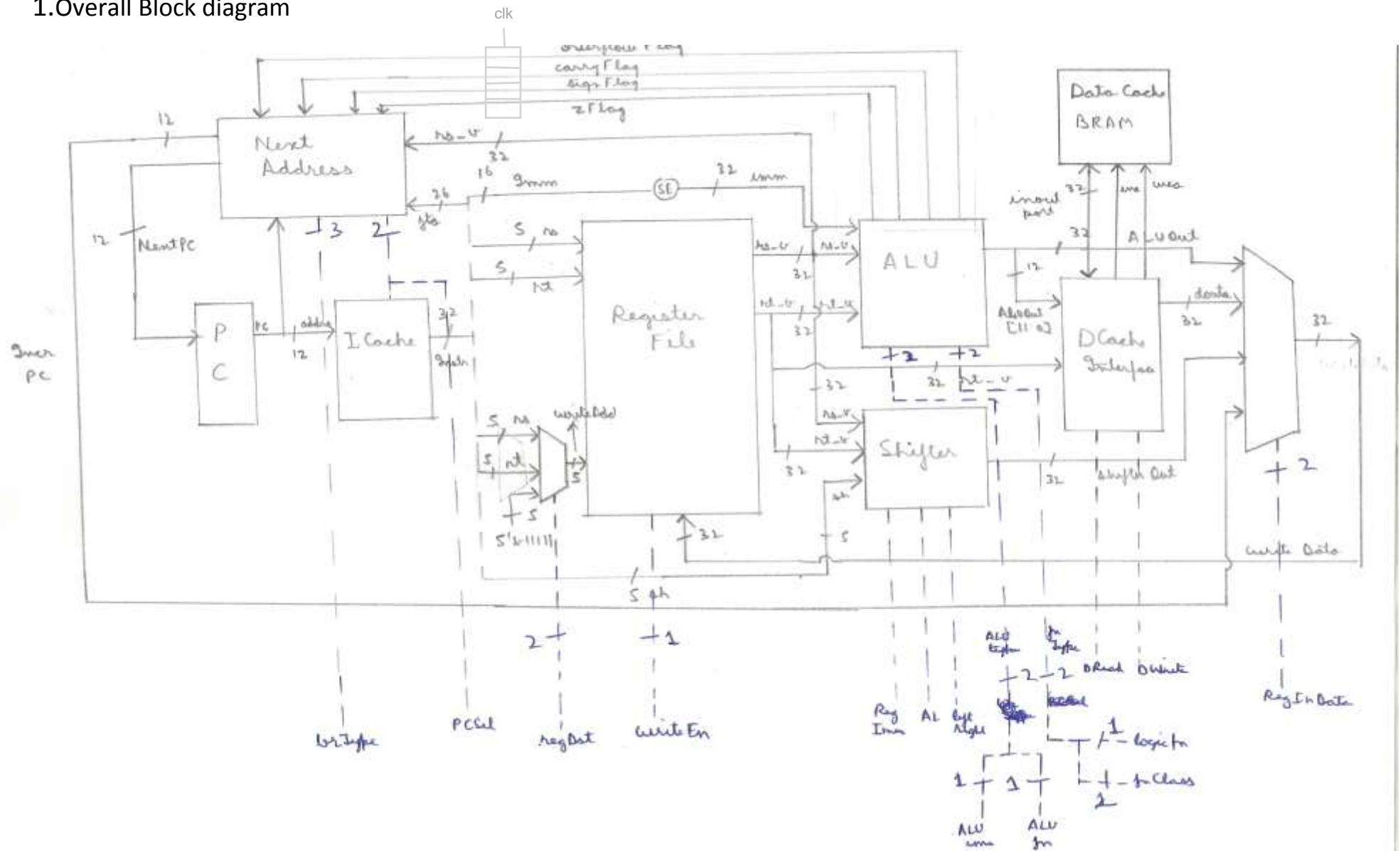
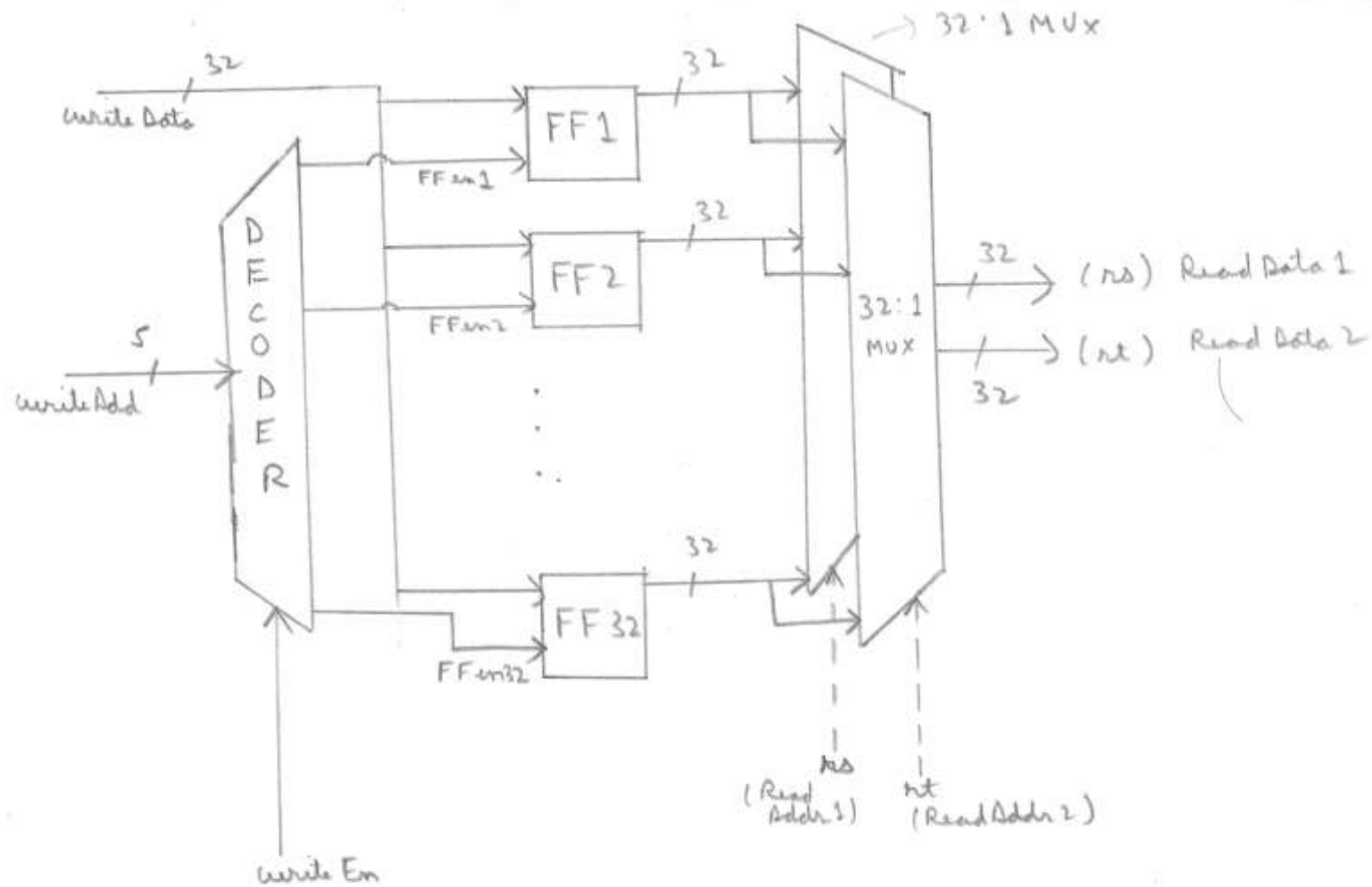


Schematic Diagrams of various blocks of the architecture

1.Overall Block diagram

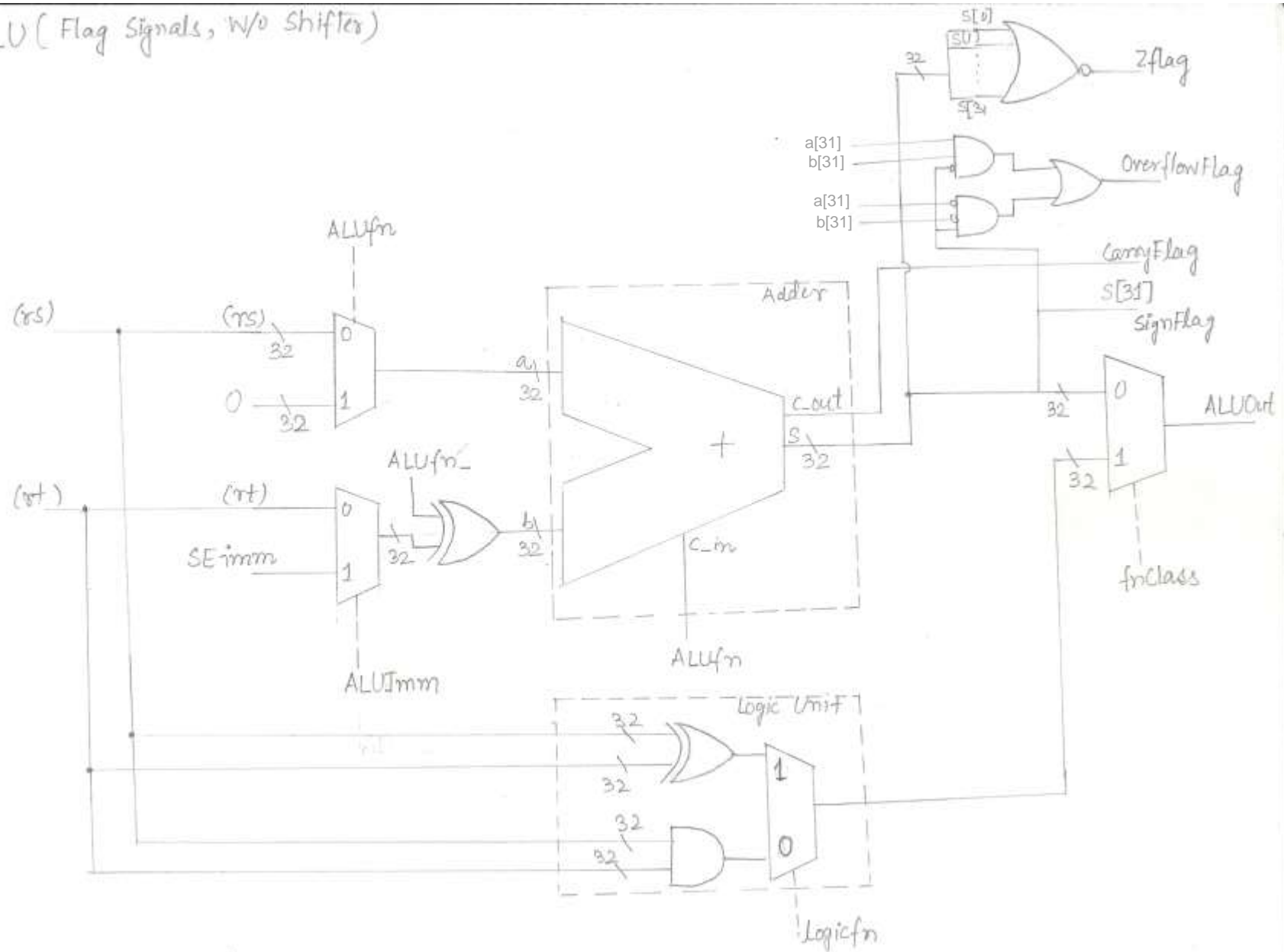


2. Register File

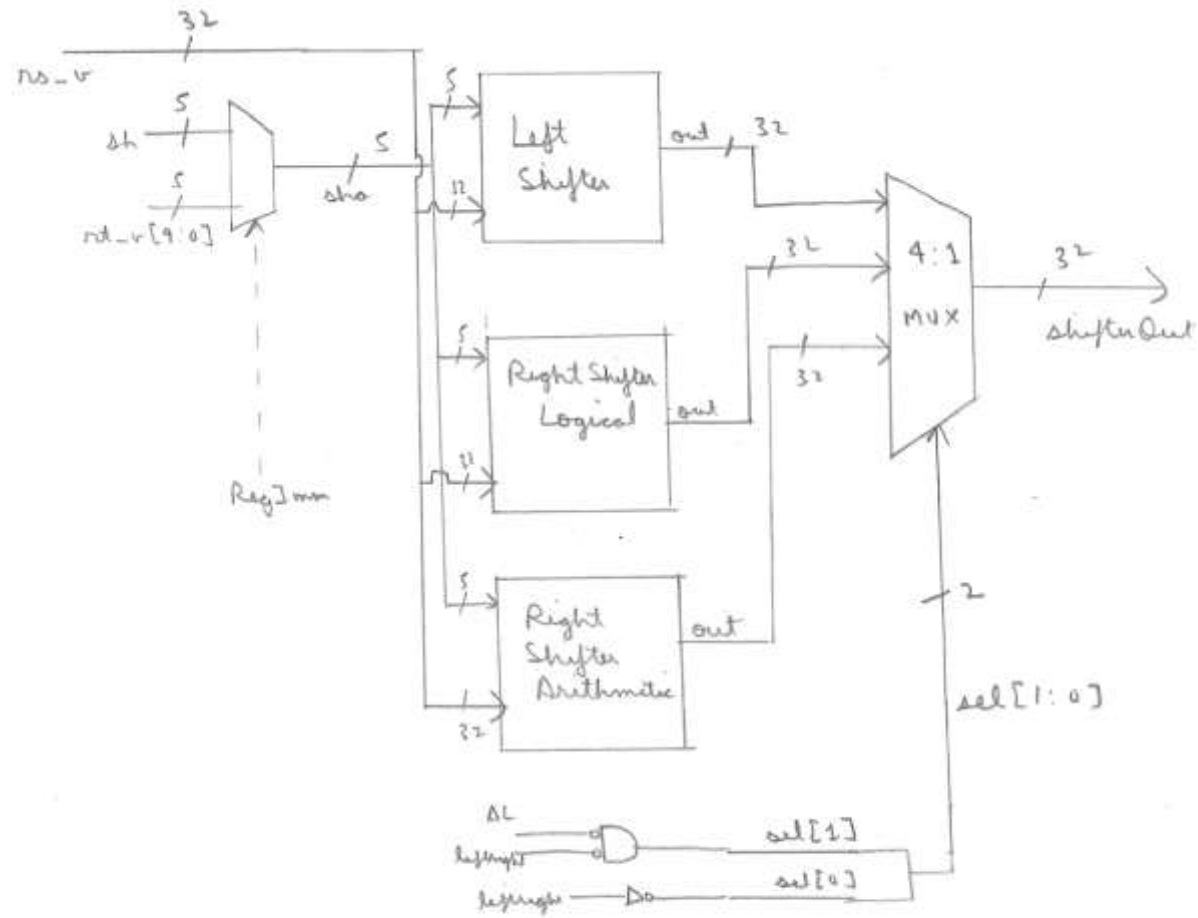


3. ALU (Without shifter)

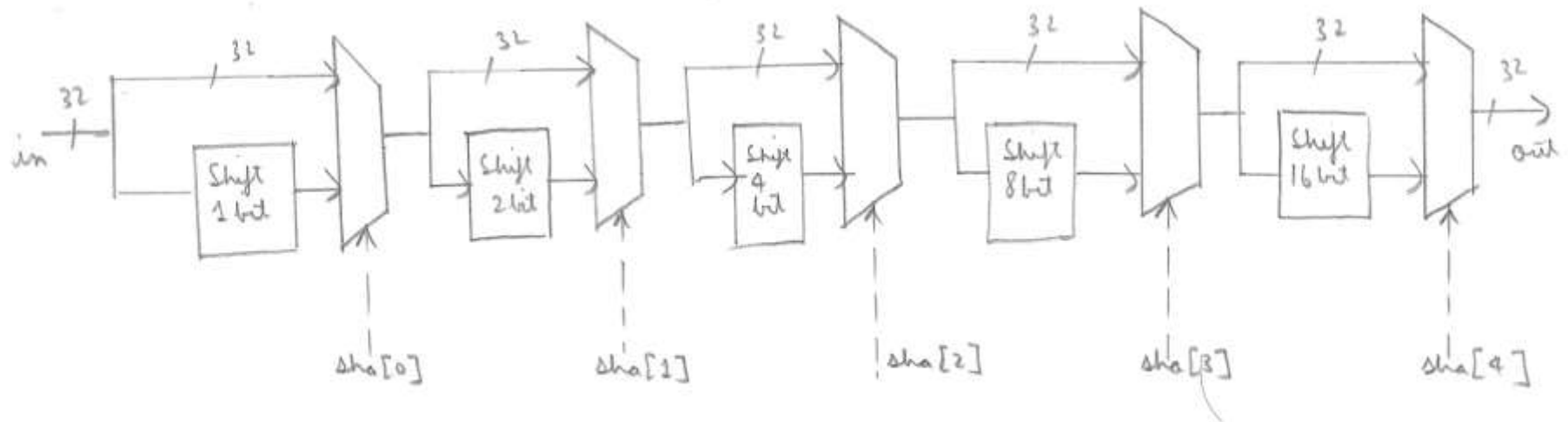
ALU (Flag Signals, w/o Shifter)



4. Shifter



Shifter
(Detailed diagram (~~see~~ schematic) of left shifter in next page)



For left shifter inside "Shift k bit"



$$\begin{aligned} \text{out}[k-1:0] &= 0 \\ \text{out}[31:k] &= \text{in}[31-k:0] \end{aligned}$$

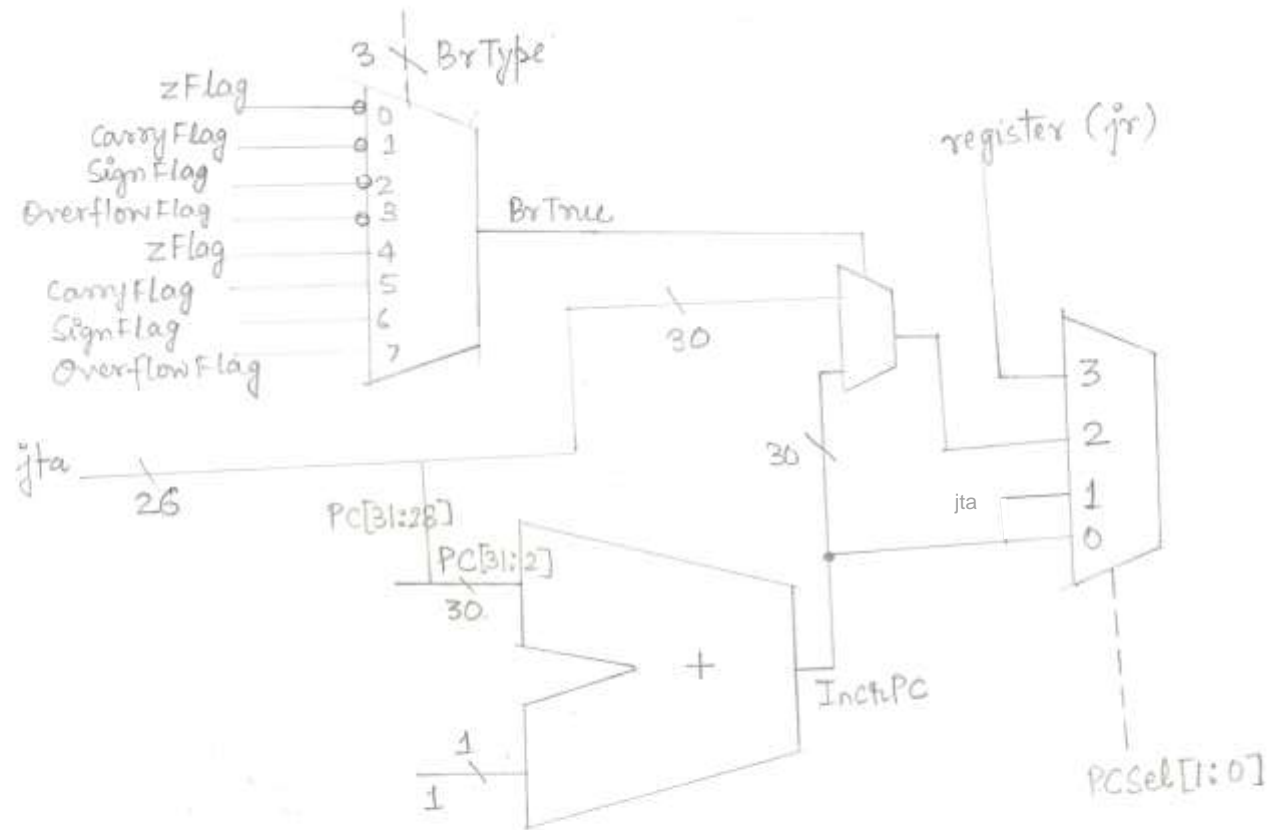
For right shifter logical inside "Shift k bit"

$$\begin{aligned} \text{out}[31-k:0] &= \text{in}[31:k] \\ \text{out}[31:31-k+1] &= 0 \end{aligned}$$

" " arith. inside "Shift k bit"

$$\begin{aligned} \text{out}[31-k:0] &= \text{in}[31:k] \\ \text{each bit from out}[31] \text{ to out}[31-k+1] \\ &\text{become in}[31] \end{aligned}$$

5. Next Address



Next Address