Lab 06

Lab	**:**	**06**
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Registration Number	**:**	**220689N**
Group No	**:**	**32**

1.0 Introduction

1.1 Lab Task

AU (Arithmetic Unit) is a very important aspect of a processor. It does all the arithmetic operations. In this lab we are going to design a simple AU with,

- A Slow clock
- Two memory registers
- A 4 bit adder

Slow clock, 4 bit adder and memory registers(D flip flops) are designed in previous labs. In this lab, we are creating 1 to 2 Decoder.

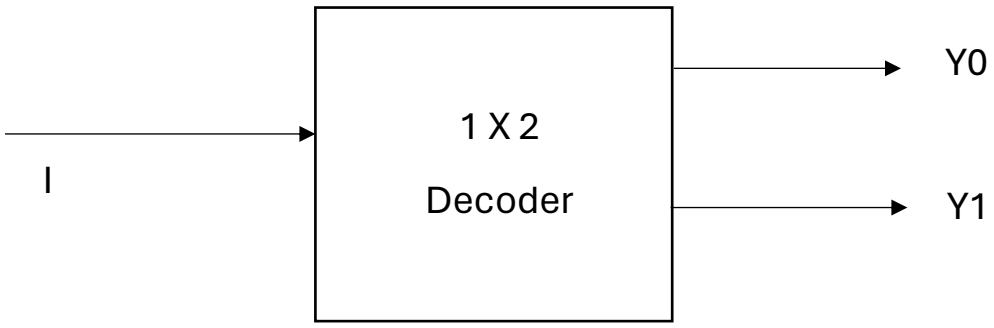
1.2 1 to 2 Decoder Implementation

We are using this decoder to select one of memory register at a time. By controlling one input, It gives us ability to use it as a enabling switch for 2 memories.

Design code and its logic is mentioned in below.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Decorder_1_to_2 is
    Port ( I : in STD_LOGIC;
           EN : in STD_LOGIC;
           Y : out STD_LOGIC_VECTOR (1 downto 0));
end Decorder_1_to_2;

architecture Behavioral of Decorder_1_to_2 is

begin
    Y(0) <= NOT(I) AND EN;
    Y(1) <= I AND EN;
```

```
end Behavioral;
```



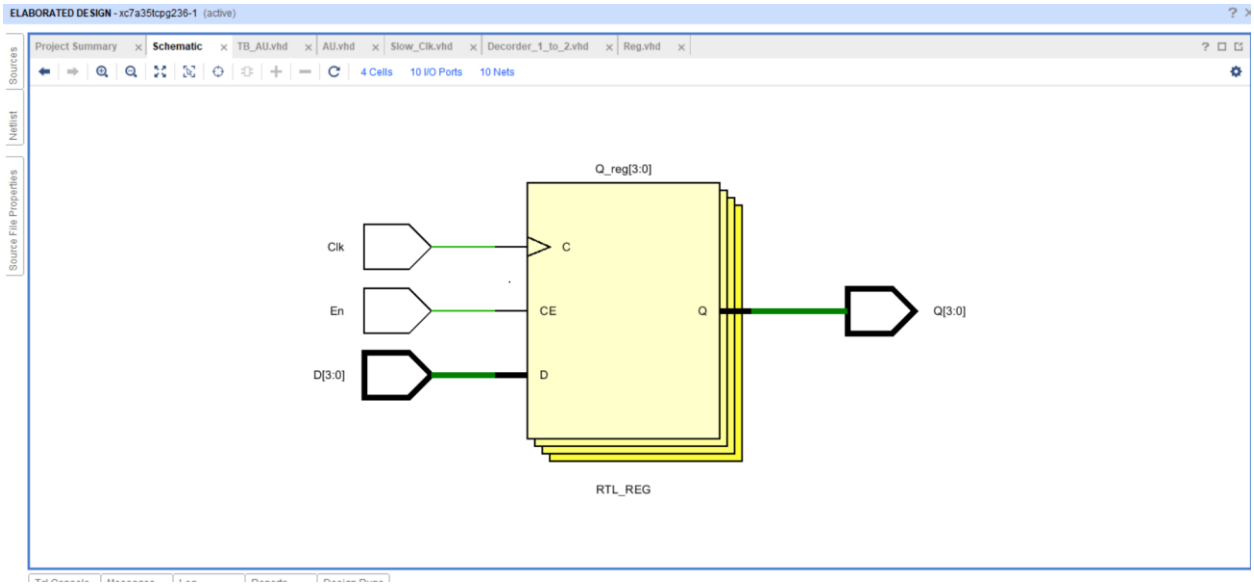
2.0 4 bit Register

2.1 Design Source File

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/12/2024 02:47:05 PM
-- Design Name:
-- Module Name: Reg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Reg is
    Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
           En : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (3 downto 0));
end Reg;

architecture Behavioral of Reg is

begin
    PROCESS (Clk)
        BEGIN
            IF (RISING_EDGE(Clk)) THEN
                IF (EN='1') THEN
                    Q<=D;
                END IF;
            END IF;
    END PROCESS;
end Behavioral;
```

2.2 Elaborated Design Schematic



3.0 Arithmetic Unit

3.1 Design Source File

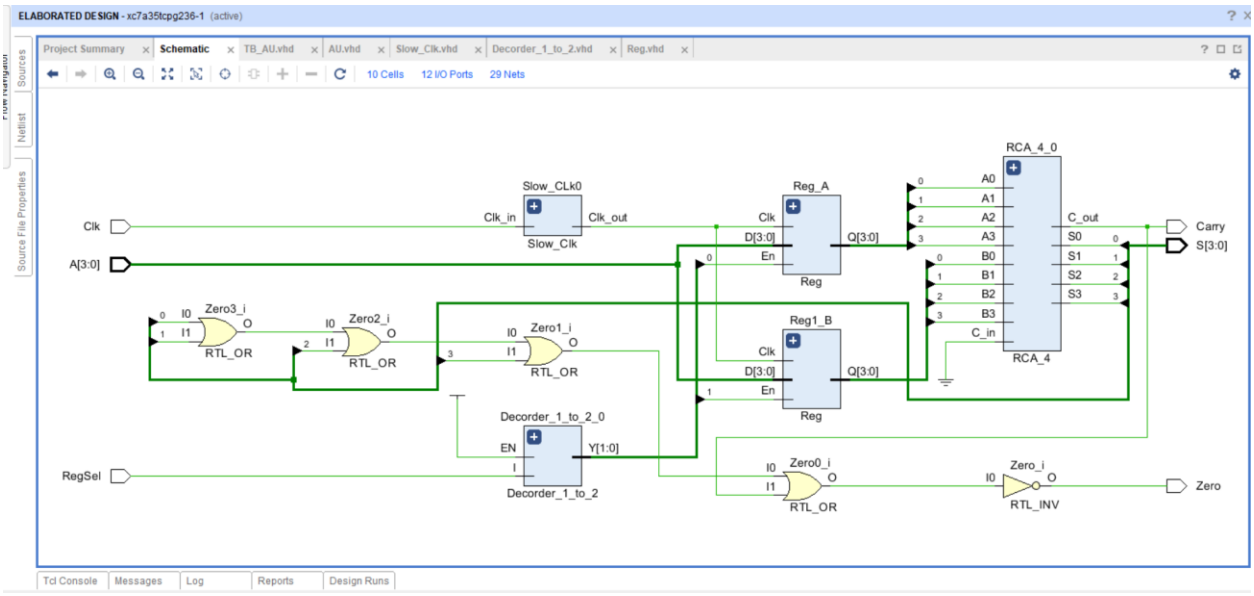
```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/12/2024 03:01:00 PM
-- Design Name:
-- Module Name: AU - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity AU is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           RegSel : in STD_LOGIC;
           Clk : in STD_LOGIC;
           S : out STD_LOGIC_VECTOR (3 downto 0);
           Zero : out STD_LOGIC;
           Carry : out STD_LOGIC);
end AU;

architecture Behavioral of AU is
COMPONENT Slow_Clk
    PORT ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end COMPONENT;
COMPONENT Reg is
    Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
           En : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (3 downto 0));
end COMPONENT;
COMPONENT RCA_4 is
    Port ( A0 : in STD_LOGIC;
           A1 : in STD_LOGIC;
           A2 : in STD_LOGIC;
           A3 : in STD_LOGIC;
           B0 : in STD_LOGIC;
           B1 : in STD_LOGIC;
           B2 : in STD_LOGIC;
           B3 : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S0 : out STD_LOGIC;
```

```
          S1 : out STD_LOGIC;
          S2 : out STD_LOGIC;
          S3 : out STD_LOGIC;
          C_out : out STD_LOGIC);
end COMPONENT;
COMPONENT Decorder_1_to_2 is
    Port ( I : in STD_LOGIC;
          EN : in STD_LOGIC;
          Y : out STD_LOGIC_VECTOR (1 downto 0));
end COMPONENT;

SIGNAL Clk_slow : STD_LOGIC;
SIGNAL In0,In1 : STD_LOGIC_VECTOR (3 DOWNTO 0); -- In0,In1 A inputs
SIGNAL Y : STD_LOGIC_VECTOR (1 DOWNTO 0); --Y Decorder Outputs
SIGNAL s0,s1,s2,s3,c : STD_LOGIC; --Outputs of the adder

begin

    Slow_Clk0 : Slow_Clk
        PORT MAP(
            Clk_in=>Clk,
            Clk_Out=>Clk_slow
        );
    Decorder_1_to_2_0 : Decorder_1_to_2
        PORT MAP(
            I => RegSel,
            EN => '1',
            Y => Y
        );
    Reg_A : Reg
        PORT MAP(
            D => A,
            En => Y(0),
            Clk => Clk_slow,
            Q => In0
        );
    Reg1_B : Reg
        PORT MAP(
            D => A,
            En => Y(1),
            Clk => Clk_slow,
            Q => In1
        );
    RCA_4_0 : RCA_4
        PORT MAP(
```

```
            A0 => In0(0),
            A1 => In0(1),
            A2 => In0(2),
            A3 => In0(3),
            B0 => In1(0),
            B1 => In1(1),
            B2 => In1(2),
            B3 => In1(3),
            C_in => '0',
            S0 => s0,
            S1 => s1,
            S2 => s2,
            S3 => s3,
            C_out => c
        );

    Zero <= NOT(s0 OR s1 OR s2 OR s3 OR c);
    S(0) <= s0;
    S(1) <= s1;
    S(2) <= s2;
    S(3) <= s3;
    Carry <= c;

end Behavioral;
```

3.2 Elaborated Design Schematic



3.3 Simulation Source File

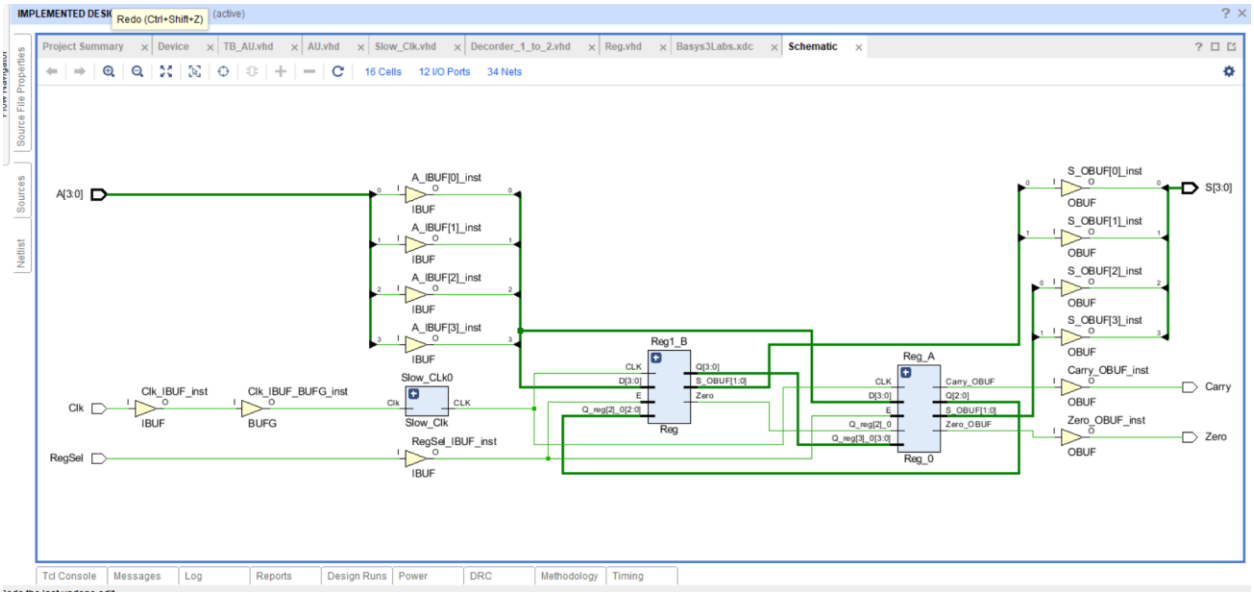
```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/12/2024 04:04:51 PM
-- Design Name:
-- Module Name: TB_AU - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_AU is
--  Port ( );
end TB_AU;

architecture Behavioral of TB_AU is
COMPONENT AU is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
```

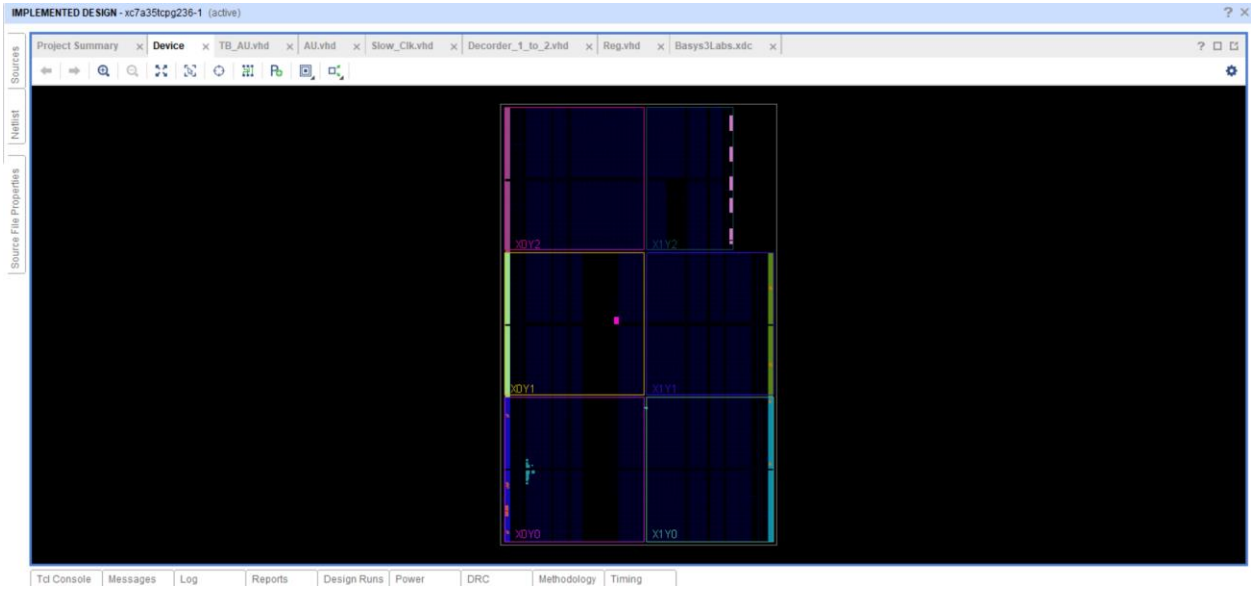
```
          RegSel : in STD_LOGIC;
          Clk : in STD_LOGIC;
          S : out STD_LOGIC_VECTOR (3 downto 0);
          Zero : out STD_LOGIC;
          Carry : out STD_LOGIC);
end COMPONENT;
SIGNAL Clk,Zero,Carry,RegSel : STD_LOGIC;
SIGNAL A,S : STD_LOGIC_VECTOR (3 DOWNTO 0);
begin
    UUT : AU
        PORT MAP(
            A => A,
            RegSel => RegSel,
            Clk => Clk,
            S => S,
            Zero => Zero,
            Carry => Carry
        );
    Clk1 : PROCESS
        BEGIN
            Clk <= '0';WAIT FOR 10 NS;
            CLK <= '1';WAIT FOR 10 NS;
    END PROCESS;
    PROCESS
        BEGIN
            --bin(220689)
            --'0b11 0101 1110 0001 0001'
            --0001
            A <= "0001";
            RegSel <= '0'; WAIT FOR 50 NS;
            RegSel <= '1'; WAIT FOR 50 NS;

            --1110
            A <= "1110";
            RegSel <= '0'; WAIT FOR 50 NS;
            RegSel <= '1'; WAIT FOR 50 NS;

            --0101
            A <= "0101";
            RegSel <= '0'; WAIT FOR 50 NS;
            RegSel <= '1'; WAIT FOR 50 NS;

            --0001
            A <= "1111";
            RegSel <= '0'; WAIT FOR 50 NS;
```

```
            RegSel <= '1'; WAIT FOR 50 NS;

            --0000
            A <= "0000";
            RegSel <= '0'; WAIT FOR 50 NS;
            RegSel <= '1'; WAIT FOR 50 NS;
    END PROCESS;



end Behavioral;
```

3.4 Timing Diagram

3.5 Implemented Design Schematic





3.6 Constraints File

```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports Clk]
    set_property IOSTANDARD LVCMOS33 [get_ports Clk]
    create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports
Clk]

## Switches
set_property PACKAGE_PIN V17 [get_ports {A[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
```

```
set_property PACKAGE_PIN V16 [get_ports {A[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
set_property PACKAGE_PIN W16 [get_ports {A[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
set_property PACKAGE_PIN W17 [get_ports {A[3]}]
      set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
set_property PACKAGE_PIN R2 [get_ports {RegSel}]
    set_property IOSTANDARD LVCMOS33 [get_ports {RegSel}]


## LEDs
set_property PACKAGE_PIN U16 [get_ports {S[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S[0]}]
set_property PACKAGE_PIN E19 [get_ports {S[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S[1]}]
set_property PACKAGE_PIN U19 [get_ports {S[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S[2]}]
set_property PACKAGE_PIN V19 [get_ports {S[3]}]
      set_property IOSTANDARD LVCMOS33 [get_ports {S[3]}]
set_property PACKAGE_PIN P1 [get_ports {Carry}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Carry}]
set_property PACKAGE_PIN L1 [get_ports {Zero}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Zero}]
```

4.0 Conclusion

In this lab we have designed and implemented simple AU including 2 registers, a 1 to 2 decoder, a slow clock and a 4-bit adder. In order to build a nano processor we can assemble part by part together like this AU.