Lab 07

Lab : **07**

Name : **MKSL Weerasiri**

Registration Number : **220689N**

Group No : **32**

1.0 Introduction

1.1 Lab Task

In this lab, we are going to design and implement a 7–segment display. The 7 – Segment Display is a very basic display that has 7 segments to display a given value such as integers or some English letters. This lab is to connect it to our AU (Result of Lab 6) and display our AU results through it using a lookup table instead of using a logic function. Lookup table is a simple ROM, that is used to store and retrieve desired output without logic functions, just by looking at data in the memory.

1.2 Completed Table of Segments to Switch On

7 - Segment Display type in Basys3 board: common anode

Output from RCA					Segments to Switch On						
S3	S2	S1	S0	Hex.	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	1	0	0	1	1	1	1
0	0	1	0	2	0	0	1	0	0	1	0
0	0	1	1	3	0	0	0	0	1	1	0
0	1	0	0	4	1	0	0	1	1	0	0
0	1	0	1	5	0	1	0	0	1	0	0
0	1	1	0	6	0	1	0	0	0	0	0
0	1	1	1	7	0	0	0	1	1	1	1
1	0	0	0	8	0	0	0	0	0	0	0
1	0	0	1	9	0	0	0	0	1	0	0
1	0	1	0	A	0	0	0	1	0	0	0
1	0	1	1	B	1	1	0	0	0	0	0
1	1	0	0	C	0	1	1	0	0	0	1
1	1	0	1	D	1	0	0	0	0	1	0
1	1	1	0	E	0	1	1	0	0	0	0
1	1	1	1	F	0	1	1	1	0	0	0

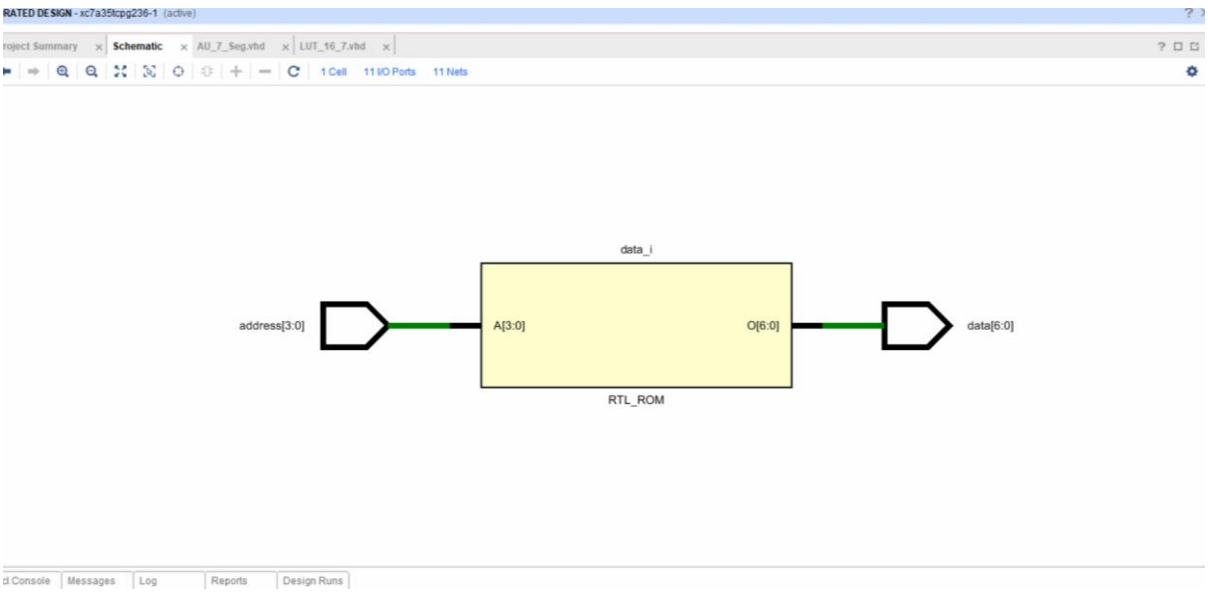
2.0 Lookup Table

2.1 Design Source File

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/19/2024 01:09:33 PM
-- Design Name:
-- Module Name: LUT_16_7 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity LUT_16_7 is
    Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
           data : out STD_LOGIC_VECTOR (6 downto 0));
end LUT_16_7;

architecture Behavioral of LUT_16_7 is
```

```
TYPE rom_type IS ARRAY (0 TO 15) OF STD_LOGIC_VECTOR (6 DOWNTO 0);
SIGNAL sevenSegment_ROM : rom_type := (
    "1000000",--0
    "1111001",--1
    "0100100",--2
    "0110000",--3
    "0011001",--4
    "0010010",--5
    "0000010",--6
    "1111000",--7
    "0000000",--8
    "0010000",--9
    "0001000",--A
    "0000011",--B
    "1000110",--C
    "0100001",--D
    "0000110",--E
    "0001110"--F
    );

begin
    data <= sevenSegment_ROM (TO_INTEGER(UNSIGNED(address)));
end Behavioral;
```

2.2 Elaborated Design Schematic

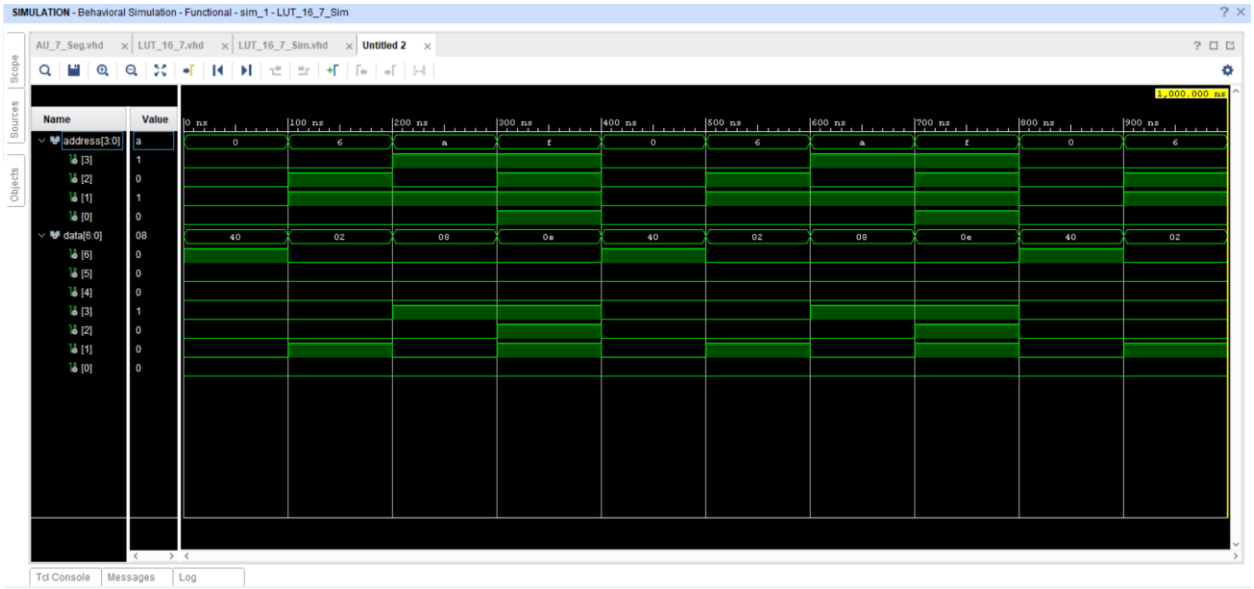


2.3 Simulation Source file

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/19/2024 01:28:00 PM
-- Design Name:
-- Module Name: LUT_16_7_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity LUT_16_7_Sim is
--  Port ( );
end LUT_16_7_Sim;

architecture Behavioral of LUT_16_7_Sim is
COMPONENT LUT_16_7
    Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
           data : out STD_LOGIC_VECTOR (6 downto 0));
END COMPONENT;
```

```
SIGNAL address : STD_LOGIC_VECTOR (3 DOWNTO 0);
SIGNAL data : STD_LOGIC_VECTOR (6 DOWNTO 0);
begin
    UUT : LUT_16_7
        PORT MAP(
            address => address,
            data => data
        );
    PROCESS
        BEGIN
            address <= "0000";WAIT FOR 100 NS;
            address <= "0110";WAIT FOR 100 NS;
            address <= "1010";WAIT FOR 100 NS;
            address <= "1111";WAIT FOR 100 NS;
    END PROCESS;

end Behavioral;
```

2.4 Timing Diagram



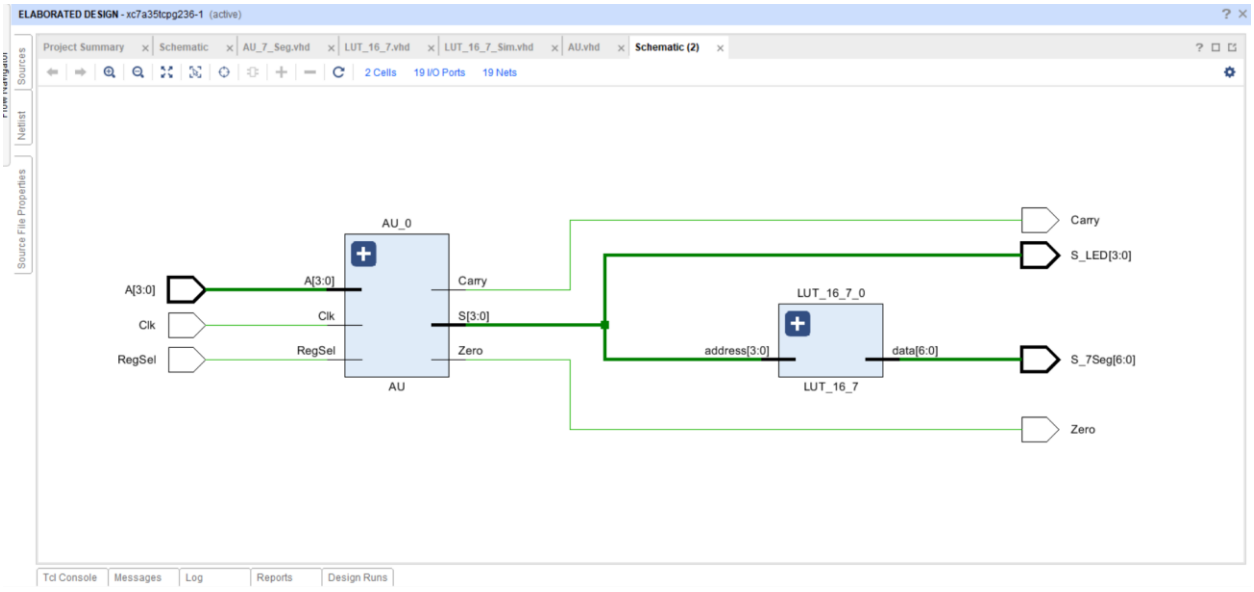
3.0 7 Segment Display

3.1 Design Source File

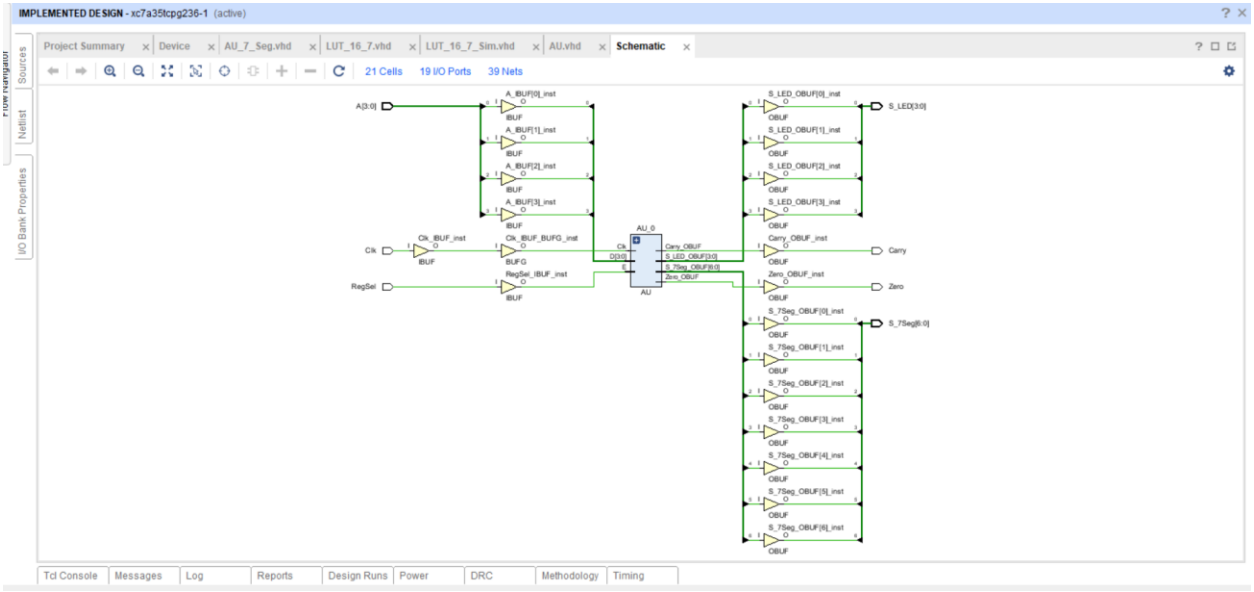
```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/19/2024 01:40:25 PM
-- Design Name:
-- Module Name: AU_7_Seg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity AU_7_Seg is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           Clk : in STD_LOGIC;
           RegSel : in STD_LOGIC;
           S_LED : out STD_LOGIC_VECTOR (3 downto 0);
           S_7Seg : out STD_LOGIC_VECTOR (6 downto 0);
           Carry : out STD_LOGIC;
```

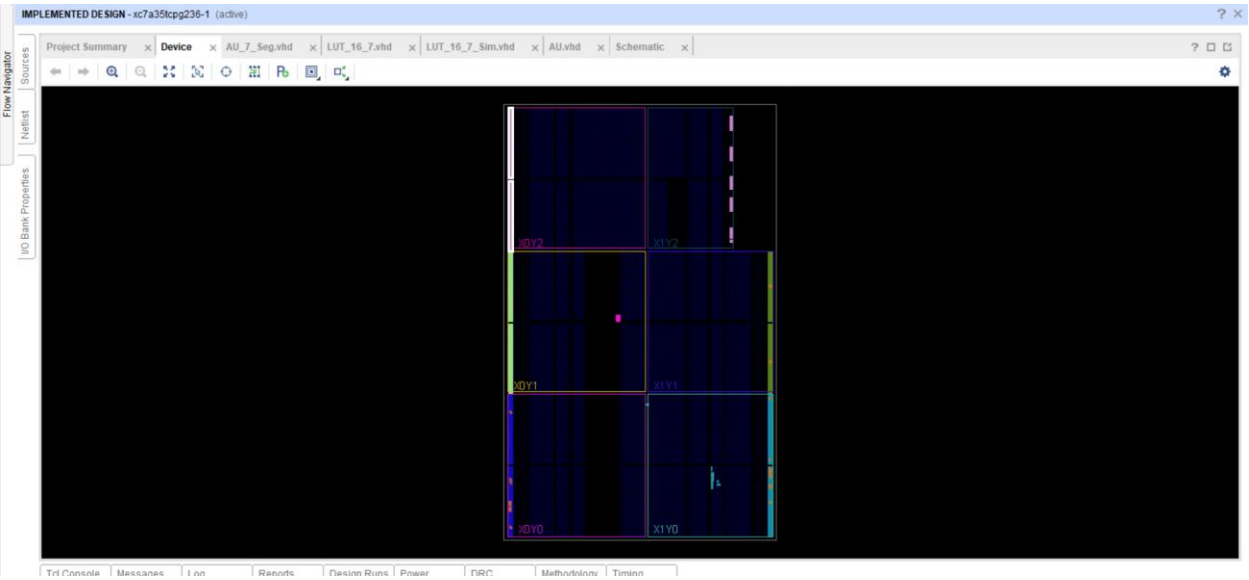
```
           Zero : out STD_LOGIC);
end AU_7_Seg;

architecture Behavioral of AU_7_Seg is
COMPONENT AU
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           RegSel : in STD_LOGIC;
           Clk : in STD_LOGIC;
           S : out STD_LOGIC_VECTOR (3 downto 0);
           Zero : out STD_LOGIC;
           Carry : out STD_LOGIC);
END COMPONENT;
COMPONENT LUT_16_7
    Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
           data : out STD_LOGIC_VECTOR (6 downto 0));
END COMPONENT;
SIGNAL S_adder : STD_LOGIC_VECTOR (3 DOWNTO 0);
begin
    AU_0 : AU
        PORT MAP(
            A => A,
            RegSel => RegSel,
            Clk => Clk,
            S => S_adder,
            Carry => Carry,
            Zero => Zero
        );
    LUT_16_7_0 : LUT_16_7
        PORT MAP(
            address => S_adder,
            data => S_7Seg
        );
    S_LED <= S_adder;
end Behavioral;
```

3.2 Elaborated Design Schematic



3.3 Implemented Design Schematic





3.4 Constraints File

```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports Clk]
    set_property IOSTANDARD LVCMOS33 [get_ports Clk]
    create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports
Clk]

## Switches
set_property PACKAGE_PIN V17 [get_ports {A[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
set_property PACKAGE_PIN V16 [get_ports {A[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
set_property PACKAGE_PIN W16 [get_ports {A[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
set_property PACKAGE_PIN W17 [get_ports {A[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
set_property PACKAGE_PIN R2 [get_ports {RegSel}]
    set_property IOSTANDARD LVCMOS33 [get_ports {RegSel}]


## LEDs
set_property PACKAGE_PIN U16 [get_ports {S_LED[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[0]}]
set_property PACKAGE_PIN E19 [get_ports {S_LED[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[1]}]
set_property PACKAGE_PIN U19 [get_ports {S_LED[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[2]}]
```

```
set_property PACKAGE_PIN V19 [get_ports {S_LED[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[3]}]
set_property PACKAGE_PIN P1 [get_ports {Carry}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Carry}]
set_property PACKAGE_PIN L1 [get_ports {Zero}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Zero}]


##7 segment display
set_property PACKAGE_PIN W7 [get_ports {S_7Seg[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[0]}]
set_property PACKAGE_PIN W6 [get_ports {S_7Seg[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[1]}]
set_property PACKAGE_PIN U8 [get_ports {S_7Seg[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[2]}]
set_property PACKAGE_PIN V8 [get_ports {S_7Seg[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[3]}]
set_property PACKAGE_PIN U5 [get_ports {S_7Seg[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[4]}]
set_property PACKAGE_PIN V5 [get_ports {S_7Seg[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[5]}]
set_property PACKAGE_PIN U7 [get_ports {S_7Seg[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[6]}]
```

4.0 Conclusion

In this lab, we have designed and implemented a simple display called a 7-segment display and checked it using our AU. And, to do that we have implemented a simple ROM to map our AU's outputs to 7-segment display inputs.