Lab 5 (Multiplier)

> Lab : 5 (Multiplier)
> Student Name : M.K.S.L. Weerasiri
> Registration No. : 220689N
> Group No. : 32

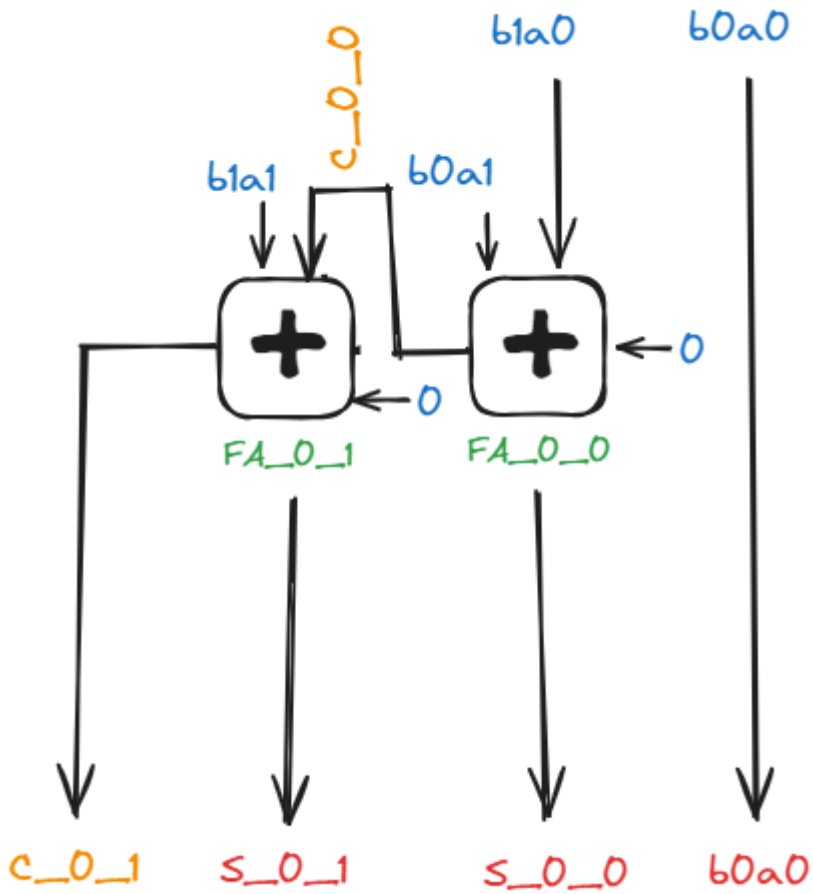
1.0 Introduction

> Multiplier is an essential component in ***ALU***. When we have to multiply we can't use *Full Adders* again and again to multiply through additions. Because it will be reduced the performance of our ***CPU***. To avoid this situation we are going to build several kind of ***Multipliers***.

In this lab,

- We are going to design and implement ***2x2 Multiplier*** with ***Full Adders***
- After that we are going to design and implement ***4x4 Multiplier*** with ***Full Adders***

2.0 2x2 Multiplier



Design Source File

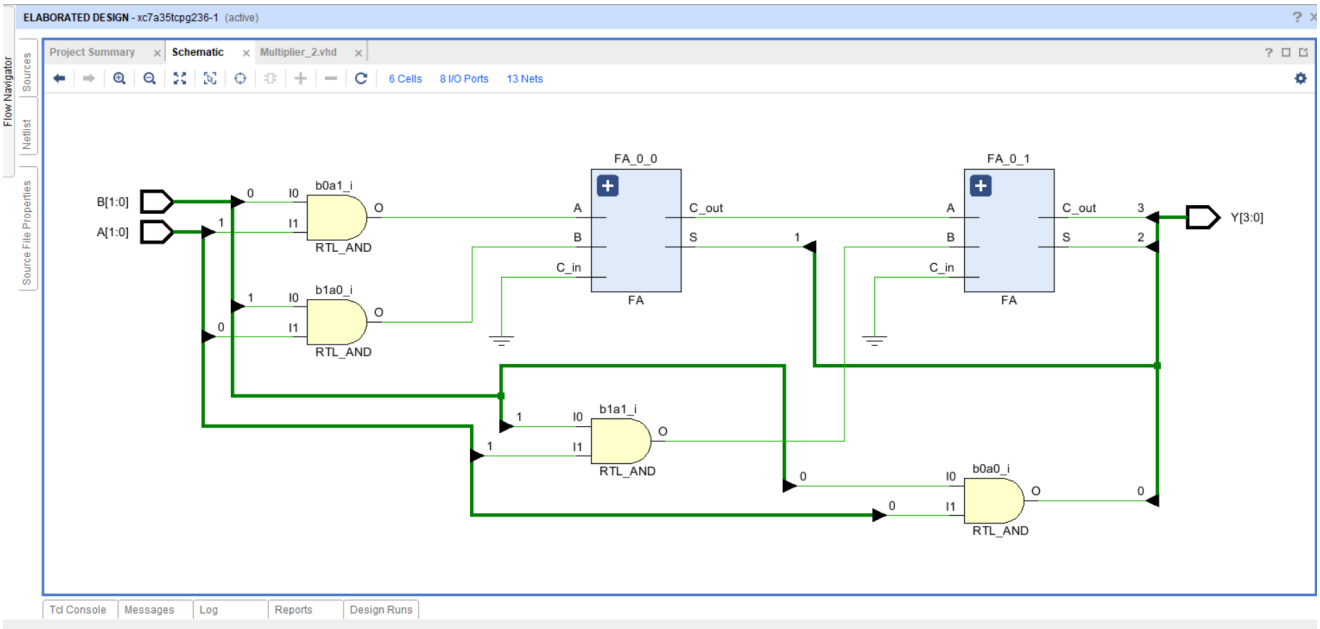
Multiplier_2.vhd

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 02/27/2024 02:11:55 PM
-- Design Name:
-- Module Name: Multiplier_2 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
```

```
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Multiplier_2 is
    Port ( A : in STD_LOGIC_VECTOR (1 downto 0);
           B : in STD_LOGIC_VECTOR (1 downto 0);
           Y : out STD_LOGIC_VECTOR (3 downto 0));
end Multiplier_2;

architecture Behavioral of Multiplier_2 is
COMPONENT FA is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S : out STD_LOGIC;
           C_out : out STD_LOGIC);
end COMPONENT;
SIGNAL b0a0,b1a0,b0a1,b1a1,c_0_1,c_0_2,s_0_1,s_0_2 : STD_LOGIC;

begin

    b0a0 <= B(0) AND A(0);  b1a0 <= B(1) AND A(0);  b0a1 <= B(0) AND A(1);  b1a1
<= B(1) AND A(1);


    FA_0_0 : FA
        PORT MAP(
            A => b0a1,
            B => b1a0,
            C_in => '0',
            S => s_0_1,
            C_out => c_0_1
        );
    FA_0_1 : FA
        PORT MAP(
            A => c_0_1,
            B => b1a1,
```

```
            C_in => '0',
            S => s_0_2,
            C_out => c_0_2
        );


    Y(0) <= b0a0;    Y(1) <= s_0_1;    Y(2) <= s_0_2;    Y(3) <= c_0_2;


end Behavioral;
```

Elaborated design schematic



Simulation source file

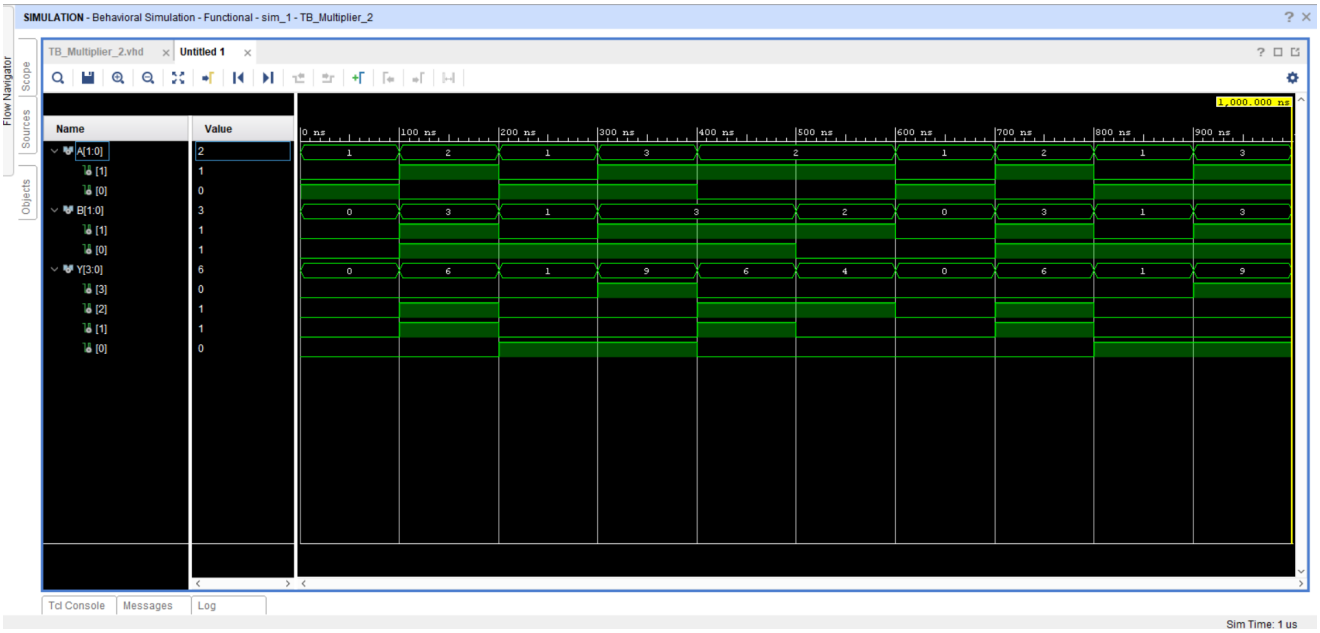
TB_Multiplier_2.vhd

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 02/27/2024 02:32:29 PM
-- Design Name:
-- Module Name: TB_Multiplier_2 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
```

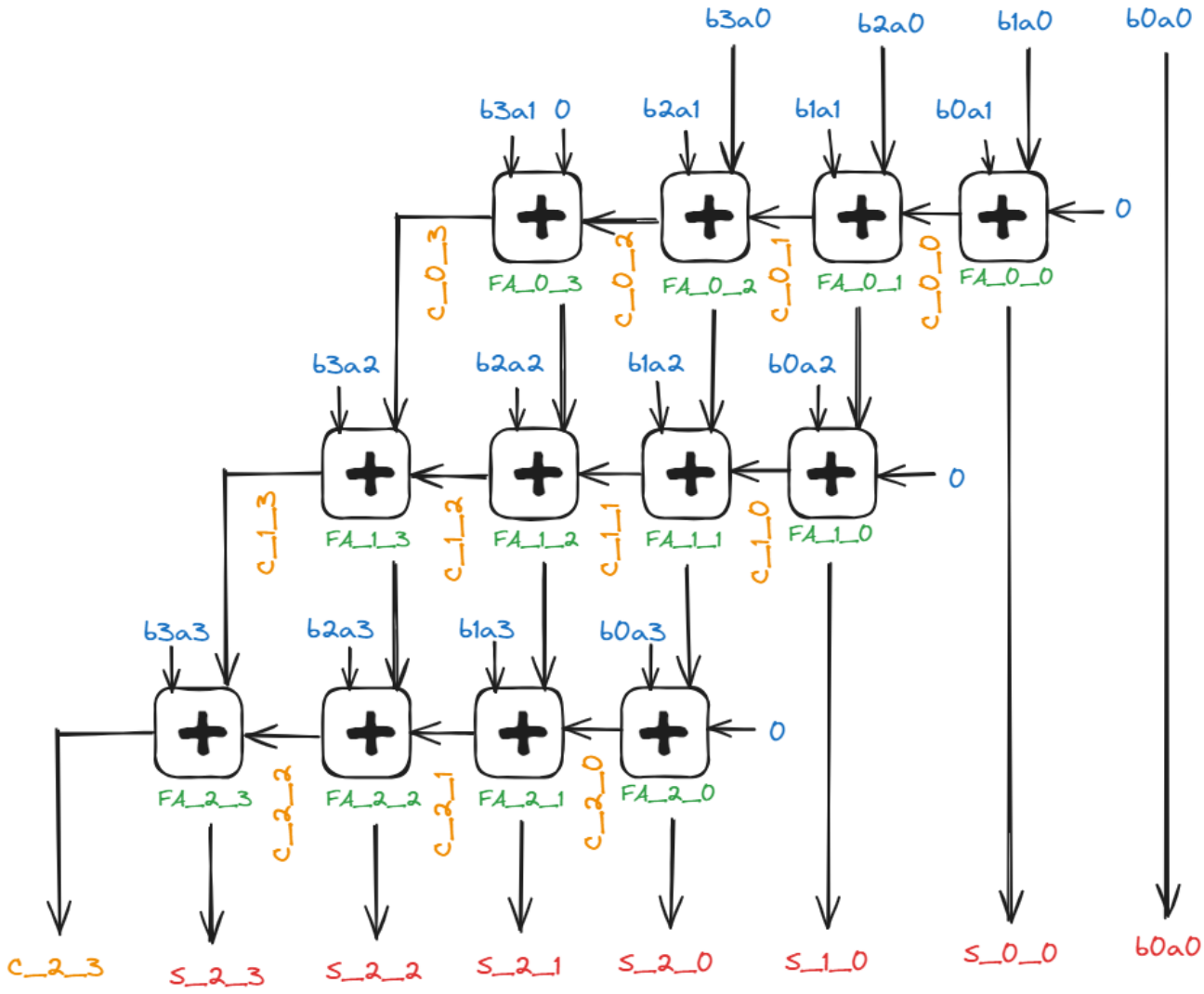
```
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_Multiplier_2 is
--  Port ( );
end TB_Multiplier_2;

architecture Behavioral of TB_Multiplier_2 is
COMPONENT Multiplier_2 is
    Port ( A : in STD_LOGIC_VECTOR (1 downto 0);
           B : in STD_LOGIC_VECTOR (1 downto 0);
           Y : out STD_LOGIC_VECTOR (3 downto 0));
end COMPONENT;

SIGNAL A,B : STD_LOGIC_VECTOR(1 DOWNTO 0);
SIGNAL Y : STD_LOGIC_VECTOR(3 DOWNTO 0);
begin

    UUT : Multiplier_2
        PORT MAP(
            A => A,
            B => B,
            Y => Y
        );

    PROCESS
        BEGIN
            --bin(220689)
```

```
            --'0b 11 | 01 01 | 11 10 | 00 01 | 00 01'
            --00 01
            A<="01";B<="00";WAIT FOR 100 NS;

            --00 01 (Duplicate)
            --A<="01";B<="00";WAIT FOR 100 NS;

            --11 10
            A<="10";B<="11";WAIT FOR 100 NS;

            --01 01
            A<="01";B<="01";WAIT FOR 100 NS;

            --Aditional
            --11 11
            A<="11";B<="11";WAIT FOR 100 NS;

            --10 11
            A<="10";B<="11";WAIT FOR 100 NS;

            --10 10
            A<="10";B<="10";WAIT FOR 100 NS;

    END PROCESS;


end Behavioral;
```

Timing diagram



3.0 4x4 Multiplier



Design Source File

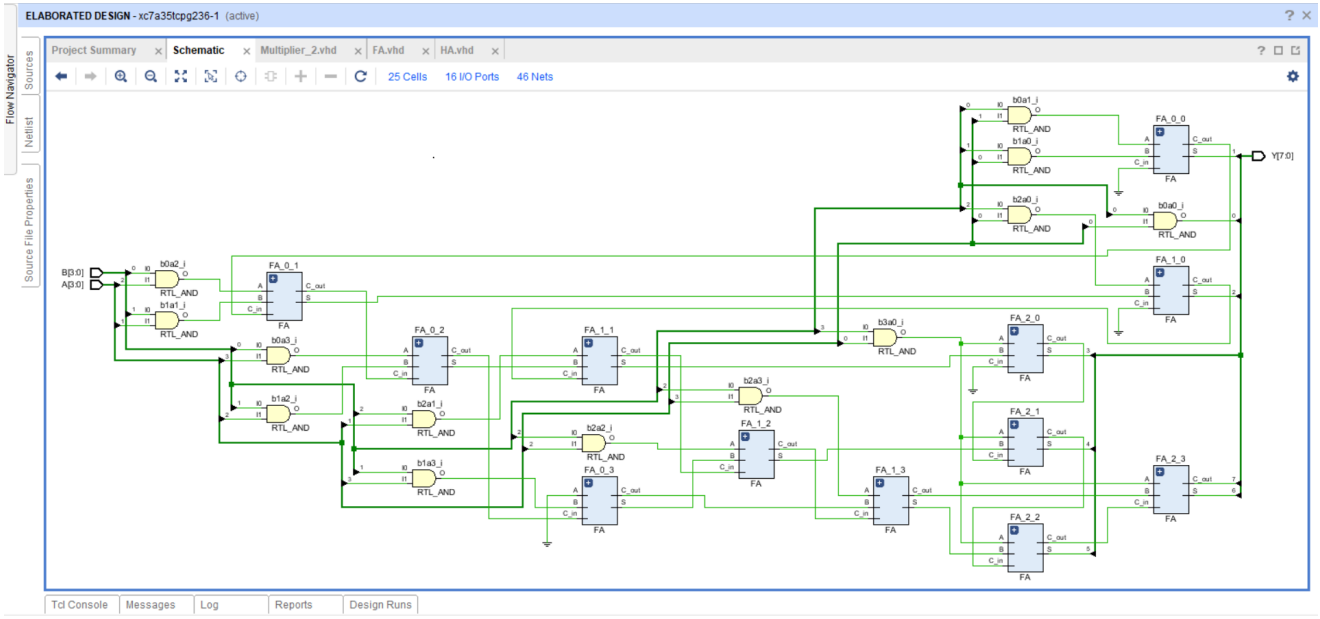
Multiplier_4.vhd

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 02/27/2024 02:59:40 PM
-- Design Name:
-- Module Name: Multiplier_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
```

```
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Multiplier_4 is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           B : in STD_LOGIC_VECTOR (3 downto 0);
           Y : out STD_LOGIC_VECTOR (7 downto 0));
end Multiplier_4;

architecture Behavioral of Multiplier_4 is
COMPONENT FA is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S : out STD_LOGIC;
           C_out : out STD_LOGIC);
end COMPONENT;
SIGNAL
b0a0,b1a0,b2a0,b3a0,b0a1,b1a1,b2a1,b3a1,b0a2,b1a2,b2a2,b3a2,b0a3,b1a3,b2a3,b3a3 :
STD_LOGIC;
SIGNAL s_0_0,s_0_1,s_0_2,s_0_3,s_1_0,s_1_1,s_1_2,s_1_3,s_2_0,s_2_1,s_2_2,s_2_3 :
STD_LOGIC;
SIGNAL c_0_0,c_0_1,c_0_2,c_0_3,c_1_0,c_1_1,c_1_2,c_1_3,c_2_0,c_2_1,c_2_2,c_2_3 :
STD_LOGIC;
begin
    b0a0 <= B(0) AND A(0);  b1a0 <= B(1) AND A(0);  b2a0 <= B(2) AND A(0);  b3a0
<= B(3) AND A(0);
    b0a1 <= B(0) AND A(1);  b1a1 <= B(1) AND A(1);  b2a1 <= B(2) AND A(1);  b3a1
<= B(3) AND A(1);
    b0a2 <= B(0) AND A(2);  b1a2 <= B(1) AND A(2);  b2a2 <= B(2) AND A(2);  b3a2
<= B(3) AND A(2);
    b0a3 <= B(0) AND A(3);  b1a3 <= B(1) AND A(3);  b2a3 <= B(2) AND A(3);  b3a3
```

```
<= B(3) AND A(3);


    FA_0_0 : FA PORT MAP( A => b0a1,    B => b1a0,      C_in => '0',    S =>
s_0_0,    C_out => c_0_0 );
    FA_0_1 : FA PORT MAP( A => b0a2,    B => b1a1,      C_in => c_0_0,    S =>
s_0_1,    C_out => c_0_1 );
    FA_0_2 : FA PORT MAP( A => b0a3,    B => b1a2,      C_in => c_0_1,    S =>
s_0_2,    C_out => c_0_2 );
    FA_0_3 : FA PORT MAP( A => '0',    B => b1a3,      C_in => c_0_2,    S =>
s_0_3,    C_out => c_0_3 );

    FA_1_0 : FA PORT MAP( A => b2a0,    B => s_0_1,      C_in => '0',    S =>
s_1_0,    C_out => c_1_0 );
    FA_1_1 : FA PORT MAP( A => b2a1,    B => s_0_2,      C_in => c_1_0,    S =>
s_1_1,    C_out => c_1_1 );
    FA_1_2 : FA PORT MAP( A => b2a2,    B => s_0_3,      C_in => c_1_1,    S =>
s_1_2,    C_out => c_1_2 );
    FA_1_3 : FA PORT MAP( A => b2a3,    B => c_0_3,      C_in => c_1_2,    S =>
s_1_3,    C_out => c_1_3 );

    FA_2_0 : FA PORT MAP( A => b3a0,    B => s_1_1,      C_in => '0',    S =>
s_2_0,    C_out => c_2_0 );
    FA_2_1 : FA PORT MAP( A => b3a0,    B => s_1_2,      C_in => c_2_0,    S =>
s_2_1,    C_out => c_2_1 );
    FA_2_2 : FA PORT MAP( A => b3a0,    B => s_1_3,      C_in => c_2_1,    S =>
s_2_2,    C_out => c_2_2 );
    FA_2_3 : FA PORT MAP( A => b3a0,    B => c_1_3,      C_in => c_2_2,    S =>
s_2_3,    C_out => c_2_3 );

    Y(0) <= b0a0;
    Y(1) <= s_0_0;
    Y(2) <= s_1_0;
    Y(3) <= s_2_0;
    Y(4) <= s_2_1;
    Y(5) <= s_2_2;
    Y(6) <= s_2_3;
    Y(7) <= c_2_3;

end Behavioral;
```

Elaborated design schematic



Simulation source file

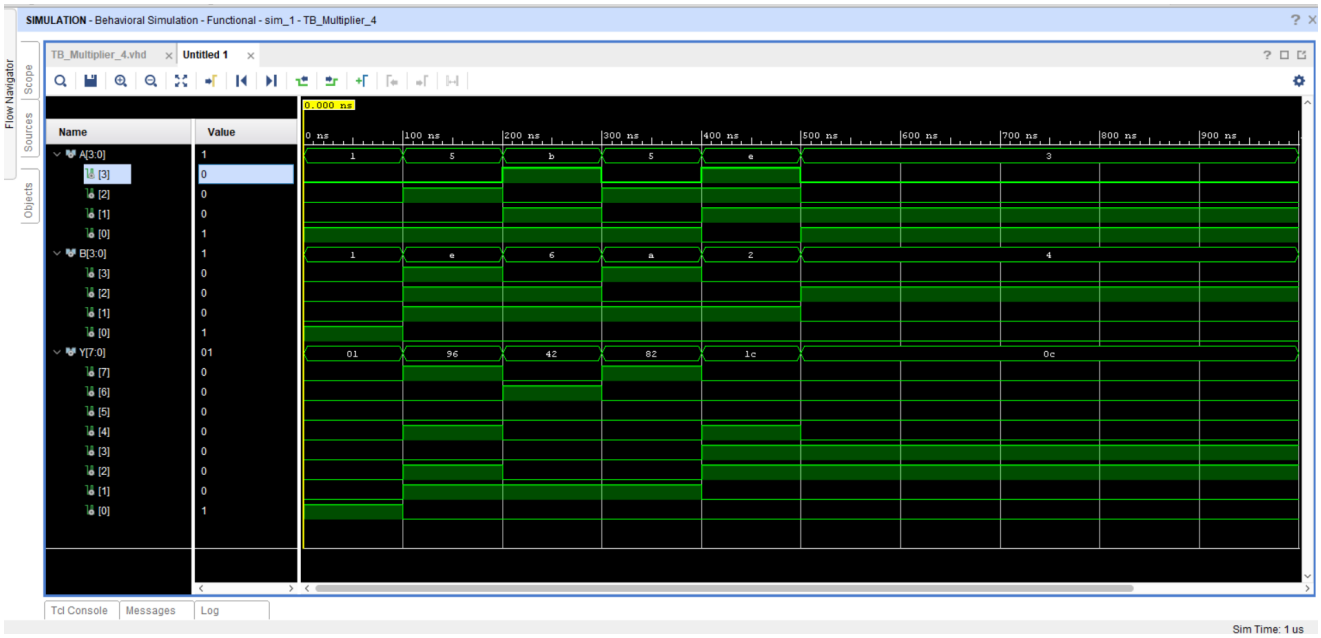
TB_Multiplier_4.vhd

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 02/28/2024 11:55:45 PM
-- Design Name:
-- Module Name: TB_Multiplier_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
```

```
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_Multiplier_4 is
--  Port ( );
end TB_Multiplier_4;

architecture Behavioral of TB_Multiplier_4 is
COMPONENT Multiplier_4 is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           B : in STD_LOGIC_VECTOR (3 downto 0);
           Y : out STD_LOGIC_VECTOR (7 downto 0));
end COMPONENT;

SIGNAL A,B : STD_LOGIC_VECTOR (3 DOWNTO 0);
SIGNAL Y : STD_LOGIC_VECTOR (7 DOWNTO 0);

begin
    UUT : Multiplier_4
        PORT MAP(
            A => A,
            B => B,
            Y => Y
        );

    PROCESS
        BEGIN
            --bin(220689)
            --'0b 11 | 0101 1110 | 0001 0001'
            --0001 0001
            A<="0001";B<="0001";WAIT FOR 100 NS;

            --0101 1110
            A<="0101";B<="1110";WAIT FOR 100 NS;

            --Additional
            --1011 0110
            A<="1011";B<="0110";WAIT FOR 100 NS;

            --0101 1010
            A<="0101";B<="1010";WAIT FOR 100 NS;

            --1110 0010
            A<="1110";B<="0010";WAIT FOR 100 NS;

            --0011 0100
```

```
            A<="0011";B<="0100";WAIT;


    END PROCESS;
end Behavioral;
```

Timing diagram



Additional source files

- *Full Adder*

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 02/13/2024 06:59:40 PM
-- Design Name:
-- Module Name: FA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
```

```
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity FA is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S : out STD_LOGIC;
           C_out : out STD_LOGIC);
end FA;

architecture Behavioral of FA is
COMPONENT HA
    PORT(
        A : IN STD_LOGIC;
        B : IN STD_LOGIC;
        S : OUT STD_LOGIC;
        C : OUT STD_LOGIC
    );
END COMPONENT;

SIGNAL HA0_S, HA0_C, HA1_S, HA1_C : STD_LOGIC;

begin
    HA_0 : HA
        PORT MAP(
            A => A,
            B => B,
            S => HA0_S,
            C => HA0_C
        );
     HA_1 : HA
        PORT MAP(
            A => HA0_S,
            B => C_in,
            S => HA1_S,
```

```
            C => HA1_C
        );

    --S <= A XOR B XOR C_in;
    S <= HA1_S;
    --C_out <= (A AND B) or (C_in and(A XOR B));
    C_out <= HA1_C OR HA0_C;

end Behavioral;
```

- *Half Adder*

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 02/13/2024 06:47:22 PM
-- Design Name:
-- Module Name: HA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity HA is
```

```
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           S : out STD_LOGIC;
           C : out STD_LOGIC);
end HA;

architecture Behavioral of HA is

begin

    S <= A XOR B;
    C <= A AND B;


end Behavioral;
```