- Lab : Lab 5 (D-Flip-Flop, Slow Clock, Counter)
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- Registration Number : 220689N
- Group No : 32

1.0 Introduction

Up to this level, we have designed ***Combinational Logic Circuits***. But in order to build a ***Nano processor*** we need to have a memory. ***The Memory Registers*** contain a bunch of ***Flip Flops*** also known as ***"Sequential Circuits"*** which work with a ***Clock***. So to build a small-scale memory register we have to design and implement those things. So in this lab, we are going to design and implement a clock, a D flip-flop, and a counter (Practical example of a flip-flop).

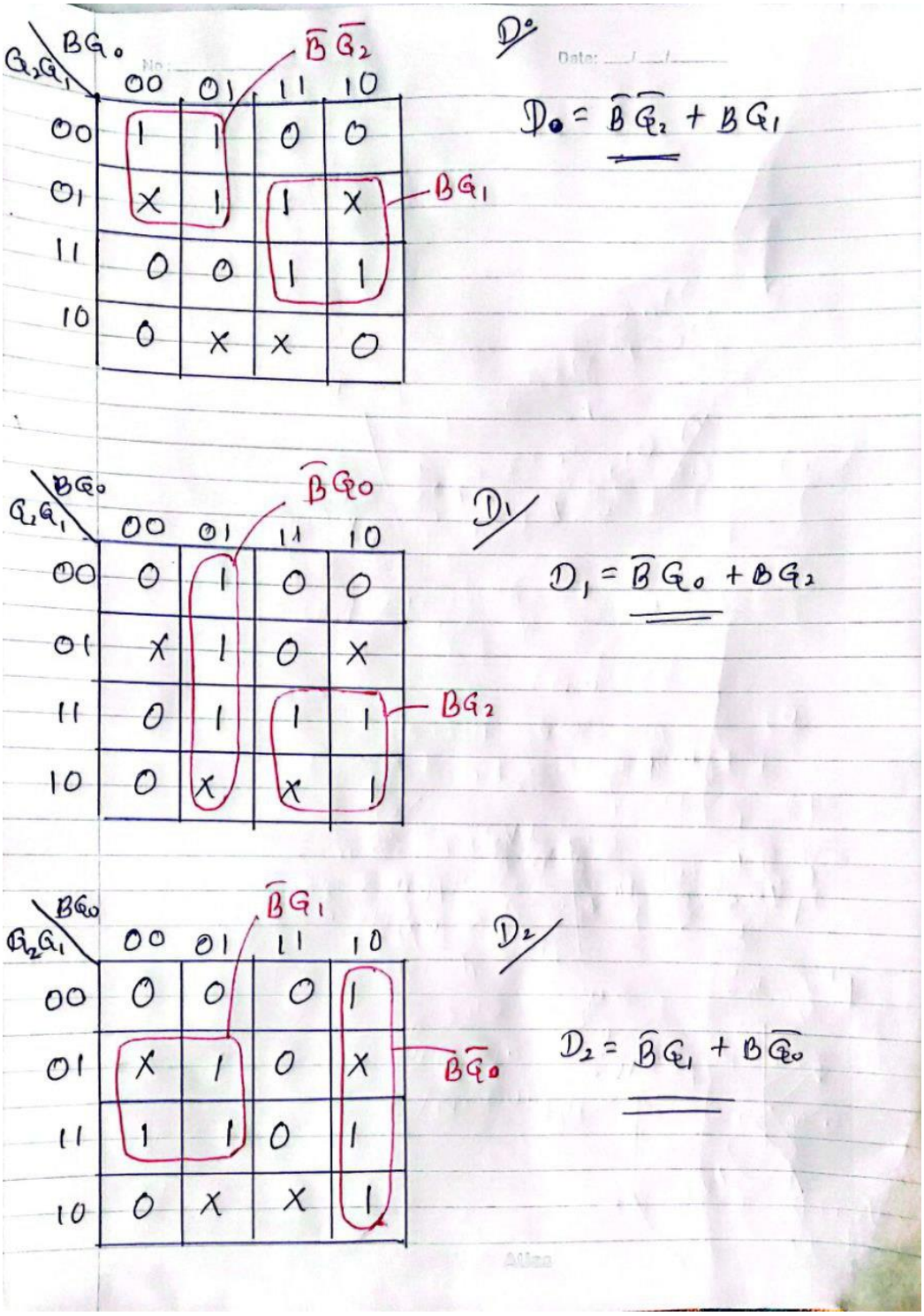
1.0 Lab Task

- Design and Implement a D Flip-Flop
- Design and Implement a Slow Clock
- Design and Implement a Counter for the given pattern using D Flip-flop and the Slow Clock

2.0 Excitation Table

Qt			Button	Qt+1			D2	D1	D0
Q2	Q1	Q0		Q2	Q1	Q0			
0	0	0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	1	0	0
0	0	1	0	0	1	1	0	1	1
0	0	1	1	0	0	0	0	0	0
0	1	0	0	X	X	X	X	X	X
0	1	0	1	X	X	X	X	X	X
0	1	1	0	1	1	1	1	1	1
0	1	1	1	0	0	1	0	0	1
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	1	0
1	0	1	0	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X
1	1	0	0	1	0	0	1	0	0
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	0	1	1	0
1	1	1	1	0	1	1	0	1	1

3.0 K-maps and simplified expressions



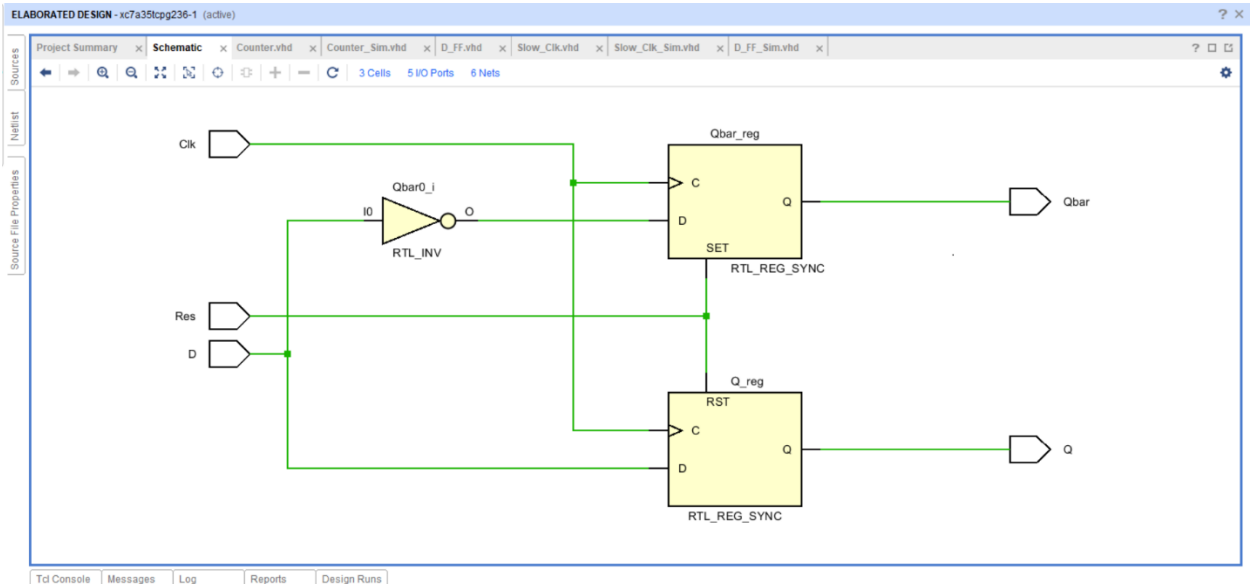
2.0 D Flip-Flop

1.0 Design source file

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/05/2024 02:28:15 PM
-- Design Name:
-- Module Name: D_FF - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity D_FF is
    Port ( D : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC;
           Qbar : out STD_LOGIC);
end D_FF;
```

```
architecture Behavioral of D_FF is

begin
    PROCESS (Clk) BEGIN
        IF (rising_edge(Clk)) THEN
            IF Res = '1' THEN
                Q <= '0';
                Qbar <= '1';
            ELSE
                Q <= D;
                Qbar <= NOT D;
            END IF;
        END IF;
    END PROCESS;

end Behavioral;
```

2.0 Elaborated design schematic



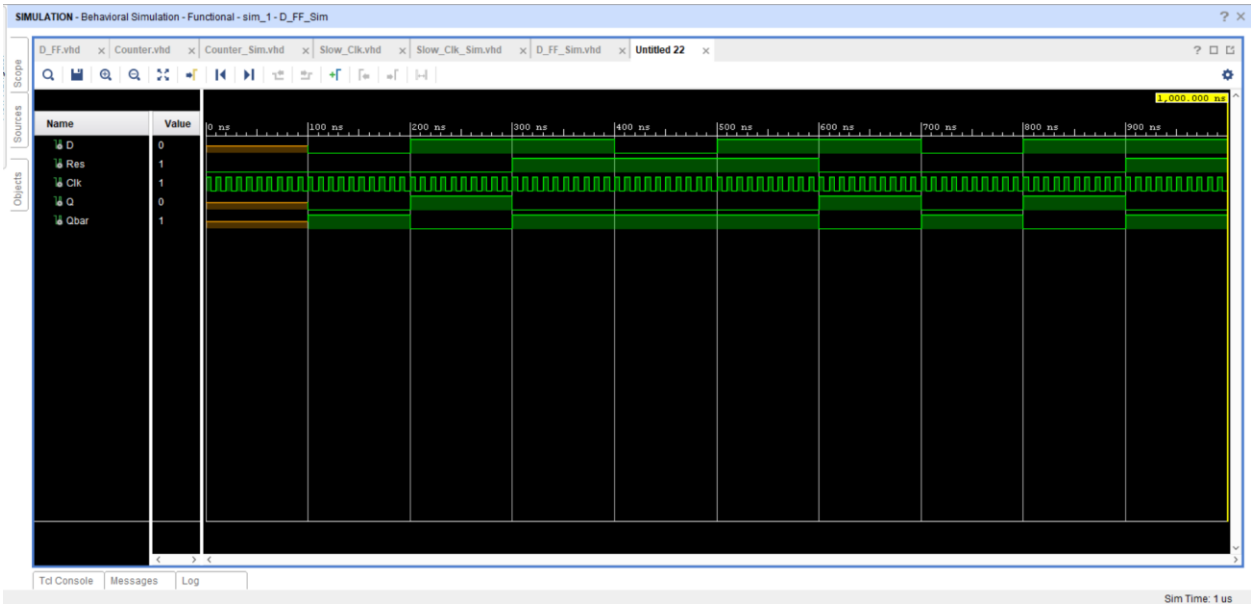
3.0 Simulation source file

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
```

```
-- Create Date: 03/05/2024 02:31:28 PM
-- Design Name:
-- Module Name: D_FF_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity D_FF_Sim is
--  Port ( );
end D_FF_Sim;

architecture Behavioral of D_FF_Sim is
COMPONENT D_FF
    PORT(
        D,Res,Clk : IN STD_LOGIC;
        Q,Qbar : OUT STD_LOGIC
    );
END COMPONENT;
SIGNAL D,Res,Clk,Q,Qbar : STD_LOGIC;
begin
    UUT : D_FF
        PORT MAP(
```

```
            D => D,
            Res => Res,
            Clk => Clk,
            Q => Q,
            Qbar => Qbar
        );

    Clk1 : PROCESS
        BEGIN
            Clk <= '1';WAIT FOR 5 NS;

            Clk <= '0';WAIT FOR 5 NS;

    END PROCESS;
    PROCESS
        BEGIN
            Res <= '0';WAIT FOR 100 NS;
            D <= '0';WAIT FOR 100 NS;

            D <= '1';WAIT FOR 100 NS;


            Res <= '1';WAIT FOR 100 NS;
            D <= '0';WAIT FOR 100 NS;

            D <= '1';WAIT FOR 100 NS;

    END PROCESS;
end Behavioral;
```

4.0 Timing diagram



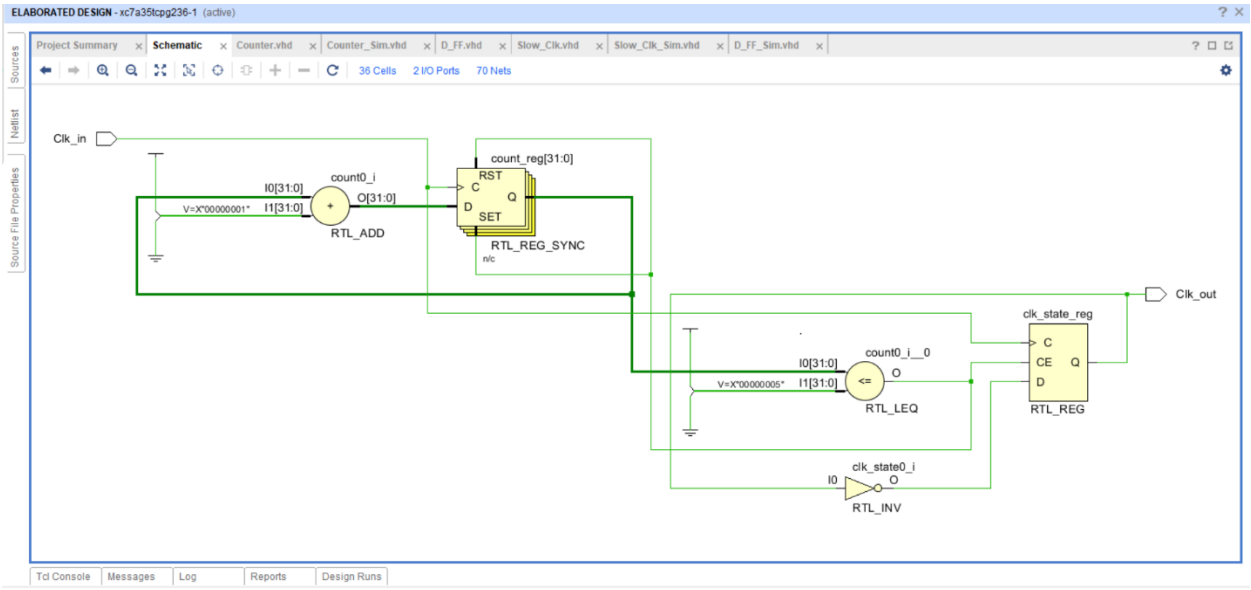
3.0 Slow Clock

1.0 Design source file

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/05/2024 11:44:19 PM
-- Design Name:
-- Module Name: Slow_Clk - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk is
    Port ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is
SIGNAL count : INTEGER := 1;
SIGNAL clk_state : STD_LOGIC := '0';

begin
    PROCESS (Clk_in)
        BEGIN
            IF (rising_edge(Clk_in)) THEN
                count <= count+1;
                IF (count <= 50000000 ) THEN --count 50M pulses (1/2 of period) ;
100 MHz / 2 = 50 MHz
                    clk_state <= NOT clk_state;
                    count <= 1;
                END IF;
            END IF;
            Clk_out <= clk_state;
    END PROCESS;


end Behavioral;
```

2.0 Elaborated design schematic

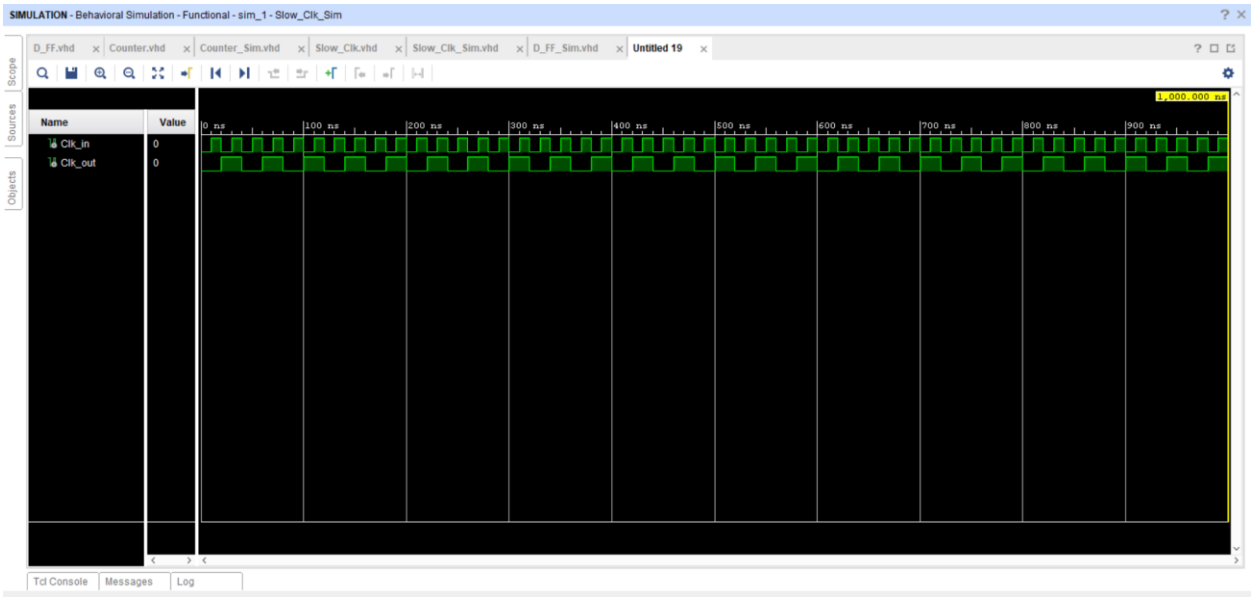


3.0 Simulation source file

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/05/2024 11:56:17 PM
-- Design Name:
-- Module Name: Slow_Clk_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk_Sim is
--  Port ( );
end Slow_Clk_Sim;

architecture Behavioral of Slow_Clk_Sim is
COMPONENT Slow_Clk
    PORT ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end COMPONENT;
SIGNAL Clk_in,Clk_out : STD_LOGIC;
begin
    UUT : Slow_Clk
        PORT MAP(
            Clk_in => Clk_in,
            Clk_out => Clk_out
        );
    Clk : PROCESS
        BEGIN
            Clk_in <= '0';WAIT FOR 10 NS;
            Clk_in <= '1';WAIT FOR 10 NS;
    END PROCESS;

end Behavioral;
```

4.0 Timing diagram



4.0 Counter

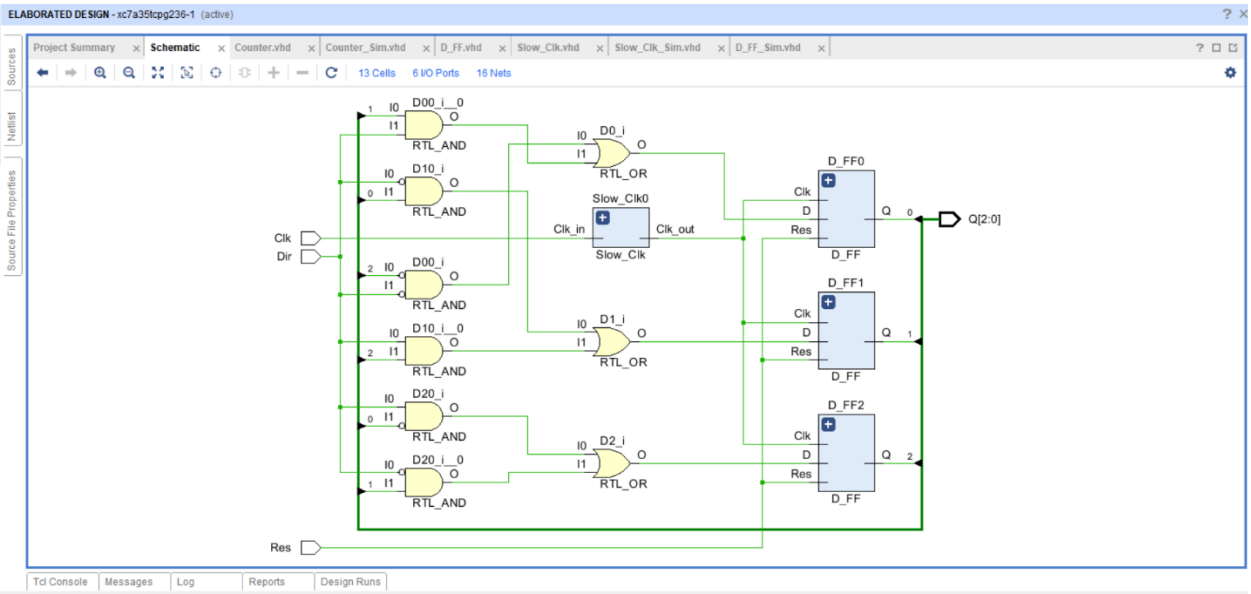
1.0 Design source file

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/06/2024 09:24:32 AM
-- Design Name:
-- Module Name: Counter - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Counter is
    Port ( Dir : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (2 downto 0));
end Counter;

architecture Behavioral of Counter is
COMPONENT D_FF
    PORT(
        D,Res,Clk : IN STD_LOGIC;
        Q,Qbar : OUT STD_LOGIC
    );
END COMPONENT;
COMPONENT Slow_Clk
    PORT ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end COMPONENT;
SIGNAL D0,D1,D2,Q0,Q1,Q2,Clk_slow : STD_LOGIC;

begin


    Slow_Clk0 : Slow_Clk
        PORT MAP(
            Clk_in => Clk,
            Clk_out => Clk_slow
        );
    D0 <= ((NOT Q2) AND (NOT Dir)) OR (Q1 AND Dir);
    D1 <= ((NOT Dir) AND Q0) OR (Dir AND Q2);
    D2 <= (Dir AND (NOT Q0)) OR ((NOT Dir) AND Q1);
```

```
    D_FF0 : D_FF
        PORT MAP(
            D => D0,
            Res => Res,
            Clk => Clk_slow,
            Q => Q0
        );
    D_FF1 : D_FF
        PORT MAP(
            D => D1,
            Res => Res,
            Clk => Clk_slow,
            Q => Q1
        );
    D_FF2 : D_FF
        PORT MAP(
            D => D2,
            Res => Res,
            Clk => Clk_slow,
            Q => Q2
        );

    Q(0) <= Q0;
    Q(1) <= Q1;
    Q(2) <= Q2;

end Behavioral;
```

2.0 Elaborated design schematic



3.0 Simulation source file

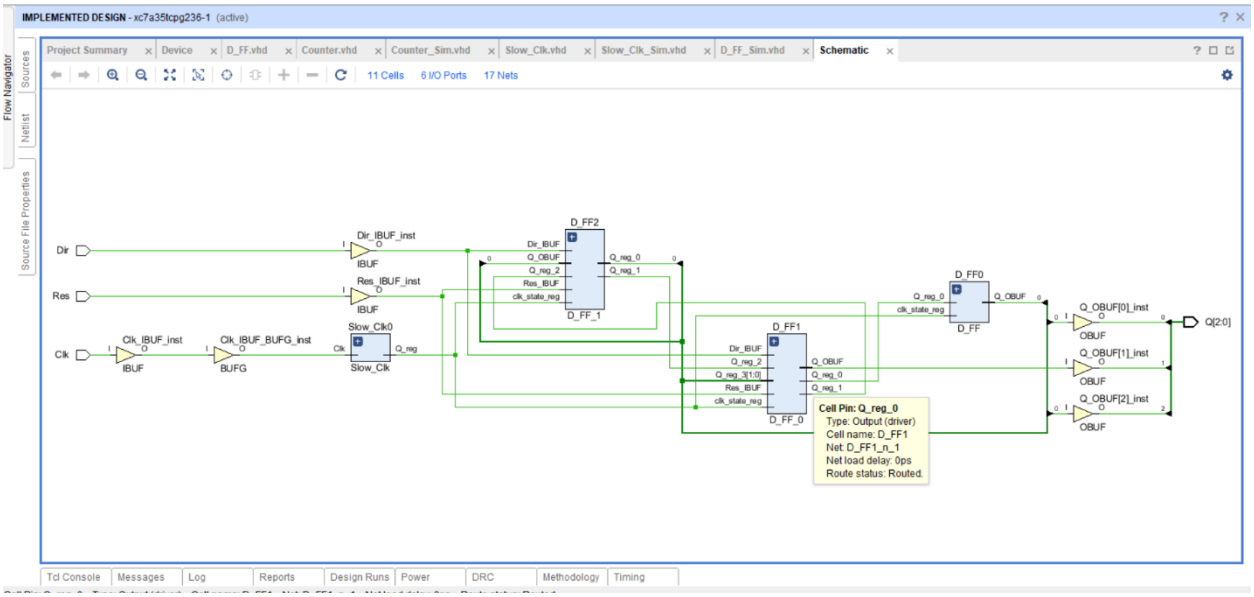
```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 03/06/2024 12:44:58 PM
-- Design Name:
-- Module Name: Counter_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Counter_Sim is
--  Port ( );
end Counter_Sim;

architecture Behavioral of Counter_Sim is
COMPONENT Counter is
    Port ( Dir : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (2 downto 0));
end COMPONENT;
SIGNAL Dir,Res,Clk : STD_LOGIC;
SIGNAL Q : STD_LOGIC_VECTOR (2 DOWNTO 0);
begin
    UUT : Counter
        PORT MAP(
            Dir => Dir,
            Res => Res,
            Clk => Clk,
            Q => Q
        );
    Clk1 : PROCESS
        BEGIN
            Clk <= '1';WAIT FOR 10 NS;
            Clk <= '0';WAIT FOR 10 NS;
        END PROCESS;
    PROCESS
        BEGIN
            Res <= '1';
            WAIT FOR 100 NS;

            Res <= '0';

            Dir <= '0';WAIT FOR 300 NS;
```

```
            Res <= '1';
            WAIT FOR 100 NS;

            Res <= '0';

             Dir <= '1';WAIT FOR 600 NS;
    END PROCESS;

end Behavioral;
```

4.0 Timing diagram

5.0 Implemented design schematic



6.0 Constraints file (XDC file - without commented lines)

```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports Clk]
    set_property IOSTANDARD LVCMOS33 [get_ports Clk]
    create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports
Clk]

## Switches
set_property PACKAGE_PIN V17 [get_ports {Dir}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Dir}]

## LEDs
set_property PACKAGE_PIN U16 [get_ports {Q[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Q[0]}]
set_property PACKAGE_PIN E19 [get_ports {Q[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Q[1]}]
set_property PACKAGE_PIN U19 [get_ports {Q[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Q[2]}]

##Buttons
set_property PACKAGE_PIN U17 [get_ports Res]
    set_property IOSTANDARD LVCMOS33 [get_ports Res]
```

5.0 Conclusion

This lab is to design and implement a D Flip-Flop, Slow Clock and a Counter for a given pattern. These things are very important building blocks in memory registers.