Lab	**: 03 (Adder)**
Student Name	**: M.K.S.L.Weerasiri**
Index Number	**: 220689N**
Group	**: Group 32**
Link for Lab3 files	**:** https://drive.google.com/drive/folders/1E4wiEwofWTYo-r6p6gkapLjP6yISQdFP?usp=sharing

Lab Task

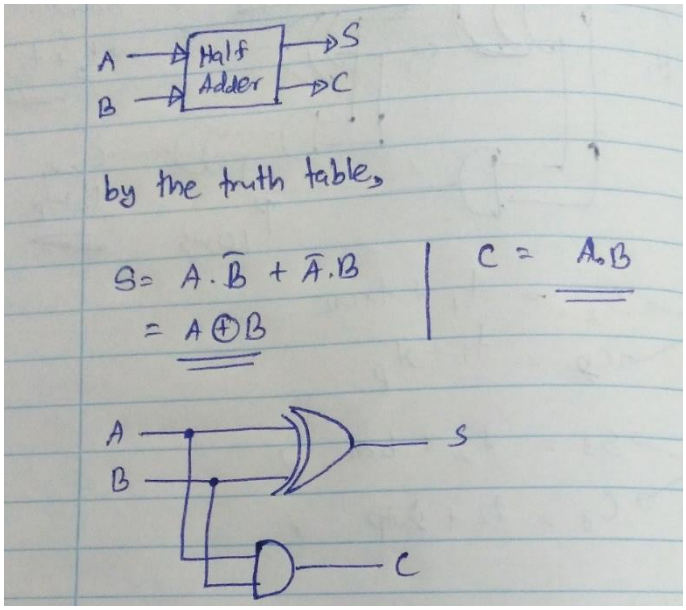
- Design and simulate a half adder.
  (Inputs -> A,B and Outputs -> S,C)
- Design and simulate a full adder using two half adders.
  (Inputs -> A,B,C_in and Outputs -> S,C_out)
- Create a macro symbol of the full adder or future use.
- Add that IP Block to the current project.
- Design and simulate a 4-bit adder using 4 full adders.
  (Inputs -> A0,A1,A2,A3,B0,B1,B2,B3,C_in and Outputs -> S0,S1,S2,S3,C_out)

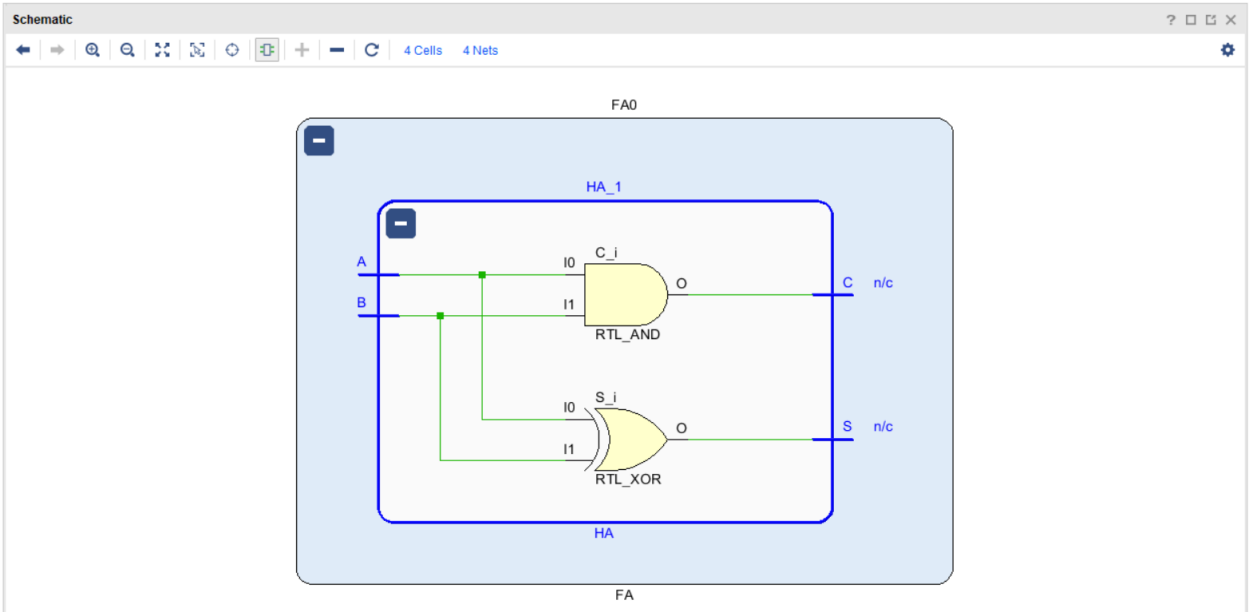
Half Adder

- **Truth table**

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- **Simplification Steps**





- **VHDL files**

➢ **HA.vhd :** https://drive.google.com/file/d/1mjJeb3ZEZBsYW0rrdVs47WJL6Gb7At6E/view?usp=sharing

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/13/2024 06:47:22 PM
-- Design Name:
-- Module Name: HA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity HA is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           S : out STD_LOGIC;
           C : out STD_LOGIC);
end HA;

architecture Behavioral of HA is

begin

    S <= A XOR B;
    C <= A AND B;


end Behavioral;
```

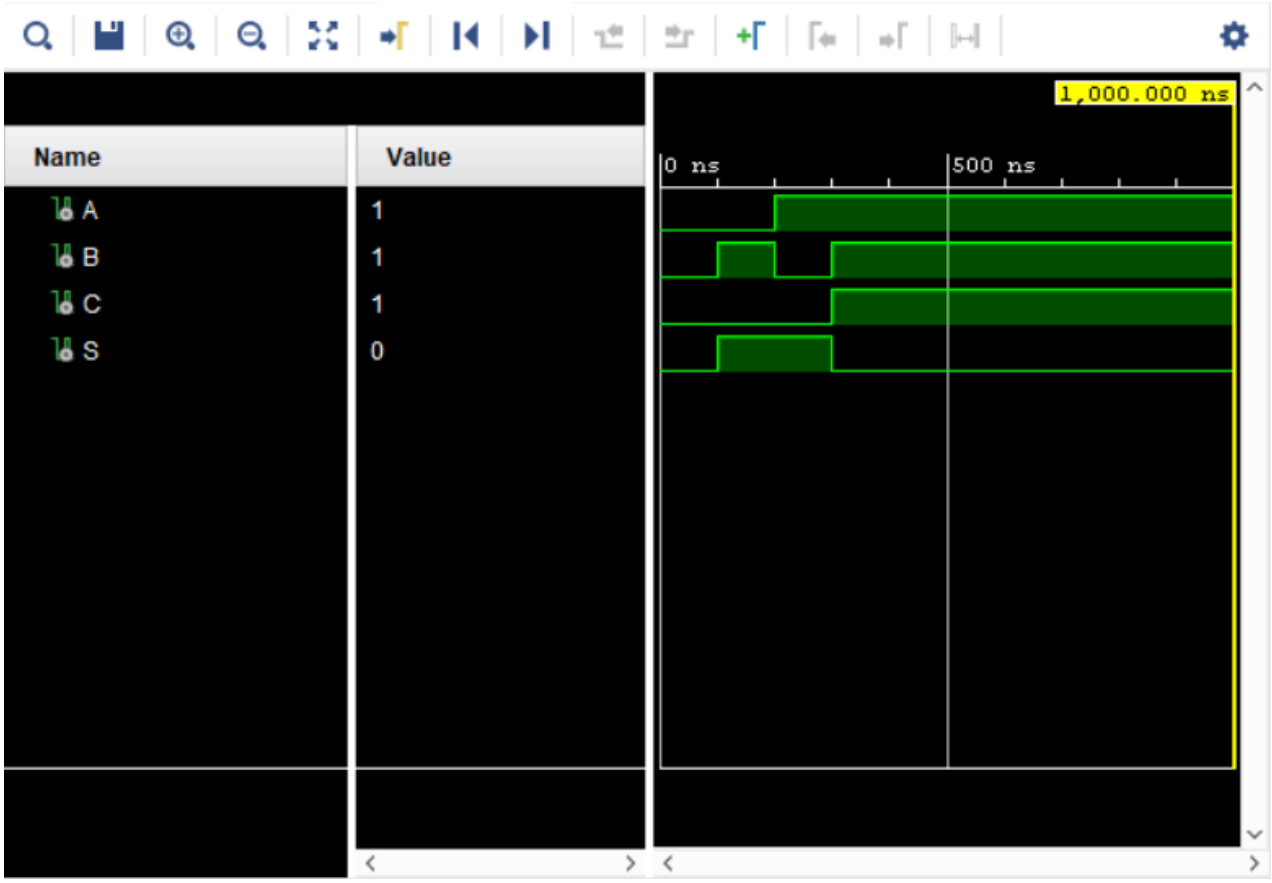
- **TB_HA.vhd :**
  https://drive.google.com/file/d/1VVmDnlIhTDZ8KAMEamBngMYhAqVUgjrz/view?usp=sharing

```
      ----------------------------------------------------------------------------------
-----------

-- Company:
-- Engineer:
--
-- Create Date: 02/13/2024 06:48:59 PM
-- Design Name:
-- Module Name: TB_HA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
```

```
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_HA is
--  Port ( );
end TB_HA;

architecture Behavioral of TB_HA is
COMPONENT HA
    PORT(
        A,B : IN STD_LOGIC;
        S,C : OUT STD_LOGIC
    );
END COMPONENT;
SIGNAL A,B,C,S: STD_LOGIC;

begin
    UUT: HA
        PORT MAP(
        A => A,
        B => B,
        S => S,
        C => C
    );

    PROCESS
        BEGIN
            A <= '0'; B <= '0'; WAIT FOR 100 NS;
```

```
            B <= '1'; WAIT FOR 100 NS;

            A <= '1'; B <= '0'; WAIT FOR 100 NS;

            B <= '1'; WAIT;
    END PROCESS;

end Behavioral;
```

- **Timing Diagram (for all combinations)**



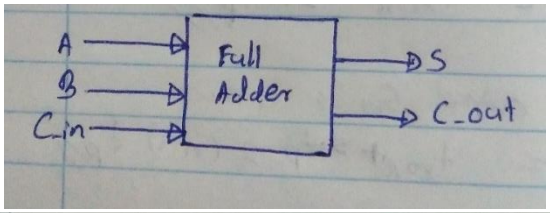
GIF :
https://drive.google.com/file/d/1lgvmlpkaKoXQOVgpMiTRAw4a2LoXK7Qr/view?usp=sharing

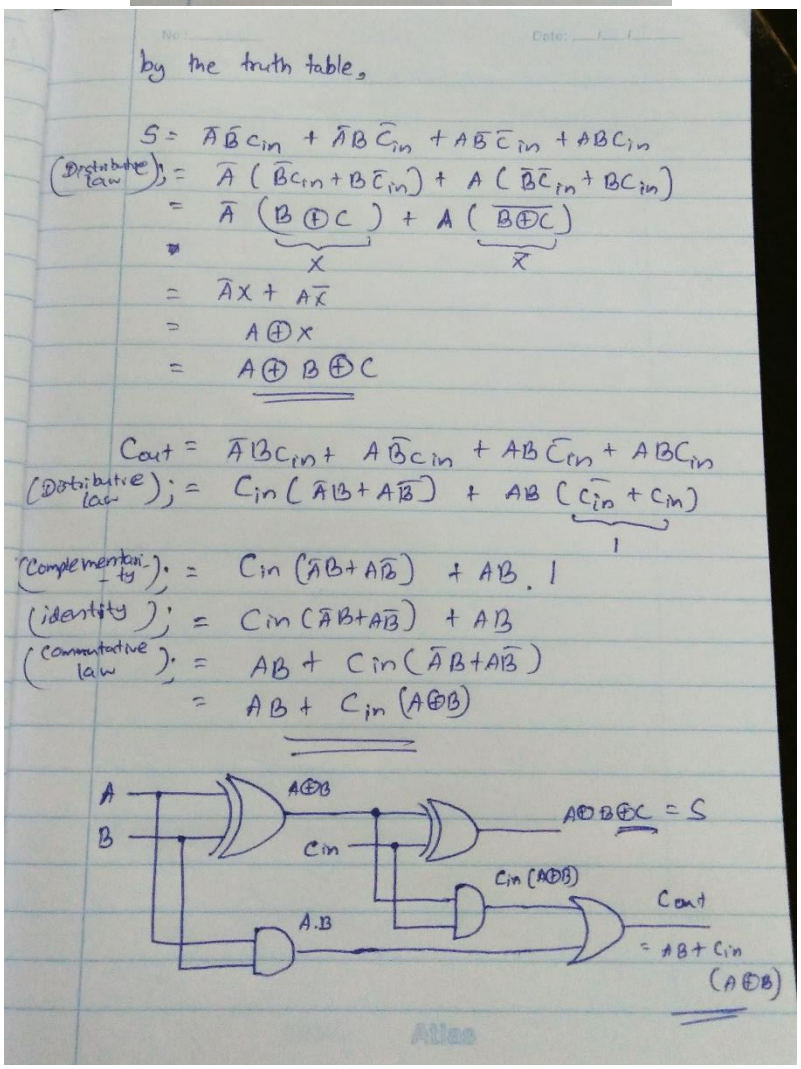
Full Adder

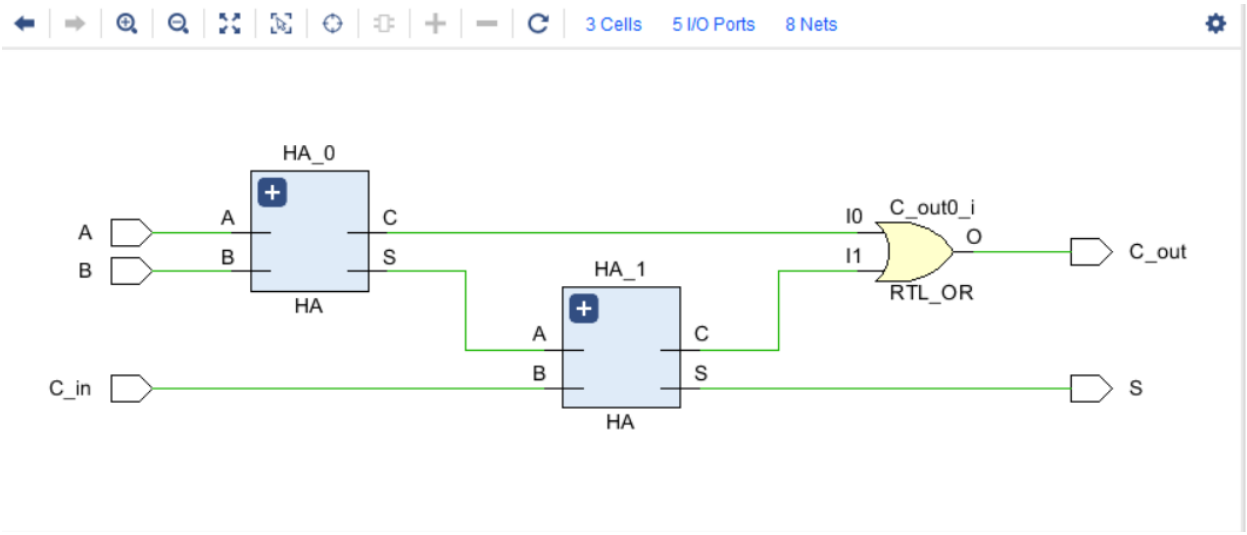
- **Truth table**

A	B	C_in	S	C_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- **Simplification Steps**







- **VHDL files**

➢ **FA.vhd :**
https://drive.google.com/file/d/19Qa-PNRu54O1iwlXDjCUxUFUrB3LnZbw/view?usp=sharing

```
----------------------------------------------------------------------------------
----
-- Company:
-- Engineer:
--
-- Create Date: 02/13/2024 06:59:40 PM
-- Design Name:
-- Module Name: FA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
----


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
```

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity FA is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S : out STD_LOGIC;
           C_out : out STD_LOGIC);
end FA;

architecture Behavioral of FA is
COMPONENT HA
    PORT(
        A : IN STD_LOGIC;
        B : IN STD_LOGIC;
        S : OUT STD_LOGIC;
        C : OUT STD_LOGIC
    );
END COMPONENT;

SIGNAL HA0_S, HA0_C, HA1_S, HA1_C : STD_LOGIC;

begin
    HA_0 : HA
        PORT MAP(
            A => A,
            B => B,
            S => HA0_S,
            C => HA0_C
        );
     HA_1 : HA
        PORT MAP(
            A => HA0_S,
            B => C_in,
            S => HA1_S,
            C => HA1_C
        );

    S <= A XOR B XOR C_in;
    --S <= HA1_S;
    C_out <= (A AND B) or (C_in and(A XOR B));
    --C_out <= HA1_C;
```

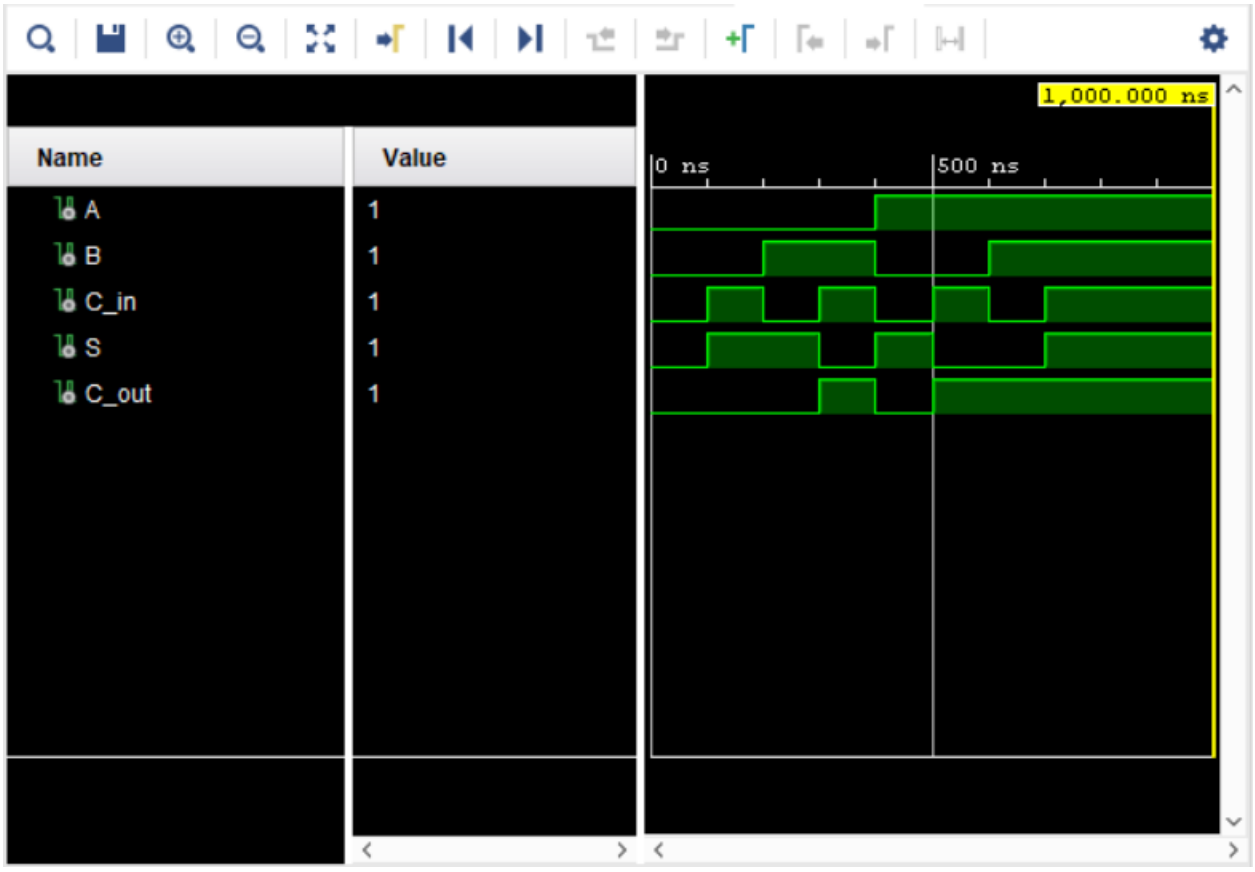
```
end Behavioral;
```

- **TB_FA.vhd :** https://drive.google.com/file/d/1WVcXIUVeKUDHlMEGP11DU__c02zHbHhk/view?usp=sharing

```
----------------------------------------------------------------------------------
----
-- Company:
-- Engineer:
--
-- Create Date: 02/13/2024 07:09:19 PM
-- Design Name:
-- Module Name: TB_FA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
----


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_FA is
--  Port ( );
end TB_FA;
```

```
architecture Behavioral of TB_FA is
COMPONENT FA
    PORT(
        A : IN STD_LOGIC;
        B : IN STD_LOGIC;
        C_in : IN STD_LOGIC;
        S : OUT STD_LOGIC;
        C_out : OUT STD_LOGIC
    );
END COMPONENT;
SIGNAL A,B,C_in,S,C_out : STD_LOGIC;
begin
    UUT : FA
        PORT MAP(
            A => A,
            B => B,
            C_in => C_in,
            S => S,
            C_out => C_out
        );

    PROCESS
        BEGIN
            A <= '0';B <= '0';C_in <= '0'; WAIT FOR 100 NS;

            C_in <= '1'; WAIT FOR 100 NS;

            B <= '1';C_in <= '0'; WAIT FOR 100 NS;

            C_in <= '1'; WAIT FOR 100 NS;

            A <= '1';B <= '0';C_in <= '0'; WAIT FOR 100 NS;

            C_in <= '1'; WAIT FOR 100 NS;

            B <= '1';C_in <= '0'; WAIT FOR 100 NS;

            C_in <= '1'; WAIT;
    END PROCESS;

end Behavioral;
```

- **Timing Diagram (for all combinations)**



GIF :
https://drive.google.com/file/d/1EXGOPfFmZqB8ZzYsvaCTHTrmvufC5Pjj/view?usp=sharing

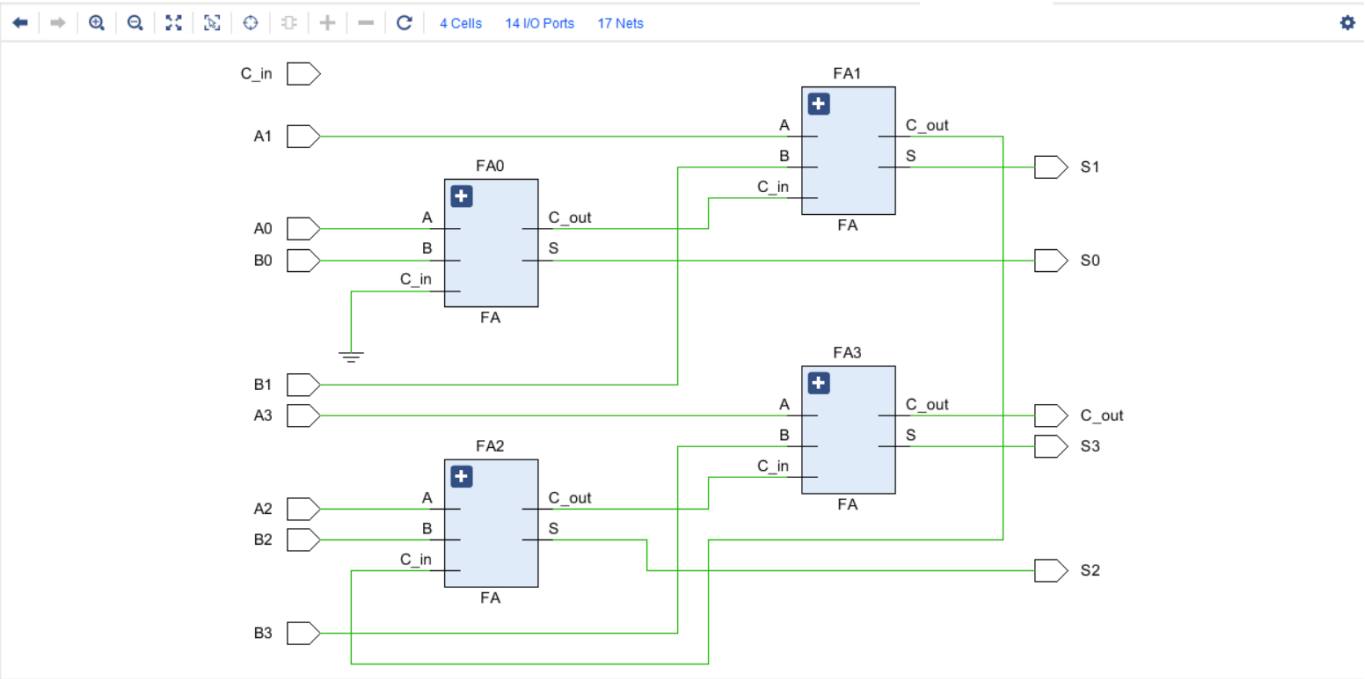
4-bit Adder

- **Truth table (Only for test cases)**

(Registration No in binary 11 0101 1110 0001 0001_2)

Case	A3	A2	A1	A0	B3	B2	B1	B0	C_in	S3	S2	S1	S0	C_ou
Registration No $0001_2 + 0001_2$	0	0	0	1	0	0	0	1	0	0	0	1	0	0
Registration No $0101_2 + 1110_2$	1	1	1	0	0	1	0	1	0	0	0	1	1	1
$0010_2 + 1110_2$	0	0	1	0	1	1	1	0	0	0	0	0	0	1
$0101_2 + 1011_2$	0	1	0	1	1	0	1	1	0	0	0	0	0	1
$0111_2 + 1111_2$	0	1	1	1	1	1	1	1	0	0	1	1	0	1
$1001_2 + 1100_2$	1	0	0	1	1	1	0	0	0	0	1	0	1	1
$0011_2 + 1100_2$	0	0	1	1	1	1	0	0	0	1	1	1	1	0
$1101_2 + 1011_2$	1	1	0	1	1	0	1	1	0	1	0	0	0	1
$1111_2 + 1111_2$	1	1	1	1	1	1	1	1	0	1	1	1	0	1

- **Simplification Steps**



- **VHDL files**

➢ **RCA_4.vhd :**
https://drive.google.com/file/d/1vcQj4_dNP08nJ69q9F7wV5CN6jmm080P/view?usp=sharing

```
----------------------------------------------------------------------------
----
-- Company:
-- Engineer:
--
-- Create Date: 02/13/2024 07:30:53 PM
-- Design Name:
-- Module Name: RCA_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
----


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity RCA_4 is
    Port ( A0 : in STD_LOGIC;
           A1 : in STD_LOGIC;
           A2 : in STD_LOGIC;
           A3 : in STD_LOGIC;
           B0 : in STD_LOGIC;
           B1 : in STD_LOGIC;
           B2 : in STD_LOGIC;
           B3 : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S0 : out STD_LOGIC;
           S1 : out STD_LOGIC;
           S2 : out STD_LOGIC;
           S3 : out STD_LOGIC;
```

```
          C_out : out STD_LOGIC);
end RCA_4;

architecture Behavioral of RCA_4 is
COMPONENT FA
    PORT(
        A : IN STD_LOGIC;
        B : IN STD_LOGIC;
        C_in : IN STD_LOGIC;
        S : OUT STD_LOGIC;
        C_out : OUT STD_LOGIC
    );
END COMPONENT;
SIGNAL FA0_C,FA1_C,FA2_C,FA3_C : STD_LOGIC;
begin
    FA0 : FA
        PORT MAP(
            A => A0,
            B => B0,
            C_in => '0',
            S => S0,
            C_out => FA0_C
        );
    FA1 : FA
        PORT MAP(
            A => A1,
            B => B1,
            C_in => FA0_C,
            S => S1,
            C_out => FA1_C
        );
    FA2 : FA
        PORT MAP(
            A => A2,
            B => B2,
            C_in => FA1_C,
            S => S2,
            C_out => FA2_C
        );
    FA3 : FA
        PORT MAP(
            A => A3,
            B => B3,
            C_in => FA2_C,
            S => S3,
            C_out => FA3_C
        );
```

```
    C_out <= FA3_C;

end Behavioral;
```

- **TB_4_RCA.vhd :** https://drive.google.com/file/d/1gp_i1lee1e0EBlp9dBoPtButKe5yxJ2U/view?usp=sharing

```
----------------------------------------------------------------------------------
----
-- Company:
-- Engineer:
--
-- Create Date: 02/13/2024 07:42:46 PM
-- Design Name:
-- Module Name: TB_4_RCA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
----


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_4_RCA is
--  Port ( );
end TB_4_RCA;

architecture Behavioral of TB_4_RCA is
```

```
COMPONENT RCA_4
    Port ( A0 : in STD_LOGIC;
           A1 : in STD_LOGIC;
           A2 : in STD_LOGIC;
           A3 : in STD_LOGIC;
           B0 : in STD_LOGIC;
           B1 : in STD_LOGIC;
           B2 : in STD_LOGIC;
           B3 : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S0 : out STD_LOGIC;
           S1 : out STD_LOGIC;
           S2 : out STD_LOGIC;
           S3 : out STD_LOGIC;
           C_out : out STD_LOGIC);
END COMPONENT;

SIGNAL A0,A1,A2,A3,B0,B1,B2,B3,C_in,S0,S1,S2,S3,C_out : STD_LOGIC;

begin

    UUT : RCA_4
        PORT MAP(
            A0 => A0,
            A1 => A1,
            A2 => A2,
            A3 => A3,
            B0 => B0,
            B1 => B1,
            B2 => B2,
            B3 => B3,
            C_in => C_in,
            S0 => S0,
            S1 => S1,
            S2 => S2,
            S3 => S3,
            C_out => C_out
        );

        PROCESS
            BEGIN
                --My Index  220689N
                -->>bin(220689)
                -->>0b110101111000010001
                -->> A : 0001 ,   B : 0001
                A0 <= '1';A1 <= '0';A2 <= '0';A3 <= '0';B0 <= '1';B1 <= '0';B2
<= '0';B3 <= '0';C_in <= '0';
                WAIT FOR 100 NS;
```

```
                -->> A : 1110 ,   B : 0101
                A0 <= '0';A1 <= '1';A2 <= '1';A3 <= '1';B0 <= '1';B1 <= '0';B2
<= '1';B3 <= '0';C_in <= '0';
                WAIT FOR 100 NS;

                -- 0010 + 1110
                A0 <= '0';A1 <= '1';A2 <= '0';A3 <= '0';B0 <= '0';B1 <= '1';B2
<= '1';B3 <= '1';C_in <= '0';
                WAIT FOR 100 NS;

                -- 0101 + 1011
                A0 <= '1';A1 <= '0';A2 <= '1';A3 <= '0';B0 <= '1';B1 <= '1';B2
<= '0';B3 <= '1';C_in <= '0';
                WAIT FOR 100 NS;

                -- 0111 + 1111
                A0 <= '1';A1 <= '1';A2 <= '1';A3 <= '0';B0 <= '1';B1 <= '1';B2
<= '1';B3 <= '1';C_in <= '0';
                WAIT FOR 100 NS;

                --1001 + 1100
                A0 <= '1';A1 <= '0';A2 <= '0';A3 <= '1';B0 <= '0';B1 <= '0';B2
<= '1';B3 <= '1';C_in <= '0';
                WAIT FOR 100 NS;

                --0011 + 1100
                A0 <= '1';A1 <= '1';A2 <= '0';A3 <= '0';B0 <= '0';B1 <= '0';B2
<= '1';B3 <= '1';C_in <= '0';
                WAIT FOR 100 NS;

                --1101 + 1011
                A0 <= '1';A1 <= '0';A2 <= '1';A3 <= '1';B0 <= '1';B1 <= '1';B2
<= '0';B3 <= '1';C_in <= '0';
                WAIT FOR 100 NS;

                --1111 + 1111
                A0 <= '1';A1 <= '1';A2 <= '1';A3 <= '1';B0 <= '1';B1 <= '1';B2
<= '1';B3 <= '1';C_in <= '0';
                WAIT FOR 100 NS;

        END PROCESS;


end Behavioral;
```

- **Timing Diagram (for some combinations)**

GIF :
https://drive.google.com/file/d/1czOvbyOyvWggfad8wHjzMwBYDOInekm8/view?usp=sharing

Discussion

- **Discuss why some of the input combinations results in outputs that cannot be represented using LED LD0-LD3.**

In this lab,

LD0 refers the value of S0, LD1 refers the value of S1, LD2 refers the value of S2, LD3 refers the value of S3.

But there are some input combinations that need at least 5 bits to represent the answer (when the inputs are restricted to 4 bits).

Ex :- $0001_2 + 1111_2 = 1\ 0000_2$

Because of that, we can't represent all the combinations only with LD0-LD3 LEDs. We need at least one additional LED, and we use LD15 for that task.

- **Discuss the role of LD15**

In this lab,

LD15 refers the value of C_out of the whole 4-bit adder.

It means the carry bit at the end of the calculation.

If (the result of the adder > 1111_2){

    LD15 is ON; //Carry bit is available

}else{

    LD15 is OFF; //No Carry bit

}