EEE211

PSpice experiment – Part 2

Design of an Operational Amplifier

QUESTION FORM

NAME: **STUDENT ID:**

Sahand Sabour **1614650**

Questions

1. *Briefly explain how an 'active load' doubles the gain of the differential input stage (10%)*

   The following figure (Figure 1) displays the circuit diagram for the differential input stage when a passive load is implemented.

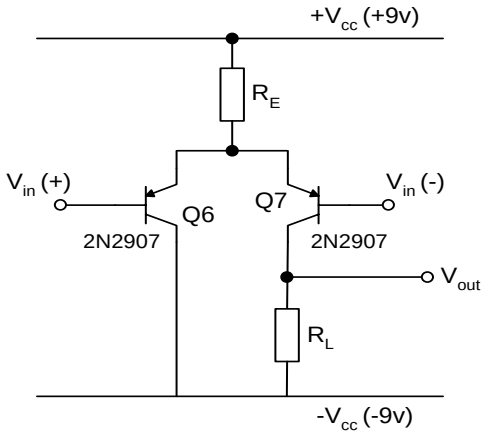

Figure 1: a pnp long tailed pair (with passive load)

Therefore, according to the above figure, the voltage gain for the circuit can be obtained as follows:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{i_c \times {R_L}'}{V_{in}}$$

Where ${R_L}'$ is the total effective load seen by the collector of Q7. Moreover, collector current i_c can be written as $g_m V_\pi$, where V_π calculated is as follows:

$$V_\pi = \frac{V_{in}}{2}$$

Which gives

$$\boldsymbol{A_V = \frac{V_{out}}{V_{in}} = \frac{\frac{g_m V_{in}}{2} \times {R_L}'}{V_{in}} = \frac{g_m {R_L}'}{2}}$$

By replacing the load resistor R_L with a current mirror circuit, an active load is applied to the circuit. Figure 2 displays the differential input stage with an active load.

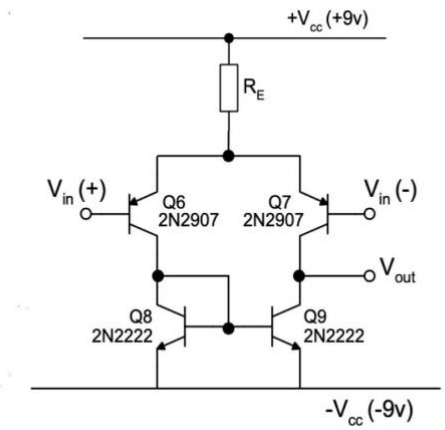

Figure 2: a pnp long tailed pair (with active load)

Therefore, the gain for this circuit can be obtained by the following equation:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{i_{out} \times R_L{}'}{V_{in}}$$

Where $R_L{}'$ is the total effective load seen by the collector of Q7. Moreover, collector current i_{out} can be written as follows.

$$i_{out} = i_{C7} - i_{C9} = i_{C7} - i_{C6} = g_m v_{in}(+) - g_m v_{in}(-)$$

Since $V_{in} = v_{in}(+) - v_{in}(-)$

$$i_{out} = g_m V_{in}$$

Which gives the voltage gain with an active load as the following equation:

$$\boldsymbol{A_V = \frac{g_m V_{in} \times R_L{}'}{V_{in}} = g_m R_L{}'}$$

Therefore, it was demonstrated that an 'active load' has doubled the gain of the differential input stage.

2. *Give the circuit diagram of your differential amplifier input circuit and show your calculation of the differential input resistance and voltage gain of the input stage. (15%)*

   The following figure (Figure 3) displays the circuit diagram for the differential amplifier circuit used for this section of the experiment.

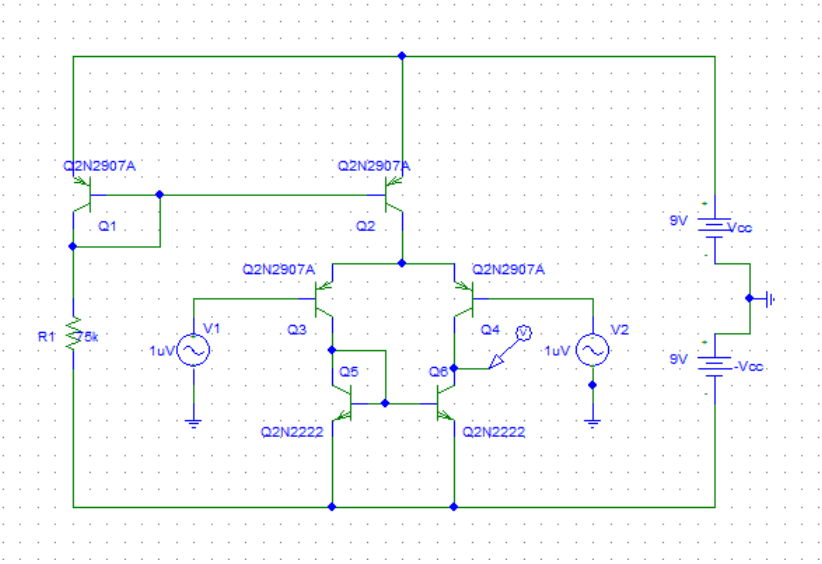

Figure 3: the circuit diagram for the differential amplifier circuit

As the first step of the required calculations for this section, the reference current of the current mirror is to be calculated. Therefore, according to the above figure, we are able to get the following equation.

$$I_{Ref} = \frac{V_{CC} - V_{be\,Q1}(on) - (-V_{CC})}{R_1}$$

$$I_{Ref} = \frac{9 - 0.7 - (-9)}{75 \times 10^3} \cong 0.23\ mA$$

Subsequently, as known in the current mirror configuration, the collector current of Q3 and Q4 are of equal values and are equal to half of the reference current, which suggests the following equation.

$$I_{C3} = I_{C4} = \frac{0.23\ mA}{2} = 0.115\ mA$$

Additionally, I_{C3} can be used in order to calculate $r_{\pi 3}$, which would be used in order to calculate the input resistance. The calculation procedure for the mentioned goes as follows.

$$r_{\pi 3} = \frac{\beta}{40 I_{C3}} = \frac{251}{4.6} = 54.56\ k\Omega$$

$$R_{in} = 2r_{\pi 3} = 109.12 k\Omega$$

Accordingly, R_L' is to be calculated in order to find the voltage gain of the input stage.

$$R_L' = r_{o4}\,||r_{o6}$$

Where the required values of r_o can be obtained by the following equations:

$$r_{o4} = \frac{V_A}{I_{C4}} = \frac{113}{0.115 \times 10^{-3}} = 982.6\ k\Omega$$

$$r_{o6} = \frac{V_A}{I_{C4}} = \frac{74}{0.115 \times 10^{-3}} = 643.4\ k\Omega$$

Therefore, the value of R_L' can be calculated.

$$R_L' = \frac{r_{o4} \times r_{o6}}{r_{o4} + r_{o6}} = \frac{632.2}{1626} = 388.8\ k\Omega$$

Furthermore, the voltage gain for the input stage can be calculated.

$$A_V = -g_m R_L' = -40 \times I_{C3} \times R_L'$$

$$A_V = -40 \times 0.115 \times 388.8 = -1788.5$$

Therefore, the required values were obtained as follows.

$$\mathbf{A_V = -1788.5}$$

and

$$\mathbf{R_{in} = 109.12k\Omega}$$

3. *Give your measurements used to obtain the input resistance and voltage gain of the input stage by simulation of the circuit. (10%)*

The below figure (Figure 4) provides the measurements to obtain the required values.

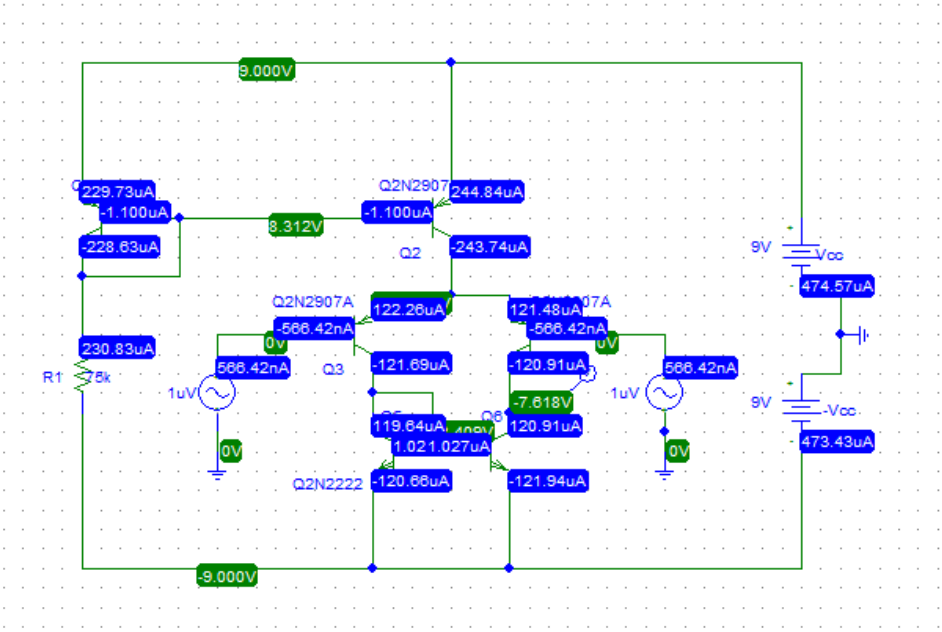

Figure 4: The measurements used to obtain R_{in} and A_V

Furthermore, the provided circuit and measurements were used to perform an AC sweep. Subsequently, traces corresponding to input resistance and voltage gain of the input stage were added and the obtained graphs were recorded respectively.
As the input resistance is equal to the difference of resistance between each input side, the trace corresponding to the input resistance was written as

$$\frac{V(V_1{:}+)}{I(V_1)} - \frac{V(V_2{:}-)}{I(V_2)}$$

The mentioned trace produced the following graph for input resistance (Figure 5).

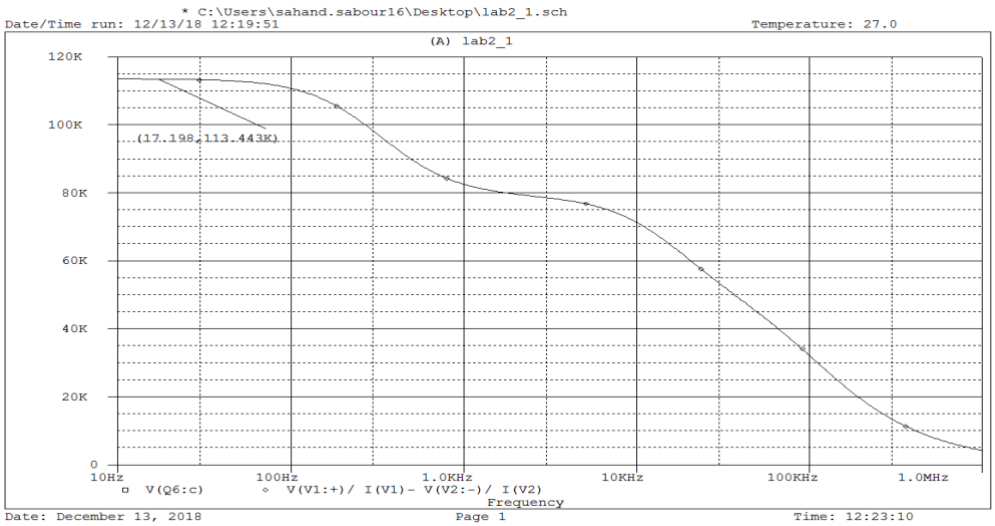

Figure 5: The obtained graph for R_{in} from the simulation

Moreover, as the output voltage is the collector voltage of Q6 while the input voltage is the difference between input voltages of each input side (Q1 and Q2), the following trace was added in order to graph the plot for the voltage gain of the input stage:

$$\frac{V(Q6{:}\,c)}{V(V_1{:}+) - V(V_2{:}-)}$$

Accordingly, the mentioned trace resulted in the following graph (Figure 6)

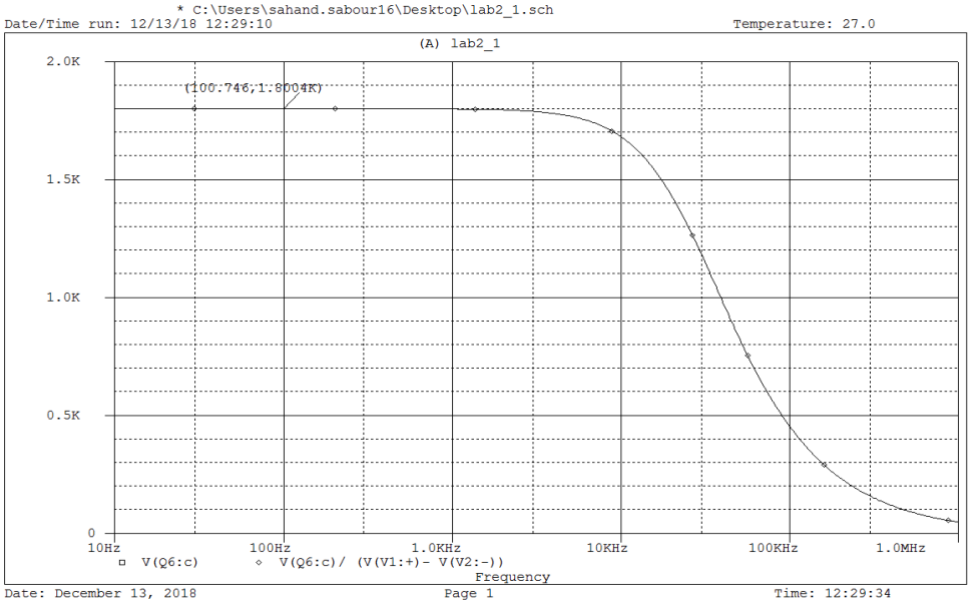

Figure 6: The obtained graph for A_V from the simulation

Therefore, according to the provided figures, the obtained results for the input stage of the circuit can be summarized as the following:

$$\mathbf{R_{in} = 113.443\ k\Omega}$$

and

$$\mathbf{A_V = 1800.4}$$

4. *Show the voltage transfer characteristic obtained by simulation. (10%)*

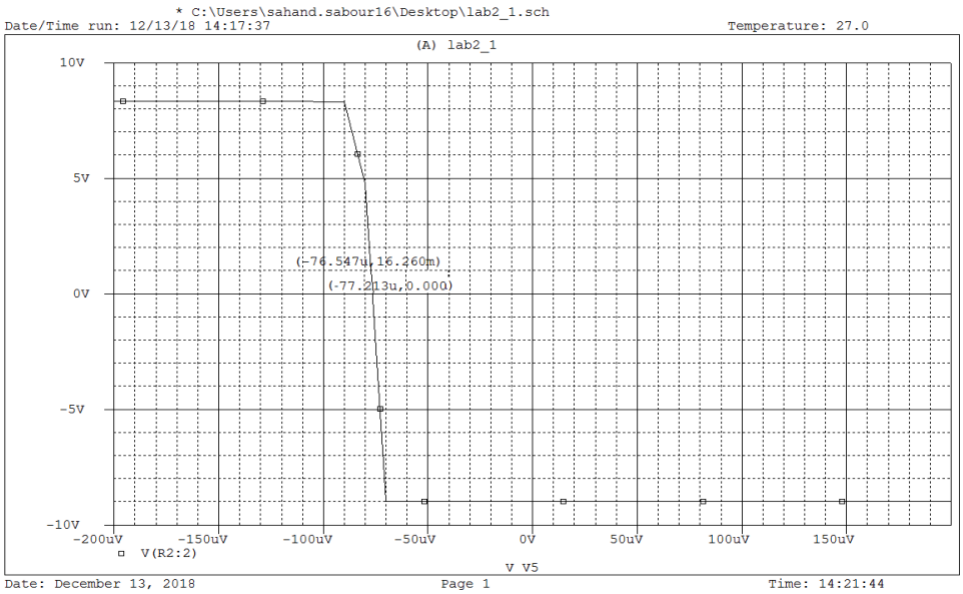

Figure 7: The voltage transfer characteristics obtained by the simulation

5. *Give your calculation of the open-loop differential voltage gain and the output resistance of the whole amplifier. You should make reference to the amplifier properties sheet included in the laboratory script and make reasonable approximations. (20%)*

After obtaining the results for the previous section, the value of the DC voltage source was set to -77.214 and the circuit was modified as shown in Figure 8.

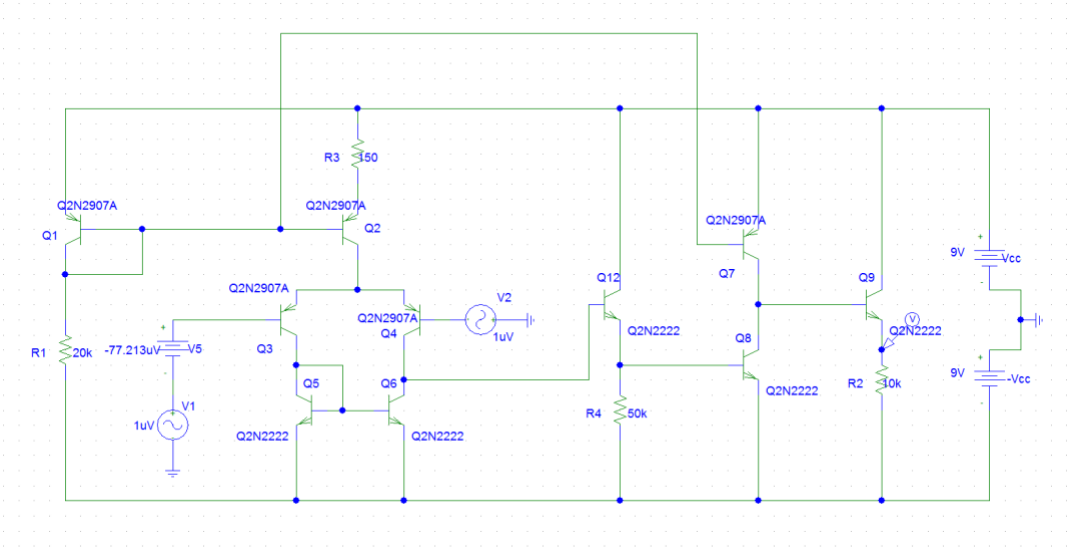

Figure 8: The modified completed circuit diagram

Moreover, in order to obtain the voltage and current values for the required equations regarding the calculation of the open-loop differential voltage gain and the output resistance, the following two figures (Figure 9 and Figure 10) were recorded.

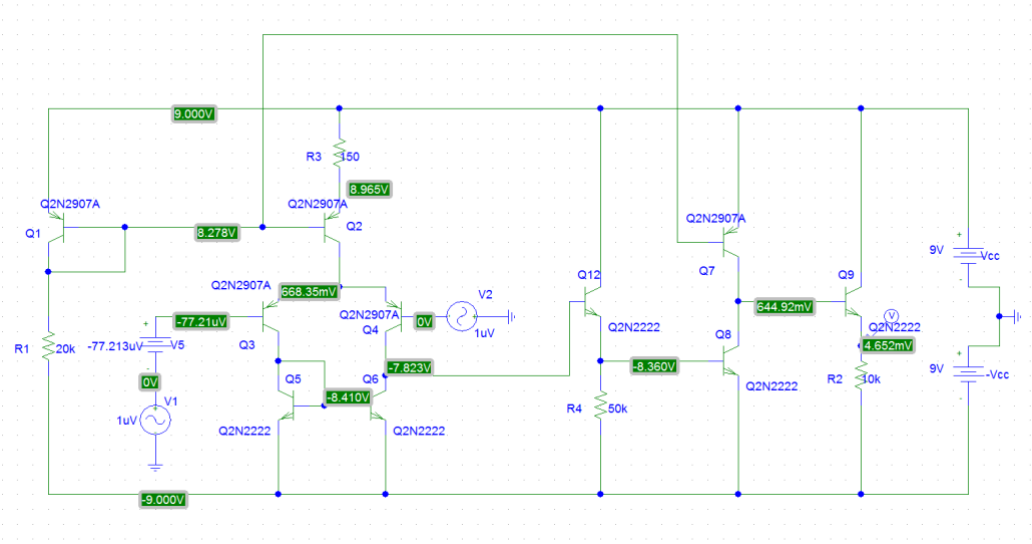

Figure 9: Voltage values for the completed circuit diagram

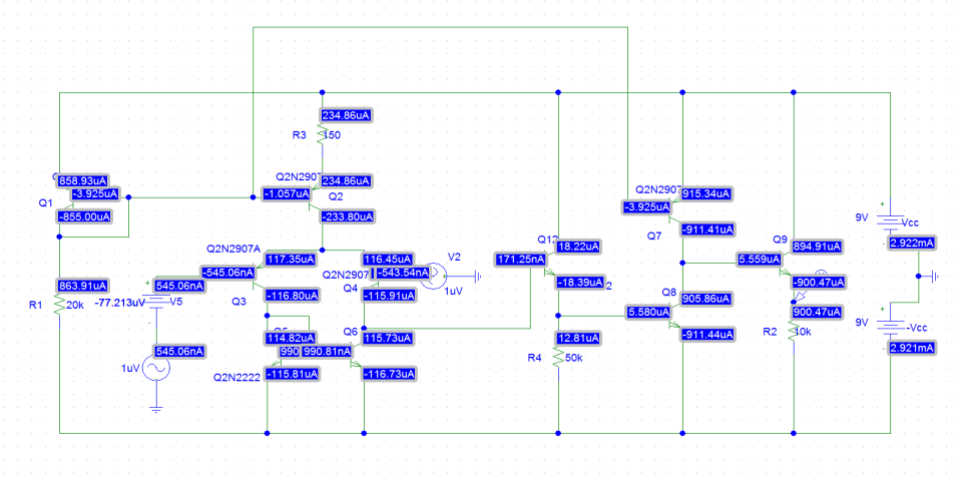

Figure 10: Current values for the completed circuit diagram

There is a total of five stages in this circuit. The first stage is a bias reference section of a current mirror formed with Q2 and Q7. The second stage is a differential amplifier. The third and fifth stages are common collector amplifiers, whose gain can be assumed to be unity. The fourth stage is a common emitter amplifier.

Based on the mentioned stages, the open-loop voltage gain can be obtained as follows.

$$A_v = A_{v2} \times A_{v3} \times A_{v4} \times A_{v5} = A_{v2} \times A_{v4}$$

Therefore, in order to calculate the overall open-loop gain, the gain of the second and the fourth stages are to be calculated initially.

For the fourth stage, we have that

$$A_{v4} = -g_{m8}\left(r_{07} \| r_{o8} \| R_{iQ10}\right)$$

According to Figure 10, we have that

$$I_{C8} = I_{C7} - \frac{I_{C9}}{\beta}$$

Where

$$I_{C9} = \frac{-(-V_{CC})}{R_2} = \frac{9\ V}{10\ k\Omega} = 0.9\ mA$$

And

$$I_{C7} = \frac{V_{CC} - V_{BE}(on) - (-V_{CC})}{R_1}$$

$$I_{C7} = \frac{9 - 0.7 - (-9)\ V}{20\ k\Omega} = 0.865\ mA$$

Therefore

$$I_{C8} = 0.865 - \frac{0.9}{167} \approx 0.86\ mA$$

Which gives

$$g_{m8} = 40 \times I_{C8} = 34.4\ mA/V$$

Furthermore, we also have that

$$r_{07} \approx \frac{V_A}{I_{C7}} = \frac{113}{0.865} = 130.6\ k\Omega$$

$$r_{08} \approx \frac{V_A}{I_{C8}} = \frac{74}{0.86} = 84\ k\Omega$$

As $R_{iQ10} = r_{\pi 9} + (1+\beta)(R_2)$, $r_{\pi 9}$ must be calculated in order to obtain R_{iQ10}.

$$r_{\pi 9} = \frac{\beta}{40\ \times I_{C9}} = \frac{167}{36} = 4.64\ k\Omega$$

Which gives

$$R_{iQ10} = 4.64 + (168)(10) = 1684.64\ k\Omega$$

Therefore, the voltage gain for the fourth stage can be obtained.

$$A_{v4} = -34.4 \times 49.62 = -1706.7$$

For the second stage, we have that

$$A_{v2} = -g_{m4}\left(r_{04}||r_{o6}||R_{iQ12}\right)$$

Where

$$g_{m4} = 40 \times I_{C4} = 40 \times 0.115\ mA = 4.6\frac{mA}{V}$$

(note that the value of I_{C4} was calculated in the previous sections)

$$r_{04} = \frac{V_A}{I_{C4}} = \frac{113}{0.115\ mA} = 982.6\ k\Omega$$

$$r_{06} = \frac{V_A}{I_{C4}} = \frac{74}{0.115\ mA} = 643.48\ k\Omega$$

$$R_{iQ12} = (1+\beta)(50k\ ||r_{\pi 8}) + r_{\pi 12}$$

Where

$$r_{\pi 8} = \frac{\beta}{g_{m8}} = \frac{167}{34.4} = 4.85\ k\Omega$$

And

$$r_{\pi 12} = \frac{\beta}{g_{m12}} = \frac{167}{0.56} = 298.2\ k\Omega$$

Giving

$$R_{iQ12} = 742.8 + 298.2 = 1041\ k\Omega$$

Therefore, the voltage gain for the second stage can be obtained.

$$A_{v2} = -4.6 \times 283.12 = -1302$$

In conclusion, the obtained values can be used in order to obtain the overall open-loop gain AV.

$$A_v = -1302 \times -1706.7 \approx 2.23 \times 10^6$$

For the output resistance of the whole complete circuit, the following equation can be written based on the circuit diagram.

$$R_{out} = \frac{r_{\pi 9} + (r_{07} || r_{08})}{\beta + 1} || R_2$$

$$R_{out} = \frac{4.64 + \frac{130.6 \times 89}{130.6 + 89}}{168} || 10k\Omega$$

$$R_{out} = \frac{0.34 \times 10}{0.34 + 10} = 0.32\ k\Omega$$

Therefore, the obtained could be summarized as the following:

$$\mathbf{A_v = 2.23 \times 10^6}$$

and

$$\mathbf{R_{out} = 0.32\ k\Omega}$$

6. *Complete the table below.*

Specification	**Open loop voltage gain**	**Input resistance (MΩ)**	**Output resistance (kΩ)**	**Current from supply (mA)**	**Input offset voltage Vos**
Specified value	**> 5 x10^5**	**> 0.1MΩ**	**< 1kΩ**	**< 5mA**	**---------**
Measured value	**1.28×10^6**	**107.98 kΩ**	**0.321 kΩ**	**2.922mA**	**-77.213µV**
Calculated value	**2.23×10^6**	**112.8 kΩ**	**0.32 kΩ**	**2.875 mA**	**---------**

In order to measure the open loop voltage gain, an AC sweep of the circuit was conducted and the trace for the output resistance, which is V(R2:2) was added. Figure 11 displays the obtained result from the mentioned procedure.

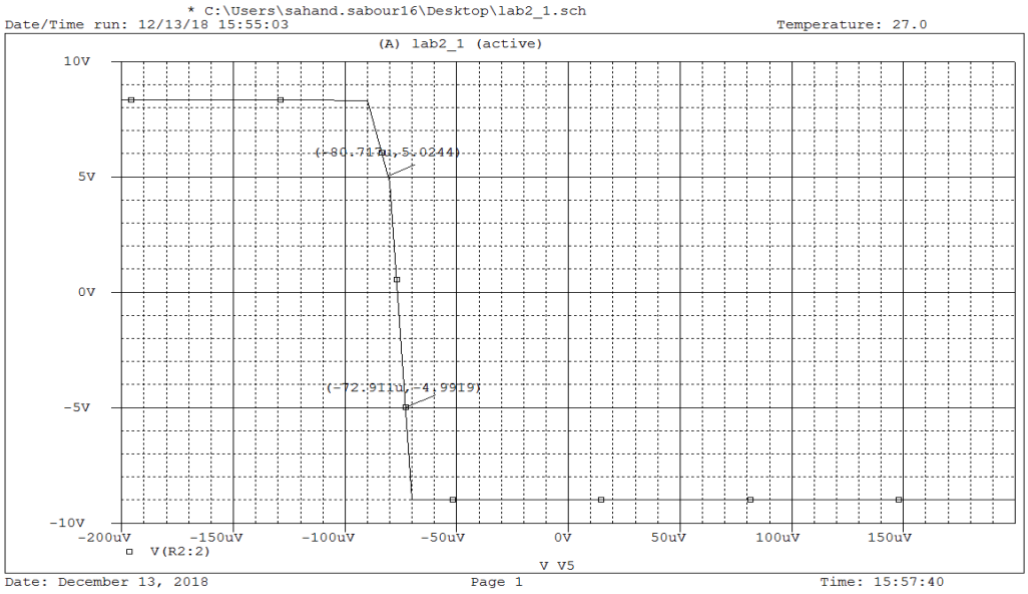

Figure 11: graph for AC sweep from simulation

As the slope of the later section of the graph is equal to the open-loop voltage gain, two arbitrary points were chosen from this section and the slope was measured.

Point 1: (-80,717µ, 5.0244)
Point 2: (-72.911 µ, -4.9919)

$$\text{Measured } A_V = \frac{5.0244 - (-4.9919)}{(-80.717 - (-72.911))\mu} = -1.28 \times 10^6$$

In order to measure the input resistance, the following trace was added to the already conducted AC sweep. This is due to the input resistance being equal to sum of resistance from each input side.

$$\frac{V(V1:+)}{IB(Q3)} + \frac{V(V2:-)}{IB(Q4)}$$

The following figure (Figure 12) displays the result of the mentioned trace.

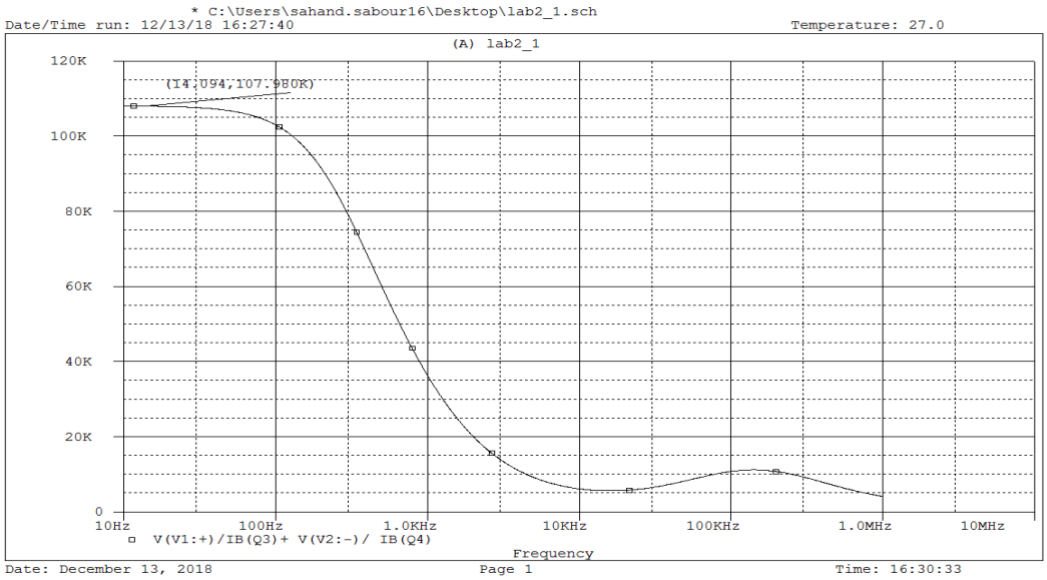

Figure 12: input resistance graph from the simulation

Furthermore, in order to measure the output resistance, the following trace was added to the already conducted AC sweep. This is due to the output resistance being equal to the division of the output voltage by the output current.

$$\frac{V(V6:+)}{I(V6)}$$

The following figure (Figure 13) was obtained as the result of the mentioned trace.

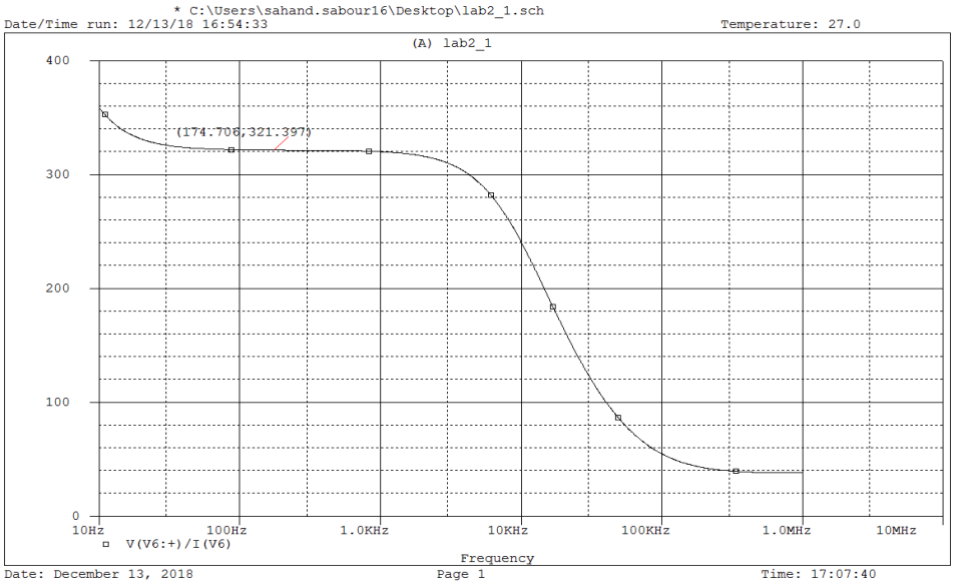

Figure 13: Output resistance graph from the simulation

Moreover, the current from supply was also measured via simulation (check Figure 10).

Regarding the calculated values, the open-loop voltage gain and output resistance were calculated in the previous section. As for the input resistance and the current from supply, the following equations were used to calculate the required values.
For the current supply, we have that

$$\text{current from supply} = I_{e1} + I_{e2} + I_{C12} + I_{e7} + I_{C9}$$
$$\text{current from supply} = 0.865 + 0.231 + 0.014 + 0.865 + 0.9$$
$$\text{current from supply} = 2.875\ mA$$

For the input resistance, we have that

$$R_{in} = \frac{V1}{I_B(Q3)} + \frac{V2}{I_B(Q4)}$$

$$R_{in} = \frac{V1}{\frac{I_e(Q3)}{\beta + 1}} + \frac{V2}{\frac{I_e(Q4)}{\beta + 1}}$$

Where $I_e(Q3) = I_e(Q4) = \frac{I_e(Q2)}{2} \approx 0.115\ mA$

$$R_{in} = \frac{77.213\mu}{\frac{0.115}{168}} + \frac{0\mu}{\frac{0.115}{168}} \approx 112.8\ \text{k}\Omega$$

Compare your measured and calculated values given in the table and account for any significant discrepancies. (10%)

The measured and calculated values have minor discrepancies, which are believed to be due to approximations that were made in the calculation process. It is also believed that by making the approximations more precise, the calculated values would become more similar to the measured values. However, the obtained calculated values are still valuable as the discrepancies are minor and inconsiderable.

7. *Give your measured Bode plots*

(a) log_{10} gain magnitude vs log_{10} frequency, and

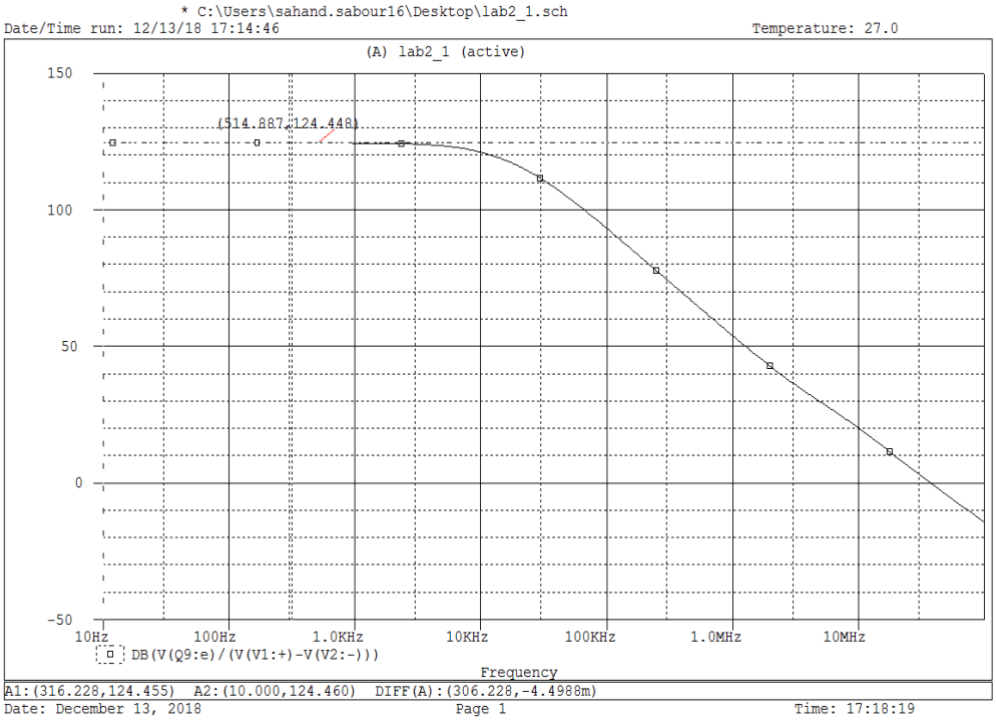

Figure 14: The bode plot for the gain magnitude (in dB)

(b) linear phase vs log_{10} frequency

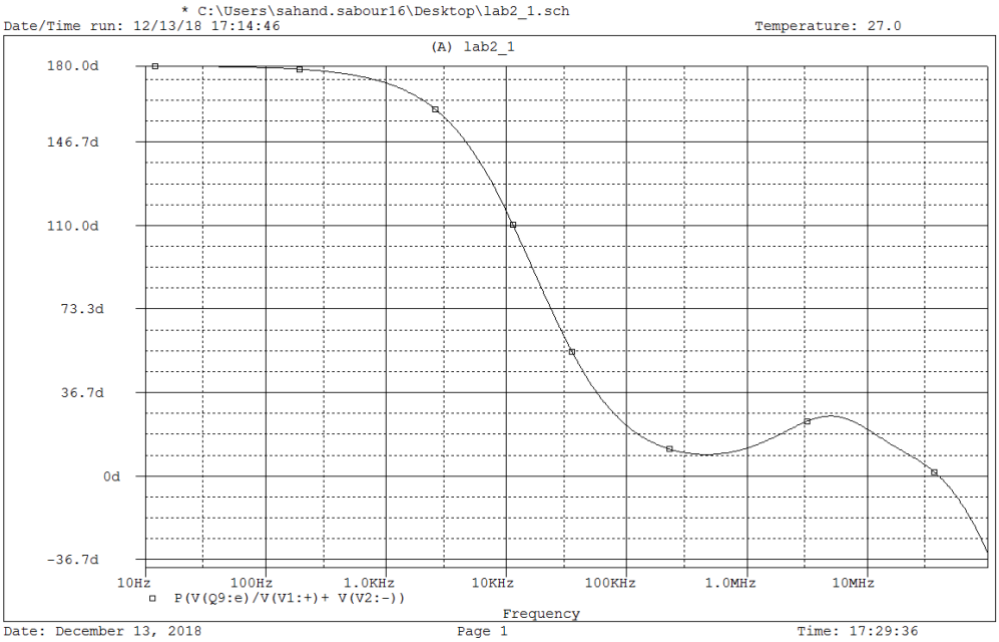

Figure 15: The bode plot for the linear phase

for the op-amp. What can you deduce about the stability of your amplifier from the Bode plots when it is used in a negative feedback circuit? (15%)

In order to obtain the gain magnitude and linear phase graphs for when using a negative feedback circuit, the previous circuit was to be modified. Accordingly, Figure 16 displays the modified circuit.

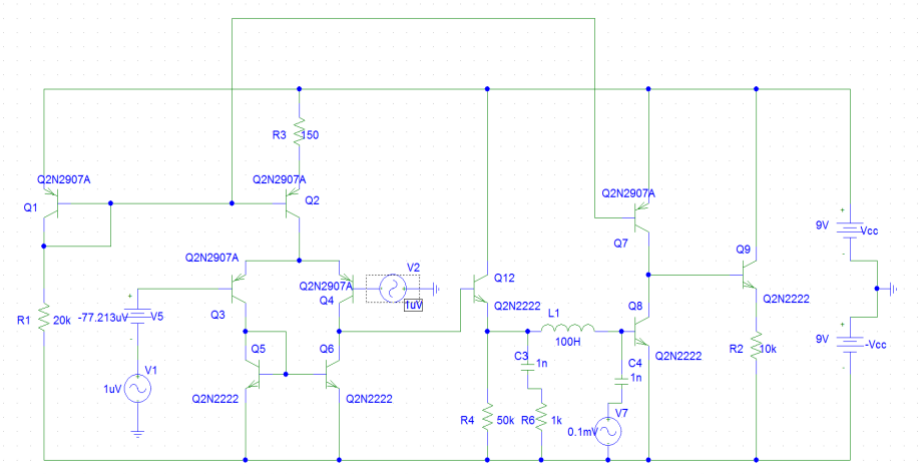

Figure 16: The negative feedback circuit

By simulating the circuit using an AC sweep and adding the previously used traces for gain and phase respectively, the following figures (Figure 17 and Figure 18) were obtained.

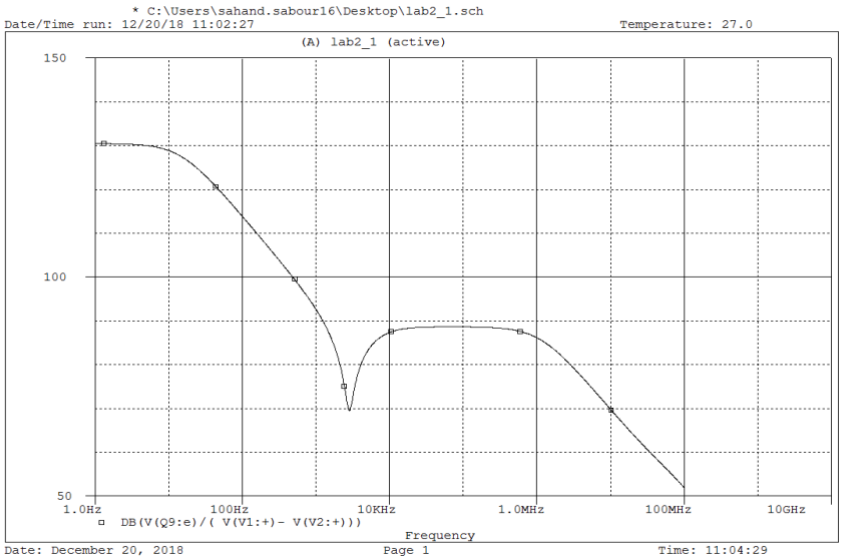

Figure 17: The bode plot for the gain magnitude (in dB)

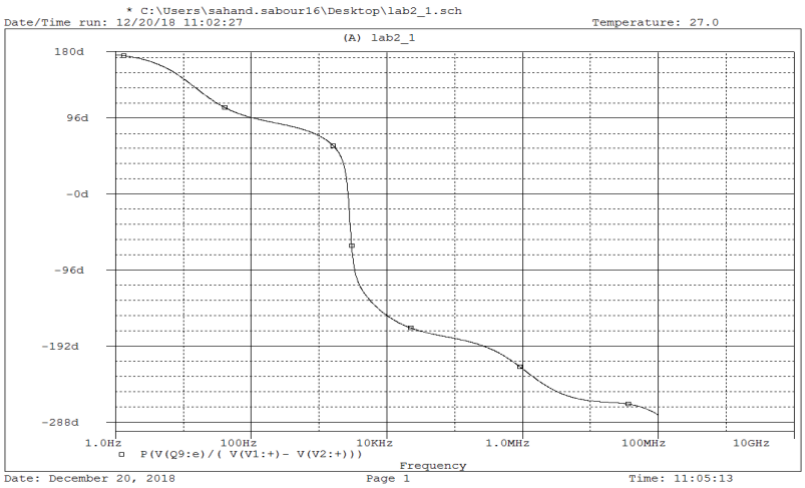

Figure 18: The bode plot for the linear phase

As the comparison between the bode plots for the previous circuit and the bode plots for the modified circuit suggests, the stability of the system is seen to decrease considerably when using a negative feedback circuit. The mentioned assumption was made based on the following factors:

1) By comparing the gain bode plots, it can be noticed that the bandwidth has decreased greatly in the negative feedback circuit. Moreover, the rate of decrease regarding gain is considerably higher in a negative feedback circuit. For instance, in the original circuit, the gain reaches 100 at frequencies less than 100kHz, whereas in the negative feedback circuit, the gain reaches 100 at frequencies less than 10kHz, which indicate 10 times faster decrease when having negative feedback.
2) By comparing the phase bode plots, the changes in the phase can be seen as highly distorted when using negative feedback. Moreover, the rate of this change has also become considerably faster. The mentioned are believed to be signs of instability.

8. *Give your results for the Bode plots obtained with the 'phase compensating capacitor', C_C, added. With reference to these results, comment on how the addition of C_C affects the stability of the op-amp discussed in Question 7. (10%)*

For this section, the previously used circuit was modified and a phase compensating capacitor C_C between the base of Q5 and the emitter of Q7, which resulted in the circuit diagram displayed in Figure 19.

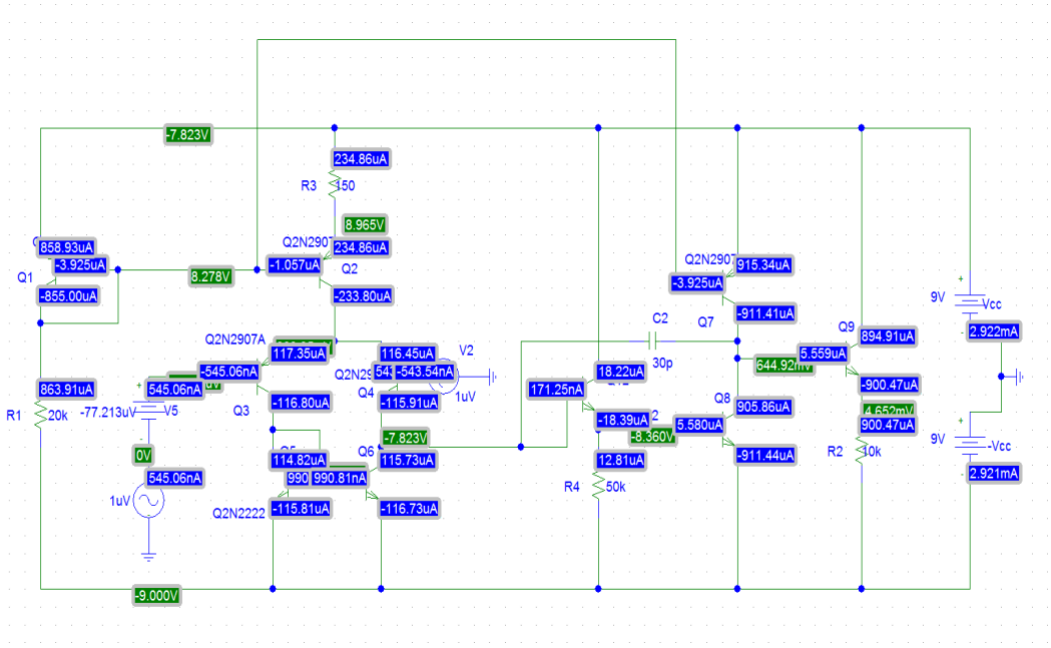

Figure 19: the modified circuit with C_C

By simulating the newly modified circuit and adding the traces, which were used in the previous section, the following two graphs (Figure 20 and Figure 21) were obtained as the gain magnitude and linear phase graph respectively.

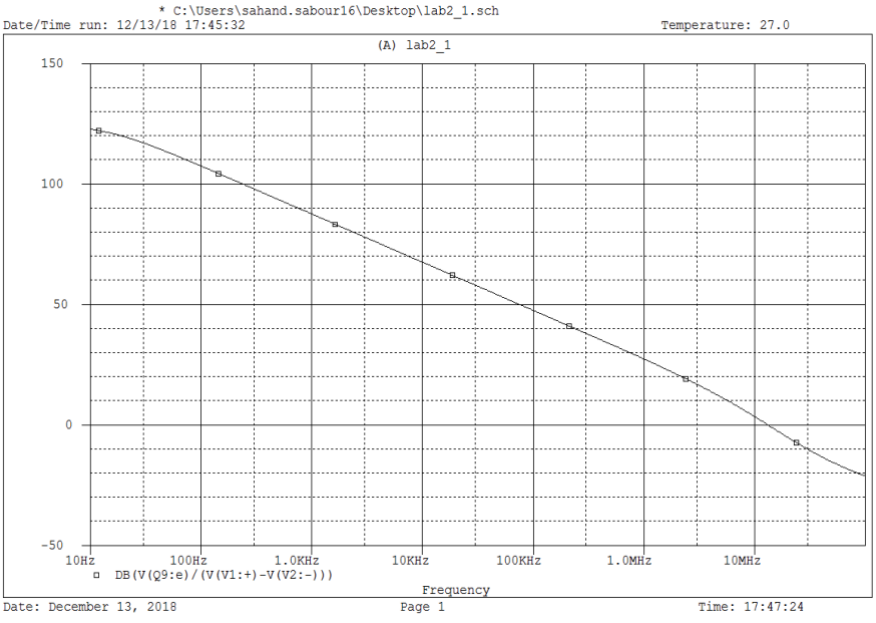

Figure 20: The bode plot for the gain magnitude (in dB)

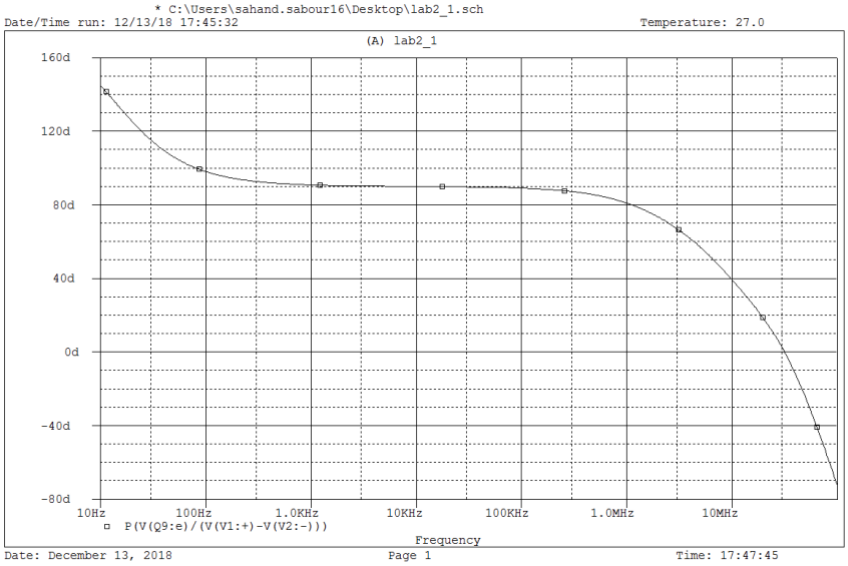

Figure 21: The bode plot for the linear phase

By comparing the obtained graphs in this section with the previous section's graphs, it can be noticed that after adding the phase compensating capacitor C_C, the stability of the system has improved considerably. This can be noticed for frequencies near 10Hz, where the magnitude starts to change compared to the previous stage, where the magnitude change started from frequencies of approximately 1kHz. Moreover, the changes in the phase have become considerably less apparent compared to the previous sections' obtained phase graph.