EEE205 Altera Lab

Digital Electronics II

Name: Sahand Sabour

Student ID: 1614650

Submission Date: 2018/12/05

Submission Deadline: 2018/12/06

Altera Experiment Report

Table of contents

Introduction

Programmable Logic Devices (PLDs) have gained an important role in digital electronics as they can be used to implement both combinational and sequential logic circuits. These devices are programmable and their implemented logic could be modified by hardware description languages, such as AHDL. In this experiment, the students were provided with an FPGA development board (DE1) and were required to complete sections of the issued lab manual. This was believed to familiarize students with the teaching material and also introduce them to a considerably important component of digital electronics, which is Field Programmable Gate Array (FPGA) and its implementation.

The apparatus used for conducting this experiment consisted of an ALTERA board, its USB cable and a computer system that had Quartes II software pre-installed. Each section of this experiment was completed by using the mentioned apparatus and occasional checks of the obtained results by the teaching assistants who were present at the lab session.

Experiment procedure

Section 1: the dec7448 design

After creating a new project for dec7448, as instructed, a Block Diagram/ Schematic File (saved as dec7448.bdf) was created. Accordingly, the graphics editor window was used in order to emulate a 7448, whose symbol exists in the primitive symbols section (in the mentioned file). Furthermore, this window was also used in order to add VCC, input and output symbols to the design. After connecting the inputs and outputs to the assigned pins and renaming each of the inputs and outputs to the provided names, the design was compiled in order to guarantee its correctness. The following figures (Figure 1 and Figure 2) show the mentioned design and the compilation message respectively.

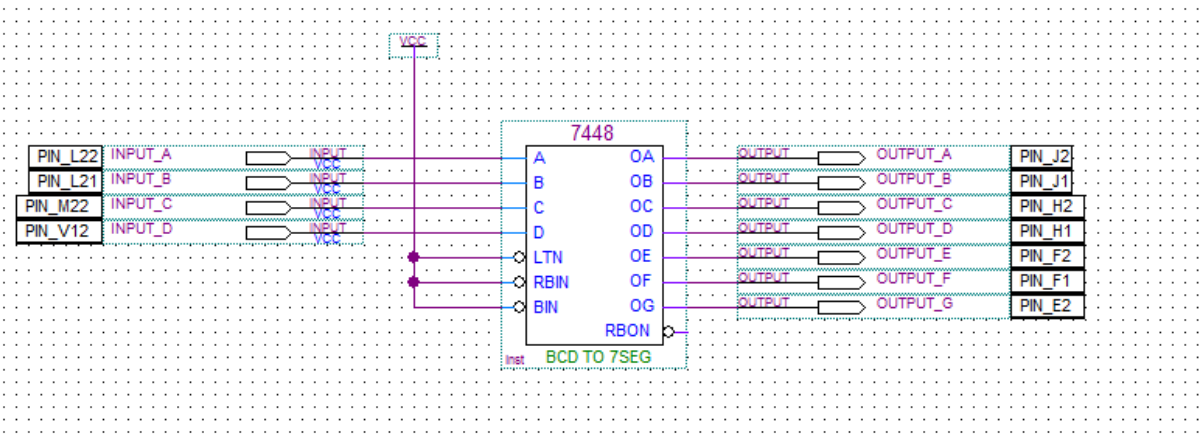

Figure 1: The design in Section 2.3

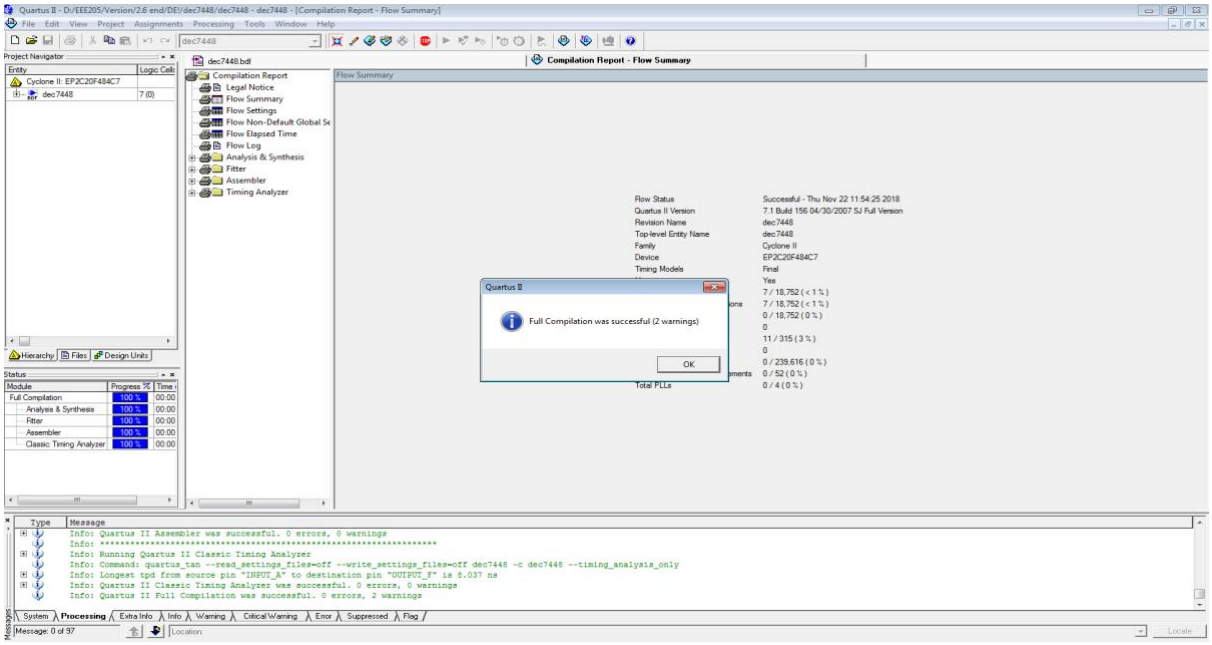

Figure 2: The compilation result for Section 2.3

As provided in the lab manual, an incorrect design was also required to be assembled and complied. It is believed that the reason for doing so was for the students to achieve an understanding of compilation errors. Therefore, an extra output symbol with a duplicate name was added to the design without it being connected to any of the pins (Figure 3). After compiling this design, a message informing the user that the compilation was not successful was displayed (Figure 4). This error was due to use of an output with a duplicate name (OUTPUT_G).

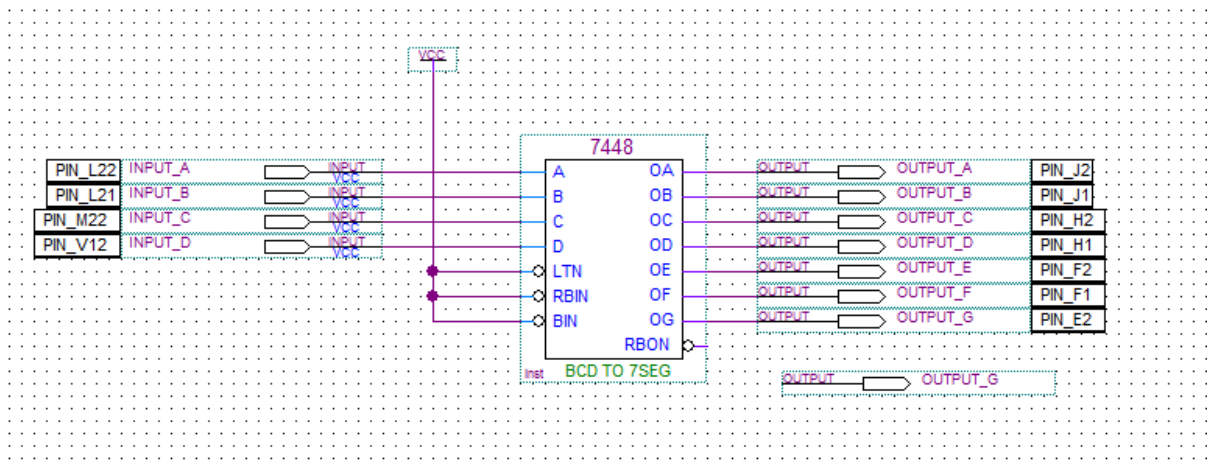

Figure 3: The design in Section 2.4

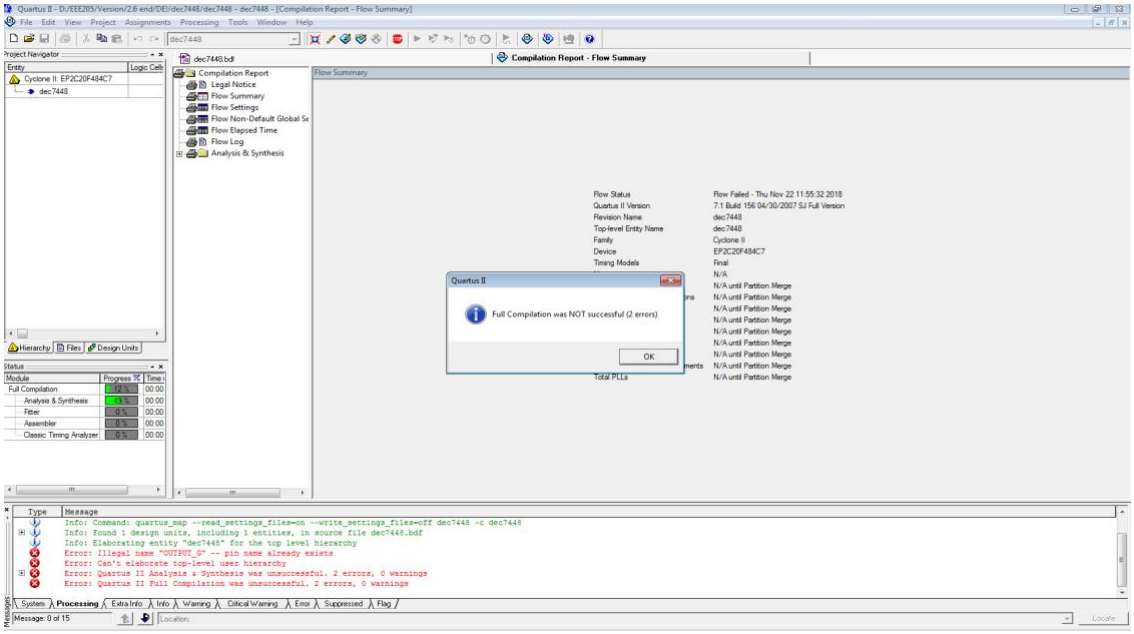

Figure 4: The compilation result for Section 2.4

To analyze the design's characteristics, a Vector Waveform File (dec7448.vmf) was to be created and simulated accordingly. Therefore, the .vmf file was created and drawn as it was required in the lab manual (regarding the mentioned End Time, Grid Size and given signals for inputs A-D). By simulating the mentioned .vmf file, the following figure (Figure 5) was obtained and recorded.

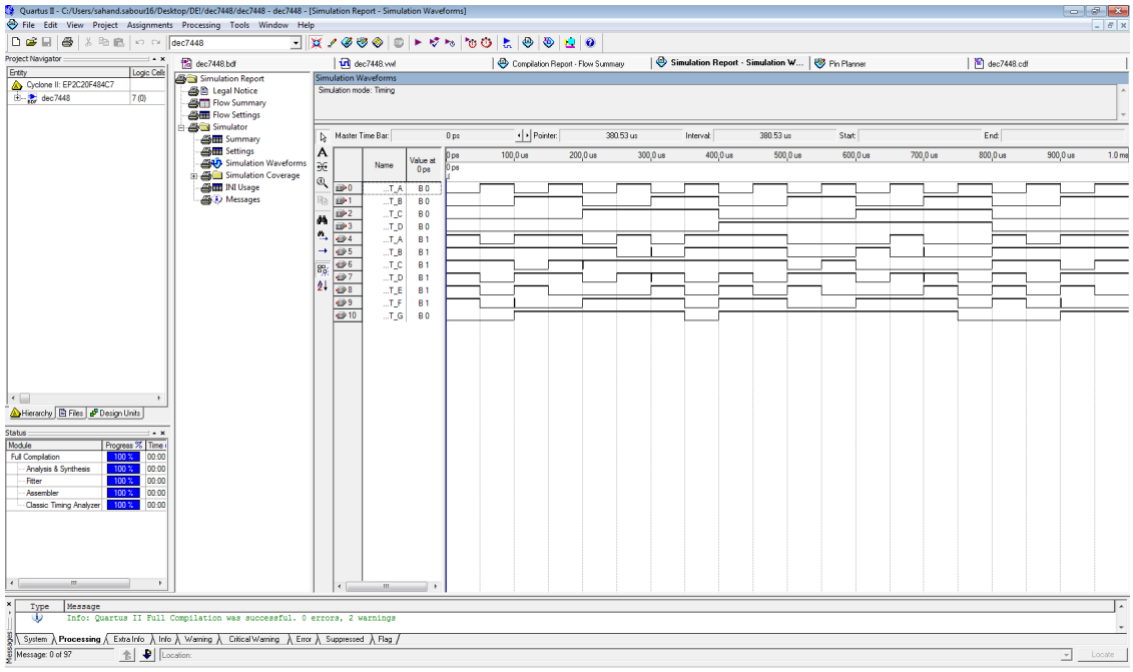

Figure 5: The simulation waveform in Section 2.6

After achieving a successful compilation and displaying the simulation, the process would reach the pre-programming stage. Before programming the provided ALTERA board, it was

required to assign a pin to each of the inputs and outputs of the design. In that case, the role of each pin would be defined for the board. Therefore, the pin planner tool of the software was used in order to proceed with this stage. The pin assignments were as follows:

INPUTS:

INPUT_A ==> PIN_L22 INPUT_B ==> PIN_L21 INPUT_C ==> PIN_M22

INPUT_D ==> PIN_V12

OUTPUTS:

OUTPUT_A ==> PIN_J2 OUTPUT_B ==> PIN_J1 OUTPUT_C ==> PIN_H2

OUTPUT_D ==> PIN_H1 OUTPUT_E ==> PIN_F2 OUTPUT_F ==> PIN_F1

OUTPUT_G ==> PIN_E2

Furthermore, as a Low-level voltage causes each segment to light up, the inversion for each of the output ports (OA-OG) of the 7448 was changed from 'None' to 'All' to invert all the output ports. The following design in Figure 6 was obtained as the result of the mentioned modifications.

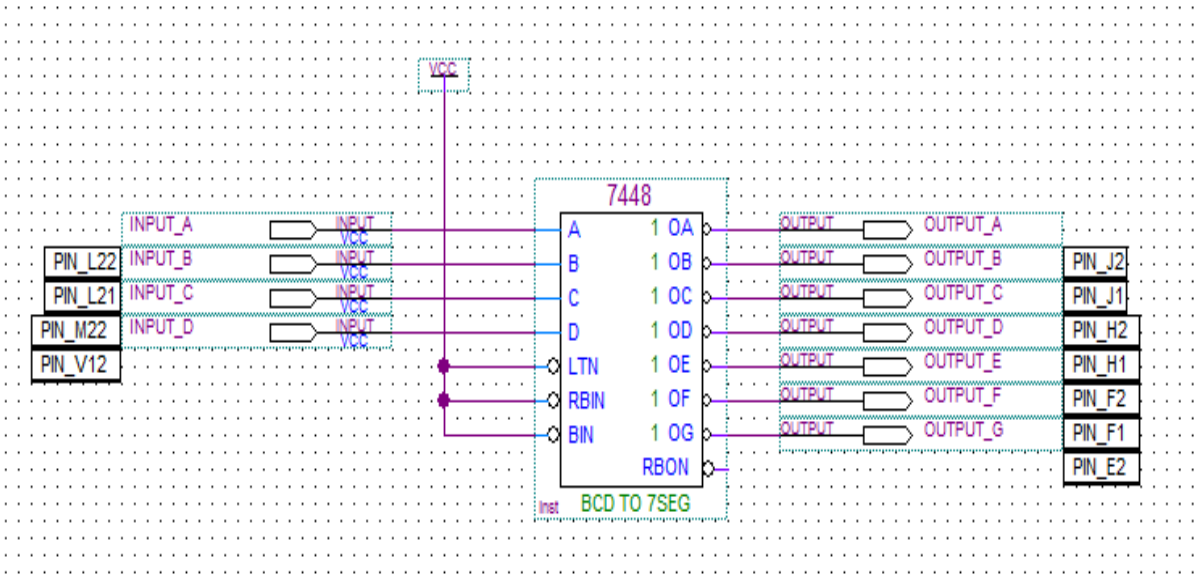

Figure 6: The modified design in Section 2.7

Additionally, the design was compiled and simulated to display that it is working properly and the following figure (Figure 7) was obtained as the result of the simulation:

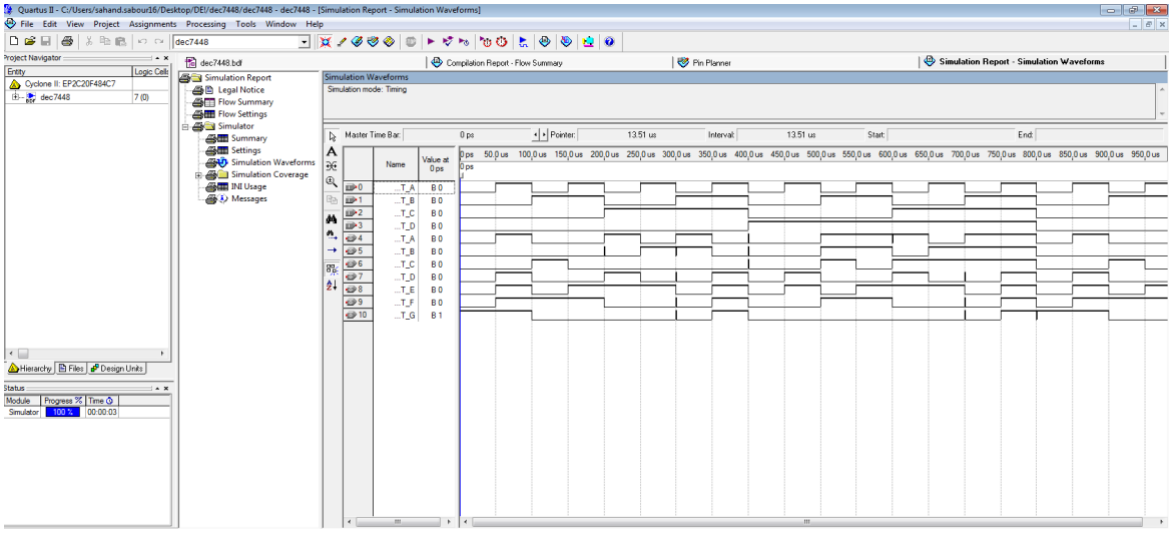

Figure 7: The re-simulation in Section 2.7

Furthermore, the following figures were collectively recorded as the sixteen possible combinations on the ALTERA board were tested (Figure 8). As seen in the figure, only digits 1-9 were displayed correctly on the board and the counter would become distorted after counting to 9. This is due to the fact that the current design relates to a decade decoder and as the name suggests, it can only display 10 consecutive digits (0-9).

Figure 8: results shown on ALTERA board in Section 2.7

Section 2: AHDL combinational design (using 7 segment decoder)

After creating a new project for the 7-segment decoder and the corresponding .bdf file, since the design depended on a 7-segment decoder, the mentioned decoder was required to be created and programmed in AHDL. Therefore, an AHDL file (.tdf file) was created in order to

write the AHDL code for the decoder. It should be noted that using the same name for both the .bdf and .tdf files would cause problems in the compilation and simulation stages. Therefore, extra attention should be paid when choosing names for the project files. Accordingly, with the aid of the help feature in the software, 7segment.tdf was created and is shown in Figure below (Figure 9).

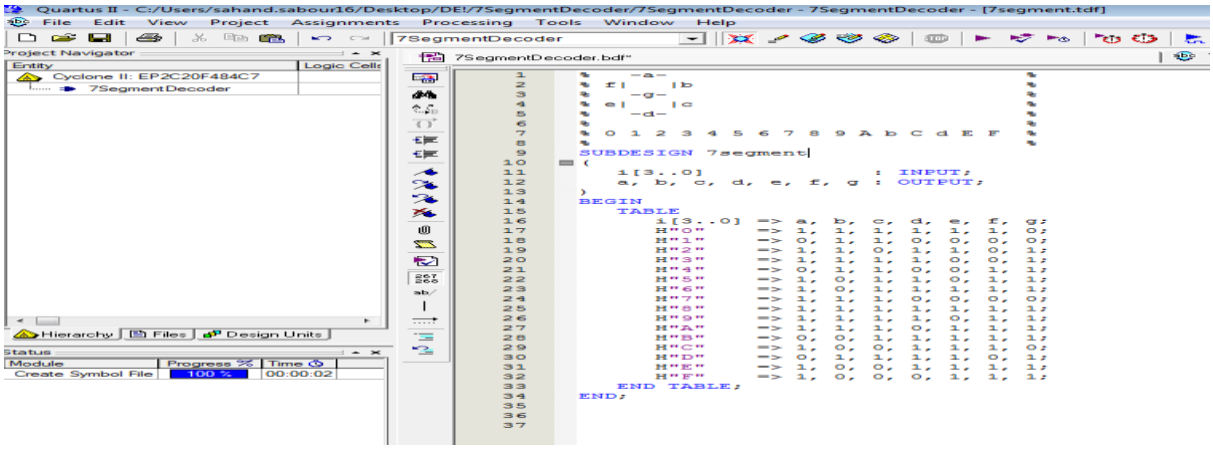

Figure 9: The 7segment.tdf of Section 3.9

Following the previous step, the AHDL file was used in order to create a symbol that can be used in the design (using the Create Symbol Files for Current File option). Subsequently, with respect to adding the decoder symbol to the design and similar to the previous section, input and output symbols were added to the design and were connected to the decoder pins correspondingly. However, since the ports were not inverted, compared to the previous section, an inverter (NOT symbol) was added between each output port and output symbol. Figure 10 displays the resulting design.

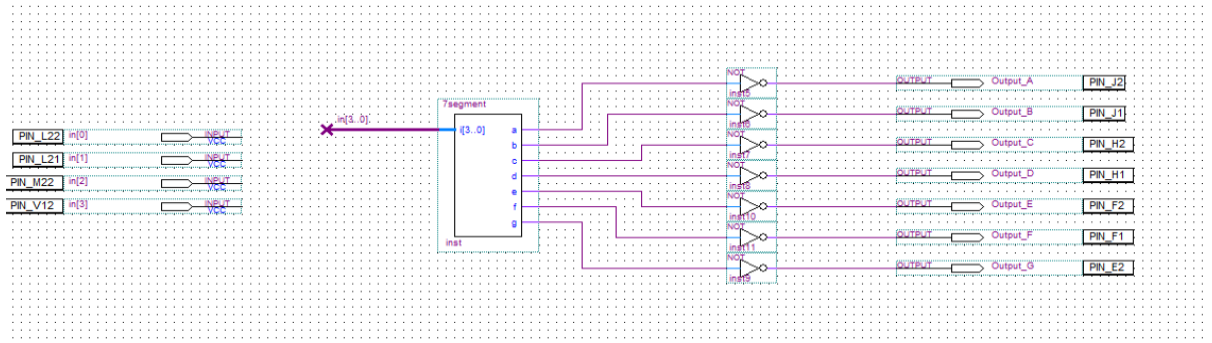

Figure 10: The hexdec.bdf of Section 3.9

It should be noted that, due to the fact that the 4 bits in the input of the 7segment are inseparable, the inputs could not be connected to their corresponding port respectively and therefore, are disconnected completely from the 7segment in the figure above.

This design was compiled and simulated consequently and the following figure (Figure 11) displays the result of the mentioned simulation. As for the 4-bit input signal, hexadecimal values varying from 0-F (0-9 and A-F) were generated.

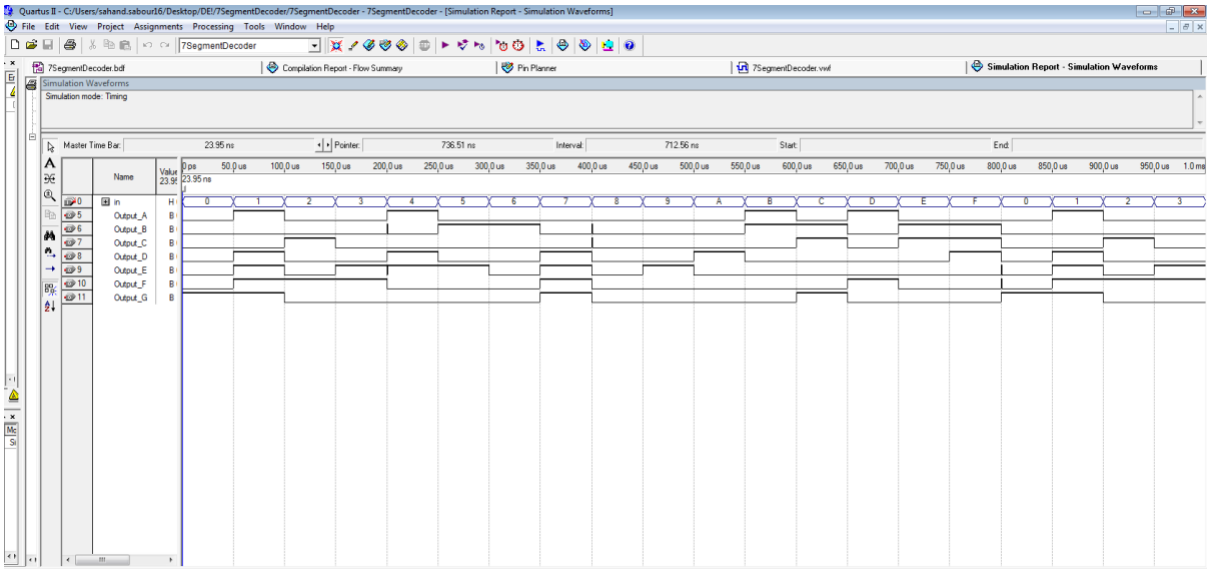

Figure 11: The simulation of hexdex in Section 3.9

Since the compilation and the simulation were both successful, it was allowed for the pins to be assigned to the corresponding port on the pin planner window. The ALTERA board was programmed accordingly. It should be noted that the pin assignments for this section were set to be similar to the previous section. The following figure (Figure 12) displays all of the sixteen possible outputs for the LED segments collectively.

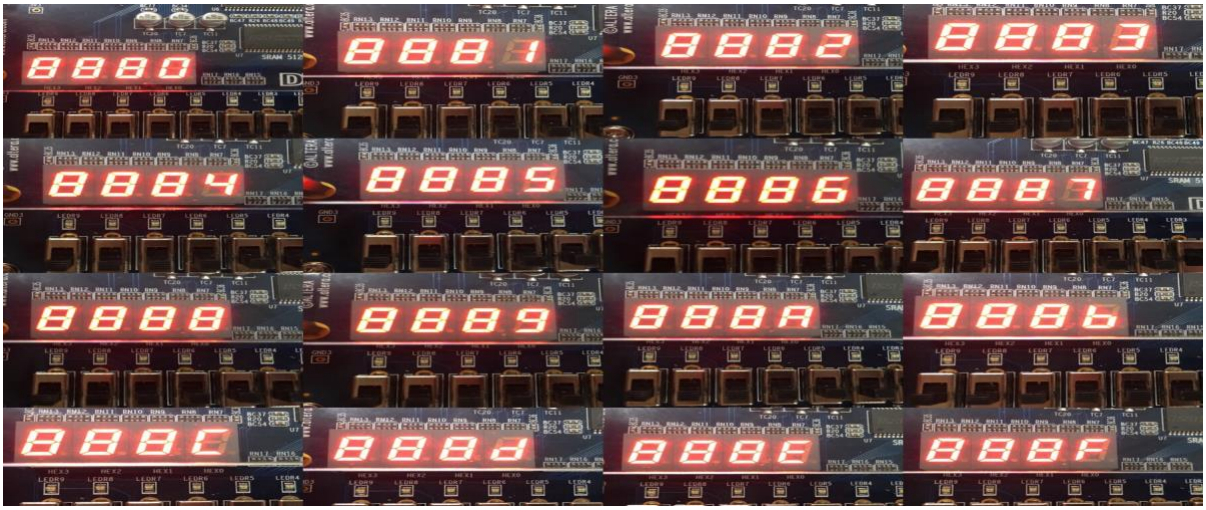

Figure 12: results shown on ALTERA board in Section 3.9

This decoder is believed to be an improvement to the decoder that was implemented in the previous section as it does not possess the same distortions. As can be seen in the figure above, the decoder can successfully display all of the sixteen possible outcomes that is required from the design and therefore, it can be considered as a successful implementation.

Section 3: AHDL sequential design (using counters)

For the first step of the design regarding this section of the experiment, a decade counter was required to be defined. Therefore, the dec_count.tdf file was created and made to a symbol so that it could be implemented in the block diagram. Figure 13 displays the content of the mentioned AHDL file.

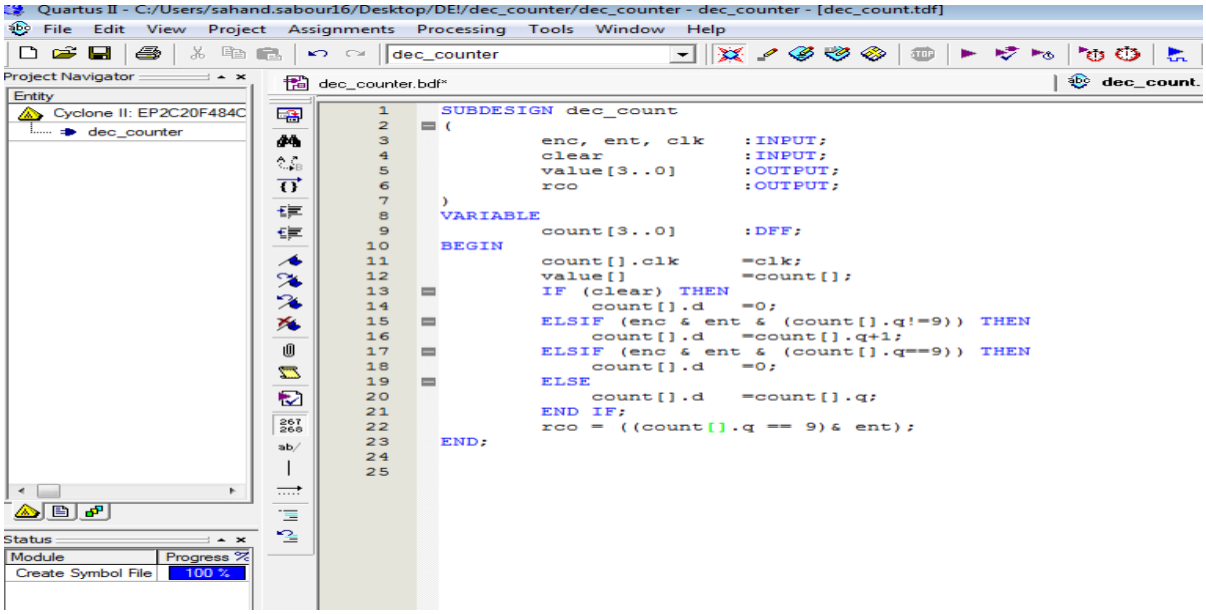

Figure 13: The dec_count in Section 4.3

Subsequently, the newly created symbol for the dec_count, alongside input and output symbols corresponding to inputs and outputs provided in the lab manual, was implemented to create the appropriate design for this section (Figure 14).

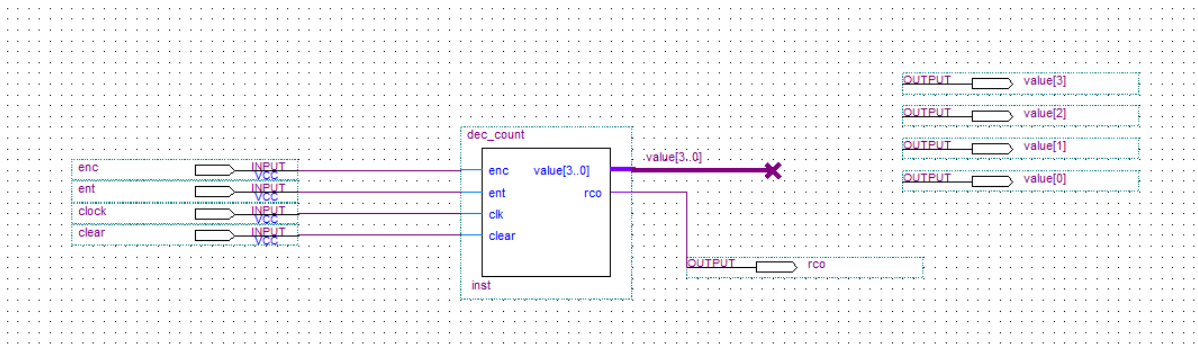

Figure 14: The bdf file in Section 4.3

Since, the 4 bits in the output of the dec_count are inseparable, there would not be 4 separate output ports for this counter. As a result, the outputs cannot be connected to their corresponding port respectively and therefore, are completely disconnect in the design shown in figure 14.

With successful implementation of the symbols and completing the design, the project has to be both complied and simulated to prevent any errors that might occur during this part of the process. The figure below (Figure 15) was obtained from the design simulation.

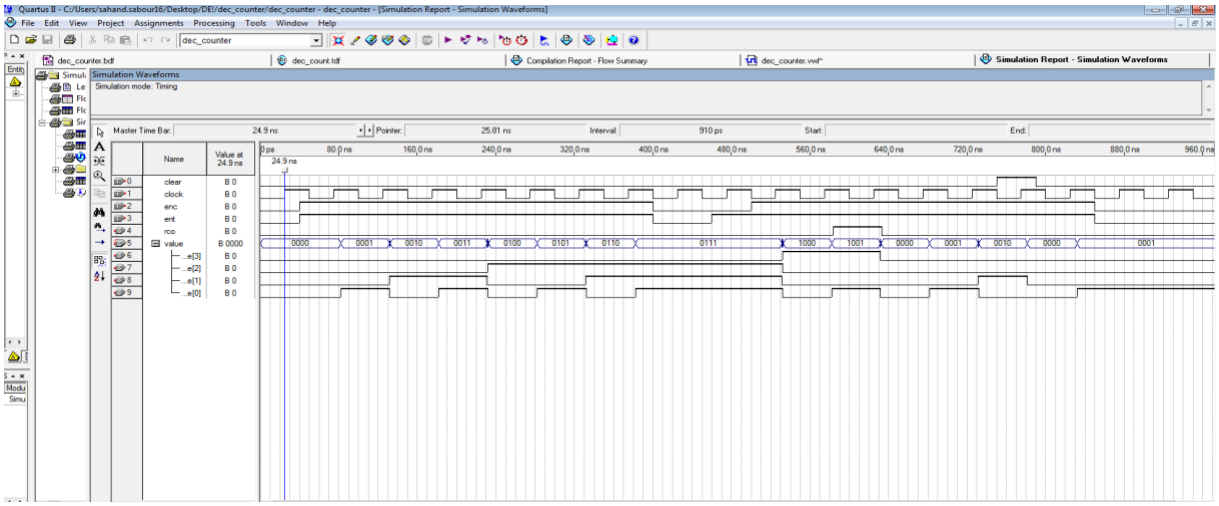

Figure 15: The simulation file in Section 4.3

In order to modify this design, as suggested by the lab manual, a second counter was to be added. Therefore, the corresponding AHDL code for this counter was written (Figure 16) and the symbol regarding this counter was created accordingly. It should be noted that initially, the value used for the counter's limit was set to be 27000000 and therefore, 27 bits were used for D flip-flop. However, this was persumably a rather large number for the simulation and therefore, was decreased to 5. Consequently, the number of bits for D flip-flop was also decreased ([25..0] to [2..0] or from 26 bits to 3 bits, since decimal 5 can be shown by using merely three binary digits).

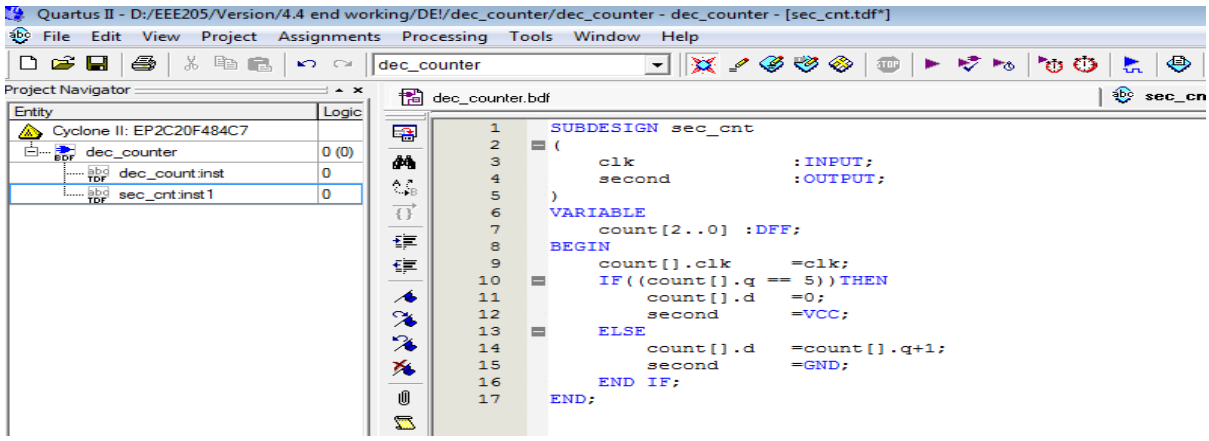

Figure 16: The sec_cnt file in Section 4.4

As the second counter's symbol had been made available, it was implemented in the design to produce the following modified block diagram (Figure 17).

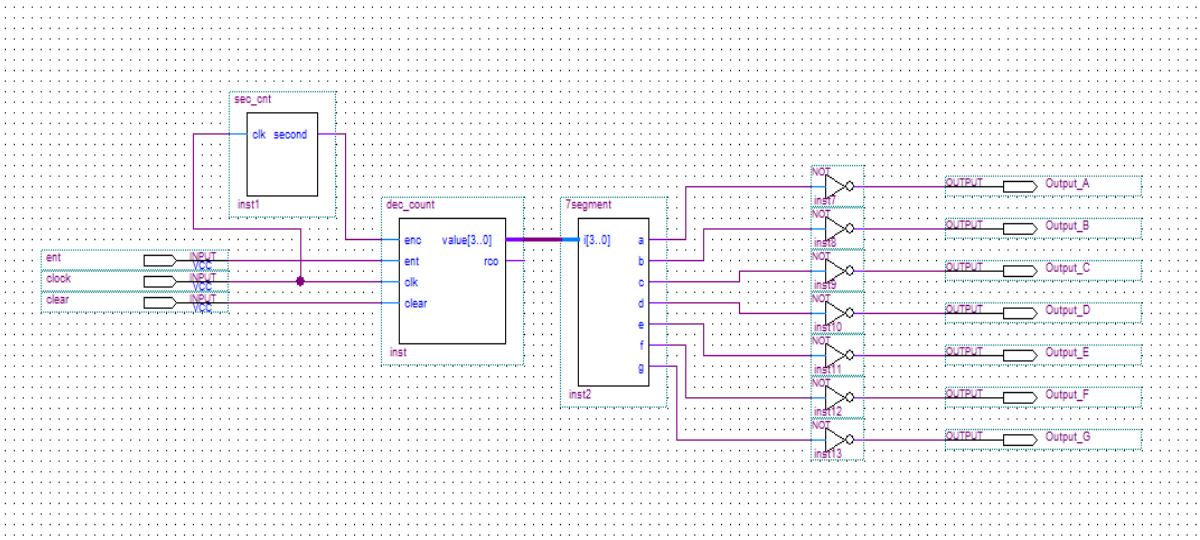

Figure 17: The bdf file in Section 4.4

In order for the proper functioning of the design to be approved, it had to be compiled and simulated. The result of the simulation is displayed in the following figure (Figure 18).

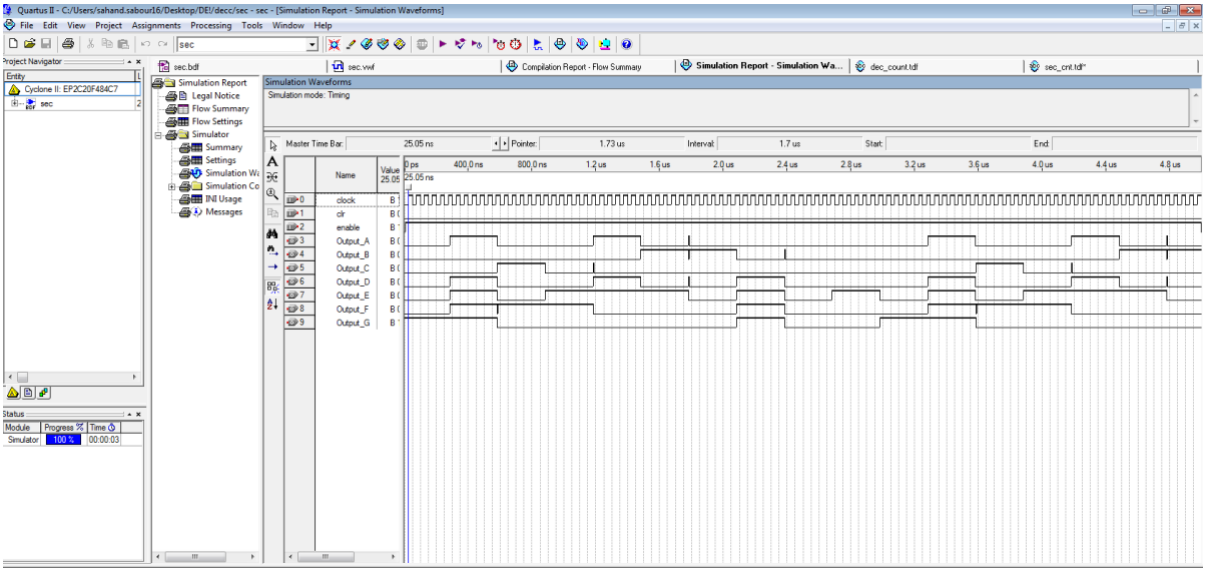

Figure 18: The simulation waveform of Section 4.4

After assigning the pins via the pin planner feature, the provided ALTERA board was programmed. It was witnessed that the after flipping the first switch, the first display starts counting from zero, with increments of one unit, until nine. Subsequently, after the counter displayed '9', it was reset to '0'.

Section 4: Bonus (divide-by-12 counter)

As the bonus part for this experiment, a divide-by-12 counter using two 7 segment decoders was to be designed. Since the components for this design were all already made available due to the completion of the previous sections, creating more symbols was not considered as a necessity in this section of the experiment.

```
SUBDESIGN dec_count
(
    enc, ent, clk : INPUT;
    clear : INPUT;
    value[3..0] : OUTPUT;
    rco : OUTPUT;
)
VARIABLE
    count[3..0] : DFF;
BEGIN
    count[].clk = clk;
    value[] = count[];
    IF (clear) THEN
        count[].d = 0;
    ELSIF (enc & ent & (count[].q != 11)) THEN
        count[].d = count[].q + 1;
    ELSIF (enc & ent & (count[].q == 11)) THEN
        count[].d = 0;
    ELSE
        count[].d = count[].q;
    END IF;
    rco = ((count[].q == 11) & ent);
END;
```

Figure 19: divide-by-12 counter AHDL code

However, the AHDL code for the counter was to be modified. The modification could be easily achieved by changing '9' in the code to '11' in the statements that 'q == 9' is used (Figure 19). This change in the value of q resets the counter every after eleven increments rather than nine, which is what is required by a divide-by-12 counter. Consequently, the newly obtained symbol was implemented in the circuit design in order to create a divide-by-12 counter circuit. Figure 20 was obtained as the design for the mentioned counter, based on the given requirements.

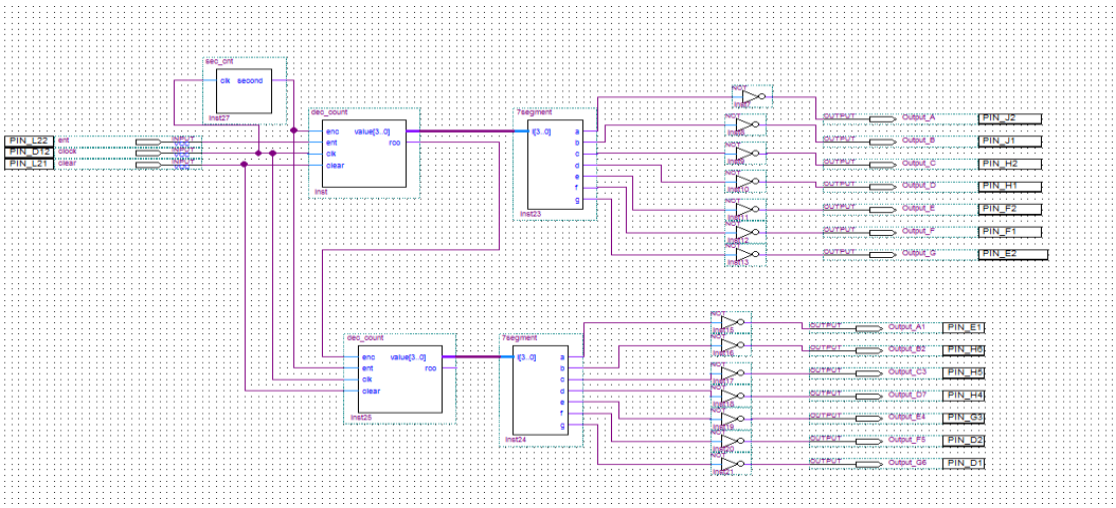

Figure 20: The bdf file for the divide-by-12 counter

After programming the ALTERA board, the board initiated counting from 00 until bb (where b is the hexadecimal for '11'), which corresponds to the result of a divide-by-12 counter on two seven segments. Therefore, it could be concluded that the counter was functioning properly.

Conclusion

Achievements

It is believed that after conducting this experiment, valuable knowledge regarding the QUARTUS II software, ALTERA boards and many aspects that were introduced in the lab manual was obtained. Moreover, it is also believed that by conducting this experiment, deeper understanding of the lecture materials, which were taught in the EEE205 module, was achieved. The ability to write and assess AHDL codes, as well as designing circuit units such as decoders and counters while analyzing the mentioned designs, was improved likewise.

Possible changes

The computers in the provided computer laboratory rooms were mostly in a critical condition. Some of the systems were not functioning properly. Moreover, as it is believed that the provided systems were overly outdated, which delayed the data processing actions regarding compilation and simulation features that were used quite frequently in this experiment.

Suggestions

It is suggested that the computer systems in the lab would be checked for malfunctions regularly, as they have an essential role in this experiment. Frequent improvements to the lab manual are also suggested to be considered. The number of teaching assistant present in the lab session could be increased likewise, as it was noticed that two teaching assistants per classroom may not be sufficient.

Comments

In conclusion, it is believed that this experiment was a highly valuable experience. It is also believed that with the implementation of the mentioned suggestions, this experiment could be improved greatly. Consequently, considerable improvement in the experiment procedure could positively affect both XJTLU students and the staff.

References

[1] *EEE205 Lab Altera Experiment*, 4 ed., Xi'an Jiaotong Liverpool University, Department of Electrical and Electronic Engineering, Suzhou, 2008