Xi'an JIAOTONG-LIVERPOOL UNIVERSITY

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COURSEWORK SUBMISSION COVER SHEET

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Contents

Abstract

MOSFETs play an important role in today's world of electronics and electrical engineering. In this design project, students were asked to design a n-channel MOSFET IC circuit according to the logic circuit that they were provided with. In this report, firstly a brief introduction of this project as well as a short explanation of the given problem (problem statement) is provided. Following the introduction, the fabrication process that is required for this design is explained in details. The layout rules and regulations relating to this design are also added likewise. After explaining the fabrication process, the required truth tables and calculations regarding the aspect ratios and size of the chips in the design is shown respectively. Consequently, the obtained results and illustrated designs as well as different possible cases for the design are mentioned and discussed. Following the discussion, a brief conclusion of the project is provided. In this section, comments and suggestions regarding this project were added likewise. In conclusion, it is believed that this project was considered as a valuable learning experience and it can be mentioned that all of the required aims and objectives regarding this project were successfully achieved.

Introduction

A metal oxide semiconductor field effect transistor (MOSFET) is mainly constructed by controlled oxidation of silicon. MOSFETs play an essential role in the current generation of circuitry and examples of their applications can be seen in various high voltage controlling devices.

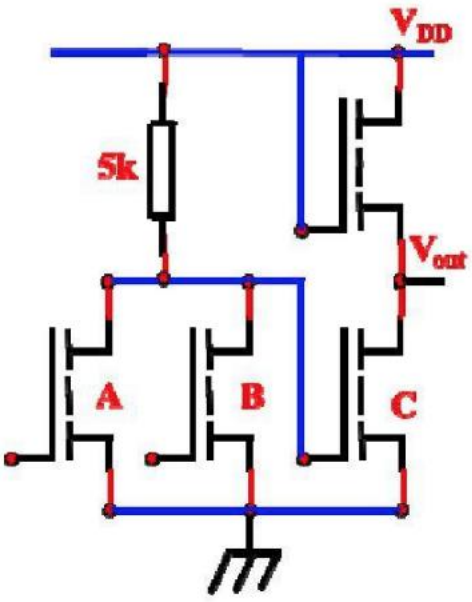

Figure 1: The IC circuit's logic circuit

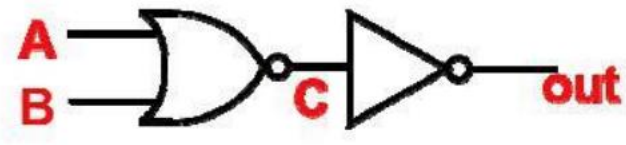

Figure 2: The IC circuit's logic symbol

In this experiment, we are required to design an integrated circuit regarding a n-channel MOSFET (nMOS) according to the given logic circuit (Figure 1) and symbol (Figure 2). Moreover, the design is required to obey the provided rules and regulations and the given criteria, which are included in the design section. Furthermore, the design is expected to present a rather minimized and efficient solution.

Fabrication process

The process of fabricating the required nMOS IC circuit includes a number of various steps and applies four masks in total. Each step is briefly explained and shown respectively below:

1) **Attain a Si Substrate (P):** This is the Substrate that we would use as our base for the first mask; the active region mask (Figure 3).

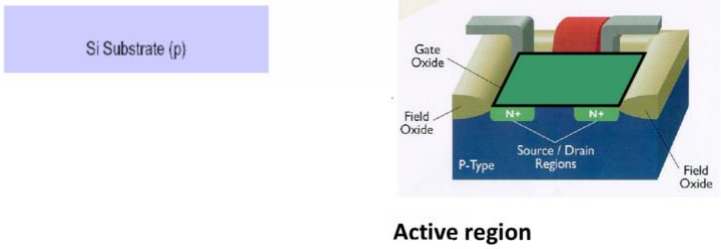

Figure 3: the Si Substrate

2) **Applying mask 1:** First, we apply a layer of SiO2 Field Oxide (Thick Oxide) on the given substrate. This is the first oxidation (Layering) of the fabrication process and the applied layer would be referred to as Oxide 1. Then, we would do the Oxide etching (patterning) to implement the first mask; the active region mask (Figure 4).

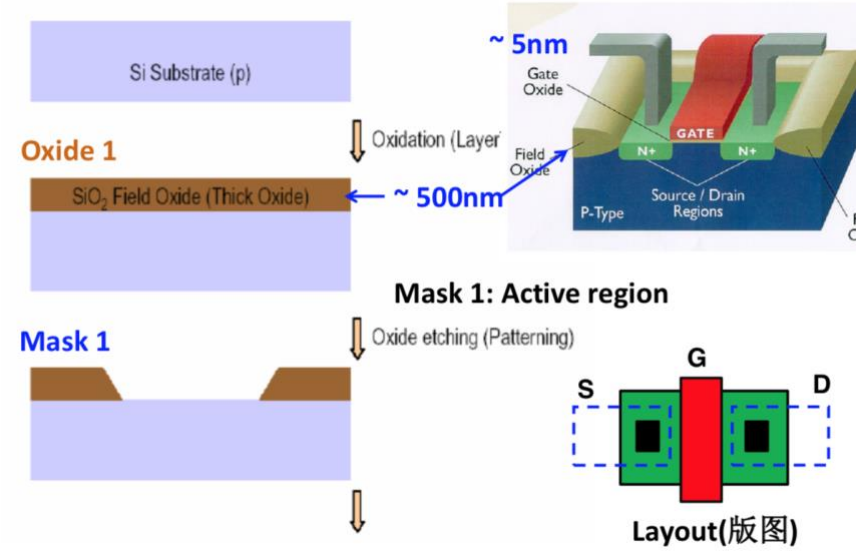

Figure 4: Oxidation (Layering) and Oxide etching process

3) **Applying mask 2:** As the first stage, a layer of SiO2 gate oxide (thin oxide) is applied and referred to as Oxide 2. This stage is the oxidation (layering) stage. Consequently, the mentioned layer is covered by a layer of polysilicon, referred to as Oxide 3. As the final step, we need to proceed with polysilicon etching and pattern the polysilicon to form the second mask; gate stripe mask, similar to shown in the figure (Figure 5)

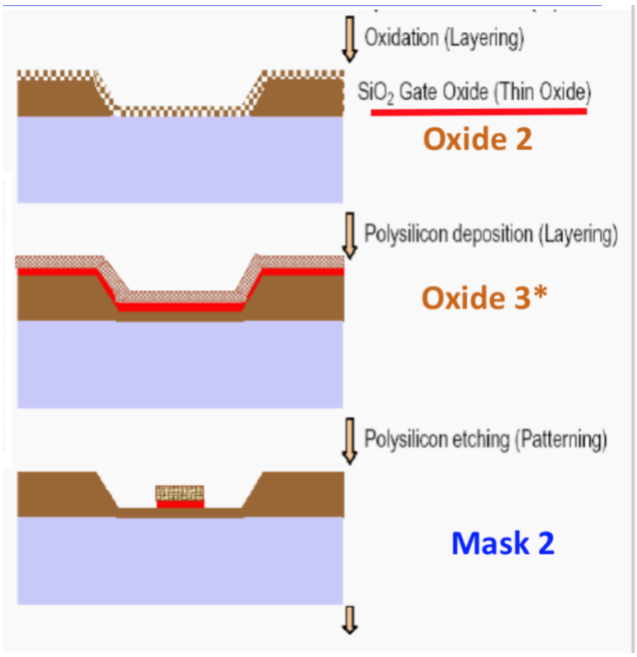

Figure 5: Oxidation, polysilicon deposition and etching process

4) **Applying Mask 3:** Initially, we use oxide etching (patterning) to remove the remaining polysilicon layer. Consequently, we would proceed with doping using n-type materials. This stage of the process is known as the ion implementation. After the doping stage is completed, a layer of SiO2 insulated oxide (Oxide 4) would be applied (Figure 6).

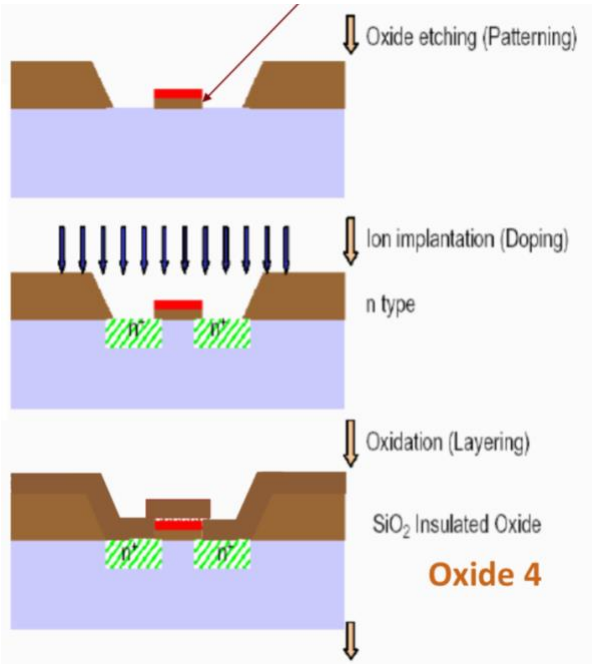

Figure 6: Oxide patterning, ion implementation and layering process

As mask 3 refers to the contacts mask, we implement an oxide etching (patterning) in order to fabricate the required contact windows (Figure 7).

5) **Applying Mask 4:** Metal mask, referred to as Mask 4, is the final mask to be implemented. Therefore, a layer of metal, Al evaporation, would be added (metal deposition) and then, it would be patterned, in a stage known as metal etching, to present Mask4 (Figure 7).

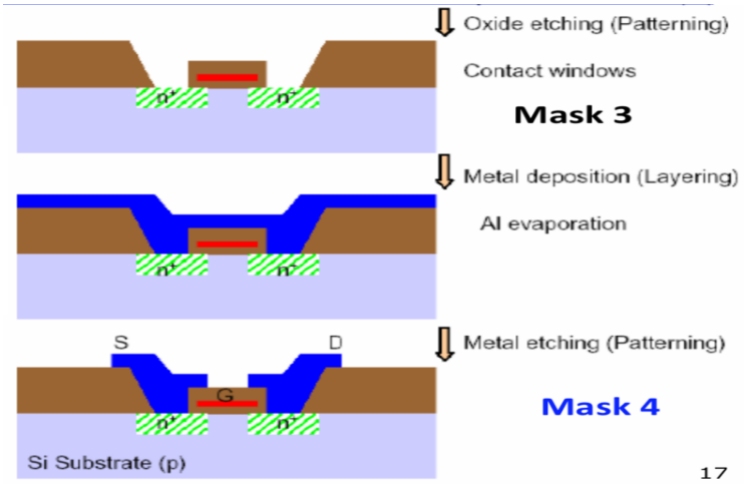

Figure 7: Oxide etching along with metal deposition and etching

The following is the summary of the explanation provided above:
First, a clean slice of silicon is oxidized (Oxide 1) and then Mask 1 is applied to open a window in the oxide. Then, the silicon slice is oxidized again (Oxide 2) and following the second oxide, a layer of polycrystalline silicon covers the full slice. Consequently, mask 2 is fabricated by photoengraving the mentioned oxide and polysilicon layers. The oxide and drain regions are removed likewise as the next step of the fabrication process. Then, a layer of oxide (Oxide 4) would be applied to cover the surface and mask 3 is applied afterwards (Opening holes). For Mask 4, which is the metal mask, the surface is covered with aluminum and the evaporated aluminum is covered with photoresist afterwards. Consequently, mask 4 is the aluminum layer patterned with respect to conductor pattern shapes.

For designing this nMOS IC circuit, there are a set of rules and regulations which provide us with certain limits regarding the implemented spacings in our design. Below is the complete list of all the measurements required for this experiment's design (Figure 8):

MOSIS Layout Design Rules

Active Area Rules

R1	Minimum Active area Width	3λ
R2	Minimum Active area Spacing	3λ

Poly-Silicon Rules

R3	Minimum Poly Width	2λ
R4	Minimum Poly Spacing	2λ
R5	Minimum Gate extension of Poly over Active	2λ
R6	Minimum Poly-Active Edge Spacing (Poly Outside of Active area)	λ
R7	Minimum Poly-Active Edge Spacing (Poly Inside of Active area)	3λ

Metal Rules

R8	Minimum Metal Width	3λ
R9	Minimum Metal Spacing	3λ

Contact Rules

R10	Poly Contact size	2λ
R11	Minimum Poly Contact Spacing	2λ
R12	Minimum Poly Contact to Poly Edge Spacing	λ
R13	Minimum Poly Contact to Metal Edge Spacing	λ
R14	Minimum Poly Contact to Active Edge Spacing	3λ
R15	Active Contact size	2λ
R16	Minimum Active Contact Spacing (On the same Active region)	2λ
R17	Minimum Active Contact to Active Edge Spacing	λ
R18	Minimum Active Contact to Metal Edge Spacing	λ
R19	Minimum Active Contact to Poly Edge Spacing	2λ
R20	Minimum Active Contact Spacing (On different Active regions)	6λ

Supply Rail Metal

R21	V_{DD}	>3λ
R22	Ground	>3λ

Resistor Rules

R23	Minimum resistor width	2λ

Figure 8: nMOS design rules

Design

The required circuit consists of a NOR gate followed by a NOT gate (inverter). The following truth table contains the expected results for the mentioned gates.

A	B	C	OUT
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Normalized Device Constant β_0	1.8×10^{-4} A/V^2
Threshold Voltage V_T	0.3 V
Supply Voltage V_{DD}	5 V
High Input Voltages (A and B) V_{IN}	V_{DD}
Low Input Voltages (A and B) V_{IN}	0 V
MOSFET Load Resistance R_L	5 kΩ
Sheet Resistance R_S	100 Ω/□

Figure 9: the given process parameters

Furthermore, there are 3 aspect ratios (W/L) that we need to calculate in order to accurately design the nMOS IC. The provided values to be used in this design are given in Figure 9. The following are the necessary calculations to obtain the required measures:

If $V_A = V_B = V_{DD}$, let Vout = 0.1V << V_T, then in the potential divider we get:

$\frac{0.5\,R_D}{0.5\,R_D+R_L} = \frac{V_{out}}{V_{DD}} = \frac{0.1}{5} = 0.02$, which gives $R_D \approx 200\Omega$ (1)

(Note that since A and B are parallel, the equivalent resistant for the combination of A and B is $\frac{R_D * R_D}{R_D+R_D} = 0.5\,R_D$)

Since we have that $I_D = \frac{\beta[(V_G-V_T)V_D-V_D^2]}{2} \approx \beta[(V_G - V_T)]$, we can say that

$R_D = \frac{V_{Out}}{I_D} = \frac{1}{\beta[(V_G-V_T)]}$ and therefore $200 = \frac{1}{\beta(5-0.3)}$, which gives $\beta \approx 10^{-3}$ (2)

Moreover, we can use the $\beta = \beta_0 \left(\frac{W}{L}\right)$ with the obtained value (2) to find that the first aspect ratio, which is the $\frac{W}{L}$ regarding A and B, is 6.

Furthermore, we can use this ratio for C as well. As the next step, the second aspect ratio, which is for the load, would be calculated.

If $V_{in}=V_{DD}$, let Vout = 0.1V << V_T, then

Since we have that $I_D = \frac{\beta[(V_G-V_T)V_D-V_D^2]}{2} \approx \beta[(V_G - V_T)]$, we can say that

$R_D = \frac{V_{Out}}{I_D} = \frac{1}{6\beta[(V_G-V_T)]} = 200\Omega$ and therefore, by $\frac{R_D}{R_D+R_L} = \frac{V_{out}}{V_{DD}} = \frac{0.1}{5} = 0.02$ we can get $R_L \approx 10k\Omega$ (3)

Since $I_D = \frac{\beta_L(V_{DD}-V_T)^2}{2}$ and $R_L = \frac{V_{DD}-V_{out}}{I_D}$, we get $\beta_L = 4.4 * 10^{-5}$ (4)

Now, we can use the $\beta = \beta_0 (\frac{W}{L})$ with the obtained value (4) to find the second aspect ratio, which is the $\frac{W}{L}$ regarding the load, is 0.25.

As the last step of the calculation, the aspect ratio for the resistor is calculated.

We have that $R = R_S (\frac{L}{W})$, and since it is given that $R = 5k\Omega$ and $R_S = 100\Omega/\text{sq}$, we get $\frac{W}{L} = \frac{1}{50}$.

In summary, for the design implemented in this experiment, the aspect ratio of A and B were chosen to be 6 and the aspect ratio of 12 and 0.5 were chosen as the aspect ratios of C and the load respectively. Moreover, the aspect ratio of 0.02 was applied for the resistor.

Results and Discussion

The design rules that were mentioned in the previous section play an important role in this assignment and it effects the design of all four masks. For the first mask, which is regarding the device's active area, a 3λ distance for both the width and the spacing was implemented. For the other masks, the width and spacings were chosen accordingly. Moreover, for the V_{DD} and the ground a 4λ measurement was chosen as the width and a 2λ measurement was used as the width for the resistor.

For the calculation chip area, the aspect ratios are applied to find out the ratio of relation between width and length. Moreover, the ratio for each piece can be enhanced

proportional to their related pieces. For instance, in this assignment, 6 was calculated to be used as the aspect ratio for A, B and C and the aspect ratio for the load was calculated as 0.025. Therefore, the aspect ratio of the load was enhanced and changed to 0.5 while the aspect ratio for C was enhanced correspondingly and was doubled likewise (aspect ratio = 12). Furthermore, as mentioned in the lab manual, using the same drain and source for A and B as well as replacing the resistor with an active resistor could also play an important role in minimizing the chip area.

In the normal case, as mentioned previously, it is assumed that $A = B = 1$, which gives

$$(1)\frac{R_D}{R_D + 5k} = \frac{V_{out}}{V_{DD}} = \frac{0.1}{5} ==> R_D \approx 200\Omega ==> R_A = R_B \approx 200\Omega$$

As mentioned by the teaching assistant present at the lab session, the worst case occurs when it assumed that $A = 1$ and $B = 0$, which gives that

$$(2)\ V_{out} = V_{DD}\ \frac{R_D}{R_D + 5k} = 0.2\ V$$

Therefore, we can no longer say $V_{out} << V_T$.

In addition, based on formula (1), it can be noticed that R_D is proportional to V_{out}. As mentioned previously, β depends on and likewise. And since we have shown that the aspect ratio depends on β based on $\beta = \beta_0(\frac{W}{L})$. Therefore, it can be concluded that by considerably decreasing the V_{out} (from 0.1 V to 0.01 V), the aspect ratio would be heavily influenced and this change would considerably affect the size of the drivers.

Conclusion

It is believed that after conducting this experiment, a deeper understanding of the teaching material, which was used in the lectures, was achieved. Moreover, it is believed that the ability to design the layout and masks for a nMOS IC circuit is obtained. This lab assignment is believed to stimulate our interest in the subject and present us with an opportunity to examine our ability in layout design.

It can be mentioned that the teaching assistants present at the lab session were considerably helpful, guided us through any misunderstanding that occurred and answered any questions that we had regarding this assignment likewise. It can also

be mentioned that the lack of time and also self-made mistakes caused the progress to occur at a slower pace. It is suggested that in future instances, more exercises as well as more time is provided to prevent such mistakes.

References

EEE112 Integrated Electronics and Design nMOS IC Design Project, XJTLU, Suzhou, Jiangsu, 2018.

EEE112 Lecture notes, XJTLU, Suzhou, Jiangsu, 2018.

The figures that were used in this report and a considerable portion of the descriptions and explanations were inspired by the lab manual and also the lecture notes provided for the EEE112 module by the electronics and electrical engineering department in XJTLU.