EEE104 Lab

Digital Electronics

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Abstract

One of the most crucial and considerable branches of electronics is related to digital electronics. In digital electronics, logic gates are implemented and/or combined to produce a desired output from the given input. The type of these combinations is usually determined by a Boolean expression; an expression that allows only two possibilities for each of its entries: HIGH or LOW (1 or 0). This experiment is divided into eight sections and in each section the aim is to assemble a number of various circuits containing logic gates and to examine the output of each circuit as the given input changes. Moreover, achieving a better understanding of logic gates as well as obtaining the ability to implement logic gates in circuits is believed to another part of the objective of this experiment likewise. As for each section, a brief yet complete instruction is provided to ensure that the procedure is clear to the reader. Moreover, circuit diagrams and graphs are included to further ease the understanding of the explanation. After the procedure explanation, the results that were obtained from conducting this experiment are provided for each section respectively. Based on the obtained results, it can be concluded that the mentioned objectives were successfully achieved. Furthermore, a set of comments and suggestions regarding this experiment is provided as the last part of this report.

Introduction

Digital electronics, defined as the type of electronics implemented with the use of digital signals, plays an essential role in designing circuitry, especially for computer systems. In digital electronics, the main apparatus to be used for circuit design are logic gates. The aim of using logic gates is to create Boolean expressions that allow different varieties of signal combinations. In this experiment, a number of logic gates are implemented in order to analyze and record the output corresponding to the given input. As the results of this experiment are examined and studied, a further understanding of logic gates' functionalities is believed to be achieved as an outcome.

Apparatus

The apparatus used for conducting this experiment consisted of a NAND gate, a NOR gate, a NOT gate, an AND gate, an OR gate, a XOR gate, two D flip-flops, two J-K flip-flops, four 330Ω resistors and four LED diodes along with connecting wires, a breadboard, a multimeter, a DC power supply and a signal generator.

Experiment procedure

The procedure of this experiment was divided into eight sections. The process regarding each section is explained respectively below:

Section 1: Test of basic logic gates

As the first stage of this section, a digital circuit containing a NOT gate (Figure 1) was assembled (connect the input wire to pin-13 and connect the output wire to pin-12). Consequently, the circuit was examined and tested for different inputs and the resulting outputs were recorded in a truth table.

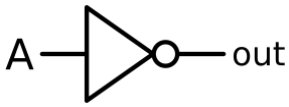

Figure 1: a NOT logic gate

In the second stage of this section, a 2-input AND gate (Figure 2) was used to assemble the required circuit (connect the input wire to pin-13 and pin-12 and connect the output wire to pin-11). The circuit was supplied with different inputs and the obtained corresponding outputs were recorded in a truth table.

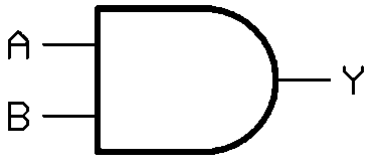

Figure 2: an AND logic gate

As the third and final stage of this section, a circuit using a 2-input NOR gate (Figure 3) was assembled (connect the input wire to pin-13 and pin-12 and connect the output wire to pin-11). Then, the circuit was analyzed for different input possibilities and each of the corresponding outputs were recorded in a truth table respectively.

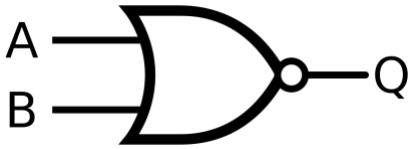

Figure 3: a NOR logic gate

Section 2: DeMorgan's theorem

In this section, there are two circuit designs (Figure 4), which were provided in the lab manual. We are asked to use the designs in order to assemble corresponding circuits.

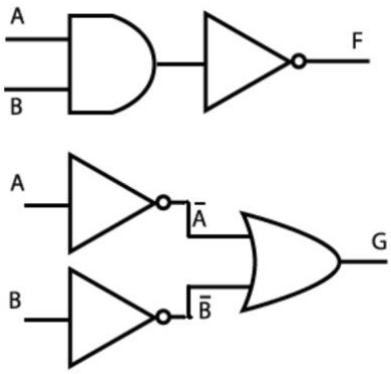

Figure 4: provided circuit designs

For the first figure, we use a 2-input AND gate (connect the input wire to pin-13 and pin-12) and then connect its output to a NOT gate (connect a wire between pin-11 of the AND gate and pin-13 of the NOT gate. Then, connect the output wire to pin-12 of the NOT gate). Consequently, we test and record the output as we change the input values in a truth table.

Moreover, we assemble the second circuit design by connecting each of the inputs to a NOT gate (Connect one input wire to pin-13 and one wire to pin-11 of the NOT gate) and use each of the outputs as an input for a 2-input OR gate (Connect pin-12 and pin-10 of the NOT gate to pin-13 and pin-12 of the OR gate and then, connect the output wire to pin-11 of the OR gate). As done in the previous stage, we test and recorded the obtained values respectively in a truth table.

Section 3: Combinational logic circuits

In the lab manual, we were given a statement that represented a real-life situation. Furthermore, we are asked to transform this statement into a Boolean expression form and then use the newly obtained expression to design and implement a circuit. It is

also mentioned in the lab manual to consider A as whether her mother had given her permission, B as whether her father had given her permission, C as Whether joe would pick her up, D as whether Tom would pick her up, and F as the output of this expression which represents whether she (Mary) would go to the cinema or not.

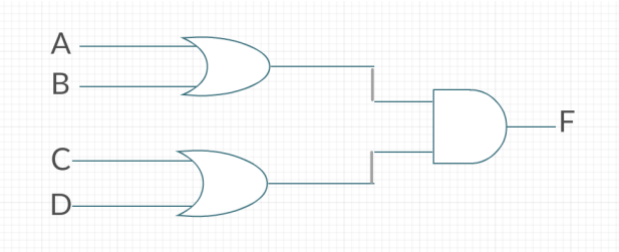

Figure 5: logic circuit for the Boolean expression F = (A+B) (C+D)

The Boolean expression for this statement is given to be F = (A+B) (C+D). Based on this expression, we can connect two inputs representing A and B to a 2-input OR gate (connect the inputs to pin-13 and pin-12). Consequently, we can connect another two inputs representing C and D to another 2-input OR gate (connect the inputs to pin-10 and pin-9). As the last step of the procedure, we would connect the output of the two mentioned OR gates as inputs to a 2-input AND gate (connect pin-11 and pin-8 of the OR gate to pin-13 and pin-12 of the AND gate respectively. Then, connect the output wire to pin-11). After completely assembling the circuit, we use a multimeter to observe and record the output as the inputs change. Furthermore, the logic circuit diagram of this drawn and shown as a figure (Figure 5).

Section 4: Implementation of a Half Adder

The aim of this section of the experiment is to assemble a circuit containing a half adder (Figure 6). In this circuit we use a XOR gate and an AND gate to obtain the required results regarding the sum and the carry respectively. For the XOR gate, we connect the input wire to pin-13 and pin-12 and connect the output wire to pin-11 of the gate. The same pin numbers are used to connect the AND gate. As we change the inputs, we record the obtained data in a truth table and answer the question, which was asked in the lab manual, accordingly.

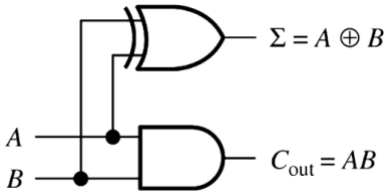

Figure 6: The half adder circuit

Section 5: The S-R Latch

In this section, an S-R latch is assembled using NOR gates according to the provided figure (Figure 7). We would use two OR gates for designing this circuit. Firstly, we would connect an input S to one OR gate and a R input to the other OR gate (connect the first input wire to pin-13 and connect the second input to pin-10). Now, as the output of one gate is used as one of the inputs for the other gate, we connect the outputs of the gates to the other's input (connect pin-12 to pin-8 and connect pin-11 to pin-9).

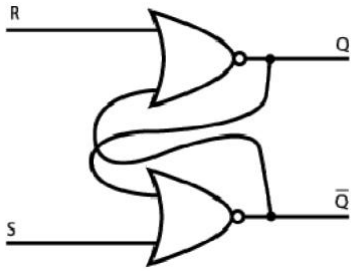

Figure 7: An S-R latch created using NOR fates

For analyzing the output, we connect a wire to each of these outputs and connect the other head of these wires to a 330Ω resistor and then connect the resistor to a LED, where when the light is on, the signal is HIGH.

After the circuit is assembled, we vary the inputs in order to obtain and observe the required outputs. As the final step of this section, we record the obtained results inside a truth table and discuss how this circuit works, as it is tasked in the lab manual.

Section 6: The Edge-triggered D flip-flop

To assemble a circuit contacting a D flip-flop we need to implement four NAND gates and a NOT gate. Firstly, we connect a wire as an input to two of the 2-input NAND gates (connect the clock signal to pin-13 and pin-10). As the clock is supposed to

produce a square signal, we are required to modify the signal generator settings. In this step, we must check that the offset has been set to 0 and the maximum voltage is selected to be 5 volts as a result. Consequently, we connect the D wire as an input for the first NAND gate and the NOT gate (connect the D wire to pin-12 of the NAND gate and pin-13 of the NOT gate). At this stage, the output of the NOT gate should be used as the second input for the second NAND gate (connect pin-12 of the NOT gate to pin-9 of the NAND gate).

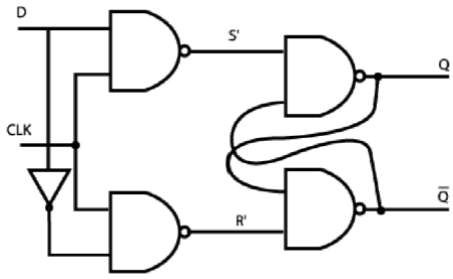

Figure 8: The D-type flip-flop

As seen in the figure (Figure 8), the outputs of the first two gates are used as one of the inputs for the second two NAND gates (on the NAND gates, connect pin-11 and pin-8 to pin-1 and pin-4 respectively). As the last step of the circuit design, the output of one of the NAND gates should be used as the input for the other (connect pin-3 to pin-5 and connect pin-2 to pin-6).

After assembling the circuit, we would acquire the required results and record them in the provided truth table. For analyzing the output, we connect a wire to each of these outputs and connect the other head of these wires to a 330Ω resistor and then connect the resistor to a LED, where when the light is on, the signal is HIGH.

Section 7: The asynchronous counter

Three J-K flip-flops are required to construct an asynchronous counter (Figure 9). Therefore, we need to use two different chips. As the first step of this section, we connect a +5v signal (HIGH) to pin-3 and pin-11 of the first chip and pin-3 of the second chip. These three pins represent the J_0, J_1 and J_2 respectively. Then, we connect a +5v signal (HIGH) to pin-2 and pin-12 of the first chip and pin-2 of the second chip. The mentioned three pins represent the K_0, K_1 and K_2 respectively.

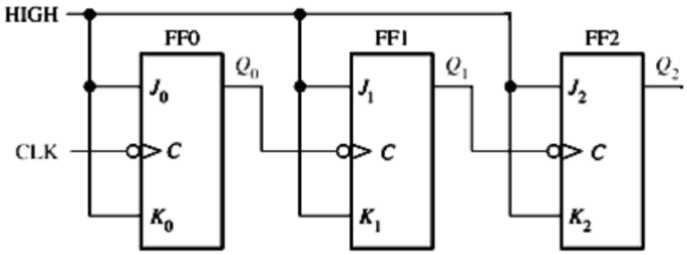

Figure 9: The asynchronous counter

As the clock is supposed to produce a square signal, we are required to modify the signal generator settings. In this step, we must check that the offset has been set to 0 and the maximum voltage is selected to be 5 volts as a result. Consequently, we connect the clock to the first J-K flip-flop (connect the signal wire to pin-1 of the first chip). As seen in the figure, the output of the first flip-flop is used as the clock for the second flip-flop (connect pin-5 to pin-13 on the first chip). Furthermore, the output of the second flip-flop is used as the clock for the third flip-flop (connect pin-9 of the first chip to pin-1 of the second chip).

Since, we want to analyze the output of this circuit for Q_2, Q_1 and Q_0 at the same time so it's not wise to use a multimeter. Instead, we connect a wire to each of these outputs and connect the other head of these wires to a 330Ω resistor and then connect the resistor to a LED. In this way, after turning on the signal generator, we can examine the outputs according to whether the LED connected to them is lit or not, where being lit shows HIGH and being off shows LOW. Similar to the previous sections, the observations are examined in detail and recorded in the provided truth table.

Section 8: The shift register

The main objective of the last section of this experiment is to assemble a 4-bit shift register, which is also known as a Johnson register (Figure 10). For assembling this register, we would need to use 4 D flip-flops; meaning that we need to implement two chips. Firstly, we are required to connect the clock signal to each of the flip-flops (connect four signal wires to pin-3 and pin-11 of the first chip and pin-3 and pin-11 of the second chip respectively).

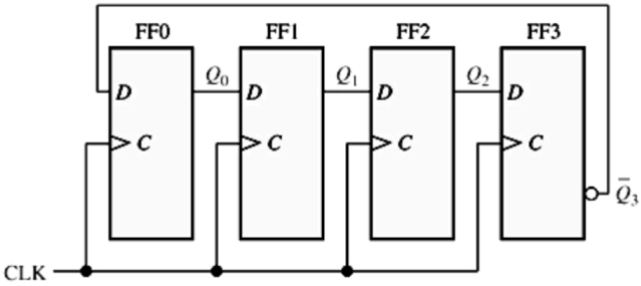

Figure 10: The 4-bit shift register

As shown in the figure, the output of the first three flip-flops is used as the D input for the next flip-flip (connect pin-5 to pin-12 of the first chip, connect pin-9 of the first chip to pin-2 of the second chip and then, connect pin-5 to pin-12 on the second chip). However, for the first flip-flop, the NOT output of the last flip-flop is used as the D input (connect pin-8 of the second chip to pin-2 on the first chip).

After the circuit is completely assembled, as explained above, we are required to apply 1~2Hz clock pulses to the circuit to observe what happens as a result. Furthermore, the observations are recorded accordingly. For analyzing the output, we connect a wire to each of these outputs and connect the other head of these wires to a 330Ω resistor and then connect the resistor to a LED, where when the light is on, the signal is HIGH.

NOTE: The mentioned measures were made using a digital multimeter. Moreover, the obtained results and truth tables are provided in the Results section of this report. It should also be mentioned that when each circuit was assembled, each gate was connected to power (connect power to pin-14) and ground (connect ground to pin-7 for the all the gates and the D flip-flop or pin-8 for the J-K flip-flops). The rest of the connections were made based on the given manual at the last page of the provided EEE104 lab manual.

Results

As the procedure for this experiment was divided and explained previously in eight sections, the obtained results are mentioned, corresponding to each section, respectively below:

Section 1: Test of basic logic gates

For the first stage regarding the function of a NOT gate, the following results were obtained (Figure 11) and recorded in a truth table:

Figure 11: obtained results for NOT logic gate

Input	Output
0 V	5.1 V
5 V	79.5 mV

As the NOT gate is known to be used as an inverter, meaning that it converts HIGH signal to low vice versa, the obtained results for the first part of this section are believed to be correct.

In the second part of this section, we tested the application of an AND logic gate. The following show the obtained results containing to different inputs respectively (Figure 12):

Input 1	Input 2	Output
0 V	0 V	114.2 mV
0 V	5 V	114.1 mV
5 V	0 V	114.1 mV
5 V	5 V	4.63 mV

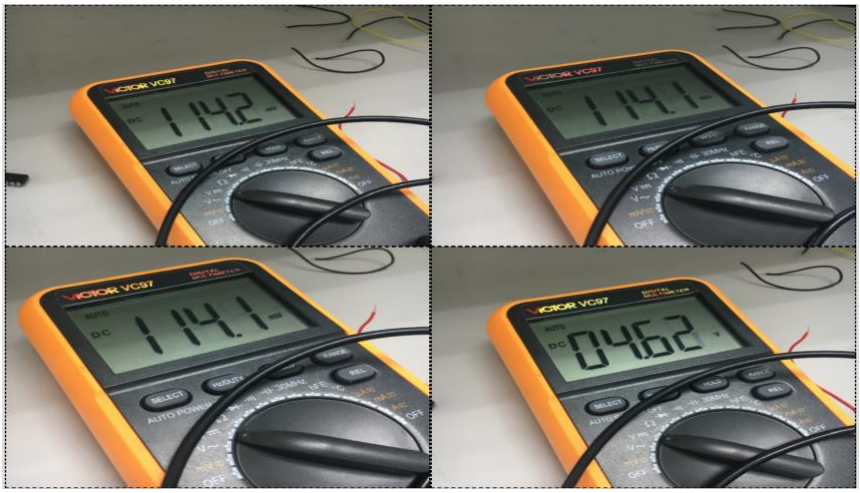

Figure 12: obtained results for an AND logic gate

The AND logic gate acts as the multiplication sign in mathematics. Therefore, the only possible way that the output of an AND gate is HIGH is when all of the inputs are HIGH. Furthermore, this suggests that for any other combination of inputs produces a LOW output. Therefore, it can be claimed that the obtained results for the second part of this section are correct likewise.

A NOR logic gate was examined in the last part of this section. The NOR gate produces the exact opposite of an output for the OR gate. Therefore, it can be known that the NOR gate would only produce a HIGH output when all of the inputs are LOW and that any other combination of inputs would produce a HIGH output. The following are the obtained results from this part of the experiment:

Figure 13: obtained results for a NOR logic gate

Input 1	Input 2	Output
0 V	0 V	4.78 V
0 V	5 V	0.692 mV
5 V	0 V	0.692 mV
5 V	5 V	0.696 mV

Since the results correspond to the claim, which was mentioned earlier, they are believed to be credible and correct as well.

Section 2: DeMorgan's theorem

There were two circuits that were assembled in this section of the experiment. In the first circuit, an AND gate was implemented and followed by a not gate to produce the required output. The following are the results obtained from testing this circuit (Figure 14):

Figure 14: results obtained from the first circuit in section 2

A	B	F
0 V	0 V	4.91 V
0 V	5 V	4.92 V
5 V	0 V	4.82 V
5 V	5 V	132.6 mV

Moreover, a second circuit contacting two NOT gates followed by an OR gate was assembled and examined. The following are the results obtained from this circuit (Figure 15):

A	B	G
0 V	0 V	4.7 V
0 V	5 V	4.92 V
5 V	0 V	4.9 V
5 V	5 V	157 mV

Figure 15: results obtained from the second circuit in section 2

As theorized, the two mentioned circuits should produce the same output. As shown by the obtained results, this claim is proved and therefore, the results for this section are believed to be correct. Moreover, we are write the Boolean expression for each of the mentioned two circuits. The following are the Boolean expressions for outputs F and G:

$$F = \overline{AB}$$

And

$$G = \overline{A} + \overline{B}$$

And based on the DeMorgan's theorem we can say that F = G.

Section 3: Combinational logic circuits

In this section, we had to test out the combination of logic circuits, which in this case where AND and OR gates. The following are the results obtained from this experiment (Figure 16 &17):

Figure 16: the results of section 3 (part 1)

A	B	C	D	F
0 V	0 V	0 V	0 V	126.6 mV
0 V	0 V	0 V	5 V	127.2 mV
0 V	0 V	5 V	0 V	127.1 mV
0 V	0 V	5 V	5 V	128.3 mV
0 V	5 V	0 V	0 V	127 mV
0 V	5 V	0 V	5 V	4.11 V
0 V	5 V	5 V	0 V	4.1 V
0 V	5 V	5 V	5 V	3.88 V
5 V	0 V	0 V	0 V	127 mV
5 V	0 V	0 V	5 V	4.19 V
5 V	0 V	5 V	0 V	4.21 V
5 V	0 V	5 V	5 V	2.8 V
5 V	5 V	0 V	0 V	127.8 mV
5 V	5 V	0 V	5 V	4.11 V
5 V	5 V	5 V	0 V	4.02 V
5 V	5 V	5 V	5 V	4.12 V

Figure 16: the results of section 3 (part 2)

The Boolean expression suggests that in order to have a HIGH output, at least one of the inputs in the first group (A OR B) and one of the inputs in the second group (C OR D) has to be HIGH. The obtained results also show the same conclusion and therefore, are believed to be credible.

Section 4: Implementation of a Half Adder

As explained in the procedure section of this report, a half adder circuit is constructed using a XOR gate and an AND gate. The outputs of this circuit were examined and recorded respectively below (Figure 17):

Figure 17: results for the half adder circuit (top row is sum and lower is carry)

A	B	$\sum = A \oplus B$	$C_{out} = AB$
0 V	0 V	29.6 mV	122.4 mV
0 V	5 V	4.76 V	123.6 mV
5 V	0 V	4.78 V	123.3 mV
5 V	5 V	138.7 mV	4,89 V

The output for the AND gate has already been explained and mentioned in the earlier section and based on that, we can say that the results regarding the carry part of the half adder are correct. As for the XOR gate, it is known that the output would be HIGH only when the inputs are different; meaning that one is HIGH while the other is LOW. Therefore, the obtained results regarding the sum part of the half adder are also deemed to be correct. It should be mentioned that based on the known characteristics of the AND and XOR gate, these results were expected.

Moreover, it should be mentioned that the half adder is not suitable for all additional operations. The reason for this statement is due to the fact that in the case of one of the inputs having a carry, the carry part would be dismissed. In other words, the half adder only adds two bits (A and B) and does not correlate to carry [1].

Section 5: The S-R Latch

In this section, a circuit containing a S-R flip-flop was assembled. The truth table below was completed based on the obtained results (Figure 18):

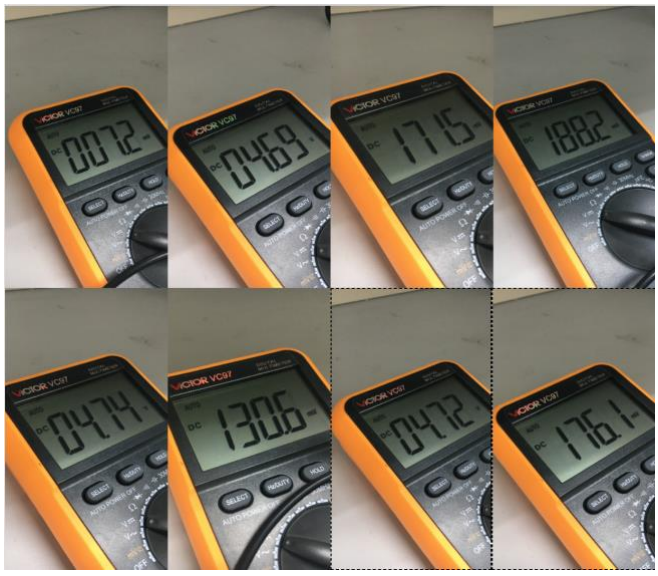

Figure 18: results for the S-R flip-flip circuit (top row is Q and lower is $\overline{Q}$)

S	R	Q	$\overline{Q}$
0 V	0 V	7.2 mV	4.74 V
0 V	5 V	4.69 V	130.6 mV
5 V	0 V	171.5 mV	4.72 V
5 V	5 V	188.2 mV	176.1 mV

As acknowledged from the S-R flip-flop characteristics, the obtained results are believed to be similar to what was expected and are therefore correct and credible. Moreover, in the lab manual we are asked to explain how this circuit would work by completing the provided truth table. The completed truth table is as follows:

Q_n	$\overline{Q}_n$	R	S	Q_{n+1}	$\overline{Q}_{n+1}$
0	1	0	0	0	1
1	0	0	0	1	0
0	1	0	1	1	0
1	0	0	1	0	1
0	1	1	0	0	1
1	0	1	0	1	0
0	1	1	1	?	?
1	0	1	1	?	?

The answers in this truth table are determined by the following logics:

1) If both R and S are LOW, the output would not change and would be identical to the previous stage.
2) If R is HIGH and S is LOW, Q would be LOW and $\overline{Q}$ would be HIGH (set).
3) If R is LOW and S is HIGH, Q would be HIGH and $\overline{Q}$ would be LOW (reset).
4) If both R and S are HIGH, we get invalid outputs.

Section 6: The Edge-triggered D flip-flop

After assembling a circuit containing a S-R flip-flop following a D flip-flop, which is also known the edge-triggered flip-flop, we were required to examine and record the outputs corresponding to different combinations of inputs. Essentially, a positive edge

triggered flip-flop is one which can only function on the positive edge cycle (when enable/E is transforms from LOW to HIGH); meaning that the output would only change in the positive edge cycle. On the contrary, we also have negative edge triggered flip-flop where the output would only change in the negative edge cycle (when enable/E is transforms from HIGH to LOW).

In the lab manual, we were given a truth table regarding the output for the D-type flip-flop and the completed version of this table is provided below:

Q_n	$\overline{Q}_n$	D	Q_{n+1}	$\overline{Q}_{n+1}$
0	1	0	0	1
1	0	0	0	1
0	1	1	1	0
1	0	1	1	0

As mentioned earlier, an edge-triggered circuit only functions when the state of the clock switches (Either from LOW to HIGH or HIGH to LOW). This can be extremely essential where more exact switching is needed in a flip-flop circuit. Moreover, an edge-triggered flip-flop could be greatly useful for circuits regarding delay detection and also noise reduction [2].

Section 7: The asynchronous counter

After completely assembling the asynchronous counter, based on the provided figure (Figure 9), we are required to test and record the given output. In this section of the experiment, similar to section 5 and 6, a multimeter is not used to measure the outputs and LEDs accompanied by resistors are implemented in the circuit instead. The following are the results obtained from this section of the experiment after connecting the circuit to a 1Hz square signal:

	Q_0	Q_1	Q_2
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0

5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1
9	0	0	0
Etc..	repeat	repeat	repeat

Where 0 represents OFF light and 1 represents ON light.

The results clearly show how the asynchronous counter functions. Since this counter is using 3 flip-flops, it can count 8 numbers (0-7), which proposes that for n flip-flops we can present 2^n numbers; meaning that we can have 2^n different states.

In this counter, Q_0, Q_1 and Q_2 represent three digits of a binary number, where Q_0 is the least significant bit (LSB) and Q_2 is the most significant bit (MSB). In this circuit, the counter starts by showing the decimal 0 (000 in binary) and counts each decimal until 7 (binary 111). After reaching 7, the counter would reset and start counting again from 0.

The reason why this circuit is called asynchronous is due to the fact that instead of all the flip-flops being connected to the same clock, the clock is only connected to the first flip-flop and the other flip-flops receive their clock signals from the output of the preceding flip-flop. Therefore, different flip-flops would receive different clocks signals and are called asynchronous as a result.

Section 8: The shift register

In the final section of this experiment, we had constructed a 4-bit shift register using four D flip-flops. After applying the 1Hz clock signal to the circuit, the observations were recorded in the following truth table:

	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0

4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

In this circuit, at first all of the Qs are 0 as the circuit is not connected to any signals. Then, the second, the third and the fourth flip-flop regard their preceding flip-flop's output (Q) as their D input. In this stage, the first flip-flop uses the inverted version of the fourth flip-flop as its D input. It is known that in D flip-fops when the CLK is HIGH, the output is the same as the input D. Therefore, in the first clock cycle (CLK1), Q_0 would be 1 ($D_0= \overline{Q}_3 = 1$) and the rest of the outputs would be 0.

In the next clock cycle (CLK2), Q_3 as is still zero, Q_0 would stay at HIGH while Q_1 turns to HIGH as well. Moreover, we can use the same logic and claim that in CLK3 and CLK4, Q_2 and Q_3 are set to HIGH respectively. In CLK5, since Q3 is HIGH, the D input for the first flip-flop would be set to LOW, which results in Q0 being set to LOW. The transformation of the LOW signal from Q_0 to Q_3 (CLK5 to CLK7 and then reset to CLK0) is expected to occur in a similar manner compared to the transformation of the HIGH signal (CLK1 to CLK4).

Since the obtained results are identical to what was expected based on the behavior of the 4-bit shift register, it can be suggested that the results regarding this section of the experiment are correct.

Conclusions

What was gained from this experiment

After conducting this experiment, it is believed that a clear understanding of the behavior of various types of logic gates, the relation between Boolean expressions, and characteristics of combinational logic gates were achieved as a result. Moreover, the ability to implement the provided logic gates in electronic circuits and examining the process of the experiment, as certain changes were made, was obtained likewise. It is believed that each section of this experiment made us familiar with the subjects, that were previously taught in EEE104 lectures, as well as causing us to acknowledge the importance of digital electronics in the technology industry.

Possible changes

It could be mentioned that the team work that was required for conducting this experiment may have been a little bit abstract to the students. As each team is given one breadboard, only one member of the team is able to assemble the circuit while the other has to observe. This could cause lack of understanding and acknowledgement for one of the members of a group. If I were to do this lab again, I would write a draft of the report beforehand and try to complete the report as the experiment was being conducted. It is believed that by doing so, the efficiency of the lab report would have been increased considerably and that the provided material could have been learned more deeply.

It should also be mentioned that the apparatus provided in the laboratory was mostly out of order and there was a high possibility that errors occur during conducting this experiment. As seen in the results, there are slight errors in values of the output that are believed to be due to the provided apparatus, such as wires, breadboard and also multimeter. In the final sections, the apparatus made huge impact on the outcome of this experiment; the reason being that the expected output could not have been obtained for a period of due to the apparatus dysfunctionality and that may cause many students to lose the limited time that they are given to conduct this experiment.

Suggestions

Firstly, as it was observed that many students either could not finish experimenting all of the given sections or spent a lot of time before completing all of the process, it is suggested to divide the laboratory sessions into two parts where in each part half of this experiment is conducted. It is believed that by doing so, the accuracy of the experiment as well as the lab report would be increased.

Moreover, it is suggested to make the necessary changes regarding the apparatus provided in the laboratory as a large portion of them are out of date and order. It is believed that by improving the laboratory conditions, less errors would occur in the output of the experiment, which results in more efficiency in both the experiment process and also the obtained results.

Comments

In conclusion, this experiment is regarded as a highly valuable experience. The teaching assistants present in the laboratory session were extremely helpful and guided us through any misunderstanding that occurred. It is believed that by making the mentioned suggestions, this experiment would be improved considerably and this improvement would affect would both XJTLU students and staff.

References

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[2] Miura, Y., Ohkawa, Y. (2014). "A noise-tolerant master-slave flip-flop", *[online] Testing Symposium (IOLTS) 2014 IEEE 20th International*, pp. 55-61, 2014.

It should be mentioned that the graphs regarding the construction of each of the circuits, which were implemented in this experiment, and the description regarding the procedure of each section of this experiment were inspired by the lab manual for EEE104 Digital Electronics provided by the Department of Electrical and Electronic Engineering in XJTLU.