UOM Exam Second half 2021_Question paper_R2019/CSC304 - DLCA /Sem-III / COMPUTER ENGINEERING / ARTIFICIAL INTELLIGENCE AND DATA SCIENCE / ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING / COMPUTER SCIENCE AND ENGINEERING (Artificial Intelligence and Machine Learning / COMPUTER SCIENCE AND ENGINEERING (Data Science) / COMPUTER SCIENCE AND ENGINEERING (Internet of Things and Cyber Security Including Block Chain Technology) / CYBER SECURITY / DATA ENGINEERING / INTERNET OF THINGS (IoT)

Dear Student,
Please note before you attempt this section of examination:
1. Q1, Q2, Q3 and Q4 carry 20 marks each.
2. This paper contains 20 Marks MCQ and 60 marks subjective section for 150 minutes duration.
3. It is mandatory for all the students to upload their answer papers in a single PDF format only.
4. You have to write Date of Examination, Seat number, Program, Scheme and semester, Subject name, Signature on EVERY PAGE.
5. Remain in the meet with your camera on and you in clear view throughout the duration of the exam.

* Required

1. Email *

2. Student Name (As per exam form filled) *

3. Seat No *
Refer Hall ticket

Solve Questions as per the instructions given separately.

- Please upload a single PDF for Q1 to Q4
- For MCQs Question write Question number & correct option with complete text in option.
- Q2 to Q4 are subjective questions - Solve Questions as per the instructions and marks allotted.

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	What is the primary motivation for using Boolean algebra to simplify logic expressions?
Option A:	It may make it easier to understand the overall function of the circuit.
Option B:	It may reduce the number of gates.
Option C:	It may reduce the number of inputs required.
Option D:	All of the above
2.	The given hexadecimal number (1E.53)16 is equivalent to _____
Option A:	(35.684)8
Option B:	(36.246)8
Option C:	(34.340)8
Option D:	(35.599)8
3.	In restoring division algorithm, after performing operations (1) 1eft shift operation on A,Q and (2) A=A-M, if sign of A is positive?
Option A:	Q0=0, A=A+M
Option B:	A=A+M
Option C:	Q0=1
Option D:	A=A-M
4.	In Booth's multiplication algorithm, if Q0=1 and Q-1=1 then it will perform which operation,
Option A:	A=A-M
Option B:	A=A+M
Option C:	Arithmetic right shift of A, Q and Q-1
Option D:	A=M-A
5.	In a system the contents of PC, Base register, Register R0, and Register R1 has contents 60, 100, 10, and 20 respectively. Content of R1 is used as the displacement value. What is the effective address computed using the Base addressing and the Relative-Base addressing modes, respectively?
Option A:	120, 80
Option B:	110, 120
Option C:	120, 160
Option D:	120, 180

6.	A J-K flip-flop with J=1 and K=1 has a 20 KHz clock input. The Q output is _____
Option A:	Constantly LOW
Option B:	Constantly HIGH
Option C:	A 20 KHz square wave
Option D:	A 10 KHz square wave
7.	Which is the simplest method of implementing hardwired control unit?
Option A:	State Table Method
Option B:	Delay Element Method
Option C:	Sequence Counter Method
Option D:	Using Circuits
8.	Highly encoded schemes that use compact codes to specify a small number of functions in each micro instruction is _____
Option A:	Horizontal organization
Option B:	Vertical organization
Option C:	Diagonal organization
Option D:	Complex microinstruction organization
9.	Which of the following statement is TRUE?
Option A:	A direct mapped cache has higher hit time than a 4-way set associative cache with same of number of sets.
Option B:	Two 4 KB caches of same block size, but with different associativity will always have same hit rate.
Option C:	A set associative cache has lower number of conflict misses than a direct mapped cache of same size.
Option D:	During a cache miss, there will be block replacements in a fully associative cache if at least one of the cache location is empty.
10.	Which of the following statement is false with respect to instruction pipeline?
Option A:	Pipelining can increase the throughput of a system.
Option B:	Pipelining partitions the system into multiple independent stages with added buffers between the stages.
Option C:	Pipelining reduce the latency of each individual instruction.
Option D:	Unbalanced lengths of pipeline stages reduces overall speedup.

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Q.2	**Solve any Two Questions out of Three.**		
	A)	Perform the following – i) Convert $(340)_{10}$ to excess-3 code. ii) Convert Hexadecimal to decimal: DADA iii) Draw OR gate using NAND gate. iv) Hexadecimal to binary conversion: 3A9D.A0C v) Represent $(52)_{10}$ into Gray code.	**10**
	B)	Draw flow chart for non-restoring division algorithm and perform the division operation 11/3 using non-restoring division algorithm.	**10**
	C)	Design a full adder using half adder and additional gates. Give its Boolean expression for Sum and Carry and truth table.	**10**
Q.3	**Solve any Two Questions out of Three.**		
	A)	With suitable steps convert decimal number 39887.5625 to IEEE 64-bit Double precision floating point representation.	**10**
	B)	With the help of diagram explain in brief: functioning of Micro programmed Control Unit.	**10**
	C)	What is Cache Memory? A 32-bit computer has a 32 bit memory address. It has 8kB of cache memory. The computer follows four-way set associative mapping. Each line size is 16 bytes. Show the memory address format and cache memory organization.	**10**
Q.4	**Solve any Two Questions out of Three.**		
	A)	What is Pipeline Hazard? Give the types of pipeline hazards. Write a difference between delayed branch and branch prediction.	**10**
	B)	With suitable diagram, explain the Flynn Classification of Computer organization.	**10**
	C)	Write a short note on Interleaved and Associative Memory.	**10**

4. Please Upload complete scanned answer copy in a single PDF file. *

Files submitted: