UOM Exam Second half 2021_Question paper_R2019/CSC304 - Digital Logic & Computer Architecture /Sem-III / COMPUTER ENGINEERING / ARTIFICIAL INTELLIGENCE AND DATA SCIENCE / ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING / COMPUTER SCIENCE AND ENGINEERING (Artificial Intelligence and Machine Learning / COMPUTER SCIENCE AND ENGINEERING (Data Science) / COMPUTER SCIENCE AND ENGINEERING (Internet of Things and Cyber Security Including Block Chain Technology) / CYBER SECURITY / DATA ENGINEERING / INTERNET OF THINGS (IoT)

Dear Student,
Please note before you attempt this section of examination:
1. Q1, Q2, Q3 and Q4 carry 20 marks each.
2. This paper contains 20 Marks MCQ and 60 marks subjective section for 150 minutes duration.
3. It is mandatory for all the students to upload their answer papers in a single PDF format only.
4. You have to write Date of Examination, Seat number, Program, Scheme and semester, Subject name, Signature on EVERY PAGE.
5. Remain in the meet with your camera on and you in clear view throughout the duration of the exam.

* Required

1. Email *

2. Student Name (As per exam form filled) *

3. Seat No *
Refer Hall ticket

Solve Questions as per the instructions given separately.

- Please upload a single PDF for Q1 to Q4
- For MCQs Question write Question number & correct option with complete text in option.
- Q2 to Q4 are subjective questions - Solve Questions as per the instructions and marks allotted.

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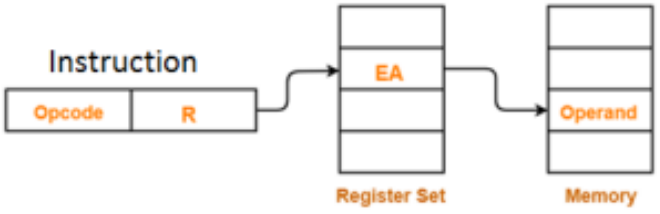
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	What is does the Program Counter Holds
Option A:	It Holds the Address of the Current Instruction
Option B:	It Holds the Address of the Next Instruction
Option C:	It Holds the Current Instruction
Option D:	It Holds the Next Instruction
2.	Arrange the steps for obtaining IEEE representation of floating point in proper format 1) calculate the biased exponent 2) convert to binary 3) convert to normalized form
Option A:	1,2,3
Option B:	3,2,1
Option C:	2,3,1
Option D:	2,1,3
3.	In Booths Algorithm in one of the step M=0010 A=0010 Q=0100 Q_{-1}=0 and count is not zero what it will be the value of M A Q and Q_{-1} in the immediate next step
Option A:	M=0010 A=0001 Q=0100 Q_{-1}=0
Option B:	M=0010 A=0001 Q=0010 Q_{-1}=0
Option C:	M=0010 A=0001 Q=0010 Q_{-1}=1
Option D:	M=0010 A=0001 Q=0000 Q_{-1}=0
4.	Identify the type of addressing mode for the diagram shown below 
Option A:	Register Addressing mode
Option B:	Register Direct Addressing Mode
Option C:	Immediate Addressing Mode
Option D:	Register Indirect Addressing Mode

5.	Which of the following is not a key characteristics of memory devices or memory system
Option A:	Location
Option B:	Physical Characteristics
Option C:	Availability
Option D:	Access Method
6.	The correspondence between the main memory blocks and those in the cache is given by _____.
Option A:	Mapping function
Option B:	Hash function
Option C:	Locale function
Option D:	Assign function
7.	Basic task for control unit is
Option A:	to perform logical operations
Option B:	to perform execution
Option C:	to initiate the resources
Option D:	to decode instructions and generate control signal
8.	Micro program consisting of _____ is stored in control memory of control unit
Option A:	Instructions
Option B:	micro instructions
Option C:	micro program
Option D:	macro program
9.	Flynn's taxonomy classifies computer architectures based on
Option A:	the number of instructions that can be executed
Option B:	how they operate on data.
Option C:	the number of instructions that can be executed and how they operate on data.
Option D:	The number of Control Signals Generated
10.	Which of the following is not a valid type of centralized bus arbitration
Option A:	Dependent Request
Option B:	Daisy chaining
Option C:	Polling method
Option D:	Independent Request

Q2	Solve any Four out of Six 5 marks each
A	Describe the detailed Von-Neumann Model.
B	Convert 12.5 in IEEE 754 Single Precision Format.
C	Write a Short note on Flip Flops.
D	Differentiate between Hardwired control unit and Micro programmed control unit.
E	Describe the Difference between SRAM & DRAM.
F	Write short notes on PCI Bus.

Q3	Solve any Four out of Six 5 marks each
A	Explain any five Addressing Modes.
B	Explain State Table design method for Hardwired control unit.
C	List the Characteristics of Memory.
D	What is Instruction Pipelining? Define the Pipeline performance Measures like SpeedUp, Efficiency, CPI, Throughput.
E	Draw the neat block diagram for Flynn's Classification (Only the Diagram).
F	Explain the Bus Arbitration.

Q4.	Solve any Two Questions out of Three 10 marks each
A	Draw the flowchart of Booth's Algorithm & perform 6 x -3 using this Algorithm
B	Describe the Micro programmed Control unit. Write micro program for the instruction ADD A, B (Register A and B are added and result is stored at Register A.).
C	Explain any two Cache memory Mapping Techniques.

4. Please Upload complete scanned answer copy in a single PDF file. *

   Files submitted:

5. Have you uploaded correct scanned copy of the answer sheets. *

   Mark only one oval.

   ◯ YES