Multiply/Divide Unit (MDU) Overview

The XYZ core features a dedicated Multiply/Divide Unit (MDU), enhancing the processing capabilities with a specialized pipeline for integer multiply/divide operations and DSP Module multiply instructions. This pipeline operates independently of the Integer Unit (IU) pipeline, ensuring that MDU operations continue seamlessly even during IU pipeline stalls. This allows partial masking of long-running MDU operations by system stalls and other integer unit instructions.

Storage result

According to the XYZ architecture, the outcome of multiply or divide operations is stored in pairs (in the absence of DSP) or in one of four pairs (with DSP enabled) of *HI* and *LO* registers. By utilizing the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be efficiently transferred to the general-purpose register file.

MDU Configuration Options

The MDU offers three configuration options:

1. Full 32x32 Multiplier Block
    - Suitable for applications prioritizing a comprehensive multiplier block.
2. Higher Performance 32x16 Multiplier Block
    - A performance-centric option providing improved speed.
3. Area-Efficient Iterative Multiplier Block
    - An option focused on conserving space while maintaining functionality.

Options 2 and 3 are available when the DSP configuration is disabled. If the DSP configuration is enabled, option 1 becomes the default setting. The choice of MDU style empowers implementers to fine-tune performance and area trade-offs based on the specific application requirements.