

Qplacer: Frequency-Aware Component Placement for Superconducting Quantum Computers

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Abstract—Noisy Intermediate-Scale Quantum (NISQ) computers face a critical limitation in qubit numbers, hindering their progression towards large-scale and fault-tolerant quantum computing. A significant challenge impeding scaling is crosstalk, characterized by unwanted interactions among neighboring components on quantum chips, including qubits, resonators, and substrate. We motivate a general approach to systematically resolving multifaceted crosstalks in a limited substrate area. We propose Qplacer, a frequency-aware electrostatic-based placement framework tailored for superconducting quantum computers, to alleviate crosstalk by isolating these components in spatial and frequency domains alongside compact substrate design. Qplacer commences with a frequency assigner that ensures frequency domain isolation for qubits and resonators. It then incorporates a padding strategy and resonator partitioning for layout flexibility. Central to our approach is the conceptualization of quantum components as charged particles, enabling strategic spatial isolation through a ‘frequency repulsive force’ concept. Our results demonstrate that Qplacer carefully crafts the physical component layout in mitigating various crosstalk impacts while maintaining a compact substrate size. On various device topologies and NISQ benchmarks, Qplacer improves fidelity by an average of $36.7\times$ and reduces spatial violations (susceptible to crosstalk) by an average of $12.76\times$, compared to classical placement engines. Regarding area optimization, compared to manual designs, Qplacer can reduce the required layout area by $2.14\times$ on average.

I. INTRODUCTION

In the ever-evolving realm of quantum computing, quantum computers (QCs) in Noisy Intermediate-Scale Quantum Computing (NISQ) [71] have captivated people’s attention, offering immense potential of computation to unravel intricate problems in chemistry [16], [45], biology [49], algorithms [32], [82], and machine learning [12], [91]. Superconducting QCs [4], [47], particularly the utilizing fixed-frequency transmon qubits anchored by Josephson junctions (JJs), stands out as a leading option for scalable quantum computing. These qubits contribute to relative rapid gate speeds [6], [7], [27], fairly extended coherence duration [90] and gate fidelities nearing fault-tolerance thresholds [80]. These merits have led to significant advancements in the field, as evidenced by the current generation of superconducting QCs, which boasts over 1000 physical qubits [41]. However, this scale of QCs is still insufficient for tackling intricate real-world problems more efficiently and outpacing classical computers [10].

In the near term, the critical barrier encountered in scaling superconducting QCs is crosstalk, a prevalent issue in many quantum architectures [3], [43], [47]. Crosstalk arises from un-

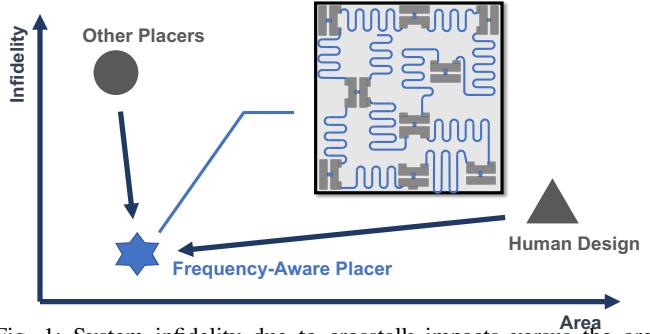


Fig. 1: System infidelity due to crosstalk impacts versus the area required for accommodating an equal number of qubits and other quantum components using different placement strategies. Qplacer is designed to optimize layout area while maintaining low infidelity.

wanted interactions between components on a quantum chip, often triggered when elements with resonating frequencies are either connected or positioned in close proximity [64], [76], [95]. In superconducting QCs, this leads to compromised computational fidelity, with inter-qubit crosstalk being a focal concern. However, crosstalk impact extends beyond qubit interactions to resonators, which are integral for entangling qubits, facilitating qubit interactions, and reading qubit states. Crosstalk between resonators can inadvertently affect gate operations, undermining qubit fidelity [14], [62], [74], [78].

Additionally, interactions between quantum components, such as qubits and resonators, and their substrate present another layer of complexity. The strong electromagnetic field coupling intrinsic to superconducting qubits becomes problematic with increased substrate size. This enlargement triggers spurious electromagnetic modes that lower the substrate frequency, leading to substrate-qubit crosstalk, inter-qubit crosstalk, and diminishing coherence times [27], [29], [34], [86]. Thus, the challenge in scaling QCs lies in expanding the qubit array while maintaining frequency or spatial isolation to reduce inter-component (qubits and resonators) crosstalk and keeping the substrate size compact to prevent spurious modes [24], [34], [48], [63], [74].

Substantial strides have been made in countering crosstalk, with the primary focus on averting unintended resonance between qubits. Current strategies predominantly include the use of compilers and schedulers in systems with fixed couplings [42], [50], as well as the integration of tunable components in more adaptive architectures [3], [5], [6], [18], [24]. These methods primarily focus on temporal or frequency domain iso-

lation to avoid crosstalk [24], [64], [65]. However, this concentration on specific forms of crosstalk is often insufficient in the system design of processor and has left other critical aspects underexplored. As quantum systems evolve in complexity and scale, a comprehensive understanding and effective mitigation of diverse forms of crosstalk become imperative. Addressing these challenges is essential for enhancing the QC robustness.

In this study, we systematically investigate and address the multifaceted challenges associated with spatial and frequency constraints in inter-qubit and resonator crosstalk, as well as keeping a compact substrate size to suppress substrate crosstalk. Recognizing the complexity of these issues, our solution pivots on a meticulously designed physical layout that not only scales up QCs but also preserves system fidelity amid these multifaceted interactions. This initiative marks a pivotal advancement in quantum chip design, harmonizing the delicate balance between component isolation and integration in sophisticated quantum systems.

To achieve these, we introduce a **frequency-aware electrostatic-based analytical placement framework**, Qplacer (analytical placement refers to the process of determining the optimal physical positions of various components on a substrate; we use placement for short). Qplacer begins with a frequency assigner that allocates distinct frequencies to qubits and resonators, ensuring frequency domain isolation for all interconnected quantum components. We then implement a padding strategy for movable quantum components to setup minimum spacing, and partitioning resonators space into smaller segments for greater flexibility in layout design. Next, we draw a parallel between the quantum device components (such as qubits and resonators), which possess specific frequency properties, and charged particles to strategically position these components. This analogy allows the application of what we term '**frequency repulsive force**', a novel concept that operates exclusively between components sharing similar frequencies. Leveraging this principle enables the strategic positioning of these components, ensuring they are sufficiently distanced from each other spatially. Finally, our framework includes a legalizer step, which integrates the segmented resonators to ensure their integrity. This comprehensive approach not only diminishes crosstalk but also maximizes the scalability of the quantum chip. By optimizing the use of available space, Qplacer results in a compact layout. Fig.1 illustrates a comparison of with classical methods and human-designed layouts, highlighting the advancements of Qplacer.

Our electrostatic-based placement approach, inspired by classical placement framework [20], [33], [56], [57], distinguishes itself with three major differences: (1) We integrate frequency penalties into our cost function to enhance the versatility of models, making it keenly responsive to crosstalk impacts and thereby bolstering the system robustness; (2) To address the unique spatial demands of quantum devices, specifically resonators, we introduce padding and partitioning strategies tailored for quantum-specific needs; (3) We also introduce a specialized legalization process, adept at managing the diverse shapes of quantum components and segmented

resonators, a notable departure from the uniformity commonly observed in classical circuit designs.

The contributions of this work are summarized as follows:

- To our knowledge, this research is the first to comprehensively address the impacts of resonator and substrate crosstalk, along with spatial constraints in quantum components, for the assessment of quantum system fidelity and scalability.
- We propose Qplacer, a framework designed to meticulously craft the physical layout of superconducting QCs effectively mitigating various crosstalk impacts while optimizing for a compact substrate size.
- To achieve this, Qplacer designs **Frequency-Aware Electrostatic-based Placement Engine**, which envisions quantum components as particles, implements a repulsion mechanism for spatially isolating components with similar frequencies.
- Qplacer proposes *padding technique*, *resonator partitioning*, and an *integration legalizer*, facilitating the placement process and addressing the unique challenges of quantum component layout.
- With techniques above, Qplacer enhances fidelity by an average of $36.7\times$ and reduces spatial violations—areas susceptible to crosstalk—by an average of $12.76\times$ compared to classical placer. For area optimization, Qplacer reduces the layout area by an average of $2.14\times$ over manual designs.

II. BACKGROUND

A. Transmon Qubits

Transmon qubits are a prominent type of superconducting qubits, integral to various widely used quantum computer architectures [3], [4], [27], [37], [38], [73]. In superconducting QCs, entanglement between transmon qubits is employed using physical coupling mechanisms such as capacitors [48], [75], resonators (linear couplers) [13], [75], and tunable couplers [3], [67]. This work primarily focuses on fixed-frequency transmon architectures coupled by resonators [47], [79], as shown in Fig.3. The resonator is a quantum harmonic oscillator composed by a linear inductor and capacitor.

Fig.2-a illustrates the physical layout of a transmon qubit. The substrate, usually a dielectric material like silicon, supports two metallic pads connected via a non-linear inductor (Josephson junctions). These components are lithographically printed on the substrate, forming the transmon qubit, a quantum anharmonic oscillator. To facilitate inter-qubit couplings, additional smaller metal pads can be added for connections. Circuit schematic is illustrated in Fig.2-b.

Transmon qubit operates as a multi-level quantum system designed to exhibit an atom-like energy spectrum, as depicted in Fig.2-c. The two lowest energy states, representing binary 0 and 1, are the ground state ($|0\rangle \equiv [1; 0]^T$) and the first excited state ($|1\rangle \equiv [0; 1]^T$). Unlike classical bits, a qubit can exist in a superposition of these states, formulated as $|\phi\rangle = \alpha|0\rangle + \beta|1\rangle = [\alpha; \beta]^T$, where α and β are complex coefficients satisfying the normalization $|\alpha|^2 + |\beta|^2 = 1$. The qubit frequency, ω_q , is defined by the energy gap between

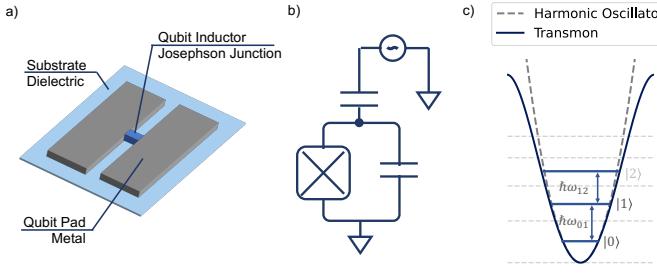


Fig. 2: a) Physical layout of a transmon qubit. b) Circuit diagram of a fixed-frequency transmon qubit featuring a capacitor, Josephson junction, and microwave control line. c) Energy levels of transmon, Josephson junction transforms energy potential from quadratic (dashed dark gray) to sinusoidal (solid blue), leading to distinct energy levels $|0\rangle$ and $|1\rangle$ for computational use, with energy separation $\hbar\omega_{01}$.

the ground state and the first excited state, expressed as $E_{01} = \hbar\omega_q = \hbar\omega_{01}$ (where \hbar is Planck's constant).

B. Gate Operations

Quantum computation relies on qubit gates, operations that transition a qubit between quantum states through unitary transformations, represented mathematically as $|\phi\rangle \rightarrow U|\phi\rangle$, where U is a unitary matrix. This section focuses on gate operations within the fixed-frequency transmon architecture.

Single Qubit Gates: These are implemented by modulating qubits with time-dependent microwave voltage signals. The process, depicted in Fig. 2-b, involves a microwave drive line connected to the qubit via a capacitor. Altering the microwave pulses frequency, phase, and amplitude allows for various single qubit gates execution [13], [48].

Two-qubit Gates: Two-qubit gates are crucial in quantum computation as they provide entangling operations, allowing transformations of one qubit to be conditional on the state of another qubit [13], [47], [48]. In fixed-frequency transmon architectures, microwave drives activate qubit interactions through all-microwave-based two-qubit gates. Advantages of this approach include longer gate lifetimes, simplified control as single-qubit gates, and minimized crosstalk [11], [23]. Resonator induced phase gate (RIP) is the leading technique for implementing these microwave-based gates, compared with other candidates [21], [80]. It does not only retains all the benefits of all-microwave-based two-qubit gates but also is adaptable to a broad range of qubit spectral profiles [22], [59], [69], [72].

The control mechanism of a RIP gate is illustrated in Fig. 3. It operates by coupling two fixed-frequency qubits to a detuned resonator. The gate operation involves applying an off-resonant pulse to the resonator, inducing a phase shift in the qubits without altering the resonator. This mechanism enables the implementation of a Controlled-PHASE (CZ) gate. Mathematically, two-qubit RIP gate operation is described as:

$$U = \exp[-i\dot{\theta}\sigma_z \otimes \sigma_z t] \quad (1)$$

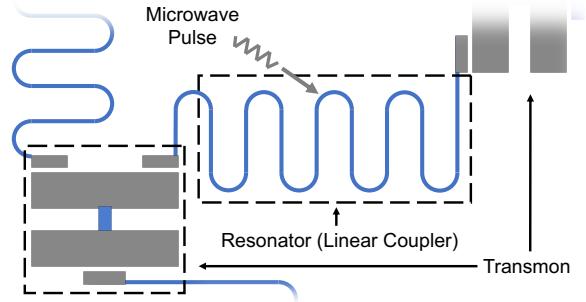


Fig. 3: Circuit diagram of two coupled transmon qubits via a resonator; Two-qubit gates (CZ, controlled Phase gate) are implemented by applying/removing an off-resonant pulse to the resonator.

Here, $\sigma_z \otimes \sigma_z$ represents the joint operation on both qubits, and $\dot{\theta}$, the coupling rate, scales according to:

$$\dot{\theta} \propto \underbrace{\left(\frac{|\Omega V_d|}{2\Delta_{cd}}\right)^2}_{\bar{n}} \frac{\chi}{\Delta_{cd}} \quad (2)$$

where \bar{n} is the average photon count in the resonator, χ the dispersive shift $\chi = g^2/|\omega_r - \omega_q|$, ω_r and ω_q represents the frequency of resonator and frequency of qubit, respectively, and Δ_{cd} the detuning between the drive and the resonator. The Controlled-Z (CZ) gate is accomplished by adjusting the product of $\dot{\theta}t = \pi/4$. Enhancing $\dot{\theta}$ is an effective approach to reducing the gate time t and thus achieving faster gate operations.

III. CROSSTALK CHALLENGES

This section illustrates three primary sources of crosstalk in transmon QCs that hinder the development of larger-scale systems as mentioned in Section I. These include crosstalk between qubits, interference within resonators, and substrate spurious mode impact. The intensity of crosstalk noise is notably influenced by the strength of interactions between qubits [13], [24], [48]. To effectively quantify the impact of crosstalk, we focus on the coupling strength as a representative measure and systematically analyze it using the Jaynes–Cummings Hamiltonian [30], [44], [83].

A. Inter-Qubit Crosstalk

Inter-qubit crosstalk presents a significant challenge in the scaling of superconducting quantum architectures. This issue is primarily rooted in the unintended interactions between qubits, especially when they are either directly coupled via capacitor or in spatial close proximity. For instance, when two qubits are near resonance, their dynamics can be represented by a Hamiltonian model that includes individual system Hamiltonians H_1 and H_2 , and an interaction Hamiltonian H_{int} as shown in Eq.(3):

$$H = H_1 + H_2 + H_{int} \quad (3)$$

Particularly, when qubits are at or near resonance ($\omega_1 \approx \omega_2$), their interaction is described by Hamiltonian H_{res} :

$$H_{res} = \omega_1\sigma_z^1 + \omega_2\sigma_z^2 + g(\sigma_+^1\sigma_-^2 + \sigma_-^1\sigma_+^2) \quad (4)$$

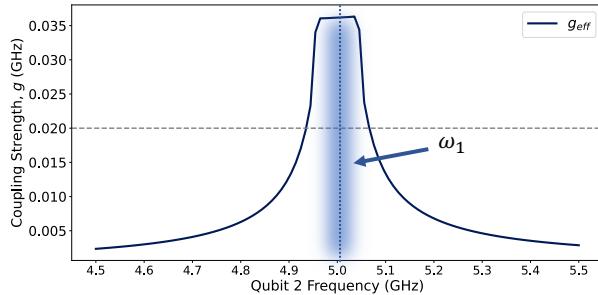


Fig. 4: Coupling strength between two directly connected transmon qubits via a capacitor. ω_n for qubit n . ω_1 is held constant while ω_2 is varied. The peak coupling strength occurs when the two transmons are resonant ($\omega_1 = \omega_2$), depicted in blue shadow. As ω_2 diverges from ω_1 , the residual coupling gradually diminishes. Coupling strength g is typically around $20 \sim 30$ MHz (gray dash line).

Where ω_i represents the frequencies of the i -th qubit. The terms σ_z^i , σ_+^i , and σ_-^i denote the Pauli Z matrices and the raising and lowering operators for the i -th qubit, while g is the coupling strength.

For significantly detuned scenarios ($\Delta = |\omega_1 - \omega_2| \gg g$), Hamiltonian $H_{\text{off-res}}$ applies [13], [48]:

$$H_{\text{off-res}} \approx \omega_1 \sigma_z^1 + \omega_2 \sigma_z^2 + g_{\text{eff}} \sigma_z^1 \sigma_z^2 \quad (5)$$

showing a reduced effective coupling strength $g_{\text{eff}} = g^2/\Delta$. Fig.4 illustrates the above interactions indicating that effective coupling can be modulated by adjusting qubit frequencies.

Existing research predominantly focuses on mitigating crosstalk by fine-tuning the frequencies of directly connected qubits [24], [48], [65], thus reducing residual coupling and preventing the system from entering chaotic states [8], [76]. However, such approaches do not fully address crosstalk in finite-sized circuits where physical distance between qubits introduces parasitic capacitive couplings [58], [76], [95], a factor often overlooked in previous studies.

To analyze these unwanted parasitic capacitive couplings, we consider scenarios with qubits in spatial close proximity with distance d , as depicted in Fig.5-a. The Hamiltonian of such a system, analogous to Eq.(5), now includes the parasitic coupling strength g which is defined as [48]:

$$g = \frac{1}{2} \sqrt{\omega_1 \omega_2} \frac{C_p}{\sqrt{C_1 + C_p} \sqrt{C_2 + C_p}} \quad (6)$$

Where C_p is the parasitic capacitance between two qubits and C_i is the capacitance of qubit i . Eq.(6) shows parasitic coupling strength g depends on parasitic capacitance C_p , which is inversely related to the distance between qubits. Fig.5-b shows the simulated C_p value from Qiskit Metal [35], [36], [63], which demonstrates an increase in parasitic capacitance as qubits are positioned closer, leading to a rise in both parasitic coupling strength g for two resonated qubits and effective coupling g^2/Δ for two detuned qubits. Therefore, effective mitigation of inter-qubit crosstalk requires assigning distinct frequencies to each pair of connected qubits

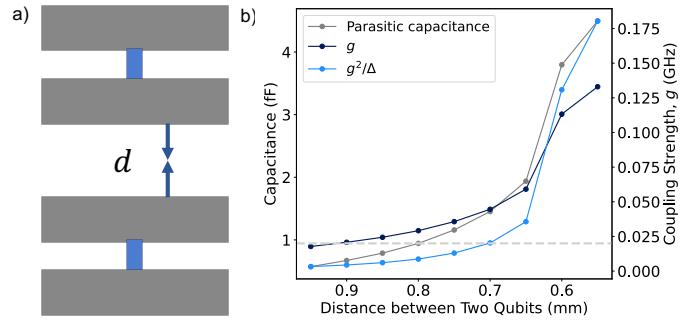


Fig. 5: a): Separation distance d between transmon qubits. b): Variation in coupling strength g , effective coupling strength g_{eff} and parasitic capacitance C_p with the distance d between two transmon qubits, indicating increased capacitance and coupling strength as d decreases.

and maintaining adequate physical separation, particularly for qubits with similar frequencies.

B. Resonator Crosstalk

In Section III-A, we discuss inter-qubit crosstalk, highlighting the need for isolation in both spatial and frequency domains. However, the available frequency spectrum for qubits is typically constrained to around 5GHz [27], [42], limited by peripheral control device costs and thermal noise vulnerability [48], [69], [97]. Limited frequency spectrum leads to “frequency crowding” in larger systems or programs employing parallelism, complicating the frequency assignment. Furthermore, architectures with direct capacitive coupling require significant tuning of qubit frequencies or the use of tunable couplers. These adjustments can introduce additional dephasing and risk accidental resonance with other qubits or environments, potentially resulting in crosstalk [13], [75].

In addressing the constraints of direct capacitor coupling and relief the frequency crowding, using resonators as quantum buses emerges as an effective alternative for mediating inter-qubit crosstalk, offering selective coupling advantages [13], [31]. The Hamiltonian of qubit-resonator interaction is:

$$H = \frac{\omega_q}{2} \sigma_z + \omega_r a^\dagger a + g(\sigma_+ a + \sigma_- a^\dagger) \quad (7)$$

where a^\dagger and a are the creation and annihilation operators for resonator, ω_q and ω_r are qubit and resonator frequency, respectively. Resonators provide distinct operational regimes. In the vacuum Rabi oscillation regime, strong energy exchange occurs when qubit and resonator frequencies are close. Conversely, in the dispersive regime where $\Delta = |\omega_q - \omega_r| \gg g$, the Hamiltonian approximates to:

$$H \approx \frac{\tilde{\omega}_q}{2} \sigma_z + \omega_r a^\dagger a + \chi \sigma_z a^\dagger a \quad (8)$$

$\chi = g^2/\Delta$ denotes the effective qubit-resonator coupling strength. In this regime, energy transfer is negligible [13], [75].

Although resonator is beneficial in mitigating inter-qubit crosstalk, it presents other challenges. As quantum oscillators, resonators can inadvertently couple with others at or near

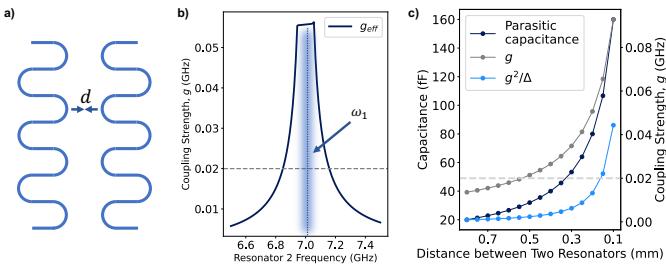


Fig. 6: a): Diagram illustrating the distance between resonators b): Maximum coupling strength at resonator resonance ($\omega_{r1} = \omega_{r2}$). c): Coupling strength and parasitic capacitance versus distance d between two resonators, as shown in (a). Decreased d leads to increased coupling strength.

resonance frequencies, leading to potential crosstalk [54], [62]. The coupling strength escalates from g^2/Δ to g with narrowing frequency detuning. Additionally, close proximity between resonators also induces parasitic capacitive coupling, described by $g \propto C_p/\sqrt{C_r^1 C_r^2}$, where C_p is the parasitic coupling capacitance and C_r^i is the i -th resonator capacitance [70]. Fig.6 illustrates these effects, showing both the frequency-dependent coupling strength and the rise in parasitic coupling as resonators come closer [62], [68], [70]. These unintended energy exchanges between resonators pose more severe challenges than inter-qubit crosstalk. They not only affect qubit fidelity and gate operations but also complicate error correction efforts by violating principles of error locality and independence [26], [77].

Moreover, resonators consume substantial substrate area due to its considerable wirelength as shown in Fig.3, which imposes additional spatial constraints in scaling up QCs. Therefore, addressing the complexities of resonator crosstalk necessitate meticulous frequency assigning and strategic layout designs in balancing the need for more qubits against the challenges in resonator placement.

C. Substrate Spurious Electromagnetic Mode

Substrate limitations is also a critical concern in scaling up superconducting QCs. Increasing the substrate size to accommodate more qubits is not a straightforward solution in NISQ systems, particularly due to the emergence of spurious electromagnetic modes (box modes) that arise with increased substrate size [29], [34]. These modes enforce a frequency constraint on the components of the chip, not allowing them to exceed the first eigenmode (TM110) of the substrate [34], [74]. For instance, TM110 drops from 12.41 GHz to 6.20 GHz when increasing from a $5 \times 5 \text{ mm}^2$ to a $10 \times 10 \text{ mm}^2$ substrate size, limiting the available frequency spectrum for qubits and resonators [34], [74]. While efforts have been made to mitigate these modes [29], [81], [86], the physical size of superconducting chips is typically limited to about $10 \times 10 \text{ mm}^2$ [34], [74]. Additionally, substrate area directly influences manufacturing costs and fridge requirements [27], [66]. Therefore, enhancing the utilization of available substrate space through innovative

analytical placement techniques becomes a viable approach to scale up quantum computers within these physical constraints.

IV. FREQUENCY-AWARE ANALYTICAL PLACEMENT

A. Overview

The proposed placement framework, as illustrated in Fig.7, outlines a systematic approach for optimizing the layout of quantum processors. It requires two primary inputs: a target connectivity topology and the allocation of frequencies to components, determined by the available frequency spectrums. The initial stage involves quantum-specific placement preprocessing, where movable components are equipped with padding and resonators space are divided into smaller segments for better management. Subsequently, the framework conceptualizes quantum device components, each with unique frequency characteristics, as charged particles. The placement engine then optimizes the locations of these particles (quantum components) and disperses them across the substrate by balancing the frequency repulsive forces of the components. The process concludes with the integration of the segmented resonator, establishing the final layout configuration.

B. Quantum Specific Placement Preprocessing

1) *Quantum Components Padding:* Padding is an essential technique for establishing minimum spacing between quantum components to mitigate crosstalk in quantum layout. As outlined in Section III, close proximity of quantum components can lead to parasitic capacitive coupling, consequently introducing unwanted crosstalk, as demonstrated in Fig.5 and 6-c. Both the direct coupling strength g and the effective coupling strength g^2/Δ surge to undesirable levels when separation distance d is small, leading to energy leakage even among detuned components [62], [76].

In placement optimization, placement engine might inadvertently position components in close adjacency, potentially causing crosstalk issues. To counteract this, padding intentionally adding extra space around each quantum component. This method establishes predefined minimum distances, denoted as d_q for qubits and d_r for resonators, ensuring adequate spatial separation between each component and its neighbors. It is visually represented in Fig.8-a and 8-b.

2) *Resonator Partitioning:* Resonator partitioning is another innovative technique to enhance the flexibility and scalability of QCs, in addressing the challenge of resonator area overhead, as highlighted in Section III-B. This technique involves dividing the required space allocated for each resonator into smaller modular segments. The process starts by reshaping the allocated resonator space into a compact rectangle of equivalent area, followed by defining a basic wire block size, l_b . Each reshaped resonator space is subsequently segmented based on this predetermined block size, as illustrated in Fig.8-c. This strategy ensures the preservation of the resonators' fundamental frequency properties, while allowing individual segments to be placed within the substrate, adhering to crosstalk constraints. Furthermore, this partitioning allows us to navigate the complexity of chip real estate, particularly

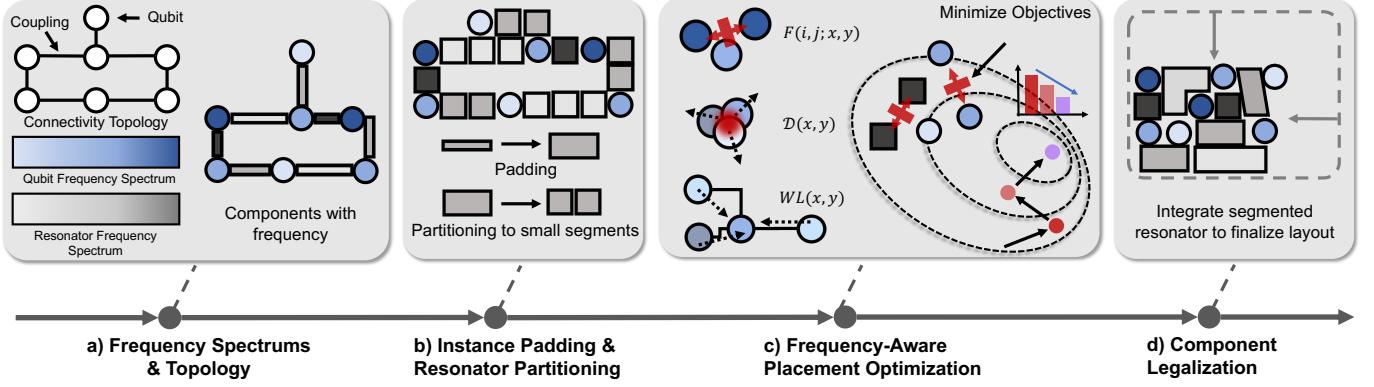


Fig. 7: Overview of Qplacer. **a:** Target connectivity topology and frequency allocation for components (qubits and resonators), based on available frequency spectrums. **b:** Padded qubits and resonators, with resonators segmented for layout flexibility **c:** Frequency-aware placement engine optimizing components' position for crosstalk mitigation, area minimization, and density balance using **frequency repulsive forces**. **d:** Integration legalizer finalizes layout, ensuring resonator coherence.

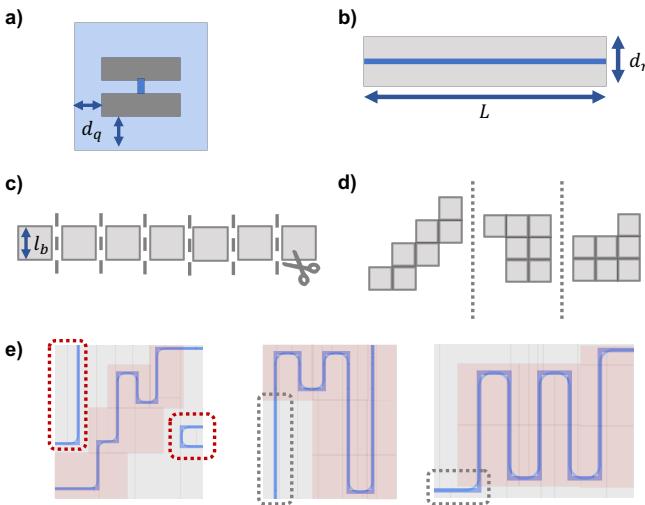


Fig. 8: **a):** Qubit padded with distance d_q . **b):** Padded resonator with wirelength L and padding distance d_r . **c):** Reshaped resonator space from (a), transformed into a compact rectangle, partitioned into segments of size l_b , retaining frequency consistency as indicated by color. **d):** Flexible placement of resonator space segments to accommodate diverse layout designs. **e):** Generated resonator routing using Qiskit Metal [36] based on the segmented placement (red shadow) in (d). red dotted box: obstacle components, gray dotted box: connections between meander resonators and qubit pins.

in densely populated areas where conventional rectangular resonator layouts are impractical. Fig.8-d showcases potential reshaped patterns for resonators. *It is important to clarify that the segmented blocks serve solely as placeholders to reserve space for the eventual placement of the resonators, rather than to physically partition the resonators themselves. The resonators are then re-routed based on the new positions of these segmented blocks.* Fig.8-e illustrated the examples of actual resonator routing in Qiskit Metal [36], following the sequence established in Fig.8-d, where the red shadow indicates the space reserved. In the left figure of Fig.8-e, the target resonator navigates around an obstacle (highlighted in a red dotted box), demonstrating the adaptability and versatility

of this method. *It is crucial to understand that resonator partitioning influences only the placement of the location of resonator, without altering its dimensional attributes such as gap width, etch depth, or metal heights. Moreover, our routing strictly adheres to the configurations in Qiskit Metal [36] to avoid sharp corners that could lead to potential surface losses, thereby minimizing associated risks [60], [93], [94].*

C. Quantum Analytical Placement

The complexity of determining quantum component locations while adhering to crosstalk constraints presents significant computational challenges. Its inherent computational intricacy means even rudimentary tasks deemed NP-complete. To navigate this complexity, our methodology bifurcates the process into two distinct stages: placement and legalization.

1) Frequency-aware Electrostatic-based Placement Engine: Our proposed frequency-aware electrostatic-based placement engine is a pivotal component in achieving efficient substrate utilization and mitigating crosstalk in designing quantum device layout. This engine translates the constraints of crosstalk into an objective function, which is then iteratively minimized to approximate an optimal layout. Within this framework, both qubits and resonator segments are treated as movable instances $i, i \in I$, each characterized by unique frequency properties ω_i

Frequency Constraint: In addressing the spatial crosstalk constraints detailed in Section III, quantum instances such as qubits and resonators necessitate to repel other instances that are on or near resonance in close distance proximity to prevent unintentional interactions. This phenomenon is analogous to charged entities repelling each other in an electrostatic field. Drawing inspiration from electrostatic systems, our model treats movable instances as charged entities, exerting a '**frequency repulse force**' F on each other when they share similar frequencies, as illustrated in Fig.9-a.

$$F(i, j; x, y) = \frac{\tau(\omega_i, \omega_j, \Delta_c)}{(x_i - x_j)^2 + (y_i - y_j)^2} \quad (9)$$

In Eq.(9), x_n and y_n denote instance n 's coordinates, while Δ_c represents the detuning threshold to avoid resonance. Res-

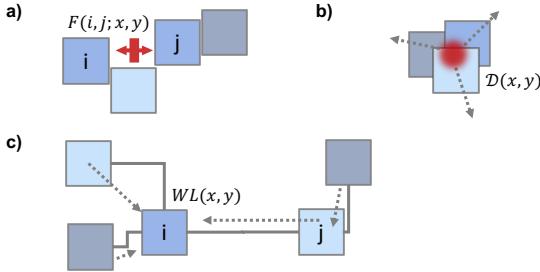


Fig. 9: Frequency-aware placement engine visualization with instances color-coded by frequency: **a)**: Frequency constraint F repels resonant instances in close proximity (red arrows depict frequency repulsive forces). **b)**: Density constraint \mathcal{D} disperses instances to achieve target density $\hat{\mathcal{D}}$ (red dots represent areas of high density). **c)**: Wirelength WL optimization minimizes substrate area by drawing instances closer together.

onance in subsequent discussions implies a detuning smaller than Δ_c . The crosstalk indicator $\tau(\cdot)$ activates (1) for frequency differences within this threshold ($|\omega_i - \omega_j| \leq \Delta_c$) and deactivates (0) otherwise. This setup selectively applies force to instances with near-resonance frequencies, optimizing their positioning to reduce crosstalk.

To ensure that resonator segments, which are partitioned for layout flexibility, are not inappropriately dispersed, we modify our frequency repulse force as shown in Eq.(10)

$$F(i, j; x, y) = \frac{\tau(\omega_i, \omega_j, \Delta_c)}{(x_i - x_j)^2 + (y_i - y_j)^2} \cdot (1 - \delta(r_i, r_j)) \quad (10)$$

Where r is the resonator index (only checking for resonator segment blocks). $\delta(\cdot)$ is the Kronecker delta function, which is 1 for identical frequencies and 0 otherwise. $(1 - \delta(r_i, r_j))$ indicator ignores the instances from the same resonator.

Note that, to efficiently compute the frequency repulse force F , a frequency collision map is constructed for each quantum instance before placement. This map identifies potential crosstalk instances, excluding those belonging to the same resonator. Typically, the map contains dozens to hundreds of instances for each quantum instance under consideration. During the placement optimization process, only the collision map is iterated through, avoiding the computationally expensive ‘all-to-all’ iterations.

Density Constraint: Frequency constrain only separate the instance with resonant frequency rather than impact the detuned instances, which results the illegally overlapped scenario among detuned instances. Density constrain is next introduced to resolve this problem, which restrict the density at any location on the substrate remains below a predefined target value $\hat{\mathcal{D}}$.

$$\mathcal{D}(x, y) \leq \hat{\mathcal{D}} \quad (11)$$

Where $\mathcal{D}(x, y)$ represents the density at a given location in the layout. This constraint is interpreted as potential energy within the electrostatic analogy. The electric potential and field distribution are governed by Poisson’s equation, incorporating charge density distribution as input [56].

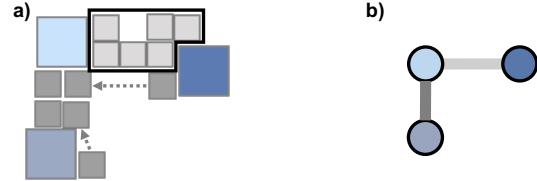


Fig. 10: **a)**: Resonator integration legalizer fixes legalized resonator and integrate the remaining resonator from its largest segment cluster. **b)**: connectivity topology is shown in **b)**

Objective Function and Optimization: The ultimate objective of placement engine is to efficiently allocate all movable instances within the legal space of the quantum chip. To efficiently quantize the area usage, we utilize the wirelength concept, a common metric in classical placement, denoted as $WL(e, x, y)$. Here, e in E is a connection between two components, and this function measures the length of each wire e . This approach underpins the formulation of our comprehensive objective function.

$$\min_{x, y} \sum_{i, j \in I; e \in E} WL(e; x, y), \quad (12)$$

$$\text{s.t. } \mathcal{D}(x, y) \leq \hat{\mathcal{D}}, F(i, j; x, y) \quad (13)$$

Penalty method is adopted to efficiently solve this constrained optimization problem, by transforming it into a series of unconstrained problems. The transformed objective is:

$$\min_{x, y} \sum_{i, j \in I; e \in E} WL(e; x, y) + \lambda \mathcal{D}(x, y) + \lambda_f F(i, j; x, y) \quad (14)$$

F and \mathcal{D} denotes the frequency penalty and density penalty, respectively, which facilitates the proper dispersion of instances across the layout. To meet these constraints, the parameter λ and λ_f are increased progressively. With smaller parameters, the placement engine focus is predominantly on reducing the area regarding wirelength. As these parameters escalates, there is a seamless shift from prioritizing area minimization to achieving a balance between area and constrain penalty optimization. Consequently, movable instances disperse methodically, ensuring the area remains optimal.

2) Integration-Aware Legalization: The final phase of Qplacer entails an integration-aware legalization, designed to legalize component arrangement. The process commences with qubit legalization, temporarily sidelining segmented resonator blocks. This involves a greedy spiral search to identify viable, non-overlapping locations for movable qubits [53], followed by a min-cost flow refinement to minimize displacement [88]. Once qubit positions are set, attention shifts to arranging segmented resonator blocks using a modified Tetris-like methodology [17], placing blocks from left to right ensuring minimal displacement and adherence to established orders.

Post-Tetris refinement, it involves a thorough evaluation of the placement, particularly concentrating on the integration of resonator segments. The criterion for successful integration

Algorithm 1 Integration-Aware Legalization

Require: Placement solution (x_i, y_i) for all instance I , $\forall i \in I$, the segment list v_r for each resonator R , $\forall r \in R$, All qubits Q , $R \cup Q = I$, resonant checker $\tau(\cdot)$, qubit legalizer Q-LG(\cdot), segment Tetris legalizer T-LG(\cdot), and resonator integration legality checker rilc(\cdot)

Ensure: legalized placement solution with resonator integration

- 1: $x_q, y_q \leftarrow \text{Q-LG}(x_q, y_q), \forall q \in Q$ \triangleright Legalize qubits
- 2: $x_i, y_i \leftarrow \text{T-LG}(x_i, y_i), \forall i \in I, i \notin Q$ \triangleright Legalize segments
- 3: **for** $v_r \in R$ **do**
- 4: **if** $\text{rilc}(v_r)$ **then**
- 5: $x_i, y_i \leftarrow \forall i \in v_r$ \triangleright fix segments
- 6: **else**
- 7: $C_{v_r} \leftarrow v_r$ \triangleright find largest segment cluster
- 8: **end if**
- 9: **end for**
- 10: $I_u \leftarrow I, R_u \leftarrow R$ \triangleright get unfixed segments and resonators
- 11: **for** $v_r \in R$ **do**
- 12: $C_{v_r} \cdot \tau(C_{v_r}) \leftarrow C_{v_r}, I_u$ \triangleright swap segments
- 13: **if** $\text{rilc}(C_{v_r})$ **then**
- 14: $x_i, y_i \leftarrow \forall i \in v_r$ \triangleright fix segments
- 15: **end if**
- 16: **end for**

mandates that all segments of a resonator should be in close proximity to at least one other segment from the same resonator. Each resonator is examined to verify its compliance with this criterion. For resonators that comply, their segments position are finalized. Conversely, for those that fall short, we find its largest contiguous segment clusters and initiate a swapping process between the neighboring instances of cluster and scattered segments associated resonant checking $\tau(\cdot)$, aiming to enlarge the clusters. This procedure ensures that resonators can be seamlessly reassembled from its constituent segments. The detailed legalization flow is described in Algorithm 1.

V. EVALUATION METHODOLOGY

A. Benchmarks

We conduct performance evaluations using a range of quantum device connectivity topologies and NISQ benchmarks, as outlined in Table I. These topologies, which are either prevalent in industrial applications or designed for algorithmic efficiency, vary in qubit count, ranging from 25 to 127. This diversity in quantum device structures allows us to thoroughly assess our engine's scalability and adaptability across different quantum processor configurations.

B. Evaluation Comparisons

The following placement schemes are assessed in several comparative evaluations to test the performance of our frequency-aware electrostatic-based quantum placer.

- **Human:** The optimal manually optimized, crosstalk-free design represented by IBM's layout, positions qubits in a 2D grid according to the connectivity topology, minimizing total edge length. Qubits are connected only to their nearest neighbors, with resonators strategically placed to prevent intersections or overlaps. The distance D between two qubits is determined by the resonator's area, which is calculated

TABLE I: TOPOLOGIES AND BENCHMARKS

Topology	Qubits	Description
Grid	25	Quantum error correction friendly architecture [3]
Heavy Hex	27	Falcon processor from IBM [42]
Heavy Hex	127	Eagle processor from IBM [42]
Octagon	40	Aspen-11 processor from Rigetti [2]
Octagon	80	Aspen-M processor from Rigetti [2]
Xtree	53	Pauli-String efficient architecture in Level 3 [51]
Benchmark	Qubits	Description
BV	4, 9, 16	Bernstein-Varzirani algorithm [9]
QAOA	4, 9	Quantum Approximate Optimization Algorithm [25]
Ising	4	Linear Ising model simulation of spin chain [7]
QGAN	4, 9	Quantum Generative Adversarial Network [55]

as the product of its length (L) and padding size (d_r). The resonator's area is then reshaped to align with the padded qubit size $(L_q + 2d_q)$, yielding $D = \frac{L \times d_r}{L_q + 2d_q}$ [39], [73].

- **Classic:** The state-of-the-art Classical placement engine [53] uses default hyperparameter settings and incorporates resonator partitioning technique detailed in Section IV-B2.
- **Qplacer:** Our proposed frequency-aware electrostatic-based quantum placement engine. For fair comparison, it adheres to the same hyperparameter settings as **Classic** baseline.

C. Experiment setup

Tool Implementation: The framework was developed using Python, utilizing PyTorch for optimizers and APIs, and C++ for low-level operations. This development was based on the open-source placement engine [53]. All experimental data were obtained from a Linux machine equipped with an Intel(R) Xeon(R) CPU E5-2687W v4 @ 3.00GHz.

Architectural Features: We utilize standard symmetric frequency-fixed pocket transmon qubits as shown in Fig.2-a, each having $400 \times 400 \mu\text{m}^2$ referred from Qiskit Metal [36] with nearly constant anharmonicity $\alpha/2\pi = (\omega_{12} - \omega_{01})/2\pi \approx 310\text{MHz}$ [42]. The available qubit frequency range Ω is set to realistic values 4.8~5.2 GHz in line with experimental data from devices [42]. The available resonator frequency range Ω_r is set to realistic values 6.0~7.0 GHz in line with experimental data from literature [59], [69], [81], [87]. The resonator lengths correspond to frequencies within 10.8~9.2 mm, calculated using $f = v_0/2L$, where $v_0 \sim 1.3 \times 10^8 \text{m/s}$ is the speed of light in wavelength [13].

To comprehensively evaluate impact of spatial isolation with catering realistic variation in fabrication, the padding length for qubit and resonator are aggressively set to $d_q = 400\mu\text{m}$ and $d_r = 100\mu\text{m}$, respectively (the minimum distance between two adjacent components are the sum of their paddings). While detuning threshold Δ_c is set to 0.1GHz. These setups result in reasonable coupling strength for any detuned qubits, but higher coupling strength between two resonance qubits, as illustrated in Fig.5 and 6-c. We adopt a 3D packaging approach, focusing on qubits and bus resonators while omitting readout resonators [37], [38]. Ground plane is currently not considered.

Metrics: To assess crosstalk susceptibility in our placement experiments, we analyse the layout quality from three perspectives:

tives: general algorithm program fidelity, area and frequency hotspots proportion.

(1) General algorithm program fidelity: program fidelity \mathcal{F} is modeled using three terms to estimate the worst case fidelity of a program benchmark under crosstalk and decoherence noises, similar to the fidelity metric used in [3], [24]:

$$\mathcal{F} = \prod_{q \in Q} (1 - \epsilon_q) \cdot \prod_{g \in G} (1 - \epsilon_g) \cdot \prod_{r \in R} (1 - \epsilon_r) \quad (15)$$

where ϵ_q represents the qubit error from single qubit gates, two-qubit gates and decoherence, decoherence error represent by decay constants T_1 and T_2 during both idle and gate operation periods [46]. The crosstalk gate error for qubits, ϵ_g , occurs when two qubits violate spatial constraints, akin to being linked by a direct capacitive coupling as detailed in Section III-A. This error results from Rabi oscillations, periodic energy exchanges between the qubits (state $|01\rangle$ and $|10\rangle$, state $|11\rangle$ and $|20\rangle$), driven by their effective coupling strength g_{eff} . The transition probability is modeled as $\text{Pr}[t] = \sin^2(g_{\text{eff}}t)$ [6], [24], the corresponding crosstalk error for idle qubits is:

$$\epsilon_g(\Delta, t) = 1 - \sin(g_{\text{eff}}(\Delta)t)^2 \quad (16)$$

Similarly, ϵ_r accounts for crosstalk errors among resonators under spatial violations, analogous to those measured for qubits. The parasitic capacitance depends on the adjacent length. It is crucial to note that these fidelity calculations pertain only to actively engaged physical qubits and resonators in layouts, as errors in inactive elements do not compromise the program's overall fidelity.

(2) Area: We define the layout's area using two parameters. $A_{\text{mer}}(I)$, which is the area of the minimum enclosing rectangle that encompasses all instances, providing a measure of the layout's overall spatial requirements; $A_{\text{poly}}(I)$ represents the total area covered by all individual instances, calculated as the sum of their polygonal areas. The substrate area utilization ratio is determined by:

$$\frac{A_{\text{poly}}(I)}{A_{\text{mer}}(I)} \quad (17)$$

which quantifies the efficiency of space usage within the defined layout perimeter.

(3) Frequency Hotspot Proportion: we introduce a novel metric, *Frequency Hotspot Proportion* (P_h) to quantify the potential for crosstalk by identifying '**frequency hotspots**'. These are defined as regions where instances are closely positioned with frequency differences smaller than a predefined threshold Δ_c , which signifies a heightened risk of crosstalk. The metric is calculated as follows:

$$P_h = \frac{\sum_{i,j \in I} (p_i \cap p_j) \cdot d_c(p_i, p_j) \cdot \tau(\omega_i, \omega_j, \Delta_c)}{A_{\text{poly}}(I)} \quad (18)$$

Here, p_n represents the polygon of instance n , $p_i \cap p_j$ is the intersection length between two instances, $d_c(p_i, p_j)$ denotes the centroid distance between their polygons, and τ is a function that assesses frequency proximity based on the threshold Δ_c . This metric effectively translates crosstalk impacts into measurable spatial terms, facilitating a detailed analysis of

crosstalk risks in quantum computing layouts and helping identify vulnerable qubits. For simplicity, the term "frequency hotspot" is often shortened to "hotspot" in discussions.

VI. RESULTS

A. Fidelity Estimation

Fig.11 presents the worst-case overall fidelity for various placement strategies, all subjected to the same hyper-parameters and estimated using our noise model—Eq.(15). And the upper subfigure in Fig.12 is the average value of Fig.11 across the topologies. The size of the resonator segments, l_b , is fixed at 0.3 mm, which was found to be optimal as detailed in Section VI-D. Given that the number of required qubits for the application is fewer than the physical qubits available on each topology, each mapping evaluation is confined to a subset of the device's qubits. To rigorously evaluate each layout, we conducted evaluations on 50 different subsets of physical qubits, aiming to encompass all the physical qubits across different topological layouts. We utilized Qiskit's mapping with L3 optimization to enhance the mappings, drawing on basis gates from IBMQ [42] to minimize the impacts from software-level by reducing circuit depth and gate numbers. This approach allows for the assessment of performance consistency across all qubits within a chip, addressing concerns that a few mapping samples might not accurately reflect the overall system performance. For consistency and fair comparison, the same mappings were used across all benchmarks and placers. Each bar in the figure represents the average fidelity of these 50 mappings for a benchmark on a specific topology layout.

Classic placer, which does not account for crosstalk, generally suffers from a significant reduction in fidelity across most circuits and topologies, managing only to produce moderate layouts for simpler topologies with fewer qubits such as grid. In contrast, Qplacer consistently achieves superior performance, improving fidelity by an average of $36.7 \times$ across all benchmarks and topologies, as illustrated in the upper subfigure of Fig.12. This includes complex benchmarks like QAOA-9, where Qplacer still maintains relatively high fidelity across various topologies. The success of Qplacer over classic strategies can be attributed to its heuristic approach of optimizing instance positions based on frequency relationships.

B. Frequency Hotspots Proportion

Fig.12 primarily illustrates the proportion of frequency hotspots, P_h , and the number of qubits affected by these hotspots under different placement strategies. Qplacer, which employs a frequency-aware placement engine and an integration legalizer, excels in achieving spatial isolation for movable instances, with an average violation rate of only 0.46%. In contrast, the classic placement engine, which does not consider crosstalk, exhibits a higher average hotspot proportion of 5.87%, indicating that Qplacer is approximately $12.76 \times$ more effective in reducing crosstalk-related spatial violation.

The correlation between program fidelity and P_h is depicted in the subfigures of Fig.12, with the upper subfigure showing

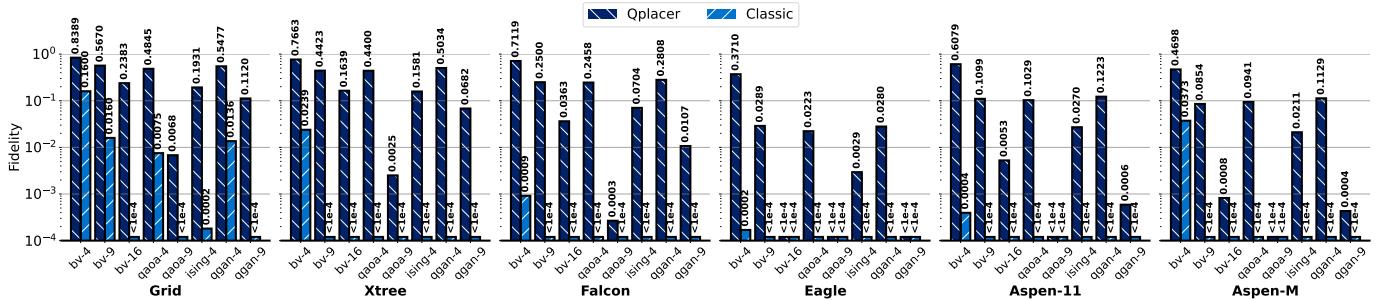


Fig. 11: Fidelity estimation from various placement strategies. A higher fidelity value indicates a better performance. Across all benchmarks, Qplacer consistently outperforms the Classic baseline, demonstrating its superior efficacy in maintaining higher fidelity levels in layouts.

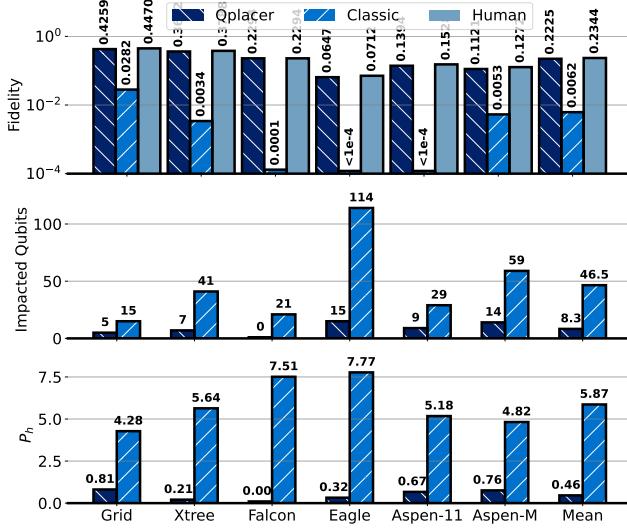


Fig. 12: A comparison of different placement schemes based on three metrics: average program fidelity, number of impacted qubits, and the proportion of frequency hotspots. For the latter two metrics, lower values indicate better performance. Across all tested topologies, Qplacer consistently excels in reducing frequency hotspots.

average benchmark fidelities for each topology and the lower subplot displaying P_h . These visuals indicate that program fidelity is inversely proportional to P_h , validating the effectiveness of P_h as a metric for assessing layout quality.

Further analysis reveals that the number of qubits impacted by hotspots is not strictly linear increase but tends to be exponential with the hotspot proportion, highlighting the non-localized nature of resonator crosstalk; even a minor misplacement can significantly affect the fidelity of all connected qubits. For instance, in the Eagle layout using a classical placement strategy, while the hotspot proportion is about 7.77%, this condition adversely affects over 110 qubits, which constitutes more than 90% of the total qubits (127). Such findings underscore the critical importance of strategic placement in mitigating the pervasive impact of crosstalk.

C. Area Optimization

Fig. 13 offers a comparative analysis of the minimum substrate area required (A_{mer}) across various placement strategies, benchmarked against Qplacer’s A_{mer} . Human-designed layouts, which typically feature qubits arranged in a 2D grid with considerable spacing (as seen in systems such as those

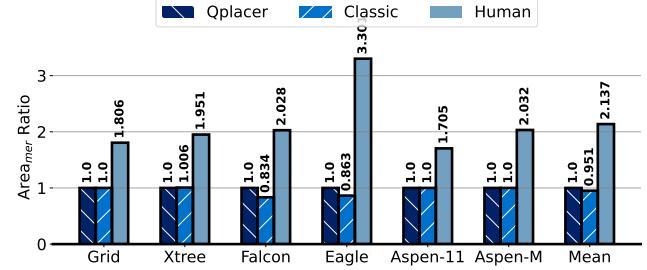


Fig. 13: Minimum enclosing rectangle area (A_{mer}) ratios of placement schemes relative to Qplacer. A smaller ratio is preferred as it indicates a more compact layout. Qplacer provides consistent benefits, outperforming the competing schemes.

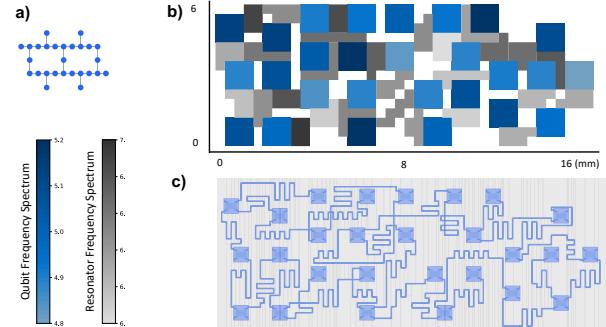


Fig. 14: a): Input frequency spectrums and connectivity topology (Falcon); b): Optimized layout by Qplacer. c): Generated GDS file from Qiskit Metal [36] based on the optimized layout in (b).

by [42], [73]), often occupy larger substrate areas. Although these layouts are effective in minimizing crosstalk among on-chip instances, they may increase the likelihood of substrate spurious effects, potentially degrading system fidelity.

Layouts generated by classical placement engines have areas comparable to those produced by Qplacer, since they share the same hyper-parameters. In stark contrast, Qplacer enhances substrate area utilization, achieving on average a $2.14\times$ improvement compared to handcrafted layouts. This efficiency underscores Qplacer’s dual capability in optimizing layout dimensions and enhancing fidelity. By balancing frequency constraints with wirelength optimization, Qplacer consistently delivers compact layouts with reduced hotspot occurrences.

Fig. 14-b presents a layout prototype for Falcon [42]. Despite some residual unoccupied space, Qplacer efficiently minimizes the required area while maintaining fidelity. The gray areas denote space reserved for resonators, as detailed in Section IV-B2. This prototype serves as a reference for users to fine-

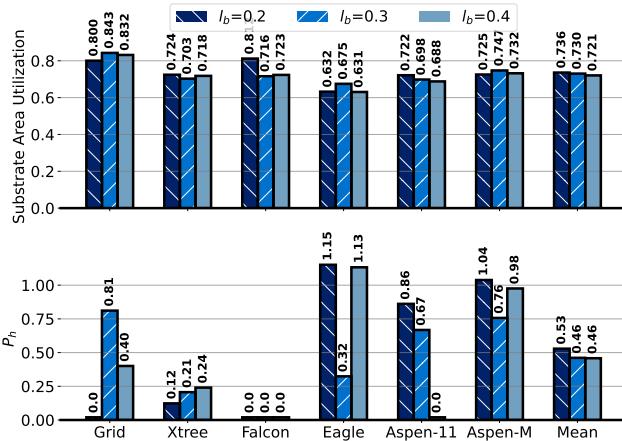


Fig. 15: Substrate area utilization and hotspot proportion P_h for Qplacer with different resonator segment sizes l_b (in mm).

TABLE II: COMPARISON ON PLACEMENT TIME, RT represents runtime in seconds, Avg represents the average runtime per iteration

Topology	$l_b = 0.2$			$l_b = 0.3$			$l_b = 0.4$		
	#cells	RT	Avg	#cells	RT	Avg	#cells	RT	Avg
Grid	1050	8.1	0.024	490	4.6	0.017	299	4.6	0.017
Xtree	1393	15.0	0.035	660	5.2	0.017	410	4.9	0.017
Falcon	744	7.6	0.020	354	6.4	0.017	218	3.7	0.017
Eagle	3810	56.1	0.165	1801	11.3	0.044	1104	7.0	0.024
Aspen-11	1272	12.4	0.030	598	7.2	0.018	369	6.5	0.017
Aspen-M	2787	28.5	0.093	1310	12.5	0.030	799	6.4	0.019
Mean	1843	21.3	0.061	869	7.9	0.023	533	5.5	0.018

tune the layout and effectively route the resonators. Moreover, an example layout in GDSII format, derived from Fig.14-b using Qiskit Metal, is displayed in Fig.14-c to illustrate the practical application of our optimized layout prototype.

D. Sweeping the Segment Size

This section evaluates the performance of resonator partitioning by exploring the impact of various resonator segment sizes (l_b) on layout optimization and placement runtime. The outcomes of the layout evaluations are depicted in Fig.15, while the corresponding placement runtimes (measured in seconds), average runtimes (in seconds), and the counts of instances (#cell) are detailed in Table II.

We analyzed three segment sizes: $l_b = 0.2, 0.3$, and 0.4 mm. Analysis identified $l_b = 0.3$ mm as the optimal segment size for these topologies, as it offers the best balance between substrate utilization and hotspot proportions, trading less than 1% in area utilization for a 16.3% reduction in hotspots. Furthermore, as shown in the last row of Table II, using $l_b = 0.2$ mm increases the number of instances by factors of $2.1\times$ and $3.5\times$ compared to $l_b = 0.3$ mm and $l_b = 0.4$ mm, respectively. This increase in instances correlates with runtime increases of $2.7\times$ and $3.87\times$, respectively. These results highlight that the smallest segment size ($l_b = 0.2$ mm) may not always be the most efficient choice; while it enhances area efficiency, it also leads to a higher number of instances, longer runtimes, and increased hotspot proportions.

Runtime data in Table II also demonstrates scalability of Qplacer in handling an increased number of qubits efficiently, enabling users to generate optimized layouts within seconds.

VII. RELATED WORK

Crosstalk in quantum computing has been a critical issue addressed by numerous studies, with primarily focusing on inter-qubit interactions. Strategies to mitigate this involve the use of compilers and schedulers in fixed coupling systems [42], [50], [52], [99] and the incorporation of tunable components in more adaptive architectures [3], [5], [6], [18], [24]. These approaches largely center on temporal or frequency isolation to prevent crosstalk [24], [64], [65], [98], [100]. However, the importance of spatial isolation is often underemphasized, which leads to detrimental parasitic couplings [58], [76], [95].

In terms of resonator-based crosstalk, modifications in hardware design, such as material selection and frequency detuning, have been explored [34], [62], [68]. Another significant factor is substrate-induced crosstalk, which escalates with increased substrate size, leading to spurious electromagnetic modes [29], [81], [86]. Efforts to enhance substrate scalability include advanced packaging techniques [15], [34], [74], through-silicon vias (TSV) integration [28], [86], [89], [96], high-dielectric substrates [15], [61], [92], air-bridge crossovers [19], and flip-chip lids [1]. Despite these advancements, spurious modes remain a bottleneck, limiting substrate size and thus impacting quantum computing scalability [10], [13], [66]. The concept of a quantum chiplet model [40], [84] has been introduced as a potential solution to these scalability issues.

From the perspective of substrate utilization for scaling up quantum processors, placement engines play crucial roles. Electrostatic-based global placement algorithms are widely used due to their effectiveness in providing smooth density penalty functions and comprehensive views of placement zones at granular levels [20], [33], [53], [56], [57]. Following placement, legalization processes such as greedy search [88], Tetris-like approaches [17], and row-based Abacus refinement [85] are critical in addressing overlaps.

VIII. CONCLUSION

We introduced Qplacer, a frequency-aware, electrostatic-based placement framework tailored for robust and scalable superconducting quantum processors. Our approach strategically positions quantum components on substrates, optimizing the usage of limited area while preserving system fidelity, particularly mitigating diverse crosstalk impacts.

Notably, other techniques like compilation and transpilation methods, can be applied orthogonally to Qplacer to further enhance system robustness. While our primary focus was on fixed-frequency architectures, its versatile design renders it suitable for a wide array of quantum architectures, including those with tunable elements which often share similar geometrical configurations with fixed ones. In addition, this work highlights the placement problem within the quantum computing community, a critical but previously overlooked issue as quantum systems scale. placement strategy not only resolves crosstalk (Our focus here) but also has the potential to mitigate other challenges like decoherence by incorporating additional chip components like airbridges, vias.

REFERENCES

- [1] D. W. Abraham, J. M. Chow, A. D. C. Gonzalez, G. A. Keefe, M. E. Rothwell, J. R. Rozen, and M. Steffen, “Removal of spurious microwave modes via flip-chip crossover,” Dec. 22 2015, uS Patent 9,219,298.
- [2] Amazon, “Rigetti superconducting quantum processors,” 2023. [Online]. Available: <https://aws.amazon.com/braket/quantum-computers/rigetti/>
- [3] F. Arute, K. Arya, R. Babbush, D. Bacon, J. Bardin, R. Barends, R. Biswas, S. Boixo, F. Brandao, D. Buell, B. Burkett, Y. Chen, J. Chen, B. Chiaro, R. Collins, W. Courtney, A. Dunsworth, E. Farhi, B. Foxen, A. Fowler, C. M. Gidney, M. Giustina, R. Graff, K. Guerin, S. Habegger, M. Harrigan, M. Hartmann, A. Ho, M. R. Hoffmann, T. Huang, T. Humble, S. Isakov, E. Jeffrey, Z. Jiang, D. Kafri, K. Kechedzhi, J. Kelly, P. Klimov, S. Knysh, A. Korotkov, F. Kostritsa, D. Landhuis, M. Lindmark, E. Lucero, D. Lyakh, S. Mandrà, J. R. McClean, M. McEwen, A. Megrant, X. Mi, K. Michielsen, M. Mohseni, J. Mutus, O. Naaman, M. Neeley, C. Neill, M. Y. Niu, E. Ostby, A. Petukhov, J. Platt, C. Quintana, E. G. Rieffel, P. Roushan, N. Rubin, D. Sank, K. J. Satzinger, V. Smelyanskiy, K. J. Sung, M. Trevithick, A. Vainsencher, B. Villalonga, T. White, Z. J. Yao, P. Yeh, A. Zalcman, H. Neven, and J. Martinis, “Quantum supremacy using a programmable superconducting processor,” *Nature*, vol. 574, 2019. [Online]. Available: <https://www.nature.com/articles/s41586-019-1666-5>
- [4] R. Barends, J. Kelly, A. Megrant, D. Sank, E. Jeffrey, Y. Chen, Y. Yin, B. Chiaro, J. Mutus, C. Neill, P. O’Malley, P. Roushan, J. Wenner, T. C. White, A. N. Cleland, and J. M. Martinis, “Coherent josephson qubit suitable for scalable quantum integrated circuits,” *Phys. Rev. Lett.*, vol. 111, p. 080502, Aug 2013. [Online]. Available: <https://link.aps.org/doi/10.1103/PhysRevLett.111.080502>
- [5] R. Barends, J. Kelly, A. Megrant, A. Veitia, D. Sank, E. Jeffrey, T. White, J. Mutus, A. Fowler, B. Campbell, Y. Chen, Z. Chen, B. Chiaro, A. Dunsworth, C. Neill, P. O’Malley, P. Roushan, A. Vainsencher, J. Wenner, and J. Martinis, “Superconducting quantum circuits at the surface code threshold for fault tolerance,” *Nature*, vol. 508, pp. 500–3, 04 2014.
- [6] R. Barends, C. M. Quintana, A. G. Petukhov, Y. Chen, D. Kafri, K. Kechedzhi, R. Collins, O. Naaman, S. Boixo, F. Arute, K. Arya, D. Buell, B. Burkett, Z. Chen, B. Chiaro, A. Dunsworth, B. Foxen, A. Fowler, C. Gidney, M. Giustina, R. Graff, T. Huang, E. Jeffrey, J. Kelly, P. V. Klimov, F. Kostritsa, D. Landhuis, E. Lucero, M. McEwen, A. Megrant, X. Mi, J. Mutus, M. Neeley, C. Neill, E. Ostby, P. Roushan, D. Sank, K. J. Satzinger, A. Vainsencher, T. White, J. Yao, P. Yeh, A. Zalcman, H. Neven, V. N. Smelyanskiy, and J. M. Martinis, “Diabatic gates for frequency-tunable superconducting qubits,” *Phys. Rev. Lett.*, vol. 123, p. 210501, Nov 2019. [Online]. Available: <https://link.aps.org/doi/10.1103/PhysRevLett.123.210501>
- [7] R. Barends, A. Shabani, L. Lamata, J. Kelly, A. Mezzacapo, U. L. Heras, R. Babbush, A. Fowler, B. Campbell, Y. Chen, Z. Chen, B. Chiaro, A. Dunsworth, E. Jeffrey, E. Lucero, A. Megrant, J. Mutus, M. Neeley, C. Neill, P. O’Malley, C. Quintana, E. Solano, T. White, J. Wenner, A. Vainsencher, D. Sank, P. Roushan, H. Neven, and J. Martinis, “Digitized adiabatic quantum computing with a superconducting circuit,” *Nature*, vol. 534, pp. 222–226, 2016. [Online]. Available: <http://www.nature.com/nature/journal/v534/n7606/full/nature17658.html>
- [8] C. Berke, E. Varvelis, S. Trebst, A. Altland, and D. P. DiVincenzo, “Transmon platform for quantum computing challenged by chaotic fluctuations,” *Nature communications*, vol. 13, no. 1, p. 2495, 2022.
- [9] E. Bernstein and U. Vazirani, “Quantum complexity theory,” in *Proceedings of the twenty-fifth annual ACM symposium on Theory of computing*, 1993, pp. 11–20.
- [10] M. E. Beverland, P. Murali, M. Troyer, K. M. Svore, T. Hoeffler, V. Kliuchnikov, G. H. Low, M. Soeken, A. Sundaram, and A. Vaschillo, “Assessing requirements to scale to practical quantum advantage,” *arXiv preprint arXiv:2211.07629*, 2022.
- [11] R. Bialczak, M. Ansmann, M. Hofheinz, E. Lucero, M. Neeley, D. Sank, W. Hwang, J. Wenner, M. Steffen, A. Cleland, and J. Martinis, “Quantum process tomography of a universal entangling gate implemented with josephson phase qubits,” *Nature Physics*, vol. 6, pp. 409–413, 04 2010.
- [12] J. Biamonte, P. Wittek, N. Pancotti, P. Rebentrost, N. Wiebe, and S. Lloyd, “Quantum machine learning,” *Nature*, vol. 549, no. 7671, pp. 195–202, 2017.
- [13] A. Blais, A. L. Grimsme, S. M. Girvin, and A. Wallraff, “Circuit quantum electrodynamics,” *Reviews of Modern Physics*, vol. 93, no. 2, p. 025005, 2021.
- [14] M. Brink, J. M. Chow, J. Hertzberg, E. Magesan, and S. Rosenblatt, “Device challenges for near term superconducting quantum processors: frequency collisions,” in *2018 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2018, pp. 6–1.
- [15] N. T. Bronn, V. P. Adiga, S. B. Olivadese, X. Wu, J. M. Chow, and D. P. Pappas, “High coherence plane breaking packaging for superconducting qubits,” *Quantum science and technology*, vol. 3, no. 2, p. 024007, 2018.
- [16] Y. Cao, J. Romero, J. P. Olson, M. Degroote, P. D. Johnson, M. Kieferová, I. D. Kivlichan, T. Menke, B. Peropadre, N. P. D. Sawaya, S. Sim, L. Veis, and A. Aspuru-Guzik, “Quantum chemistry in the age of quantum computing,” *Chemical Reviews*, vol. 119, no. 19, pp. 10856–10915, 2019, pMID: 31469277. [Online]. Available: <https://doi.org/10.1021/crrev.8b00803>
- [17] T.-C. Chen, Z.-W. Jiang, T.-C. Hsu, H.-C. Chen, and Y.-W. Chang, “Ntuplace3: An analytical placer for large-scale mixed-size designs with preplaced blocks and density constraints,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 7, pp. 1228–1240, 2008.
- [18] Y. Chen, C. Neill, P. Roushan, N. Leung, M. Fang, R. Barends, J. Kelly, B. Campbell, Z. Chen, B. Chiaro, A. Dunsworth, E. Jeffrey, A. Megrant, J. Y. Mutus, P. J. J. O’Malley, C. M. Quintana, D. Sank, A. Vainsencher, J. Wenner, T. C. White, M. R. Geller, A. N. Cleland, and J. M. Martinis, “Qubit architecture with high coherence and fast tunable coupling,” *Phys. Rev. Lett.*, vol. 113, p. 220502, Nov 2014. [Online]. Available: <https://link.aps.org/doi/10.1103/PhysRevLett.113.220502>
- [19] Z. Chen, A. Megrant, J. Kelly, R. Barends, J. Bochmann, Y. Chen, B. Chiaro, A. Dunsworth, E. Jeffrey, J. Mutus, P. O’Malley, C. Neill, P. Roushan, D. Sank, A. Vainsencher, J. Wenner, T. White, A. Cleland, and J. Martinis, “Fabrication and characterization of aluminum airbridges for superconducting microwave circuits,” *Applied Physics Letters*, vol. 104, 10 2013.
- [20] C.-K. Cheng, A. B. Kahng, I. Kang, and L. Wang, “Replace: Advancing solution quality and routability validation in global placement,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 38, no. 9, pp. 1717–1730, 2018.
- [21] J. M. Chow, J. M. Gambetta, A. W. Cross, S. T. Merkel, C. Rigetti, and M. Steffen, “Microwave-activated conditional-phase gate for superconducting qubits,” *New Journal of Physics*, vol. 15, no. 11, p. 115012, 2013.
- [22] A. W. Cross and J. M. Gambetta, “Optimized pulse shapes for a resonator-induced phase gate,” *Physical Review A*, vol. 91, no. 3, p. 032325, 2015.
- [23] A. Dewes, F. R. Ong, V. Schmitt, R. Lauro, N. Boulant, P. Bertet, D. Vion, and D. Esteve, “Characterization of a two-transmon processor with individual single-shot qubit readout,” *Physical review letters*, vol. 108, no. 5, p. 057002, 2012.
- [24] Y. Ding, P. Gokhale, S. F. Lin, R. Rines, T. Propson, and F. T. Chong, “Systematic crosstalk mitigation for superconducting qubits via frequency-aware compilation,” in *2020 53rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*. IEEE, 2020, pp. 201–214.
- [25] E. Farhi, J. Goldstone, and S. Gutmann, “A quantum approximate optimization algorithm,” *arXiv preprint arXiv:1411.4028*, 2014.
- [26] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland, “Surface codes: Towards practical large-scale quantum computation,” *Physical Review A*, vol. 86, no. 3, p. 032324, 2012.
- [27] J. M. Gambetta, J. M. Chow, and M. Steffen, “Building logical qubits in a superconducting quantum computing system,” *npj quantum information*, vol. 3, no. 1, p. 2, 2017.
- [28] J. M. Gambetta, J. M. Chow, and M. Steffen, “Building logical qubits in a superconducting quantum computing system,” *npj quantum information*, vol. 3, no. 1, p. 2, 2017.
- [29] Y. Y. Gao, M. A. Rol, S. Touzard, and C. Wang, “Practical guide for building superconducting quantum devices,” *PRX Quantum*, vol. 2, no. 4, p. 040202, 2021.

- [30] C. C. Gerry and P. L. Knight, *Introductory quantum optics*. Cambridge university press, 2023.
- [31] S. M. Girvin, “Circuit qed: superconducting qubits coupled to microwave photons,” *Quantum machines: measurement and control of engineered quantum systems*, pp. 113–256, 2014.
- [32] L. K. Grover, “A fast quantum mechanical algorithm for database search,” in *Proceedings of the twenty-eighth annual ACM symposium on Theory of computing*, 1996, pp. 212–219.
- [33] J. Gu, Z. Jiang, Y. Lin, and D. Z. Pan, “Dreamplace 3.0: Multi-electrostatics based robust vlsi placement with region constraints,” in *2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, 2020, pp. 1–9.
- [34] S. Huang, B. Lienhard, G. Calusine, A. Vepsäläinen, J. Braumüller, D. K. Kim, A. J. Melville, B. M. Niedzielski, J. L. Yoder, B. Kannan, T. P. Orlando, S. Gustavsson, and W. D. Oliver, “Microwave package design for superconducting quantum processors,” *PRX Quantum*, vol. 2, p. 020306, Apr 2021. [Online]. Available: <https://link.aps.org/doi/10.1103/PRXQuantum.2.020306>
- [35] IBM, “Qiskit,” 2021. [Online]. Available: <https://www.ibm.com/quantum/qiskit>
- [36] IBM, “Qiskit metal,” 2021. [Online]. Available: <https://github.com/qiskit-community/qiskit-metal>
- [37] IBM, “Eagle’s quantum performance progress,” 2022. [Online]. Available: <https://research.ibm.com/blog/eagle-quantum-processor-performance>
- [38] IBM, “Ibm quantum breaks the 100-qubit processor barrier,” 2022. [Online]. Available: <https://research.ibm.com/blog/127-qubit-quantum-processor-eagle>
- [39] IBM, “A new eagle in the poughkeepsie quantum datacenter: Ibm quantum’s most performant system yet,” 2022. [Online]. Available: <https://research.ibm.com/blog/eagle-quantum-error-mitigation>
- [40] IBM, “Expanding the ibm quantum roadmap to anticipate the future of quantum-centric supercomputing,” 2023. [Online]. Available: <https://www.ibm.com/quantum/blog/ibm-quantum-roadmap-2025>
- [41] IBM, “The hardware and software for the era of quantum utility is here,” 2023. [Online]. Available: <https://www.ibm.com/quantum/blog/quantum-roadmap-2033>
- [42] IBM, “Ibm quantum,” 2023. [Online]. Available: <https://quantum-computing.ibm.com/>
- [43] IonQ, “Trapped ion quantum computing,” 2023. [Online]. Available: <https://ionq.com/>
- [44] E. T. Jaynes and F. W. Cummings, “Comparison of quantum and semiclassical radiation theories with application to the beam maser,” *Proceedings of the IEEE*, vol. 51, no. 1, pp. 89–109, 1963.
- [45] A. Kandala, A. Mezzacapo, K. Temme, M. Takita, M. Brink, J. M. Chow, and J. M. Gambetta, “Hardware-efficient variational quantum eigensolver for small molecules and quantum magnets,” *Nature*, vol. 549, no. 7671, pp. 242–246, 2017.
- [46] M. Kjaergaard, M. E. Schwartz, A. Greene, G. O. Samach, A. Bengtsson, M. O’Keeffe, C. M. McNally, J. Braumüller, D. K. Kim, P. Krantz, M. Marvian, A. Melville, B. M. Niedzielski, Y. Sung, R. Winik, J. Yoder, D. Rosenberg, K. Obenland, S. Lloyd, T. P. Orlando, I. Marvian, S. Gustavsson, and W. D. Oliver, “Programming a quantum computer with quantum instructions,” 2020.
- [47] J. Koch, M. Y. Terri, J. Gambetta, A. A. Houck, D. I. Schuster, J. Majer, A. Blais, M. H. Devoret, S. M. Girvin, and R. J. Schoelkopf, “Charge-insensitive qubit design derived from the cooper pair box,” *Physical Review A*, vol. 76, no. 4, p. 042319, 2007.
- [48] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver, “A quantum engineer’s guide to superconducting qubits,” *Applied physics reviews*, vol. 6, no. 2, 2019.
- [49] N. Lambert, Y.-N. Chen, Y.-C. Cheng, C.-M. Li, G.-Y. Chen, and F. Nori, “Quantum biology,” *Nature Physics*, vol. 9, no. 1, pp. 10–18, 2013.
- [50] G. Li, Y. Ding, and Y. Xie, “Towards efficient superconducting quantum processor architecture design,” in *Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems*, 2020, pp. 1031–1045.
- [51] G. Li, Y. Shi, and A. Javadi-Abhari, “Software-hardware co-optimization for computational chemistry on superconducting quantum processors,” in *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA)*. IEEE, 2021, pp. 832–845.
- [52] Z. Liang, H. Wang, J. Cheng, Y. Ding, H. Ren, Z. Gao, Z. Hu, D. S. Boning, X. Qian, S. Han, W. Jiang, and Y. Shi, “Variational quantum pulse learning,” in *2022 IEEE International Conference on Quantum Computing and Engineering (QCE)*, 2022, pp. 556–565.
- [53] Y. Lin, S. Dhar, W. Li, H. Ren, B. Khailany, and D. Z. Pan, “Dreamplace: Deep learning toolkit-enabled gpu acceleration for modern vlsi placement,” in *Proceedings of the 56th Annual Design Automation Conference 2019*, 2019, pp. 1–6.
- [54] Z. Liu, J. Li, Z. Liu, W. Li, J. Li, C. Gu, and Z.-Y. Li, “Fano resonance rabi splitting of surface plasmons,” *Scientific reports*, vol. 7, no. 1, p. 8010, 2017.
- [55] S. Lloyd and C. Weedbrook, “Quantum generative adversarial learning,” *Physical review letters*, vol. 121, no. 4, p. 040502, 2018.
- [56] J. Lu, P. Chen, C.-C. Chang, L. Sha, D. J.-H. Huang, C.-C. Teng, and C.-K. Cheng, “Eplace: Electrostatics-based placement using fast fourier transform and nesterov’s method,” *Association for Computing Machinery*, vol. 20, no. 2, mar 2015. [Online]. Available: <https://doi.org/10.1145/2699873>
- [57] J. Lu, H. Zhuang, P. Chen, H. Chang, C.-C. Chang, Y.-C. Wong, L. Sha, D. Huang, Y. Luo, C.-C. Teng, and C.-K. Cheng, “eplace-ms: Electrostatics-based placement for mixed-size circuits,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 5, pp. 685–698, 2015.
- [58] K. Luo, W. Huang, Z. Tao, L. Zhang, Y. Zhou, J. Chu, W. Liu, B. Wang, J. Cui, S. Liu, F. Yan, M.-H. Yung, Y. Chen, T. Yan, and D. Yu, “Experimental realization of two qutrits gate with tunable coupling in superconducting circuits,” *Phys. Rev. Lett.*, vol. 130, p. 030603, Jan 2023. [Online]. Available: <https://link.aps.org/doi/10.1103/PhysRevLett.130.030603>
- [59] M. Malekakhlagh, W. Shanks, and H. Paik, “Optimization of the resonator-induced phase gate for superconducting qubits,” *Physical Review A*, vol. 105, no. 2, p. 022607, 2022.
- [60] J. M. Martinis, “Surface loss calculations and design of a superconducting transmon qubit with tapered wiring,” *npj Quantum Information*, vol. 8, no. 1, p. 26, 2022.
- [61] J. M. Martinis, K. B. Cooper, R. McDermott, M. Steffen, M. Ansmann, K. Osborn, K. Cicak, S. Oh, D. P. Pappas, R. W. Simmonds, and C. C. Yu, “Decoherence in josephson qubits from dielectric loss,” *Physical review letters*, vol. 95, no. 21, p. 210503, 2005.
- [62] C. R. H. McRae, H. Wang, J. Gao, M. R. Vissers, T. Brecht, A. Dunsworth, D. P. Pappas, and J. Mutus, “Materials loss measurements using superconducting microwave resonators,” *Review of Scientific Instruments*, vol. 91, no. 9, 2020.
- [63] Z. K. Minev, T. G. McConkey, M. Takita, A. D. Corcoles, and J. M. Gambetta, “Circuit quantum electrodynamics (cqed) with modular quasi-lumped models,” *arXiv preprint arXiv:2103.10344*, 2021.
- [64] P. Mundada, G. Zhang, T. Hazard, and A. Houck, “Suppression of qubit crosstalk in a tunable coupling superconducting circuit,” *Physical Review Applied*, vol. 12, no. 5, p. 054023, 2019.
- [65] P. Murali, D. C. McKay, M. Martonosi, and A. Javadi-Abhari, “Software mitigation of crosstalk on noisy intermediate-scale quantum computers,” in *Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems*, 2020, pp. 1001–1016.
- [66] E. National Academies of Sciences and Medicine, “Quantum computing: progress and prospects,” *National Academies Press*, 2019.
- [67] C. J. Neill, *A path towards quantum supremacy with superconducting qubits*. University of California, Santa Barbara, 2017.
- [68] O. Noroozian, P. K. Day, B. H. Eom, H. G. Leduc, and J. Zmuidzinas, “Crosstalk reduction for superconducting microwave resonator arrays,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 5, pp. 1235–1243, 2012.
- [69] H. Paik, A. Mezzacapo, M. Sandberg, D. T. McClure, B. Abdo, A. D. Corcoles, O. Dial, D. F. Bogorin, B. L. T. Plourde, M. Steffen, A. W. Cross, J. M. Gambetta, and J. M. Chow, “Experimental demonstration of a resonator-induced phase gate in a multiqubit circuit-qed system,” *Phys. Rev. Lett.*, vol. 117, p. 250502, Dec 2016. [Online]. Available: <https://link.aps.org/doi/10.1103/PhysRevLett.117.250502>
- [70] L. PatrickM, “Low frequency resonators on superconducting chips,” 2015. [Online]. Available: https://qudev.phys.ethz.ch/static/content/science/Documents/semester/Brad_Mitchell_Patrick_Lenggenhager_SemesterThesis_2015Dec03_LFResonators.pdf
- [71] J. Preskill, “Quantum computing in the nisq era and beyond,” *Quantum*, vol. 2, p. 79, 2018.

- [72] S. Puri and A. Blais, "High-fidelity resonator-induced phase gate with single-mode squeezing," *Physical review letters*, vol. 116, no. 18, p. 180501, 2016.
- [73] quantware, "quantware," 2023. [Online]. Available: <https://www.quantware.eu/>
- [74] D. Rosenberg, S. J. Weber, D. Conway, D.-R. W. Yost, J. Mallek, G. Calusine, R. Das, D. Kim, M. E. Schwartz, W. Woods, J. L. Yoder, and W. D. Oliver, "Solid-state qubits: 3d integration and packaging," *IEEE Microwave Magazine*, vol. 21, no. 8, pp. 72–85, 2020.
- [75] T. E. Roth, R. Ma, and W. C. Chew, "An introduction to the transmon qubit for electromagnetic engineers," *arXiv preprint arXiv:2106.11352*, 2021.
- [76] A. C. Santos, "Role of parasitic interactions and microwave crosstalk in dispersive control of two superconducting artificial atoms," *Physical Review A*, vol. 107, no. 1, p. 012602, 2023.
- [77] M. Sarovar, T. Proctor, K. Rudinger, K. Young, E. Nielsen, and R. Blume-Kohout, "Detecting crosstalk errors in quantum information processors," *Quantum*, vol. 4, p. 321, 2020.
- [78] R. Schoelkopf and S. Girvin, "Wiring up quantum systems," *Nature*, vol. 451, no. 7179, pp. 664–669, 2008.
- [79] J. A. Schreier, A. A. Houck, J. Koch, D. I. Schuster, B. R. Johnson, J. M. Chow, J. M. Gambetta, J. Majer, L. Frunzio, M. H. Devoret, S. M. Girvin, and R. J. Schoelkopf, "Suppressing charge noise decoherence in superconducting charge qubits," *Phys. Rev. B*, vol. 77, p. 180502, May 2008. [Online]. Available: <https://link.aps.org/doi/10.1103/PhysRevB.77.180502>
- [80] S. Sheldon, E. Magesan, J. M. Chow, and J. M. Gambetta, "Procedure for systematically tuning up cross-talk in the cross-resonance gate," *Physical Review A*, vol. 93, no. 6, p. 060302, 2016.
- [81] S. Sheldon, M. Sandberg, H. Paik, B. Abdo, J. M. Chow, M. Steffen, and J. M. Gambetta, "Characterization of hidden modes in networks of superconducting qubits," *Applied Physics Letters*, vol. 111, no. 22, 2017.
- [82] P. W. Shor, "Polynomial-time algorithms for prime factorization and discrete logarithms on a quantum computer," *SIAM review*, vol. 41, no. 2, pp. 303–332, 1999.
- [83] B. W. Shore and P. L. Knight, "The jaynes-cummings model," *Journal of Modern Optics*, vol. 40, no. 7, pp. 1195–1238, 1993.
- [84] K. N. Smith, G. S. Ravi, J. M. Baker, and F. T. Chong, "Scaling superconducting quantum computers with chiplet architectures," in *2022 55th IEEE/ACM International Symposium on Microarchitecture (MICRO)*. IEEE, 2022, pp. 1092–1109.
- [85] P. Spindler, U. Schllichtmann, and F. M. Johannes, "Abacus: Fast legalization of standard cell circuits with minimal movement," in *Proceedings of the 2008 international symposium on Physical design*, 2008, pp. 47–53.
- [86] P. Spring, T. Tsunoda, B. Vlastakis, and P. Leek, "Modeling enclosures for large-scale superconducting quantum circuits," *Physical Review Applied*, vol. 14, no. 2, p. 024061, 2020.
- [87] M. Takita, A. D. Córcoles, E. Magesan, B. Abdo, M. Brink, A. Cross, J. M. Chow, and J. M. Gambetta, "Demonstration of weight-four parity measurements in the surface code architecture," *Physical review letters*, vol. 117, no. 21, p. 210505, 2016.
- [88] X. Tang, R. Tian, and M. D. Wong, "Optimal redistribution of white space for wire length minimization," in *Proceedings of the 2005 Asia and South Pacific Design Automation Conference*, 2005, pp. 412–417.
- [89] M. Vahidpour, W. O'Brien, J. T. Whyland, J. Angeles, J. Marshall, D. Scarabelli, G. Crossman, K. Yadav, Y. Mohan, C. Bui, V. Rawat, R. Renzas, N. Vodrahalli, A. Bestwick, and C. Rigetti, "Superconducting through-silicon vias for quantum integrated circuits," 2017.
- [90] C. Wang, X. Li, H. Xu, Z. Li, J. Wang, Z. Yang, Z. Mi, X. Liang, T. Su, Y. Chuhong, G. Wang, W. Wang, Y. Li, M. Chen, C. Li, K. Linghu, J. Han, Y. Zhang, Y. Feng, and H. Yu, "Towards practical quantum computers: transmon qubit with a lifetime approaching 0.5 milliseconds," *npj Quantum Information*, vol. 8, 12 2022.
- [91] H. Wang, Y. Ding, J. Gu, Y. Lin, D. Z. Pan, F. T. Chong, and S. Han, "Quantumnas: Noise-adaptive search for robust quantum circuits," in *2022 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*. IEEE, 2022, pp. 692–708.
- [92] J. Wenner, M. Neely, R. Bialczak, M. Lenander, E. Lucero, A. O'Connell, D. Sank, H. Wang, M. Weides, A. Cleland, and J. Martinis, "Wirebond crosstalk and cavity modes in large chip mounts for superconducting qubits," *Superconductor Science and Technology*, vol. 24, p. 065001, 03 2011.
- [93] J. Wenner, R. Barends, R. Bialczak, Y. Chen, J. Kelly, E. Lucero, M. Mariantoni, A. Megrant, P. O'Malley, D. Sank et al., "Surface loss simulations of superconducting coplanar waveguide resonators," *Applied Physics Letters*, vol. 99, no. 11, 2011.
- [94] W. Woods, G. Calusine, A. Melville, A. Sevi, E. Golden, D. K. Kim, D. Rosenberg, J. L. Yoder, and W. D. Oliver, "Determining interface dielectric losses in superconducting coplanar-waveguide resonators," *Physical Review Applied*, vol. 12, no. 1, p. 014012, 2019.
- [95] Y. Xu, J. Chu, J. Yuan, J. Qiu, Y. Zhou, L. Zhang, X. Tan, Y. Yu, S. Liu, J. Li, F. Yan, and D. Yu, "High-fidelity, high-scalability two-qubit gate scheme for superconducting qubits," *Phys. Rev. Lett.*, vol. 125, p. 240503, Dec 2020. [Online]. Available: <https://link.aps.org/doi/10.1103/PhysRevLett.125.240503>
- [96] D. Yost, M. Schwartz, J. Mallek, D. Rosenberg, C. Stull, J. Yoder, G. Calusine, M. Cook, R. Das, A. Day, E. Golden, D. Kim, A. Melville, B. Niedzielski, W. Woods, A. Kerman, and W. Oliver, "Solid-state qubits integrated with superconducting through-silicon vias," *npj Quantum Information*, vol. 6, 12 2020.
- [97] H. Zhang, S. Chakram, T. Roy, N. Earnest, Y. Lu, Z. Huang, D. Weiss, J. Koch, and D. I. Schuster, "Universal fast-flux control of a coherent, low-frequency qubit," *Physical Review X*, vol. 11, no. 1, p. 011010, 2021.
- [98] J. Zhang, P. Bogdan, and S. Nazarian, "C-sar: Sat attack resistant logic locking for rsfq circuits," *arXiv preprint arXiv:2301.10216*, 2023.
- [99] J. Zhang, P. Bogdan, and S. Nazarian, "A majority logic synthesis framework for single flux quantum circuits," *arXiv preprint arXiv:2301.10695*, 2023.
- [100] J. Zhang, H. Wang, G. S. Ravi, F. T. Chong, S. Han, F. Mueller, and Y. Chen, "Disq: Dynamic iteration skipping for variational quantum algorithms," in *2023 IEEE International Conference on Quantum Computing and Engineering (QCE)*, vol. 1. IEEE, 2023, pp. 1062–1073.