Smartphones - From vacuum tubes to integrated circuits

Nik Dennler

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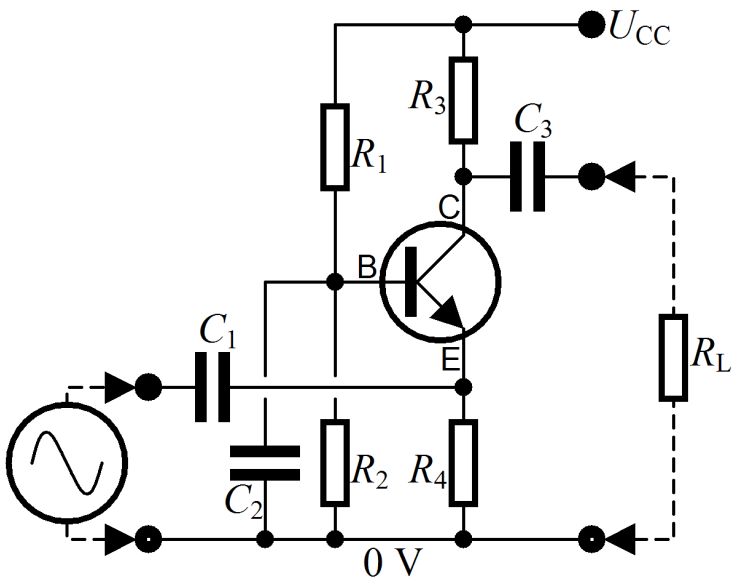

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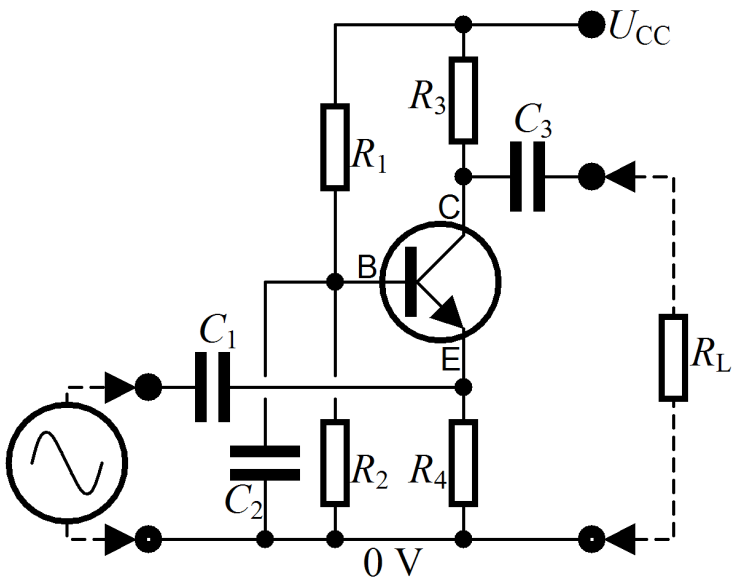

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Binary Representation

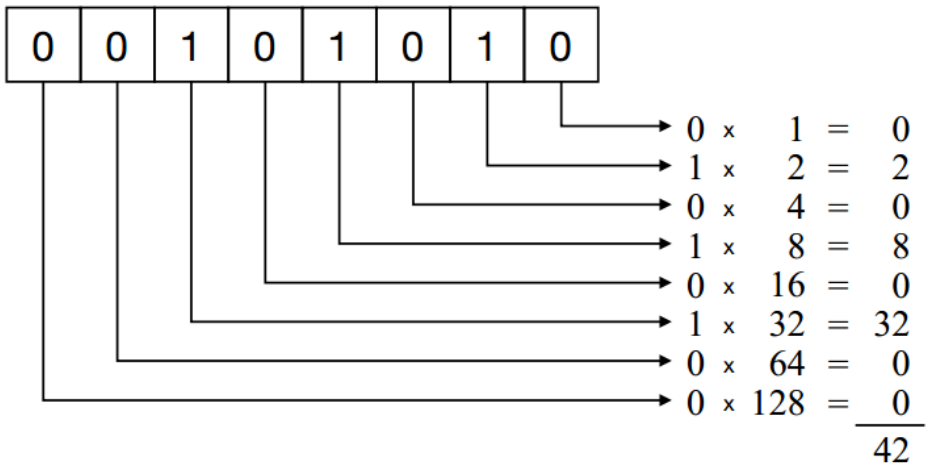

Figure : http://binarynumbersa.blogspot.ch/2012/02/representation-of-binary-numbers.html

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Bool Algebra and logical circuits

- Conjunction: $a \wedge b$ is $True$, if a is $True$ and b is $True$.
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a	b	$a \wedge b$	$a \vee b$	$\neg a$
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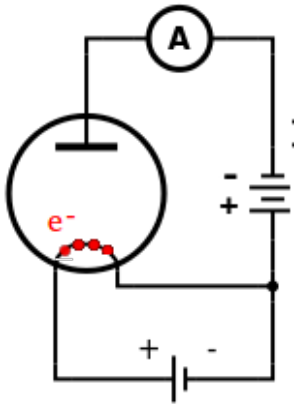

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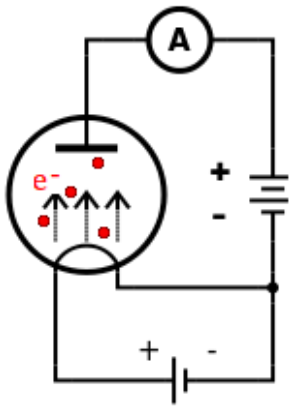

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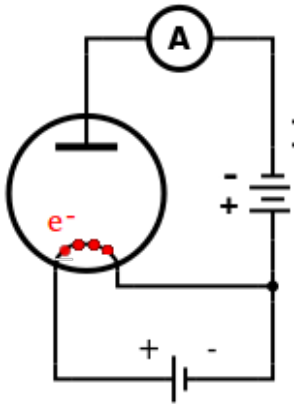

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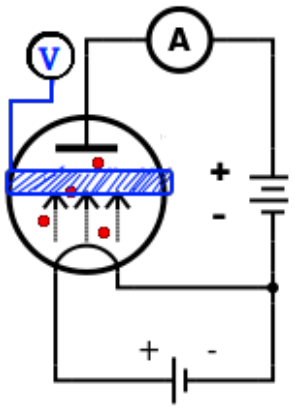

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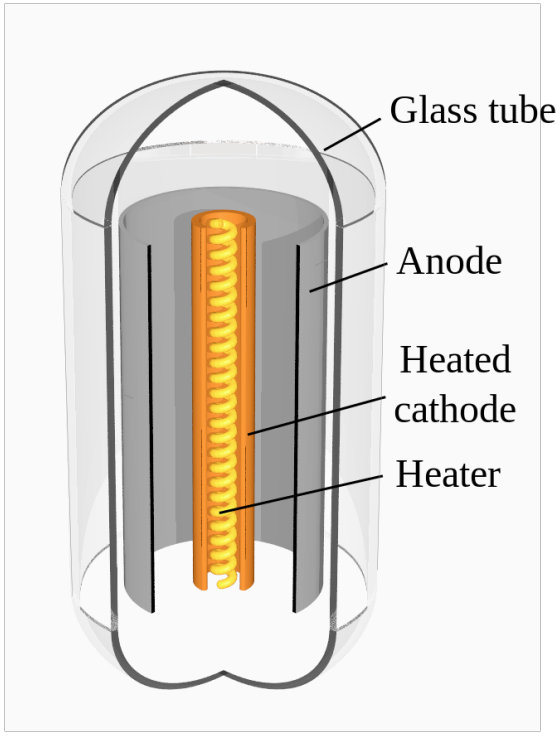

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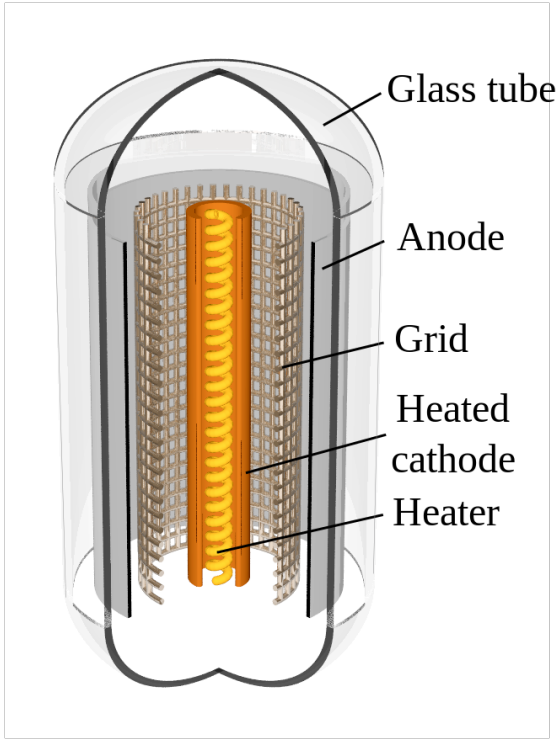

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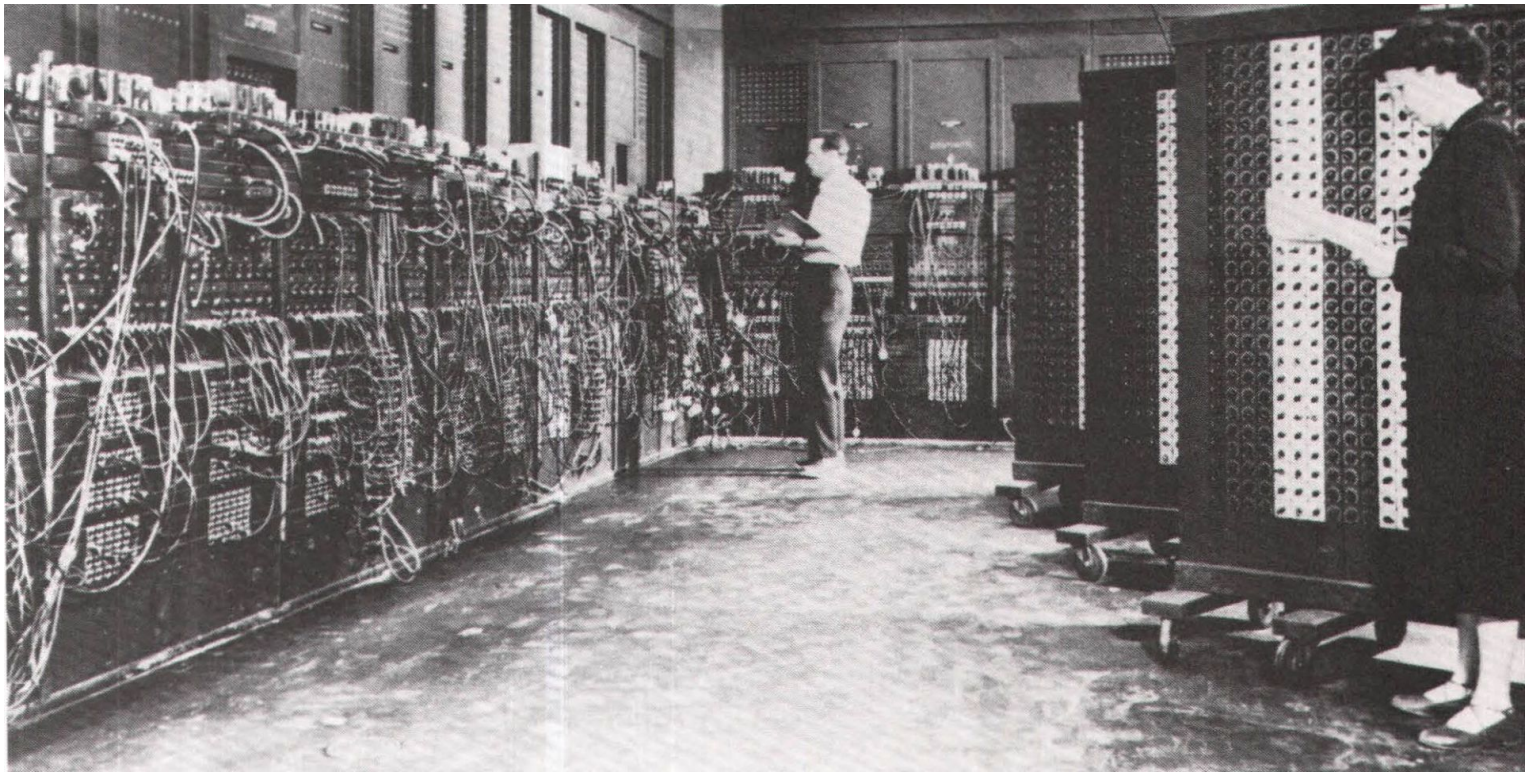

Figure : http://www.cs.kent.edu

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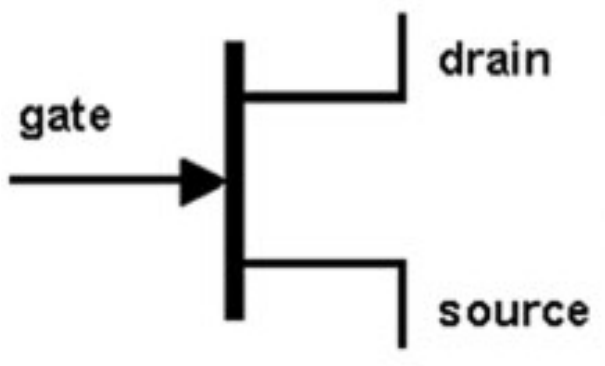

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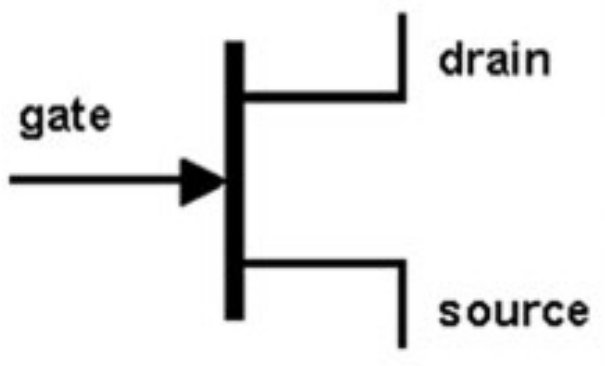

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- Logic gates printed on silicon wafer to form an integrated circuit

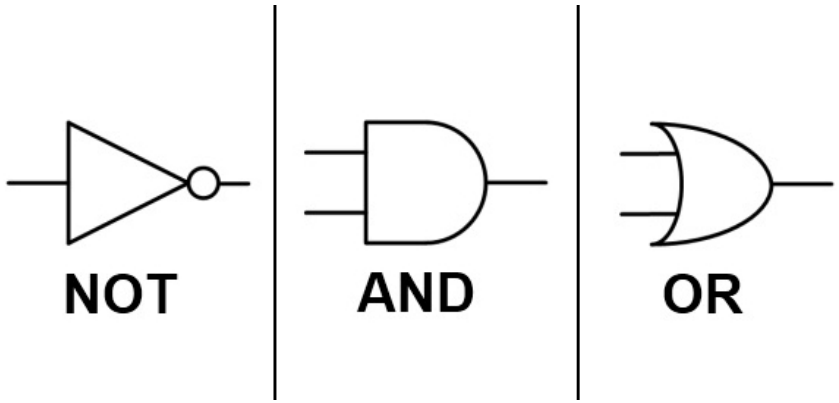

Figure: http://www.mibb-design.com

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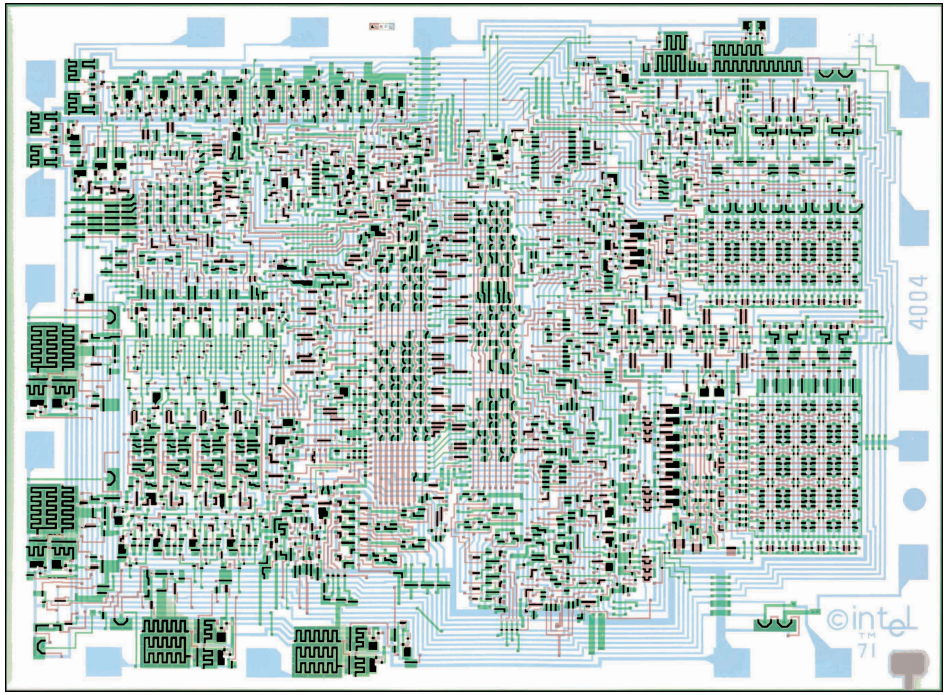

Figure: http://www.4004.com

Semiconductors

- Electric conductivity between conductor and insulator
- Electrons follow Fermi-dirac distribution:

$$f(E) = \frac{1}{1 + e^{\frac{E - \epsilon_F}{k \cdot T}}}$$

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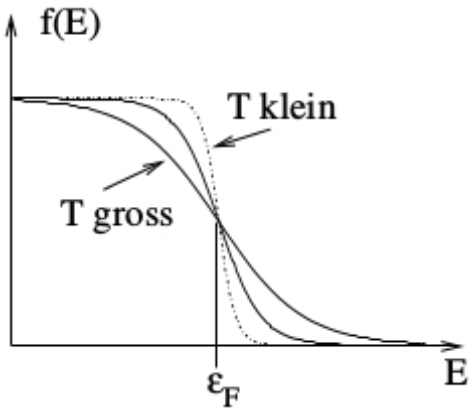

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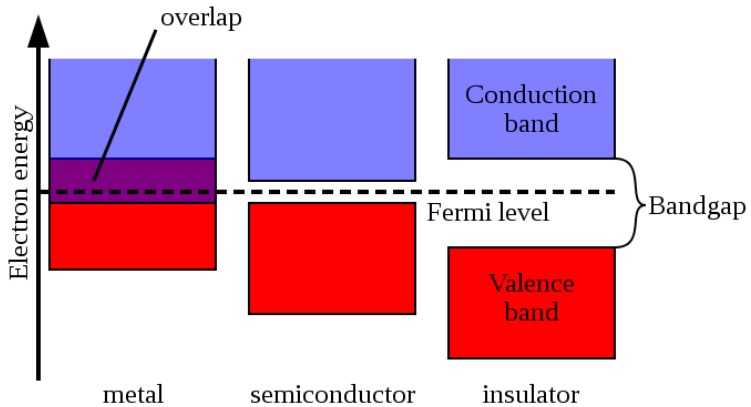

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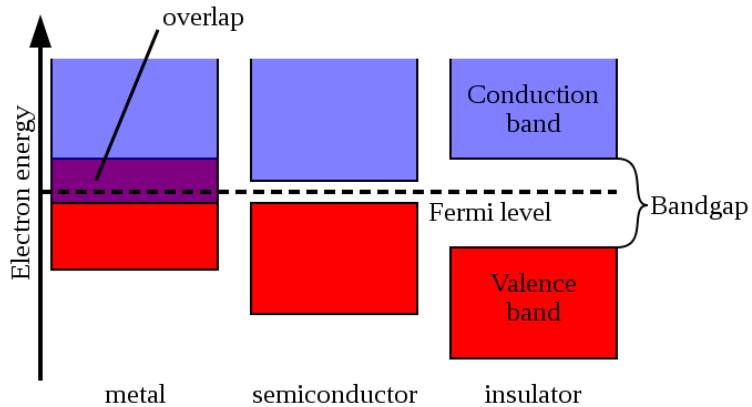

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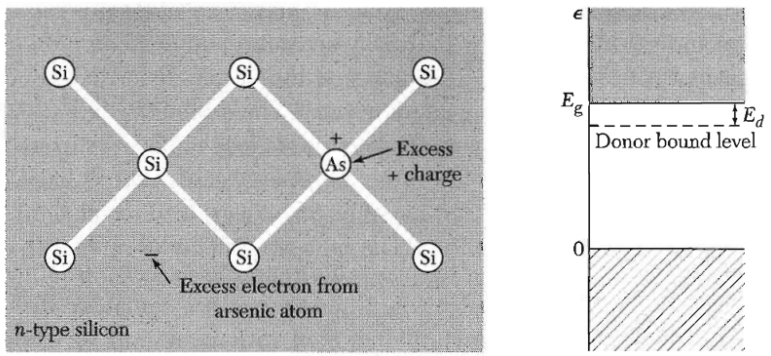

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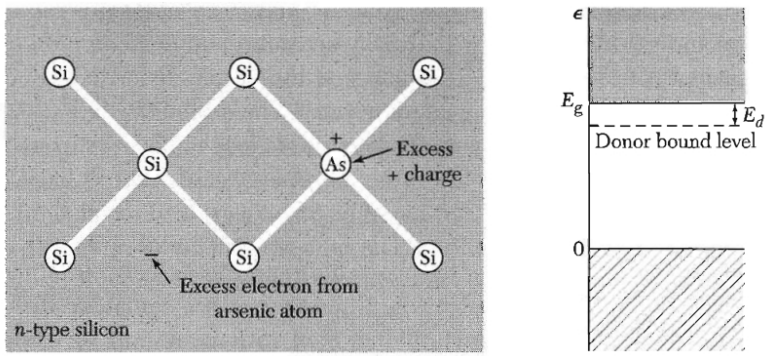

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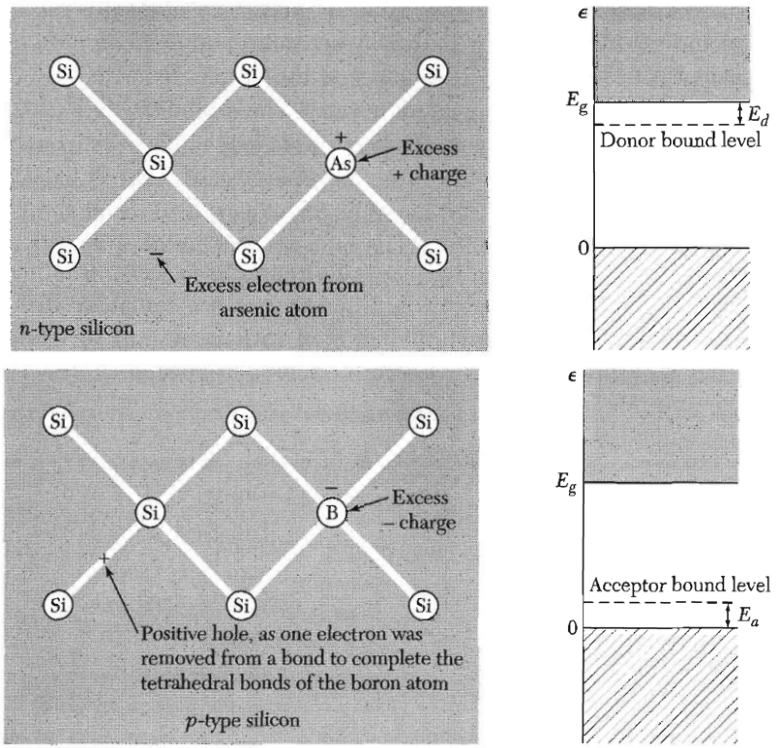

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p-n junction

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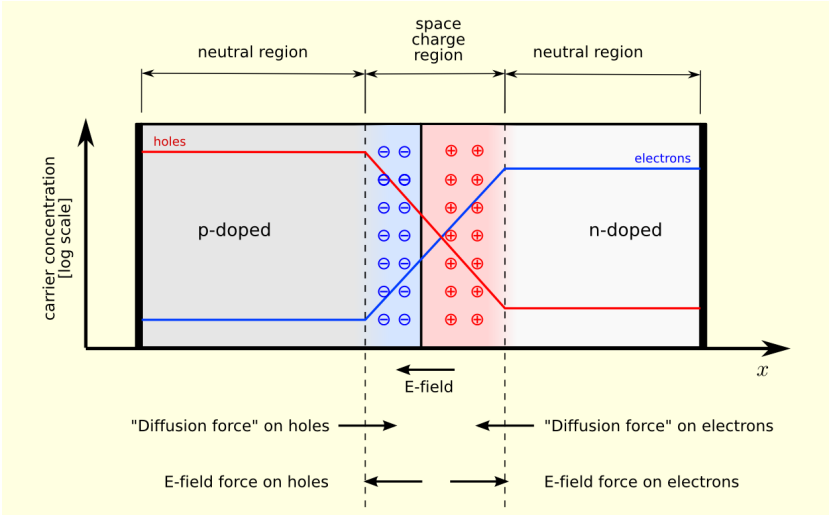

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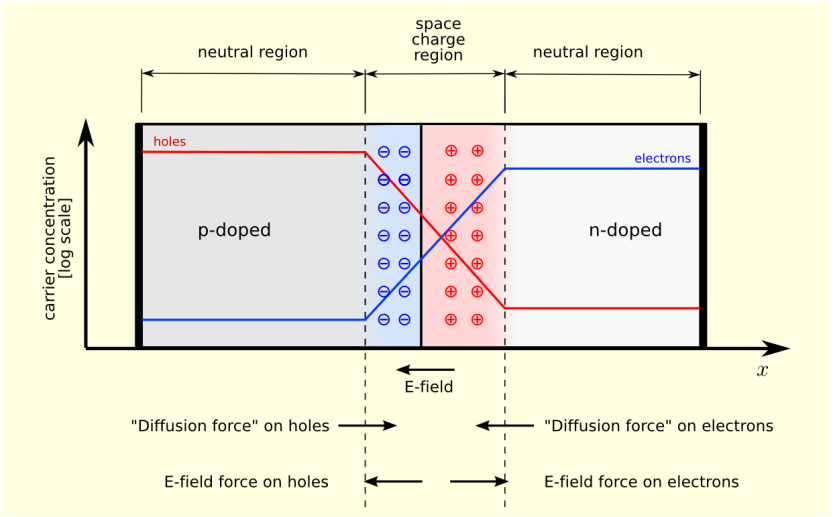

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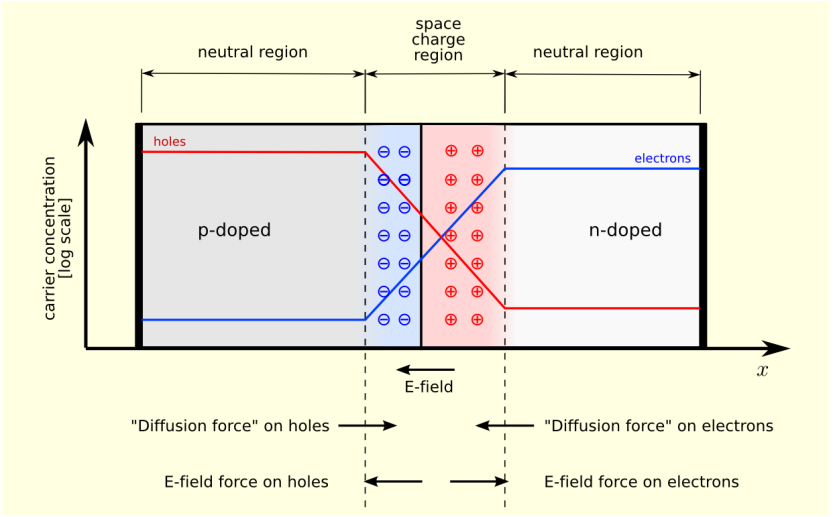

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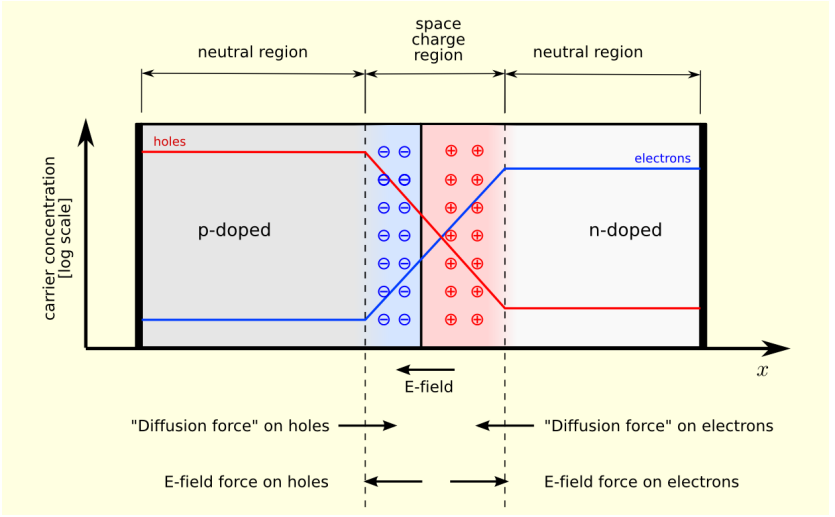

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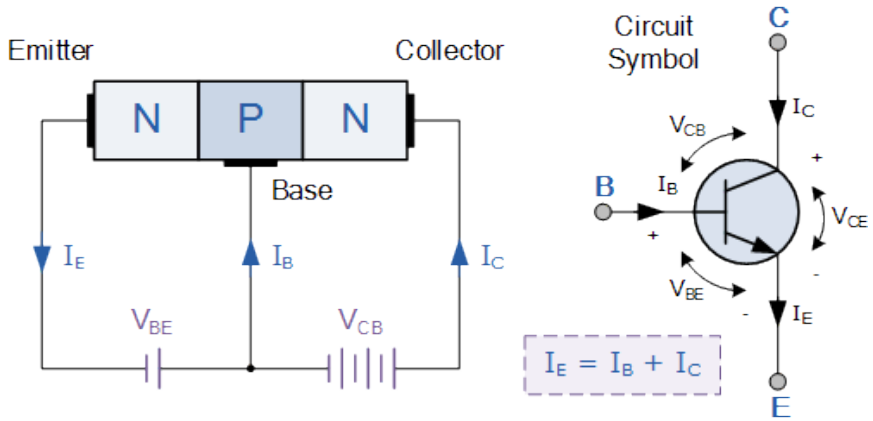
- Emitter, Base, Collector



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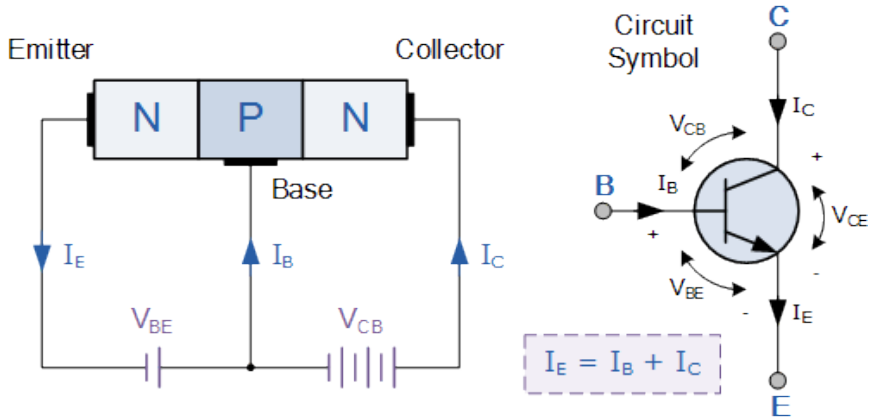

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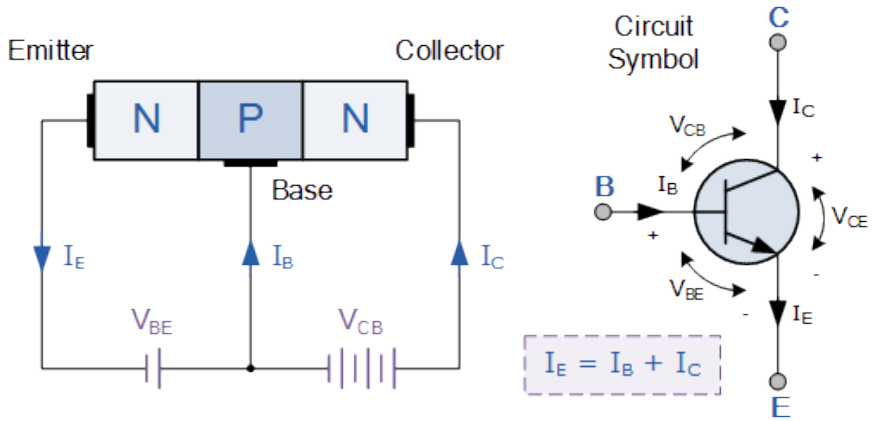

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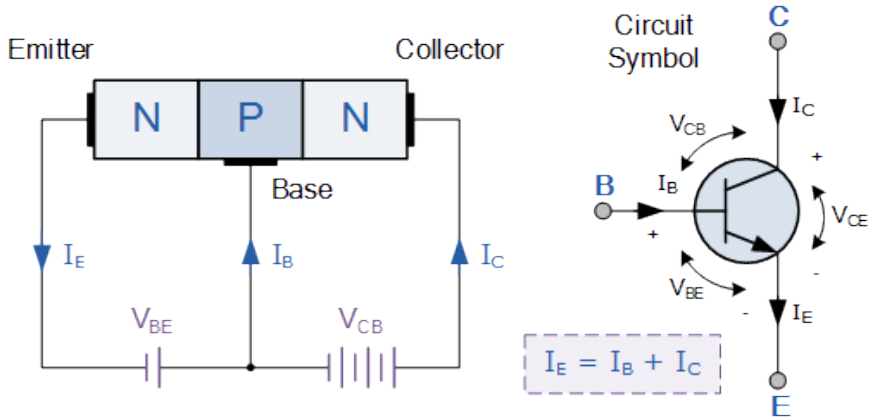

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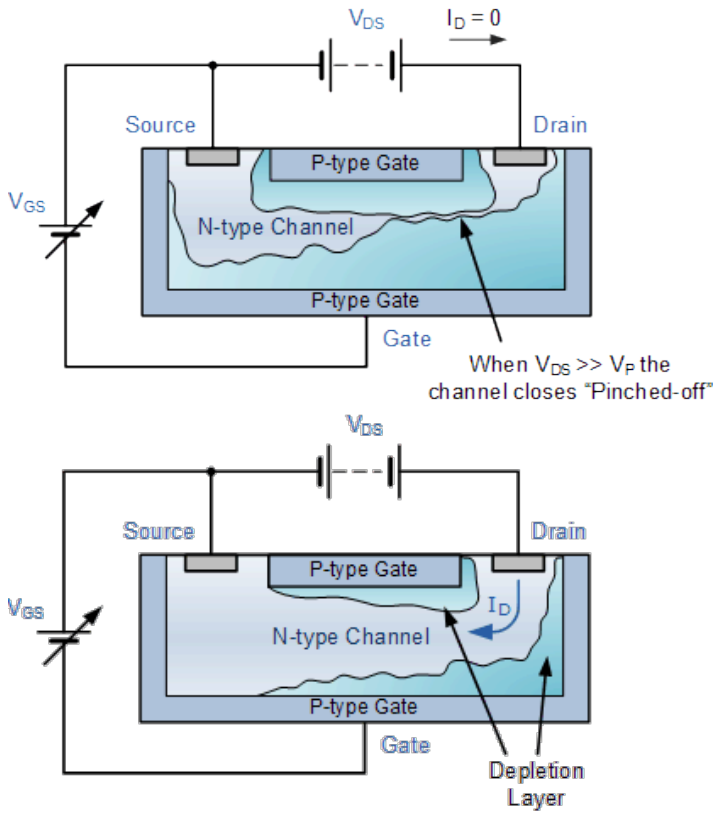

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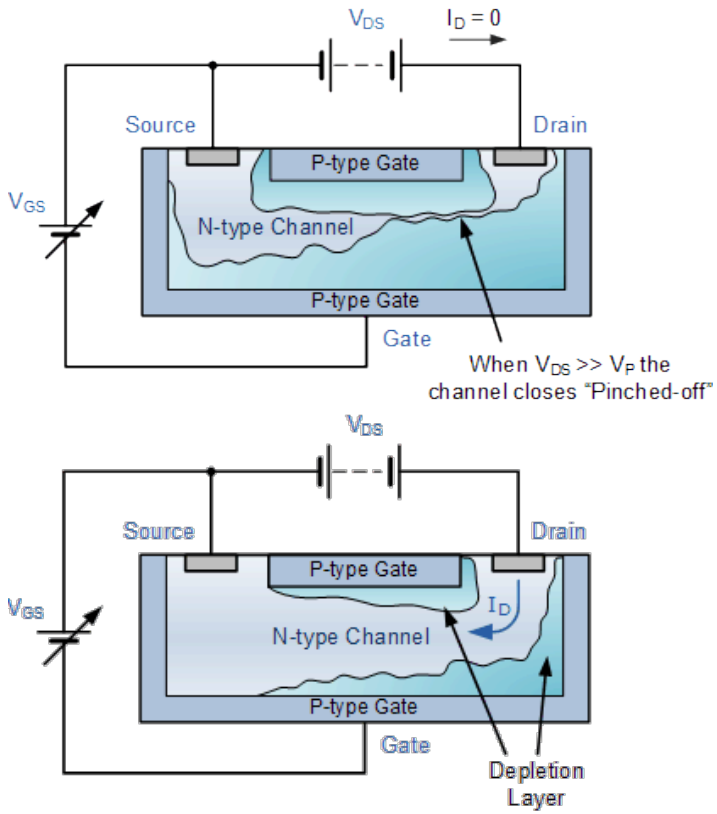

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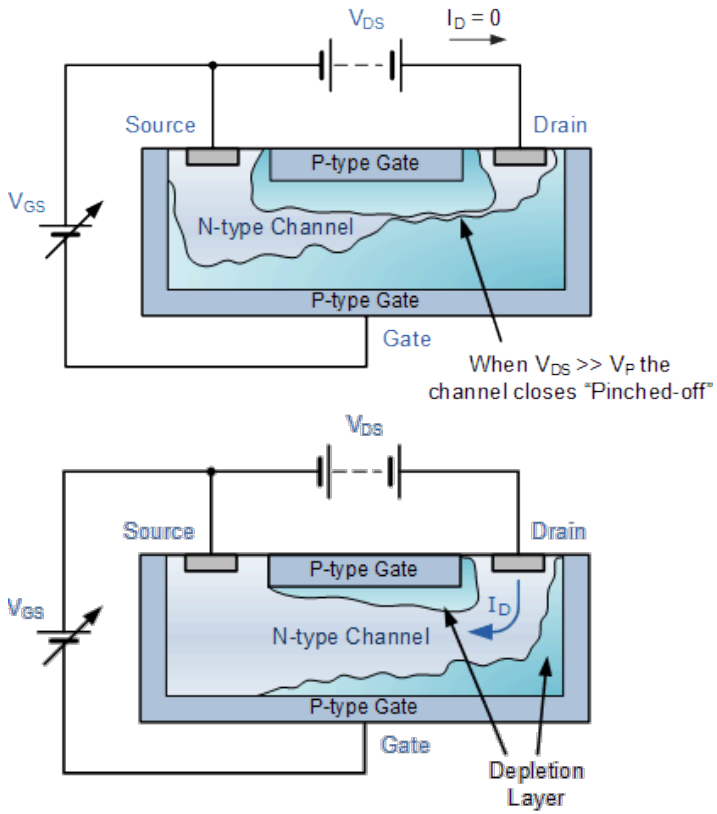

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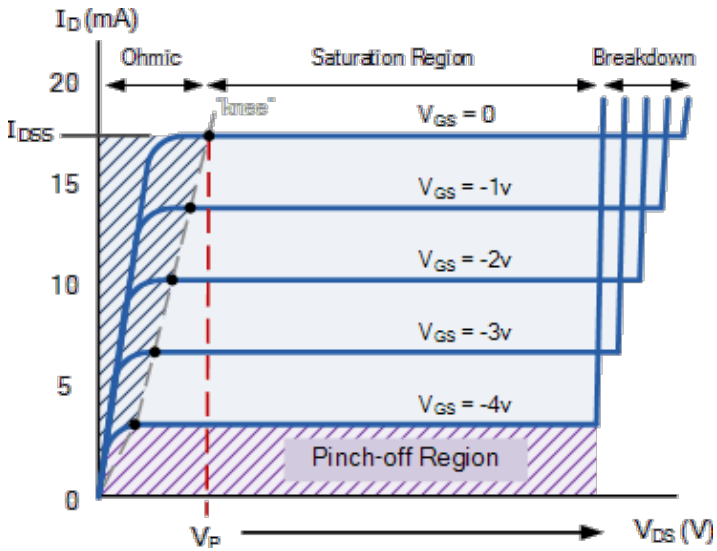

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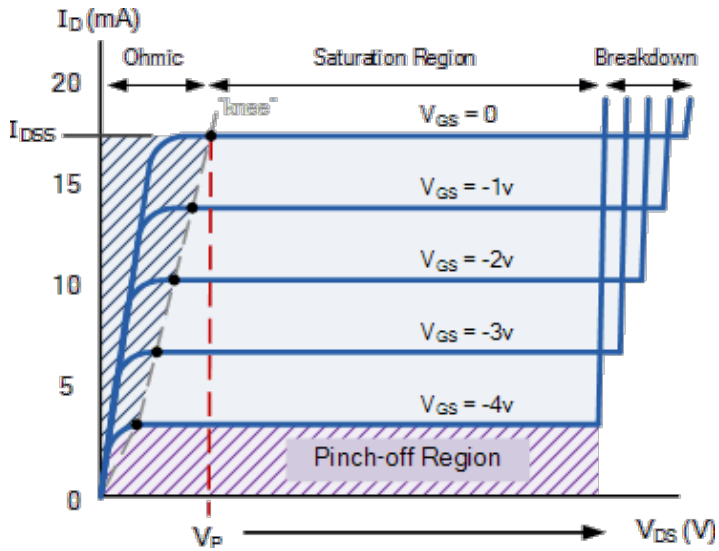

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- *Breakdown Region*: V_{DS} very large $\rightarrow$ maximum current

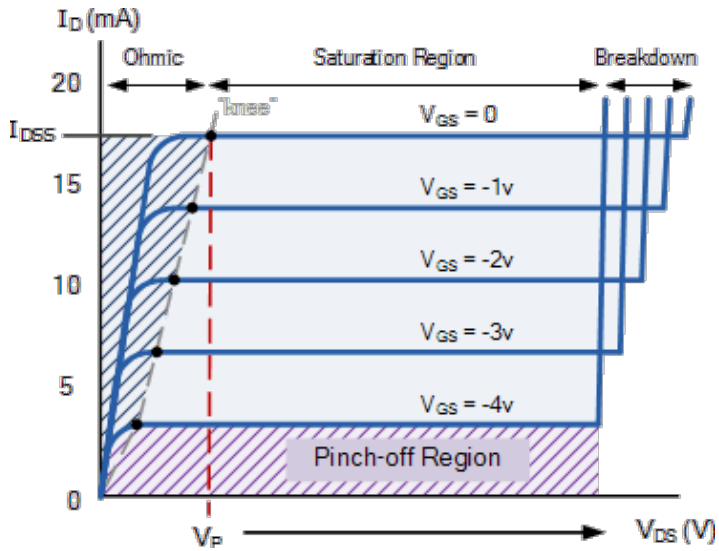

Figure : `http://www.electronics-tutorials.ws`

Field Effect Transistor (FET)

- *Cut-Off Region*: $V_{GS} = 0 \rightarrow$ no DS-current (Off-Region)
- *Ohmic Region*: $V_{GS} > 0$ and V_{DS} small $\rightarrow$ current controlled by V_{DS}
- *Saturation Region*: $V_{GS} > 0$ and V_{DS} large $\rightarrow$ DS-current controlled by drain voltage (On-Region)
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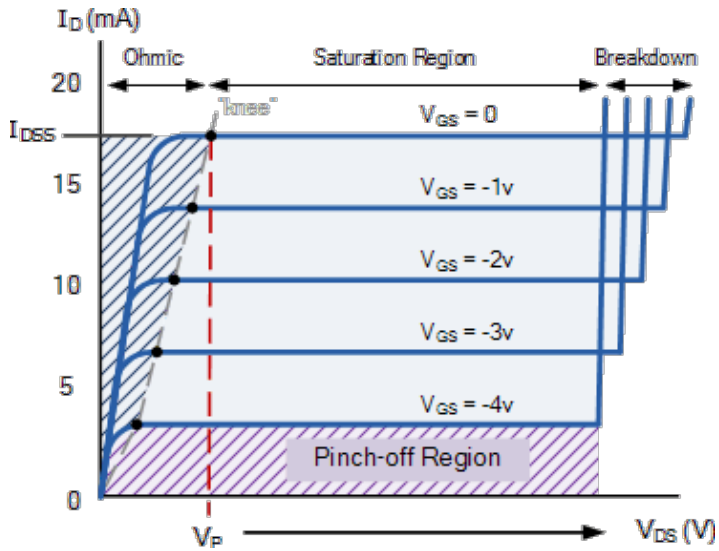

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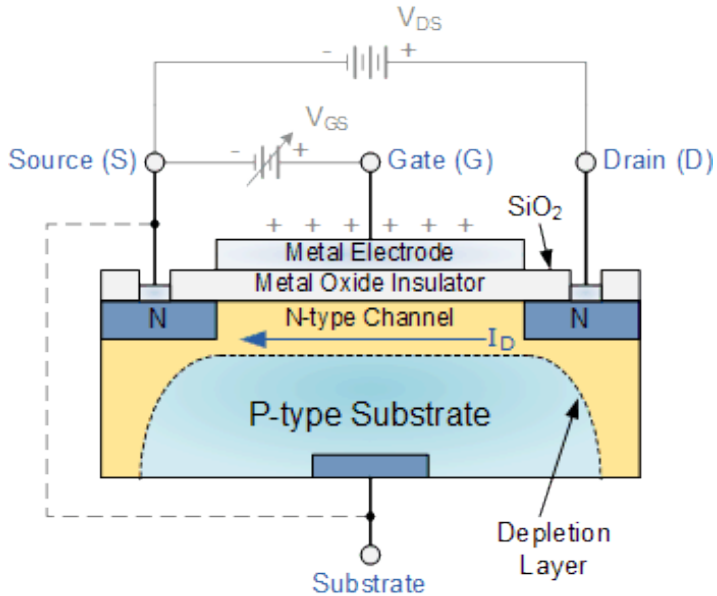
MOSFET

- JFET architecture, but small SiO_2 layer between gate and channel
- Insulating layer raises the input resistance of the MOSFET and prevents any channel-gate-current



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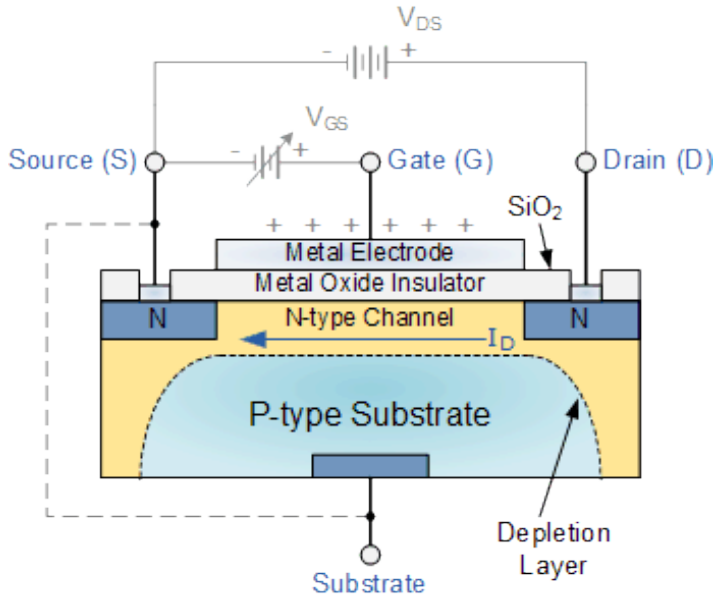

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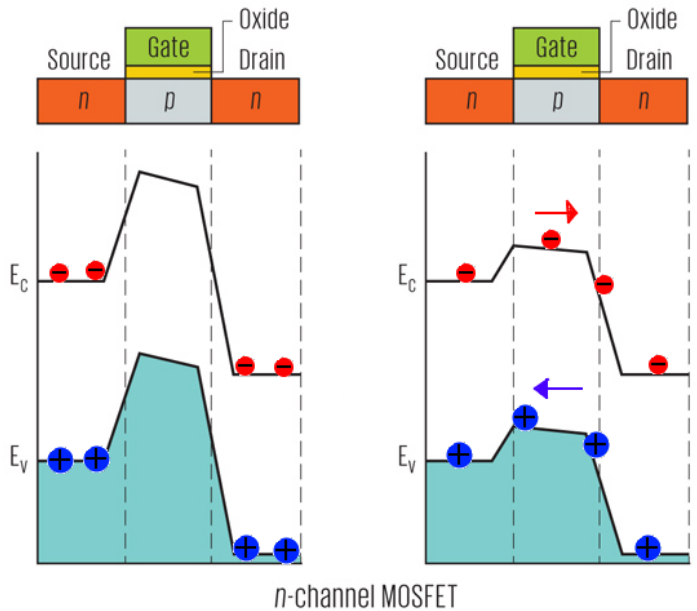
MOSFET

- Electrons in conducting band, holes in valence band
- In Off-state can charge carriers not pass big potential wall
- In On-state the potential wall is lowered and charges can pass



n-channel MOSFET

Differences, advantages and disadvantages of BJTs and MOSFETs

BJT	MOSFET
emitter, collector, base	gate, source, channel, drain
electron and hole state conduction	either electron or hole state conduction
controlled by current	controlled by voltage
less complex	
	vulnerable to electrostatic damage during installation

Differences, advantages and disadvantages of BJTs and MOSFETs

BJT	MOSFET
	much less leak current
	no additional power draw after the gate is opened or closed
	more resistent againt radiation

→ Nowadays, if in digital and analog circuits, MOSFETs are more commonly used than BJTs.

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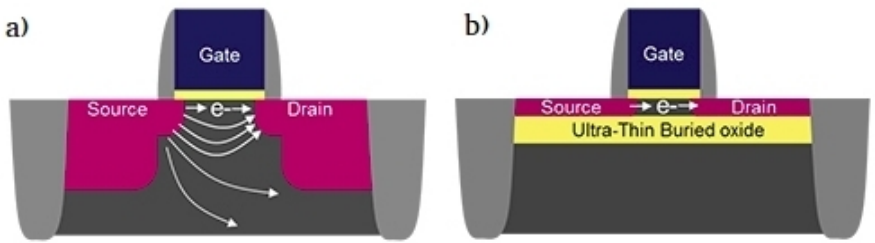
Ultrathin Body Silicon on Insulator (UTB-SOI)

- Thin layer of buried oxide on top of base silicon
- Very thin channel



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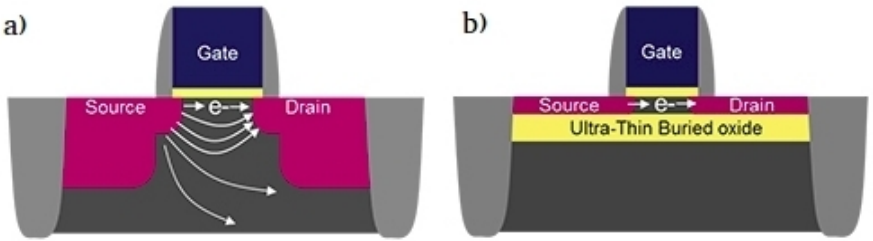

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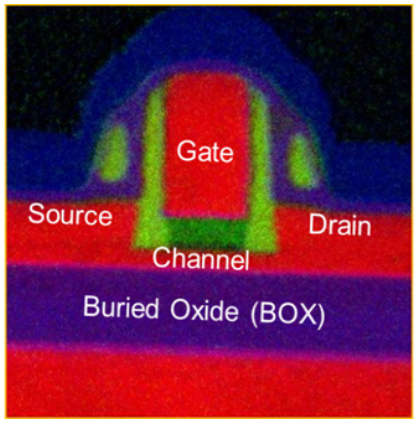

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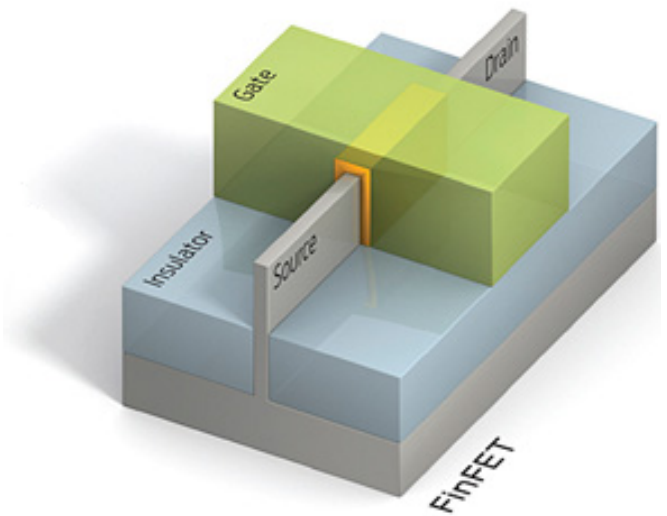
From 2D to 3D: FinFET

- 3D architecture brings the gate closer to the drain
- Conducting channel that rises above insulator level, creating a fin-shaped gate electrode



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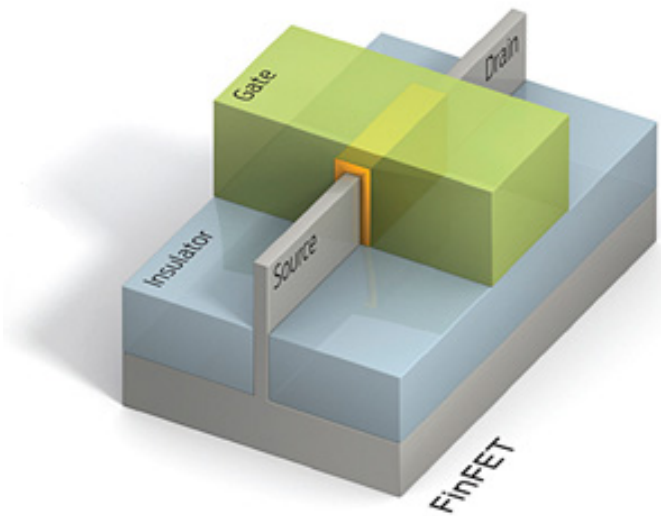

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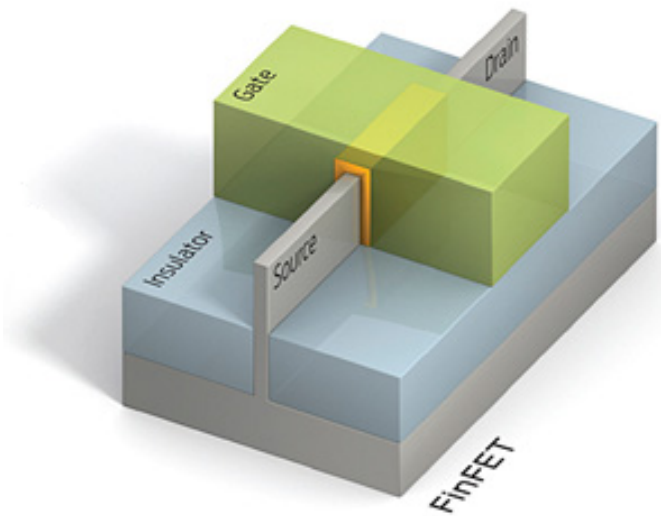

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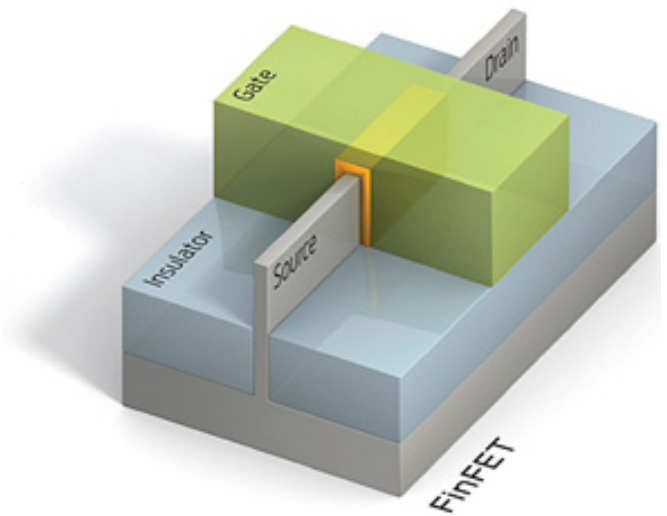

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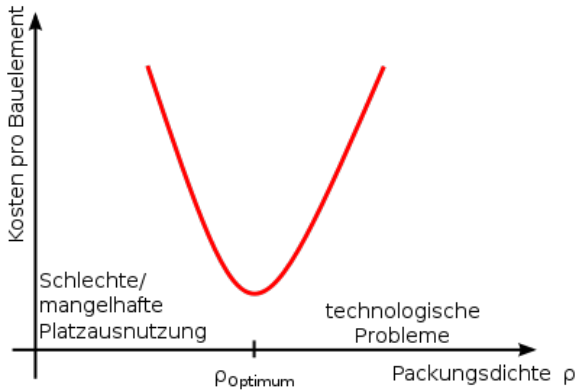
Moore's Law

- Goal: making the smallest transistor while staying in the cost optimum
- *Moore's Law* (1965): The transistor count on an integrated circuit will double every two years



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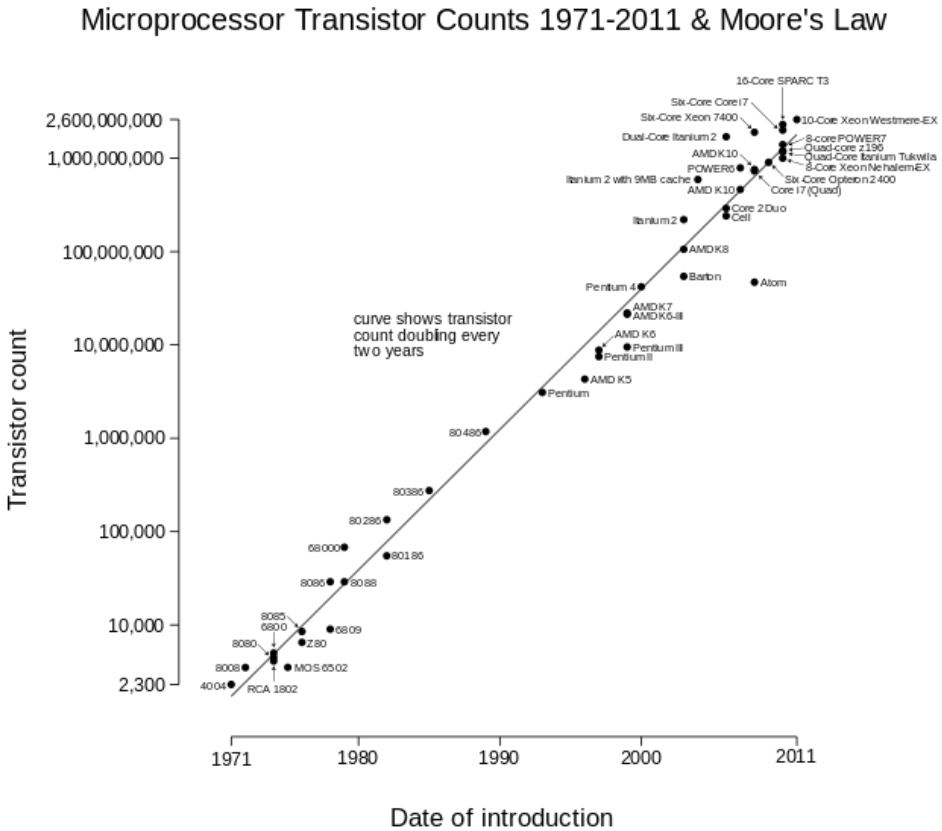

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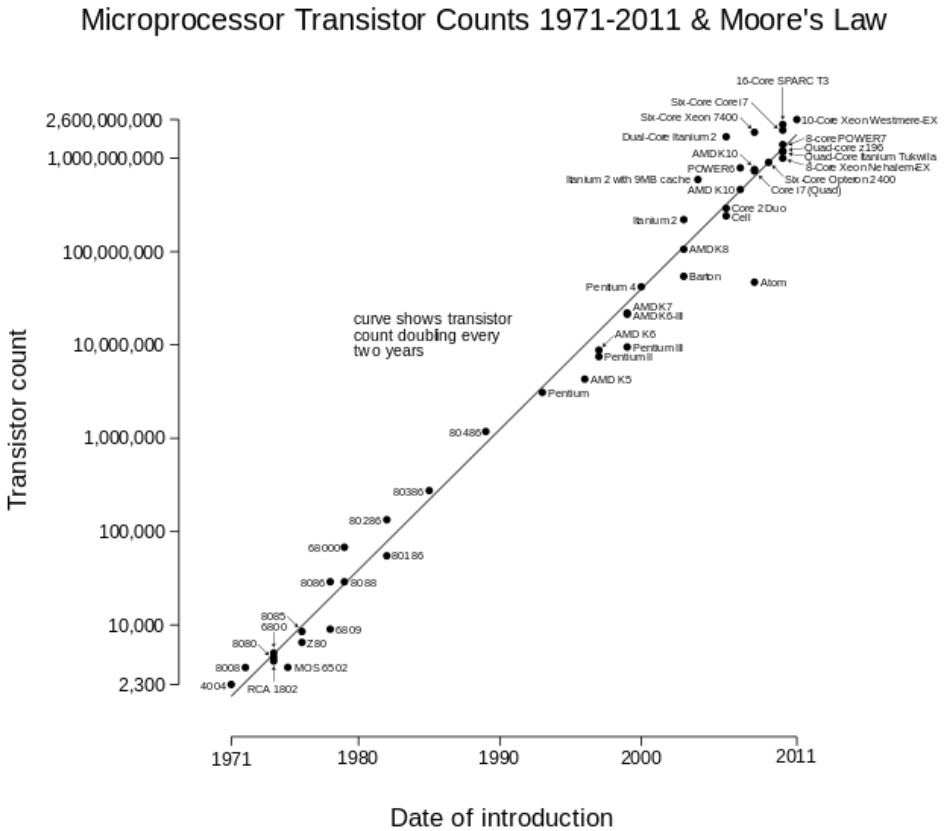

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Tunneling probability approximation (WKB)

- Time independent Schroedinger equation

$$-\frac{\hbar}{2m^*}\frac{d^2\Psi}{dx^2} + (V(x) - E)\Psi = 0,$$

has general solution $\Psi(x) = Ae^{kx} + Be^{-kx}$

- Assume potential is space-independent between x and $x + dx$:

$\Psi_{\rightarrow}(x+dx) = \Psi(x)exp(-k\ dx)$, where $k = \frac{\sqrt{2m^*[V(x) - E]}}{\hbar}$

- Plug in and get WKB approximation integral:

$$\Psi(L) = \Psi(0)exp(-\int_0^L \frac{\sqrt{2m^*[V(x) - E]}}{\hbar}dx)$$

Tunneling probability approximation (WKB)

- Use a triangular potential barrier: $V(x) - E = q\Phi_B(1 - \frac{x}{L})$ where Φ_B is the barrier height
- Calculate tunnel probability

$$\Gamma_{Tunnel}(L) = \frac{|\Psi(L)|^2}{|\Psi(0)|^2} = \frac{\Psi(L)\Psi(L)^*}{\Psi(0)\Psi(0)^*}$$

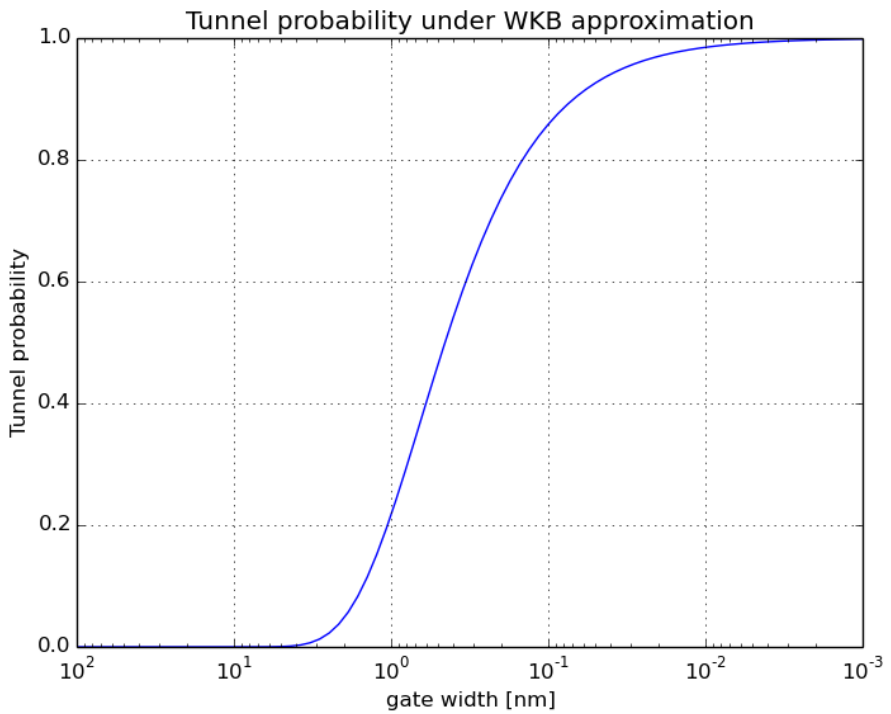
$$= exp(-2\int_0^L \frac{\sqrt{2m^*q}}{\hbar}\sqrt{\Phi_B(1-\frac{x}{L})}\,dx)$$

$$= exp(-\frac{4}{3}\frac{\sqrt{2m^*q\cdot\Phi_B}}{\hbar}\cdot L)$$

Tunneling probability approximation (WKB)

- For $q\Phi_B = q(\Phi_{ox} - \chi_{silicon}) = 0.25eV$, and $L = 1\,\mathrm{nm}$ we get

$$\Gamma \approx 21.7\%$$



Possible candidates?

- Tunnel FETS
- Gallium-Arsenide transistors
- Mott insulators
- Organic semiconductors
- Graphene transistors
- Photoemission-based microelectronic devices
- etc.

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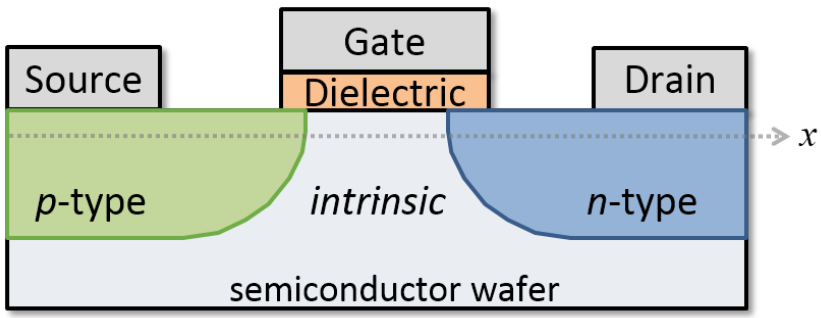
Tunnel Field Effect Transistor (TFET)

- Idea: use quantum tunneling!
- *p-i* and *i-n* junctions are used



Tunnel Field Effect Transistor (TFET)

- In Off-state, all charge carriers are initially in the valence band
- In On-state, the energy level of the intrinsic area is lowered with gate-voltage, which leads to a narrowing of the tunnel wall.
- The electrons tunnel from valence band to conducting band $\rightarrow$ current!

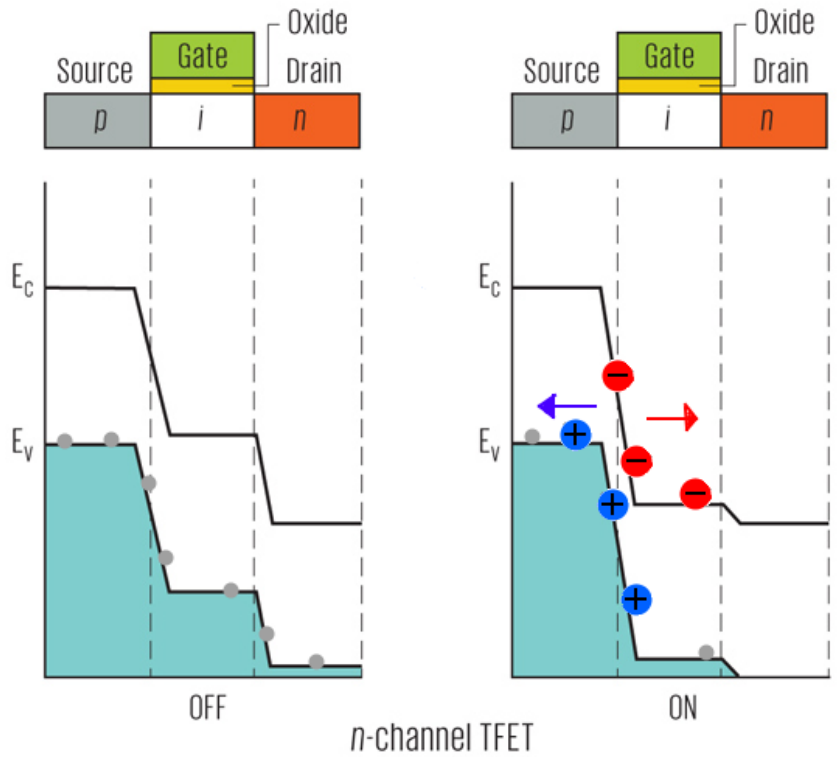


Figure: http://spectrum.ieee.org/semiconductors

Advantages and disadvantages of TFETs

- Much lower barrier thickness necessary ($\sim$ 1 atom)
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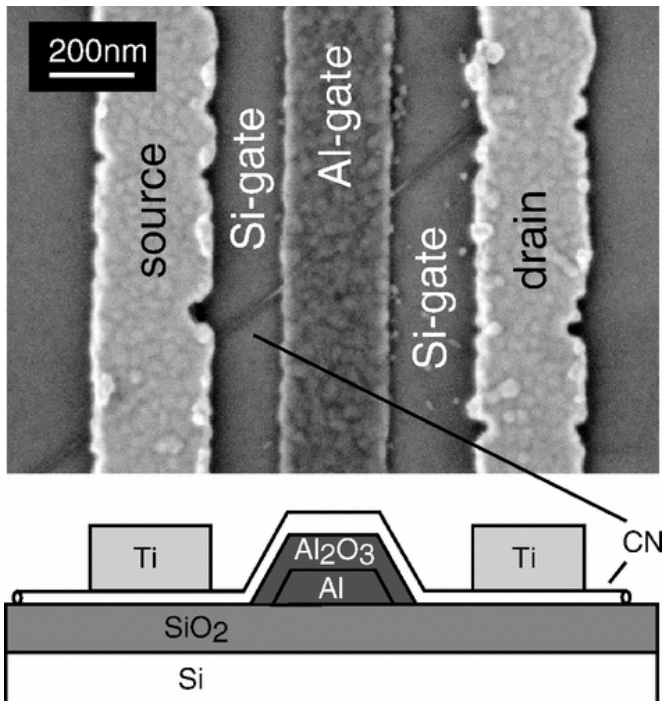

Figure: Appenzeller, J. (2004). Physical Review Letters 93 (19)

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Questions?

Backup Slides

Bipolar Junction Transistor (BJT)

- Combination of two junction diodes (*n*-*p*-*n* or *p*-*n*-*p*)
- Emitter, Base, Collector
- emitter-collector-current is controlled by current on base.
- EB in forward-bias, CE in reverse-bias

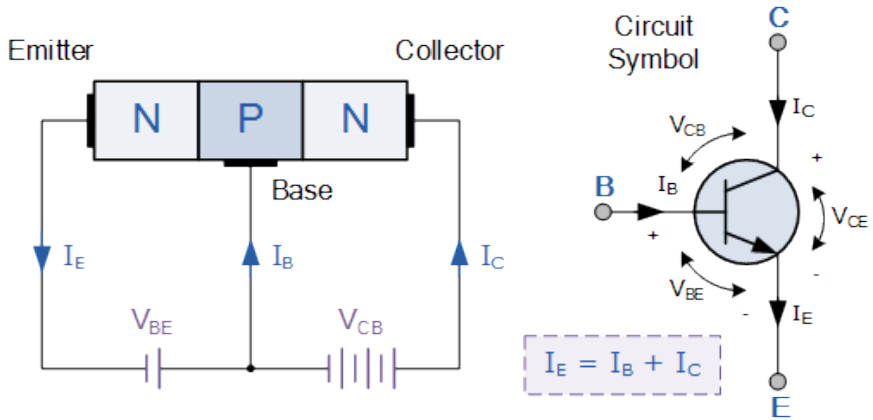


Figure : `http://www.electronics-tutorials.ws`

Bipolar Junction Transistor (BJT)

- *Cut-Off Region*: $I_B = 0 \rightarrow$ no CE-current.
- *Saturation Region*: $I_B > 0$ and V_{CE} small $\rightarrow$ large CE-current, no control
- *Active Region*: $I_B > 0$ and V_{CE} large $\rightarrow$ CE-current controlled by base-current

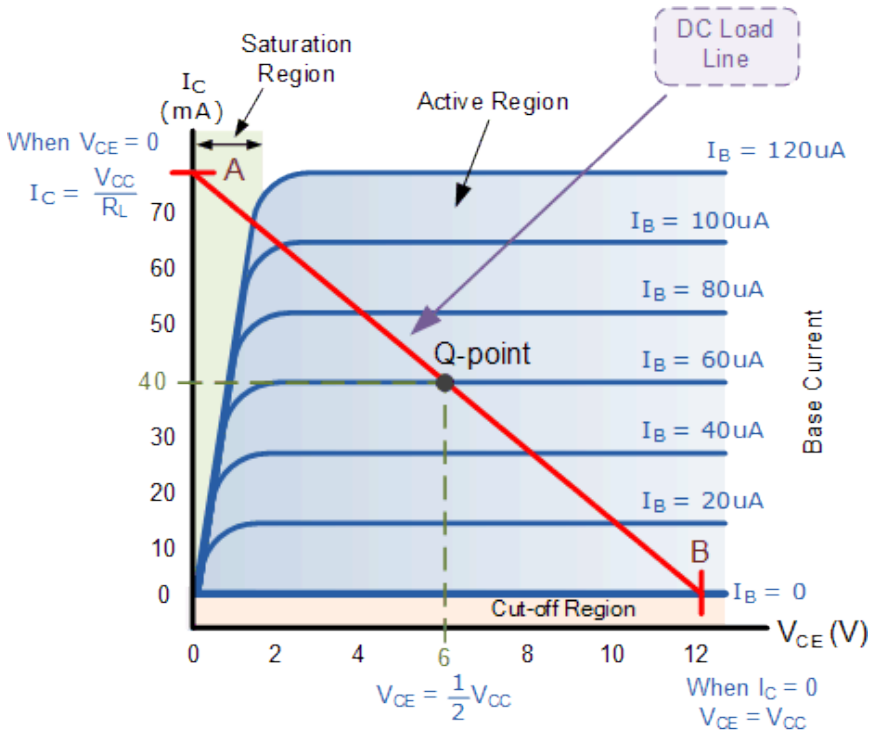
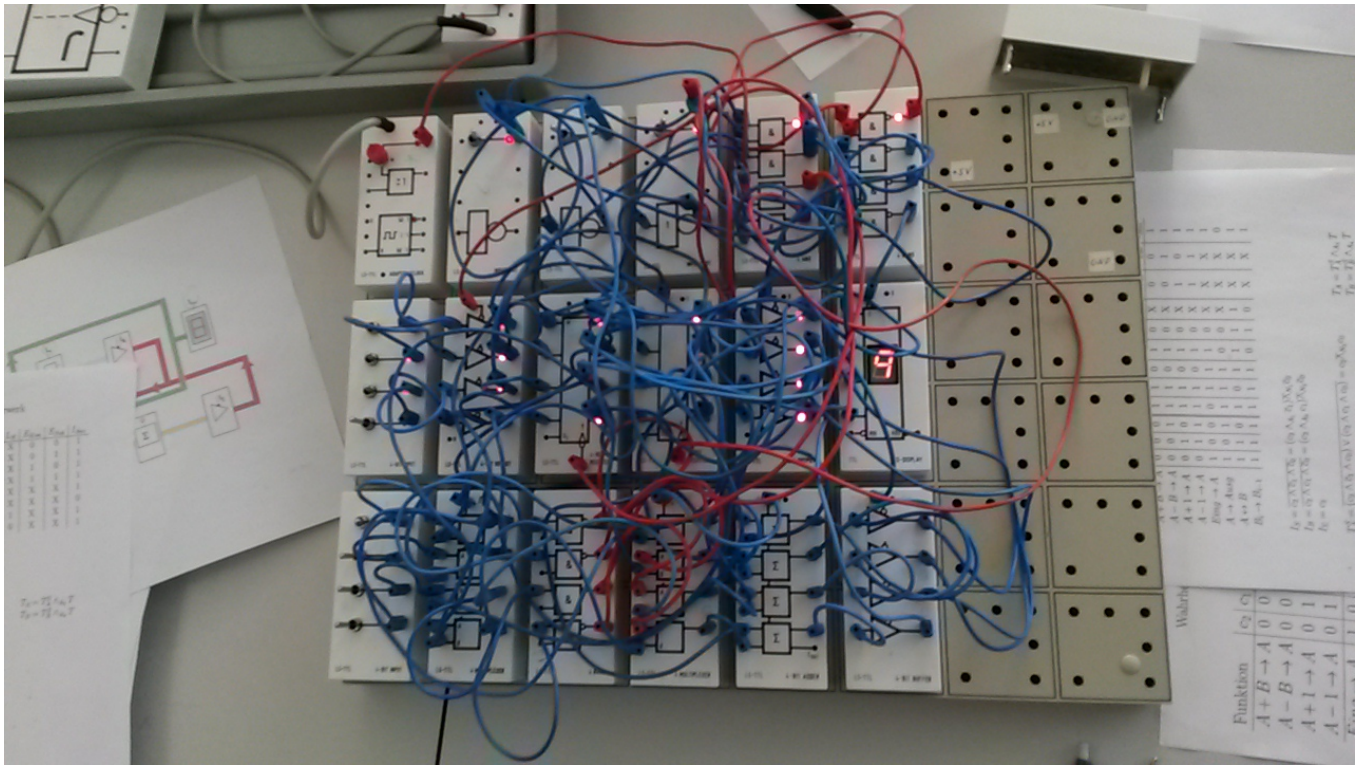


Figure : http://www.electronics-tutorials.ws

Manufacturing Process

1. Create Wafer: Sand $\xrightarrow{melting}$ Monochrystalline Silicon Ingot $\xrightarrow{slicing}$ Silicon Wafer
2. Photolithography: Applying photoresist chemical to Wafer $\rightarrow$ Exposure by masked UV-rays $\rightarrow$ Removal of soluble photoresist chemicals
3. Doping: Patterned photoresist is exposed by a beam of ions (n-type & p-type) $\rightarrow$ Removal of photoresist chemicals
4. Etching: Protect desired parts by hard mask $\rightarrow$ Photolithography again
5. Gate Formation: Form temporarily gate with silicon $\rightarrow$ Fill areas with insulator $\rightarrow$ Add dielectric $\rightarrow$ Electroplating

Logic Gates



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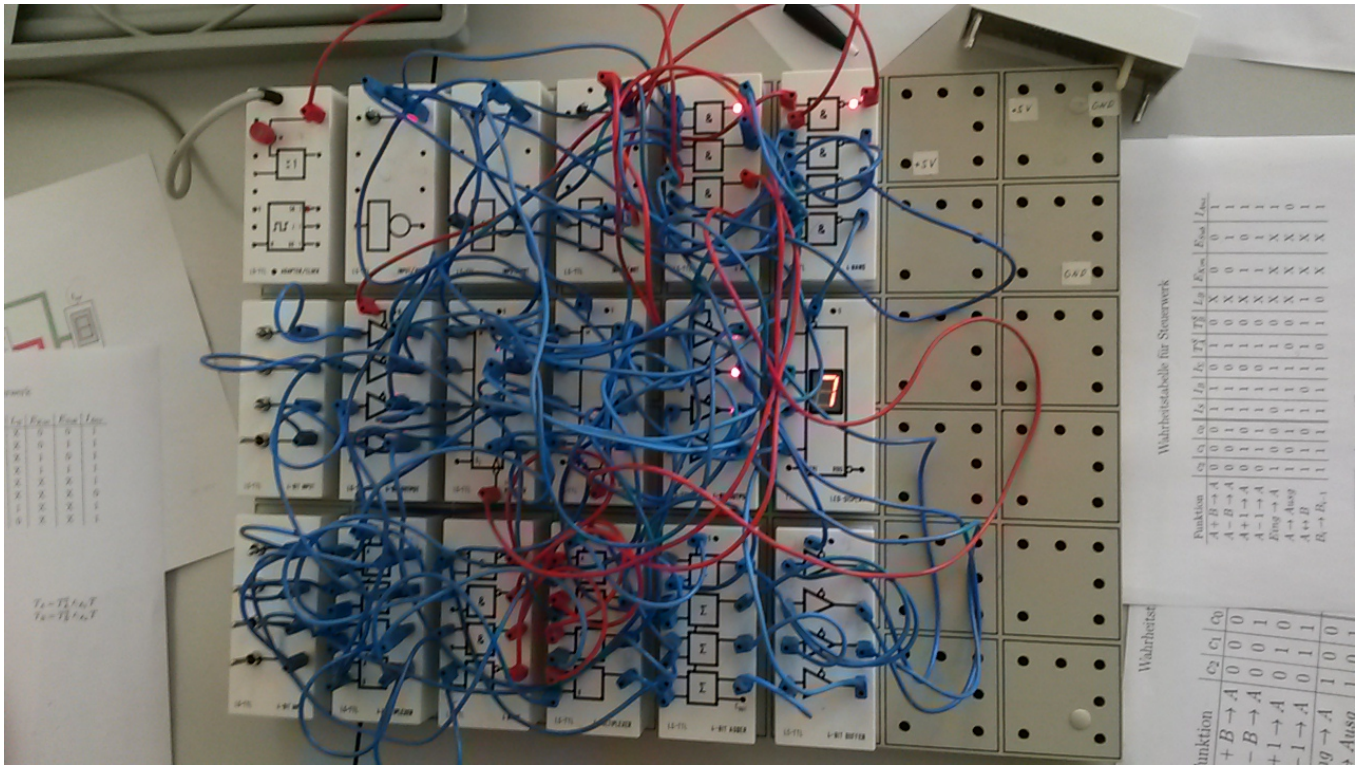

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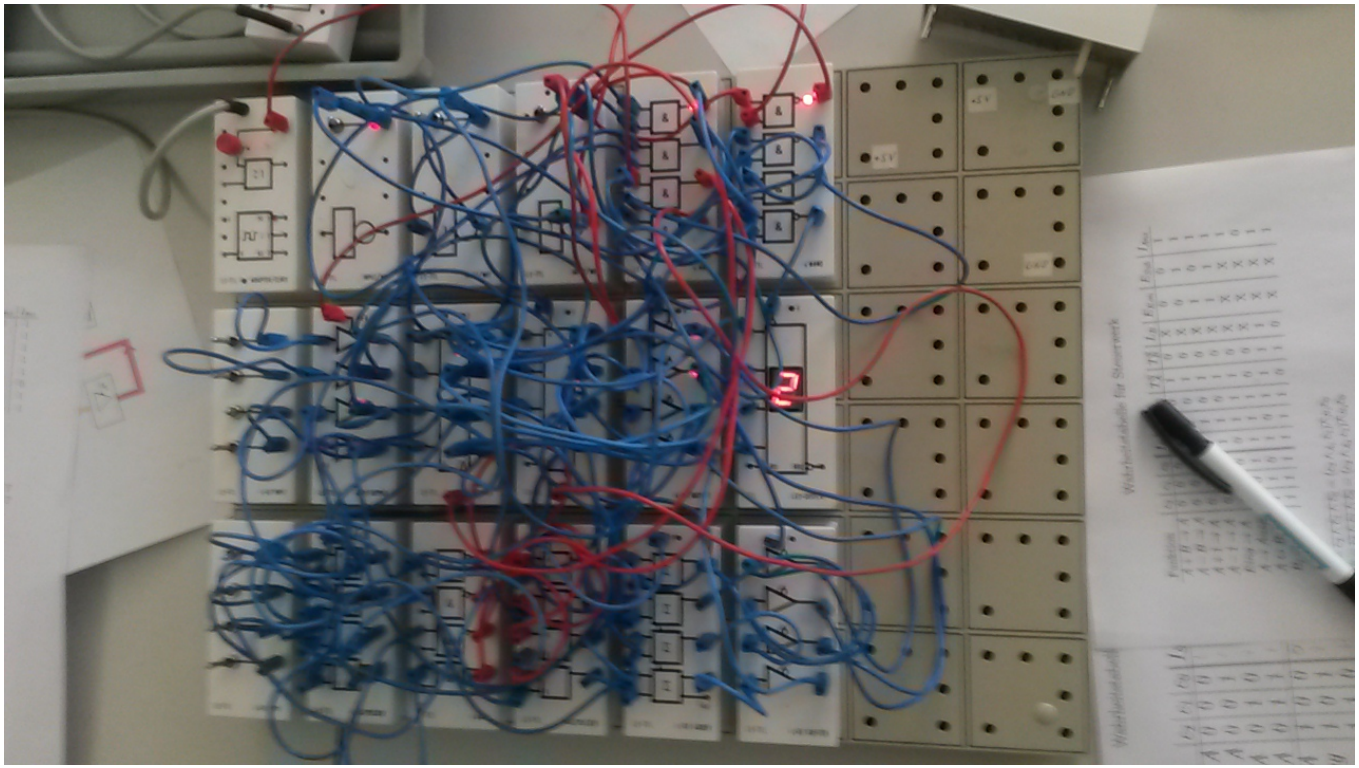

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