Ordering number : ENN*6700

CMOS IC

LC866548/40/32/28/24A

8-Bit Single Chip Microcontroller

Preliminary

Overview

- CPU : Operable at a minimum bus cycle time of 0.5µs (microsecond)
- On-chip ROM maximum capacity : 48K bytes
- On-chip RAM capacity : 1152 bytes (LC866548A/40A/32A)
  : 896 bytes (LC866528A/24A)
- VFD automatic display controller/driver
- 16-bit timer/counter (or two 8-bit timers)
- 16-bit timer/ PWM (or two 8-bit timers)
- 8-channels × 8 bit AD Converter
- Two 8-bit synchronous serial-interface circuits (1-channel × 16 bit, 1-channel × 8 bit)
- 14-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

(1) Read Only Memory (ROM)	: LC866548A	49152 × 8 bits
	: LC866540A	40960 × 8 bits
	: LC866532A	32768 × 8 bits
	: LC866528A	28672 × 8 bits
	: LC866524A	24576 × 8 bits

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(2) Random Access Memory (RAM) : LC866548A/40A/32A 1152 × 8 bits
LC866528A/24A 896 × 8 bits

(3) Bus Cycle Time / Instruction Cycle Time

The bus cycle time indicates the speed to read ROM.

Bus cycle time	Cycle time	Clock divider	System clock oscillation	Oscillation Frequency	Voltage
0.5μs	1μs	1/1	Ceramic resonator oscillation	6MHz	4.5 - 6.0V
2μs	4μs	1/2	Ceramic resonator oscillation	3MHz	4.5 - 6.0V
7.5μs	15μs	1/2	RC resonator oscillation	800MHz	4.5 - 6.0V
183μs	366μs	1/2	Crystal oscillation	32.768kHZ	4.5 - 6.0V

Note : External resisters (Rf, Rd) are required when X'tal oscillation is used.

(4) Ports

- Input/output ports : 3 ports (16 terminals : port 1, 7, 8)
  Input/output port programmable in a bit
- 15V withstand Input/output ports : 2 ports (16 terminals)
  Input/output port programmable nibble unit : 1 port (8 terminals : port 0)
  (When the N-channel open drain output is selected, the data in a bit can be inputted.)
  Input/output port programmable in a bit : 1 port (8 terminals : port 3)
- Input port : 2 ports (6 terminals : port 7, 8)
- VFD output port : 52 terminals
  Large current output for digit : 16 terminals
  Pull-down resistor option available
- Other function
  Input/output port : 2 ports (12 terminals : port F, G)
  Input port : 3 ports (24 terminals : port C, D, E)

(5) VFD automatic display controller

- Segment/digit output pattern programmable
  Any segment/digit combination available
  VFD parallel-drive available
- 16-step dimmer function available

(6) AD converter

- 8-channels × 8-bit AD converter

(7) Serial interface

- 1-channel × 16-bit serial interface circuits
- 1-channel × 8-bit serial interface circuits
- LSB first/MSB first function available
- Internal 8-bit baud-rate generator in common with two serial interface circuits
- SIO automatic transmission available (2-32 byte data can be transmitted with program automatically and continuously.)

(8) Timers

- Timer 0 : 16-bit timer/counter with 2-bit prescaler + 8-bit programmable prescaler
  - Mode 0 : Two 8-bit timers with programmable prescaler
  - Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
  - Mode 2 : 16-bit timer with a programmable prescaler
  - Mode 3 : 16-bit counter

  The resolution of Timer is tCYC. (tCYC : cycle time)
- Timer 1 : 16-bit timer/PWM with
  - Mode 0 : Two 8-bit timers
  - Mode 1 : 8-bit timer + 8-bit PWM
  - Mode 2 : 16-bit timer
  - Mode 3 : Variable-bit PWM (9-16 bits)

  In Mode 0 and Mode 1, the resolution of Timer and PWM is tCYC.
  In Mode 2 and Mode 3, the resolution of Timer and PWM selectable : tCYC or 1/2tCYC by program

- Base timer

  Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock)
  Every 976μs, 3.9ms, 15.6ms, 62.5ms overflow system (using 32.768kHz crystal oscillation for Base timer clock)
  The Base timer clock selectable ; 32.768kHz crystal oscillation, System clock, and programmable prescaler output of Timer 0

(9) Buzzer output

- The Buzzer sound frequency selectable ; 4kHz, 2kHz (using 32.768kHz crystal oscillation for Base timer clock)

(10) Remote control receiver circuit (connected to the P73/INT3/T0IN terminal)

- Noise rejection function (the time constant of noise rejection filter : 1tCYC/16tCYC/64tCYC)
  (tCYC : instruction cycle time)
- Polarity switching

(11) Watchdog timer

- The watchdog timer is taken on RC outside
- Watchdog timer operation selectable : interrupt system, system reset

(12) Interrupt system

- 14-source 10-vectored interrupts :
  1. External Interrupt INT0 (include watchdog timer)
  2. External Interrupt INT1
  3. External Interrupt INT2, Timer/counter T0L (Lower 8 bits)
  4. External Interrupt INT3, base timer
  5. Timer/counter T0H (Upper 8 bits)
  6. Timer T1H / T1L
  7. Serial interface SIO0
  8. Serial interface SIO1
  9. AD converter
  10. VFD automatic display controller, Port 0
- Built-in Interrupt priority control register

  Microcontroller allows 3 levels of interrupt ; low level, high level, and highest level of multiplex interrupt. It can specify a low level or a high level interrupt priority from INT2/T0L through port 0 (i. e. the above interrupt number from three through ten). It can also specify a low level or the highest level interrupt priority to INT0 and INT1.

(13) Subroutine stack levels

- 128 levels (Max.) : Stack area included in RAM area

(14) Multiplication and division
- 16 bit × 8 bit (7 instruction cycle times)
- 16 bit ÷ 8 bit (7 instruction cycle times)

(15) Three oscillation circuits
- On-chip RC oscillation circuit used for the system clock
- On-chip CF oscillation circuit used for the system clock
- On-chip Crystal oscillation circuit used for the system clock and for time-base clock
  Note : External resisters (Rf, Rd) are required

(16) Standby function
- HALT mode function
  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This operation mode can be released by the interrupt request signals or the initial system reset request signal.
- HOLD mode function
  The HOLD mode is used to stop all the oscillations ;
  RC (internal), CF and Crystal oscillations. This mode can be released by the following operations.
  • Reset terminal ($\overline{\text{RES}}$) set to low level.
  • Input a assigned level to P70/INT0/T0IN or P71/INT1/T0IN terminal.
  • Input a Port0 interrupt condition.

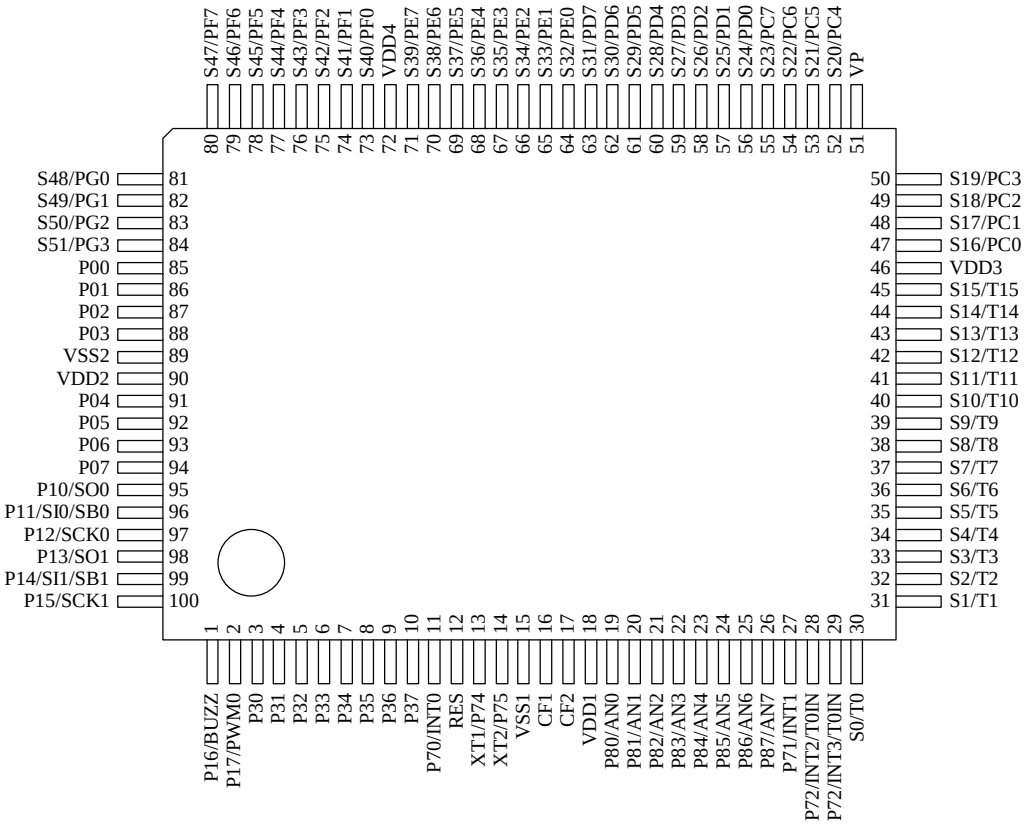
(17) Factory shipment
QFP100E delivery form

(18) Development Tools
- Evaluation chip : LC866094
- EPROM version : LC86E6548
- One time version : LC86P6548
- Emulator : EVA86000 + ECB866500 (Evaluation chip board) + POD866500 (Pod)

• Notes for use
Follow the under table.

Frequency range of the system clock	Voltage range	Clock Divider	Note
15kHz to 3MHz	4.5V to 6.0V	1/1	Can not use 1/2 divider
30kHz to 6MHz		1/1, 1/2	
Internal RC oscillation		1/1, 1/2	

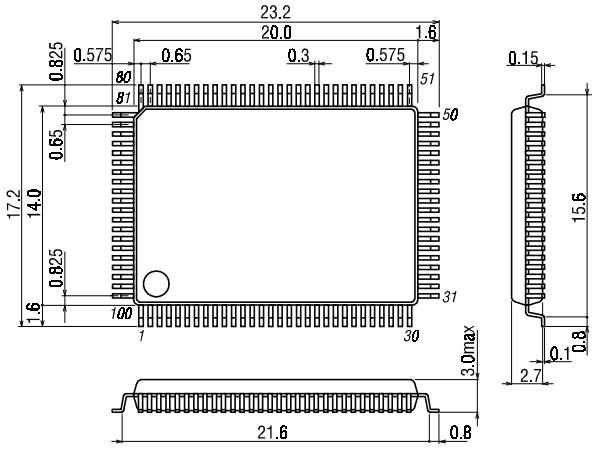
Pin Assignment QIP100E



Package Dimension

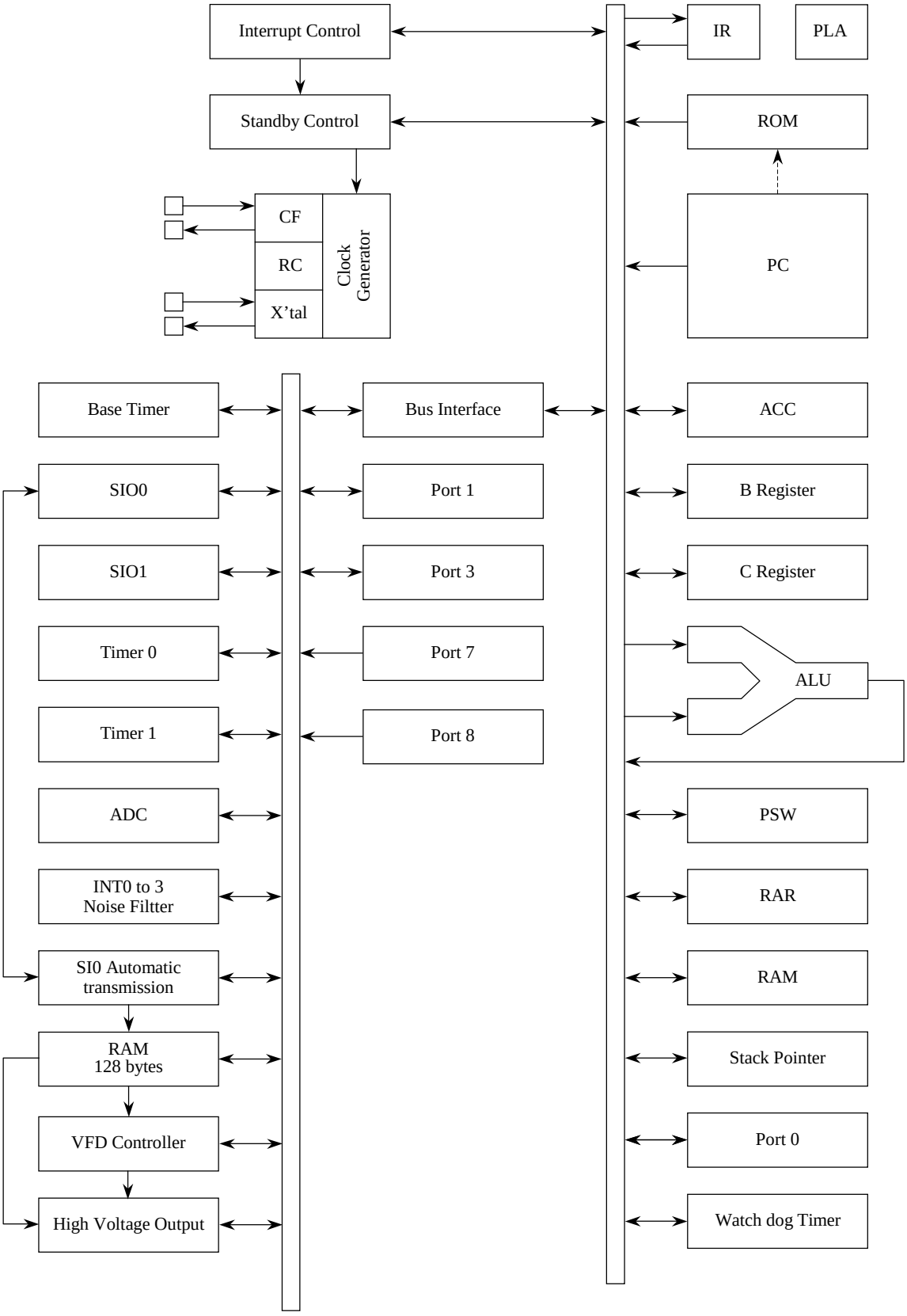
(unit : mm)

3151



SANYO : QIP-100E

System Block Diagram



LC866548A/40A/32A/28A/24A Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function Description</th><th>Option</th></tr>
<tr><td>VSS1, 2</td><td></td><td>Power pin (-) *1</td><td></td></tr>
<tr><td>VDD1,2,3,4</td><td></td><td>Power pin (+) *1</td><td></td></tr>
<tr><td>VP</td><td></td><td>Power pin (+) for the VFD output pull-down resist</td><td></td></tr>
<tr><td>Port 0
P00 - P07</td><td>I/O</td><td>•8-bit input/output port
Input/output in nibble units
•Input for port 0 interrupt
•Input for HOLD release
•15V withstand at N-channel open drain output</td><td>•Pull-up resistor :
Provided/Not provided (each nibble)
•Output form :
CMOS/N-channel open drain
(each bit)</td></tr>
<tr><td>Port 1
P10 - P17</td><td>I/O</td><td>•8-bit Input/output port
Input/output can be specified in bit unit.
•Other pin functions
<table>
<tr><td>P10</td><td>SIO0 data output</td></tr>
<tr><td>P11</td><td>SIO0 data input/bus input/output</td></tr>
<tr><td>P12</td><td>SIO0 clock input/output</td></tr>
<tr><td>P13</td><td>SIO1 data output</td></tr>
<tr><td>P14</td><td>SIO1 data input/bus input/output</td></tr>
<tr><td>P15</td><td>SIO1 clock input/output</td></tr>
<tr><td>P16</td><td>Buzzer output</td></tr>
<tr><td>P17</td><td>Timer1 output (PWM0 output)</td></tr>
</table></td><td>•Output form :
CMOS/N-channel open drain
(each bit)</td></tr>
<tr><td>Port 3
P30 - P37</td><td>I/O</td><td>•8-bit input/output port
Input/output in bit unit
•15V withstand at N-channel open drain output</td><td>•Output form :
CMOS/N-channel open drain
(each bit)</td></tr>
<tr><td>Port 7
P70 - P73
$\overline{P74}$ - P75</td><td>
I/O
I</td><td>•4-bit input/output port
Input/output in bit unit
•2-bit input port
•Other pin function
<table>
<tr><td>P70</td><td>INT0 input/HOLD release /Nch-Tr. output for watchdog timer</td></tr>
<tr><td>P71</td><td>INT1 input/HOLD release input</td></tr>
<tr><td>P72</td><td>INT2 input/timer 0 event input</td></tr>
<tr><td>P73</td><td>INT3 input with noise filter/timer 0 event input</td></tr>
<tr><td>$\overline{P74}$</td><td>Input pin XT1 for 32.768kHz crystal resonator oscillation</td></tr>
<tr><td>P75</td><td>Output pin XT2 for 32.768kHz crystal resonator oscillation</td></tr>
</table>
•Interrupt received form, vector address
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising/ falling</th><th>H level</th><th>L level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td></td></tr>
<tr><td>Port 8
P80 - P83
P84 - P87</td><td>
I
I/O</td><td>•4-bit input/output port
Input/output in bit unit
•4-bit input port
•Other function
AD input port (8 port pins)</td><td></td></tr>
<tr><td>S0/T0 to
S6/T6</td><td>O</td><td>Output for VFD display controller
segment/timing in common</td><td>Pull-down resistor :
Provided/Not provided (each bit)</td></tr>
</table>

(continue)

Pin Name	I/O	Function Description	Option
S7/T7 to S15/T15	O	•Output for VFD display controller segment/timing with internal pull-down resistor in common •Internal pull-down resistor output	
S16 to S31	I/O	•Output for VFD display controller segment •Other function S16 : High voltage input port PC0 S17 : High voltage input port PC1 S18 : High voltage input port PC2 S19 : High voltage input port PC3 S20 : High voltage input port PC4 S21 : High voltage input port PC5 S22 : High voltage input port PC6 S23 : High voltage input port PC7 S24 : High voltage input port PD0 S25 : High voltage input port PD1 S26 : High voltage input port PD2 S27 : High voltage input port PD3 S28 : High voltage input port PD4 S29 : High voltage input port PD5 S30 : High voltage input port PD6 S31 : High voltage input port PD7	Pull-down resistor : Provided/Not provided (each bit)
S32 to S47	I/O	•Output for VFD display controller segment •Other function S32 : High voltage input port PE0 S33 : High voltage input port PE1 S34 : High voltage input port PE2 S35 : High voltage input port PE3 S36 : High voltage input port PE4 S37 : High voltage input port PE5 S38 : High voltage input port PE6 S39 : High voltage input port PE7 S40 : High voltage I/O port PF0 S41 : High voltage I/O port PF1 S42 : High voltage I/O port PF2 S43 : High voltage I/O port PF3 S44 : High voltage I/O port PF4 S45 : High voltage I/O port PF5 S46 : High voltage I/O port PF6 S47 : High voltage I/O port PF7	Pull-down resistor : Provided/Not provided (each bit)
S48 to S51	I/O	•Output for VFD display controller segment •Other function S48 : High voltage I/O port PG0 S49 : High voltage I/O port PG1 S50 : High voltage I/O port PG2 S51 : High voltage I/O port PG3	
$\overline{RES}$	I	Reset pin	
XT1/ $\overline{P74}$	I	•Input pin for 32.768kHz crystal oscillation •Other function $\overline{P74}$ for input port In case of non use, connect to VDD1.	

(continue)

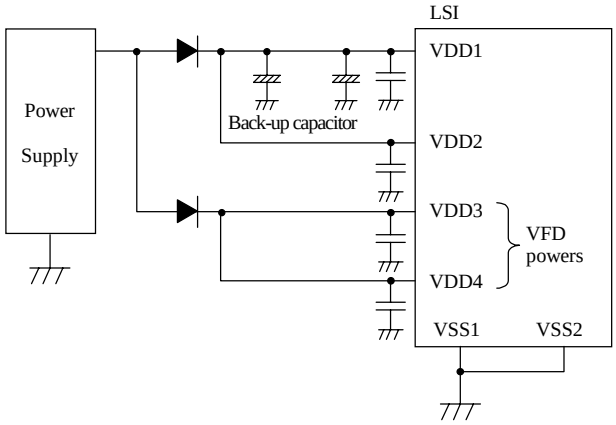
Pin Name	I/O	Function Description	Option
XT2/P75	O	•Output pin for 32.768kHz crystal oscillation •Other function P75 for input port •In case of non use, At using as oscillator, should be left opened. At using as a port, connect to VDD1.	
CF1	I	Input pin for ceramic resonator oscillation	
CF2	O	Output pin for ceramic resonator oscillation	

* All of port options (except pull-up resistor of port 0) can be specified in bit unit.
* A state of pins at reset

Pin name	Input/output mode	A state of pull-up resistor specified at pull-up option
Port 0	Input	Fixed pull-up resistor OFF
Ports 1, 3	Input	Programmable pull-up resistor OFF

S0/T0 to S15/T15	P channel Transistor OFF
S16 to S51	P channel Transistor OFF

*1 Connect like the following figure to reduce noise into a VDD1 terminal.
• Shorted the VSS1 terminal to the VSS2 terminal and to make the back-up time long.



1. Absolute Maximum Ratings at VSS1=VSS2=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions		Ratings			unit
					VDD[V]	min.	typ.	max.	
Supply voltage		VDD MAX	VDD1, VDD2 VDD3, VDD4	VDD1=VDD2 =VDD3=VDD4		-0.3		+7.0	V
Input voltage		VI(1)	•Ports $\overline{74}$,75 •Ports 80,81,82, 83 •Port 8 • $\overline{RES}$			-0.3		VDD+0.3	
		VI(2)	VP			VDD-45		VDD+0.3	
Output voltage		VO	S0/T0-S15/T15			VDD-45		VDD+0.3	
Input/output voltage		VIO(1)	•Port 1 •Ports 70,71,72, 73 •Ports 84,85,86, 87 •Ports 0, 3 at CMOS output option			-0.3		VDD+0.3	
		VIO(2)	Ports 0, 3 at N-ch open drain output option			-0.3		15	
		VIO(3)	S16 - S51			VDD-45		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 3	•CMOS output •For each pin.		-10			mA
		IOPH(2)	S0/T0-S15/T15	For each pin.		-30			
		IOPH(3)	S16 - S51	For each pin.		-15			
	Total output current	ΣIOAH(1)	Port 0	The total of all pins.		-30			
		ΣIOAH(2)	Ports 1, 3			-30			
		ΣIOAH(3)	S0/T0-S15/T15			-55			
		ΣIOAH(4)	S16 - S27			-60			
		ΣIOAH(5)	S28 - S39			-60			
		ΣIOAH(6)	S40 - S51			-60			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3	For each pin.				20	
		IOPL(2)	•Ports 70,71,72, 73 •Ports 84,85,86, 87					15	
	Total output current	ΣIOAL(1)	Port 0	The total of all pins.				60	
		ΣIOAL(2)	Ports 1, 3, 70					50	
		ΣIOAL(3)	•Ports 71,72, 73 •Ports 84,85,86, 87					20	
Power dissipation (max.)		Pdmax	QFP100E	Ta=-30 to+70°C				500	mW
Operating temperature range		Topr				-30		70	°C
Storage temperature range		Tstg				-55		125	

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Operating supply voltage range	VDD(1)	VDD1=VDD2 =VDD3=VDD4	0.98μs ≤ tCYC tCYC ≤ 400μs		4.5		6.0	V
Hold voltage	VHD	VDD1=VDD2	RAMs and the Registers hold voltage at HOLD mode.		2.0		6.0	
Pull-down voltage	VP	VP		4.5 - 6.0	-35		VDD	
Input high voltage	VIH(1)	Port 0 at CMOS output option	Output disable	4.5 - 6.0	0.33VDD +1.0		VDD	
	VIH(2)	Port 0 at N-ch open drain output	Output disable	4.5 - 6.0	0.75VDD		13.5	
	VIH(3)	•Port 1 •Ports 72, 73 •Port 3 at CMOS output option	Output disable	4.5 - 6.0	0.75VDD		VDD	
	VIH(4)	Port 3 at N-ch open drain output	Output disable Tr. OFF	4.5 - 6.0	0.75VDD		13.5	
	VIH(5)	•Port 70 port input /interrupt •Port 71 • $\overline{\text{RES}}$	Output disable	4.5 - 6.0	0.75VDD		VDD	
	VIH(6)	Port 70 Watchdog timer	Output disable	4.5 - 6.0	0.9VDD		VDD	
	VIH(7)	•Port 8 •Ports $\overline{74}$, 75	Output disable	4.5 - 6.0	0.75VDD		VDD	
	VIH(8)	S16 - S51	Output P-channel Tr. OFF	4.5 - 6.0	0.33VDD +1.0		VDD	
Input low voltage	VIL(1)	Port 0 at CMOS output option	Output disable	4.5 - 6.0	VSS		0.2VDD	
	VIL(2)	Port 0 at N-ch open drain output	Output disable	4.5 - 6.0	VSS		0.25VDD	
	VIL(3)	•Ports 1, 3 •Ports 72, 73	Output disable	4.5 - 6.0	VSS		0.25VDD	
	VIL(4)	•Port 70 port input /interrupt •Port 71 • $\overline{\text{RES}}$	Output disable	4.5 - 6.0	VSS		0.25VDD	
	VIL(5)	Port 70 Watchdog timer	Output disable	4.5 - 6.0	VSS		0.8VDD -1.0	
	VIL(6)	•Port 8 •Ports $\overline{74}$, 75	Output disable	4.5 - 6.0	VSS		0.25VDD	
	VIL(7)	S16 - S51	Output P-channel Tr. OFF	4.5 - 6.0	VP		0.2VDD	
Operation cycle time	tCYC			4.5 - 6.0	0.98		400	μs

(continue)

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 - 6.0		6		MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 - 6.0		3		
	FmRC		RC oscillation	4.5 - 6.0	0.3	0.8	3.0	
	FsX'tal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	4.5 - 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 - 6.0		0.1	3.0	ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 - 6.0		0.1	3.0	
	tssX'tal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5 - 6.0		0.7	1.0	s

(Note 1) The oscillation constant is shown on table 1.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Input high current	IIH(1)	Ports 0, 3 of open drain output	•Output disable •VIN=13.5V (including off-leak current of the output Tr.)	4.5 - 6.0			5	μA
	IIH(2)	•Port 0 without pull-up MOS Tr. •Ports 1, 3	•Output disable •Pull-up MOS Tr. OFF •VIN=VDD (including off-leak current of the output Tr.)	4.5 - 6.0			1	
	IIH(3)	•Ports70,71,72,73 •Port 8	•Output disable •VIN=VDD (including off-leak current of the output Tr.)	4.5 - 6.0			1	
	IIH(4)	$\overline{\text{RES}}$	VIN=VDD	4.5 - 6.0			1	
	IIH(5)	Ports $\overline{74}$, 75	VIN=VDD	4.5 - 6.0			1	
	IIH(6)	S16 to S51 without pull-down resistor (Ports C, D, E, F,G)	•Output P-channel Tr. OFF •VIN=VDD	4.5 - 6.0			1	
Input low current	IIL(1)	•Ports 1, 3 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF •VIN=VSS (including off-leak current of the output Tr.)	4.5 - 6.0	-1			μA
	IIL(2)	•Ports70,71,72,73 •Port 8	•Output disable •VIN=VSS (including off-leak current of the output Tr.)	4.5 - 6.0	-1			
	IIL(3)	$\overline{\text{RES}}$	VIN=VSS	4.5 - 6.0	-1			
	IIL(4)	Ports $\overline{74}$, 75	VIN=VSS	4.5 - 6.0	-1			
Output high voltage	VOH(1)	Ports 0, 1, 3 of CMOS output	IOH=-1.0mA	4.5 - 6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	4.5 - 6.0	VDD-0.5			
	VOH(3)	S0/T0 to S15/T15	IOH=-20mA	4.5 - 6.0	VDD-1.8			
	VOH(4)		•IOH=-1mA •The current of any unmeasurement pin is not over 1mA.	4.5 - 6.0	VDD-1			
	VOH(5)	S16 to S51	IOH=-5mA	4.5 - 6.0	VDD-1.8			
	VOH(6)		The current of any unmeasurement pin is not over 1mA.	4.5 - 6.0	VDD-1			

(continue)

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	typ.	max.	unit
Output low voltage	VOL(1)	Ports 0, 1, 3	IOL=10mA	4.5 - 6.0			1.5	V
	VOL(2)		IOL=1.6mA	4.5 - 6.0			0.4	
	VOL(3)	Port 70	IOL=1mA	4.5 - 6.0			0.4	
	VOL(4)	•Ports 71, 72, 73 •Ports84,85,86,87	IOL=1.6mA	4.5 - 6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	Ports 0, 1, 3	VOH=0.9VDD	4.5 - 6.0	15	40	70	KΩ
Output off-leak current	IOFF(1)	S0/T0 to S6/T6, S16 to S51 without pull-down resistor	•Output P-ch Tr. OFF •VOUT=VSS	4.5 - 6.0	-1			μA
	IOFF(2)		•Output P-ch Tr. OFF •VOUT=VDD-40V	4.5 - 6.0	-30			
Resistance of the low level hold Tr.	Rinpd	S16 to S51	•Output P-ch Tr. OFF •Using as input ports	4.5 - 6.0		200		kΩ
High voltage pull-down resistor	Rpd	S0/T0 to S15/T15, S16 to S51 with pull-down resistor	•Output P-ch Tr. OFF •VOUT=3V •Vp=-30V	5.0	60	100	200	
VP pull-down resistor	Rvppd	Vp	•VSS=GND •Vp=-30V	5.0	60	100	200	
Hysteresis voltage	VHIS	•Port 1 •Ports 70, 71, 72, 73, 75 • $\overline{\text{RES}}$	Output disable	4.5 - 6.0		0.1 VDD		V
Pin capacitance	CP	All pins	•f=1MHz •Unmeasurement terminals for the input are set to VSS level. •Ta=25°C	4.5 - 6.0		10		pF

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	•SCK0 •SCK1	Refer to figure 5.	4.5 - 6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	•SCK0 •SCK1	•Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5.	4.5 - 6.0	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set up time		tICK	SI0 SI1 SB0 SB1	•Data set-up to SCK0, 1. •Data hold from SCK0, 1. •Refer to figure 5.	4.5 - 6.0	0.1			µs
	Data hold time		tCKI				0.1			
Serial output	Output delay time (Serial clock is external clock)		tCKO(1)	SO0 SO1 SB0 SB1	•Use pull-up resistor (1kΩ) when open drain output. •Data hold from SCK0, 1 •Refer to figure 5.	4.5 - 6.0			7/12tCYC +0.2	
	Output delay time (Serial clock is internal clock)		tCKO(2)						1/3tCYC +0.2	

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 - 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is select to 1/1.)	•Interrupt acceptable •Timer0-countable	4.5 - 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is select to 1/16.)	•Interrupt acceptable •Timer0-countable	4.5 - 6.0	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock is select to 1/64.)	•Interrupt acceptable •Timer0-countable	4.5 - 6.0	128			
	tPIL(5)	$\overline{\text{RES}}$	Reset acceptable	4.5 - 6.0	200			µs

6. AD Converter Characteristics at Ta=-30°C to + 70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Resolution	N			4.5 - 6.0		8		bit
Absolute precision (Note2)	ET			4.5 - 6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time =16 × tCYC (ADCR2=0) *Note3	4.5 - 6.0	15.68 (tCYC =0.98μs)		65.28 (tCYC =4.08μs)	μs
			AD conversion time =32 × tCYC (ADCR2=1) *Note3	4.5 - 6.0	31.36 (tCYC =0.98μs)		130.56 (tCYC =4.08μs)	
Analog input voltage range	VAIN	AN0 - AN7		4.5 - 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 - 6.0			1	μA
	IAINL		VAIN=VSS	4.5 - 6.0	-1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).
(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current dissipation during basic operation (Note 4)	IDDOP(1)		•FmCF=6MHz Ceramic resonator oscillation •Internal RC oscillation stops. •FsXtal=32.768kHz Crystal oscillation •System clock : CF oscillation •1/1 divided	4.5 - 6.0		10	25	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation •Internal RC oscillation stops. •FsXtal=32.768kHz Crystal oscillation •System clock : CF oscillation •1/2 divided	4.5 - 6.0		3	9	
	IDDOP(3)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz Crystal oscillation •System clock : RC oscillation •1/2 divided	4.5 - 6.0		0.7	3.4	
	IDDOP(4)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz Crystal oscillation •System clock : Crystal oscillation •Internal RC oscillation stops. •1/2 divided	4.5 - 6.0		35	130	μA

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current dissipation HALT mode (Note 4)	IDDHALT(1)		•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz Crystal oscillation •Internal RC oscillation stops. •System clock : CF oscillation •1/1 divided	4.5 - 6.0		5	14	mA
	IDDHALT(2)		•HALT mode •FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz Crystal oscillation •Internal RC oscillation stops. •System clock : CF oscillation •1/2 divided	4.5 - 6.0		2.2	7	
	IDDHALT(3)		•HALT mode •FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz Crystal oscillation •System clock : RC oscilaltion •1/2 divided	4.5 - 6.0		400	1600	μA
	IDDHALT(4)		•HALT mode •FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz Crystal oscillation •System clock : Crystal oscilaltion •Internal RC oscillation stops. •1/2 divided	4.5 - 6.0		25	100	
Current dissipation HOLD mode (Note 4)	IDDHOLD(1)		HOLD mode	4.5 - 6.0		0.05	30	μA

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation guaranteed constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2
6MHz ceramic resonator oscillation	Murata	CSA6.00MG	33pF	33pF
		CST6.00MGW	on chip	
	Kyocera	KBR-6.0MSB	33pF	33pF
		PBRC6.00A (chip type)	33pF	33pF
		KBR-6.0MKC	on chip	
		PBRC6.00B (chip type)		
3MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33pF
		CST3.00MGW	on chip	
	Kyocera	KBR-3.0MS	33pF	33pF

* Both C1 and C2 must be a K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub clock)

Oscillation type	Maker	Oscillator	C1	C2	Rf	Rd
32.768kHz crystal oscillation	EPSON	C-002RX	18pF	18pF	10MΩ	680kΩ
	CITIZEN	CFS-308	18pF	18pF	10MΩ	330kΩ
		CFS-206				

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
•If you use other oscillators herein, we provide no guarantee for the characteristics.

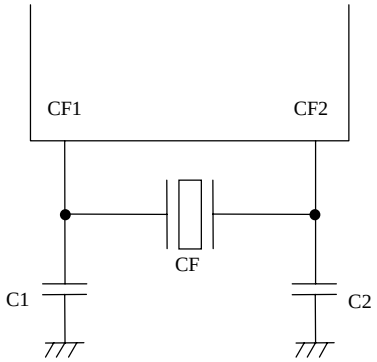


Figure 1 Ceramic oscillation circuit

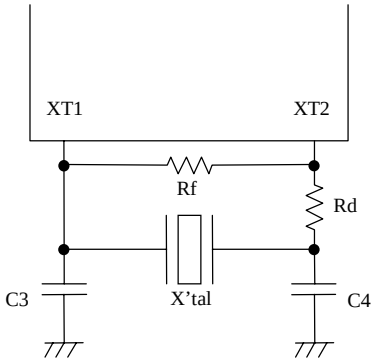
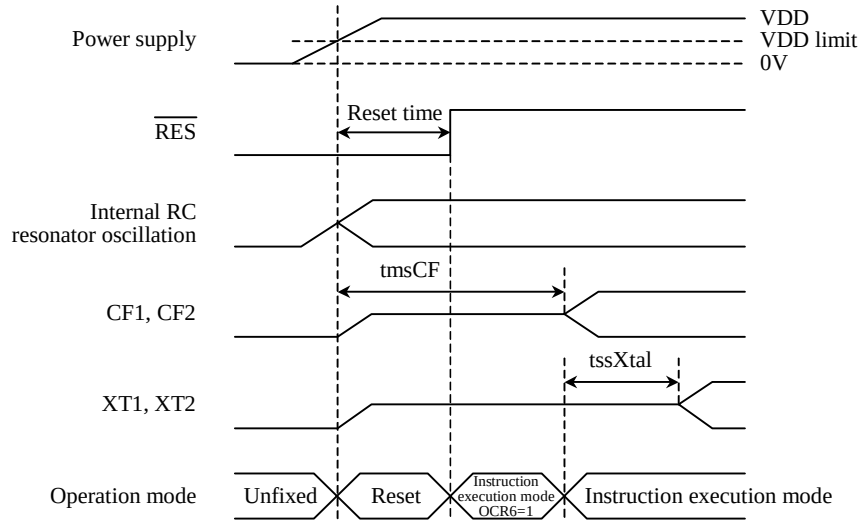
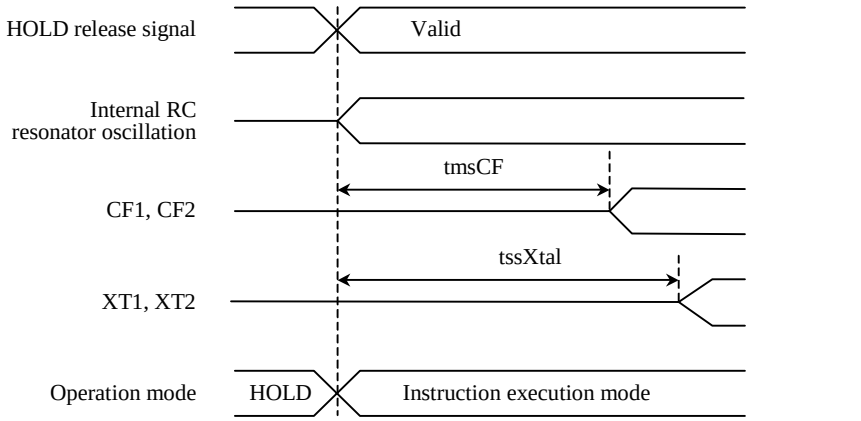


Figure 2 Crystal oscillation circuit

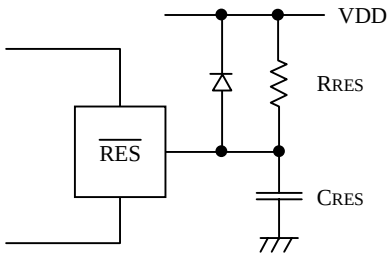


< Reset time and oscillation stabilizing time. >



< HOLD release signal and oscillation stabilizing time. >

Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

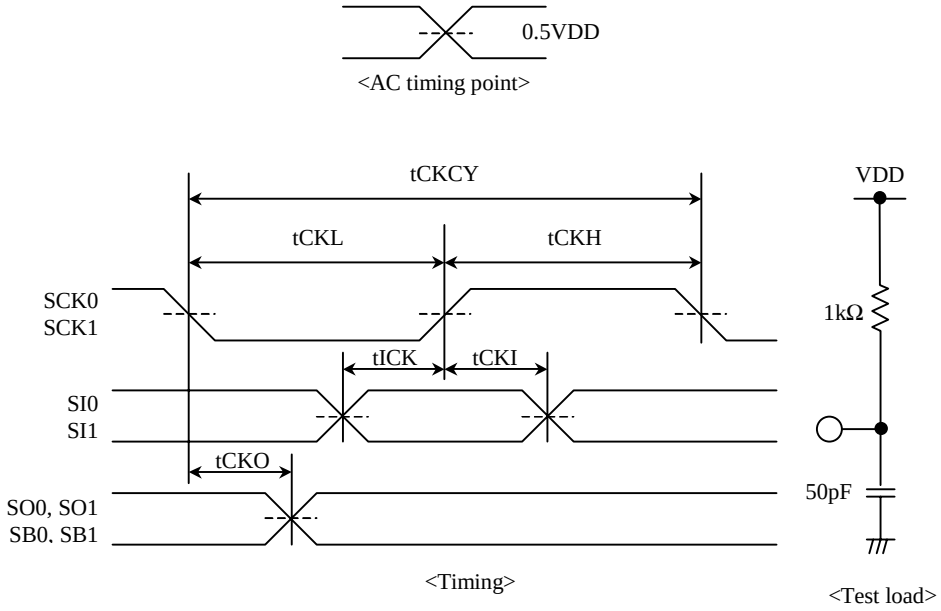


Figure 5 Serial input / output test condition

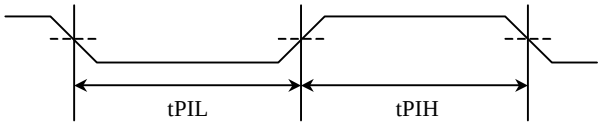


Figure 6 Pulse input timing condition