

4x RGB LEDs, E-STOP



BOARD I/O

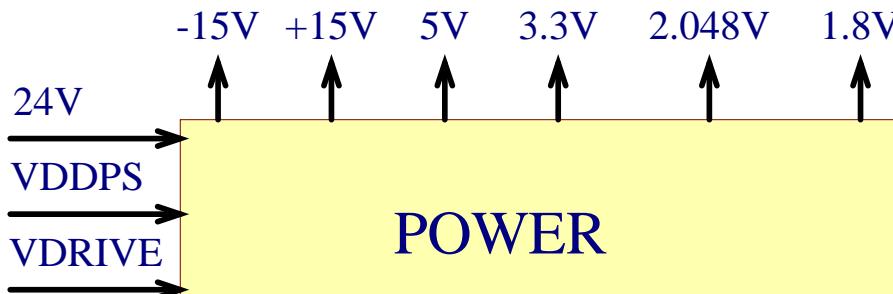
4x isoSPI
each with
interrupt I/O**isoSPI**8x channel
+/-10V diff.
pair inputs**ANALOG
INPUTS**8x full 3-phase
2-level inverters**DRIVE
OUTPUTS**2x quadrature
input (A,B,Z)**ENCODER**

PicoZed

7030

U_PicoZed

PicoZed.SchDoc

JTAG**ETHERNET****USB UART**Power inputs
to board

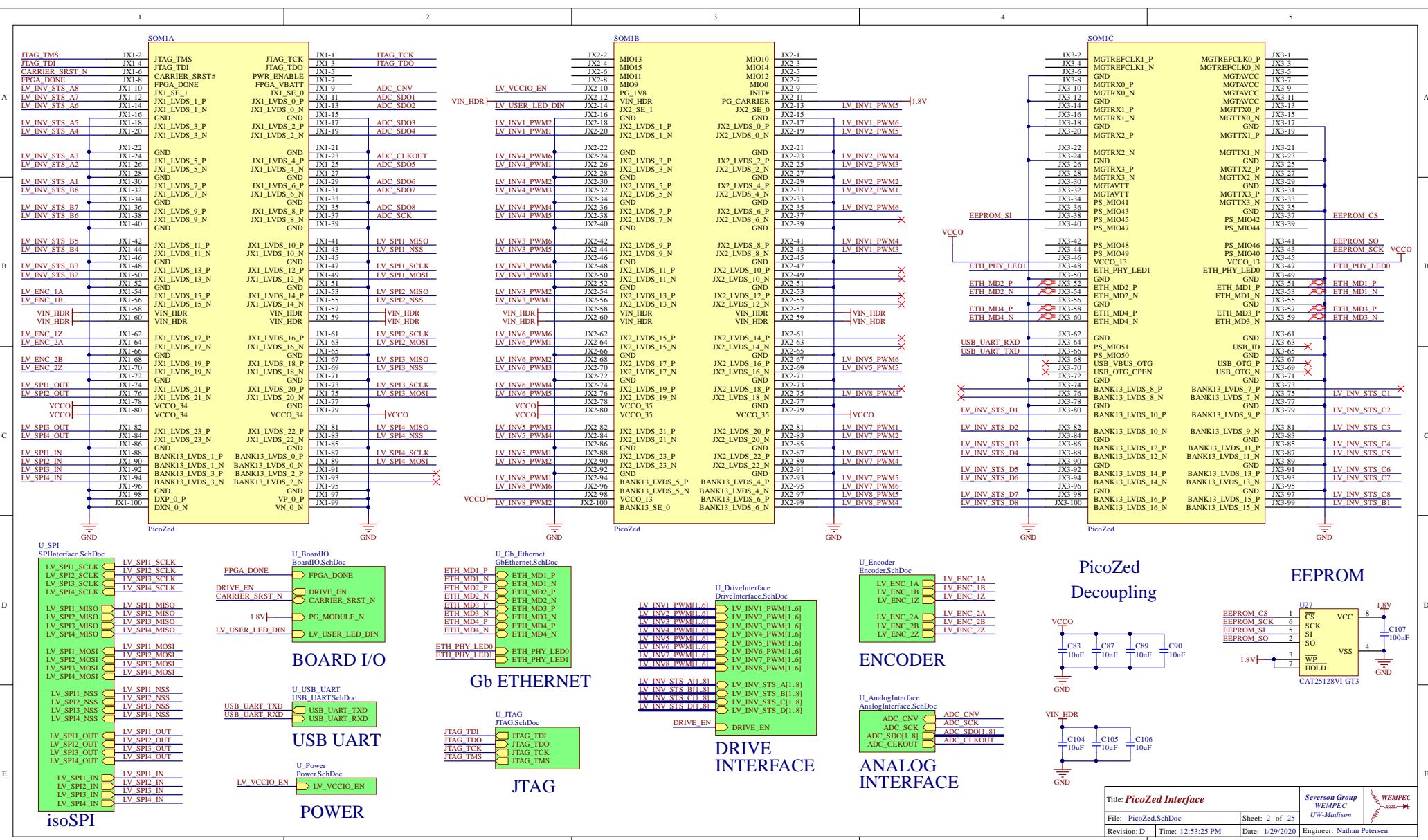
U_BackPage

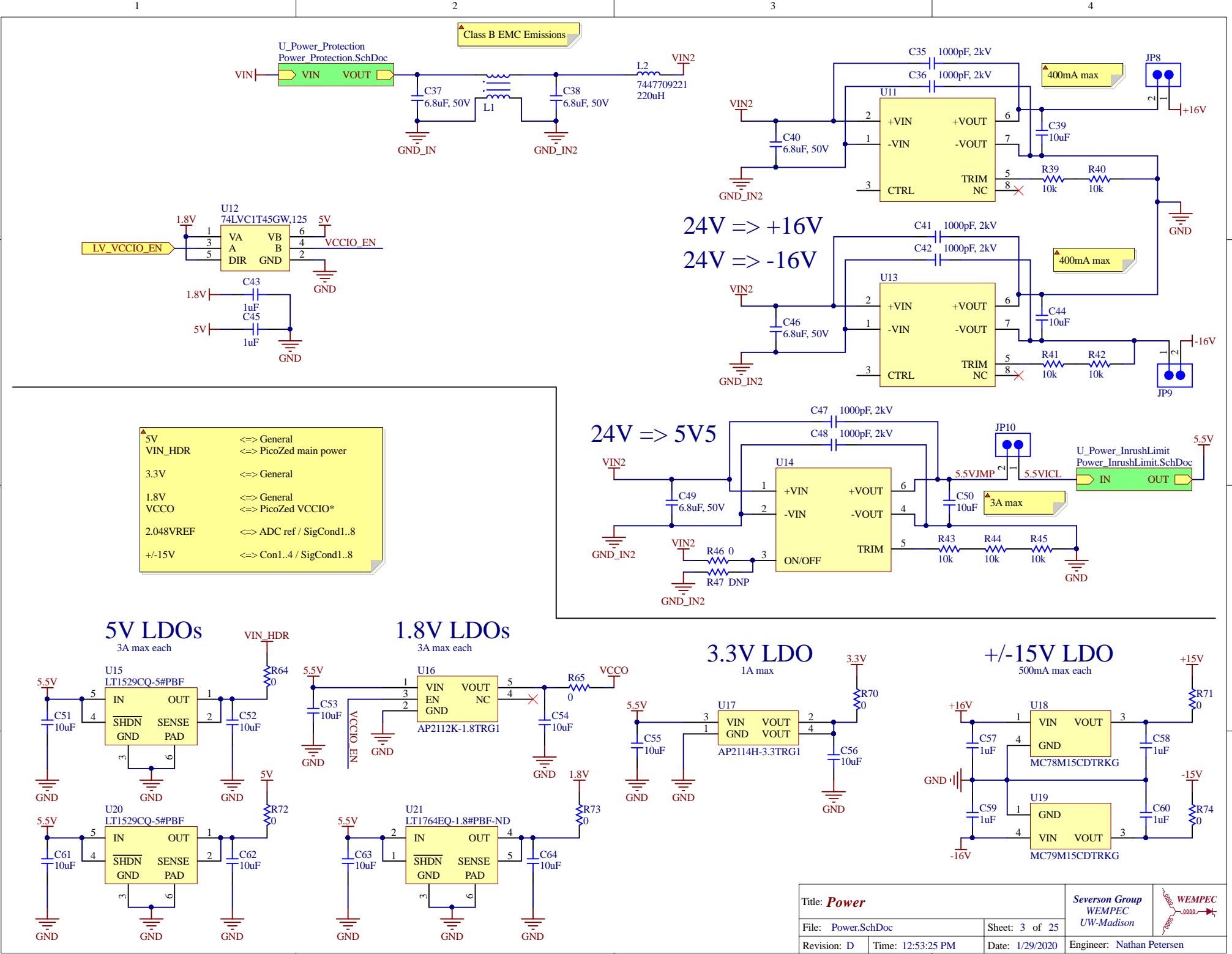
BackPage.SchDoc

U_RevisionChanges

RevisionChanges.SchDoc

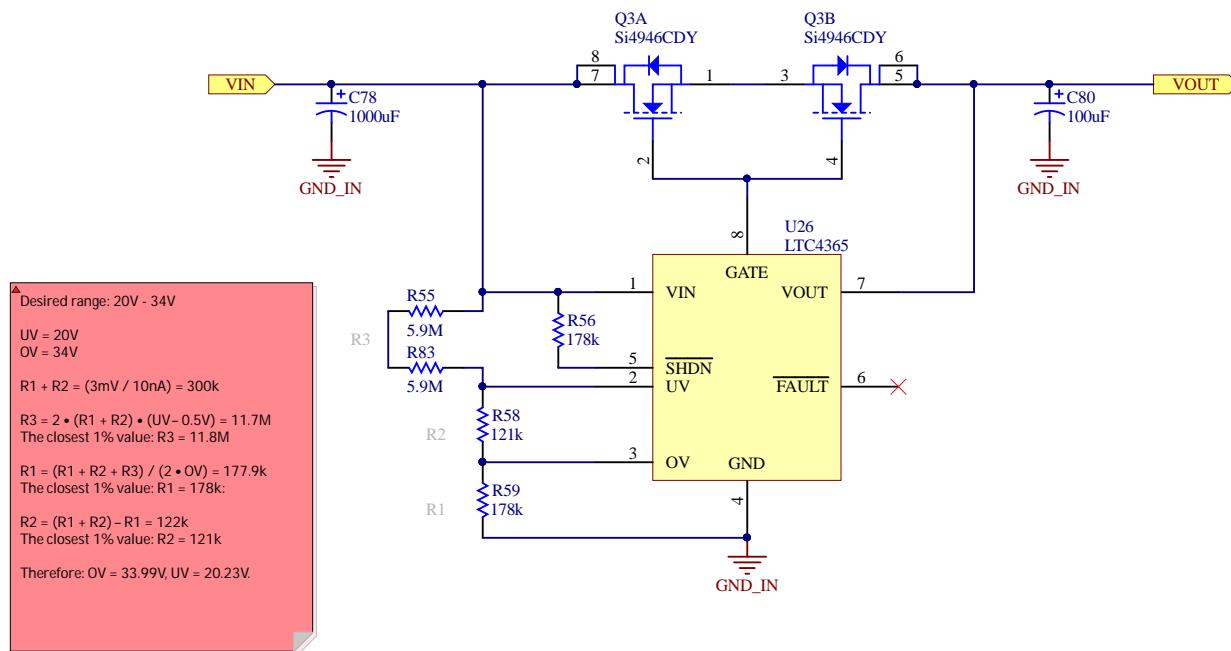
Title: **Advanced Motor Drive Controller**File: **AMDC.SchDoc** Sheet: **1 of 25**Revision: **D** Time: **12:53:25 PM** Date: **1/29/2020**
Severson Group
WEMPEC
UW-Madison
Engineer: **Nathan Petersen**





A

A



B

B

C

C

D

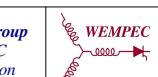
D

Title: **Power Protection**

File: Power_Protection.SchDoc

Sheet: 4 of 25

Revision: D Time: 12:53:26 PM Date: 1/29/2020

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A

A

B

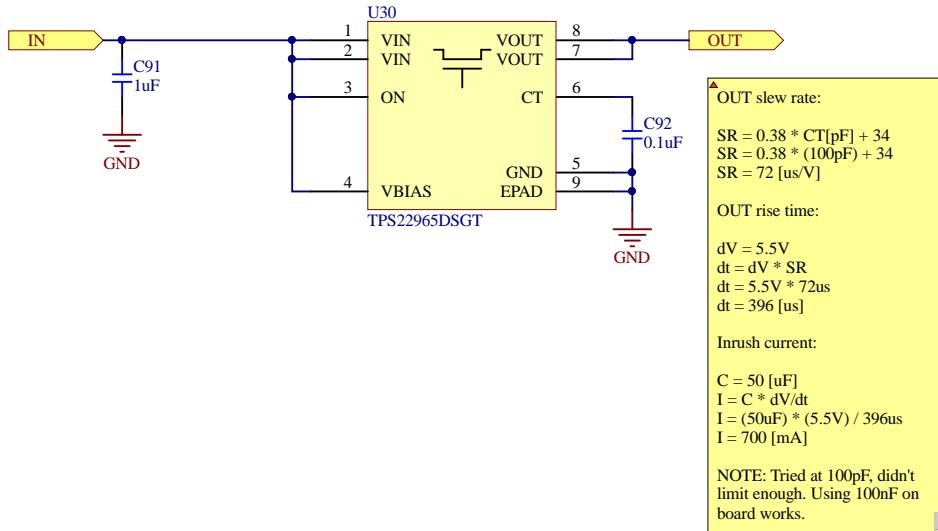
B

C

C

D

D



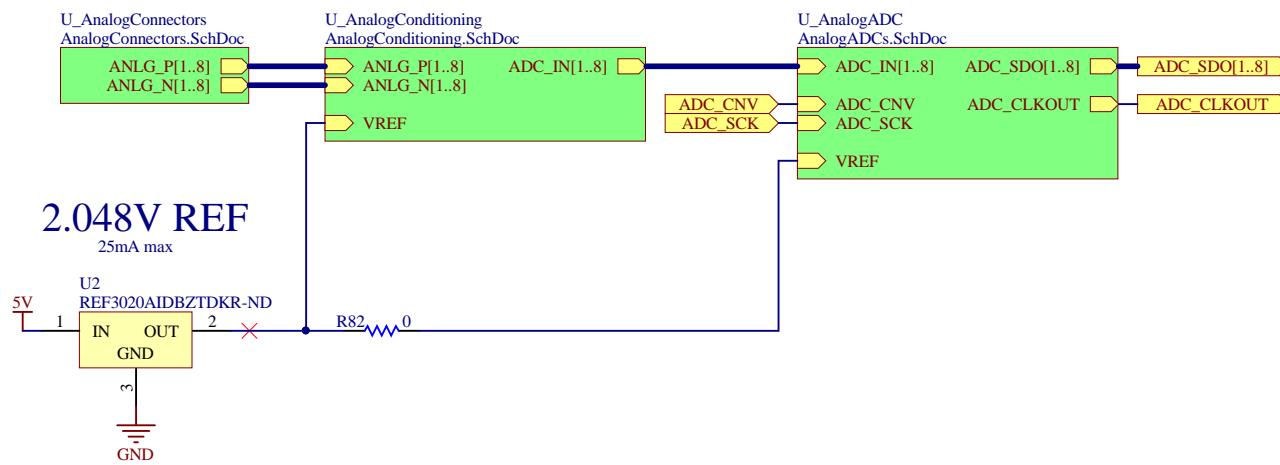
Title: Inrush Current Limiter		Severson Group WEMPEC UW-Madison
File: Power_InrushLimit.SchDoc	Sheet: 5 of 25	
Revision: D	Time: 12:53:26 PM	
Date: 1/29/2020		Engineer: Nathan Petersen

A

A

B

B



C

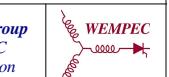
C

D

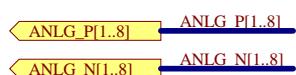
D

Title: **Analog Interface**File: **AnalogInterface.SchDoc**Sheet: **6 of 25**Revision: **D** Time: **12:53:26 PM**Date: **1/29/2020**

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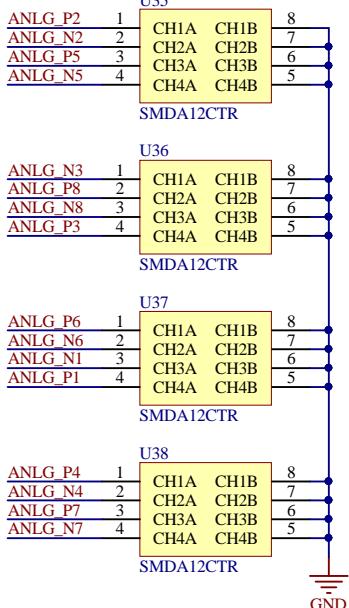
Engineer: **Nathan Petersen**

A

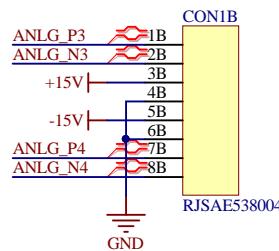
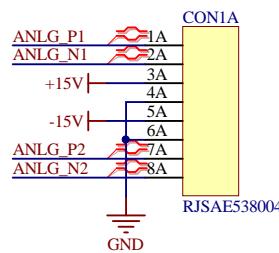


A

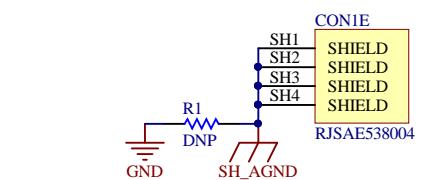
ESD Protection



B

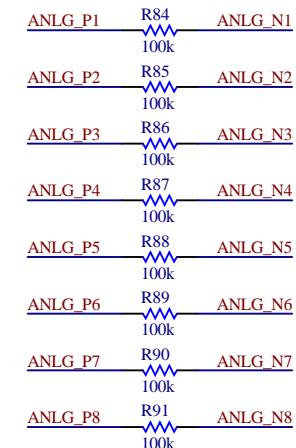


C



D

Force no input to 0V



B

C

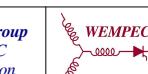
D

Title: **Analog RJ45 Connectors**

File: AnalogConnectors.SchDoc | Sheet: 7 of 25

Revision: D | Time: 12:53:26 PM | Date: 1/29/2020

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A

A

B

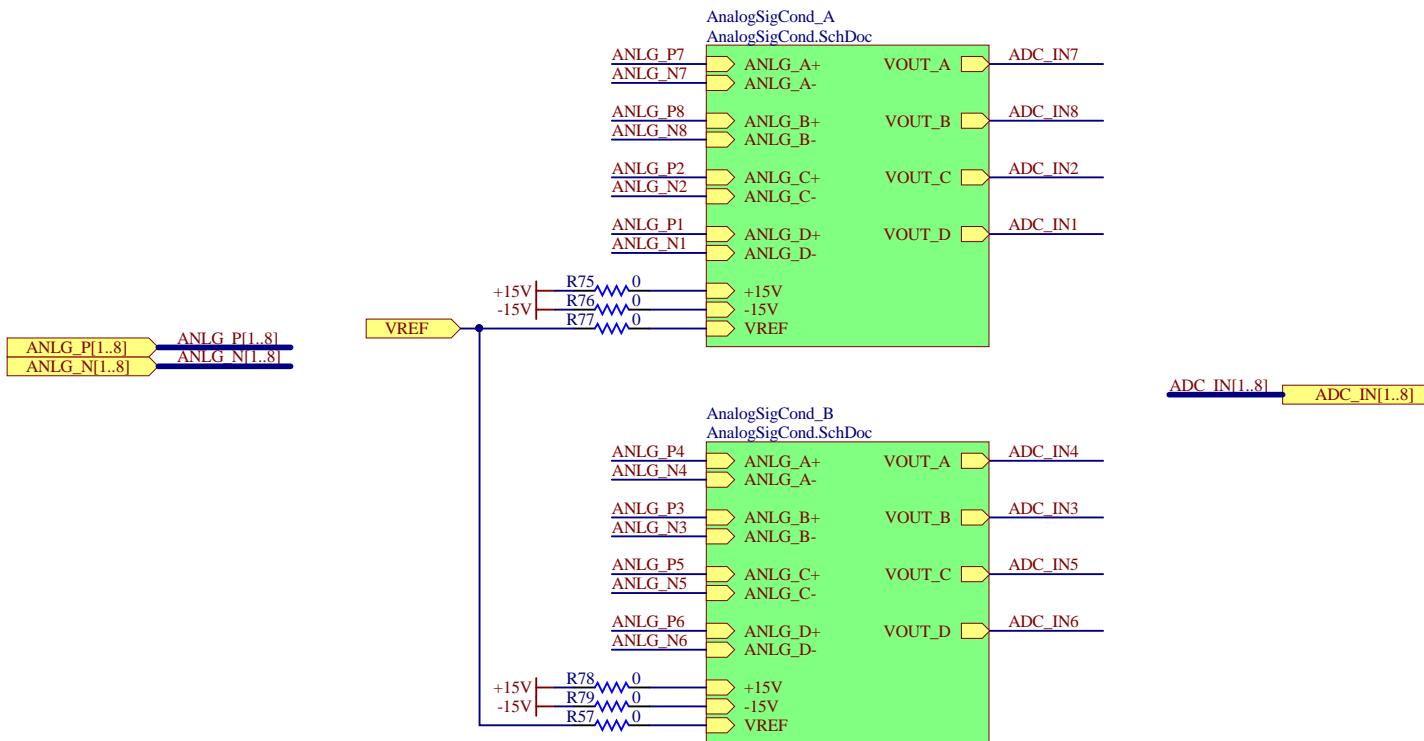
B

C

C

D

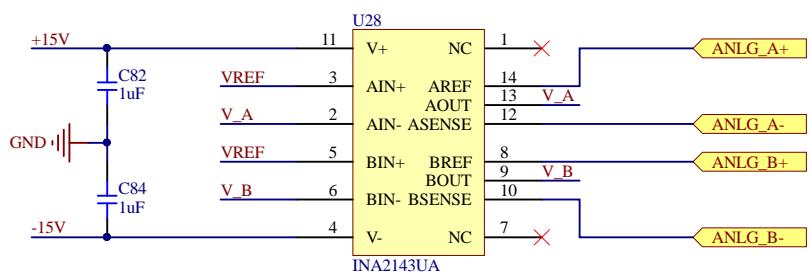
D



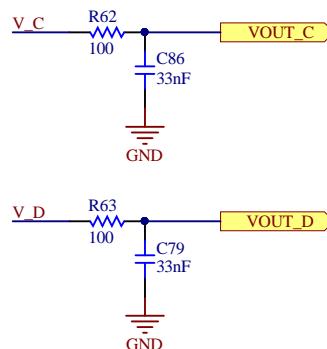
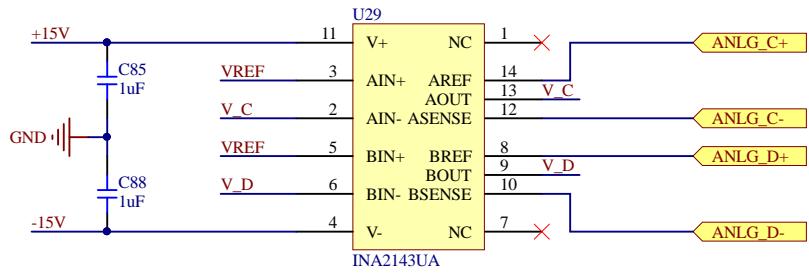
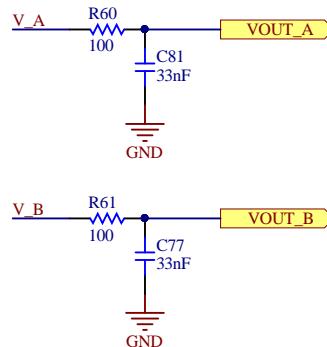
Title: Analog Signal Conditioning		Severson Group WEMPEC UW-Madison
File: AnalogConditioning.SchDoc	Sheet: 8 of 25	
Revision: D	Time: 12:53:26 PM	
Engineer: Nathan Petersen		

A

A



▲ LPF: fc = 50kHz



B

B

C

C

D

D

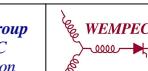
Title: **Analog Signal Front-End**

File: AnalogSigCond.SchDoc

Sheet: 9 of 25

Revision: D Time: 12:53:26 PM Date: 1/29/2020

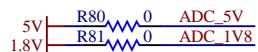
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A

10



VREF

ADC_IN[1..8] → ADC_IN[1..8]

	VREF
ADC_IN8	48
ADC_IN7	47
ADC_IN6	51
ADC_IN5	50
ADC_IN4	2
ADC_IN3	1
ADC_IN2	5
ADC_IN1	4
ADC_IN0	11
ADC_IN9	10
ADC_IN10	14
ADC_IN11	13
ADC_IN12	17
ADC_IN13	16
ADC_IN14	20
ADC_IN15	19

U1
LTC2320-14

SDO1	27	ADC_SDO1
SDO2	28	ADC_SDO2
SDO3	29	ADC_SDO3
SDO4	30	ADC_SDO4
SDO5	35	ADC_SDO5
SDO6	36	ADC_SDO6
SDO7	39	ADC_SDO7
SDO8	40	ADC_SDO8

ADC SDO[1..8]

ADC Serial Interface
Test Points

Pinout diagram for the ADC module:

- TP1: ADC_CNV
- TP2: ADC_SCK
- TP3: ADC_CLKOUT
- TP4: GND

1

3

3

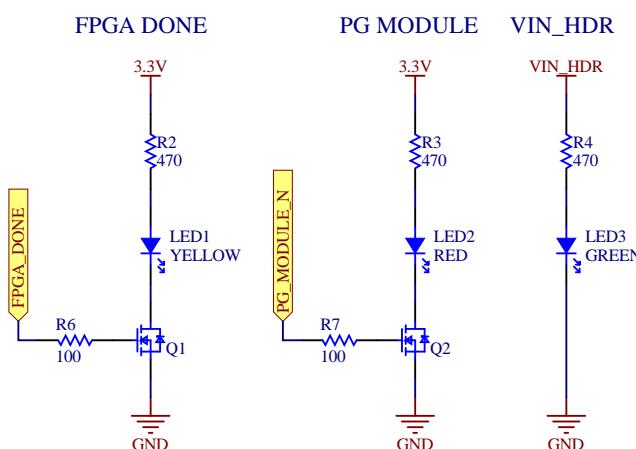
6

Title: **ADC** File: AnalogADCs.SchDoc Sheet: 10 of 25 Revision: D Time: 12:53:26 PM Date: 1/29/2020 Engineer: Nathan Petersen

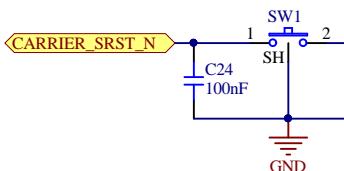
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STATUS LEDS

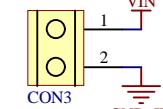


RESET BUTTON

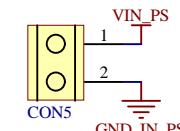


POWER CONNECTORS

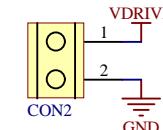
VIN (assumed 24V DC)



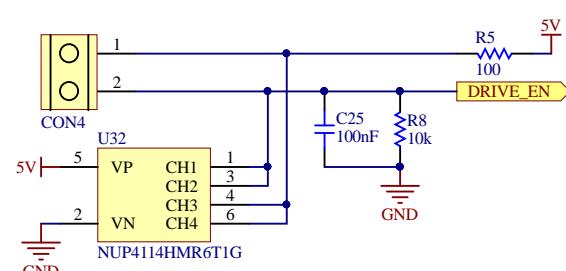
POWERSTACK VIN



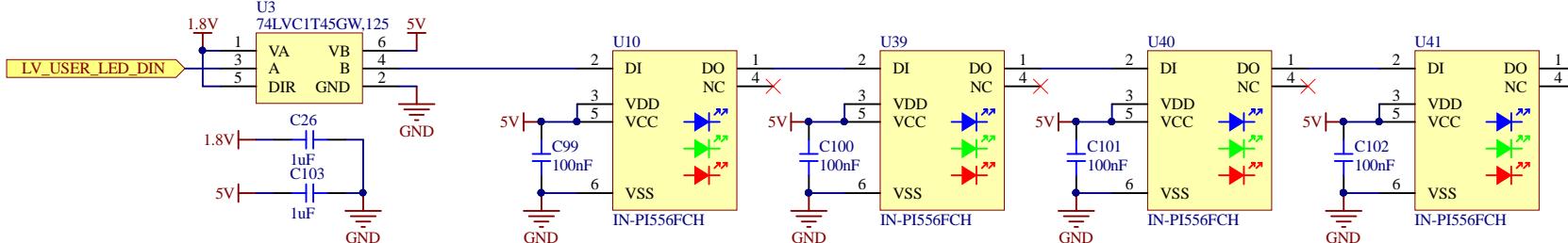
VDRIVE



DRIVE ENABLE (ESTOP)



USER RGB LEDs



Title: **Board I/O**

File: BoardIO.SchDoc

Sheet: 11 of 25

Revision: D Time: 12:53:26 PM

Date: 1/29/2020

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A

A

B

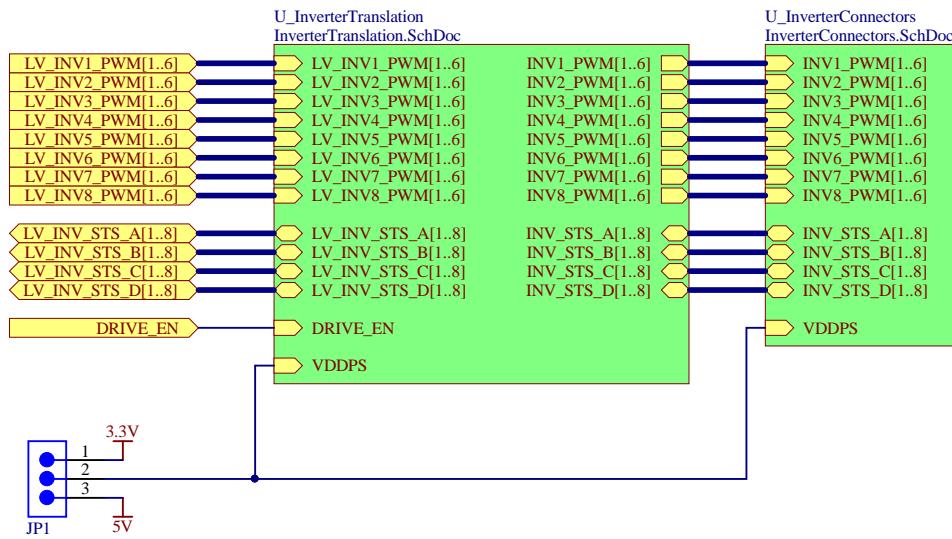
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C

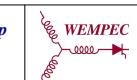
C

D

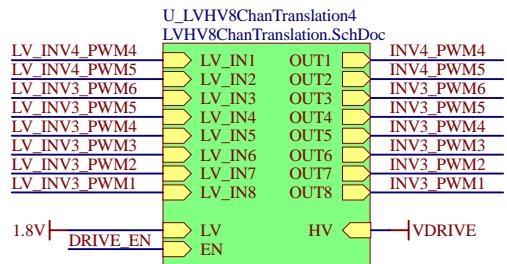
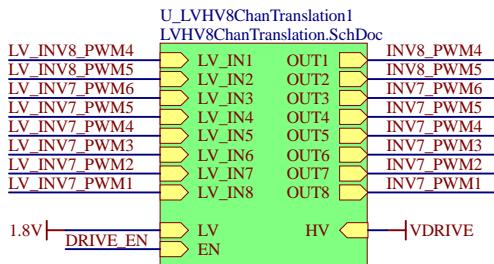
D

Title: **Drive Interface**File: **DriveInterface.SchDoc**Sheet: **12 of 25**Revision: **D** Time: **12:53:26 PM**Date: **1/29/2020** Engineer: **Nathan Petersen**

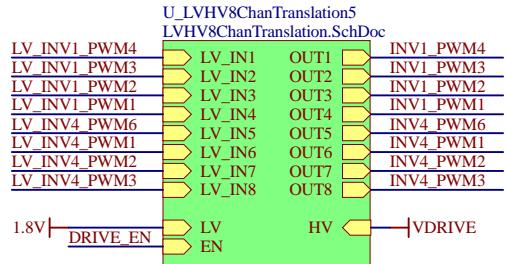
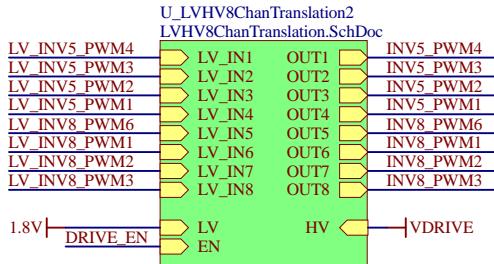
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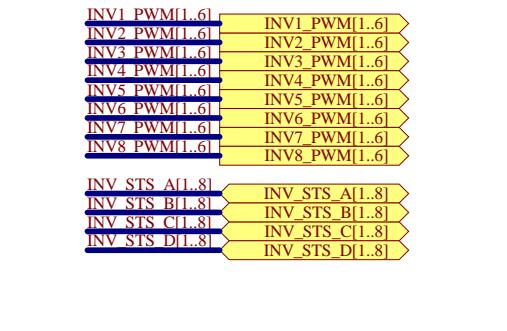
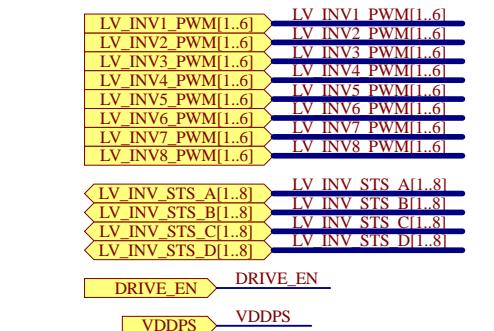
A



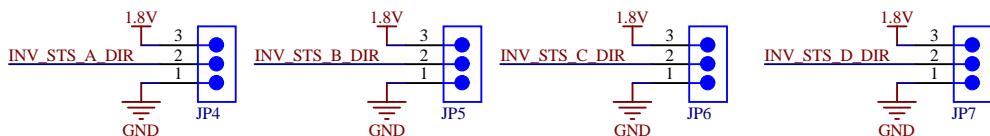
B



C



D



Title: Inverter Level Translation		Severson Group WEMPEC UW-Madison
File: InverterTranslation.SchDoc	Sheet: 13 of 25	
Revision: D	Time: 12:53:26 PM	Date: 1/29/2020
Engineer: Nathan Petersen		WEMPEC

A

A

B

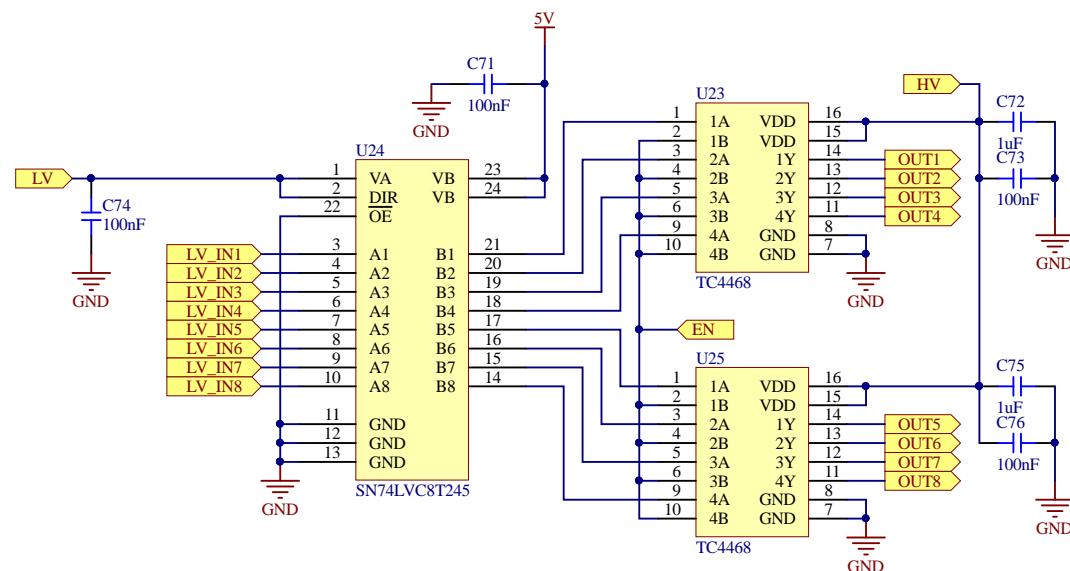
B

C

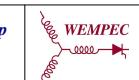
C

D

D

Title: **8-channel LV to HV Translation**File: **LVHV8ChanTranslation.SchDoc** | Sheet: 14 of 25Revision: **D** | Time: 12:53:26 PM

Date: 1/29/2020

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UW-Madison


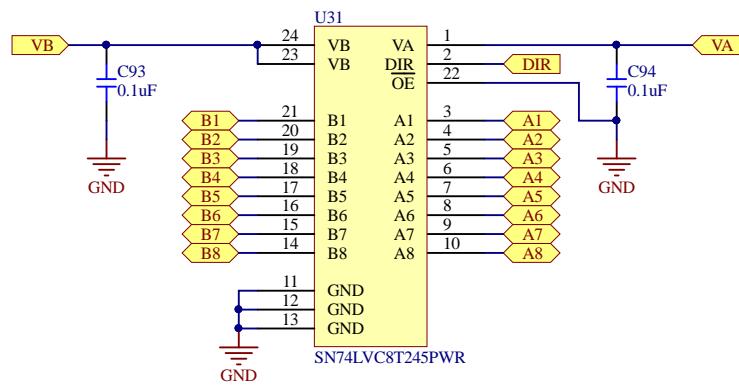
Engineer: Nathan Petersen

A

B

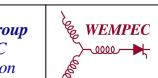
C

D

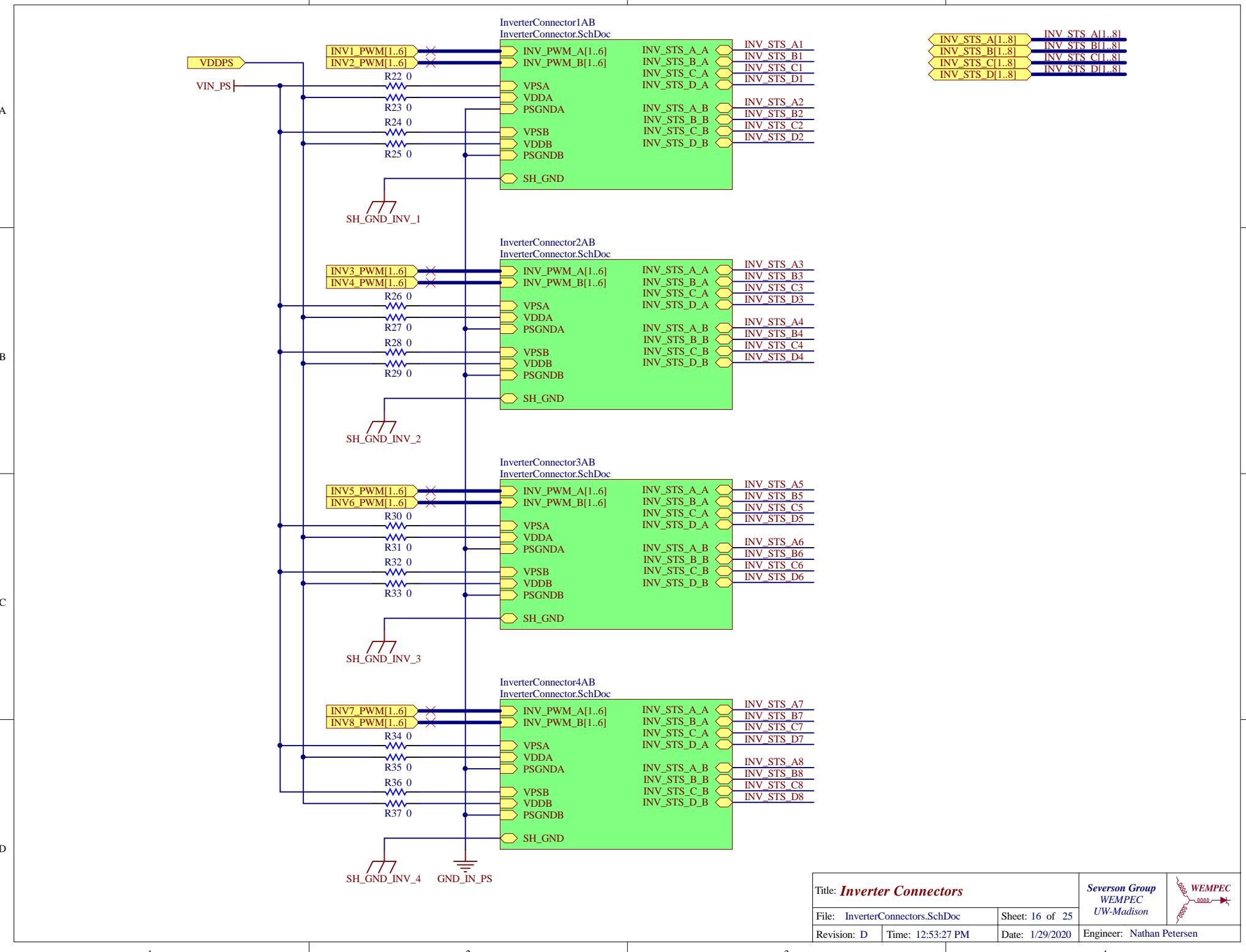
Title: **8-Channel Directional Translation**

File: TranslationDir8Chan.SchDoc Sheet: 15 of 25

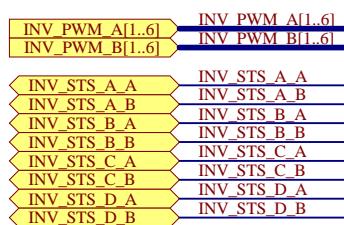
Revision: D Time: 12:53:27 PM Date: 1/29/2020

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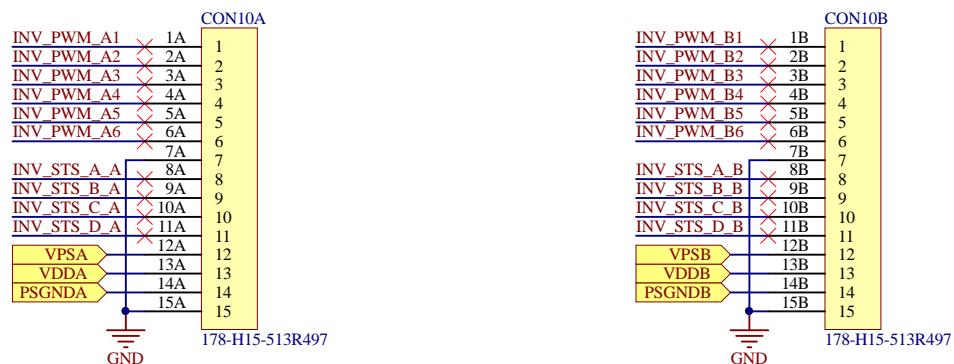
Engineer: Nathan Petersen



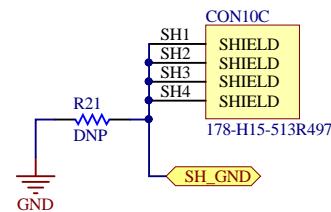
A



B



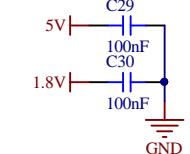
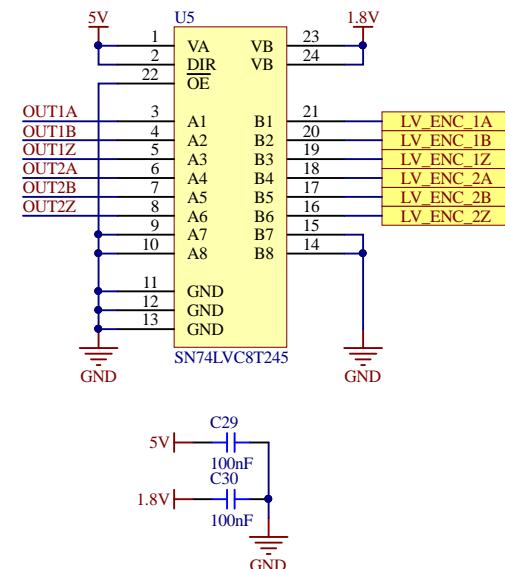
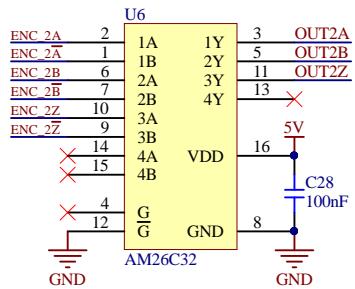
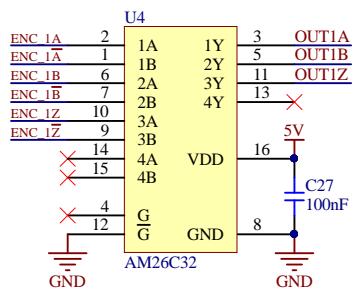
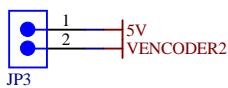
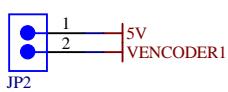
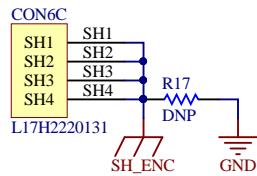
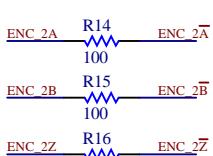
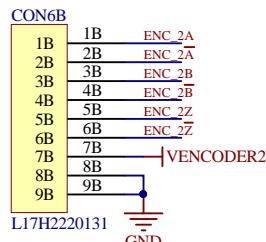
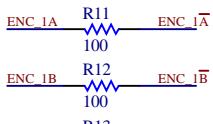
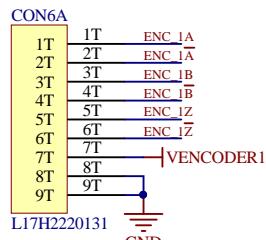
C



D

Title: Inverter Connector		Severson Group WEMPEC UW-Madison
File: InverterConnector.SchDoc	Sheet: 17 of 25	
Revision: D	Time: 12:53:27 PM	
Date: 1/29/2020		Engineer: Nathan Petersen

A

Title: **Encoders**

File: Encoder.SchDoc

Sheet: 18 of 25

Revision: D Time: 12:53:27 PM

Date: 1/29/2020

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Engineer: Nathan Petersen

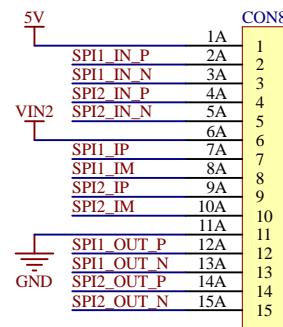
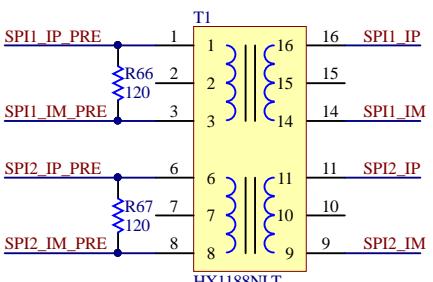
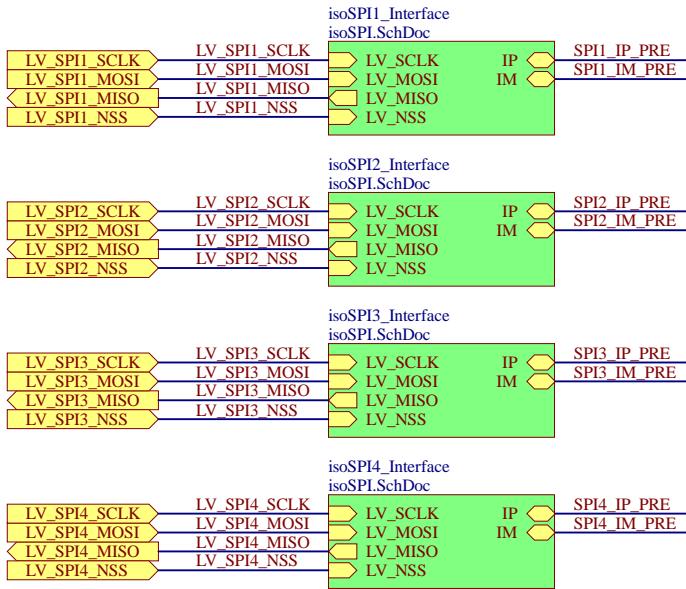
A

B

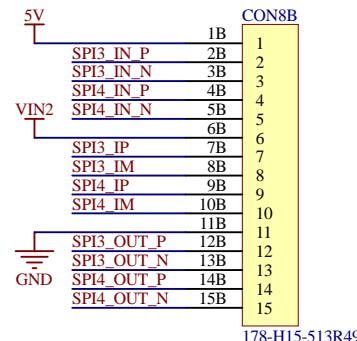
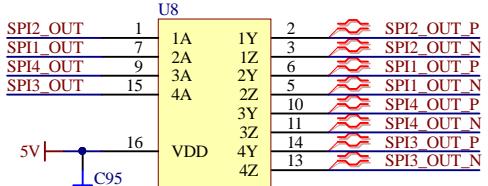
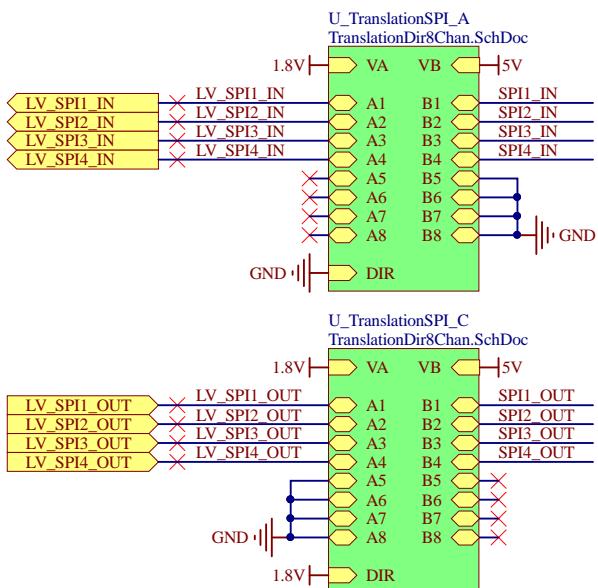
C

D

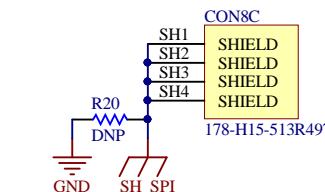
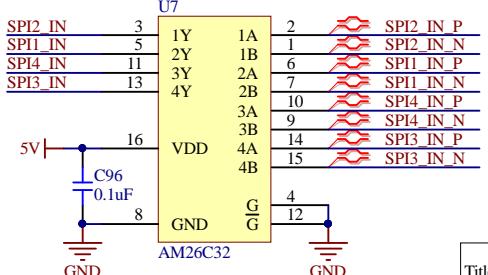
A



B



C



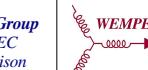
Title: SPI Interface

File: SPIInterface.SchDoc

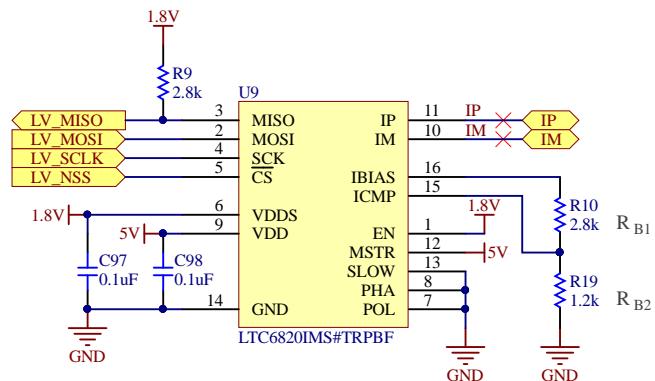
Sheet: 19 of 25

Revision: D Time: 12:53:27 PM

Date: 1/29/2020

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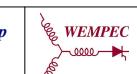


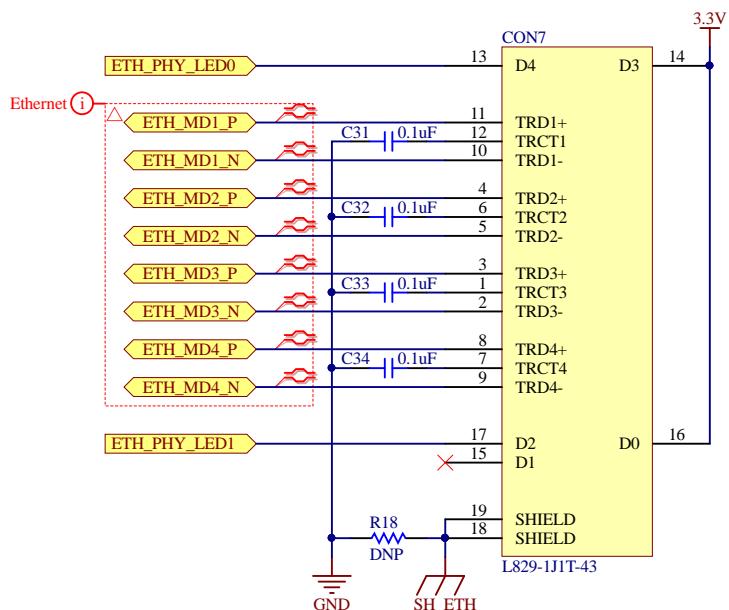
Title: *isoSPI Interface*

File: isoSPI.SchDoc Sheet: 20 of 25

Revision: D Time: 12:53:27 PM Date: 1/29/2020 Engineer: Nathan Petersen

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A

A

B

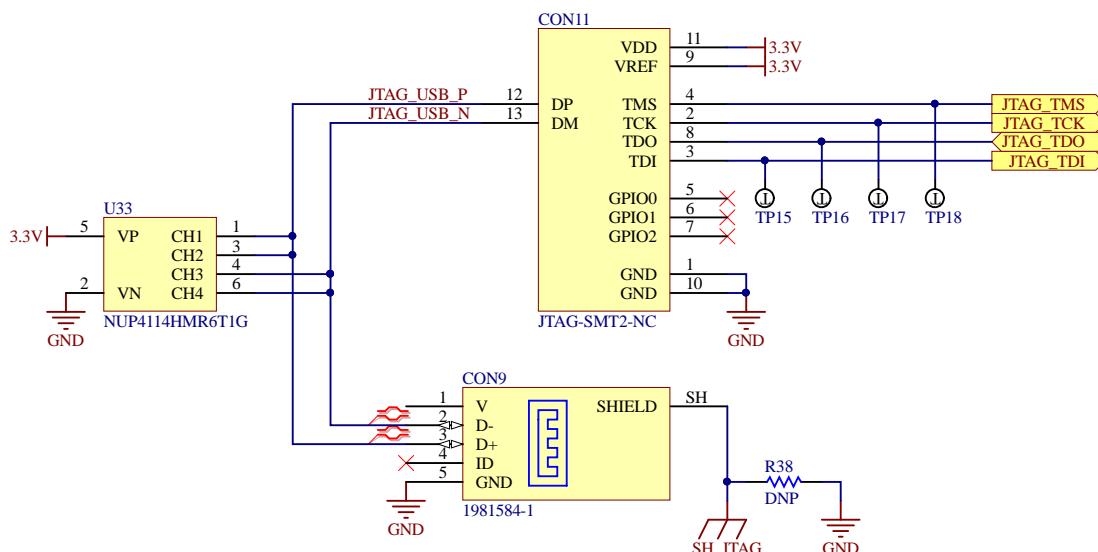
B

C

C

D

D

Title: **JTAG**File: **JTAG.SchDoc**Sheet: **22 of 25**Revision: **D** Time: **12:53:27 PM**Date: **1/29/2020**

Severson Group
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Engineer: **Nathan Petersen**

A

A

B

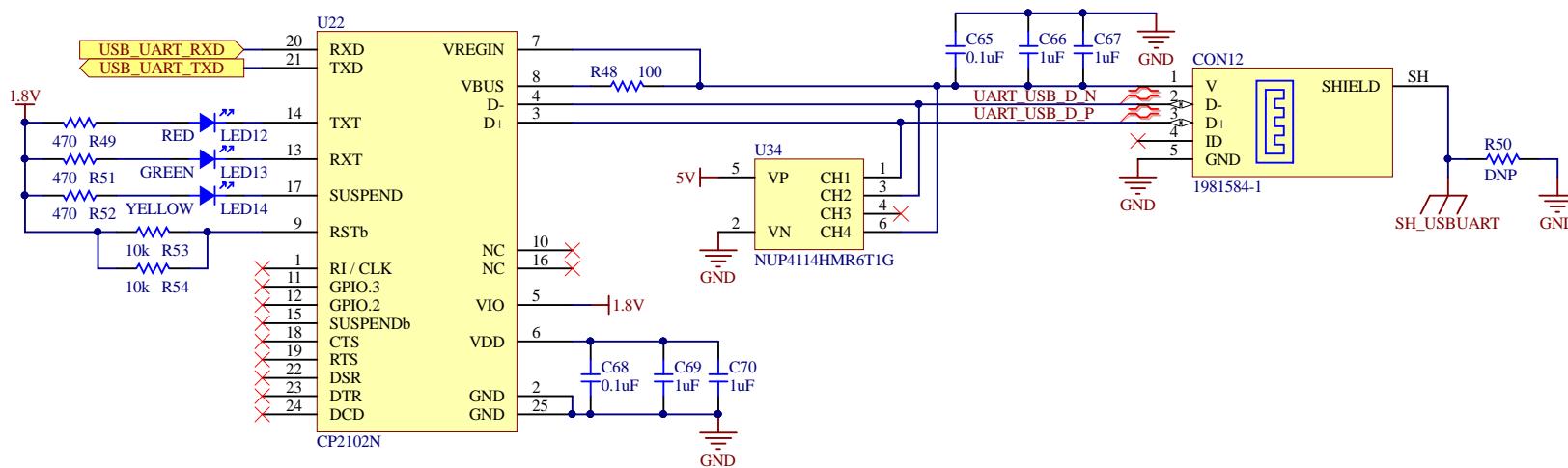
B

C

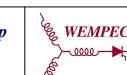
C

D

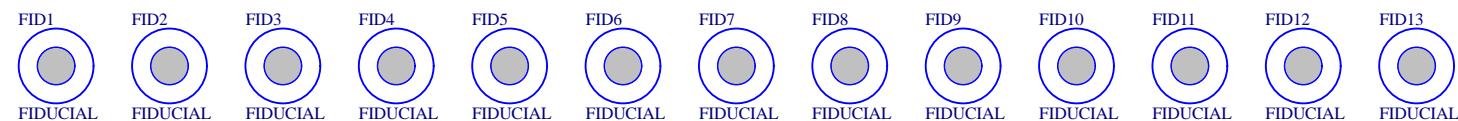
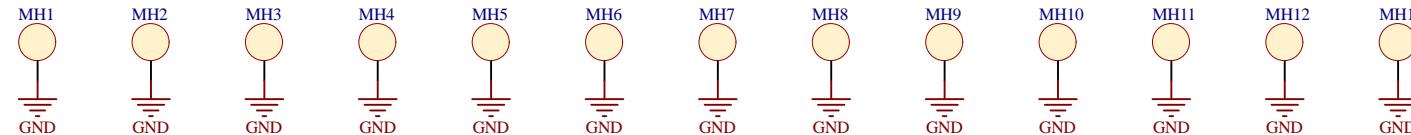
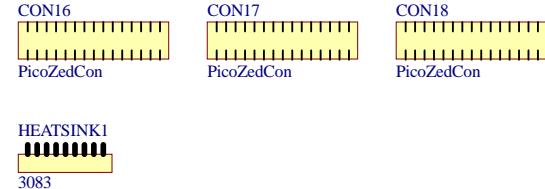
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Title: **USB UART**File: **USB_UART.SchDoc**Sheet: **23 of 25**Revision: **D** Time: **12:53:27 PM**Date: **1/29/2020**

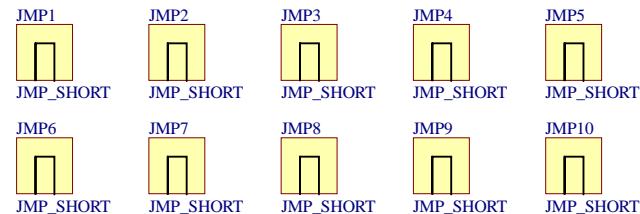
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WEMPEC
UW-Madison

Engineer: **Nathan Petersen**

A

Fiducials:**4-40 Screws:****4-40 Standoffs:****Mouting Holes:****PicoZed hardware:****Jumpers:**

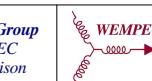
Silkscreen marked with default locations

Title: ***Back Page***File: *BackPage.SchDoc*

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Date: 1/29/2020

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Engineer: Nathan Petersen

A

A

REV A: design finalized 2018-05-25

- Initial design

REV B: design finalized 2018-07-17

- Add power input protection
- Add test points
- Add TVS to analog inputs
- Change power input DC/DC modules
- Fix BOM with correct part numbers
- Fix footprints

REV C: design finalized 2018-11-21

- Add inrush current limiting to 5V5 rail
- Add more silkscreen labels
- Add test points
- Change ADC reference from 2.5V to 2.048V
- Change trim resistors for +/-16V DC/DCs
- Swap UART Tx / Rx pins
- Separate power stack shields between connectors
- Fix footprints

REV D: design finalized 2020-01-29

- New PCB form factor (6" x 6.75", 6 layers)
- Add power stack supply rail distribution
- Add isoSPI ports
- Add extra encoder port
- Add 0R resistors to subsection power for debugging
- Add 100k resistors across analog inputs
- Add serially addressable RGB LEDs
- Add EEPROM
- Add fiducials to layout
- Remove user button / switch
- Remove discrete RGB LED
- Remove ADC2, now just one ADC
- Remove unity gain op-amp driving ADC inputs
- Reduce bulk input
- Reduce 24V power filter component current ratings
- Reduce 3V3 LDO current rating
- Change level-shifter IC for UART signals
- Change JTAG to NC module
- Change JTAG pin headers to pads
- Change values for inrush limiting circuitry
- Change FPGA driven MOSFETs to lower V_{th}
- Change FPGA pin-out mapping
- Change power stack connector I/O
- Change encoder input signal chain
- Change Ethernet routing to correct diff. impedance
- Fix footprints

B

B

C

C

D

D

Title: **Revision Changes**

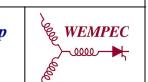
File: RevisionChanges.SchDoc

Sheet: 25 of 25

Revision: D Time: 12:53:28 PM

Date: 1/29/2020

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Engineer: Nathan Petersen