

RGB LED, 8 R/G LEDs, E-STOP



## BOARD I/O

24 channels  
5V/3.3V  
I/O

### GPIO

8 channels  
+/-10V diff.  
pair inputs

### ANALOG INPUTS

8 full 3-phase  
2-level inverters

### DRIVE OUTPUTS

Quadrature  
input (A,B,Z)

### ENCODER

# PicoZed

7030

U\_PicoZed  
PicoZed.SchDoc  
U\_BackPage  
BackPage.SchDoc

### JTAG



### ETHERNET



### USB UART

Power inputs  
to board

24V  
VDRIVE

## POWER

-15V +15V 5V 3.3V 2.048V 1.8V

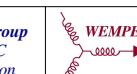
VDRIVE

Title: Advanced Motor Drive Controller

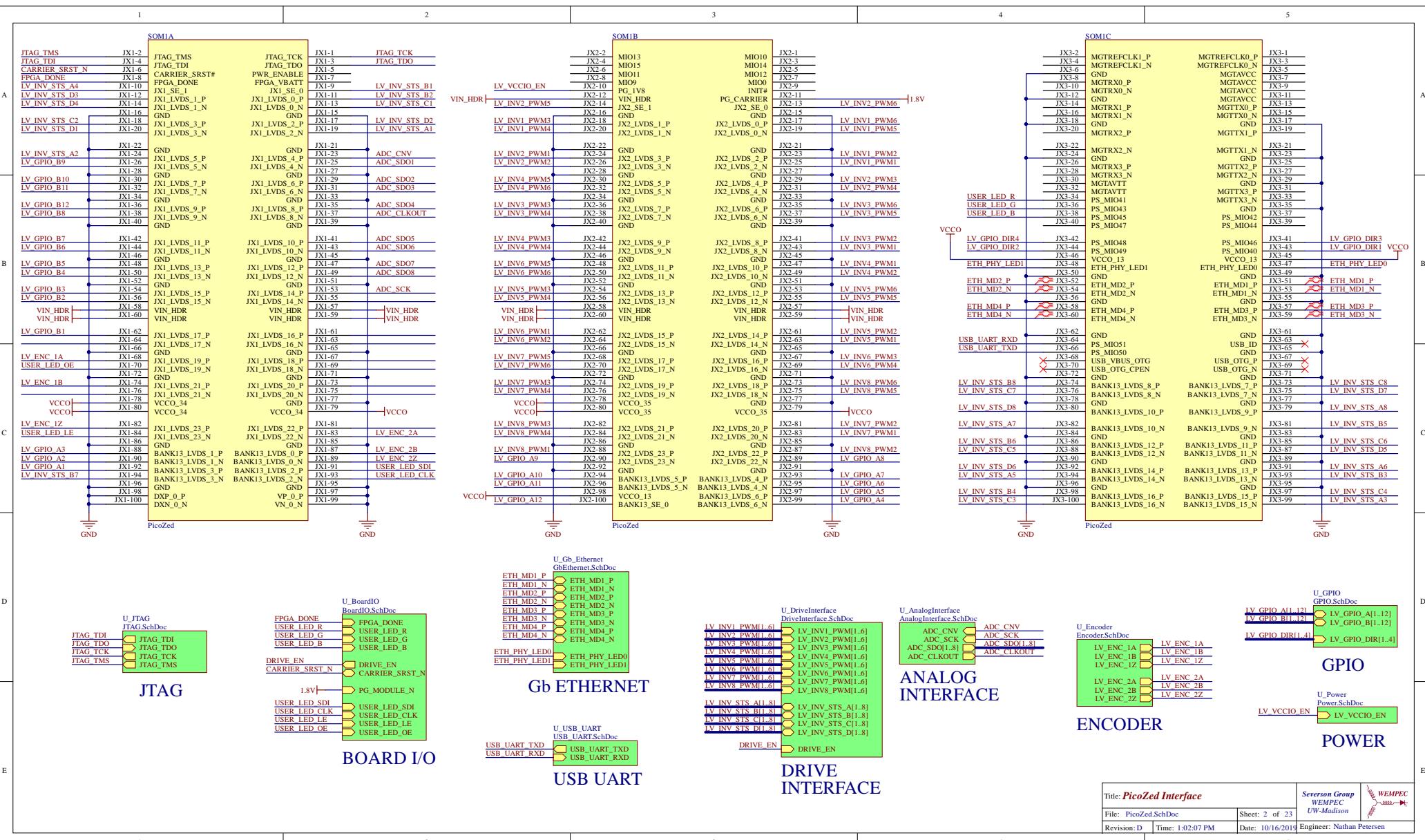
File: AMDC.SchDoc Sheet: 1 of 23

Revision: D Time: 1:02:06 PM Date: 10/16/2019

Severson Group  
WEMPEC  
UW-Madison



Engineer: Nathan Petersen



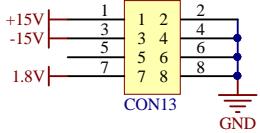
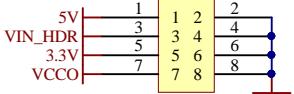
1

2

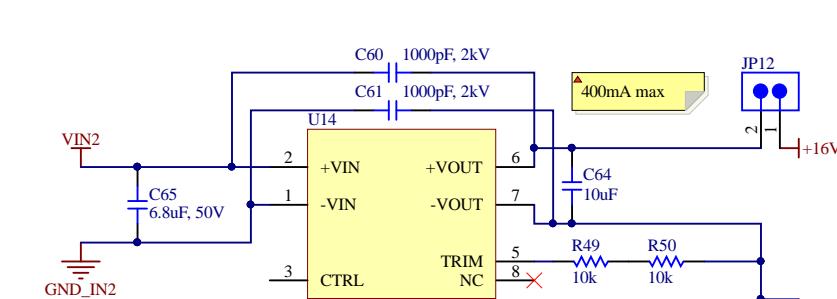
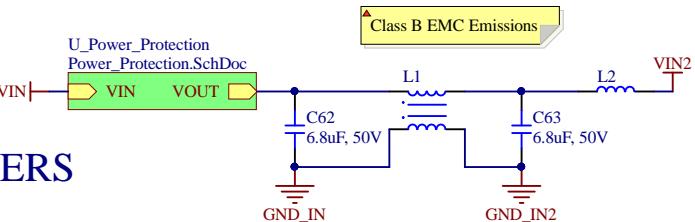
3

4

## VOLTAGE HEADERS

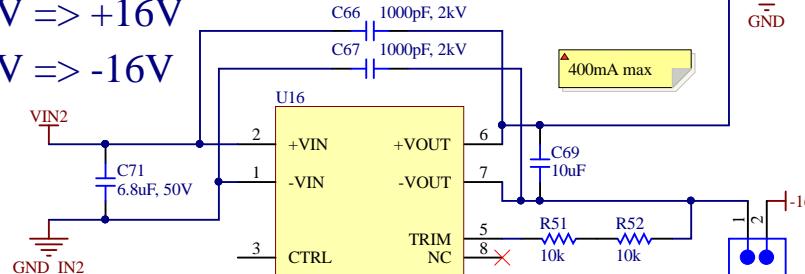


5V VIN_HDR	<=> General <=> PicoZed main power
3.3V	<=> General
1.8V VCCO	<=> General <=> PicoZed VCCIO*
2.048VREF	<=> ADC ref / SigCond1..8
+/-15V	<=> Con1..4 / SigCond1..8

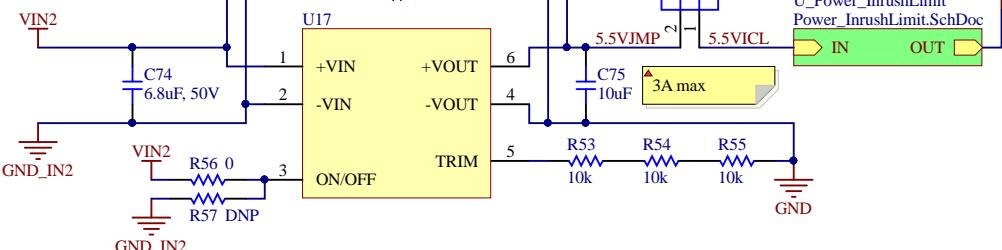


24V => +16V

24V => -16V

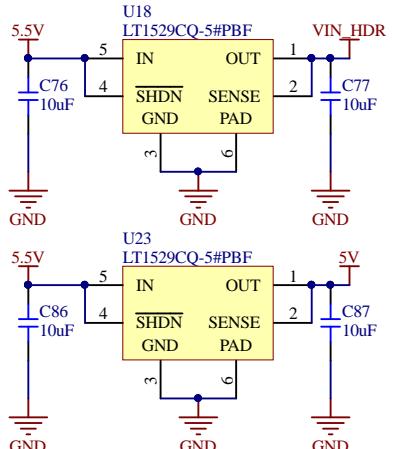


24V => 5V5



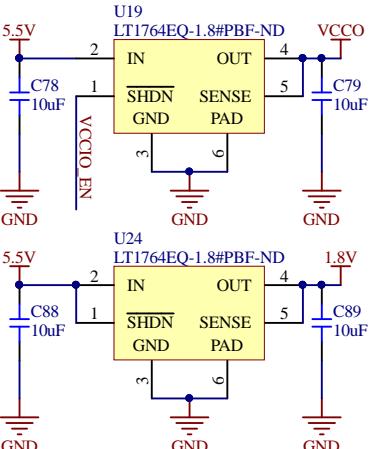
## 5V LDOs

3A max each



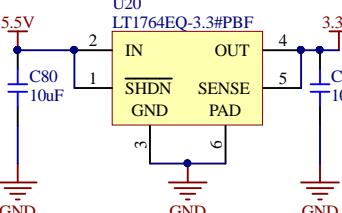
## 1.8V LDOs

3A max each



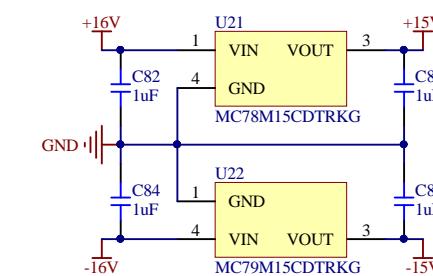
## 3.3V LDO

3A max each



## +/-15V LDO

500mA max each



Title: **Power**

File: Power.SchDoc

Revision: D Time: 1:02:08 PM

Sheet: 3 of 23 Date: 10/16/2019

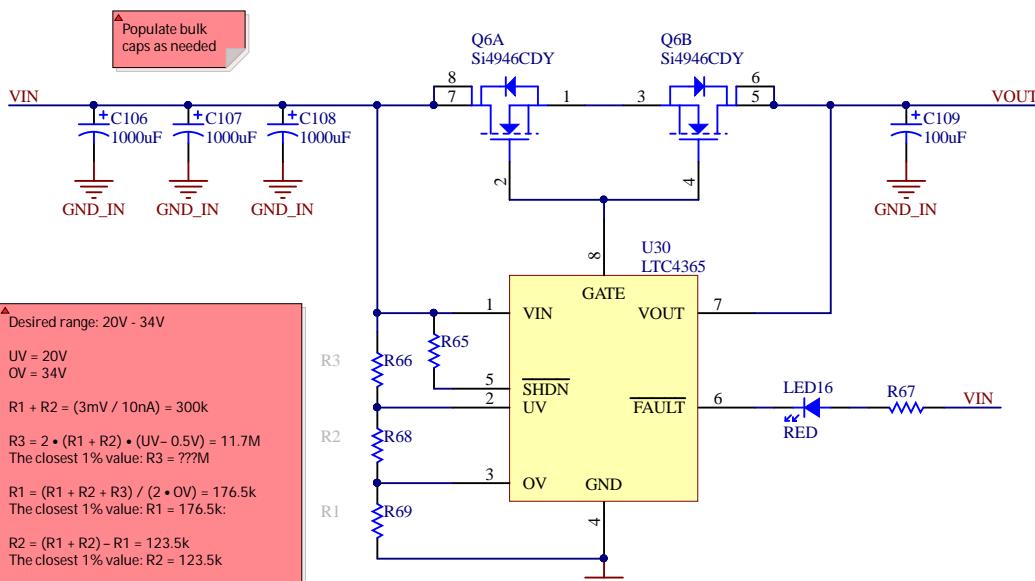
Severson Group  
WEMPEC  
UW-Madison

WEMPEC

Engineer: Nathan Petersen

A

VIN → VIN      VOUT → VOUT



B

A

B

C

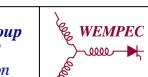
C

D

D

Title: **Power Protection**File: **Power\_Protection.SchDoc**Revision: **D** Time: **1:02:08 PM**Sheet: **4 of 23**Date: **10/16/2019**

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**WEMPEC**  
**UW-Madison**

Engineer: **Nathan Petersen**

A

A

B

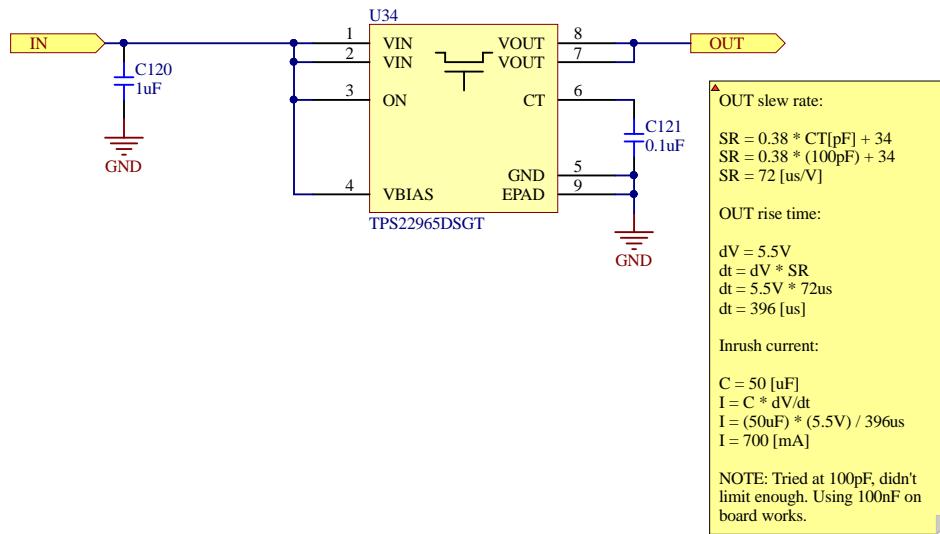
B

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C

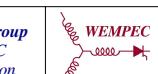
D

D

Title: **Inrush Current Limiter**

File: Power\_InrushLimit.SchDoc | Sheet: 5 of 23

Revision: D | Time: 1:02:08 PM | Date: 10/16/2019

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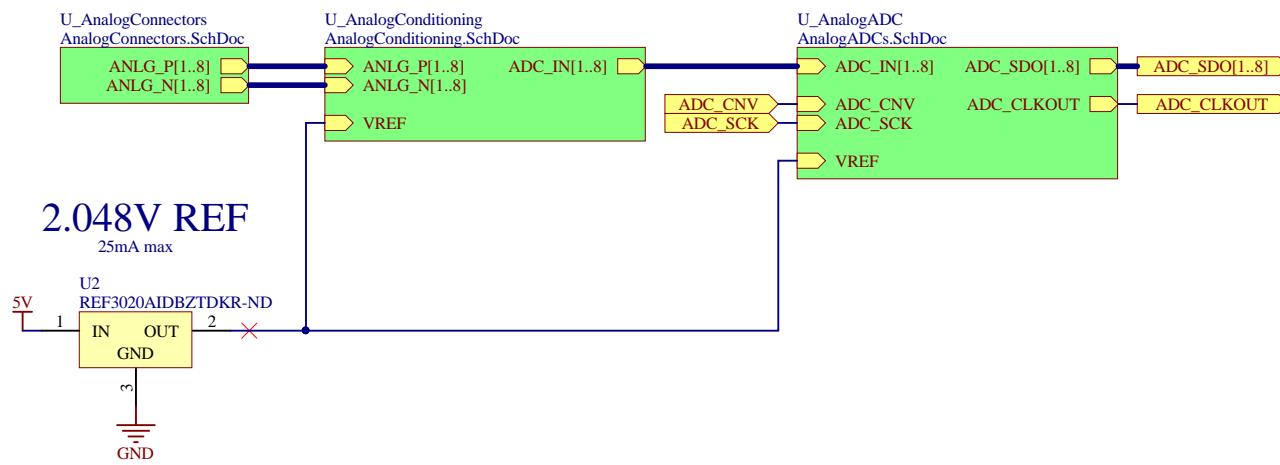
Engineer: Nathan Petersen

A

A

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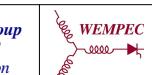


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C

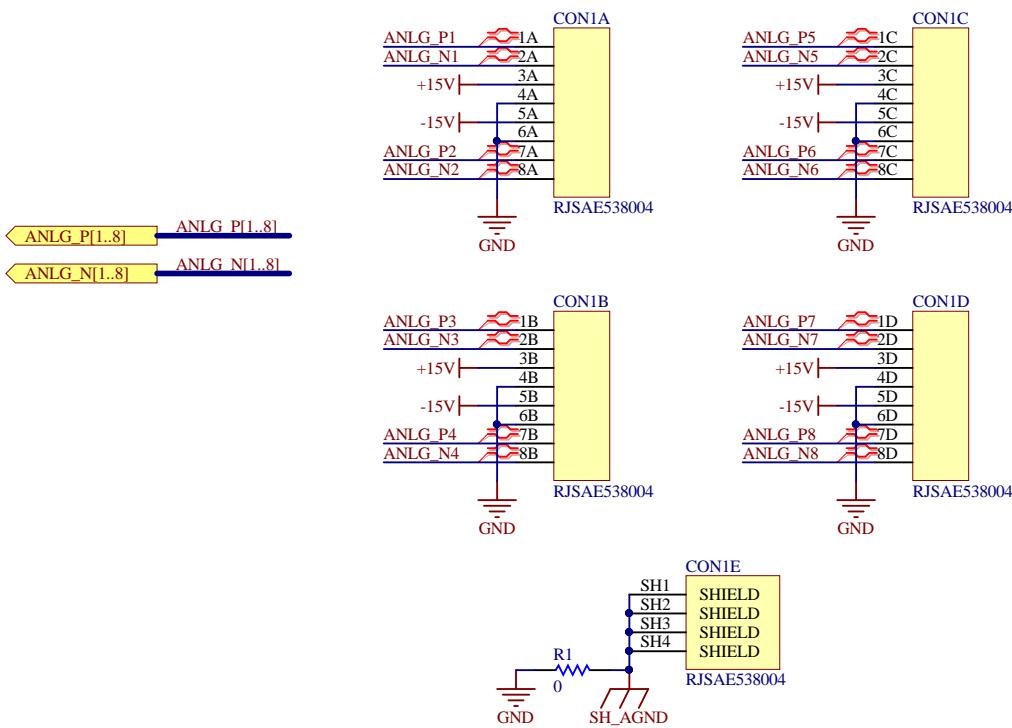
D

D

Title: **Analog Interface**File: **AnalogInterface.SchDoc**Sheet: **6 of 23**Revision: **D** Time: **1:02:08 PM**Date: **10/16/2019** Engineer: **Nathan Petersen****Severson Group**  
**WEMPEC**  
**UW-Madison**

A

A



B

B

ANLG\_P[1..8] — ANLG\_P[1..8]  
 ANLG\_N[1..8] — ANLG\_N[1..8]

C

C

D

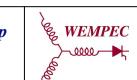
D

Title: *Analog RJ45 Connectors*

File: AnalogConnectors.SchDoc | Sheet: 7 of 23

Revision: D | Time: 1:02:08 PM

Date: 10/16/2019

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A

A

B

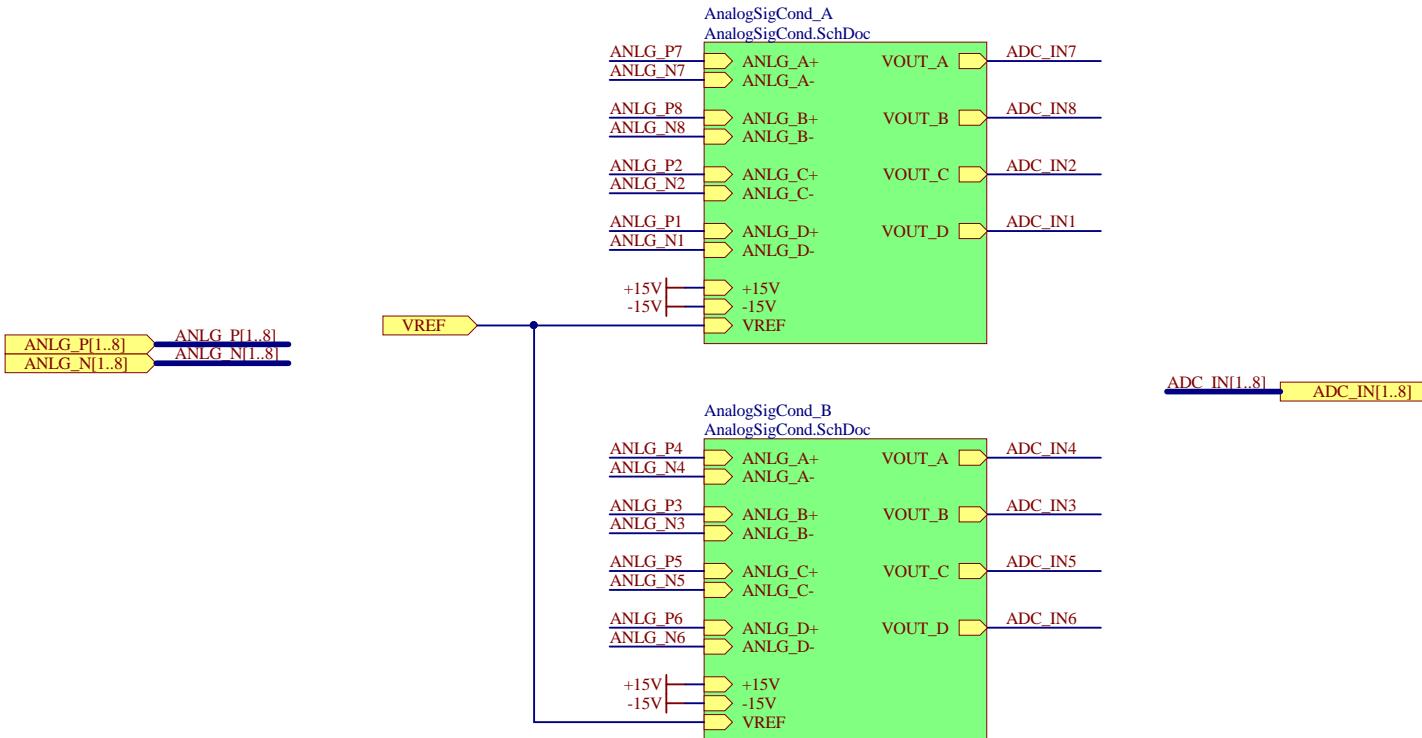
B

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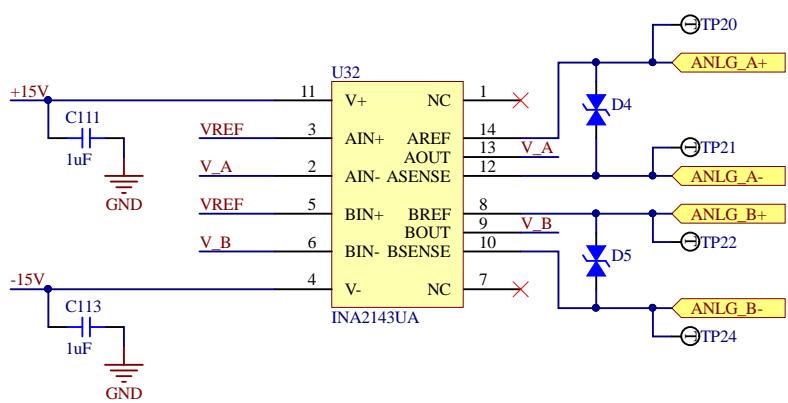
C

D

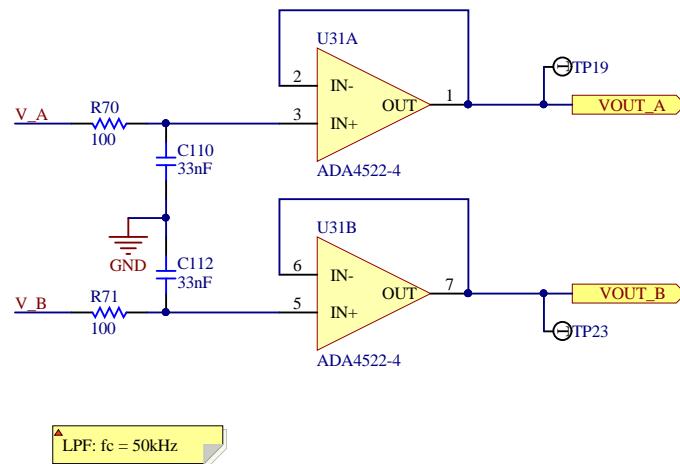
D



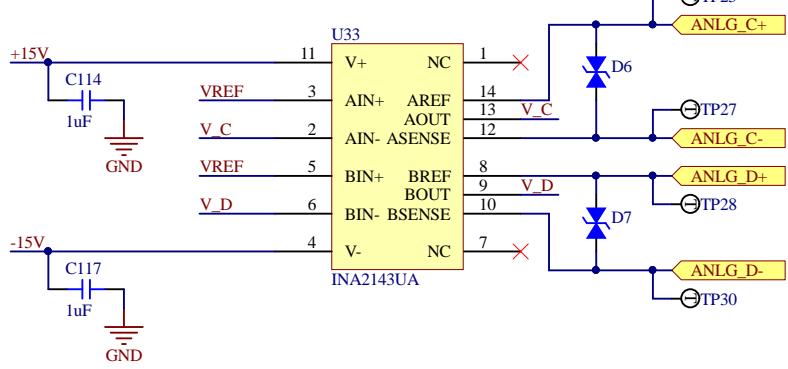
A



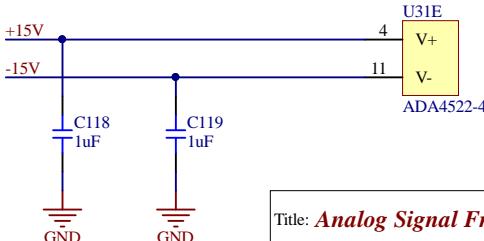
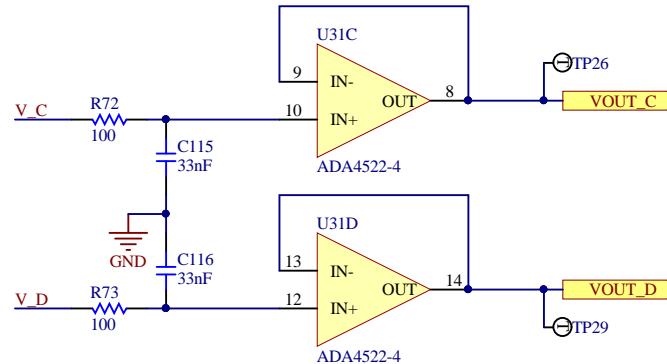
B



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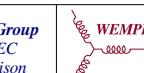
D



Title: Analog Signal Front-End

File: AnalogSigCond.SchDoc Sheet: 9 of 23

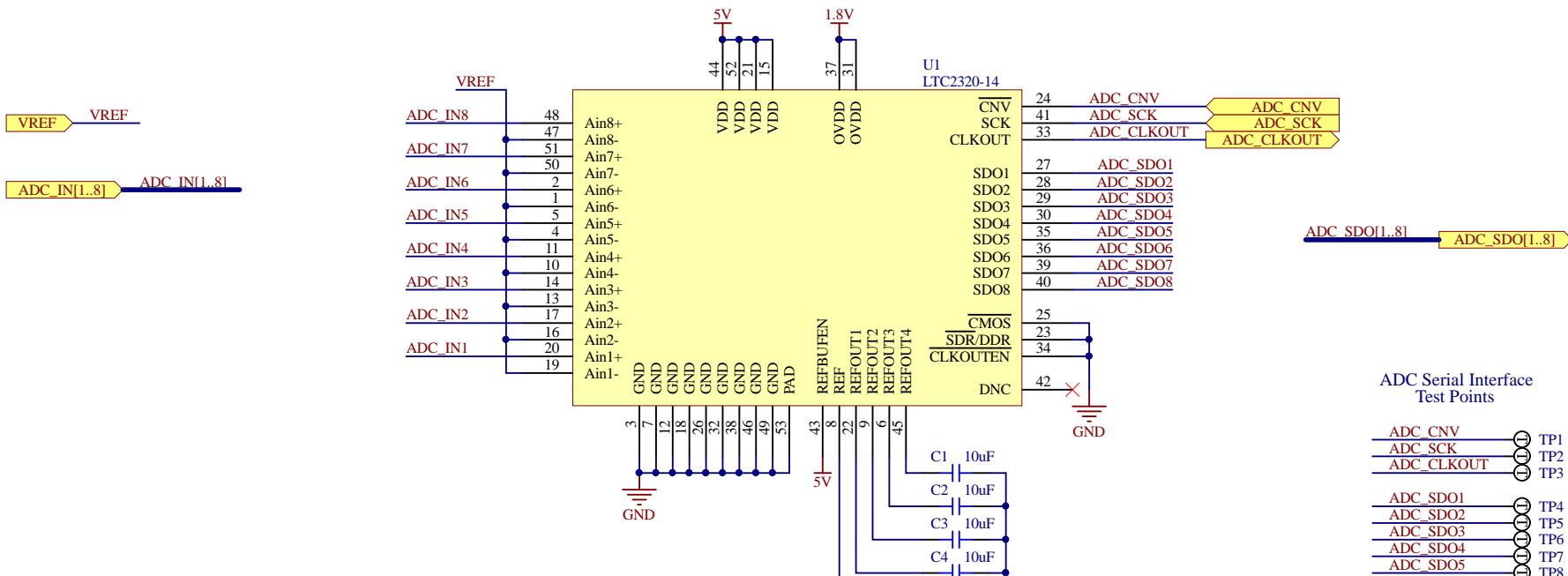
Revision: D Time: 1:02:08 PM Date: 10/16/2019

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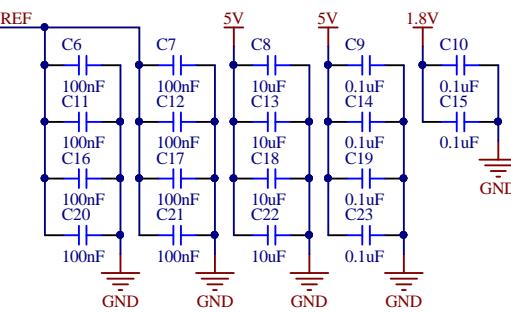
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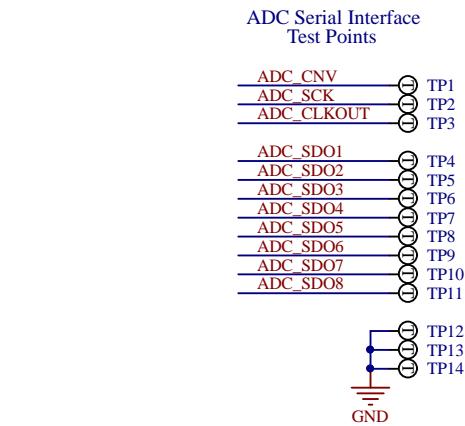
B

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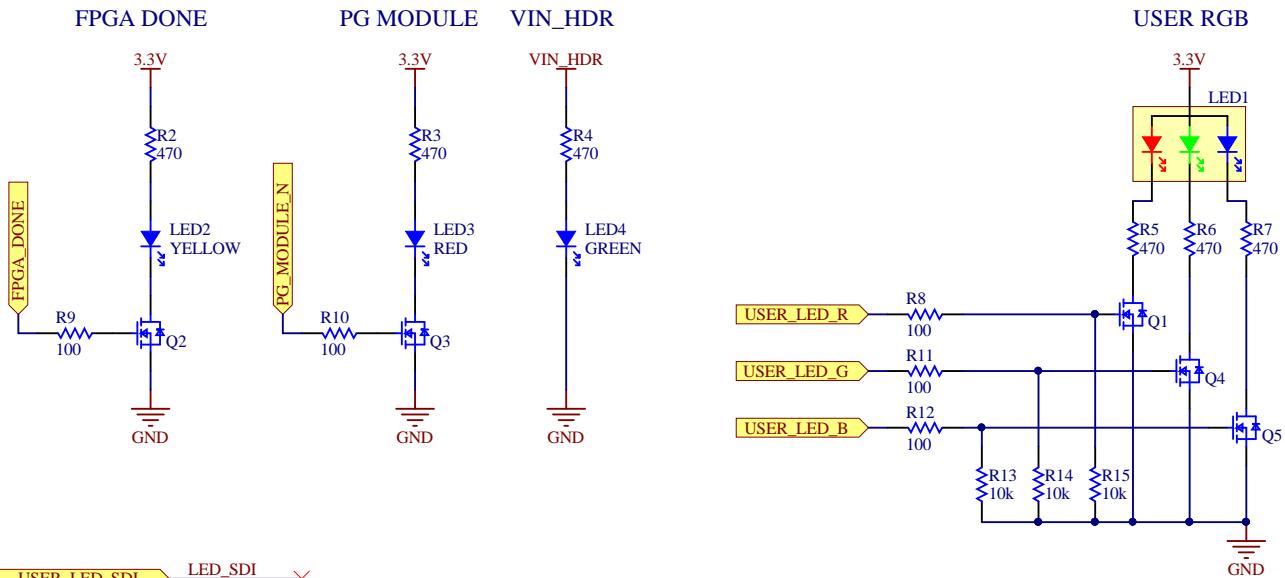


D

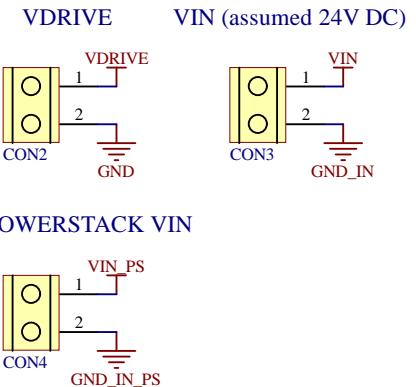
D

Title: <b>ADC</b>		Severson Group WEMPEC UW-Madison
File: AnalogADCs.SchDoc	Sheet: 10 of 23	
Revision: D	Time: 1:02:09 PM	
Date: 10/16/2019		Engineer: Nathan Petersen

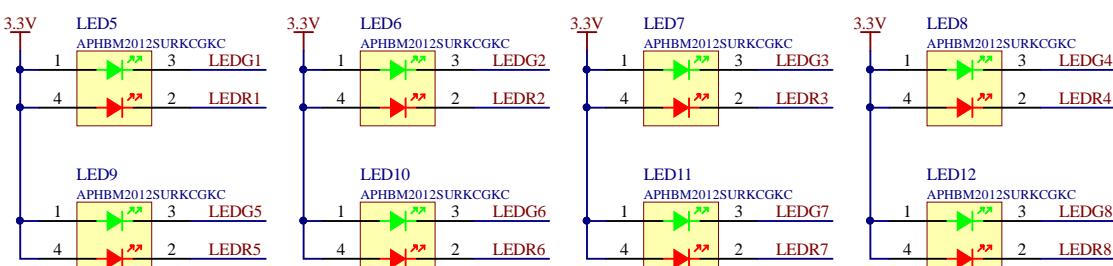
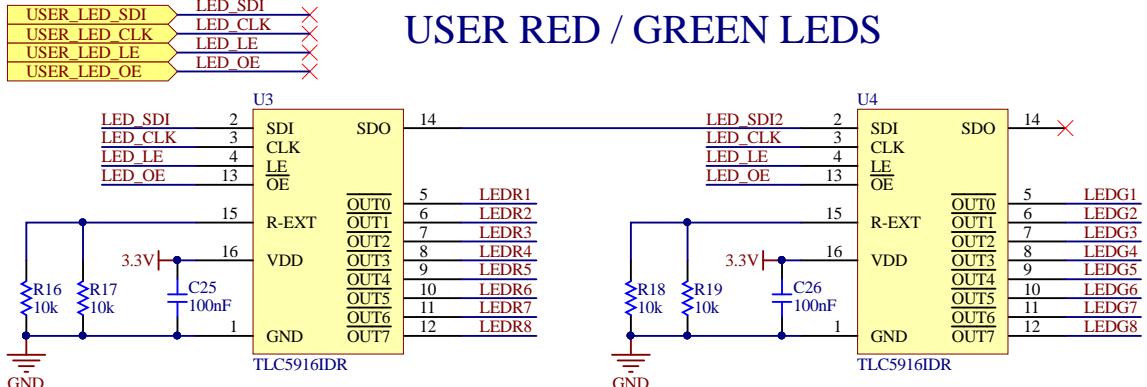
# STATUS LEDS



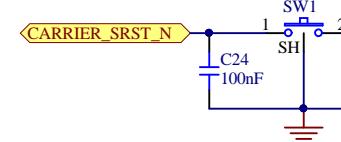
# POWER CONNECTORS



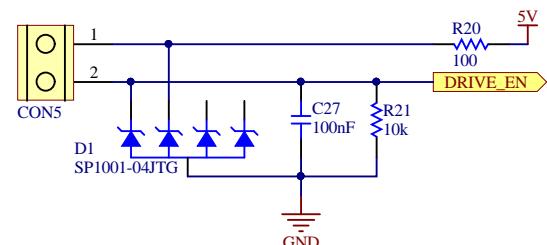
# USER RED / GREEN LEDs



# RESET BUTTON



# DRIVE ENABLE (ESTOP)



Title: **Board I/O**

File: **BoardIO.SchDoc**

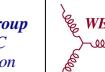
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Revision: **D**

Time: **1:02:09 PM**

Date: **10/16/2019**

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A

A

B

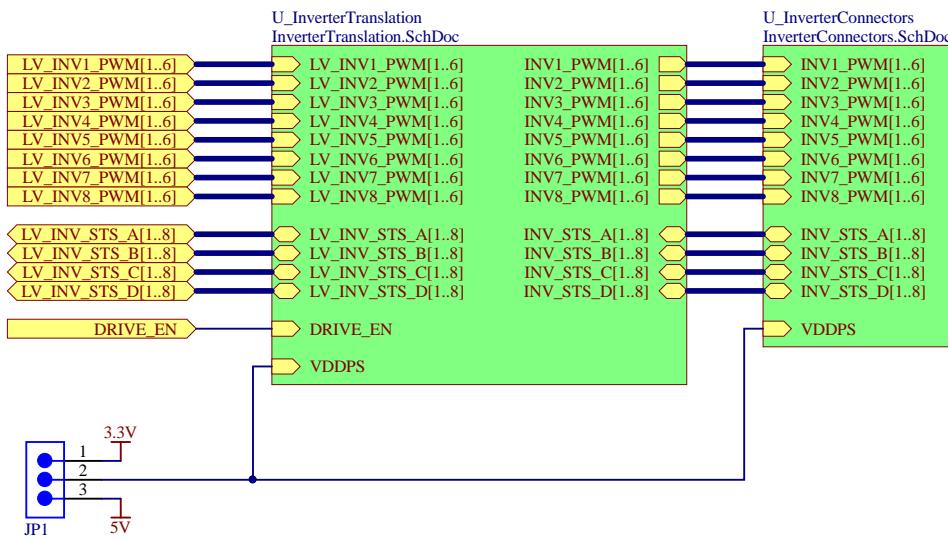
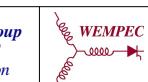
B

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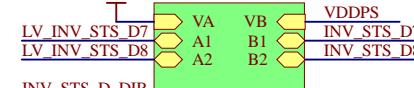
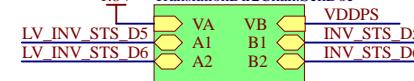
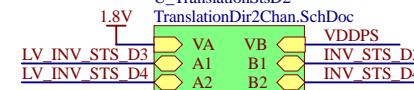
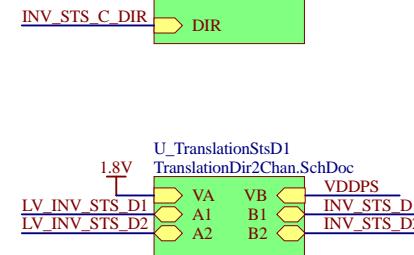
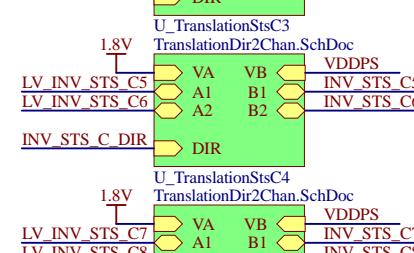
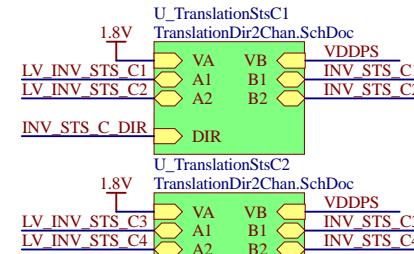
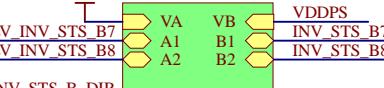
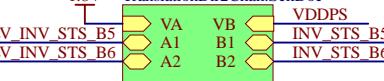
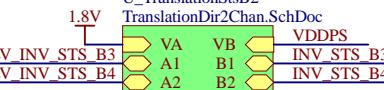
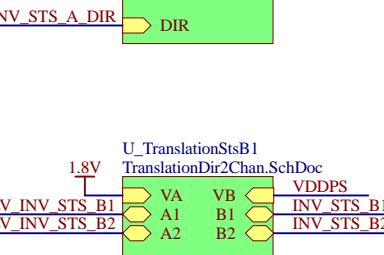
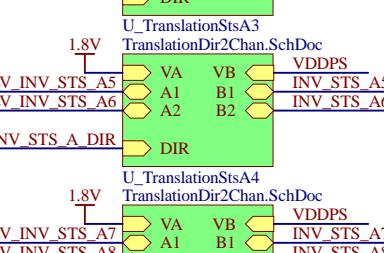
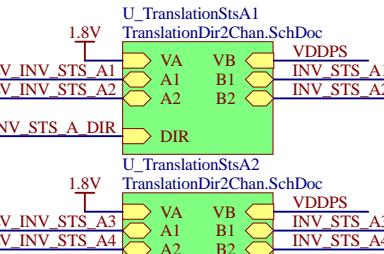
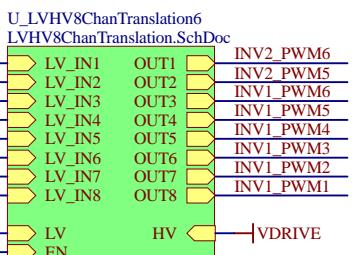
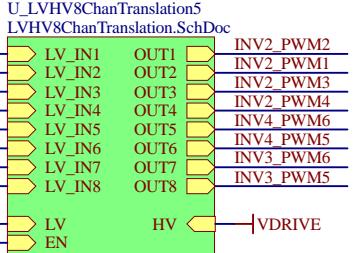
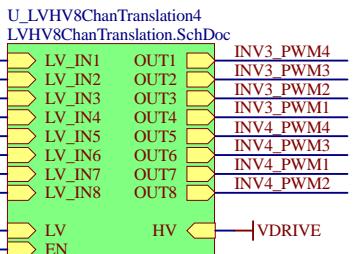
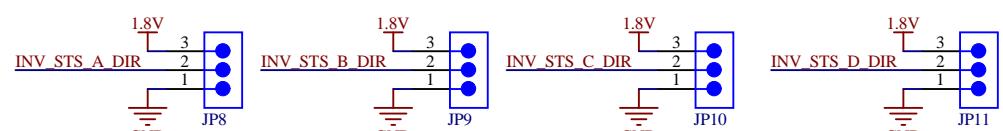
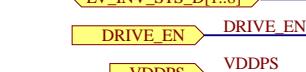
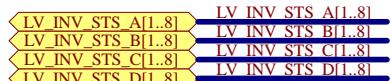
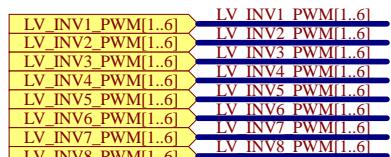
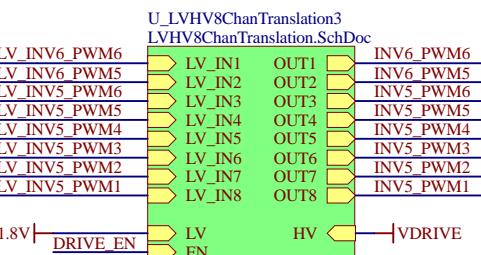
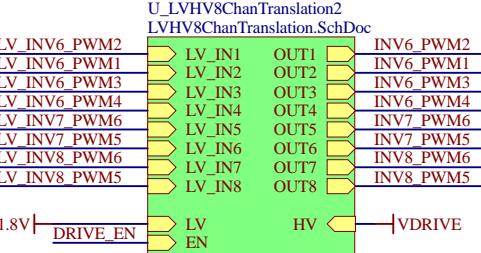
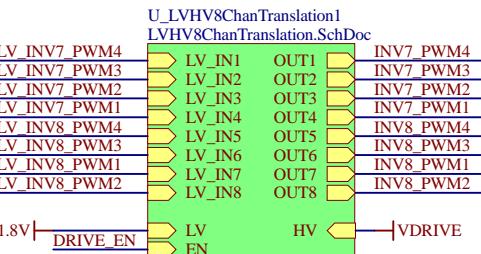
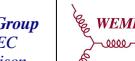
C

D

D

Title: **Drive Interface**File: **DriveInterface.SchDoc**Sheet: **12 of 23**Revision: **D** Time: **1:02:09 PM**Date: **10/16/2019**
**Severson Group**  
**WEMPEC**  
**UW-Madison**


A

Title: **Inverter Level Translation**Severson Group  
WEMPEC  
UW-Madison

File: InverterTranslation.SchDoc Sheet: 13 of 23

Revision: D Time: 1:02:09 PM Date: 10/16/2019

Engineer: Nathan Petersen

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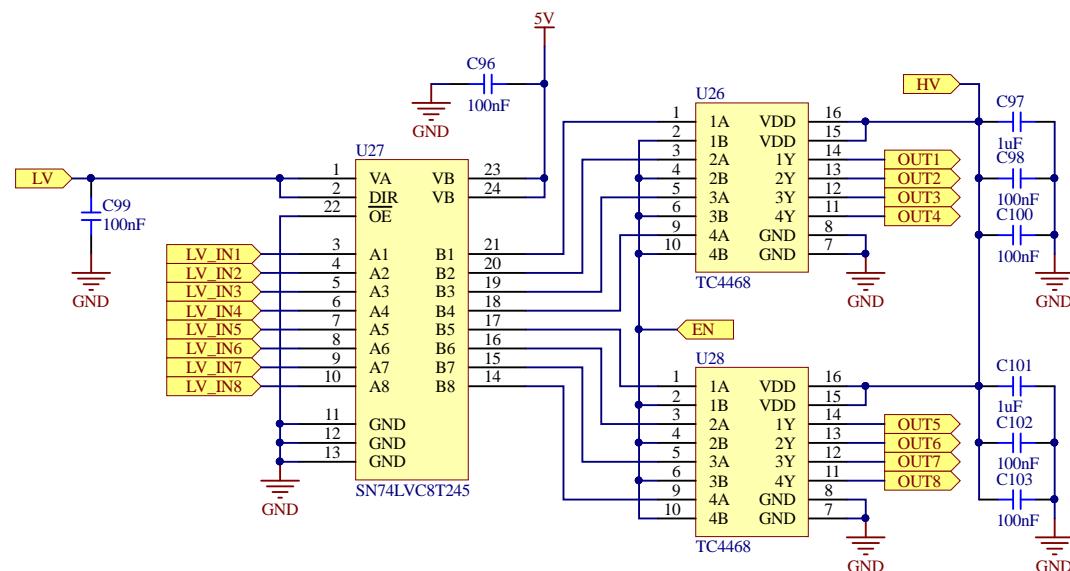
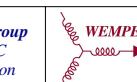
B

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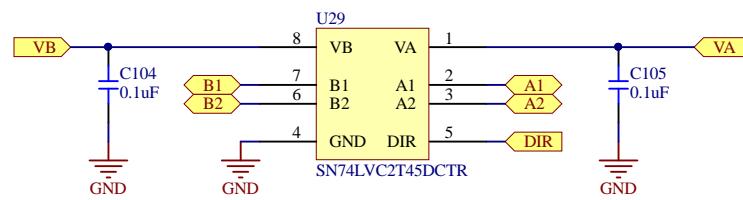
Title: **8-channel LV to HV Translation**File: **LVH8ChanTranslation.SchDoc** | Sheet: **14 of 23**Revision: **D** | Time: **1:02:10 PM**Date: **10/16/2019** | Engineer: **Nathan Petersen**
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**WEMPEC**  
**UW-Madison**


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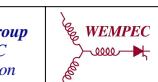
D

Title: **2-Channel Directional Translation**

File: TranslationDir2Chan.SchDoc | Sheet: 15 of 23

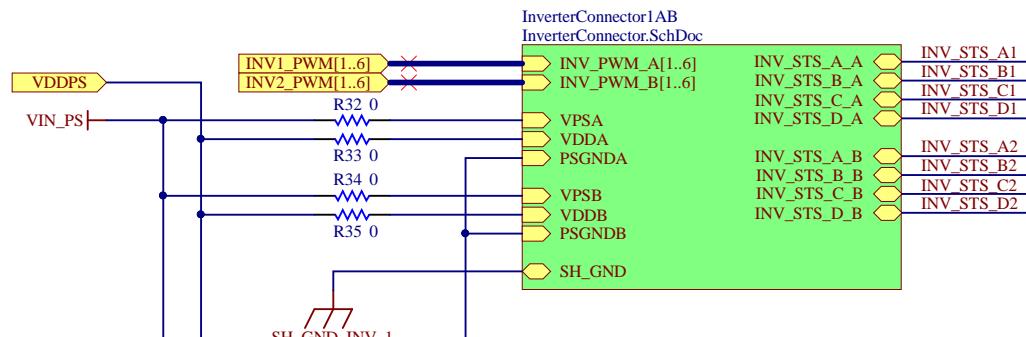
Revision: D | Time: 1:02:10 PM | Date: 10/16/2019

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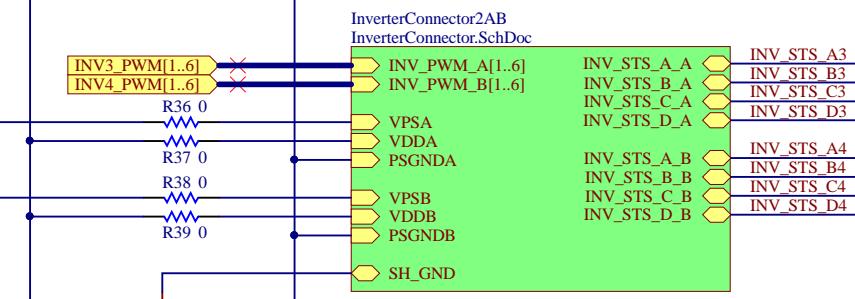


Engineer: Nathan Petersen

A

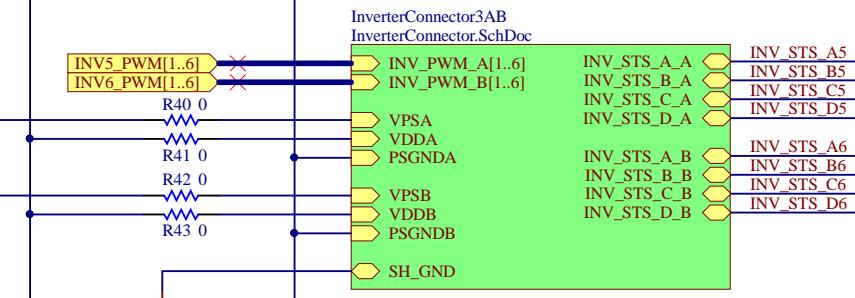


B



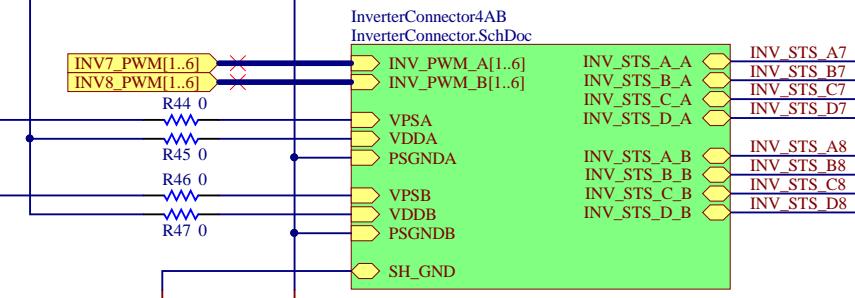
B

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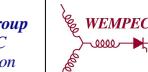


D

Title: **Inverter Connectors**

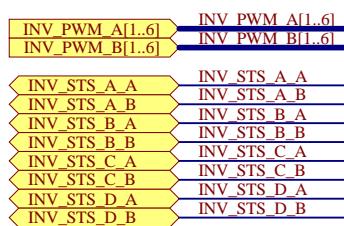
File: InverterConnectors.SchDoc | Sheet: 16 of 23

Revision: D | Time: 1:02:10 PM | Date: 10/16/2019

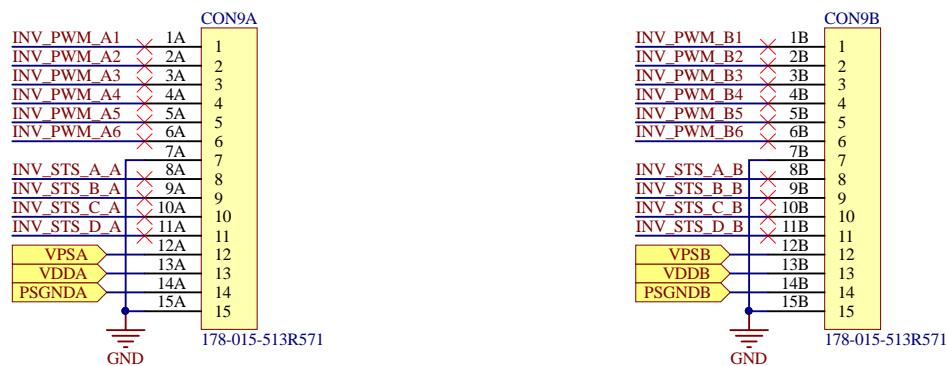
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Engineer: Nathan Petersen

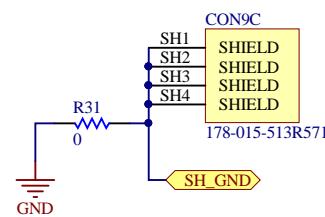
A



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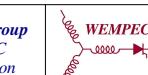
Title: **Inverter Connector**

File: InverterConnector.SchDoc

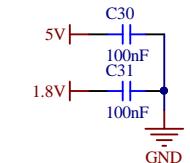
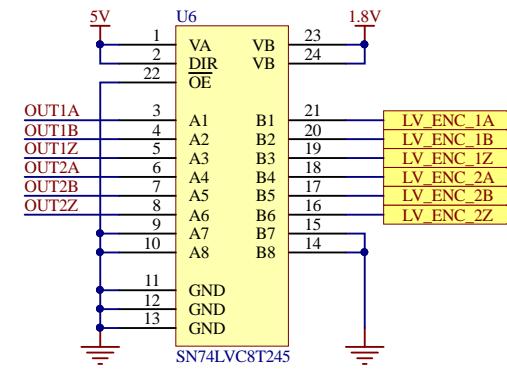
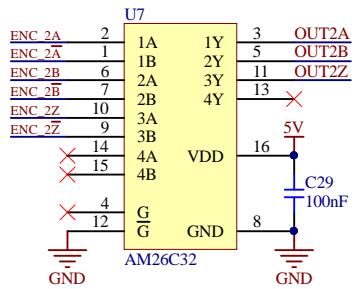
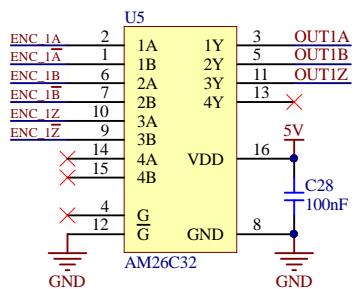
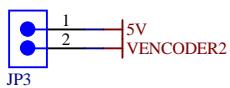
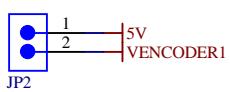
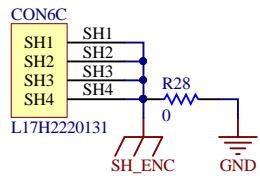
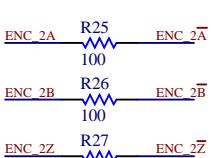
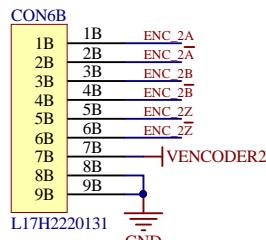
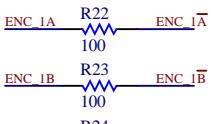
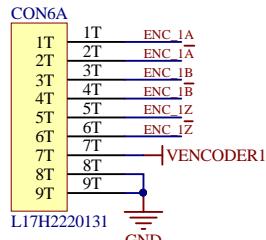
Revision: D Time: 1:02:10 PM

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Date: 10/16/2019  
Engineer: Nathan Petersen

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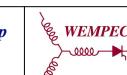
Title: **Encoders**

File: Encoder.SchDoc

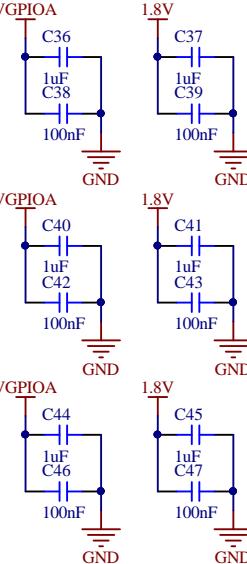
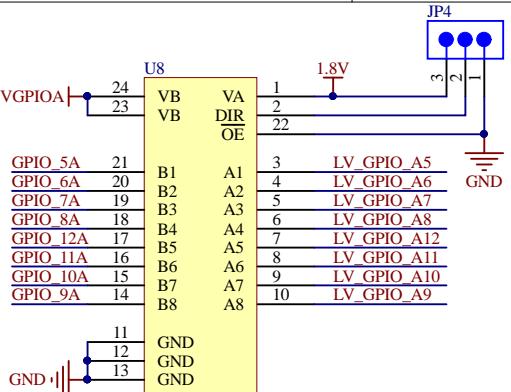
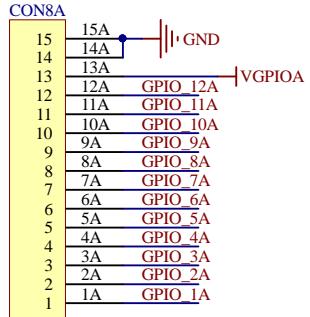
Sheet: 18 of 23

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Date: 10/16/2019

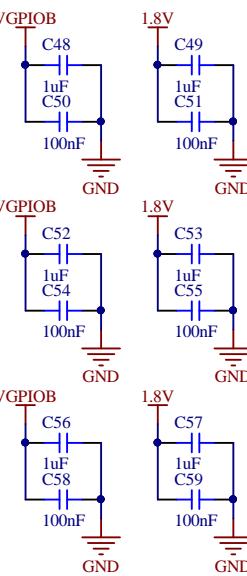
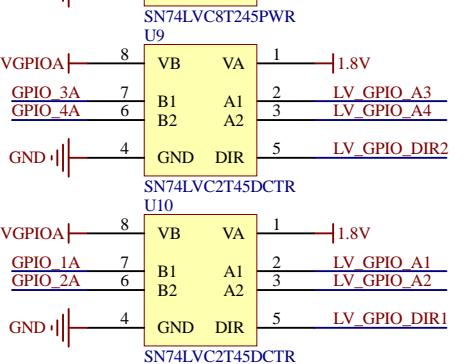
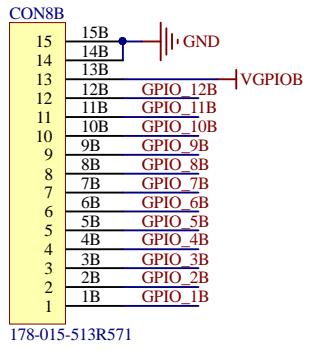
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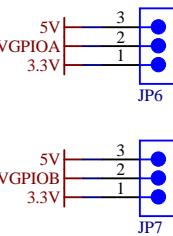
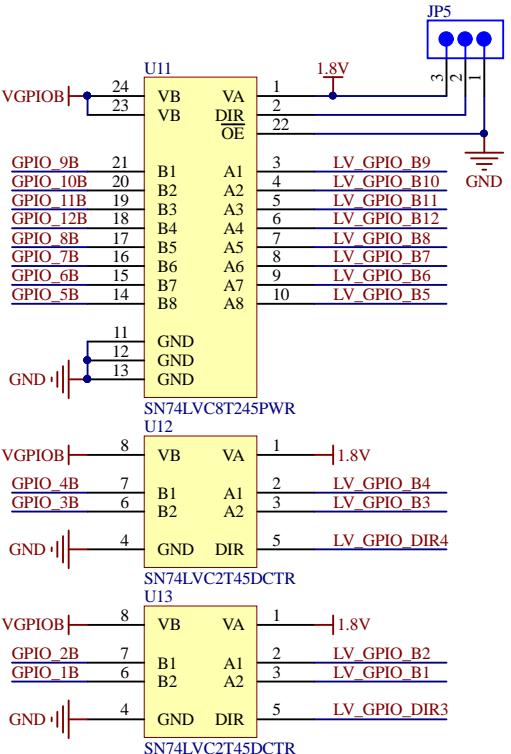
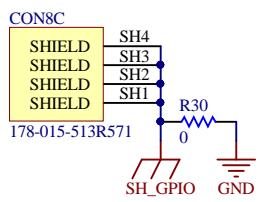


LV\_GPIO\_DIR[1..4]      LV\_GPIO\_DIR[1..4]  
 LV\_GPIO\_A[1..12]      LV\_GPIO\_A[1..12]  
 LV\_GPIO\_B[1..12]      LV\_GPIO\_B[1..12]

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Title: <b>GPIO</b>		Severson Group
File: <b>GPIO.SchDoc</b>		WEMPEC
Sheet: <b>19 of 23</b>		UW-Madison
Revision: <b>D</b>	Time: <b>1:02:11 PM</b>	Date: <b>10/16/2019</b>
Engineer: <b>Nathan Petersen</b>		WEMPEC

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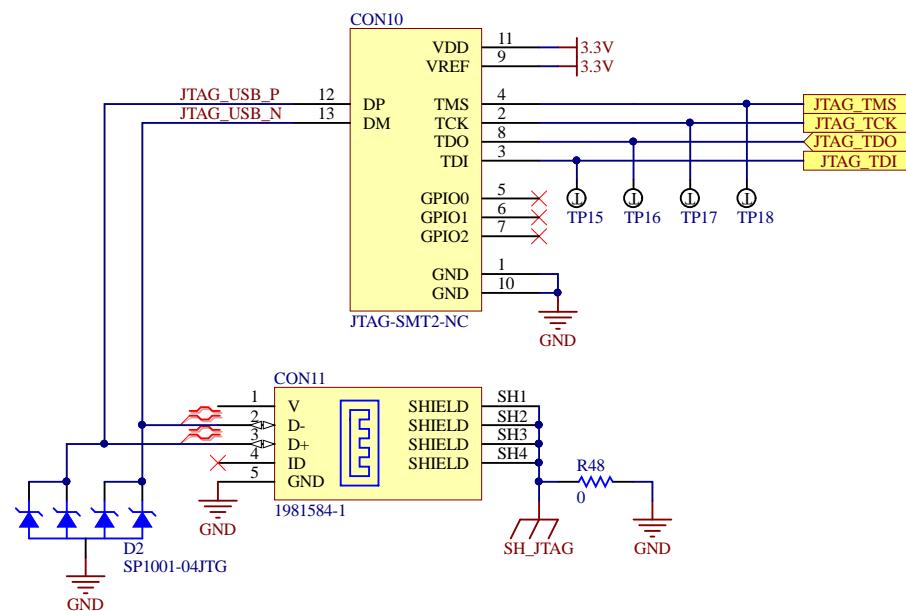
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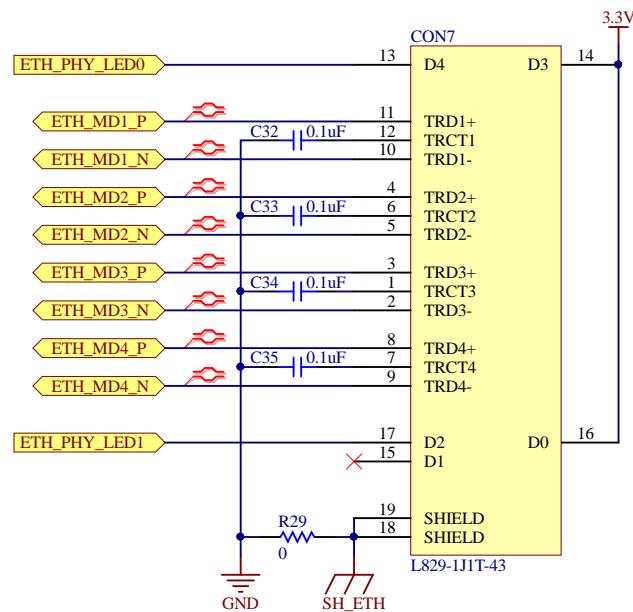
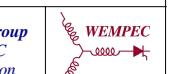
B

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Title: **SoM Gb Ethernet**File: **GbEthernet.SchDoc** Sheet: **21 of 23**Revision: **D** Time: **1:02:11 PM** Date: **10/16/2019****Severson Group**  
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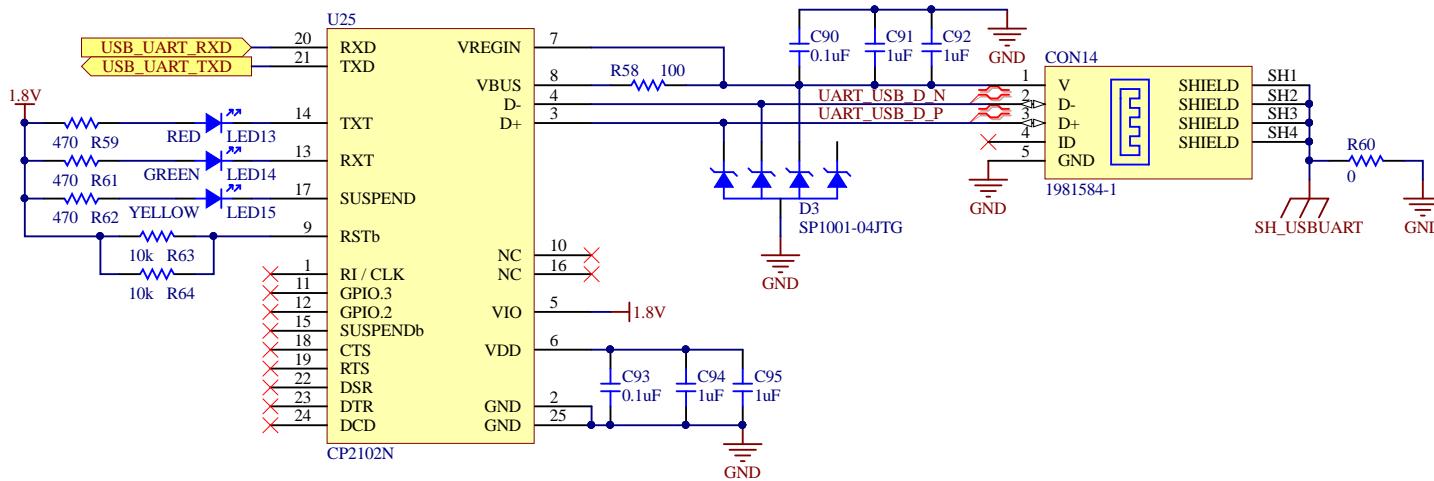
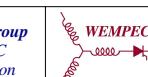
B

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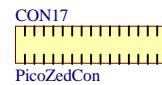
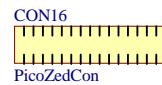
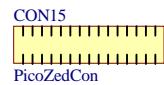
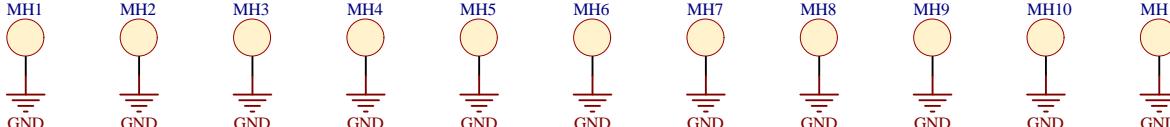
Title: **USB UART**File: **USB\_UART.SchDoc**Sheet: **22 of 23**Revision: **D** Time: **1:02:11 PM**Date: **10/16/2019**
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Engineer: **Nathan Petersen**

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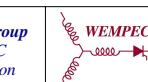
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**4-40 Screws:****4-40 Standoffs:****Mouting Holes:**Title: ***Back Page***File: **BackPage.SchDoc**Sheet: **23 of 23**Revision: **D** Time: **1:02:12 PM**Date: **10/16/2019**

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