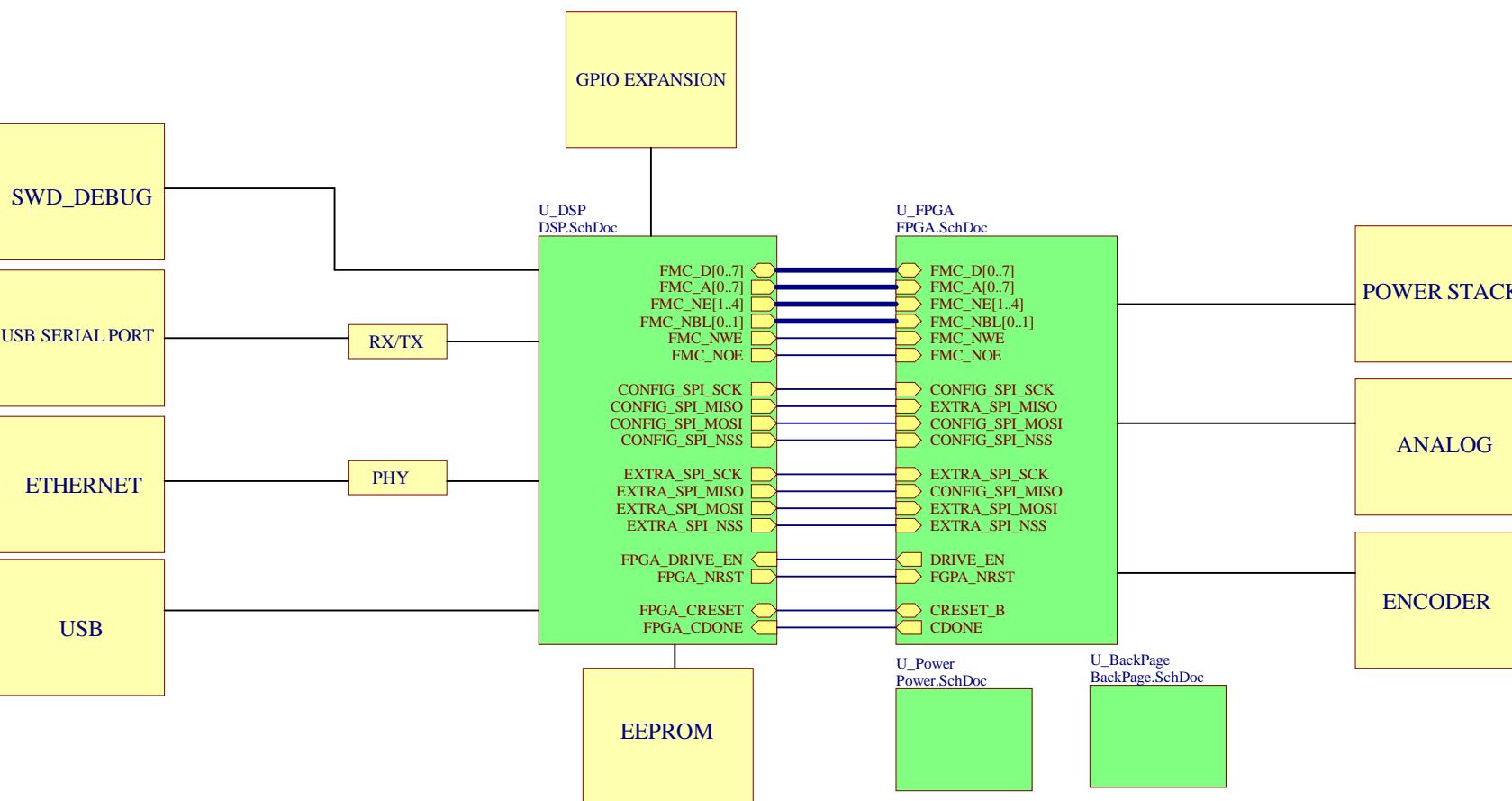


A

A



B

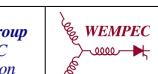
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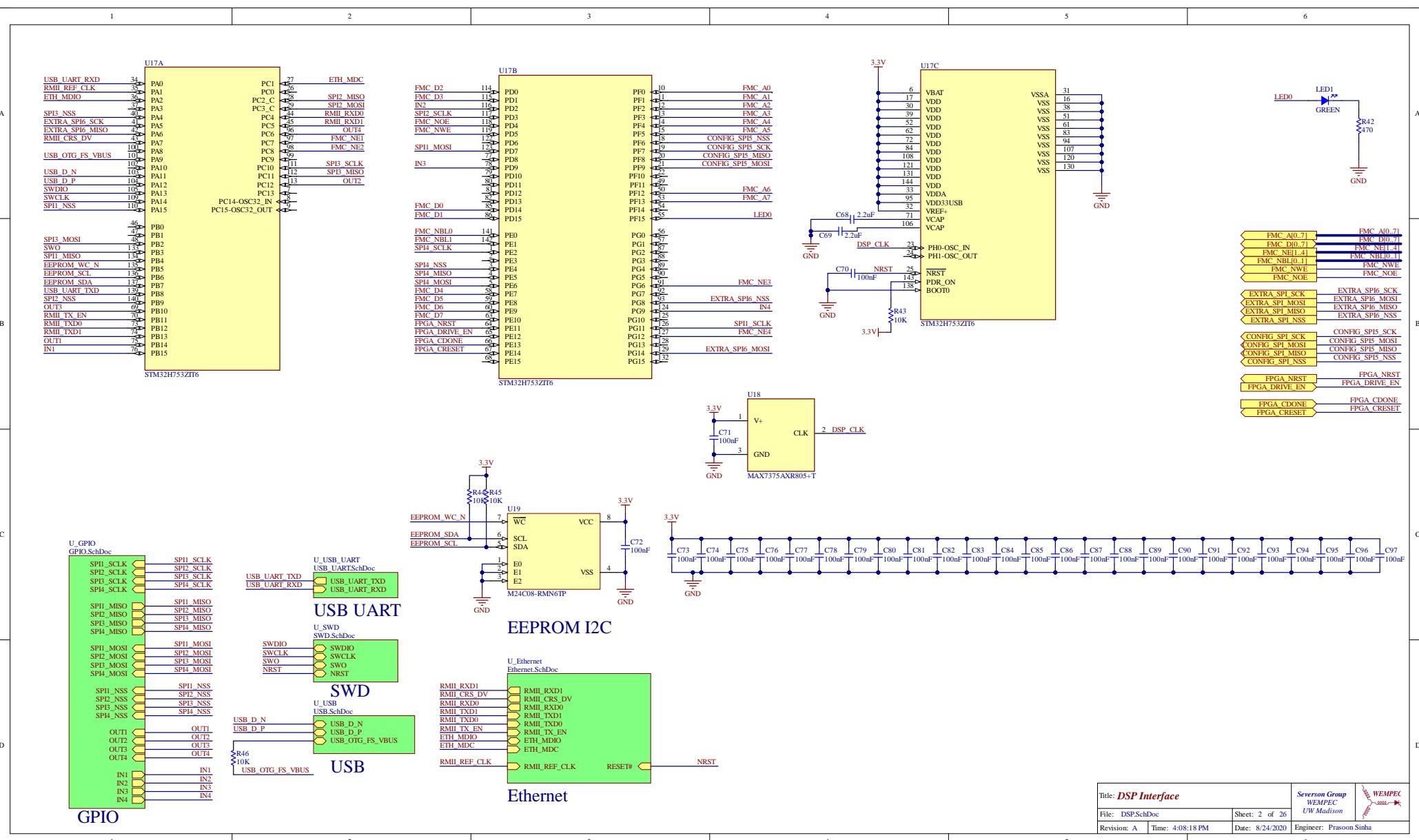
C

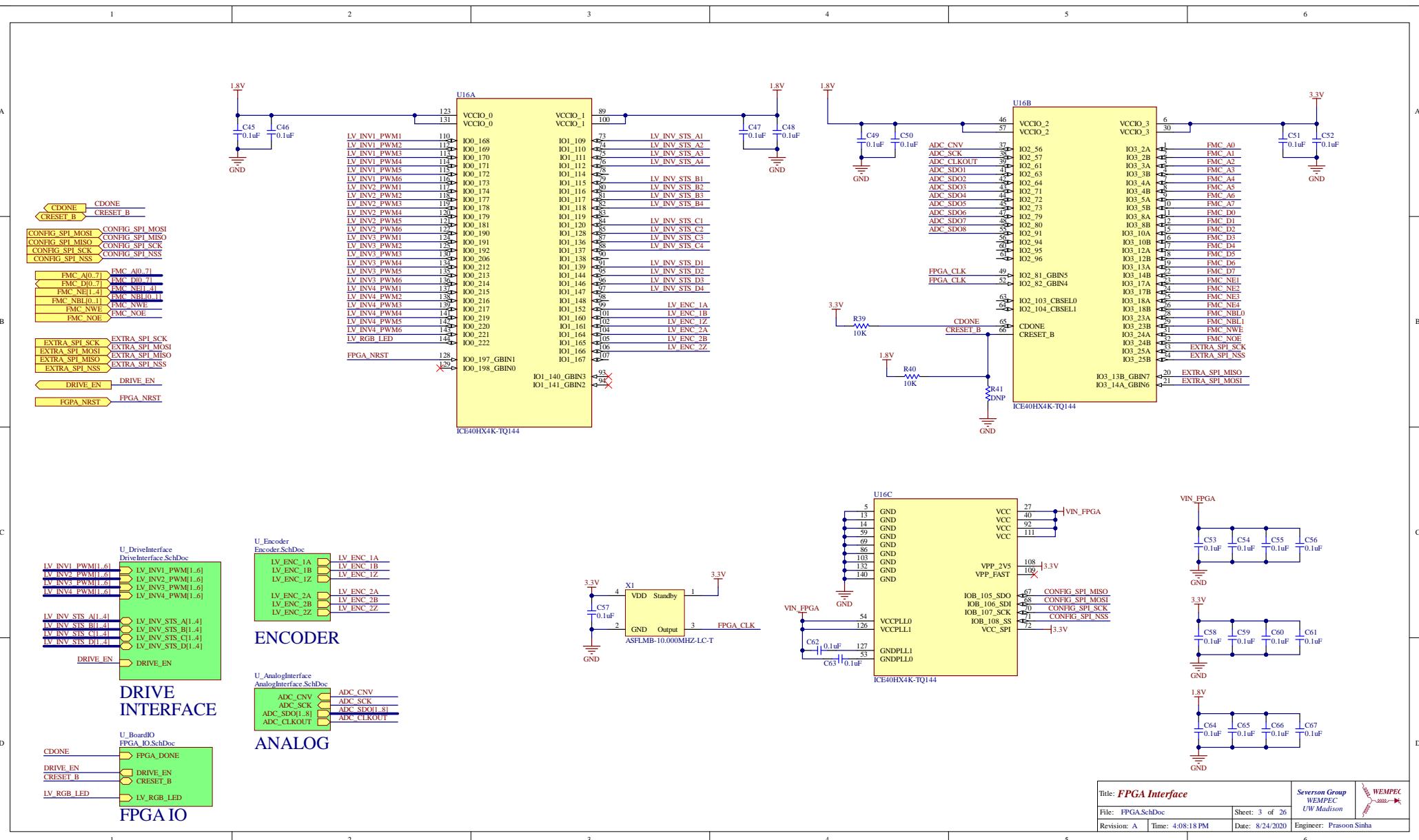
C

D

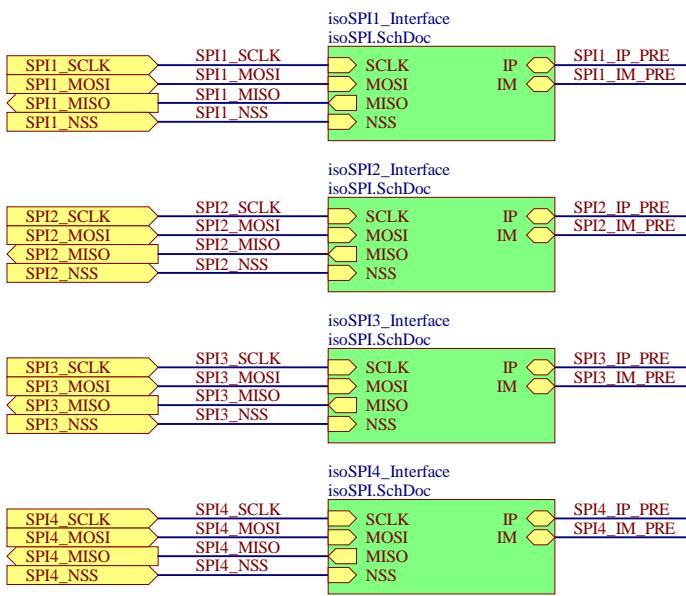
D

Title: ***uAMDC***File: ***uAMDC.SchDoc***Sheet: ***1 of 26***Revision: ***A*** Time: ***4:08:18 PM***Date: ***8/24/2020***
Severson Group
 WEMPEC
 UWMadison
Engineer: ***Prasoon Sinha***

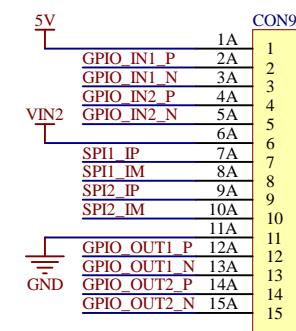
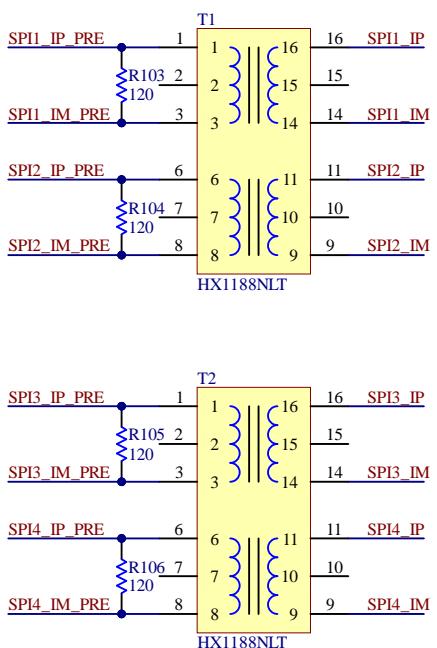




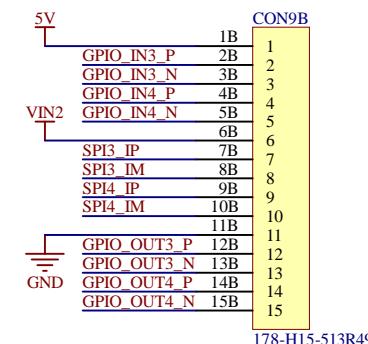
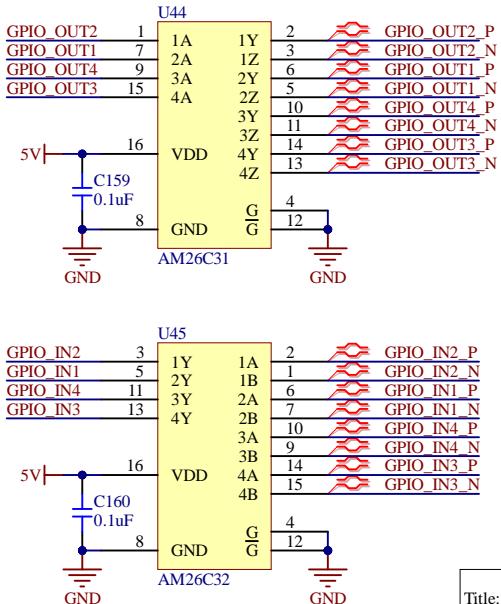
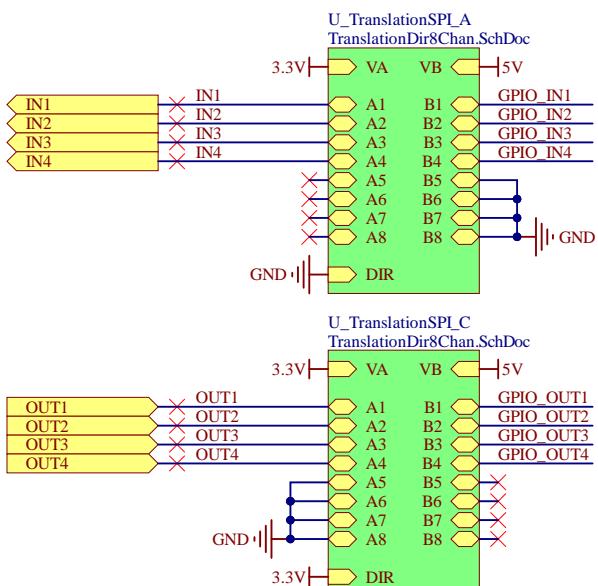
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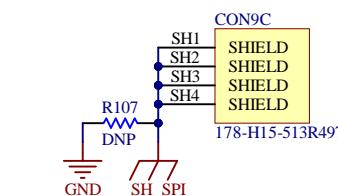
B



C



D



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B

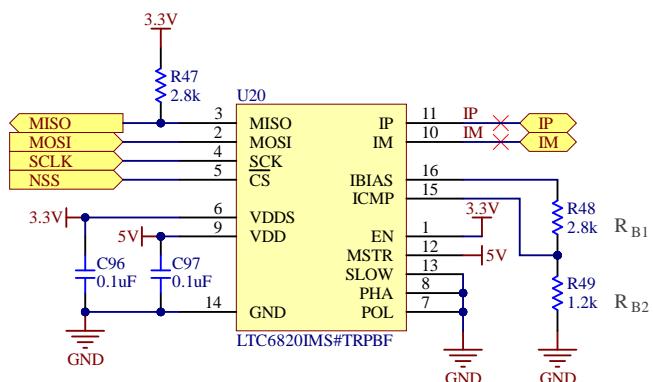
B

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C

D

D

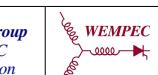
Title: *isoSPI Interface*

File: isoSPI.SchDoc

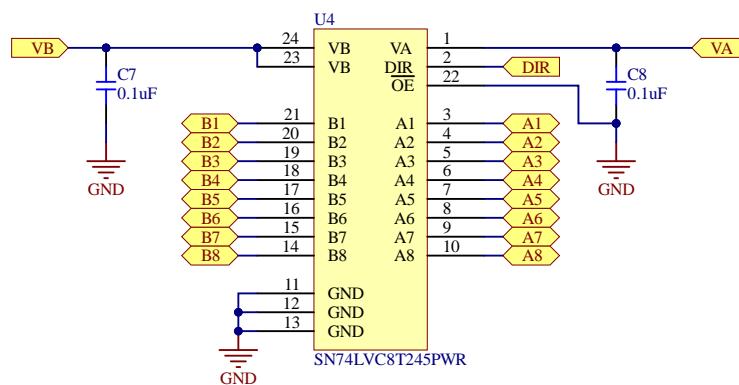
Sheet: 5 of 26

Revision: A Time: 4:08:19 PM Date: 8/24/2020

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Engineer: Nathan Petersen

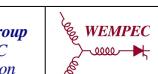


Title: **8-Channel Directional Translation**

File: **TranslationDir8Chan.SchDoc** Sheet: **6 of 26**

Revision: **A** Time: **4:08:19 PM** Date: **8/24/2020**

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Engineer: **Nathan Petersen**

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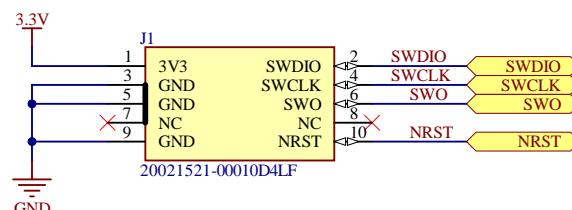
B

C

C

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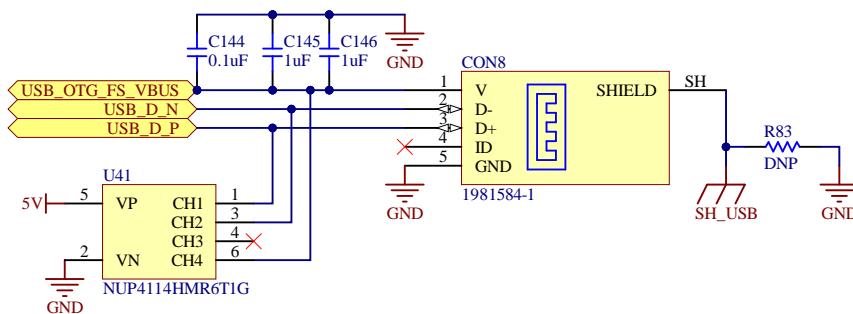
Title: SWD			Severson Group WEMPEC UWMadison
File: SWD.SchDoc	Sheet: 7 of 26		
Revision: A	Time: 4:08:19 PM	Date: 8/24/2020	
Engineer: Prasoon Sinha			WEMPEC

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Title: USB			Severson Group WEMPEC UWMadison
File: USB.SchDoc	Sheet: 8 of 26		
Revision: A	Time: 4:08:19 PM	Date: 8/24/2020	
Engineer: Prasoon Sinha			WEMPEC

A

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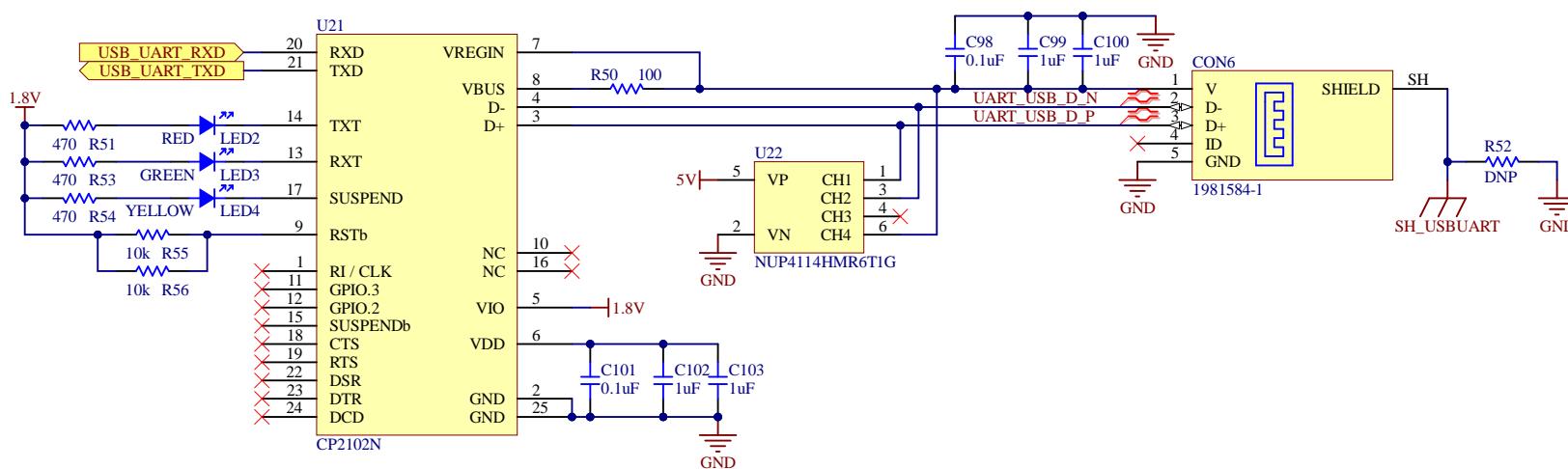
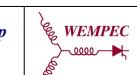
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C

C

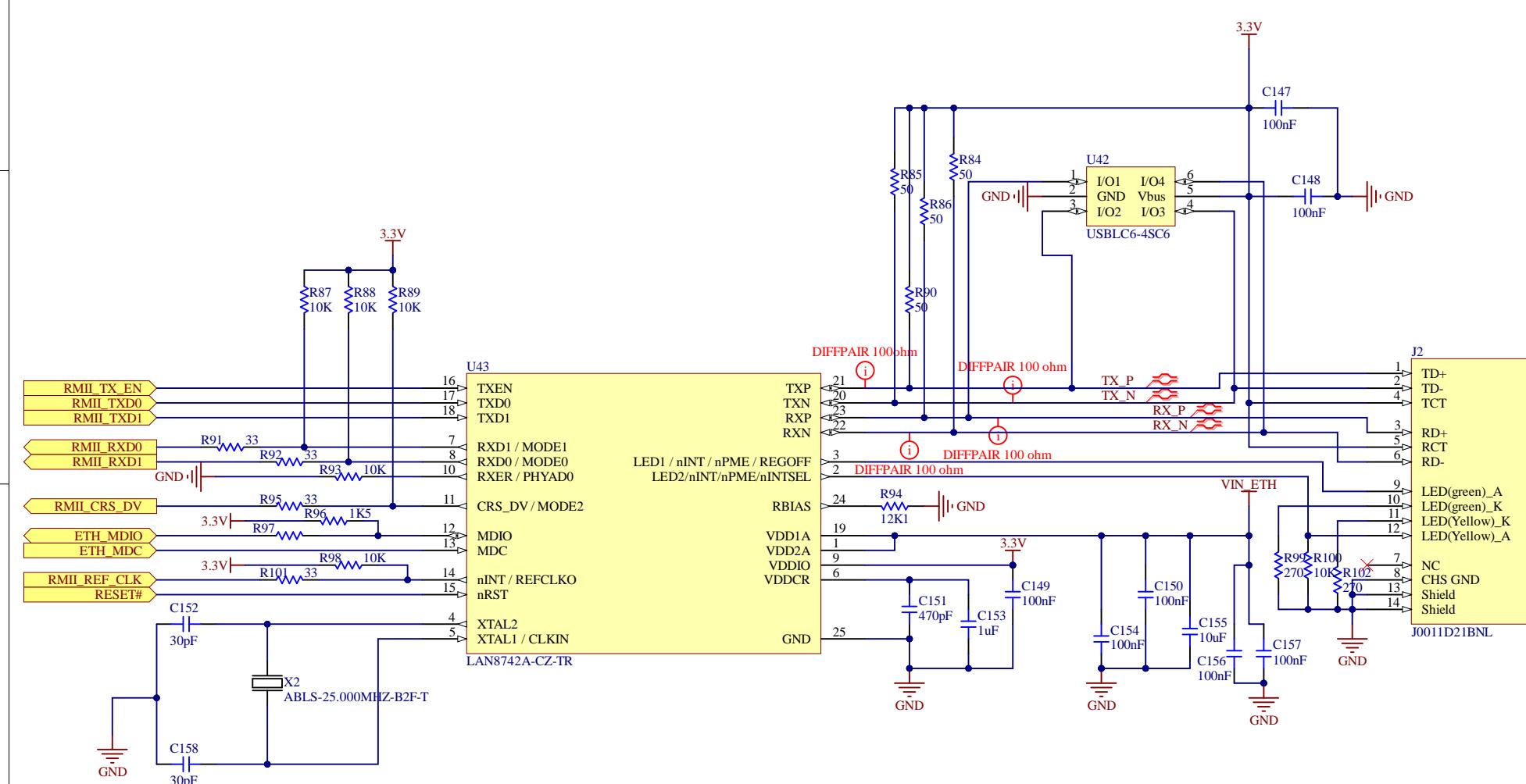
D

D

Title: **USB UART**File: **USB_UART.SchDoc**Sheet: **9 of 26**Revision: **A** Time: **4:08:19 PM**Date: **8/24/2020**
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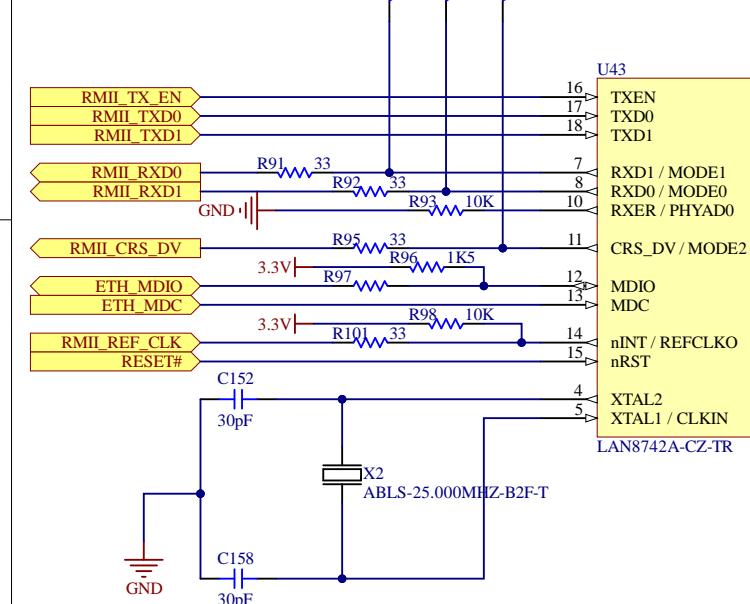
A

A



B

B



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C

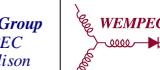
Title: *Ethernet*File: *Ethernet.SchDoc*

Revision: A

Sheet: 10 of 26

Time: 4:08:19 PM

Date: 8/24/2020

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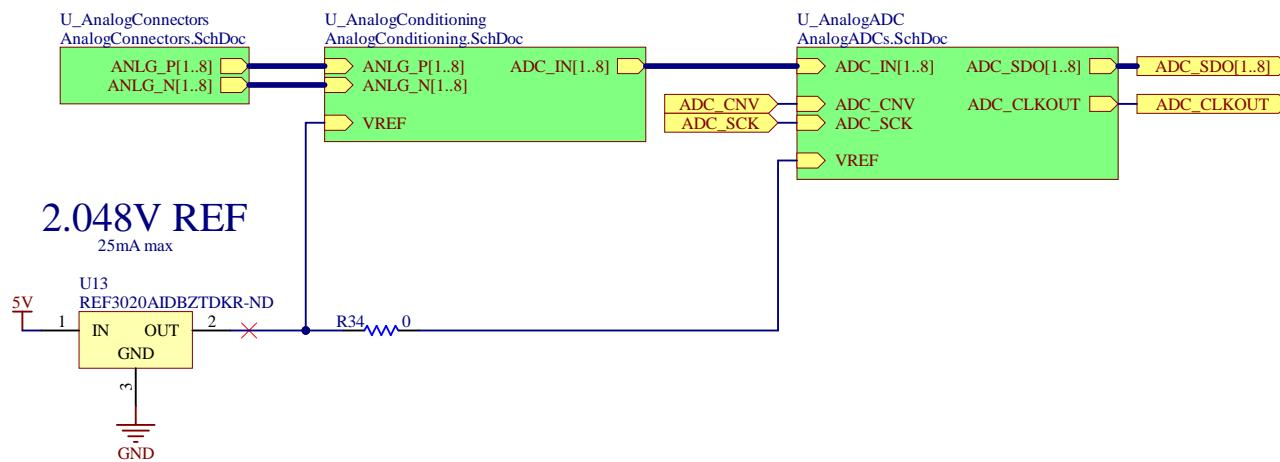
Engineer: Prasoon Sinha

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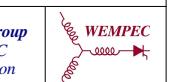


C

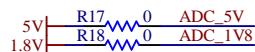
C

D

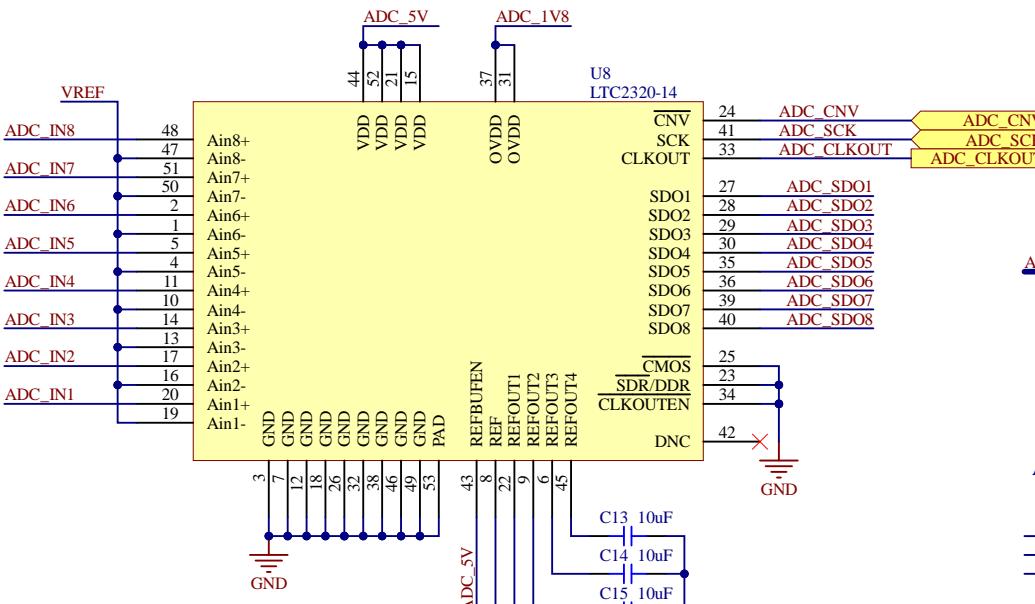
D

Title: **Analog Interface**File: **AnalogInterface.SchDoc**Sheet: **11 of 26**Revision: **A** Time: **4:08:19 PM**Date: **8/24/2020**
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UWMadison
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A

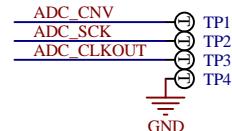


VREF
ADC_IN[1..8]

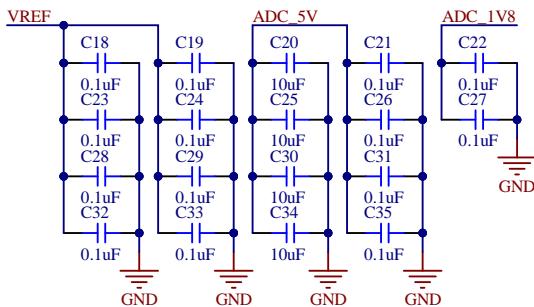


ADC_SDO[1..8] ADC_SDO[1..8]

ADC Serial Interface Test Points



B



C

A

B

C

D

A

A

B

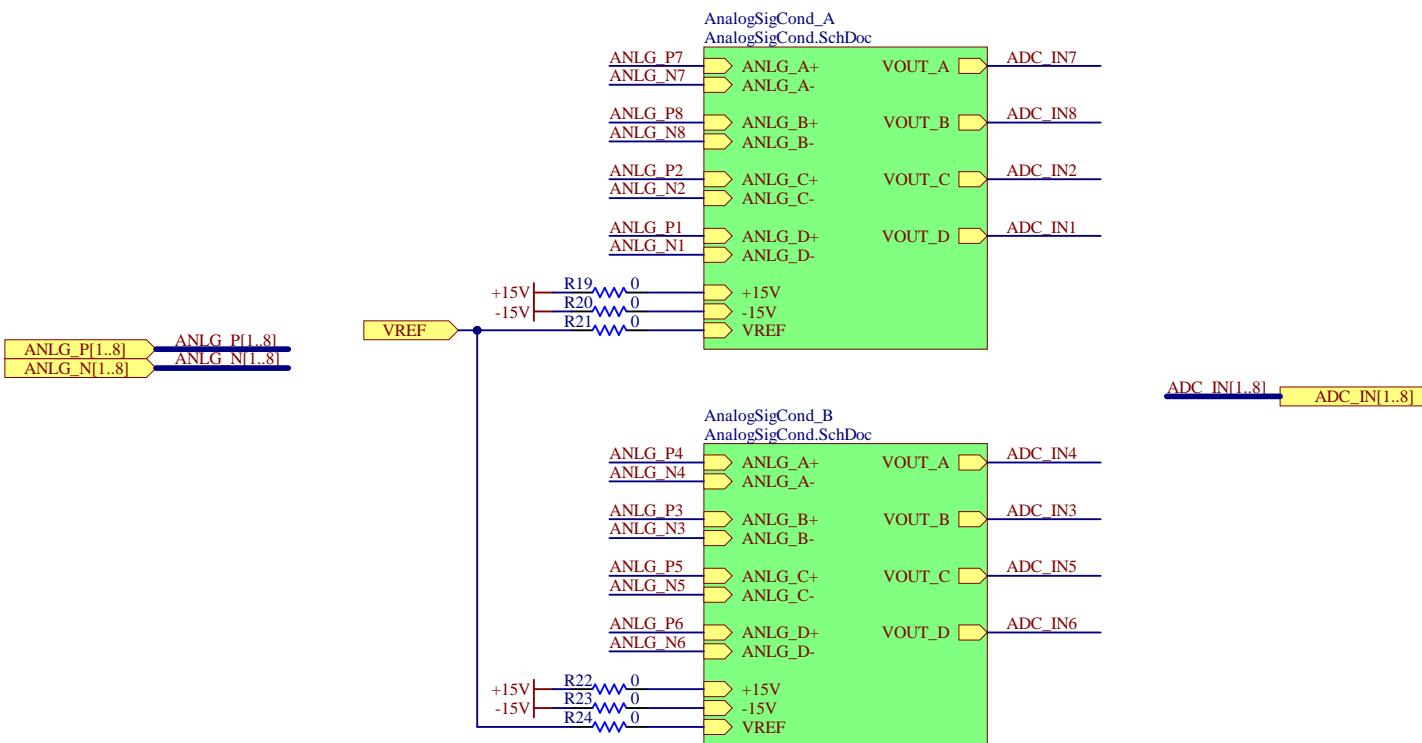
B

C

C

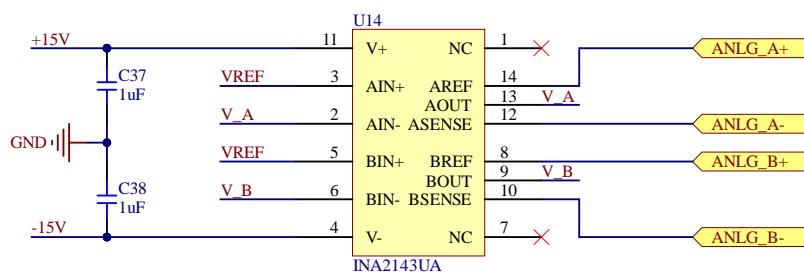
D

D



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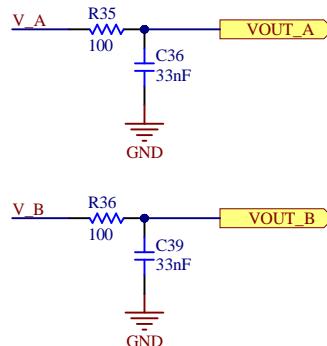
A



B

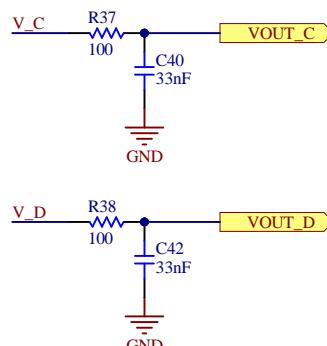
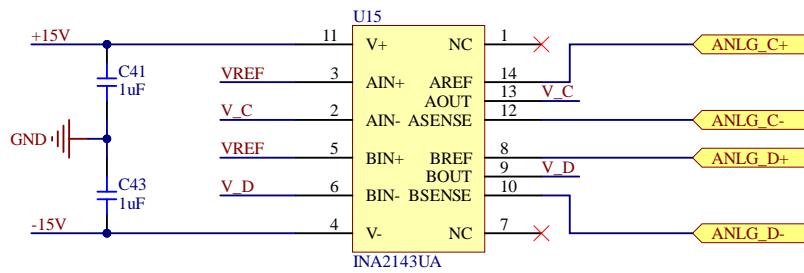
B

△ LPF: fc = 50kHz



C

C



D

D



Title: **Analog Signal Front-End**

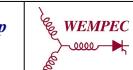
File: **AnalogSigCond.SchDoc**

Sheet: **14 of 26**

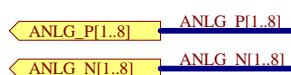
Revision: **A** Time: **4:08:19 PM**

Date: **8/24/2020** Engineer: **Nathan Petersen**

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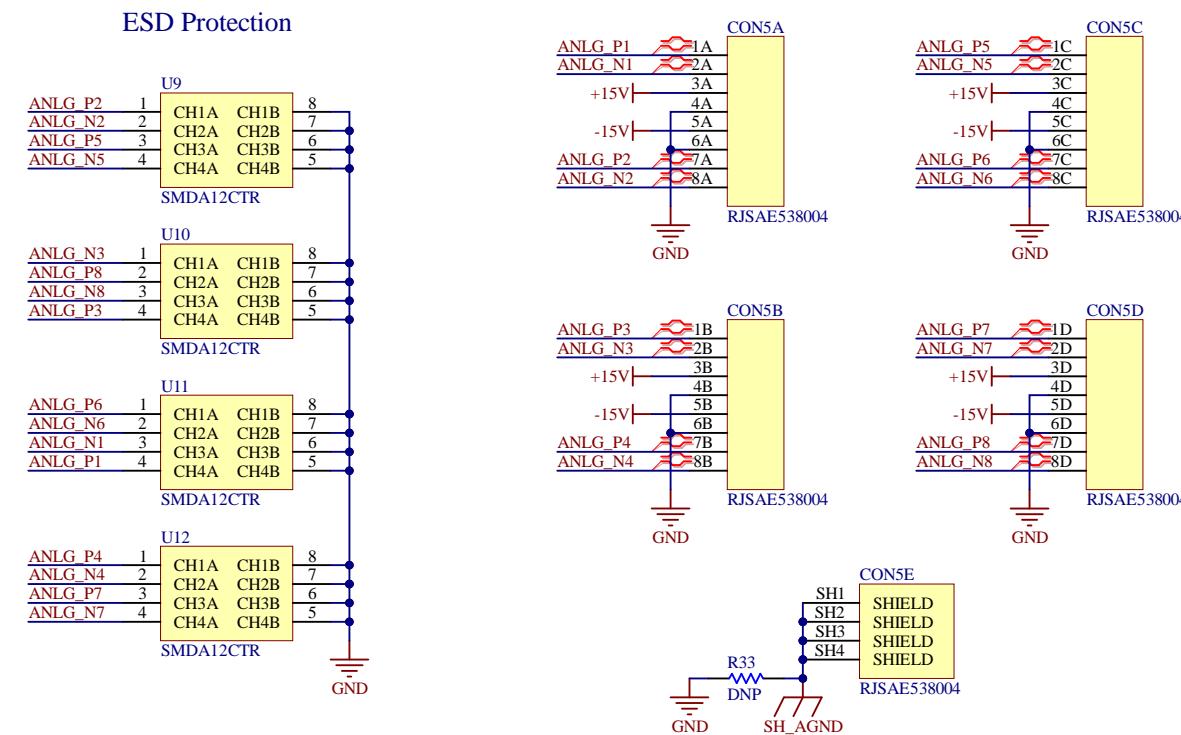


A



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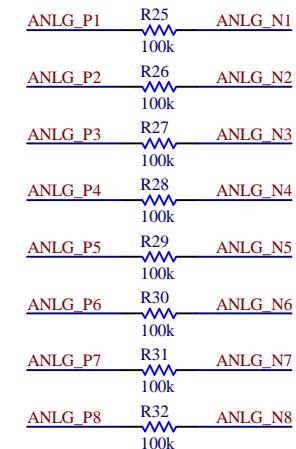
B



B

C

Force no input to 0V



C

D

Title: **Analog RJ45 Connectors**

File: **AnalogConnectors.SchDoc**

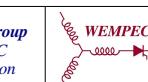
Revision: **A**

Time: **4:08:19 PM**

Sheet: **15 of 26**

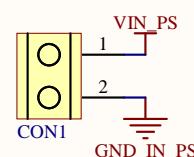
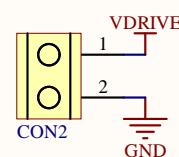
Date: **8/24/2020**

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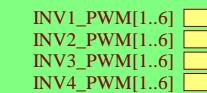
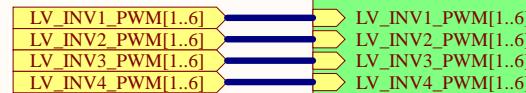
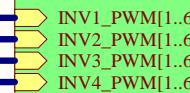


Engineer: **Nathan Petersen**

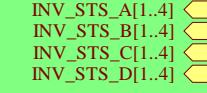
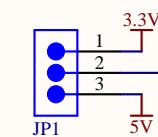
A

POWERSTACK VIN**VDRIVE**

B

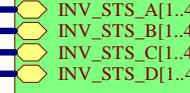
**U_InverterTranslation
InverterTranslation.SchDoc****U_InverterConnectors
InverterConnectors.SchDoc**

C



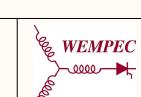
DRIVE_EN

VDDPS



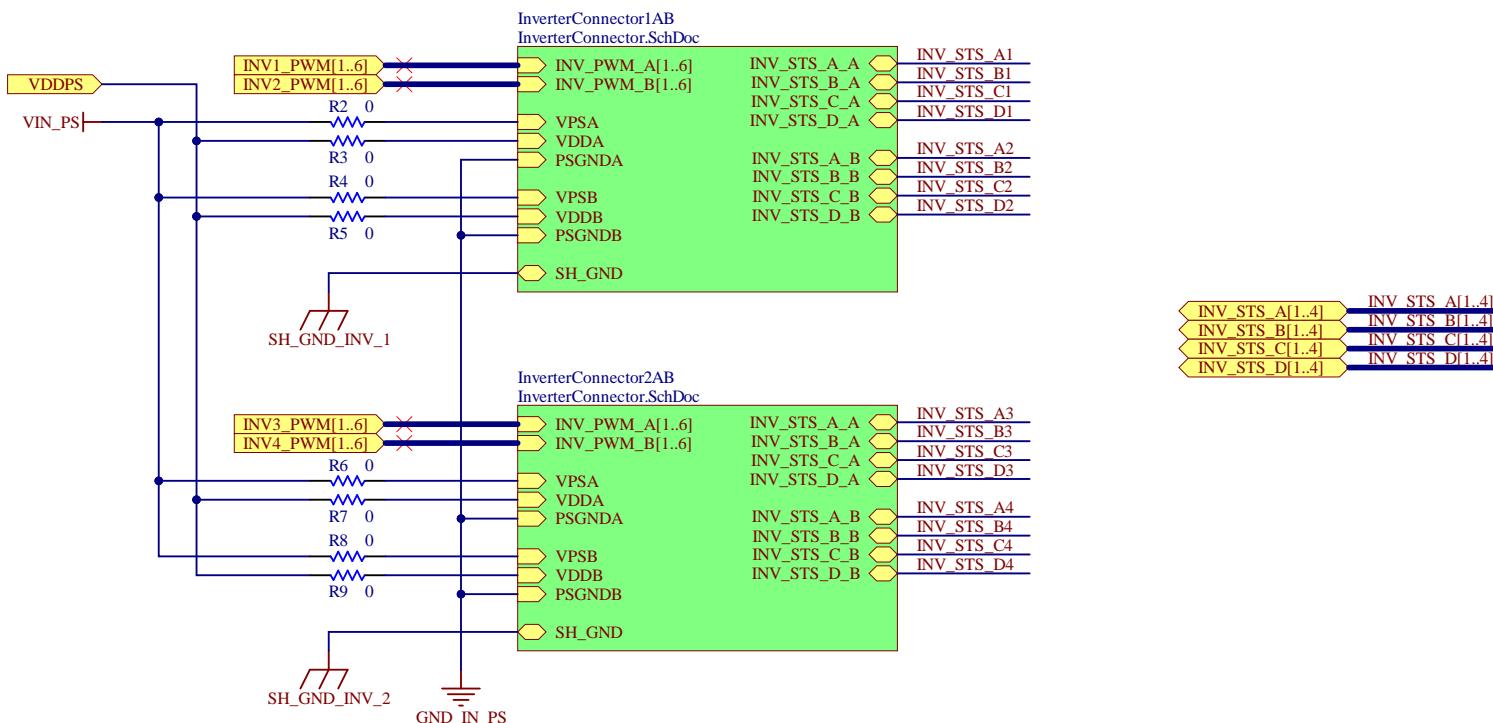
VDDPS

D

Title: **DriveInterface**File: **DriveInterface.SchDoc**Sheet: **16 of 26**Revision: **A** Time: **4:08:19 PM**Date: **8/24/2020****Severson Group
WEMPEC
UW Madison**

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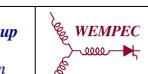
D

Title: **Inverter Connectors**

File: InverterConnectors.SchDoc | Sheet: 17 of 26

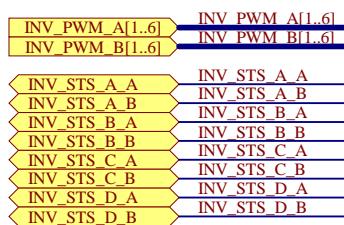
Revision: A | Time: 4:08:19 PM | Date: 8/24/2020

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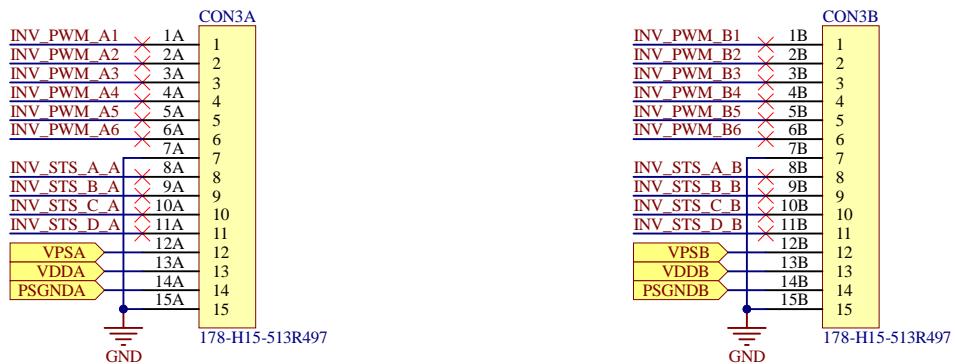


Engineer: Nathan Petersen

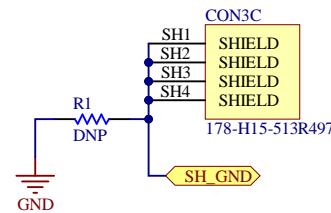
A



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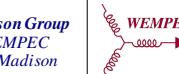
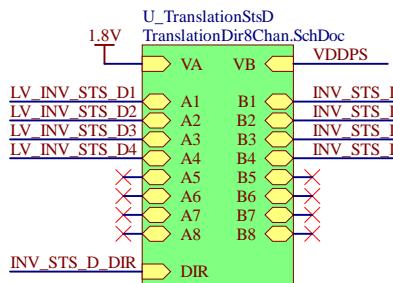
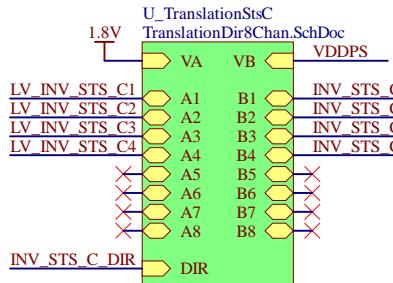
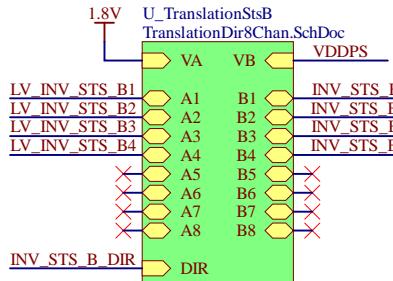
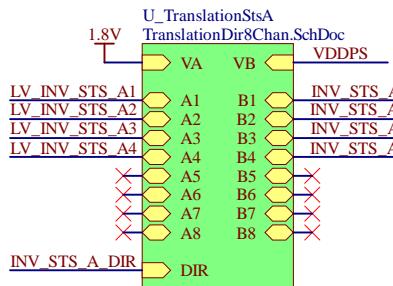
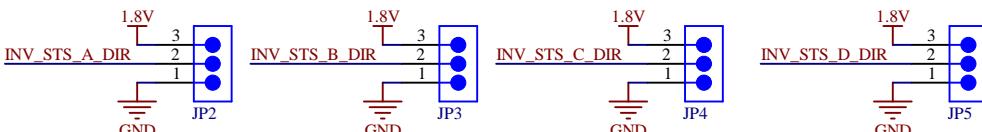
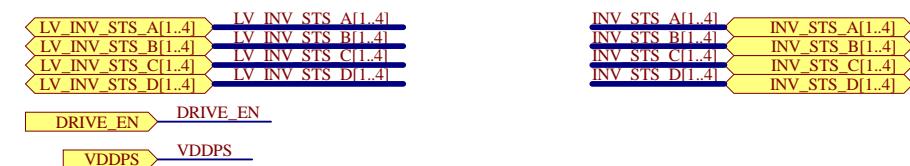
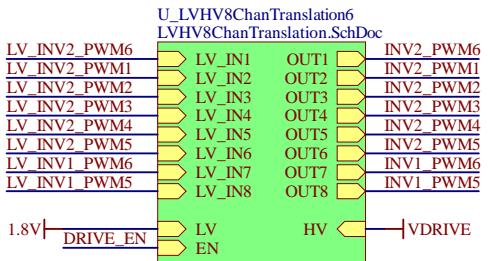
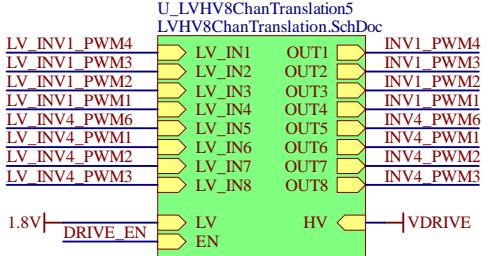
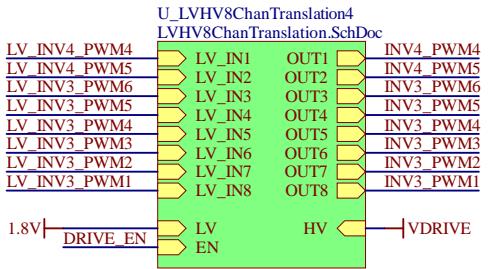
C



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Title: Inverter Connector		Severson Group WEMPEC UWMadison
File: InverterConnector.SchDoc	Sheet: 18 of 26	
Revision: A	Time: 4:08:19 PM	
Date: 8/24/2020		Engineer: Nathan Petersen

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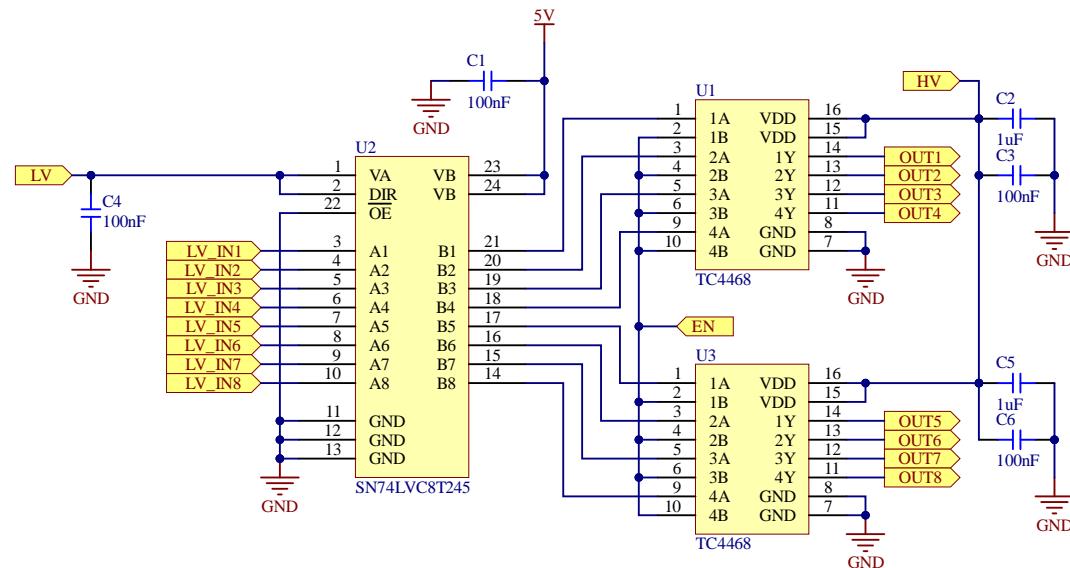
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C

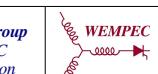
C

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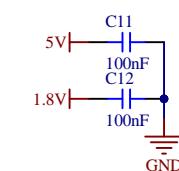
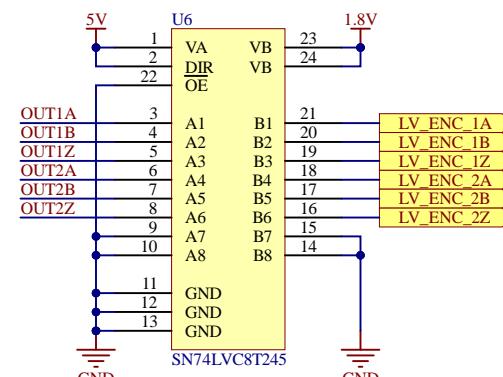
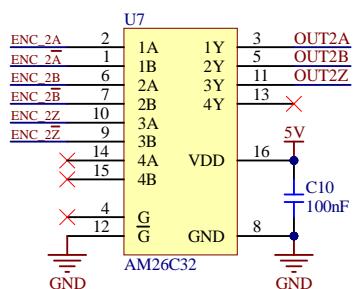
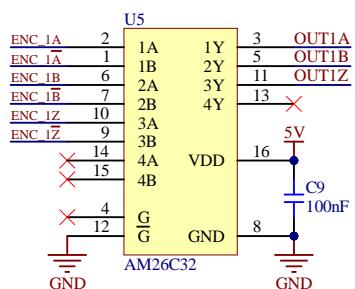
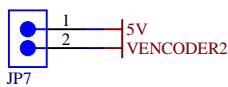
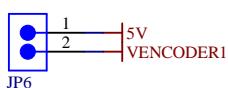
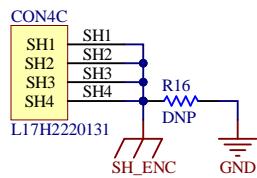
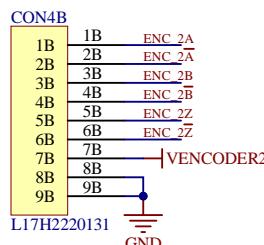
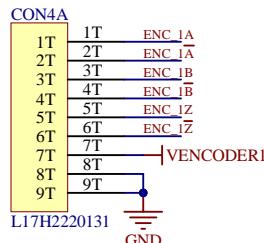
D

Title: **8-channel LV to HV Translation**File: **LVHV8ChanTranslation.SchDoc** | Sheet: 20 of 26Revision: **A** | Time: **4:08:20 PM**Date: **8/24/2020**

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Engineer: **Prasoon Sinha**

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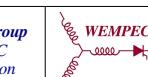
Title: **Encoders**

File: Encoder.SchDoc

Sheet: 21 of 26

Revision: A Time: 4:08:20 PM

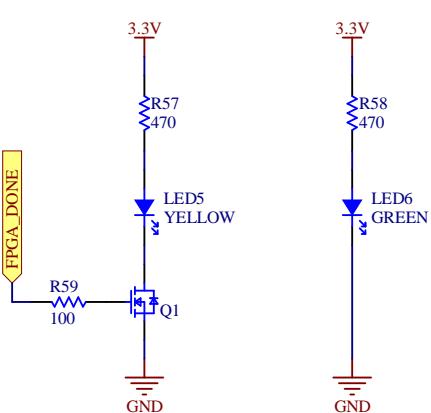
Date: 8/24/2020

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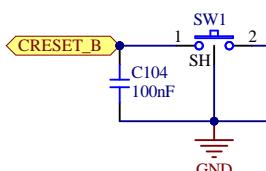
Engineer: Nathan Petersen

FPGA STATUS LEDS

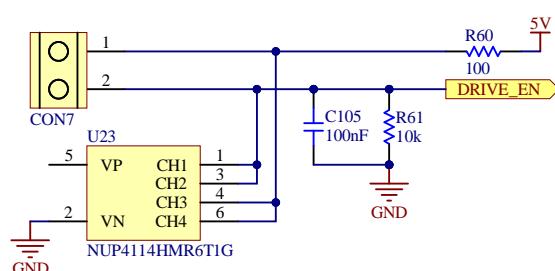
FPGA DONE



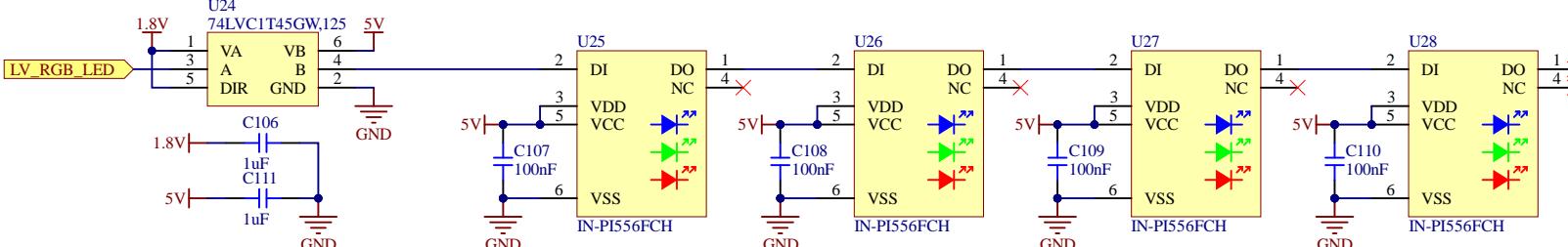
RESET BUTTON



DRIVE ENABLE (ESTOP)



FPGA RGB LEDs

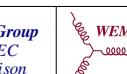


Title: **FPGA I/O Interface**

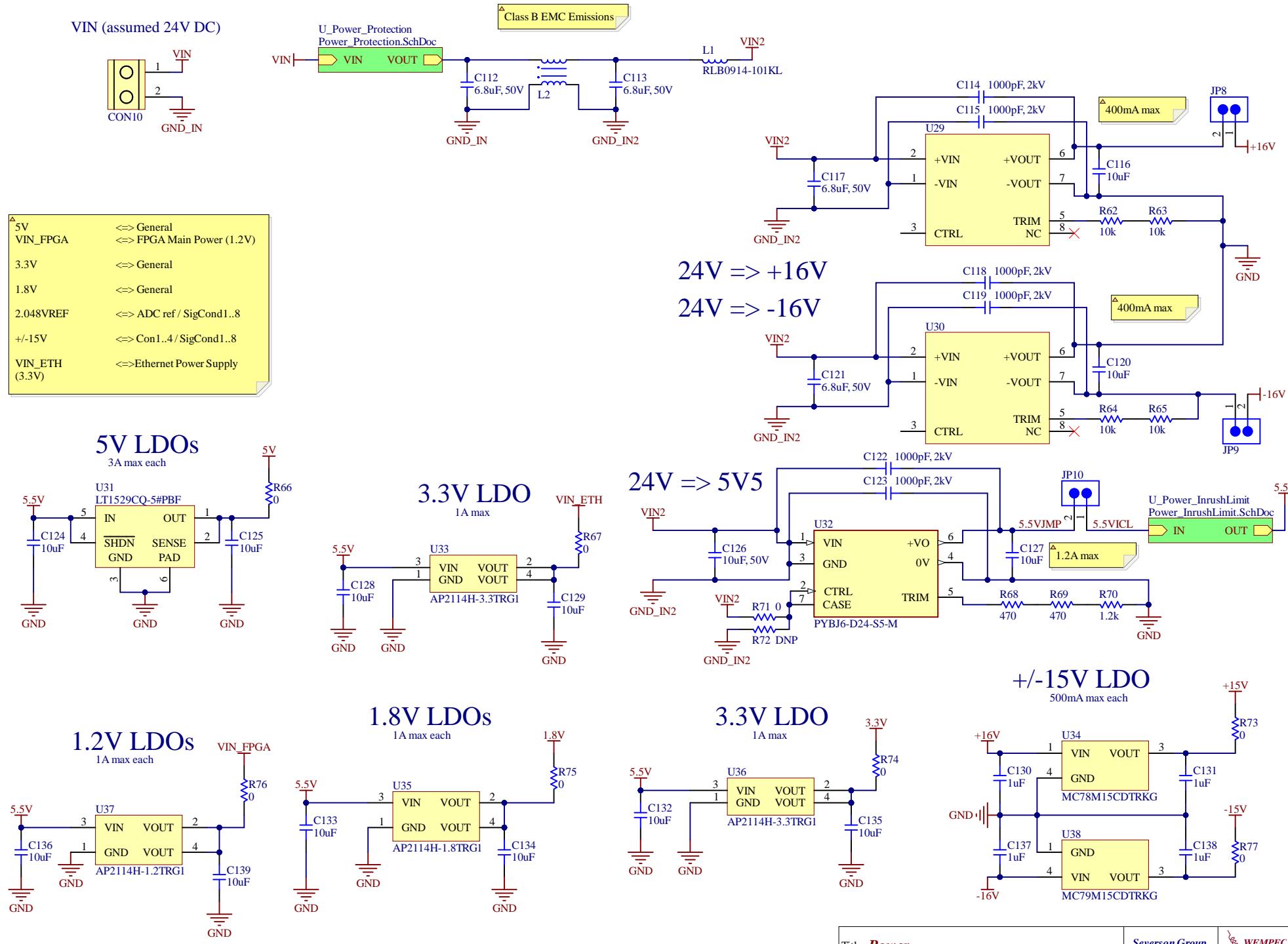
File: **FPGA_IO.SchDoc** Sheet: 22 of 26

Revision: **A** Time: 4:08:20 PM Date: 8/24/2020

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A

A

B

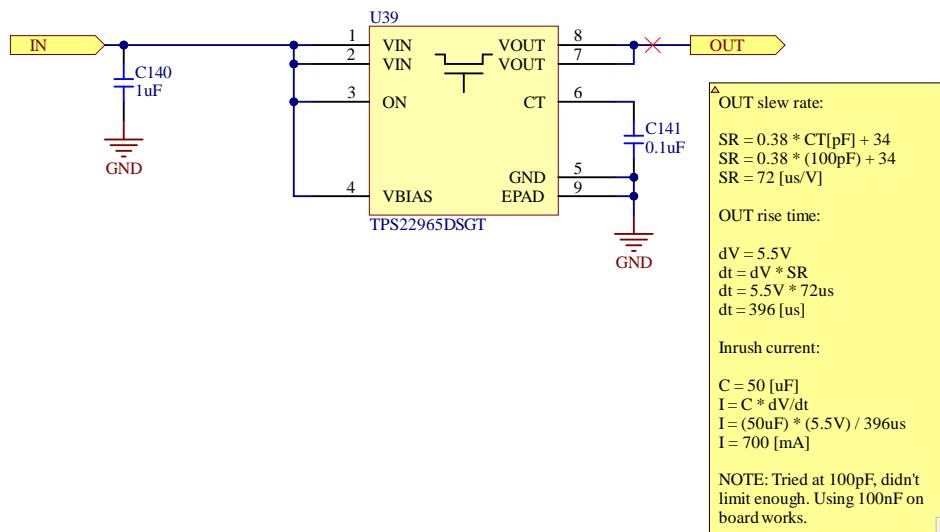
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C

C

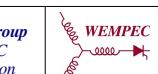
D

D

Title: **Inrush Current Limiter**

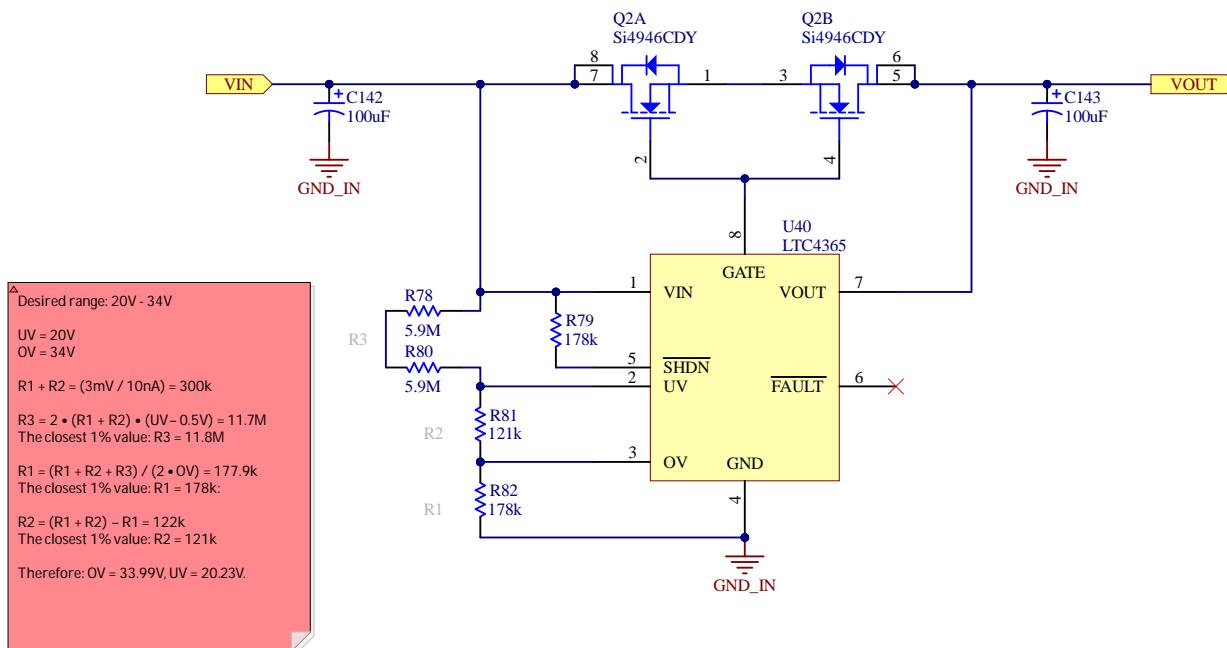
File: Power_InrushLimit.SchDoc | Sheet: 24 of 26

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A

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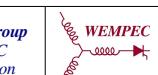
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C

C

D

D

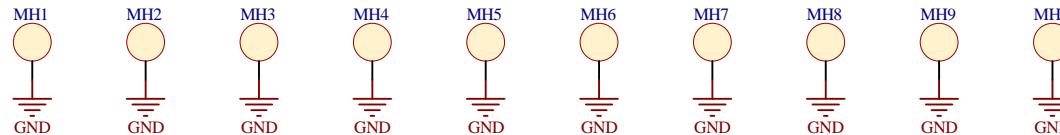
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4-40 Screws:

SCREW1 SCREW2 SCREW3 SCREW4 SCREW5 SCREW6 SCREW7 SCREW8 SCREW9 SCREW10

4-40 Standoffs:

STANDOFF1 STANDOFF2 STANDOFF3 STANDOFF4 STANDOFF5 STANDOFF6 STANDOFF7 STANDOFF8 STANDOFF9 STANDOFF10

Mouting Holes:

Title: ***Back Page***

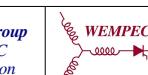
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Sheet: **26 of 26**

Revision: **A** Time: **4:08:20 PM**

Date: **8/24/2020**

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Engineer: **Nathan Petersen**