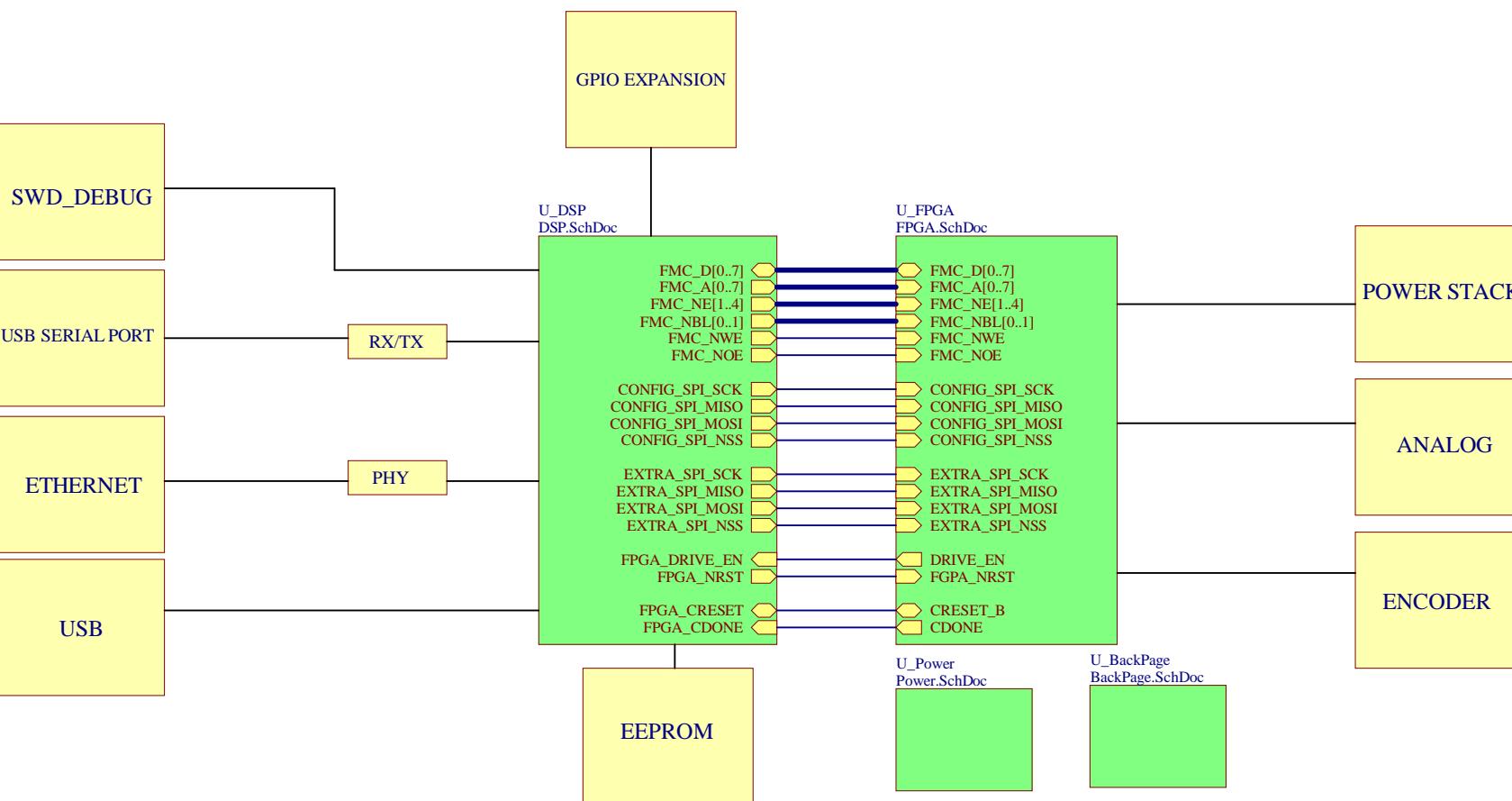


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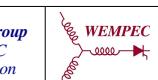
B

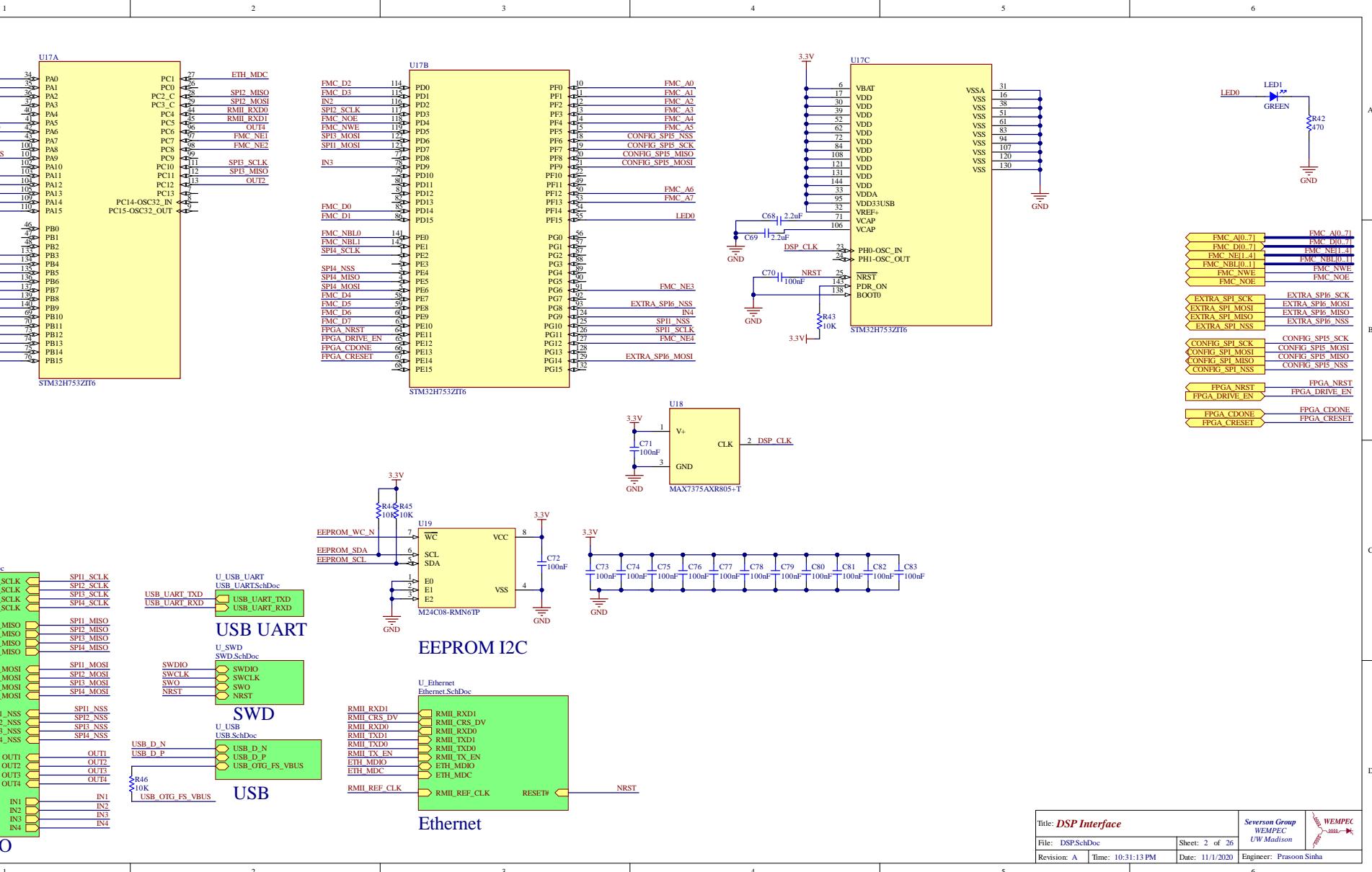
C

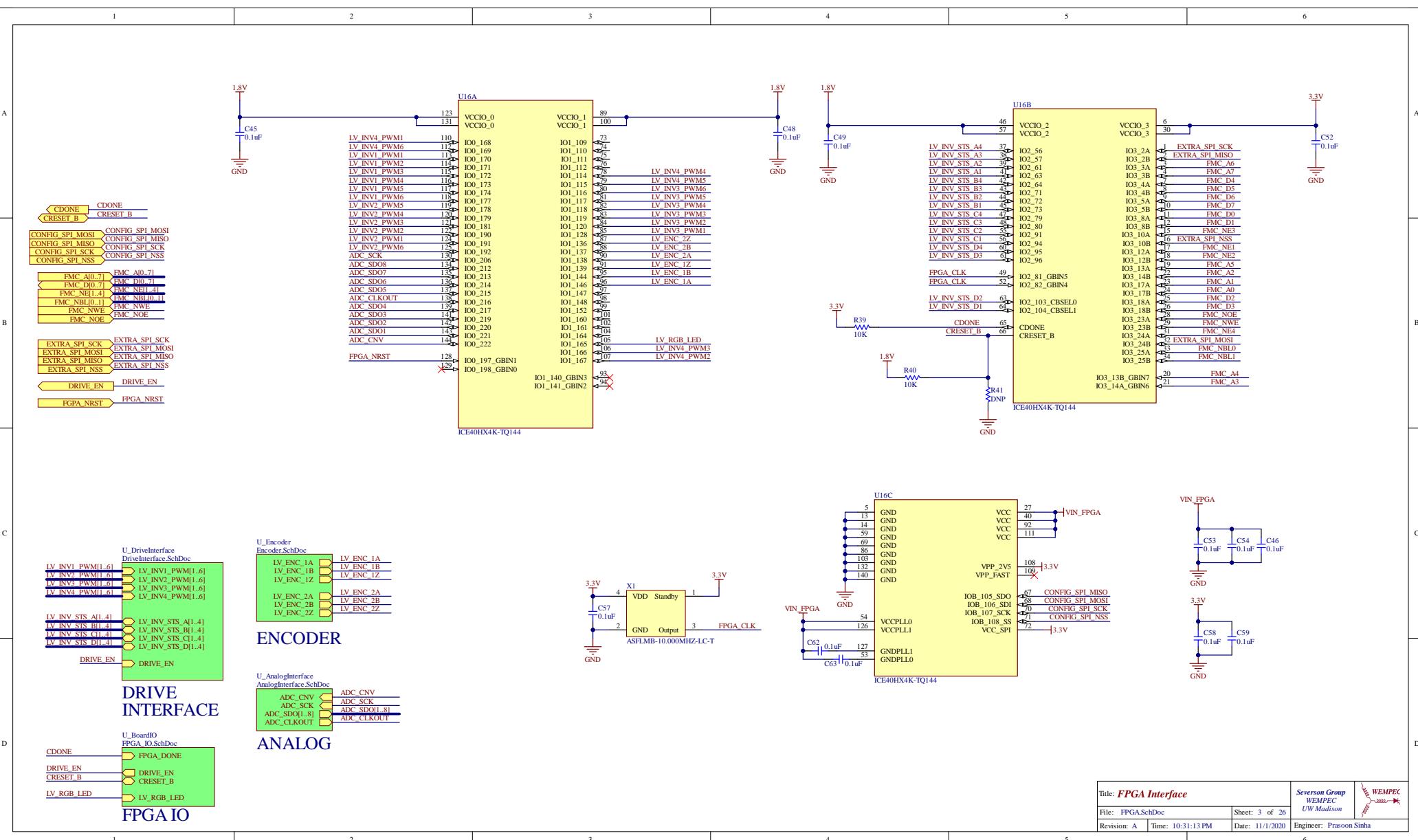
C

D

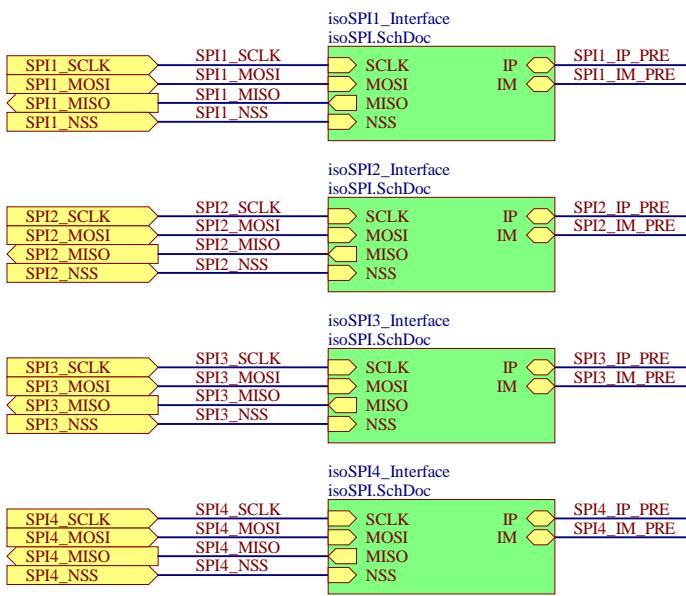
D

Title: ***uAMDC***File: ***uAMDC.SchDoc***Sheet: **1 of 26**Revision: **A**Time: **10:31:13 PM**Date: **11/1/2020**
**Severson Group**  
**WEMPEC**  
**UWMadison**
Engineer: **Prasoon Sinha**

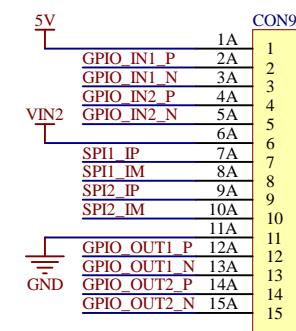
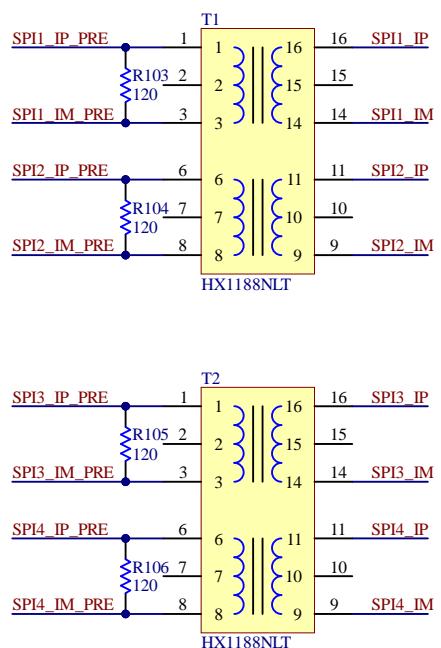




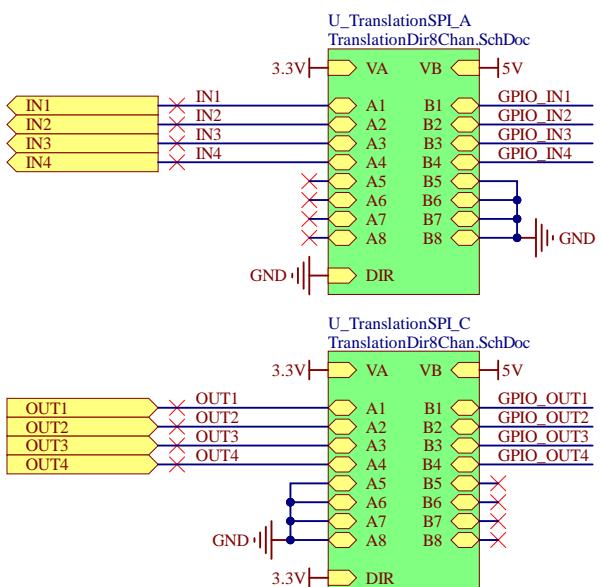
A



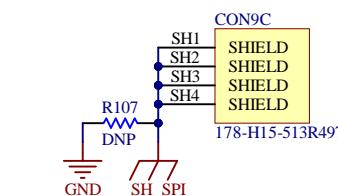
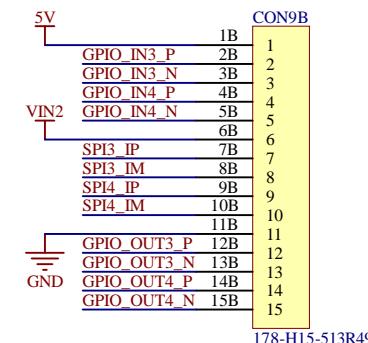
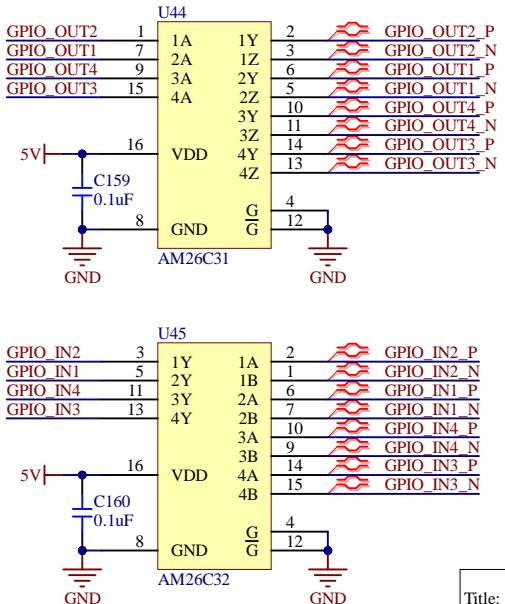
B



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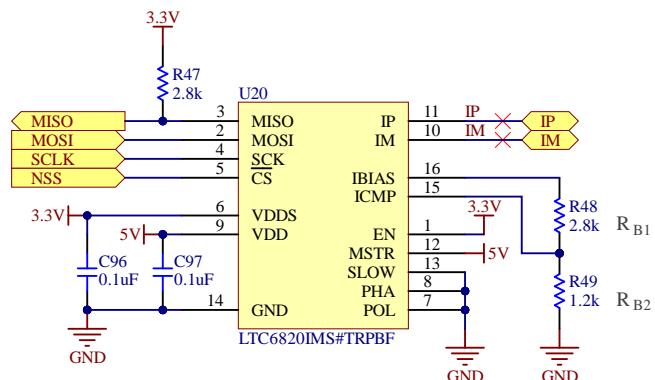
B

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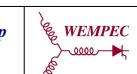
D

Title: *isoSPI Interface*

File: isoSPI.SchDoc Sheet: 5 of 26

Revision: A Time: 10:31:13 PM Date: 11/1/2020

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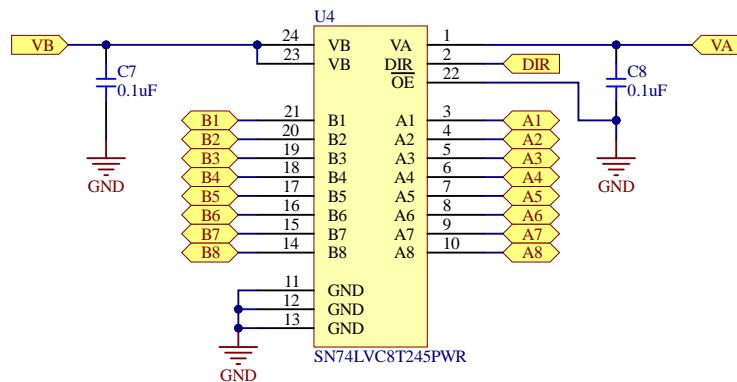
B

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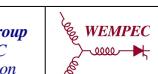
D

Title: **8-Channel Directional Translation**

File: TranslationDir8Chan.SchDoc | Sheet: 6 of 26

Revision: A | Time: 10:31:14 PM | Date: 11/1/2020

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Engineer: Nathan Petersen

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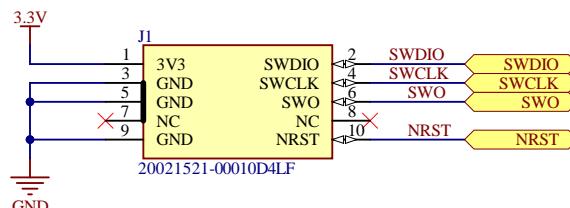
B

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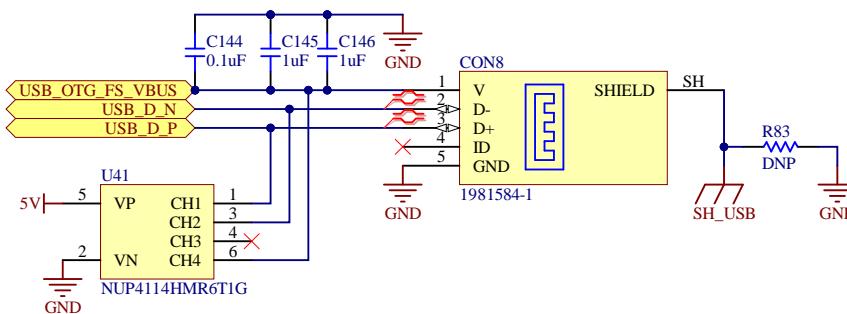
Title: <b>SWD</b>			Severson Group WEMPEC UWMadison
File: SWD.SchDoc		Sheet: 7 of 26	
Revision: A	Time: 10:31:14 PM	Date: 11/1/2020	
Engineer: Prasoon Sinha			WEMPEC

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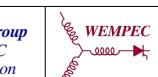
B

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Title: **USB**File: **USB.SchDoc**Sheet: **8 of 26**Revision: **A** Time: **10:31:14 PM**Date: **11/1/2020**

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**WEMPEC**  
**UWMadison**

Engineer: **Prasoon Sinha**

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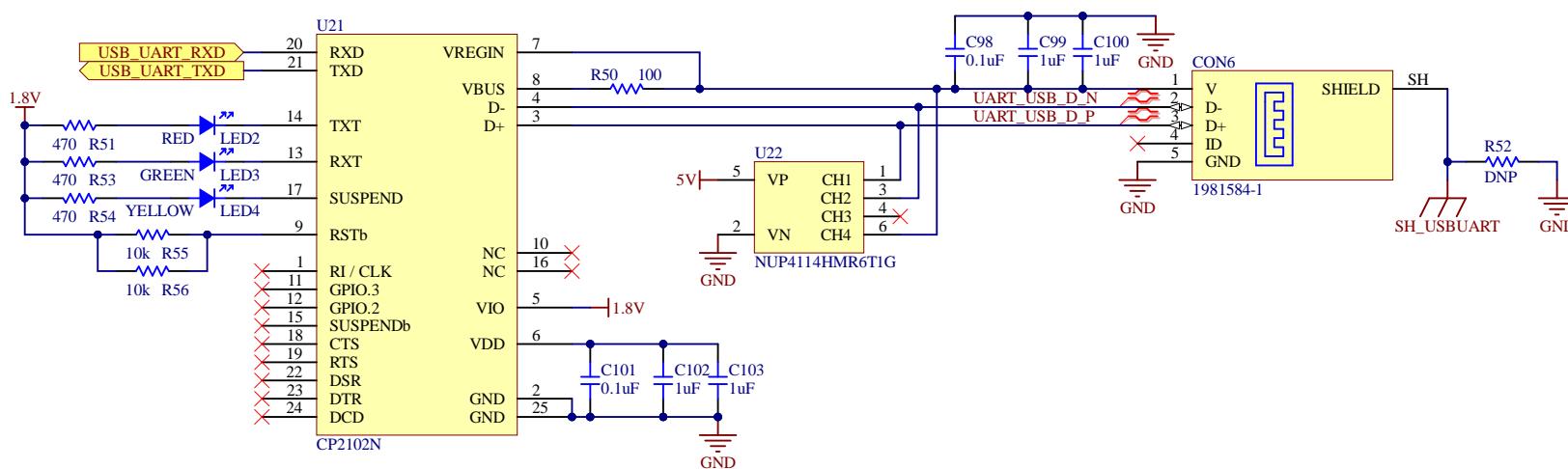
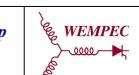
B

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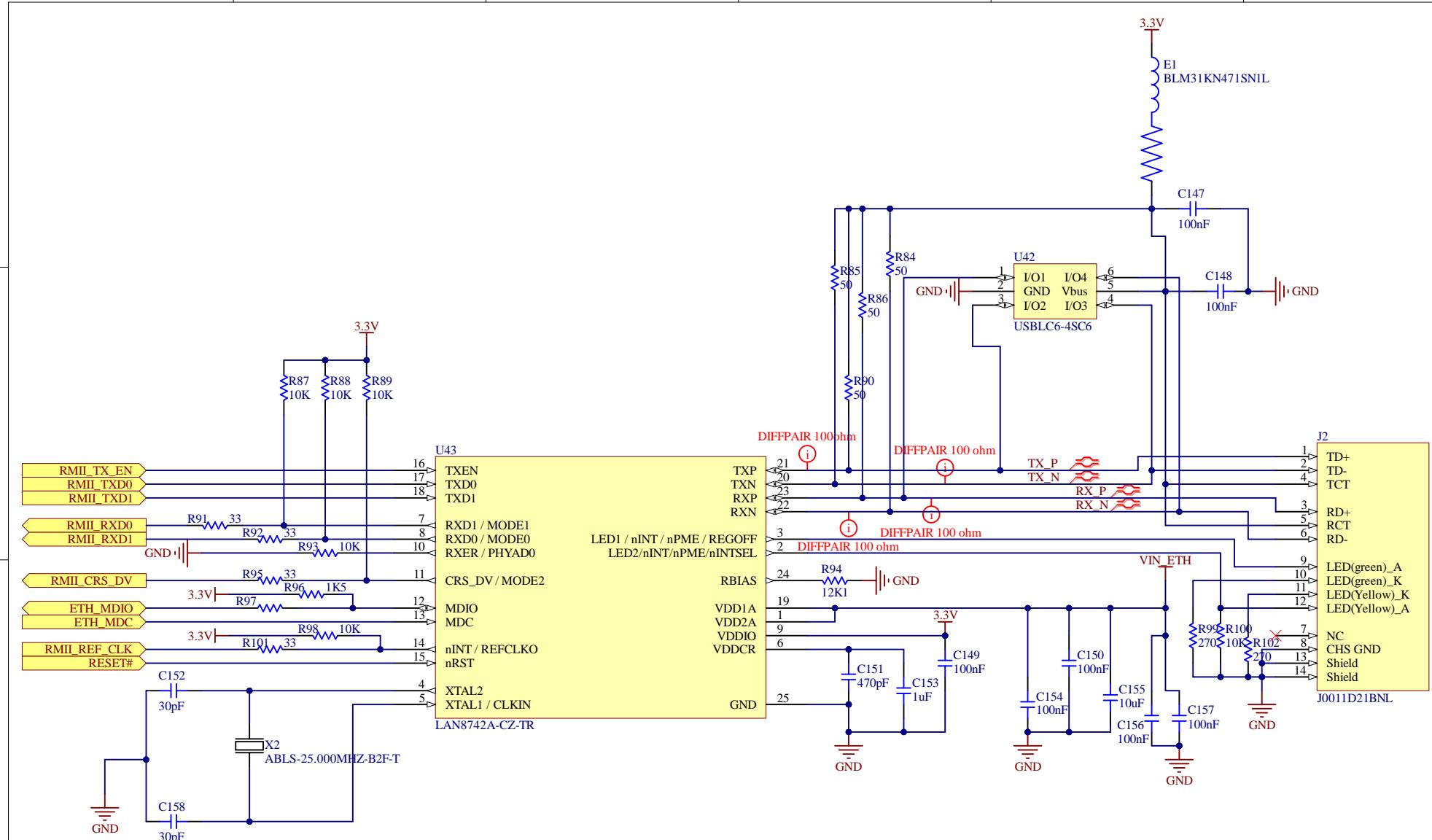
D

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Title: **USB UART**File: **USB\_UART.SchDoc**Sheet: **9 of 26**Revision: **A** Time: **10:31:14 PM**Date: **11/1/2020**
**Severson Group**  
**WEMPEC**  
**UWMadison**


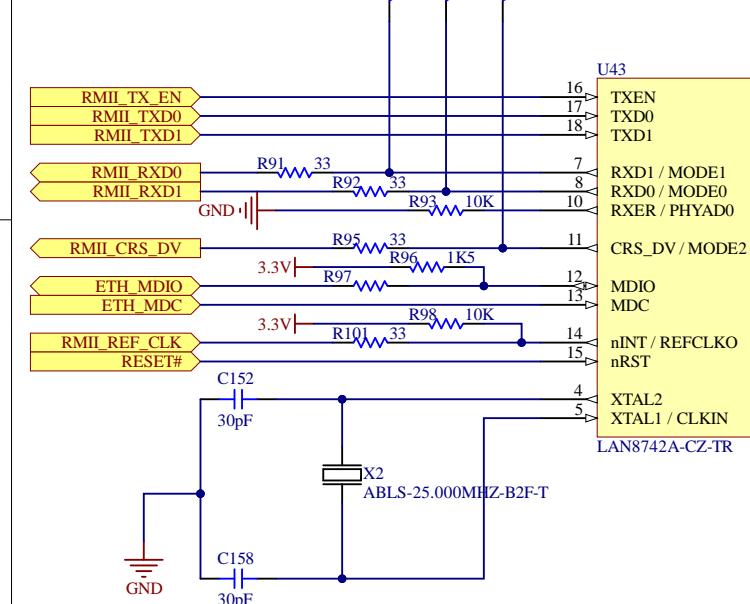
A

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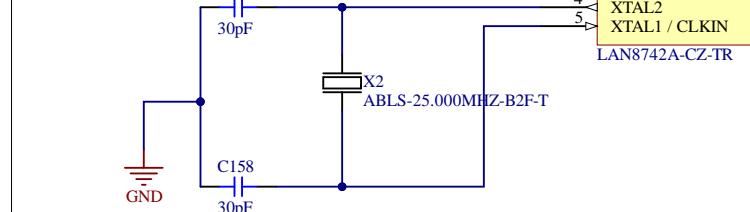
B

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Title: *Ethernet*

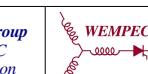
File: Ethernet.SchDoc

Sheet: 10 of 26

Revision: A Time: 10:31:14 PM

Date: 11/1/2020

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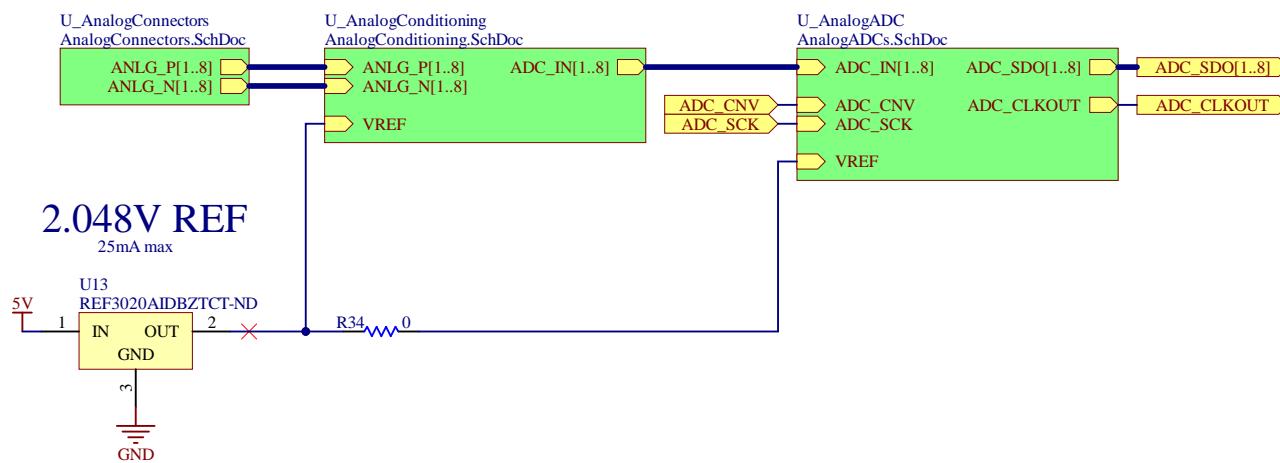
Engineer: Prasoon Sinha

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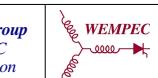
C

D

D

Title: **Analog Interface**File: **AnalogInterface.SchDoc**Sheet: **11 of 26**Revision: **A** Time: **10:31:14 PM**Date: **11/1/2020** Engineer: **Nathan Petersen**

**Severson Group**  
**WEMPEC**  
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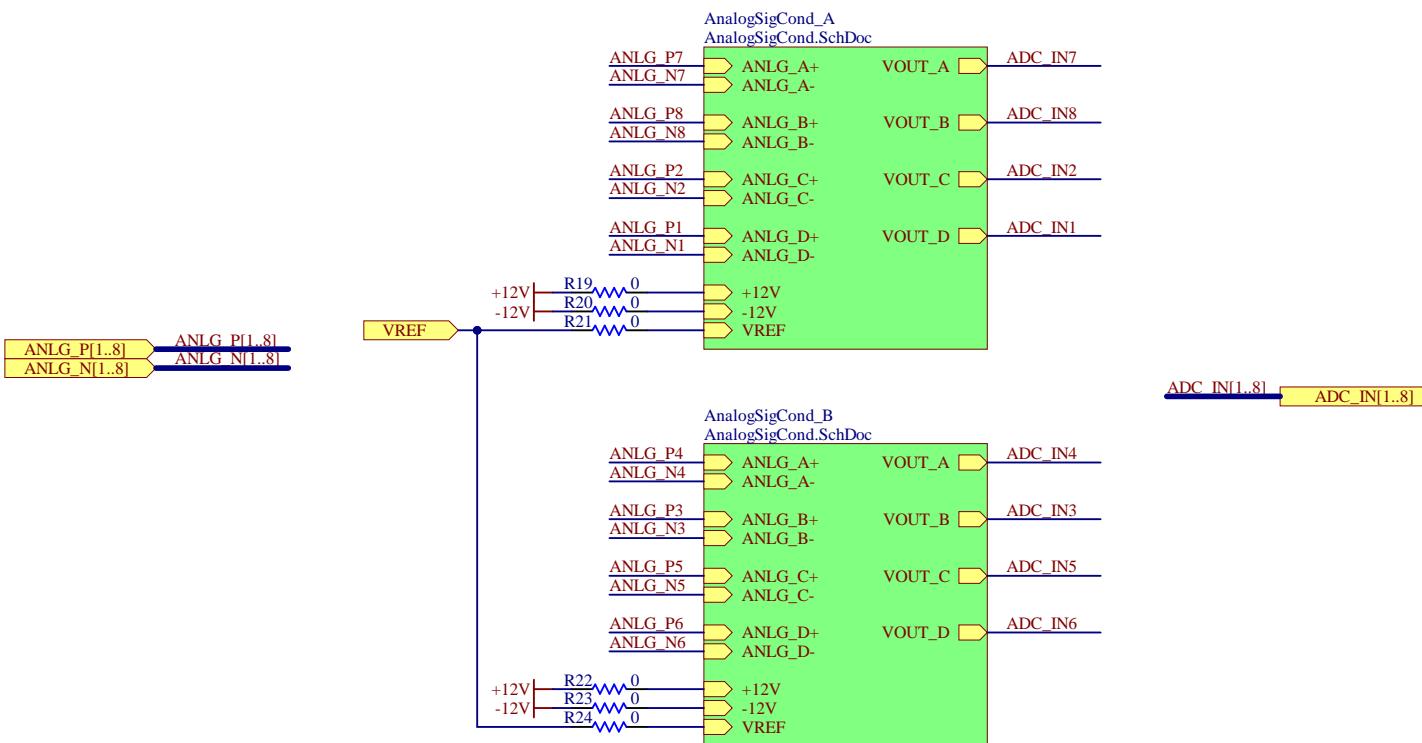
B

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C

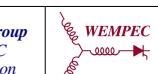
D

D

Title: *Analog Signal Conditioning*File: *AnalogConditioning.SchDoc* Sheet: 13 of 26

Revision: A Time: 10:31:16 PM Date: 11/1/2020

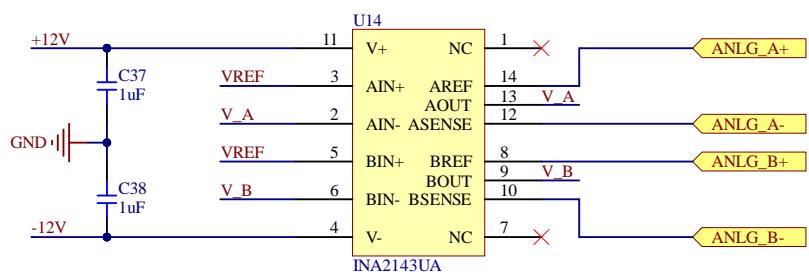
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UWMadison



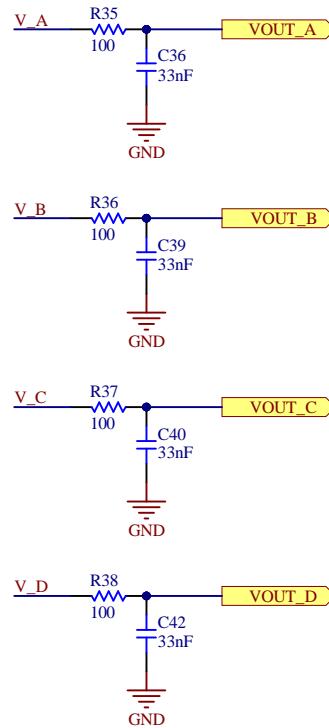
Engineer: Nathan Petersen

A

A

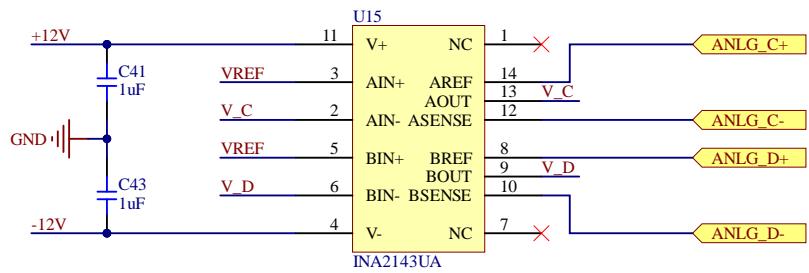


△ LPF: fc = 50kHz



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Title: **Analog Signal Front-End**

File: **AnalogSigCond.SchDoc**

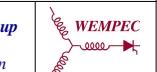
Sheet: **14 of 26**

Revision: **A**

Time: **10:31:16 PM**

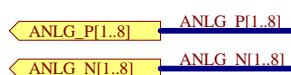
Date: **11/1/2020**

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Engineer: **Nathan Petersen**

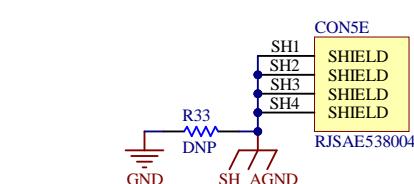
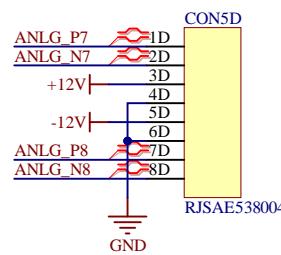
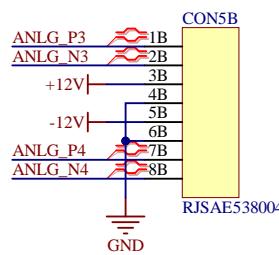
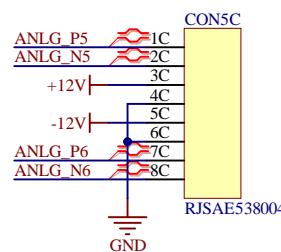
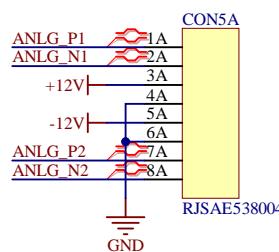
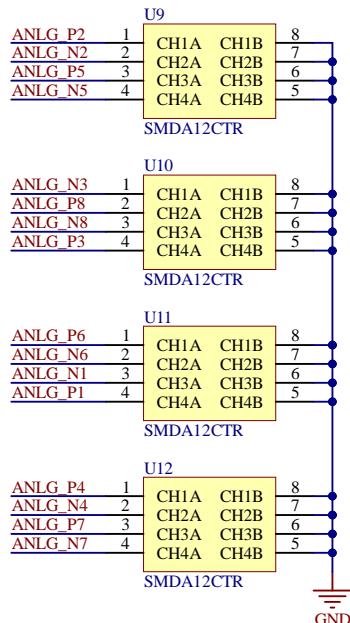
A



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### ESD Protection



Force no input to 0V

ANLG_P1	R25 100k	ANLG_N1
ANLG_P2	R26 100k	ANLG_N2
ANLG_P3	R27 100k	ANLG_N3
ANLG_P4	R28 100k	ANLG_N4
ANLG_P5	R29 100k	ANLG_N5
ANLG_P6	R30 100k	ANLG_N6
ANLG_P7	R31 100k	ANLG_N7
ANLG_P8	R32 100k	ANLG_N8

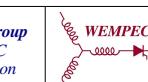
D

Title: **Analog RJ45 Connectors**

File: **AnalogConnectors.SchDoc** | Sheet: **15 of 26**

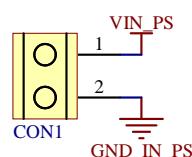
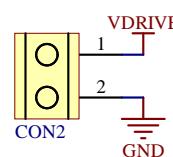
Revision: **A** | Time: **10:31:16 PM** | Date: **11/1/2020**

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**WEMPEC**  
**UWMadison**

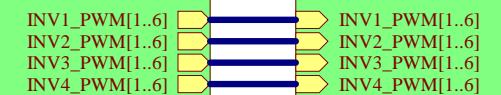
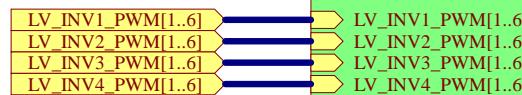


Engineer: **Nathan Petersen**

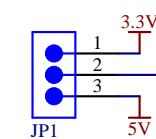
A

**POWERSTACK VIN****VDRIVE**

B

**U\_InverterTranslation  
InverterTranslation.SchDoc****U\_InverterConnectors  
InverterConnectors.SchDoc**

C

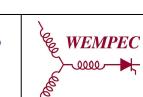


DRIVE\_EN

INV\_STS\_D[1..4]

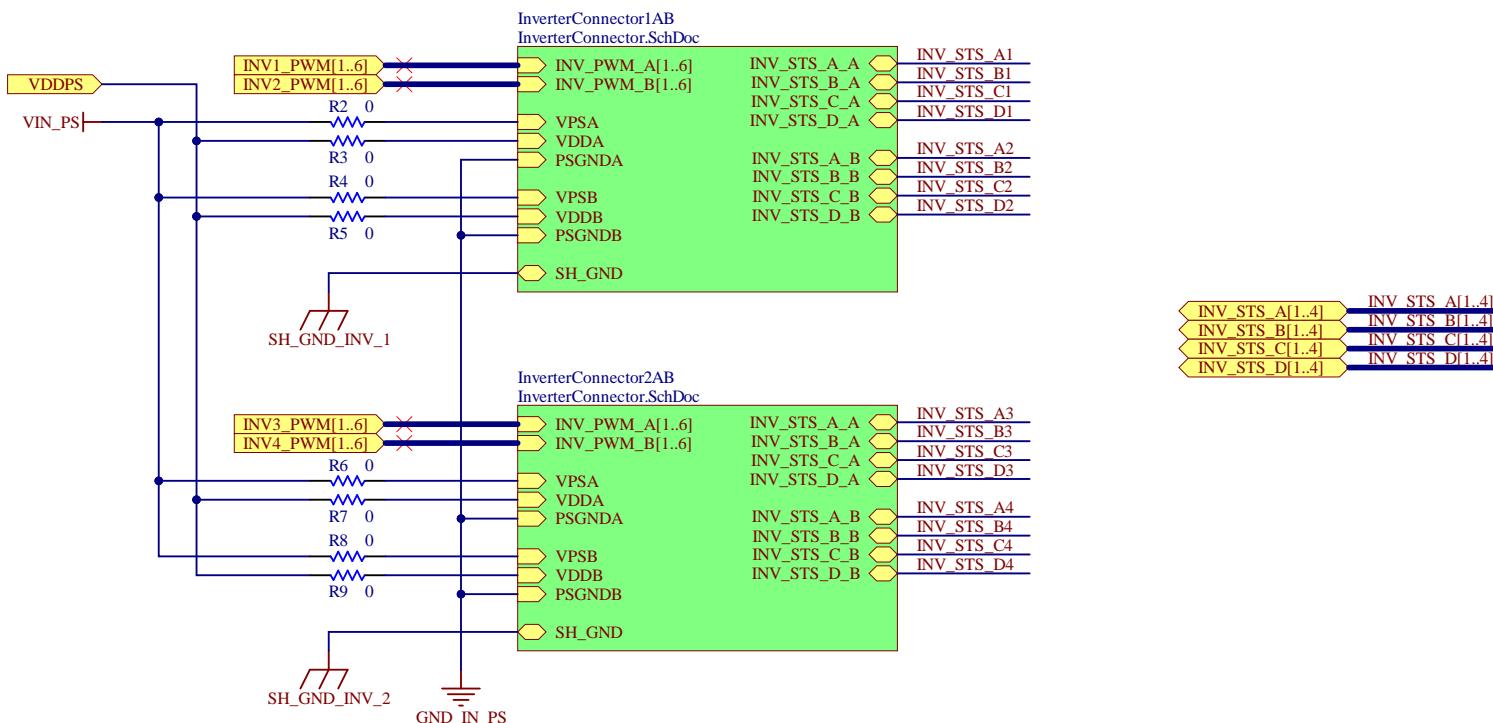
VDDPS

D

Title: **DriveInterface**File: **DriveInterface.SchDoc**Sheet: **16 of 26****Severson Group  
WEMPEC  
UW Madison**Revision: **A** Time: **10:31:16 PM**Date: **11/1/2020**Engineer: **Prasoon Sinha**

A

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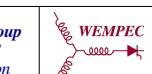
D

D

Title: **Inverter Connectors**

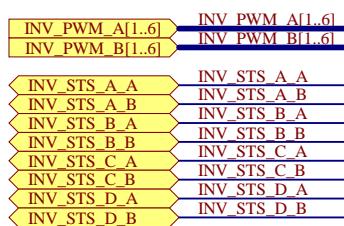
File: InverterConnectors.SchDoc | Sheet: 17 of 26

Revision: A | Time: 10:31:18 PM | Date: 11/1/2020

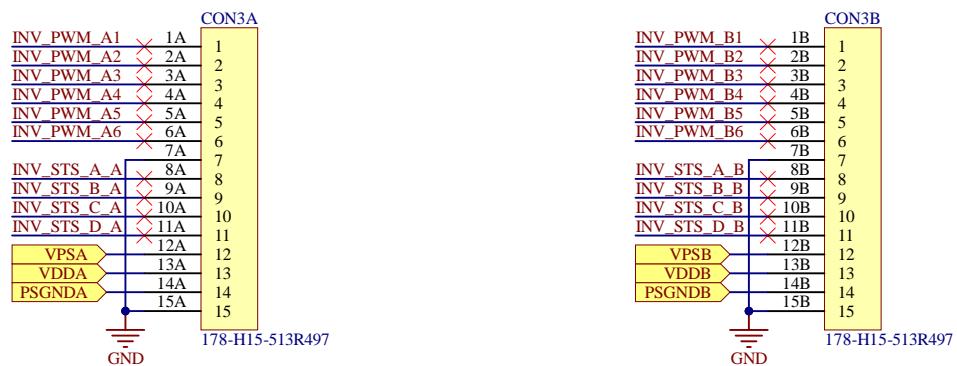
Severson Group  
WEMPEC  
UWMadison

Engineer: Nathan Petersen

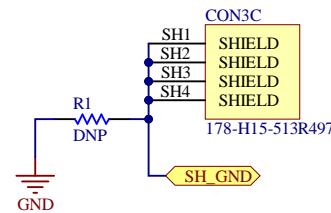
A



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Title: <b>Inverter Connector</b>			Severson Group WEMPEC UWMadison	
File: InverterConnector.SchDoc				
Sheet: 18 of 26				
Revision: A	Time: 10:31:18 PM	Date: 11/1/2020	Engineer: Nathan Petersen	

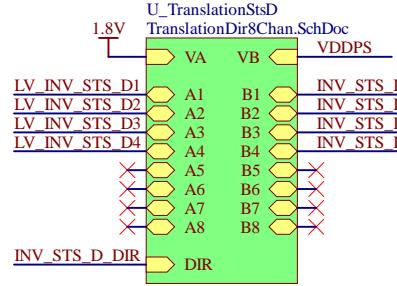
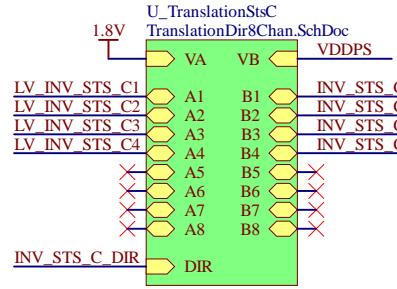
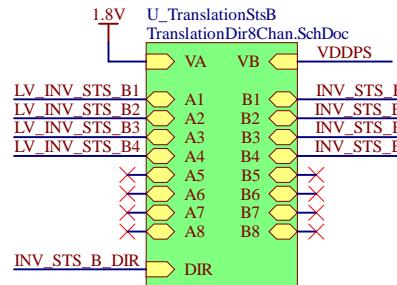
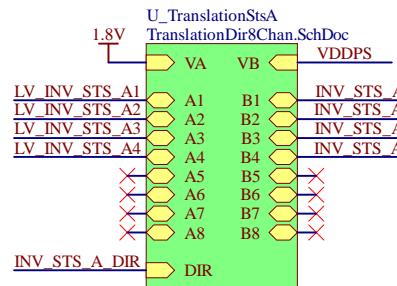
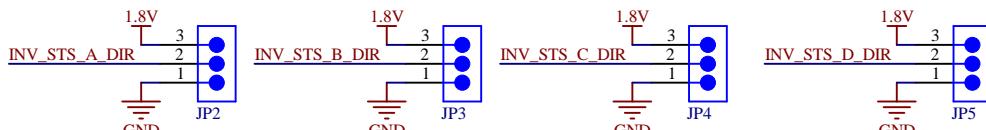
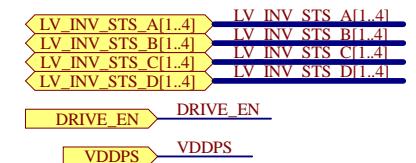
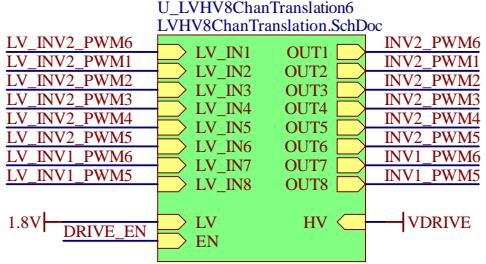
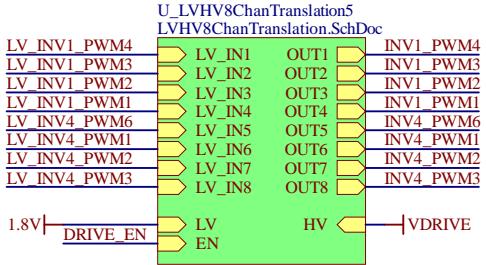
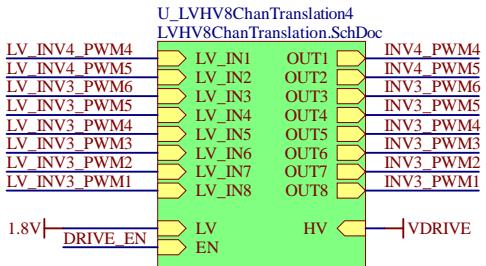
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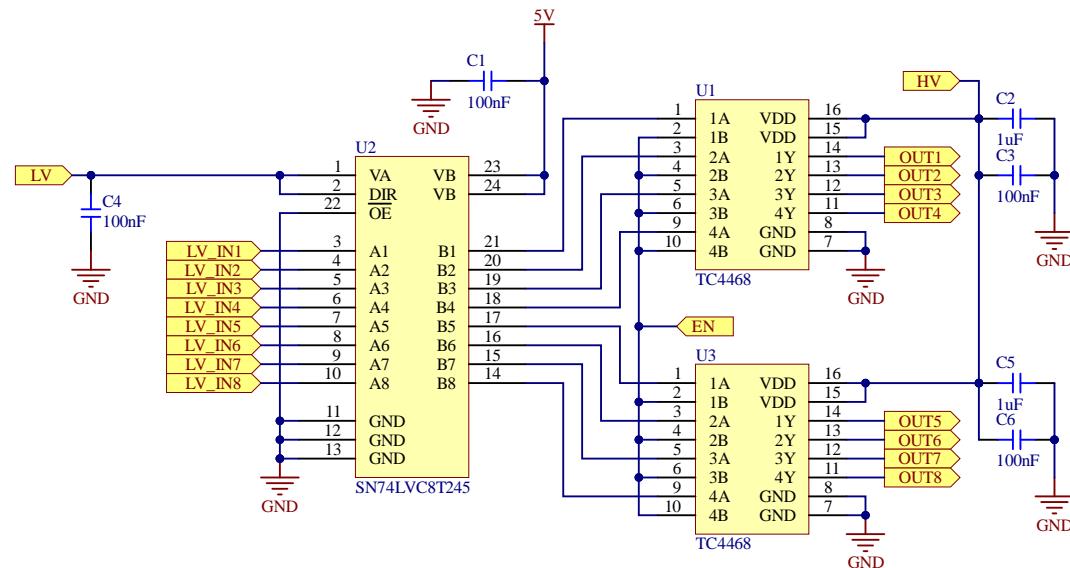
B

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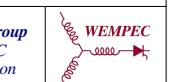
C

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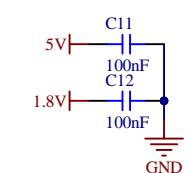
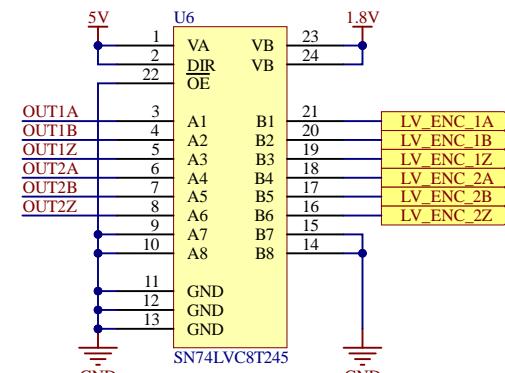
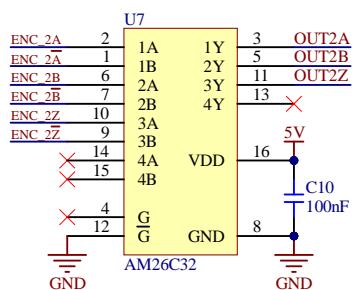
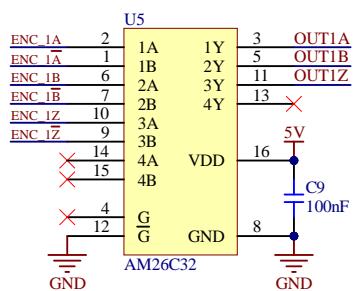
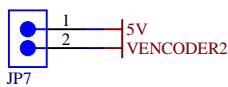
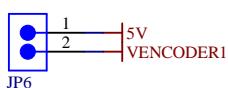
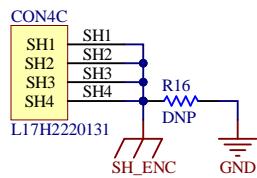
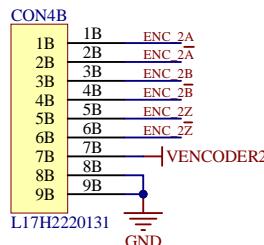
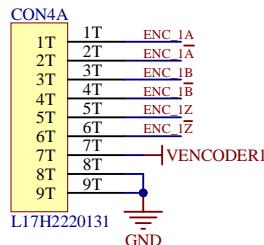
D

Title: **8-channel LV to HV Translation**File: **LVHV8ChanTranslation.SchDoc** | Sheet: **20 of 26**Revision: **A** | Time: **10:31:21 PM** | Date: **11/1/2020**

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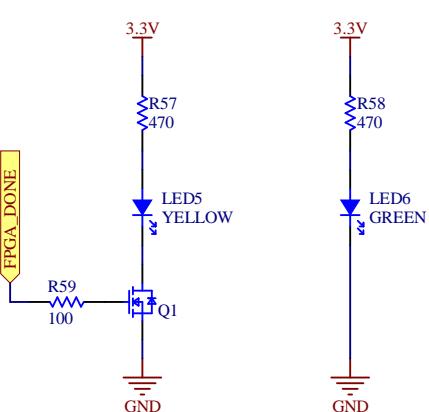
Engineer: **Prasoon Sinha**

A

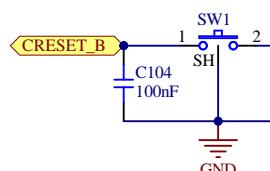


## FPGA STATUS LEDS

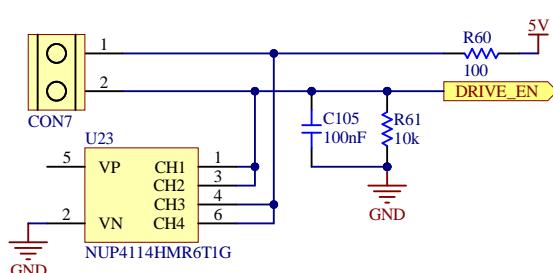
### FPGA DONE



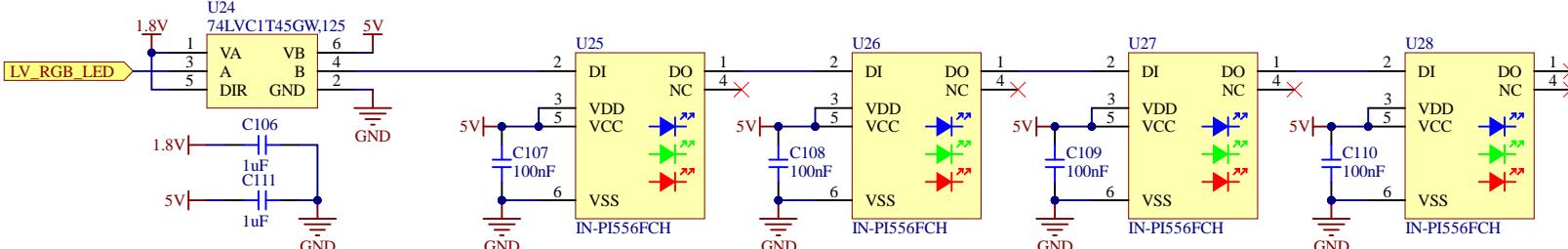
## RESET BUTTON



## DRIVE ENABLE (ESTOP)



## FPGA RGB LEDs

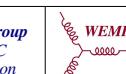


Title: **FPGA I/O Interface**

File: **FPGA\_Io.SchDoc** Sheet: **22 of 26**

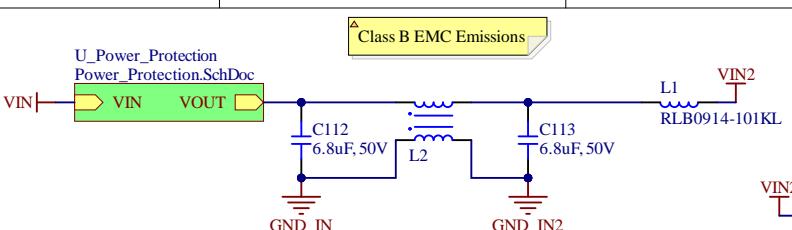
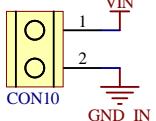
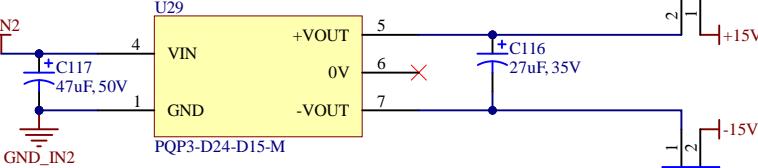
Revision: **A** Time: **10:31:21 PM** Date: **11/1/2020**

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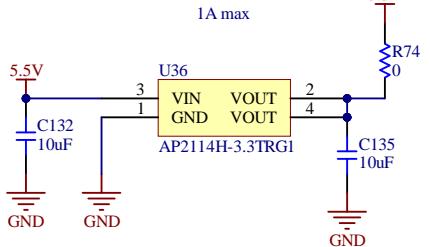
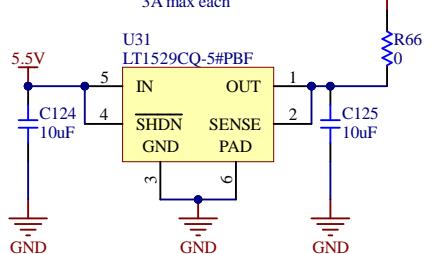
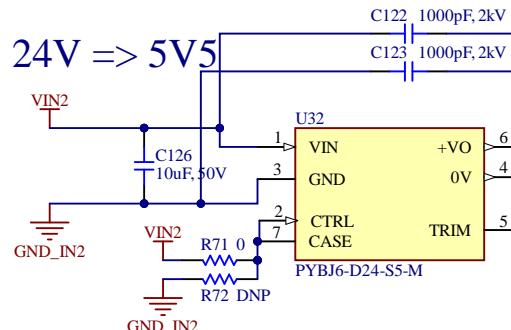
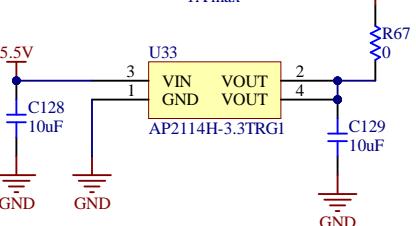
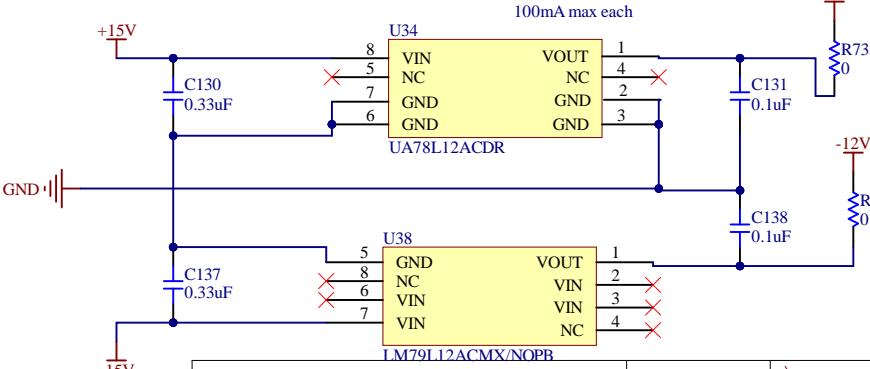
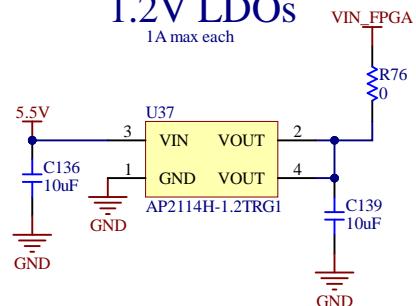
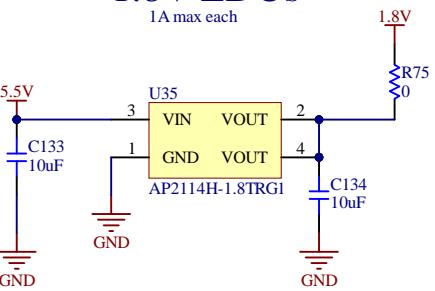


Engineer: **Prasoon Sinha**

VIN (assumed 24V DC)


 $24V \Rightarrow +15V$   
 $24V \Rightarrow -15V$ 


<b>A</b>	5V VIN_FPGA	<=> General <=> FPGA Main Power (1.2V)
	3.3V	<=> General
	1.8V	<=> General
	2.048VREF	<=> ADC ref / SigCond1..8
	+/-15V	<=> Con1..4 / SigCond1..8
	VIN_ETH (3.3V)	<=> Ethernet Power Supply

**3.3V LDO****5V LDOs****3.3V LDO****+/- 12V LDO****1.2V LDOs****1.8V LDOs**

A

A

B

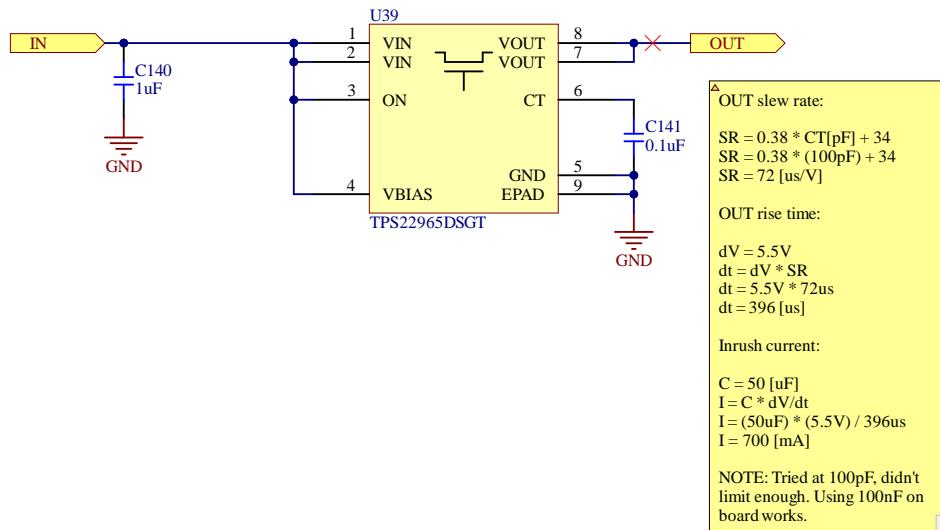
B

C

C

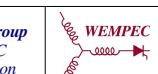
D

D

Title: **Inrush Current Limiter**

File: Power\_InrushLimit.SchDoc | Sheet: 24 of 26

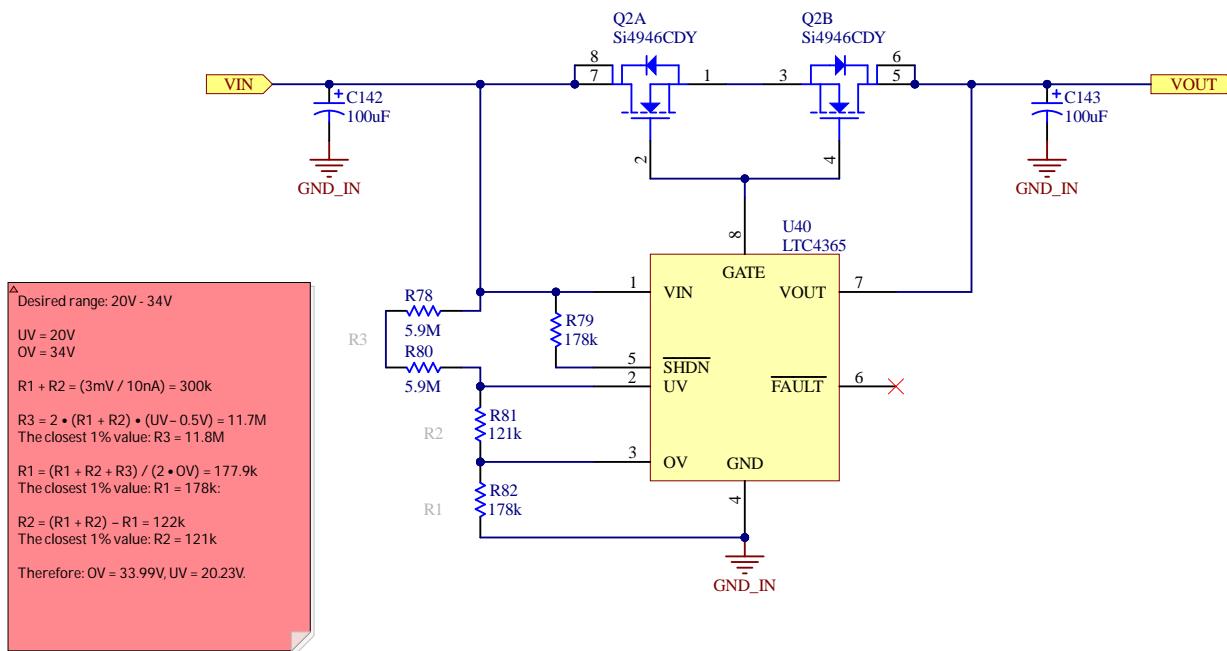
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A

A



B

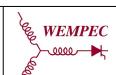
B

C

C

D

D

Title: **Power Protection**File: **Power\_Protection.SchDoc**Sheet: **25 of 26**Revision: **A** Time: **10:31:21 PM**Date: **11/1/2020** Engineer: **Nathan Petersen****Severson Group**  
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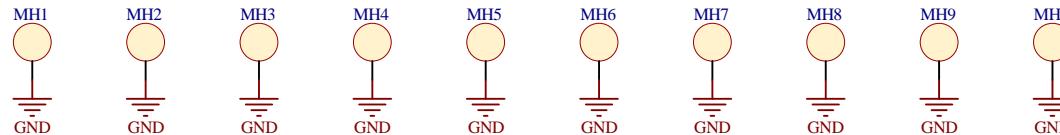
A

**4-40 Screws:**

SCREW1 SCREW2 SCREW3 SCREW4 SCREW5 SCREW6 SCREW7 SCREW8 SCREW9 SCREW10

**4-40 Standoffs:**

STANDOFF1 STANDOFF2 STANDOFF3 STANDOFF4 STANDOFF5 STANDOFF6 STANDOFF7 STANDOFF8 STANDOFF9 STANDOFF10

**Mouting Holes:**

C

C

D

D

Title: ***Back Page***

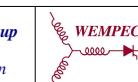
File: **BackPage.SchDoc**

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Date: **11/1/2020**

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