

RGB LED, 4x switches, 1x button, E-STOP



BOARD I/O

24 channels
5V/3.3V
I/O



GPIO

16 channels
+/-10V diff.
pair inputs



ANALOG
INPUTS

48 channels
(8 full
inverters)



DRIVE
OUTPUTS

Quadrature
input (A,B,Z)



ENCODER

PicoZed

7030

U_PicoZed
PicoZed.SchDoc

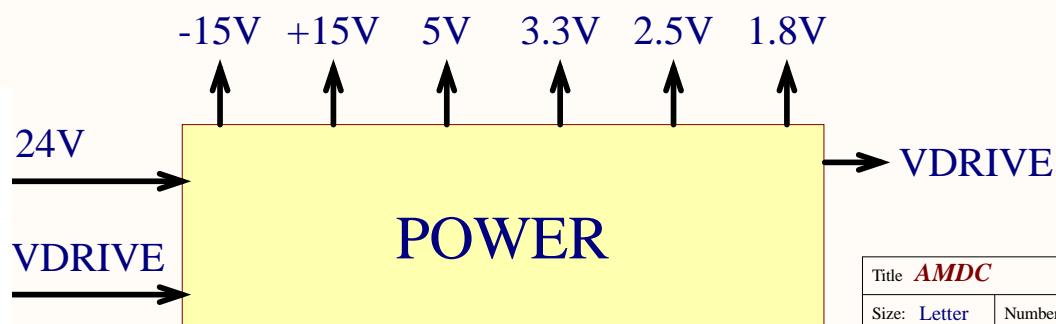
JTAG

ETHERNET

USB OTG

USB UART

Power inputs
to board



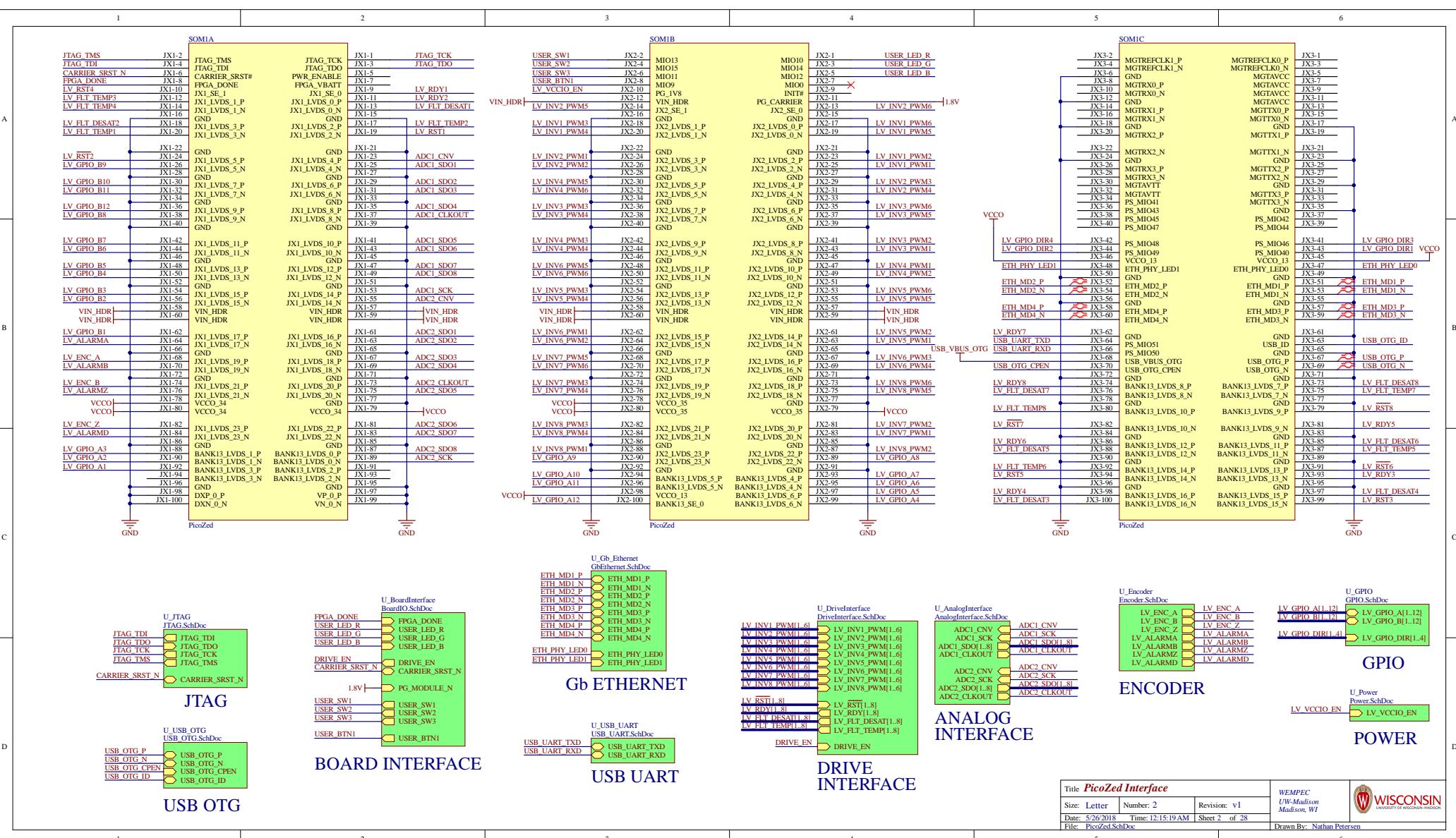
Title **AMDC**

Size:	Letter	Number:	1	Revision:	v1
Date:	5/26/2018	Time:	12:15:18 AM	Sheet:	1 of 28
File:	AMDC.SchDoc				

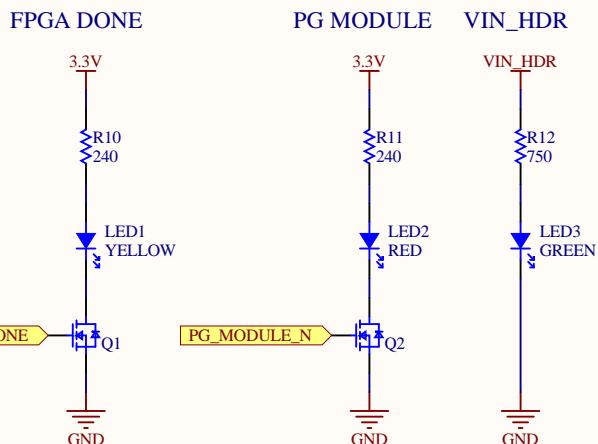
WEMPEC
UW-Madison
Madison, WI



Drawn By: Nathan Petersen

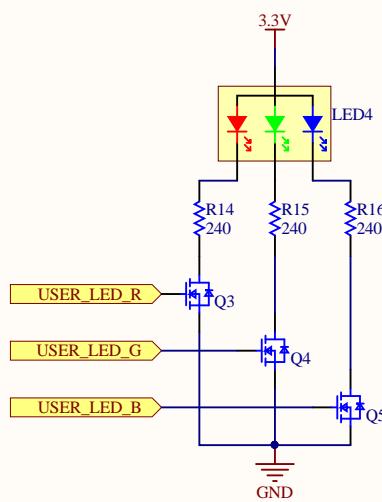
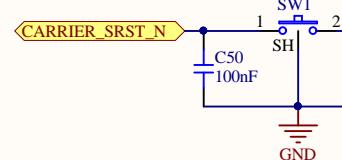


STATUS LEDS

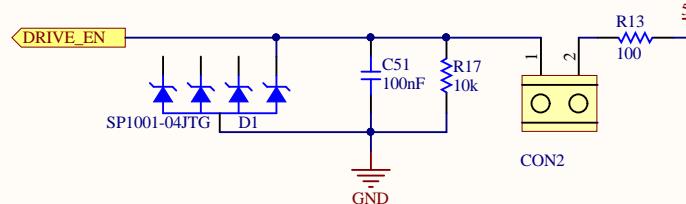


CONTROL BUTTON

CARRIER_SRST_N

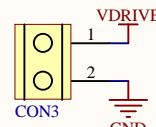


DRIVE ENABLE (ESTOP)

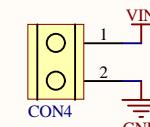


POWER CONNECTORS

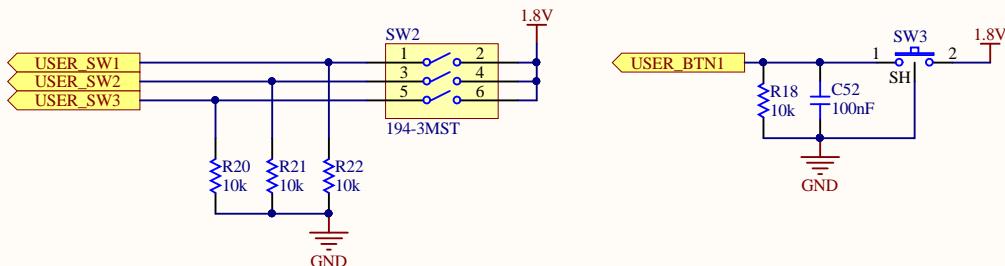
VDRIVE



VIN (assumed 24V DC)



USER INPUT



Title Board I/O

Size: Letter Number: 3 Revision: v1

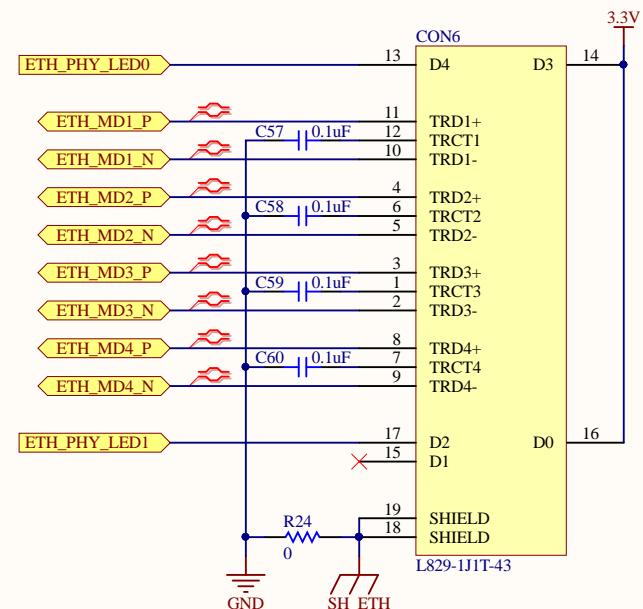
Date: 5/26/2018 Time: 12:15:19 AM Sheet 3 of 28

File: BoardIO.SchDoc

WEMPEC
UW-Madison
Madison, WI



Drawn By: Nathan Petersen



Title ***SoM Gb Ethernet***

Size: Letter	Number: 4	Revision: v1
Date: 5/26/2018	Time: 12:15:19 AM	Sheet 4 of 28
File: GbEthernet.SchDoc		Drawn By: Nathan Petersen

WEMPEC
UW-Madison
Madison, WI



A

A

B

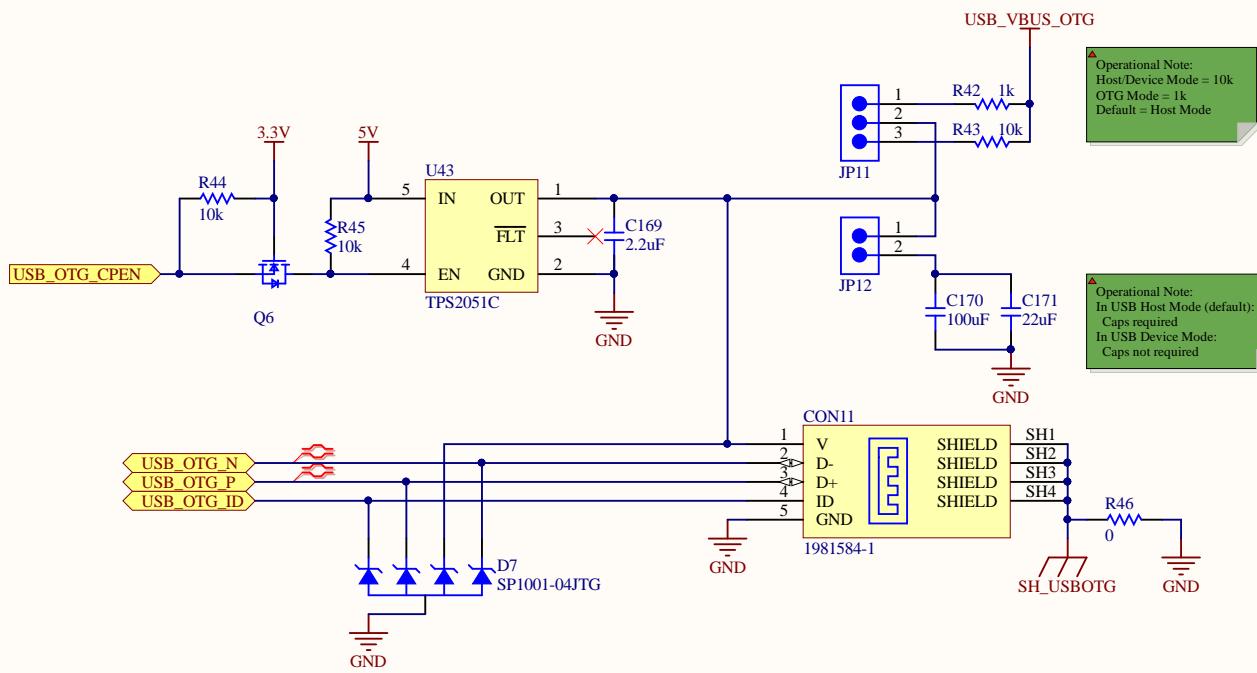
B

C

C

D

D


Title *USB OTG*

Size: Letter	Number: 5	Revision: v1
Date: 5/26/2018	Time: 12:15:20 AM	Sheet 5 of 28
File: USB_OTG.SchDoc		Drawn By: Nathan Petersen

WEMPEC
UW-Madison
Madison, WI

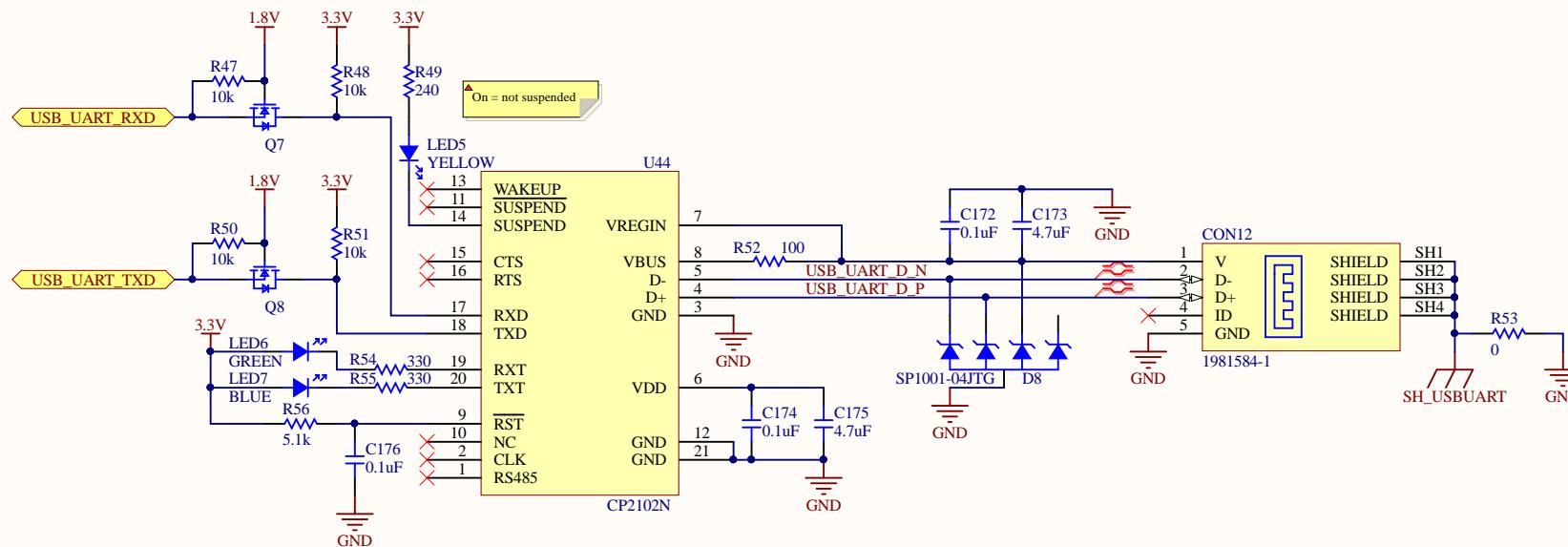

A

10

B

C

D



Title USB UART			<i>WEMPEC UW-Madison Madison, WI</i>	 WISCONSIN UNIVERSITY OF WISCONSIN-MADISON
Size: Letter	Number: 6	Revision: v1		
Date: 5/26/2018	Time: 12:15:20 AM	Sheet 6 of 28		
File: USB_UART.SchDoc			Drawn By: Nathan Petersen	

A

A

B

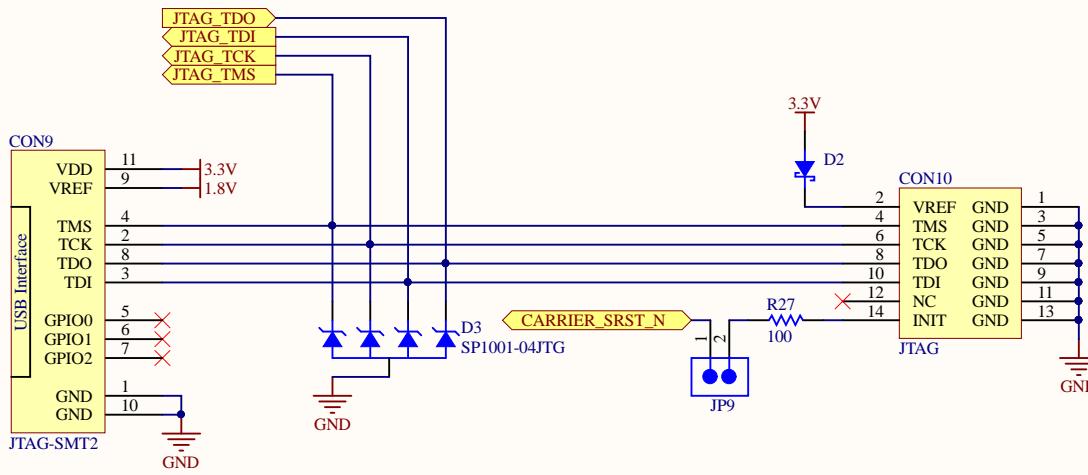
B

C

C

D

D



Title JTAG			WEMPEC UW-Madison Madison, WI	Drawn By: Nathan Petersen
Size: Letter	Number: 7	Revision: v1		
Date: 5/26/2018	Time: 12:15:20 AM	Sheet 7 of 28		
File: JTAG.SchDoc				

A

A

B

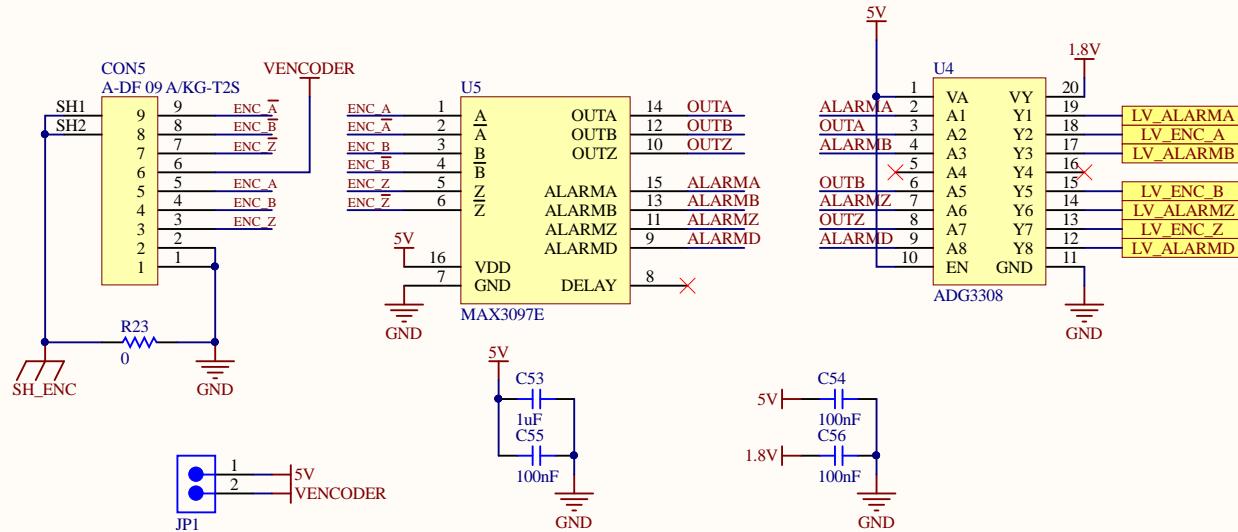
B

C

C

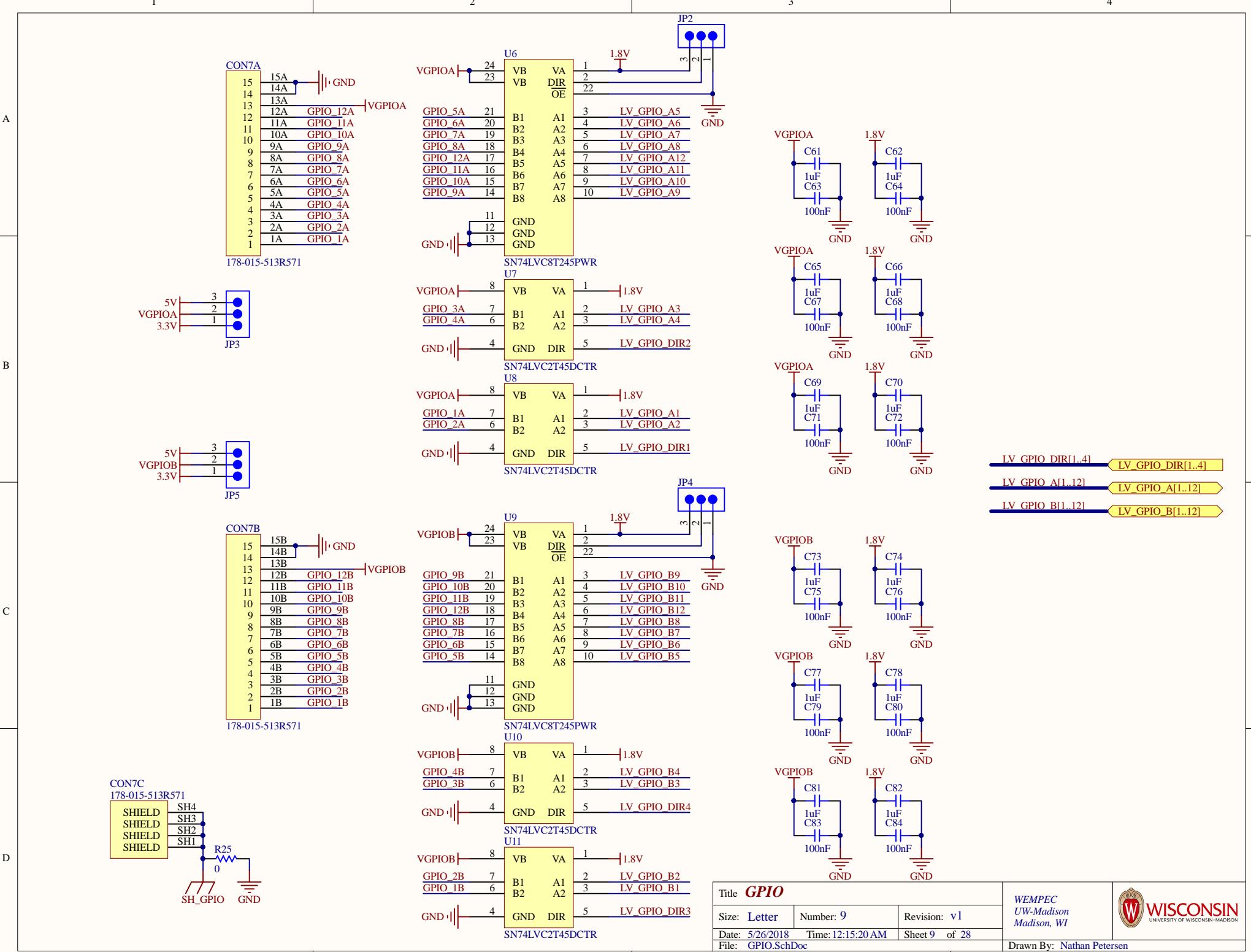
D

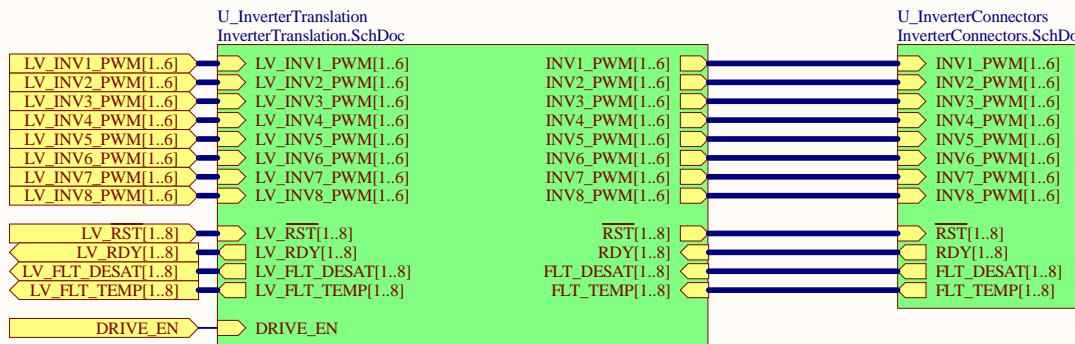
D


Title *Encoder*

Size: Letter	Number: 8	Revision: v1
Date: 5/26/2018	Time: 12:15:20 AM	Sheet 8 of 28
File: Encoder.SchDoc		Drawn By: Nathan Petersen







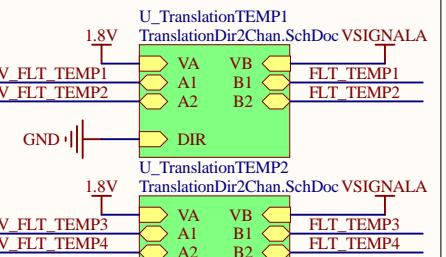
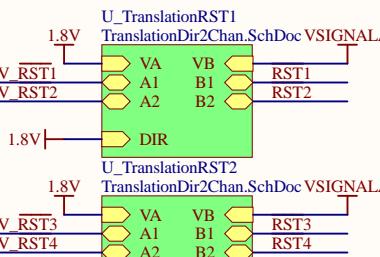
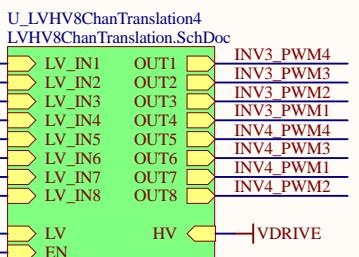
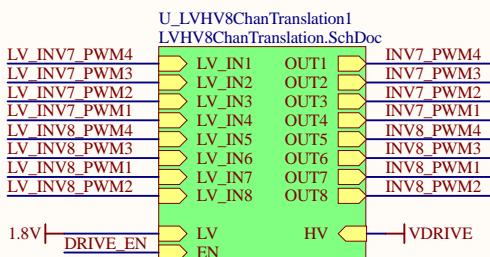
Title **Drive Interface**

Size: Letter	Number: 10	Revision: v1
Date: 5/26/2018	Time: 12:15:20 AM	Sheet 10 of 28
File: DriveInterface.SchDoc		Drawn By: Nathan Petersen

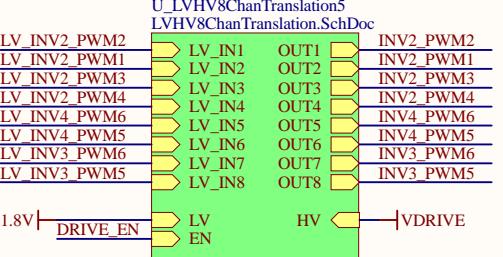
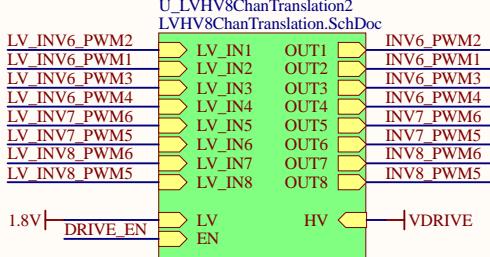


1 2 3 4

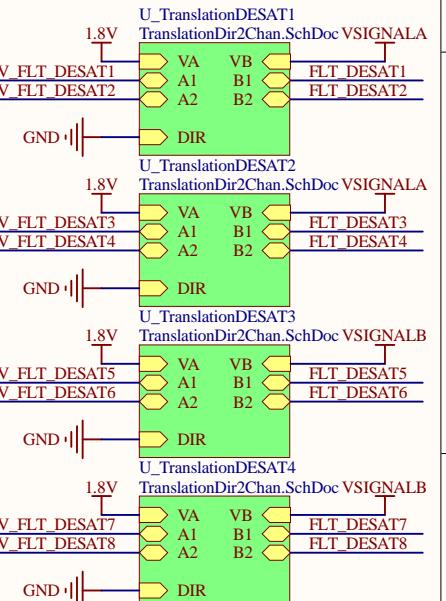
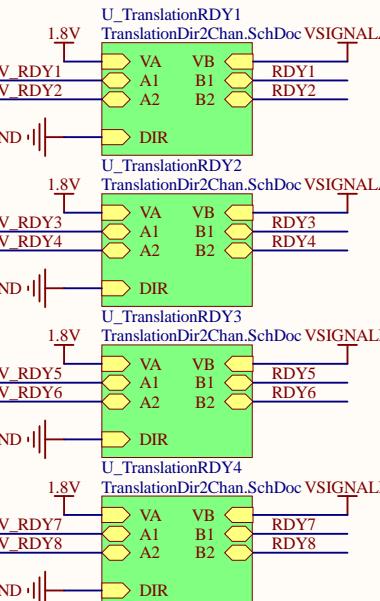
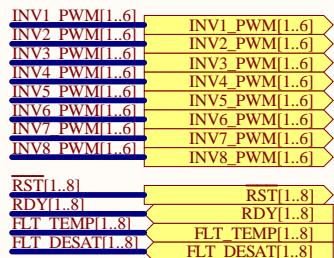
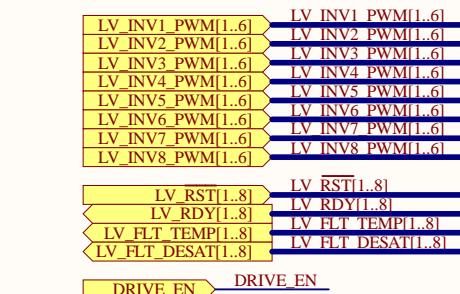
A



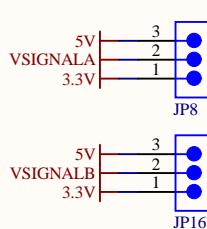
B



C



D



Title Inverter Level Translation			WEMPEC UW-Madison Madison, WI	WISCONSIN UNIVERSITY OF WISCONSIN-MADISON
Size: Letter	Number: 11	Revision: v1		
Date: 5/26/2018	Time: 12:15:20 AM	Sheet 11 of 28		
File: InverterTranslation.SchDoc				Drawn By: Nathan Petersen

1

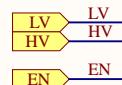
2

3

4

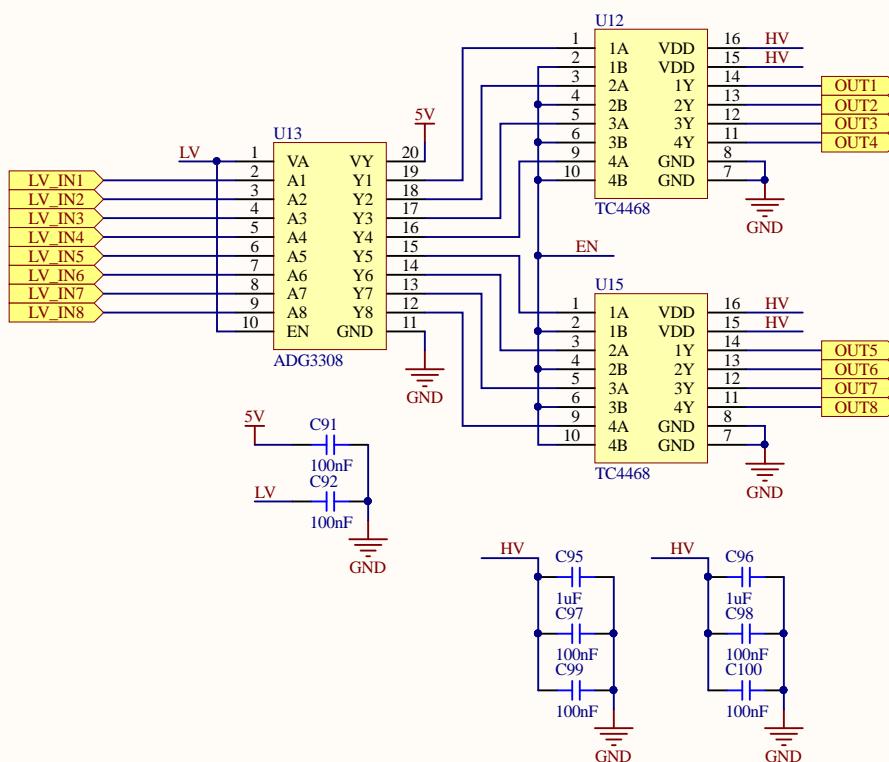
A

A



B

B



D

D

Title: **8-channel LV to HV Translation**

Size: Letter	Number: 12	Revision: v1
--------------	------------	--------------

Date: 5/26/2018	Time: 12:15:21 AM	Sheet 12 of 28
-----------------	-------------------	----------------

File: LVHV8ChanTranslation.SchDoc	
-----------------------------------	--

WEMPEC
UW-Madison
Madison, WI



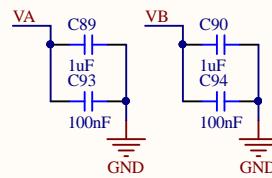
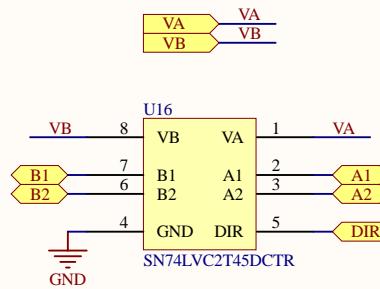
Drawn By: Nathan Petersen

A

B

C

D

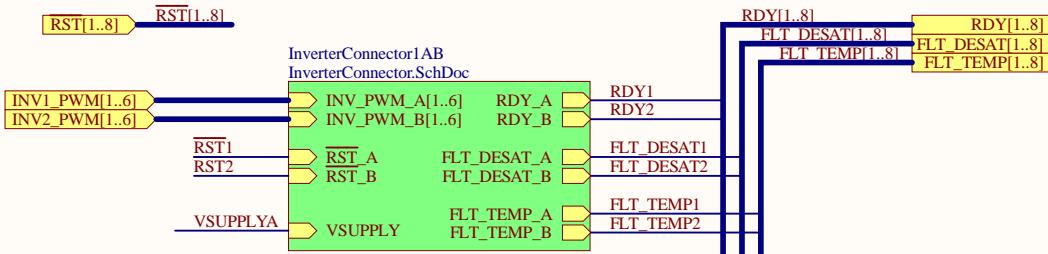


Title 2-Channel Directional Translation		
Size: Letter	Number: 13	Revision: v1
Date: 5/26/2018	Time: 12:15:21 AM	Sheet 13 of 28
File: TranslationDir2Chan.SchDoc		Drawn By: Nathan Petersen

WEMPEC
UW-Madison
Madison, WI

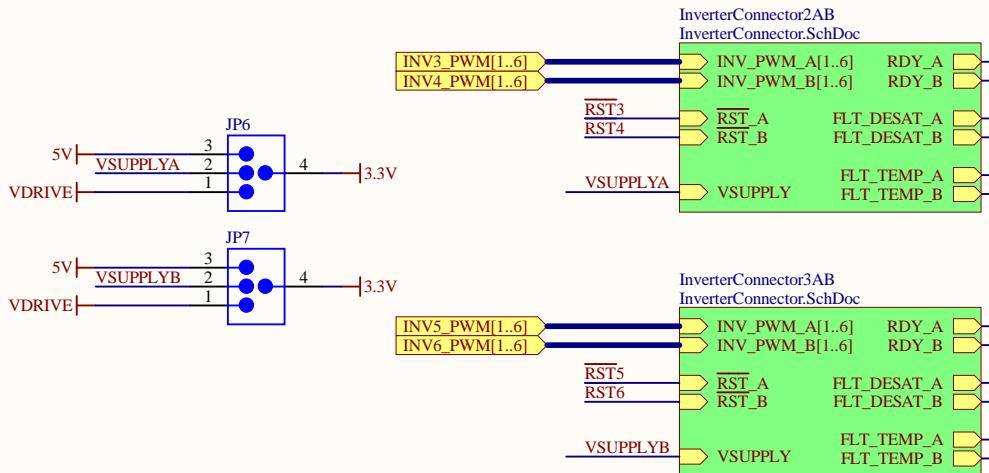


A



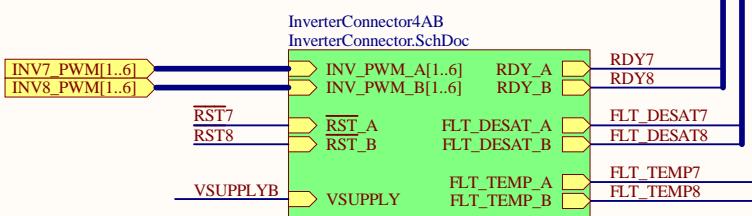
A

B



B

C



C

D

Title Inverter Connectors

Size: Letter	Number: 14	Revision: v1
Date: 5/26/2018	Time: 12:15:21 AM	Sheet 14 of 28
File: InverterConnectors.SchDoc		Drawn By: Nathan Petersen

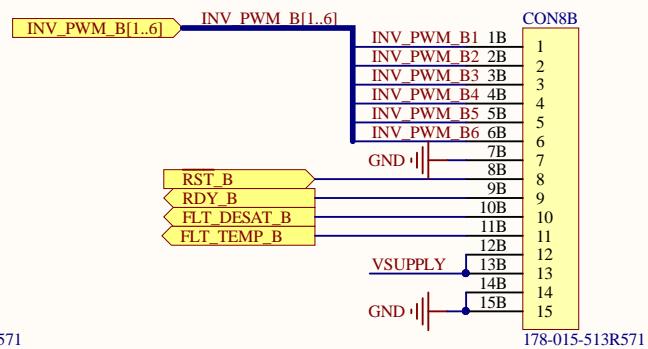
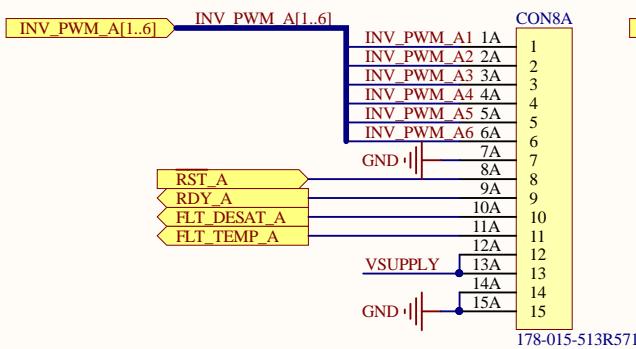
WEMPEC
UW-Madison
Madison, WI



A

A

VSUPPLY



B

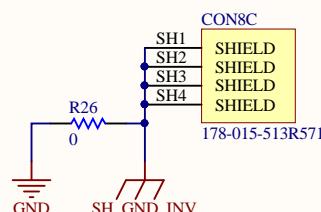
B

C

C

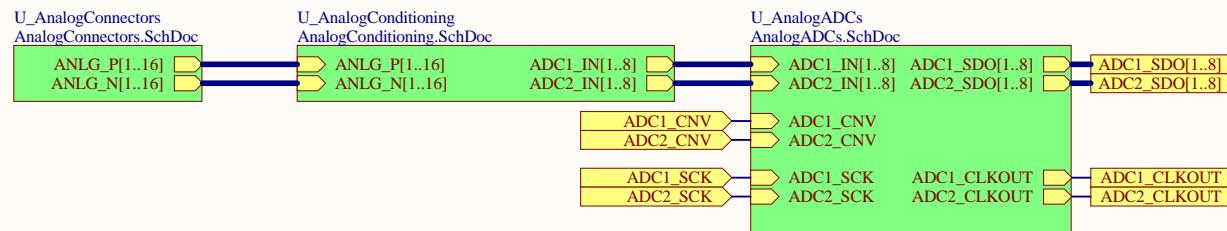
D

D

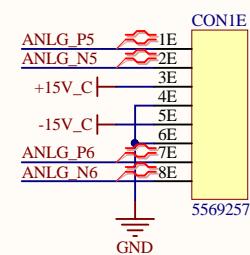
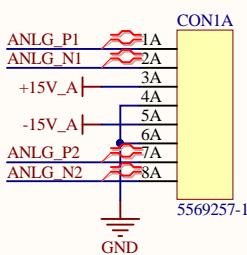

Title Inverter Connector

Size: Letter	Number: 15	Revision: v1
Date: 5/26/2018	Time: 12:15:21 AM	Sheet 15 of 28
File: InverterConnector.SchDoc		Drawn By: Nathan Petersen

 WEMPEC
 UW-Madison
 Madison, WI

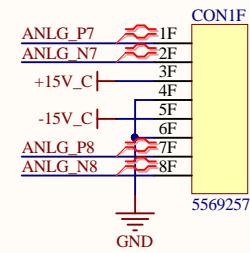
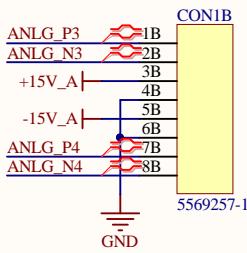



A

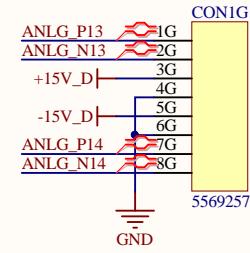
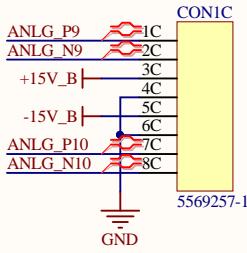


B

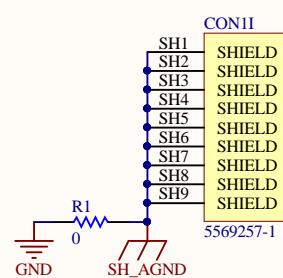
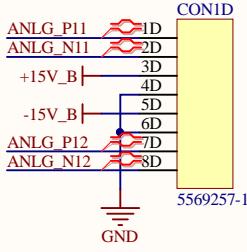
ANLG_P[1..16] ANLG_P[1..16]
 ANLG_N[1..16] ANLG_N[1..16]



C



D



Title Analog RJ45 Connectors

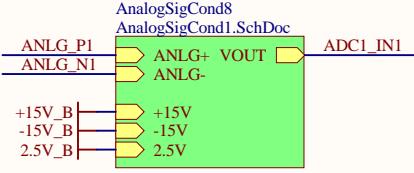
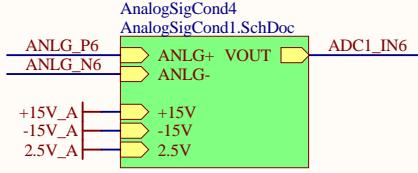
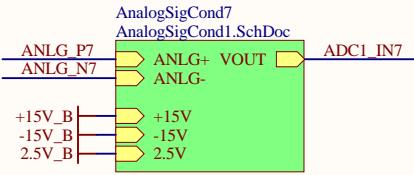
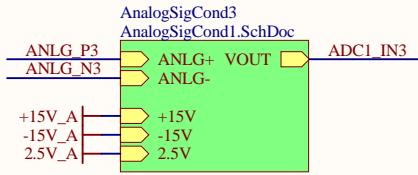
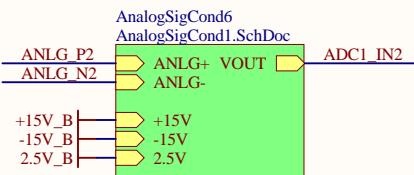
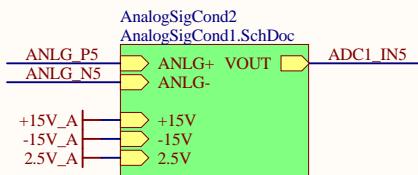
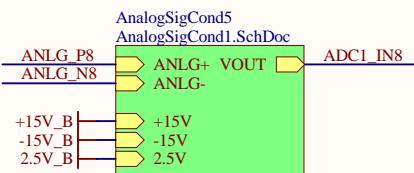
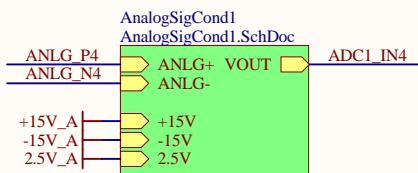
Size: Letter	Number: 17	Revision: v1
Date: 5/26/2018	Time: 12:15:22 AM	Sheet 17 of 28
File: AnalogConnectors.SchDoc		Drawn By: Nathan Petersen

WEMPEC
UW-Madison
Madison, WI



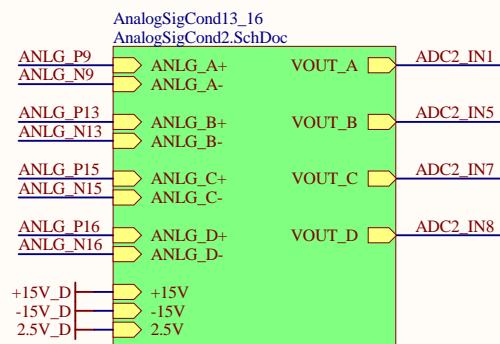
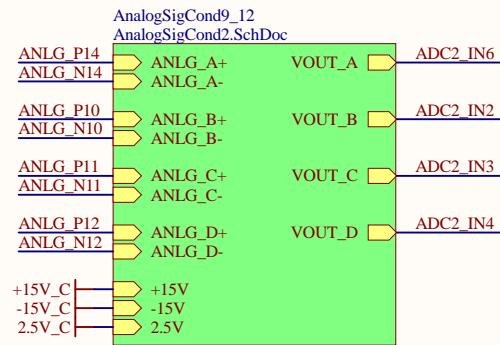
A

A



ANLG_P[1..16] ANLG_P[1..16]
ANLG_N[1..16] ANLG_N[1..16]

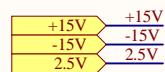
ADC1_IN[1..8] ADC1_IN[1..8]
ADC2_IN[1..8] ADC2_IN[1..8]



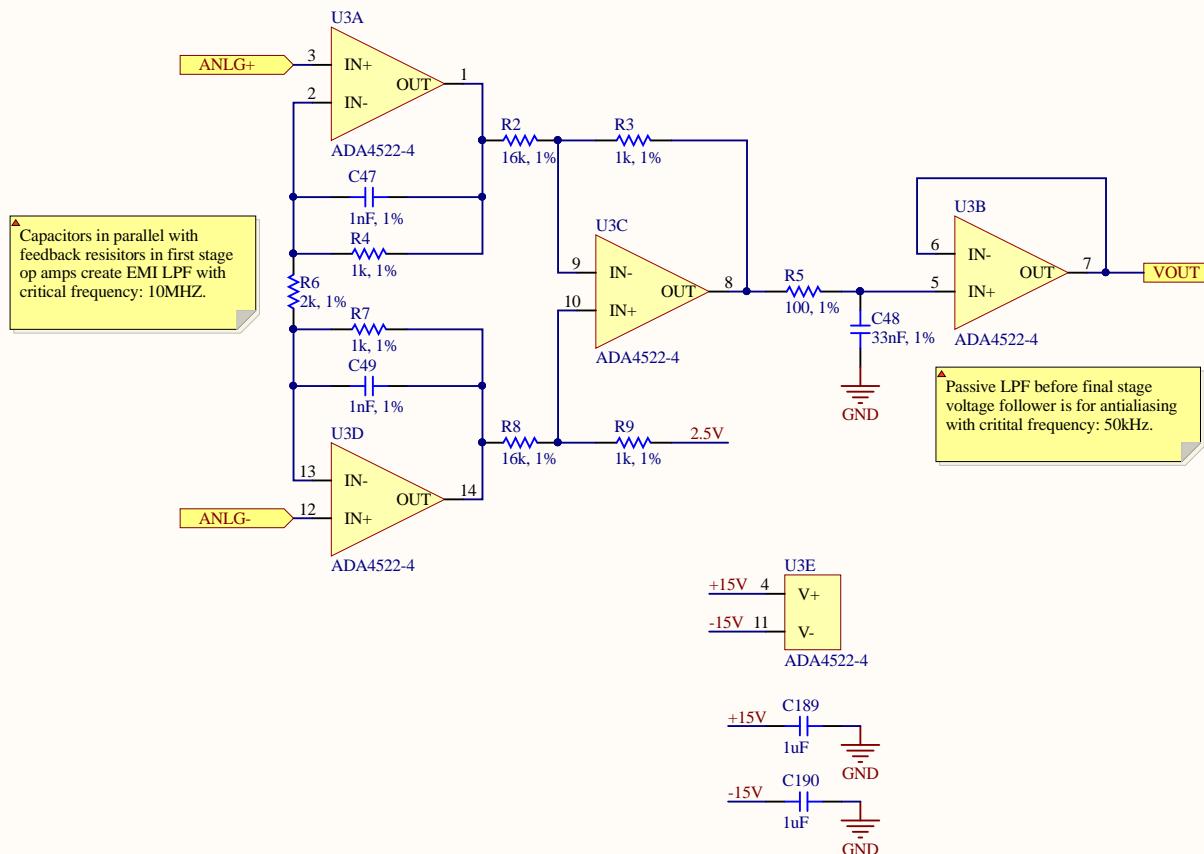
Title Analog Signal Conditioning			WEMPEC UW-Madison Madison, WI
Size: Letter	Number: 18	Revision: v1	
Date: 5/26/2018	Time: 12:15:22 AM	Sheet 18 of 28	
File: AnalogConditioning.SchDoc			Drawn By: Nathan Petersen



A



B



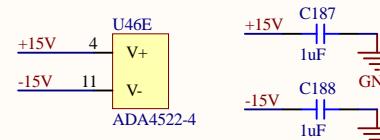
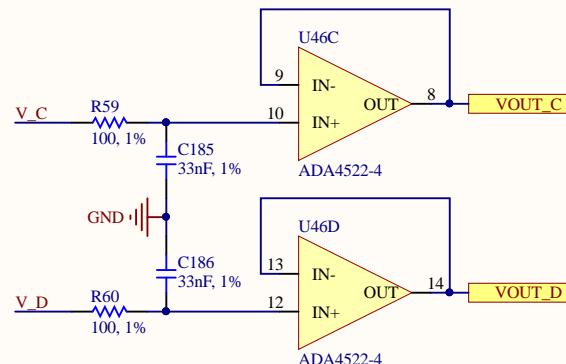
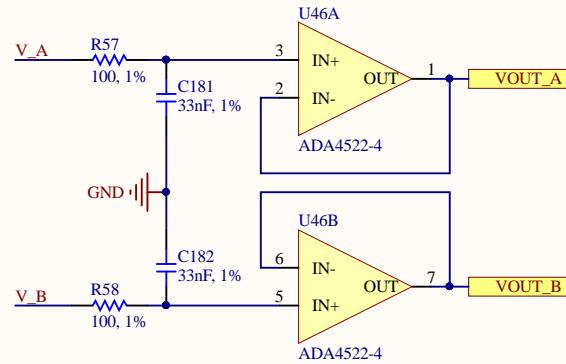
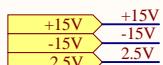
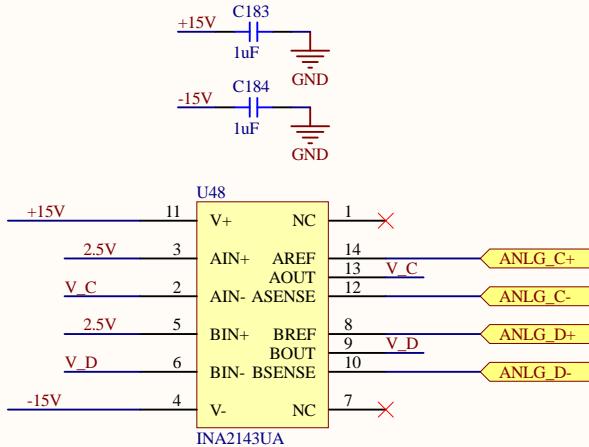
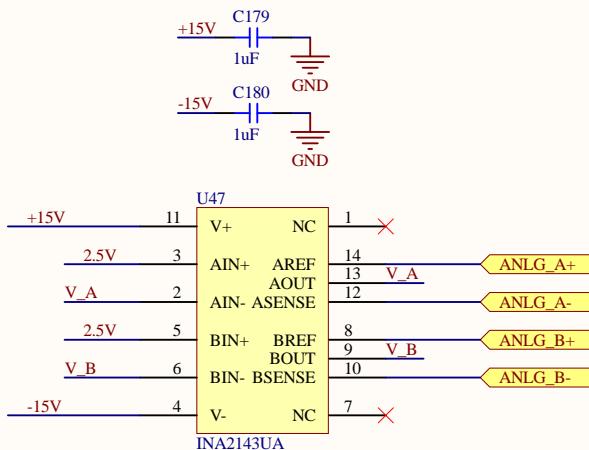
Title *Analog Signal Front-End 1*

Size: Letter	Number: 19	Revision: v1
Date: 5/26/2018	Time: 12:15:22 AM	Sheet 19 of 28
File: AnalogSigCond1.SchDoc		Drawn By: Nathan Petersen



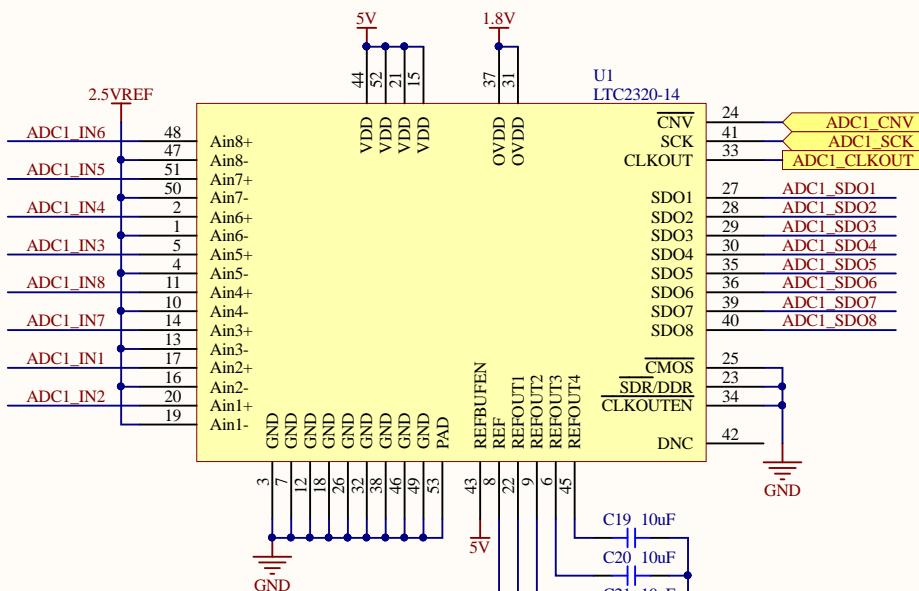
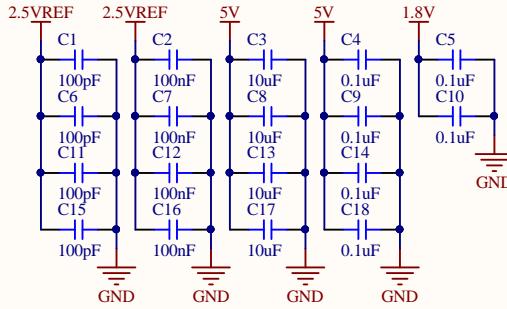
A

10



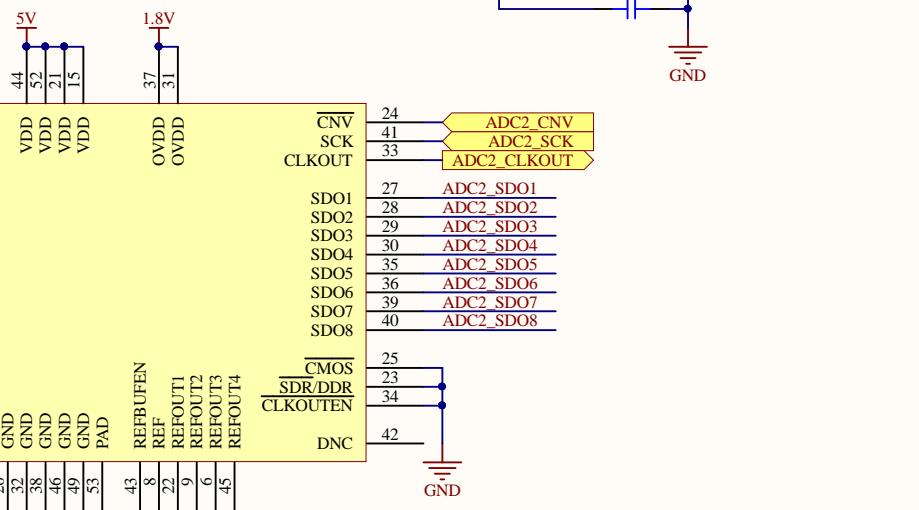
Title Analog Signal Front-End 2			<i>WEMPEC UW-Madison Madison, WI</i>	 WISCONSIN UNIVERSITY OF WISCONSIN-MADISON		
Size: Letter		Number: 20				
Revision: v1						
Date: 5/26/2018 Time: 12:15:22 AM		Sheet 20 of 28				
File: AnalogSigCond2.SchDoc			Drawn By: Nathan Petersen			

A

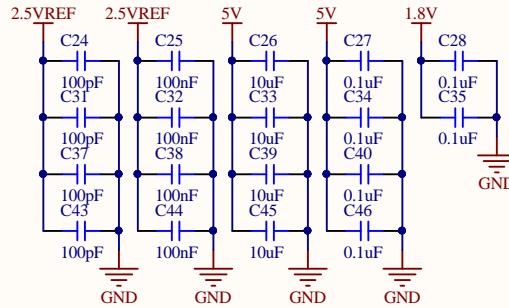


B

ADC1_IN[1..8] **ADC1_IN[1..8]**
ADC2_IN[1..8] **ADC2_IN[1..8]**



C

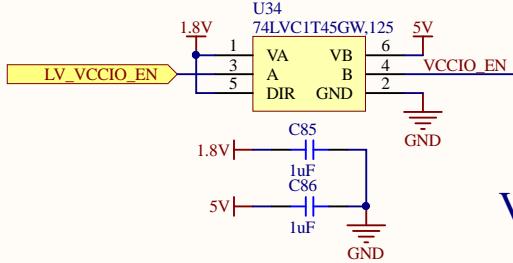


Title **ADCs**

Size: Letter	Number: 21	Revision: v1
Date: 5/26/2018	Time: 12:15:22 AM	Sheet 21 of 28
File: AnalogADCs.SchDoc		Drawn By: Nathan Petersen

ADC1_SDO[1..8] **ADC1_SDO[1..8]**
ADC2_SDO[1..8] **ADC2_SDO[1..8]**

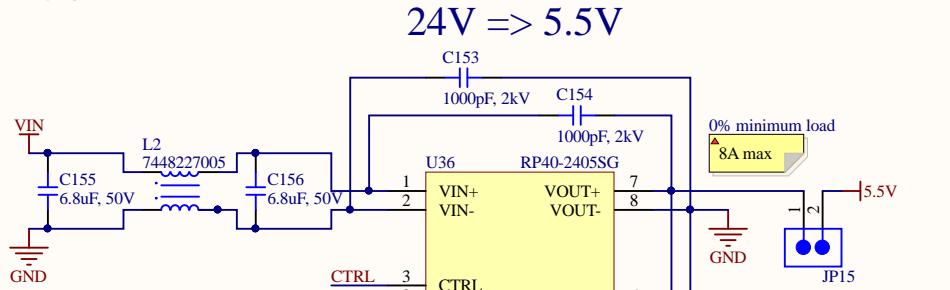
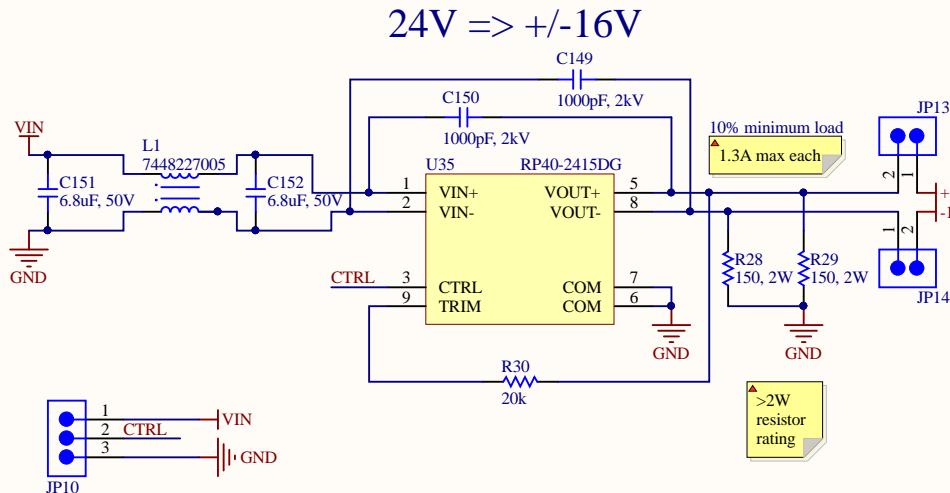
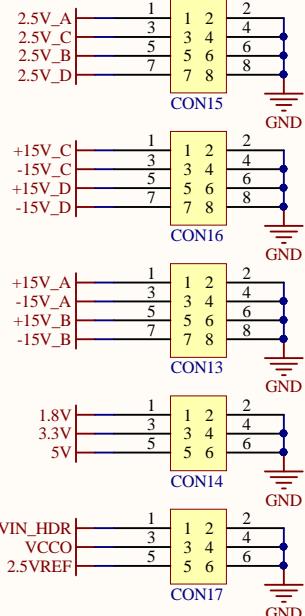




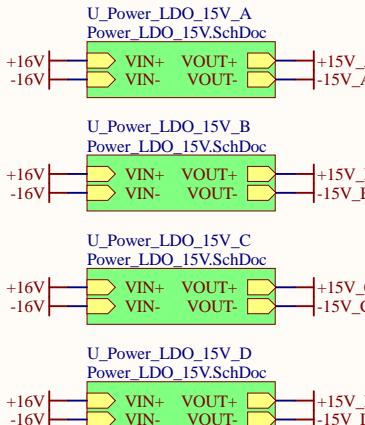
A

5V	<=> General
VIN_HDR	<=> PicoZed main power
3.3V	<=> General
1.8V	<=> General
VCCO	<=> PicoZed VCCIO*
2.5V_A	<=> SigCond1..4
2.5V_B	<=> SigCond5..8
2.5V_C	<=> SigCond9..12
2.5V_D	<=> SigCond13..16
2.5VREF	<=> ADCs input reference
+/-15V_A	<=> Con1..2 / SigCond1..4
+/-15V_B	<=> Con3..4 / SigCond5..8
+/-15V_C	<=> Con5..6 / SigCond9..12
+/-15V_D	<=> Con7..8 / SigCond13..16

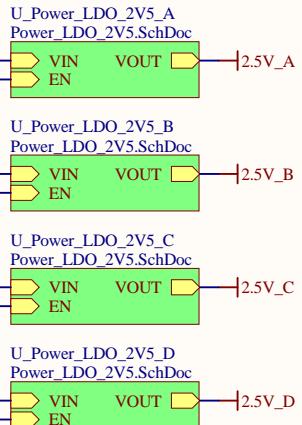
VOLTAGE HEADERS



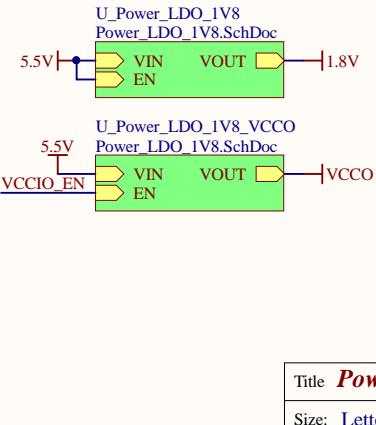
+/-15V LDOs 200mA max each



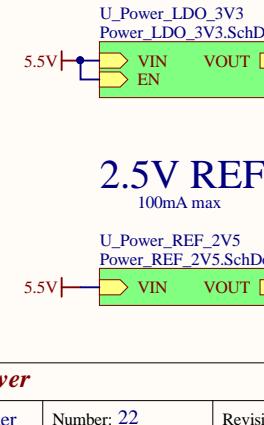
2.5V LDOs 250mA max each



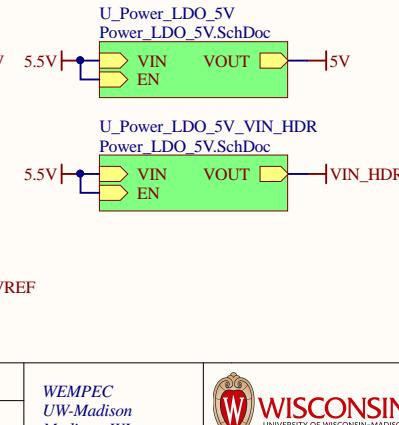
1.8V LDOs 3A max each



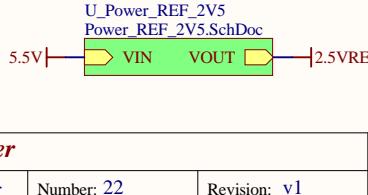
3.3V LDOs 3A max each



5V LDOs 3A max each



2.5V REF 100mA max

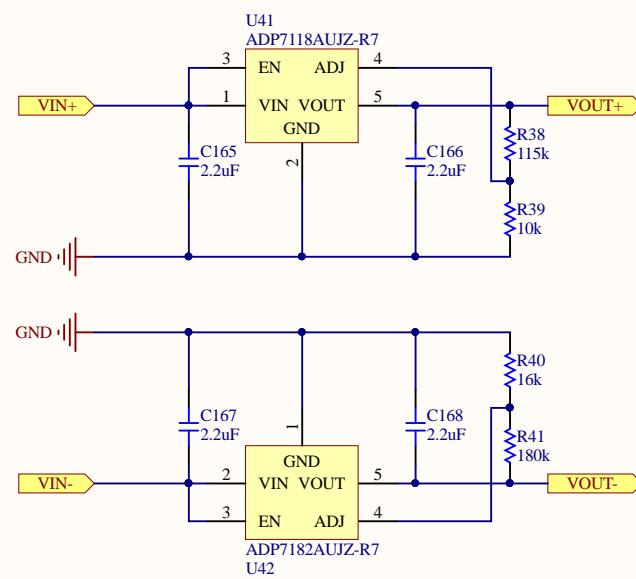


4

Title **Power**

Size: Letter	Number: 22	Revision: v1	WEMPEC UW-Madison Madison, WI
Date: 5/26/2018	Time: 12:15:23 AM	Sheet 22 of 28	
File: Power.SchDoc			

Drawn By: Nathan Petersen

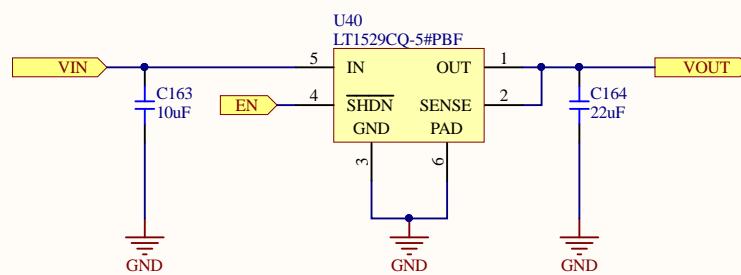


Title +/-15V LDO		
Size: Letter	Number: 23	Revision: v1
Date: 5/26/2018	Time: 12:15:23 AM	Sheet 23 of 28
File: Power_LDO_15V.SchDoc		

WEMPEC
UW-Madison
Madison, WI



Drawn By: Nathan Petersen

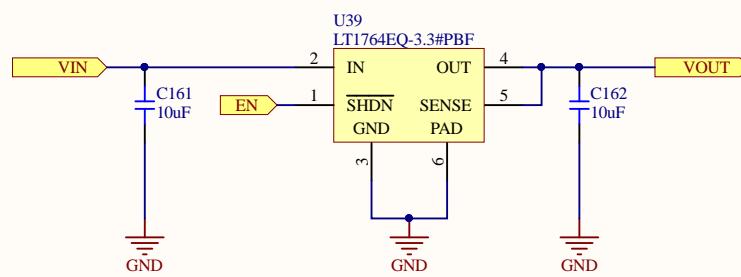


Title **5V LDO**

Size: Letter	Number: 24	Revision: v1
Date: 5/26/2018	Time: 12:15:23 AM	Sheet 24 of 28
File: Power_LDO_5V.SchDoc		Drawn By: Nathan Petersen

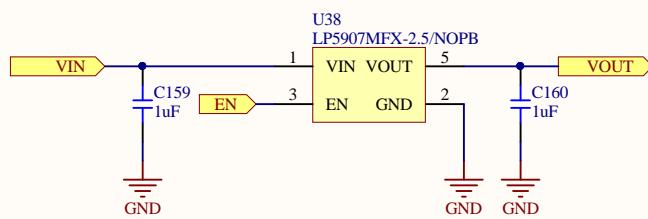
WEMPEC
UW-Madison
Madison, WI




Title 3.3V LDO

Size: Letter	Number: 25	Revision: v1
Date: 5/26/2018	Time: 12:15:23 AM	Sheet 25 of 28
File: Power_LDO_3V3.SchDoc		Drawn By: Nathan Petersen

*WEMPEC
UW-Madison
Madison, WI*

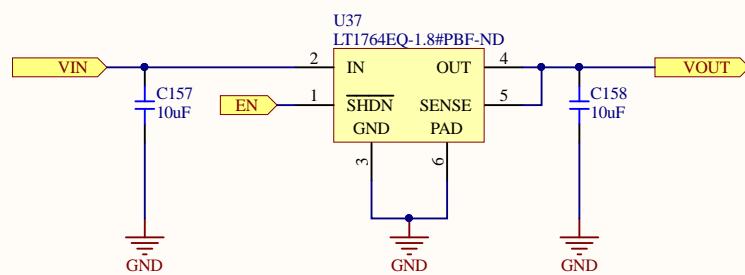



Title **2.5V LDO**

Size: Letter	Number: 26	Revision: v1
Date: 5/26/2018	Time: 12:15:23 AM	Sheet 26 of 28
File: Power_LDO_2V5.SchDoc		Drawn By: Nathan Petersen

WEMPEC
UW-Madison
Madison, WI





Title ***1.8V LDO***

Size: Letter	Number: 27	Revision: v1
--------------	------------	--------------

Date: 5/26/2018	Time: 12:15:23 AM	Sheet 27 of 28
-----------------	-------------------	----------------

File: Power_LDO_1V8.SchDoc

WEMPEC
UW-Madison
Madison, WI



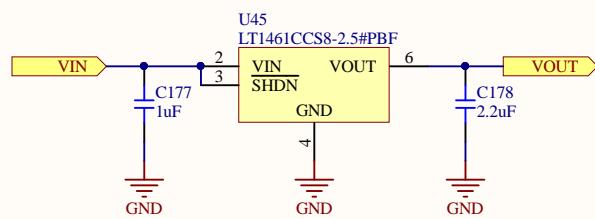
Drawn By: Nathan Petersen

A

B

C

D


Title *2.5V Reference*

Size: Letter	Number: 28	Revision: v1
Date: 5/26/2018	Time: 12:15:23 AM	Sheet 28 of 28
File: Power_REF_2V5.SchDoc		Drawn By: Nathan Petersen

*WEMPEC
UW-Madison
Madison, WI*
