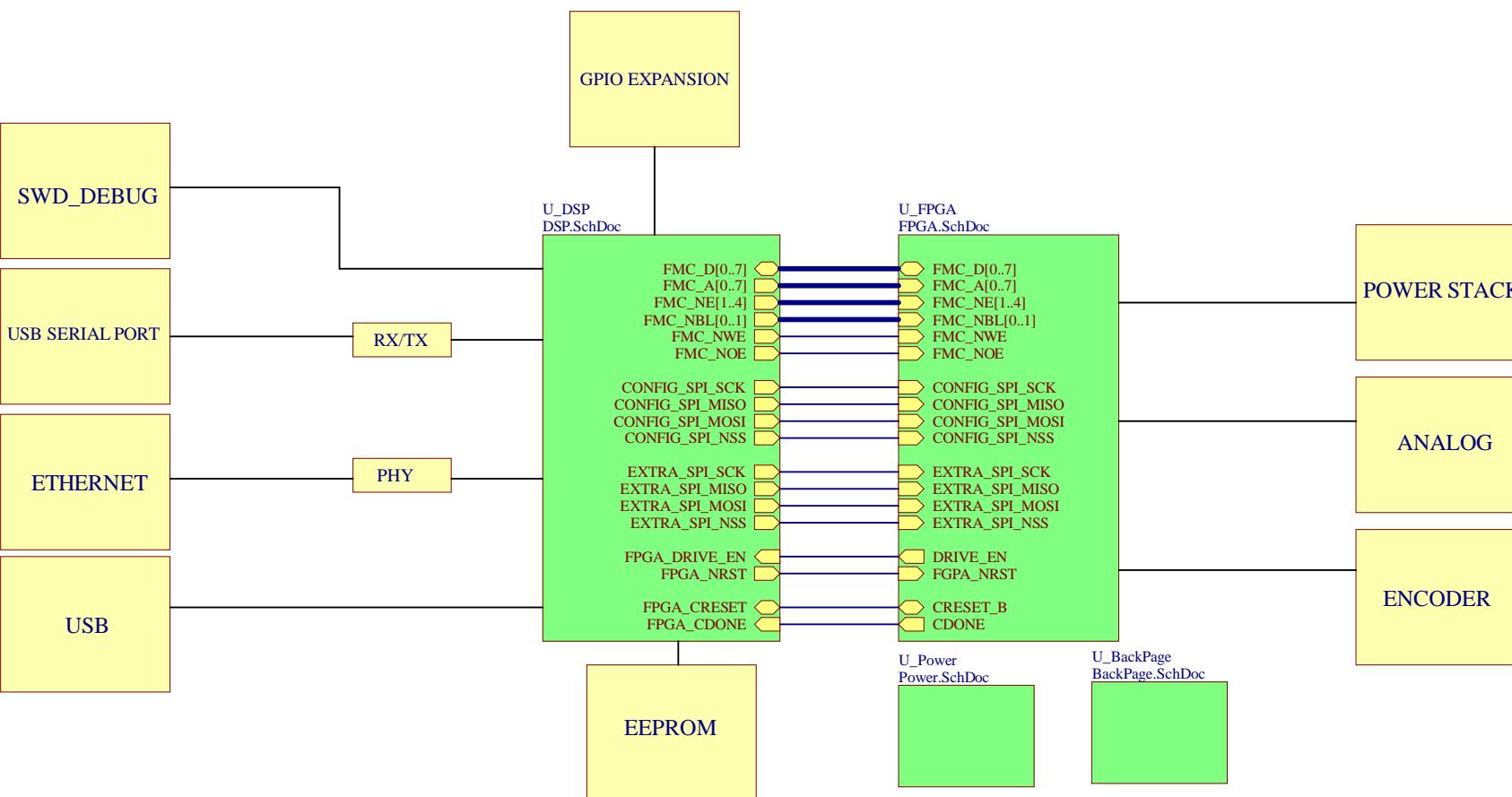


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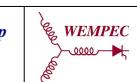
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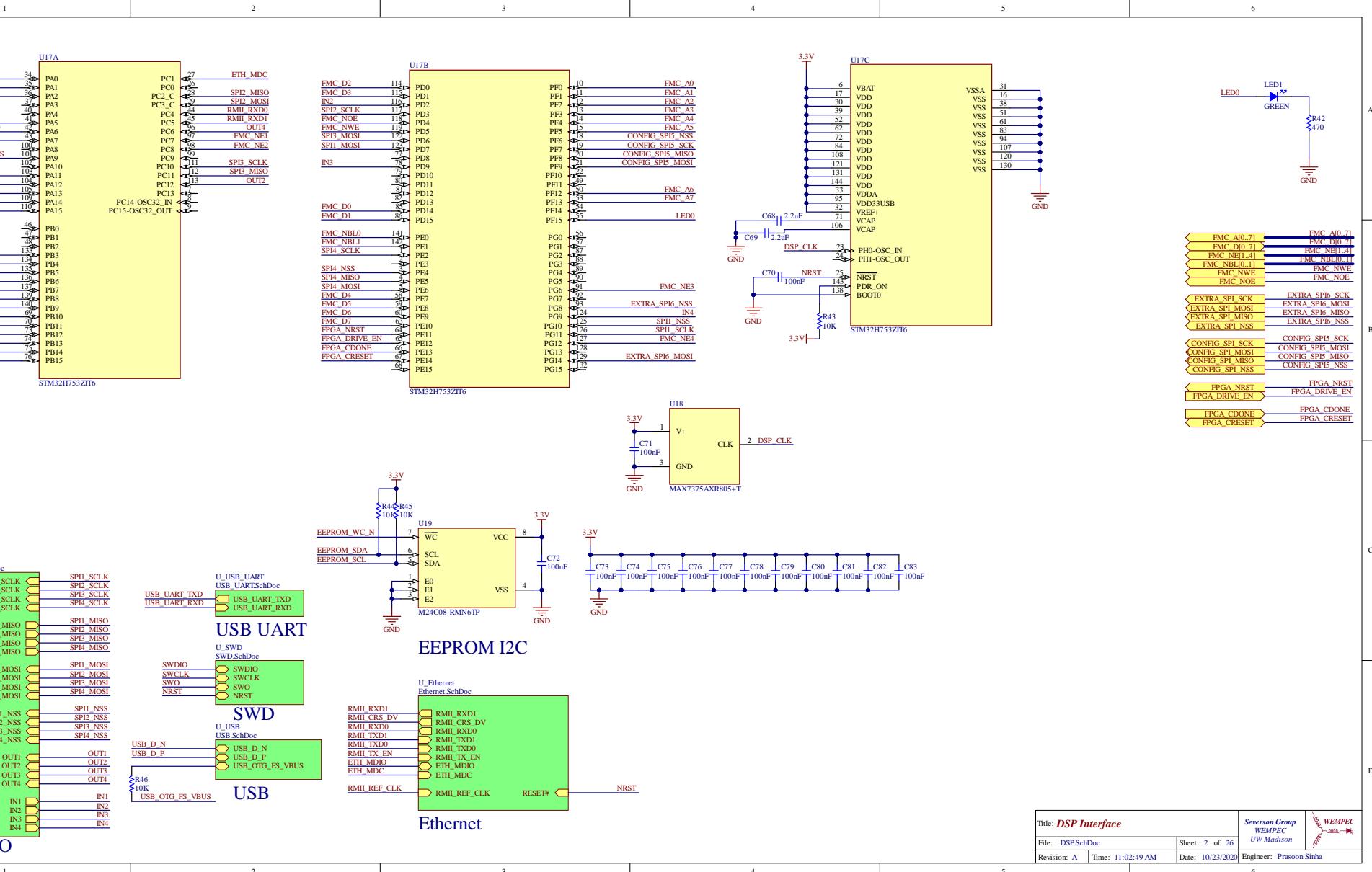
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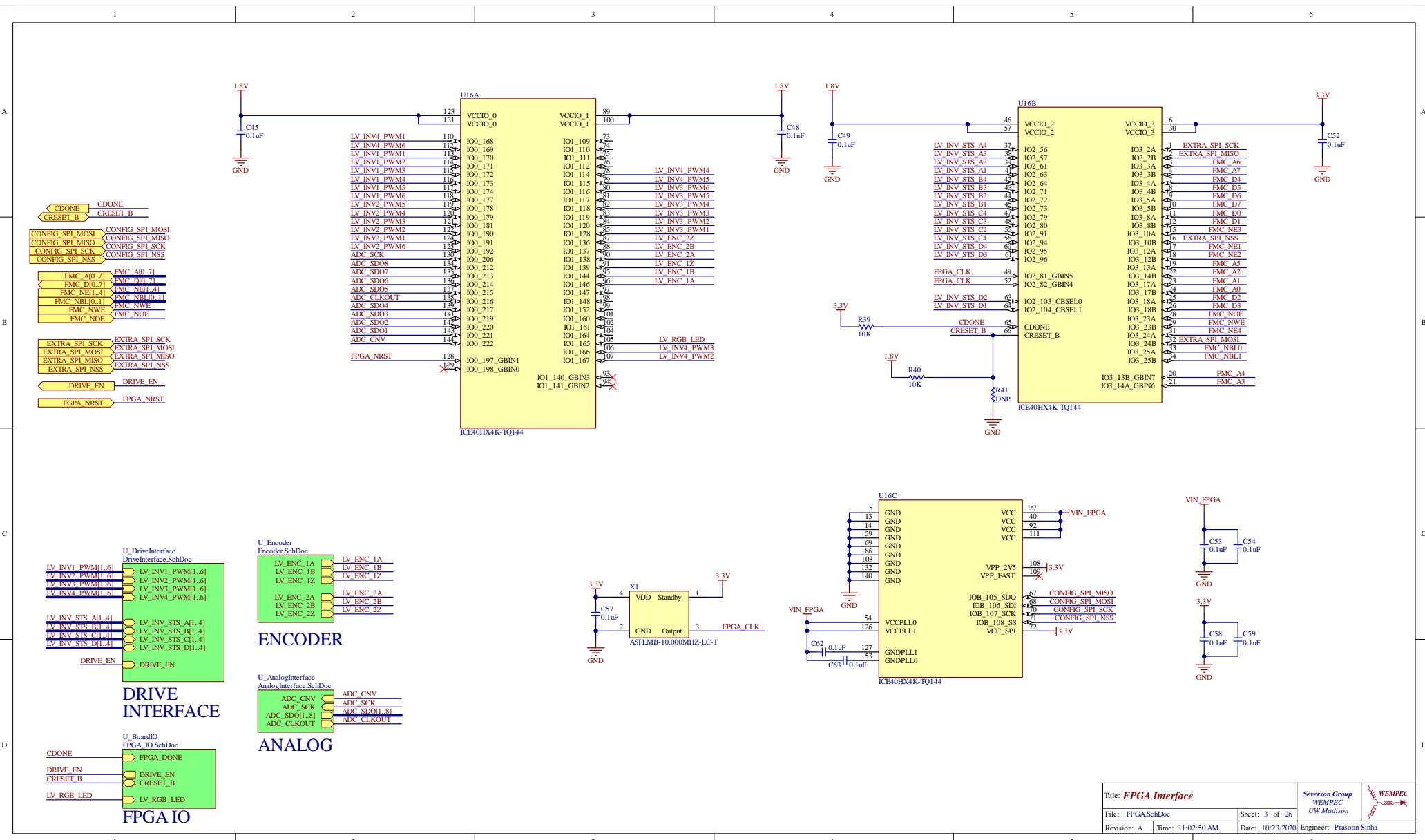
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D

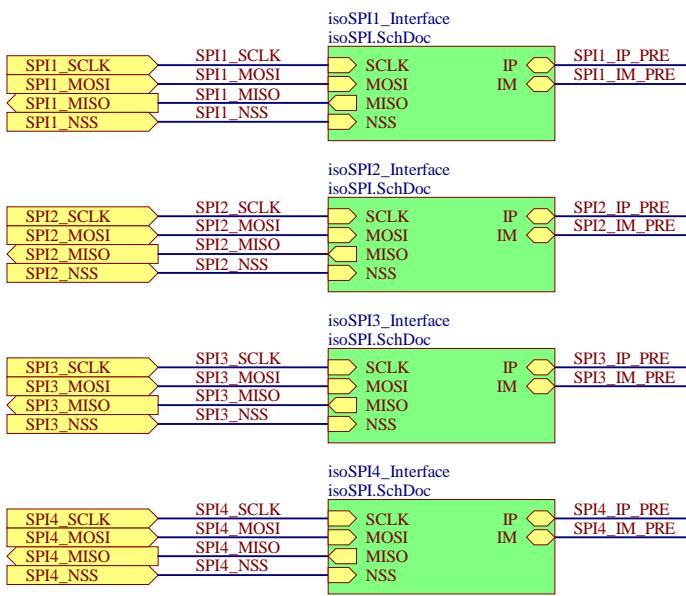
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Title: ***uAMDC***File: ***uAMDC.SchDoc***Sheet: **1 of 26**Revision: **A**Time: **11:02:49 AM**Date: **10/23/2020**
**Severson Group**  
**WEMPEC**  
**UWMadison**
Engineer: **Prasoon Sinha**

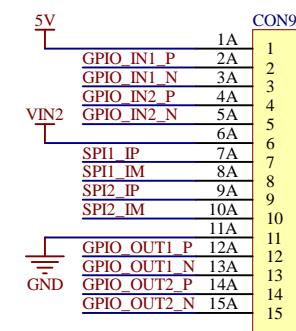
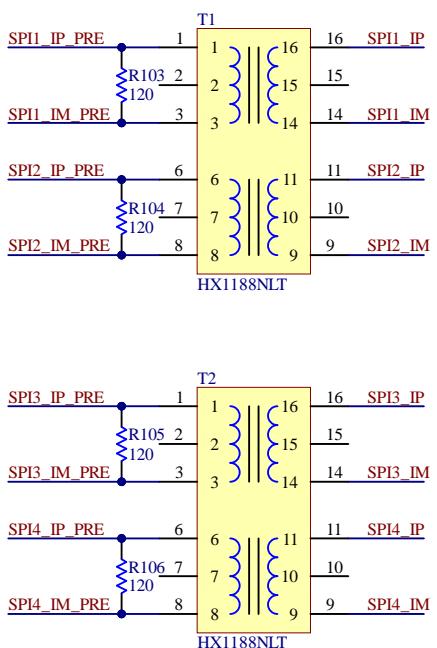




A

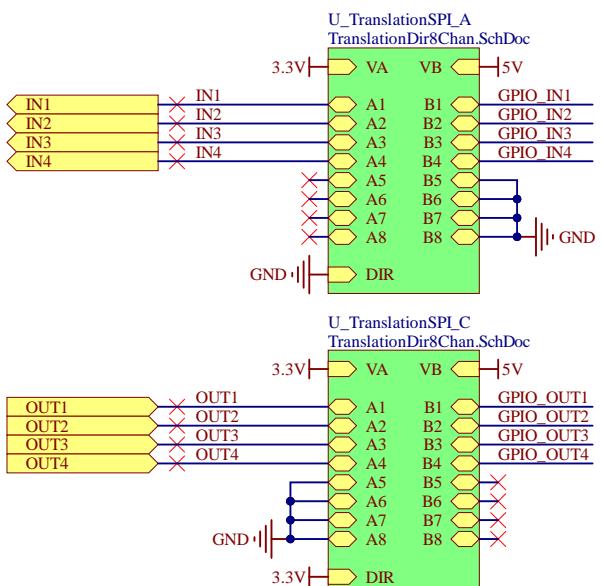


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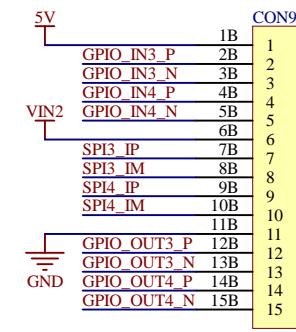
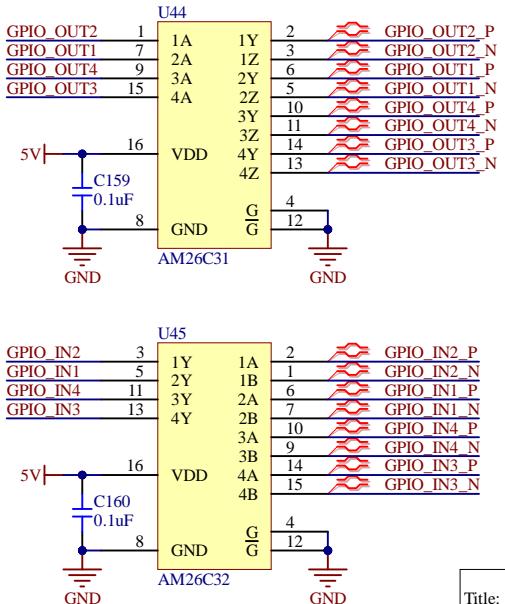


178-H15-513R497

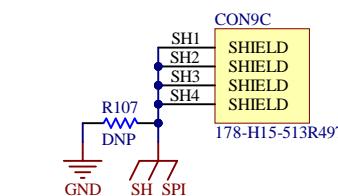
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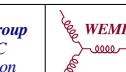
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178-H15-513R497



178-H15-513R497

Title: **GPIO**File: **GPIO.SchDoc** | Sheet: **4 of 26**Revision: **A** | Time: **11:02:50 AM** | Date: **10/23/2020**Severson Group  
WEMPEC  
UWMadison

Engineer: Prasoon Sinha

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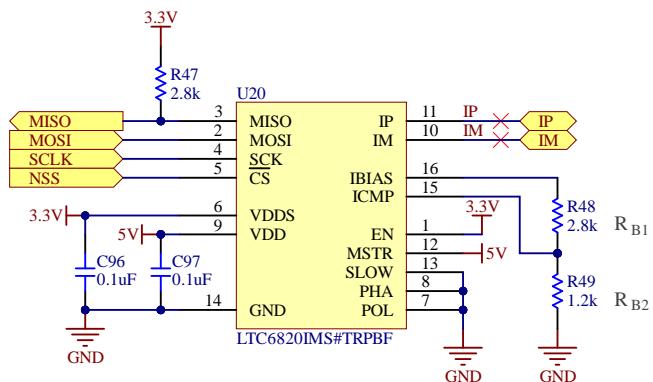
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Title: *isoSPI Interface*

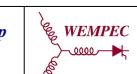
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Sheet: 5 of 26

Revision: A Time: 11:02:50 AM

Date: 10/23/2020

Severson Group  
WEMPEC  
UWMadison



Engineer: Nathan Petersen

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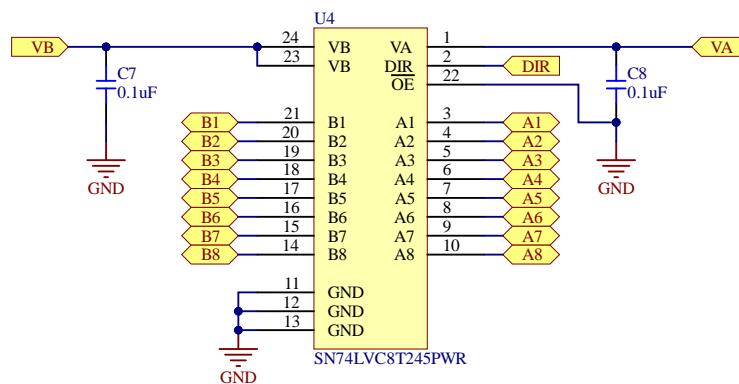
B

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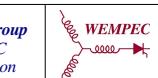
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Title: **8-Channel Directional Translation**

File: TranslationDir8Chan.SchDoc | Sheet: 6 of 26

Revision: A | Time: 11:02:50 AM | Date: 10/23/2020

Severson Group  
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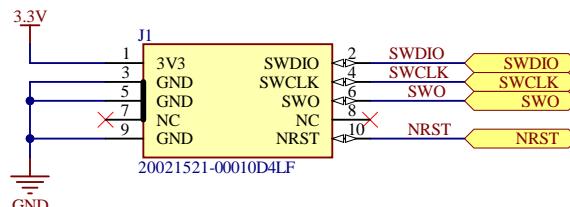
Engineer: Nathan Petersen

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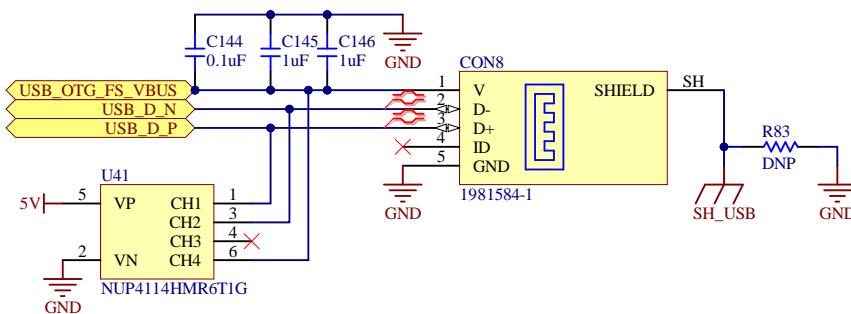
Title: <b>SWD</b>			Severson Group WEMPEC UWMadison
File: SWD.SchDoc	Sheet: 7 of 26		
Revision: A	Time: 11:02:50 AM	Date: 10/23/2020	
Engineer: Prasoon Sinha			WEMPEC

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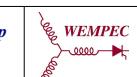
B

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Title: **USB**File: **USB.SchDoc**Sheet: **8 of 26**Revision: **A** Time: **11:02:50 AM**Date: **10/23/2020** Engineer: **Prasoon Sinha**

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**UWMadison**



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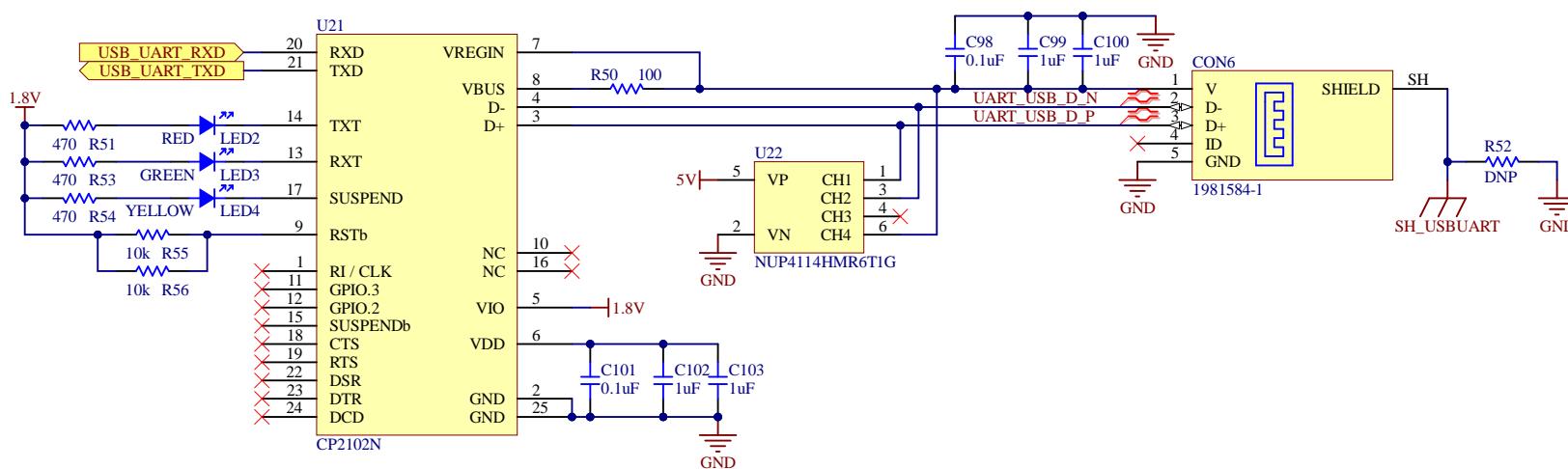
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C

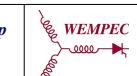
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D

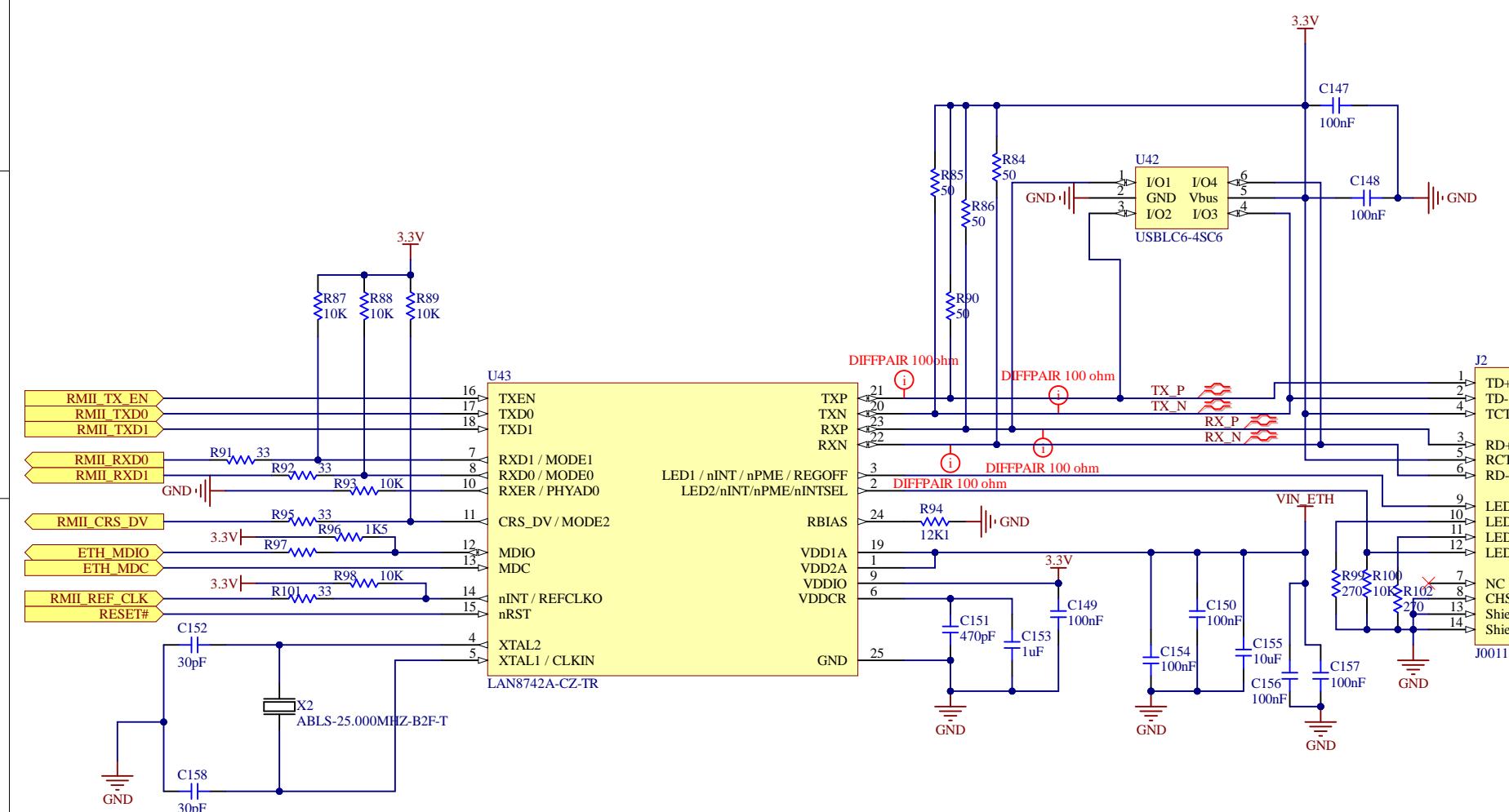
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**Severson Group**  
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Engineer: **Nathan Petersen**

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Title: *Ethernet*File: *Ethernet.SchDoc*

Sheet: 10 of 26

Revision: A Time: 11:02:50 AM

Date: 10/23/2020

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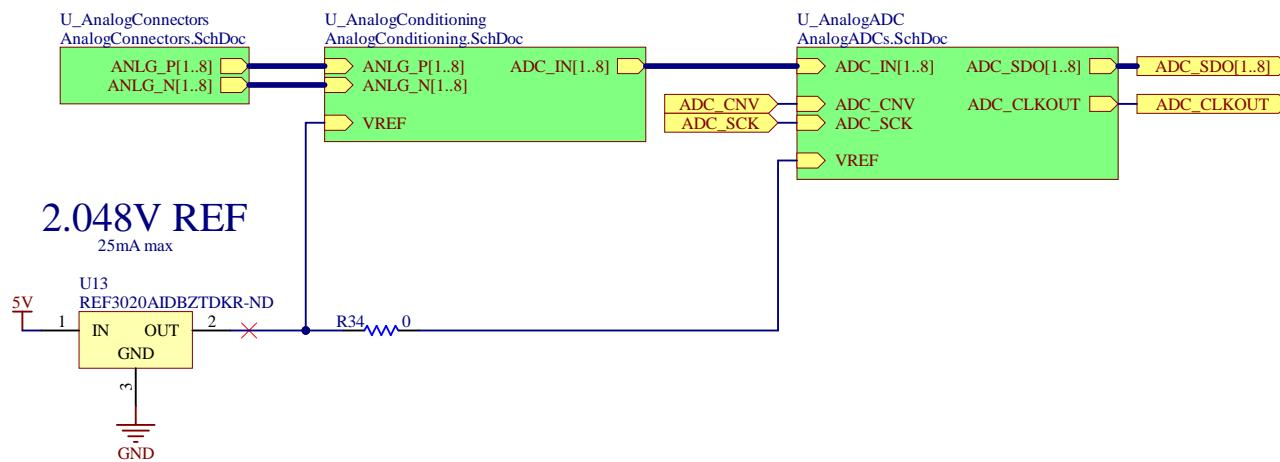
Engineer: Prasoon Sinha

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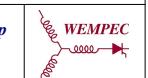
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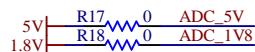
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Title: **Analog Interface**File: **AnalogInterface.SchDoc**Sheet: **11 of 26**Revision: **A** Time: **11:02:50 AM**Date: **10/23/2020** Engineer: **Nathan Petersen**

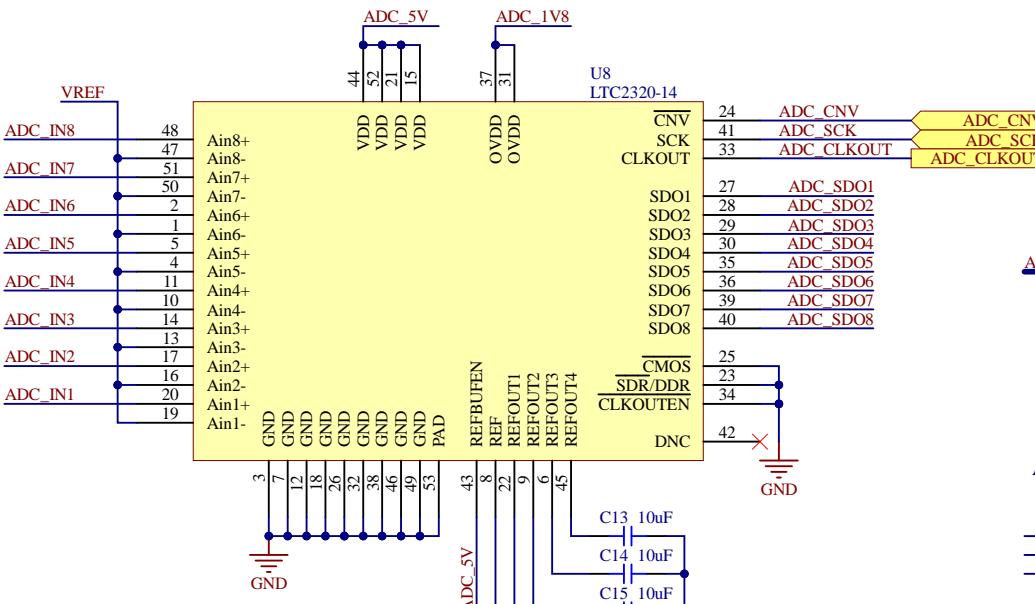
**Severson Group**  
**WEMPEC**  
**UWMadison**



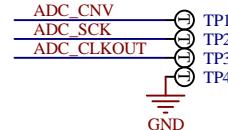
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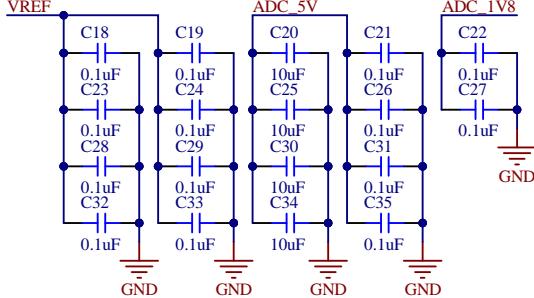
VREF  
ADC\_IN[1..8]



ADC Serial Interface Test Points



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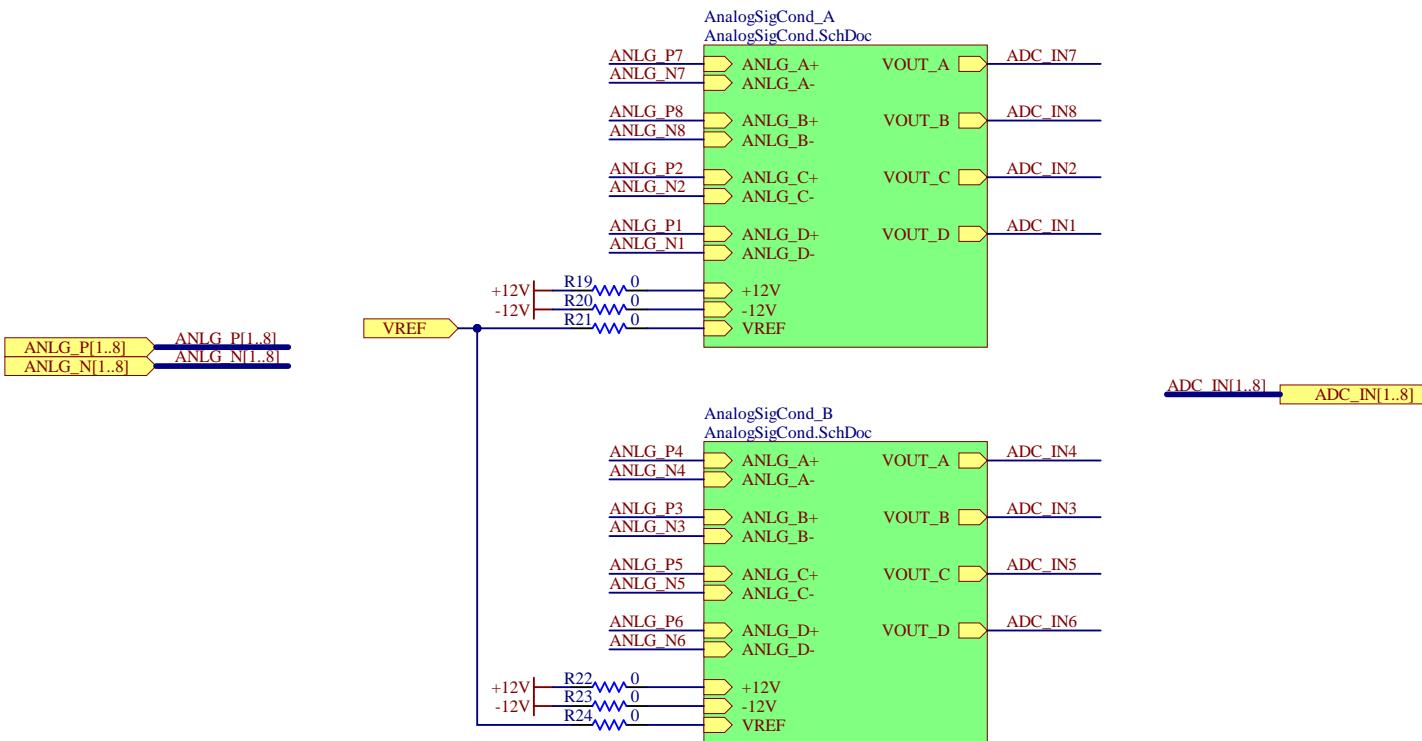
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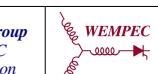
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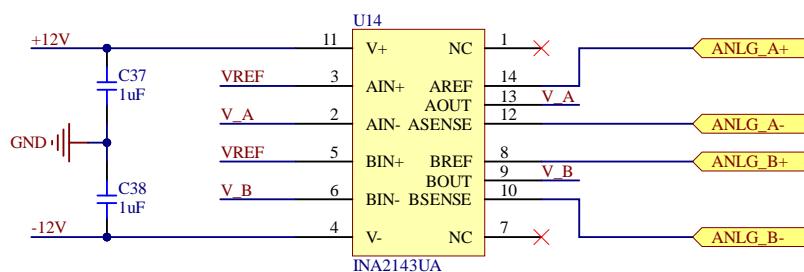
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D

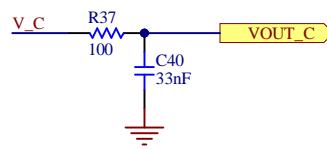
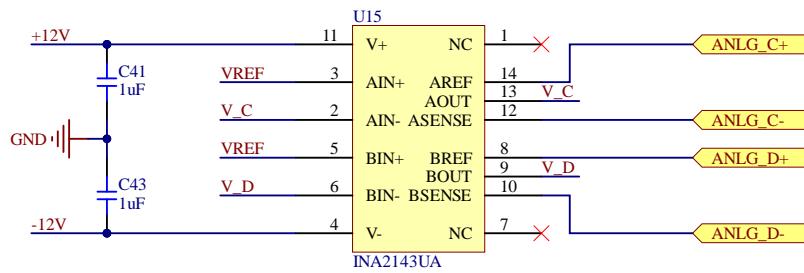
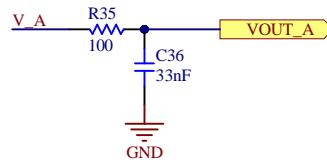
Title: **Analog Signal Conditioning**File: **AnalogConditioning.SchDoc** Sheet: **13 of 26**Revision: **A** Time: **11:02:50 AM** Date: **10/23/2020****Severson Group**  
**WEMPEC**  
**UWMadison**Engineer: **Nathan Petersen**

A

A



△ LPF: fc = 50kHz



D

D

Title: **Analog Signal Front-End**

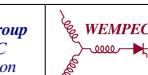
File: **AnalogSigCond.SchDoc**

Sheet: **14 of 26**

Revision: **A** Time: **11:02:50 AM**

Date: **10/23/2020**

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Engineer: **Nathan Petersen**

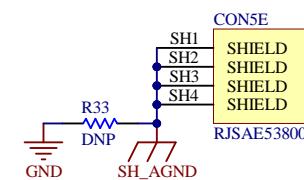
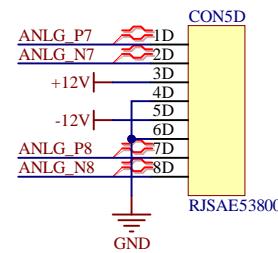
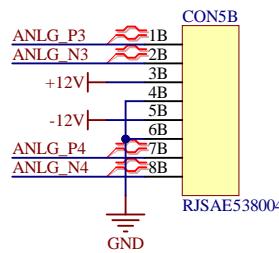
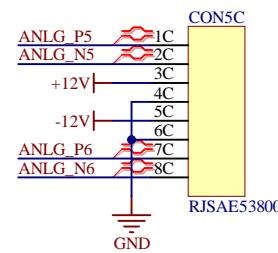
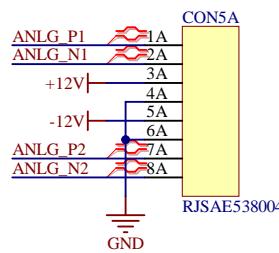
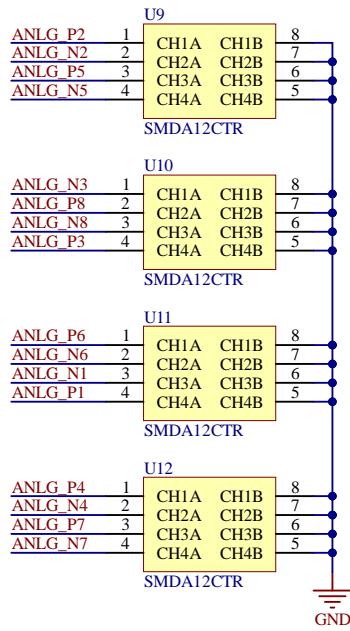
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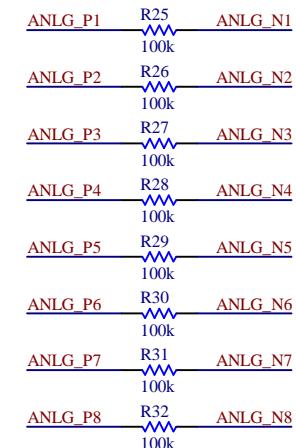
A

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### ESD Protection



Force no input to 0V



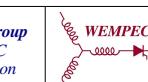
D

Title: **Analog RJ45 Connectors**

File: **AnalogConnectors.SchDoc** | Sheet: **15 of 26**

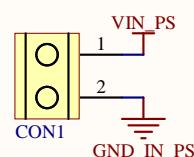
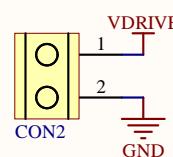
Revision: **A** | Time: **11:02:50 AM** | Date: **10/23/2020**

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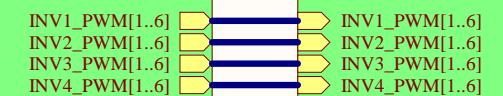
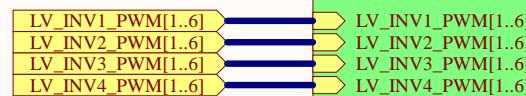


Engineer: **Nathan Petersen**

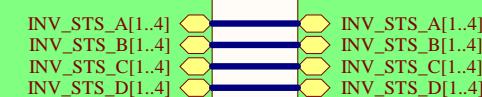
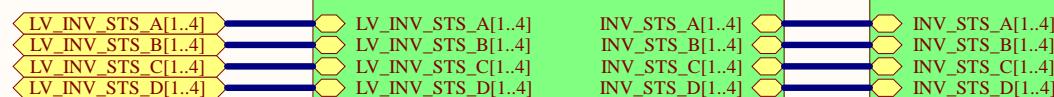
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**POWERSTACK VIN****VDRIVE**

B

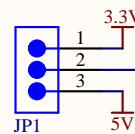
**U\_InverterTranslation  
InverterTranslation.SchDoc****U\_InverterConnectors  
InverterConnectors.SchDoc**

C

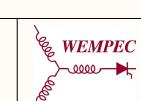


DRIVE\_EN

VDDPS

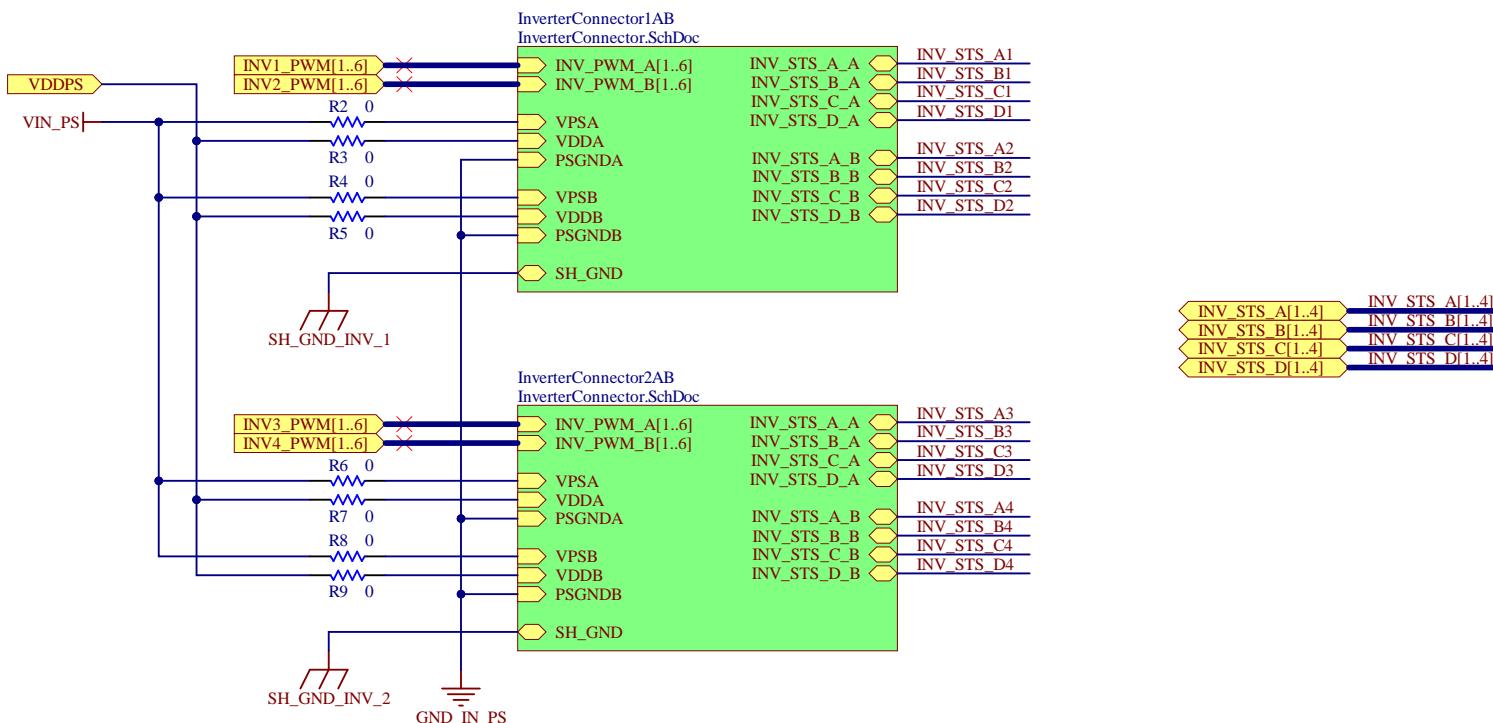


D

Title: **DriveInterface**File: **DriveInterface.SchDoc**Sheet: **16 of 26**Revision: **A** Time: **11:02:50 AM**Date: **10/23/2020** Engineer: **Prasoon Sinha****Severson Group  
WEMPEC  
UW Madison**

A

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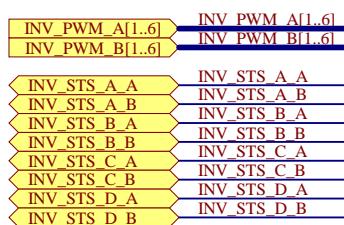
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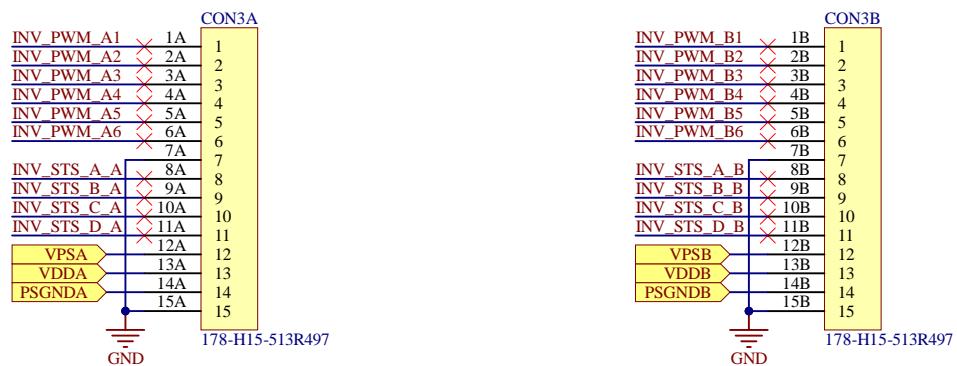
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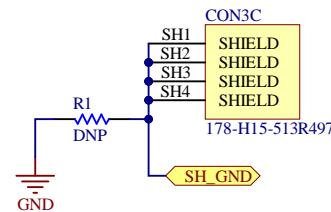
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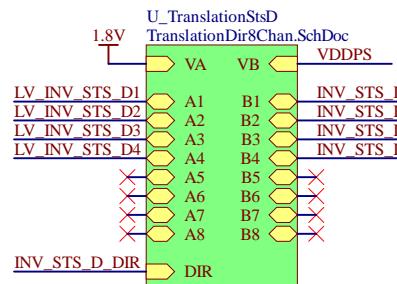
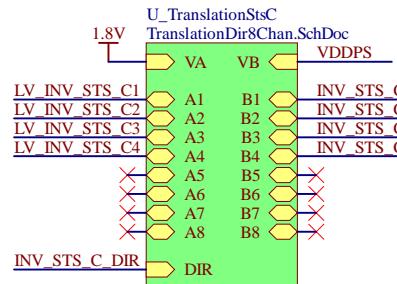
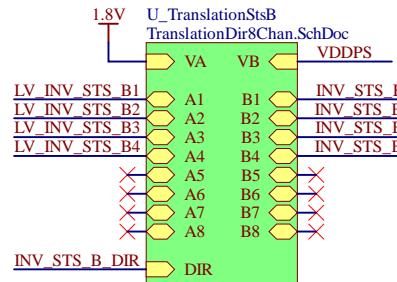
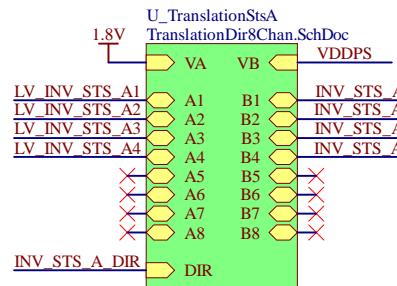
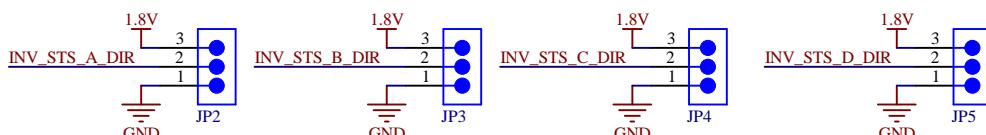
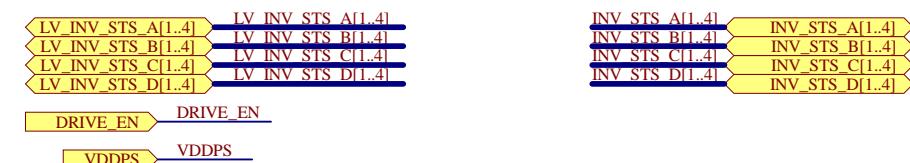
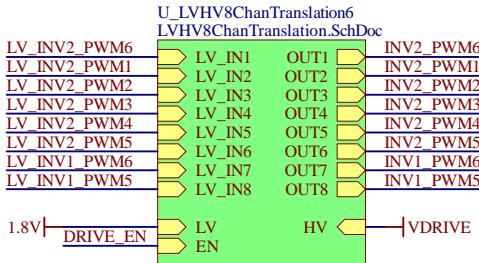
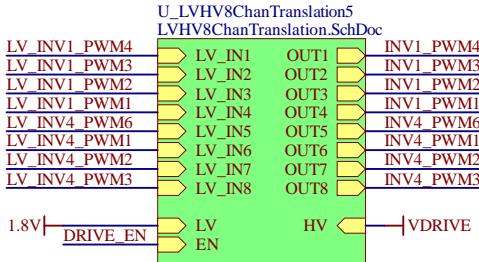
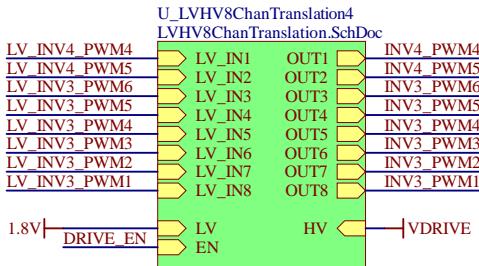
C



D

Title: <b>Inverter Connector</b>		Severson Group WEMPEC UWMadison
File: InverterConnector.SchDoc	Sheet: 18 of 26	
Revision: A	Time: 11:02:51 AM	
Date: 10/23/2020		Engineer: Nathan Petersen

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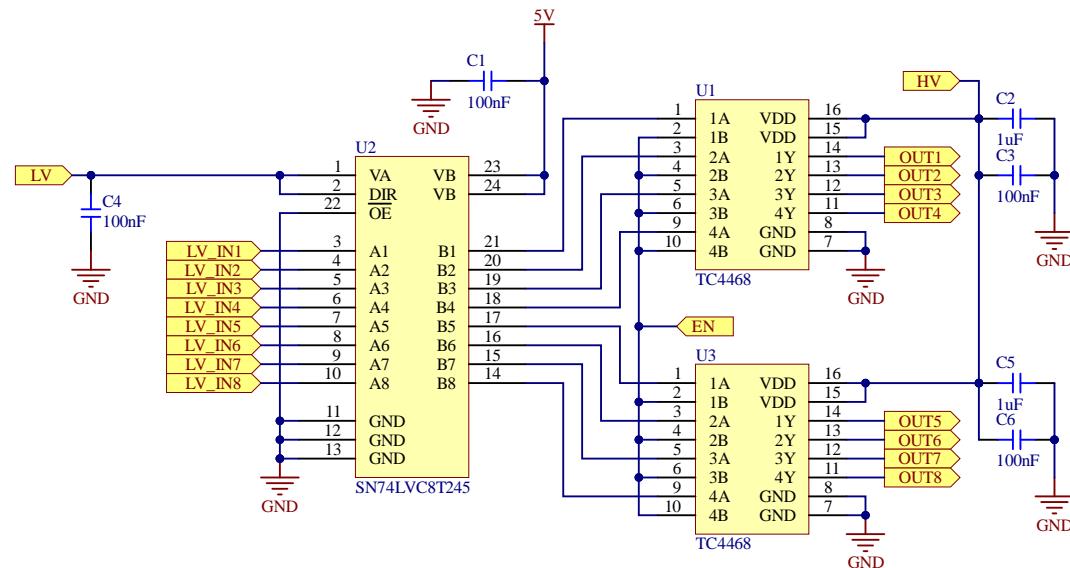
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C

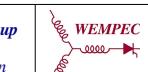
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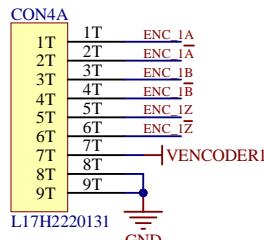
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Title: **8-channel LV to HV Translation**File: **LVHV8ChanTranslation.SchDoc** | Sheet: **20 of 26**Revision: **A** | Time: **11:02:51 AM** | Date: **10/23/2020**

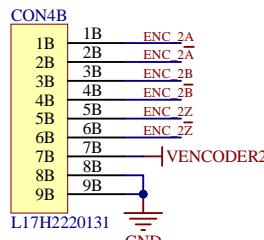
**Severson Group**  
WEMPEC  
UWMadison

Engineer: **Prasoon Sinha**

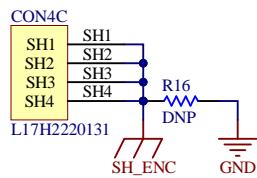
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ENC\_1A R10 ENC\_1A  
100  
ENC\_1B R11 ENC\_1B  
100  
ENC\_1Z R12 ENC\_1Z  
100

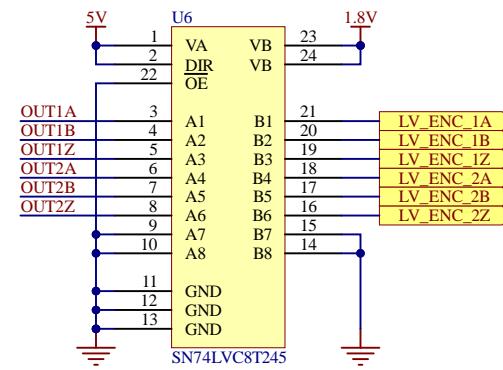
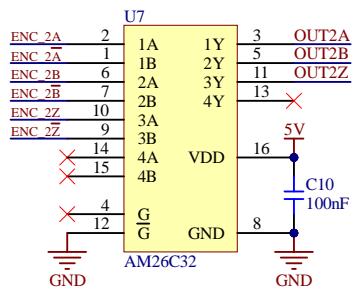
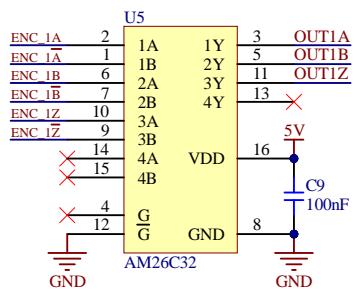


ENC\_2A R13 ENC\_2A  
100  
ENC\_2B R14 ENC\_2B  
100  
ENC\_2Z R15 ENC\_2Z  
100



JP6 1 5V VENCODER1  
2

JP7 1 5V VENCODER2  
2



5V C11 100nF C12 1.8V 100nF GND

Title: **Encoders**

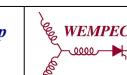
File: Encoder.SchDoc

Sheet: 21 of 26

Revision: A Time: 11:02:51 AM

Date: 10/23/2020

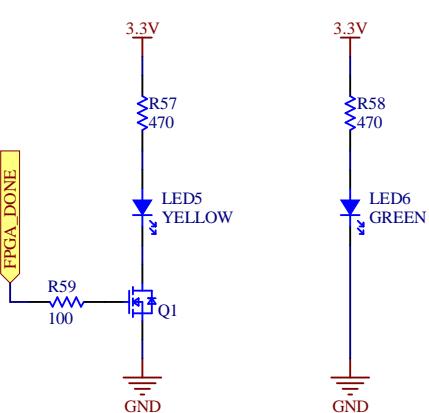
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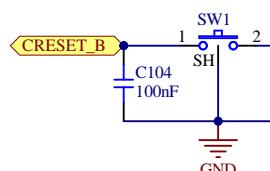
Engineer: Nathan Petersen

## FPGA STATUS LEDS

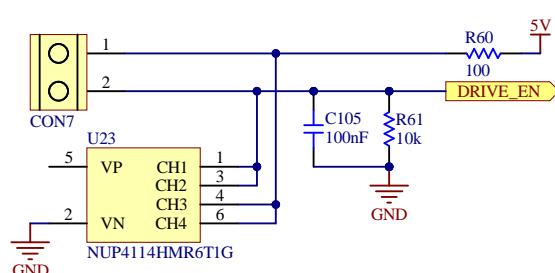
### FPGA DONE



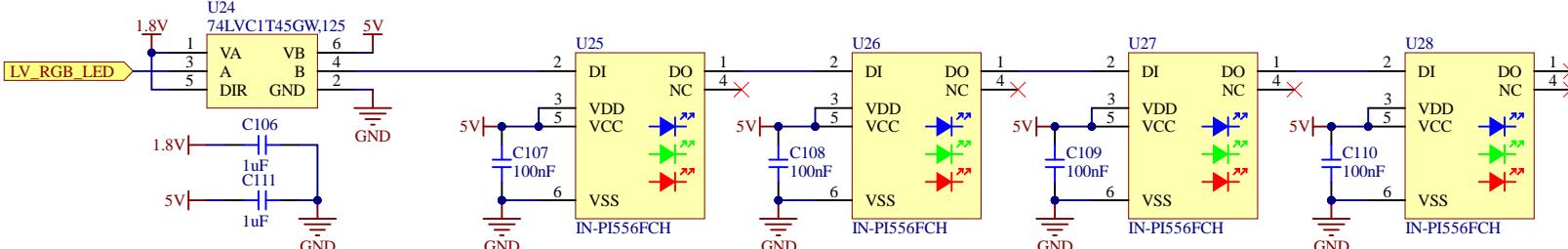
## RESET BUTTON



## DRIVE ENABLE (ESTOP)



## FPGA RGB LEDs

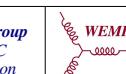


Title: **FPGA I/O Interface**

File: **FPGA\_IO.SchDoc** Sheet: **22 of 26**

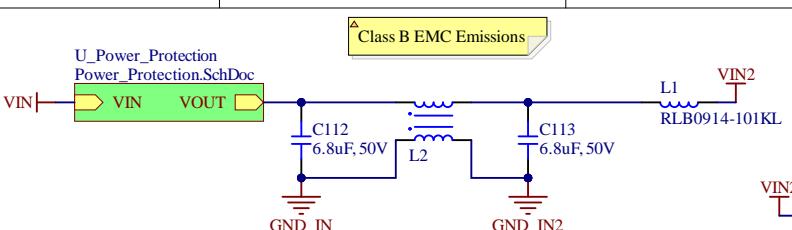
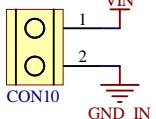
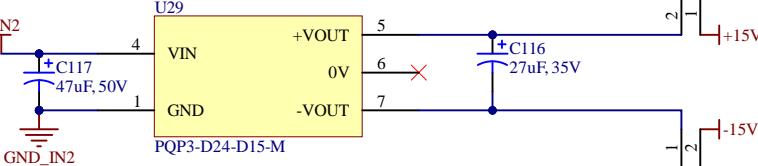
Revision: **A** Time: **11:02:51 AM** Date: **10/23/2020**

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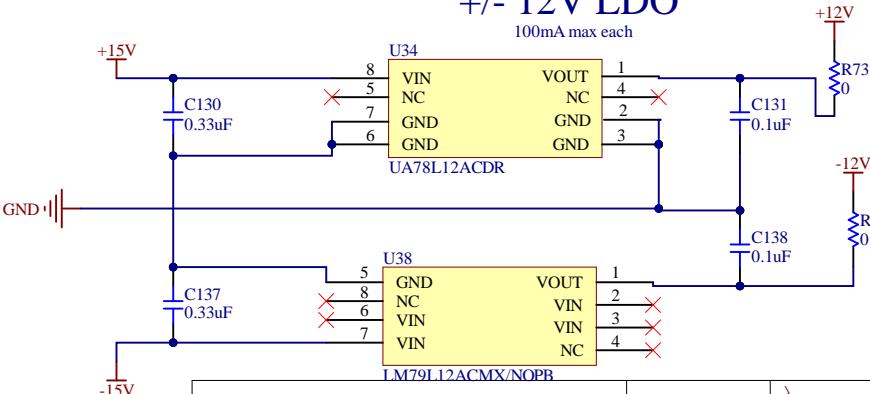
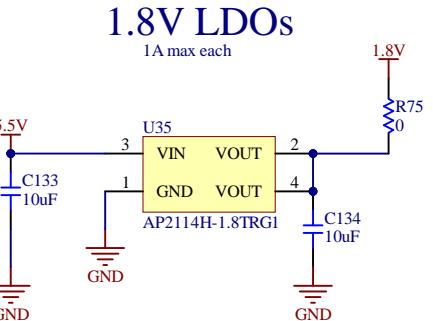
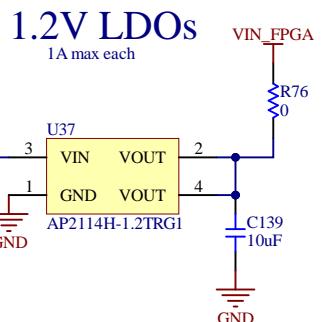
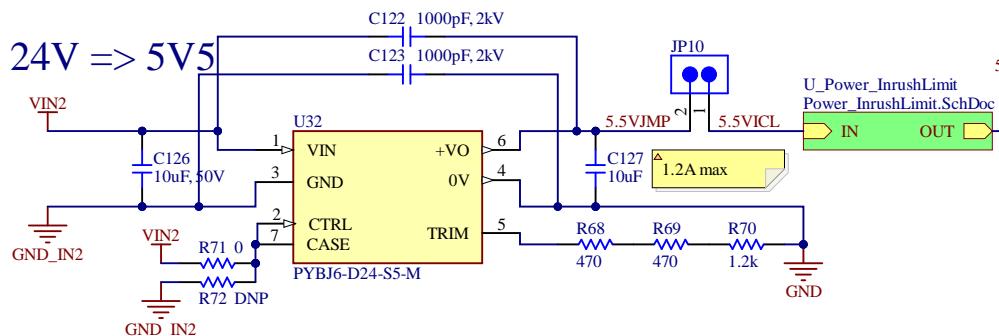
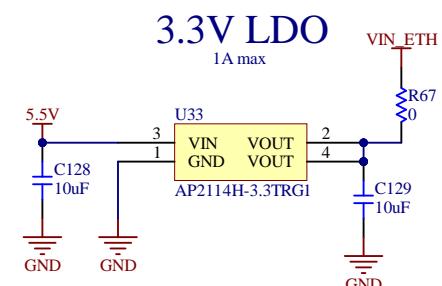
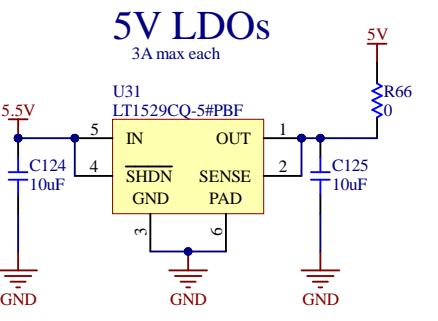


Engineer: **Prasoon Sinha**

VIN (assumed 24V DC)


 $24V \Rightarrow +15V$   
 $24V \Rightarrow -15V$ 


<b>A</b>	<table border="1"> <tr><td>5V</td><td>VIN_FPGA</td><td>&lt;=&gt; General</td></tr> <tr><td>3.3V</td><td></td><td>&lt;=&gt; General</td></tr> <tr><td>1.8V</td><td></td><td>&lt;=&gt; General</td></tr> <tr><td>2.048VREF</td><td></td><td>&lt;=&gt; ADC ref / SigCond1..8</td></tr> <tr><td>+/-15V</td><td></td><td>&lt;=&gt; Con1..4 / SigCond1..8</td></tr> <tr><td>VIN_ETH (3.3V)</td><td></td><td>&lt;=&gt; Ethernet Power Supply</td></tr> </table>	5V	VIN_FPGA	<=> General	3.3V		<=> General	1.8V		<=> General	2.048VREF		<=> ADC ref / SigCond1..8	+/-15V		<=> Con1..4 / SigCond1..8	VIN_ETH (3.3V)		<=> Ethernet Power Supply
5V	VIN_FPGA	<=> General																	
3.3V		<=> General																	
1.8V		<=> General																	
2.048VREF		<=> ADC ref / SigCond1..8																	
+/-15V		<=> Con1..4 / SigCond1..8																	
VIN_ETH (3.3V)		<=> Ethernet Power Supply																	
<b>B</b>	<p><b>3.3V LDO</b> 1A max</p> <p>U36</p> <p>VIN GND VOUT</p> <p>AP2114H-3.3TRGI</p> <p>3.3V</p> <p>R74</p> <p>C132 10uF</p> <p>GND</p> <p>C135 10uF</p> <p>GND</p>																		



A

A

B

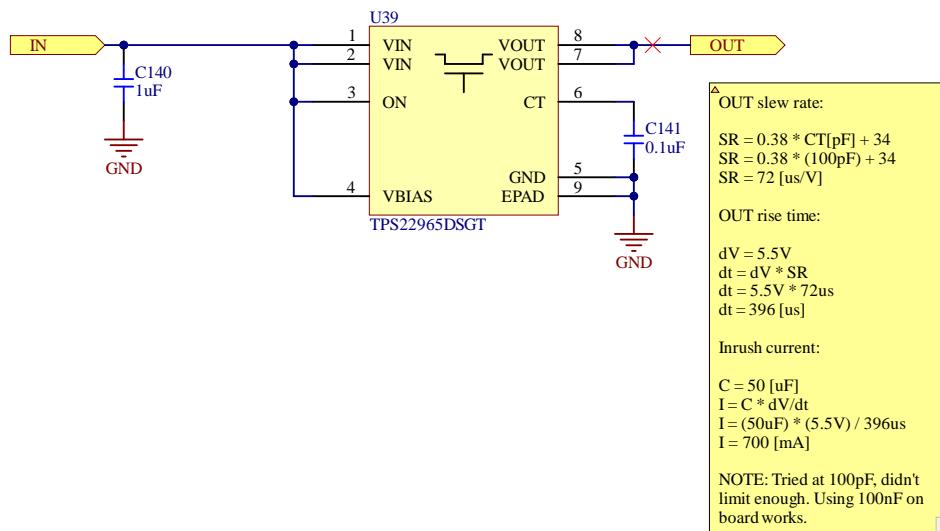
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C

C

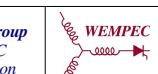
D

D

Title: **Inrush Current Limiter**

File: Power\_InrushLimit.SchDoc | Sheet: 24 of 26

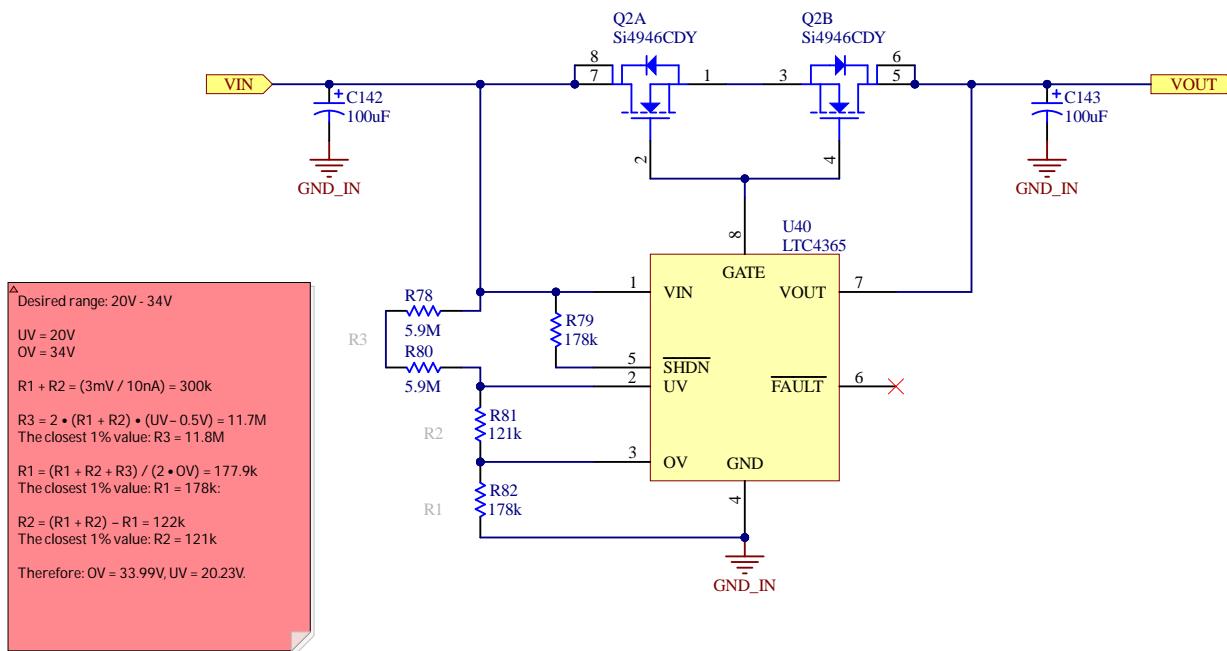
Revision: A | Time: 11:02:51 AM | Date: 10/23/2020

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A

A



B

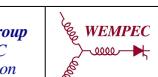
B

C

C

D

D

Title: **Power Protection**File: **Power\_Protection.SchDoc**Sheet: **25 of 26**Revision: **A** Time: **11:02:51 AM**Date: **10/23/2020**
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**4-40 Screws:**

SCREW1 SCREW2 SCREW3 SCREW4 SCREW5 SCREW6 SCREW7 SCREW8 SCREW9 SCREW10

**4-40 Standoffs:**

STANDOFF1 STANDOFF2 STANDOFF3 STANDOFF4 STANDOFF5 STANDOFF6 STANDOFF7 STANDOFF8 STANDOFF9 STANDOFF10

**Mouting Holes:**