

RGB LED, 4x switches, 1x button, E-STOP



BOARD I/O

24 channels
5V/3.3V
I/O



GPIO

ANALOG
INPUTS

DRIVE
OUTPUTS

ENCODER

16 channels
+/-10V diff.
pair inputs



48 channels
(8 full
inverters)



Quadrature
input (A,B,Z)



PicoZed

7030

U_PicoZed
PicoZed.SchDoc

JTAG

ETHERNET

USB OTG

USB UART

Power inputs
to board



24V

VDRIVE

-15V +15V 5V 3.3V 2.5V 1.8V

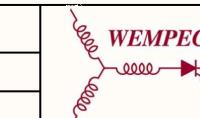
POWER

Title: AMDC

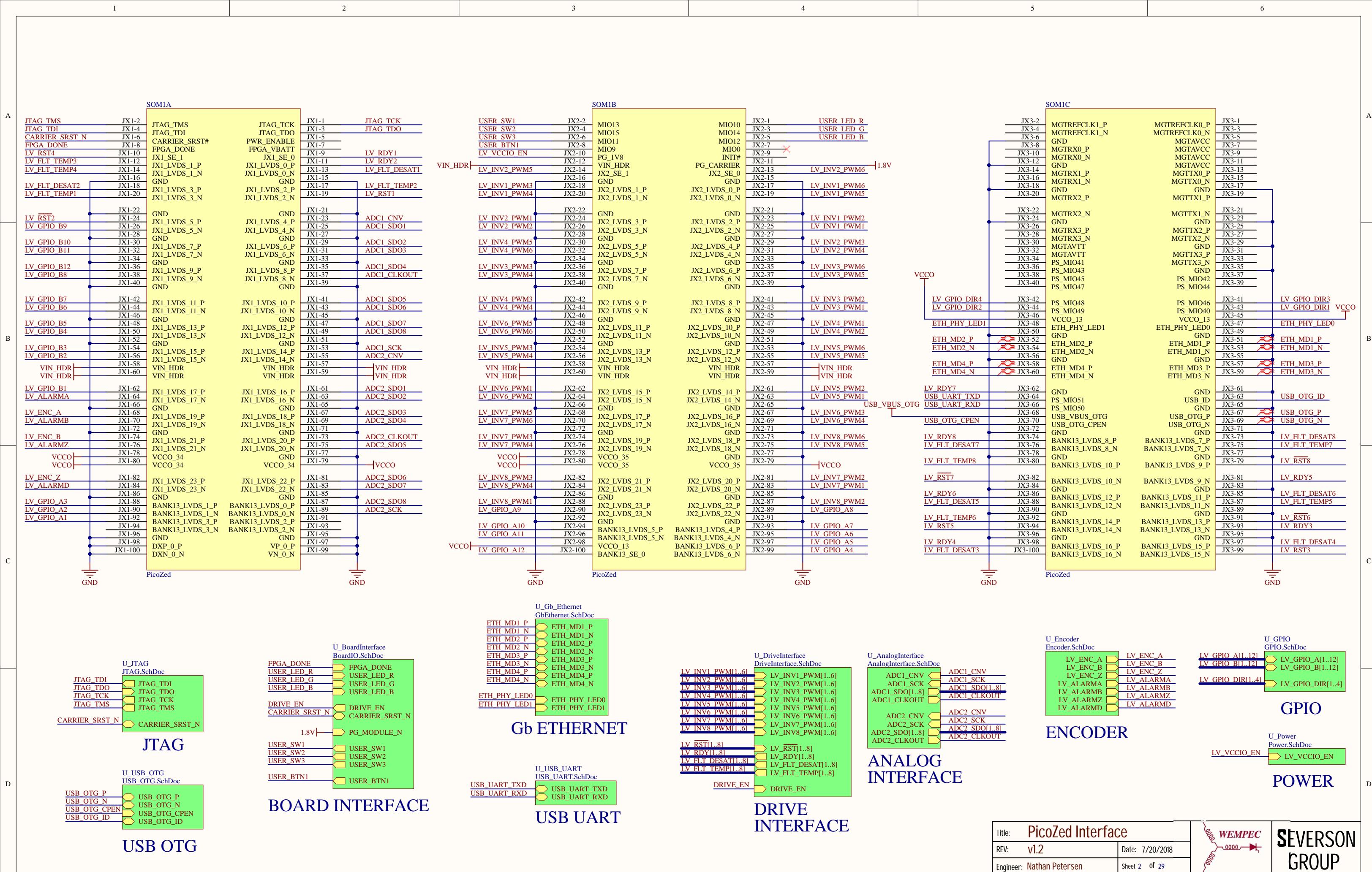
REV: v1.2

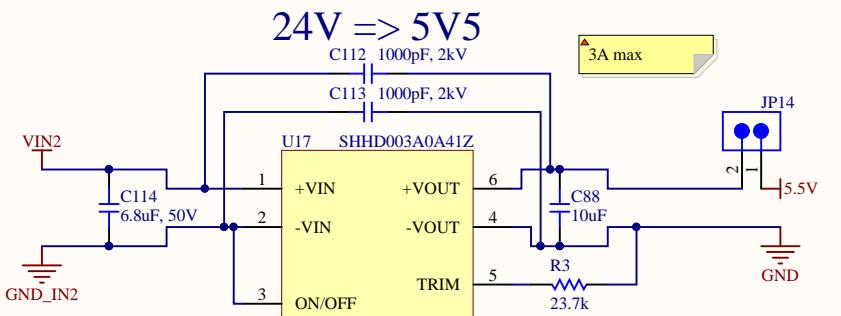
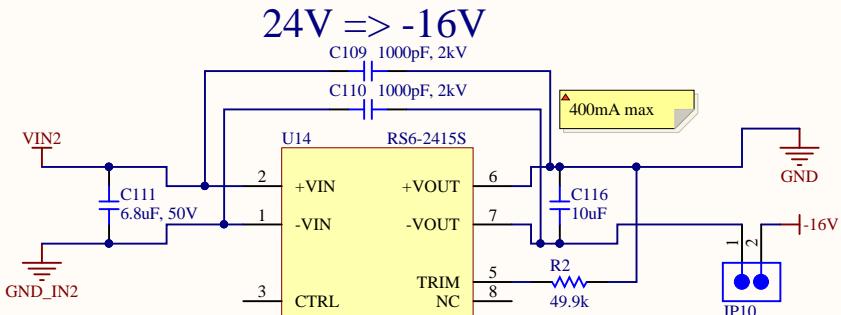
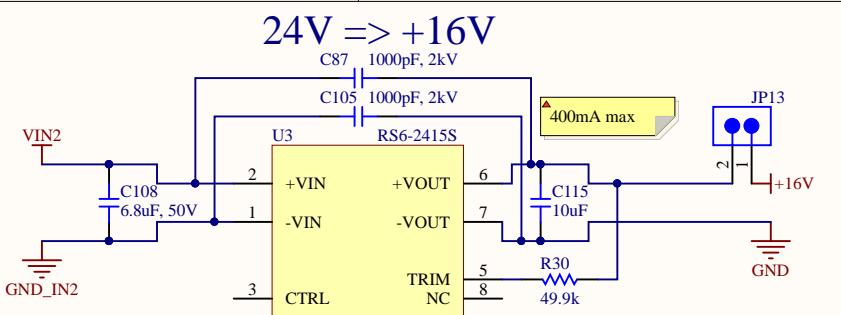
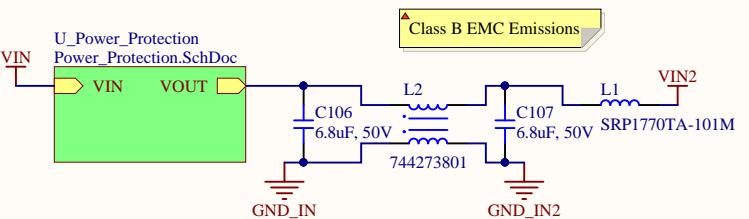
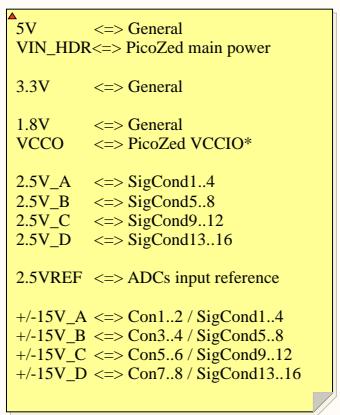
Date: 7/20/2018

Engineer: Nathan Petersen

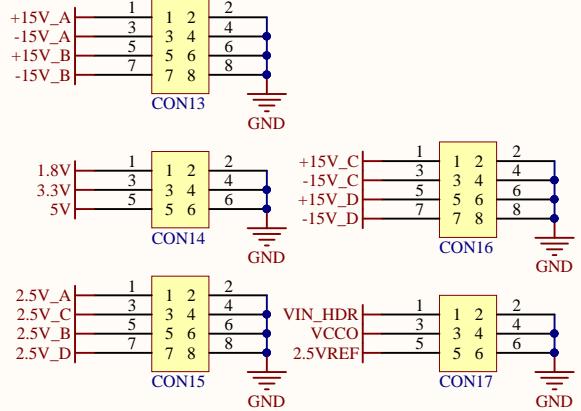


SEVERSON
GROUP

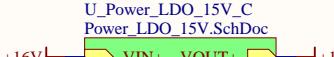
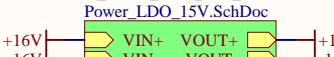
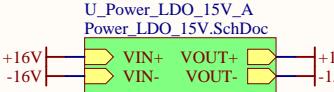




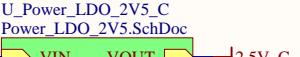
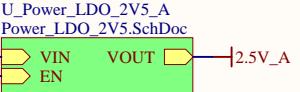
VOLTAGE HEADERS



$\pm 15V$ LDOs
200mA max each



$2.5V$ LDOs
250mA max each



$1.8V$ LDOs
3A max each



$3.3V$ LDOs
3A max each



$5V$ LDOs
3A max each



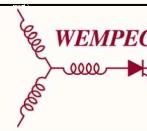
Title: Power

REV: v1.2

Date: 7/20/2018

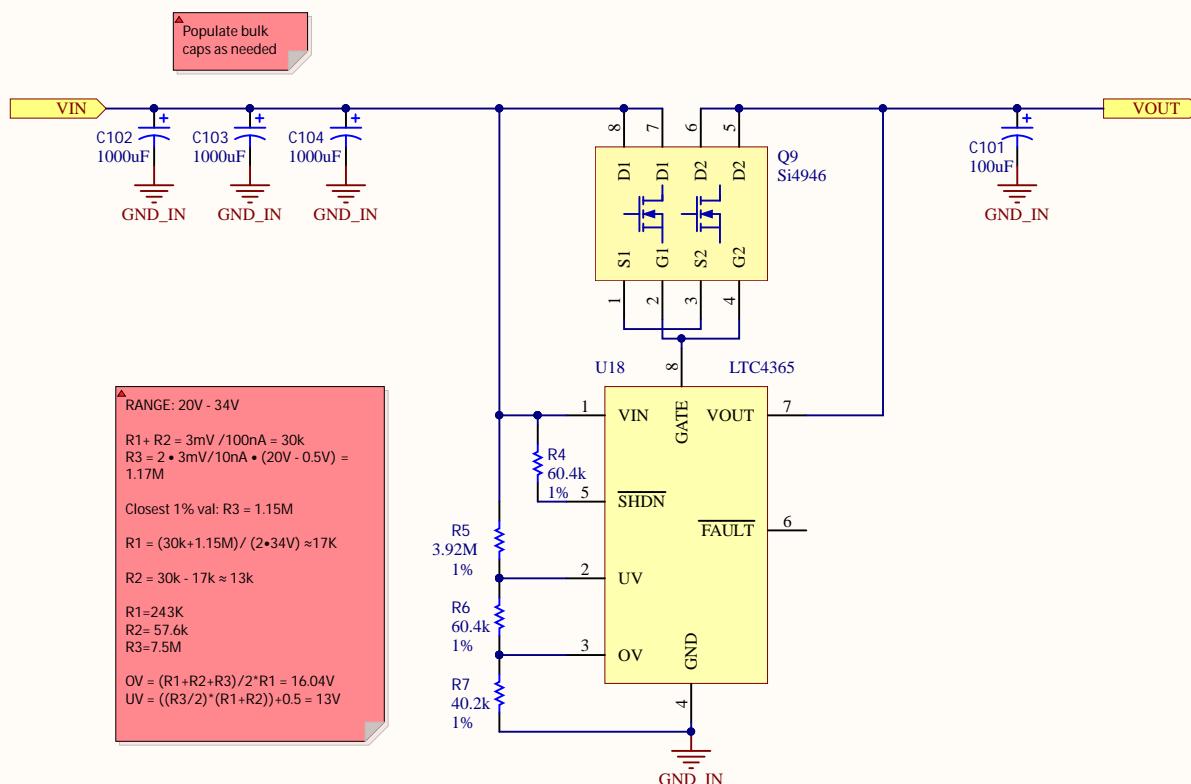
Engineer: Jason Sylvestre

Sheet 3 of 29



SEVERSON
GROUP

A



B

C

D

A

B

C

D

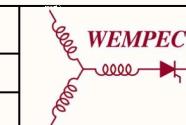
Title: Power Protection

REV: v1.2

Date: 7/20/2018

Engineer: Jason Sylvestre

Sheet 4 of 29

SEVERSON
GROUP

A

A

B

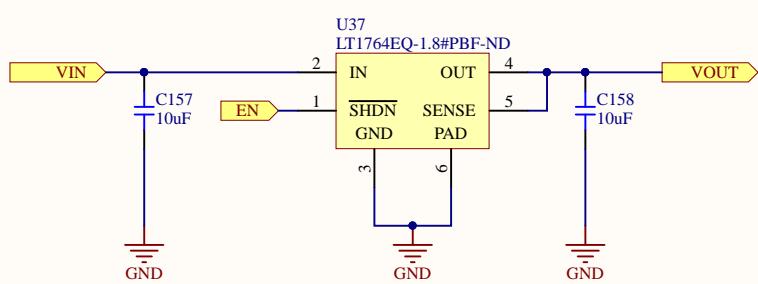
B

C

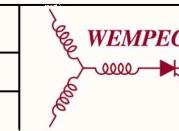
C

D

D



Title: 1.8V LDO	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 5 of 29

**SEVERSON
GROUP**

A

A

B

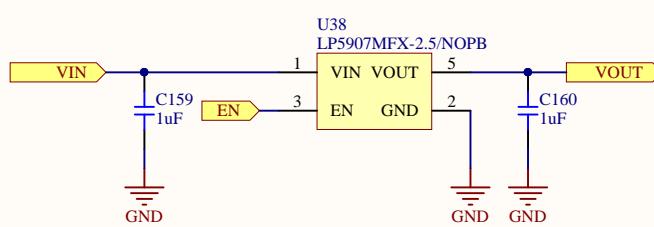
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C

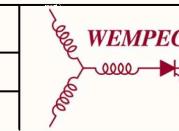
C

D

D



Title: 2.5V LDO	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 6 of 29



**SEVERSON
GROUP**

A

A

B

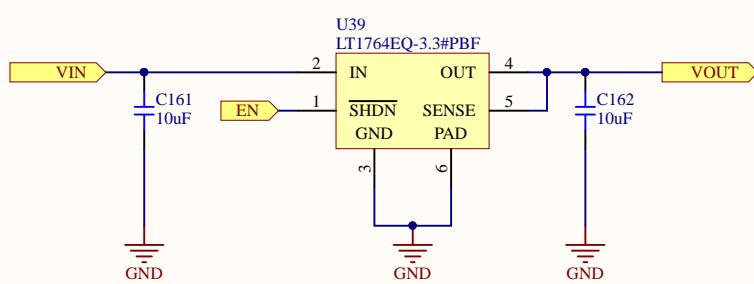
B

C

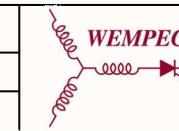
C

D

D



Title: 3.3V LDO	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 7 of 29

**SEVERSON
GROUP**

A

A

B

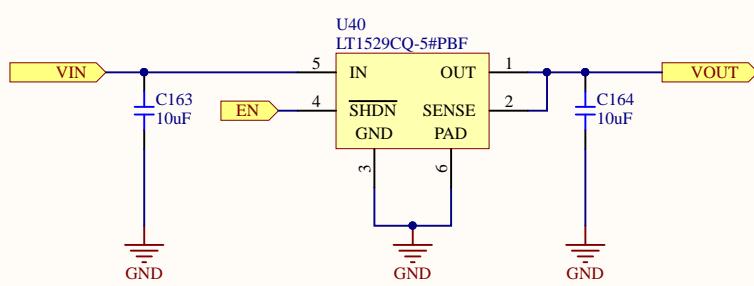
B

C

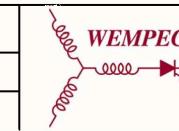
C

D

D



Title: 5V LDO	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 8 of 29



**SEVERSON
GROUP**

A

A

B

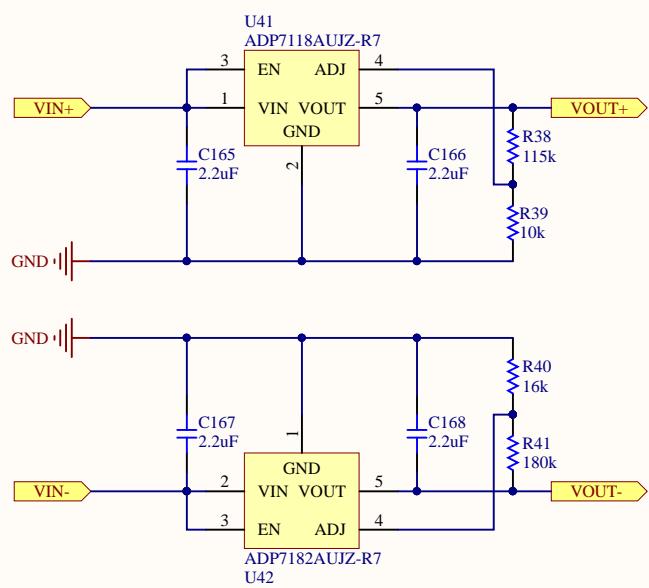
B

C

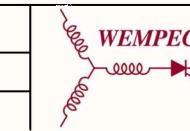
C

D

D



Title: +/-15V LDO	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 9 of 29



SEVERSON
GROUP

A

A

B

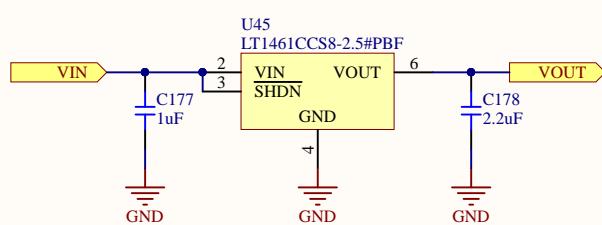
B

C

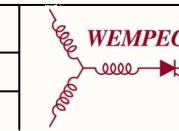
C

D

D



Title: 2.5V Reference	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 10 of 29



**SEVERSON
GROUP**

A

A

B

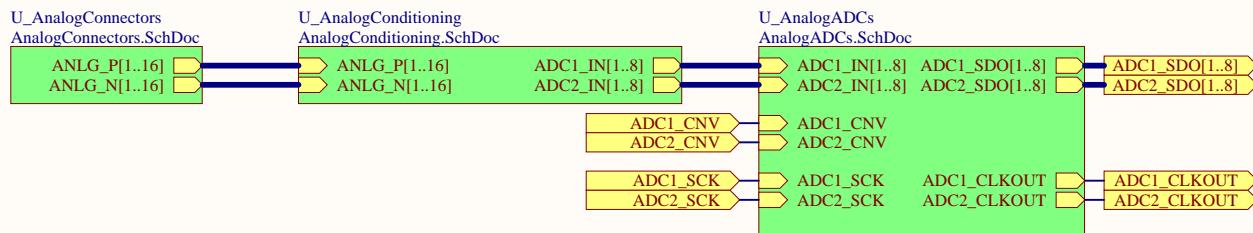
B

C

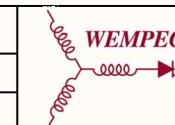
C

D

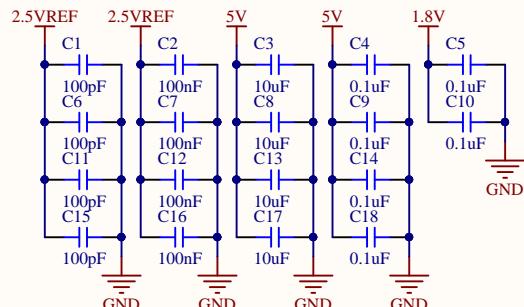
D



Title: Analog Interface	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 11 of 29

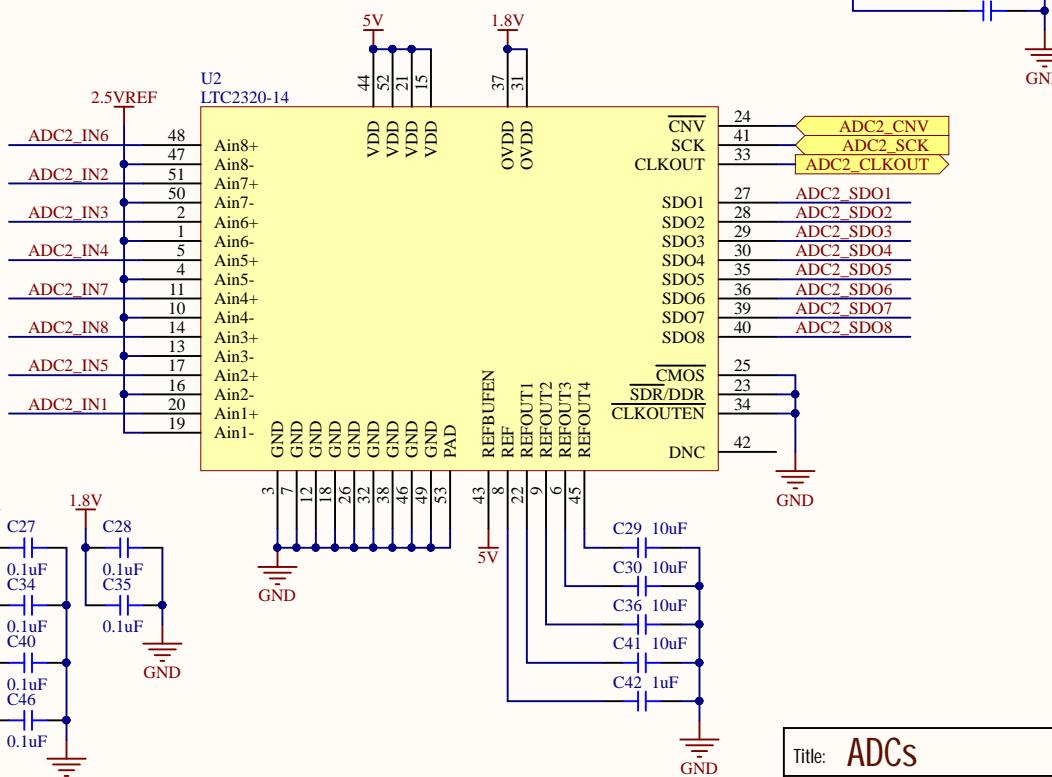

**SEVERSON
GROUP**

A

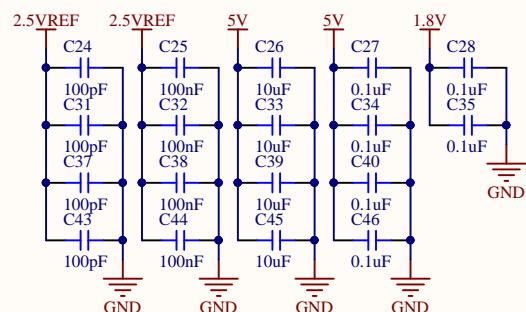


B

ADC1_IN[1..8] **ADC1_IN[1..8]**
ADC2_IN[1..8] **ADC2_IN[1..8]**



C



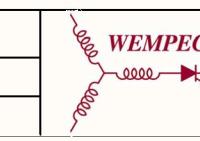
D

Title: **ADCs**

REV: **v1.2**

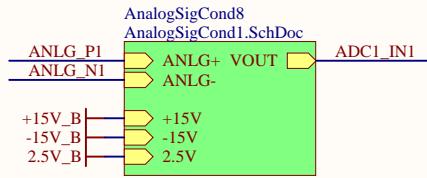
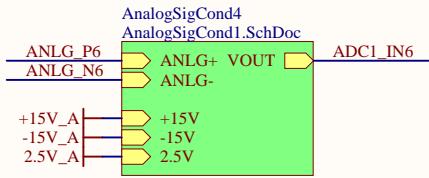
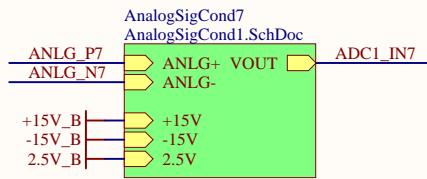
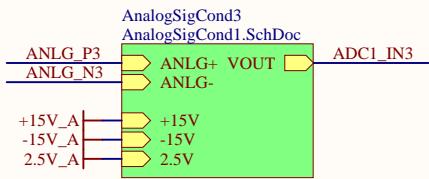
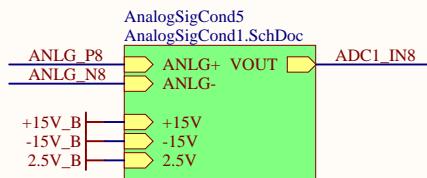
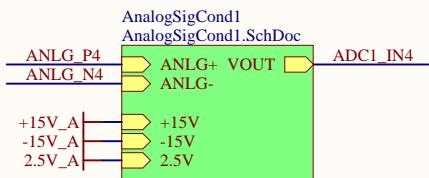
Date: **7/20/2018**

Engineer: **Nathan Petersen**



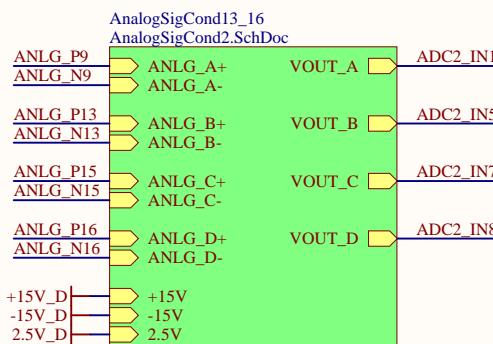
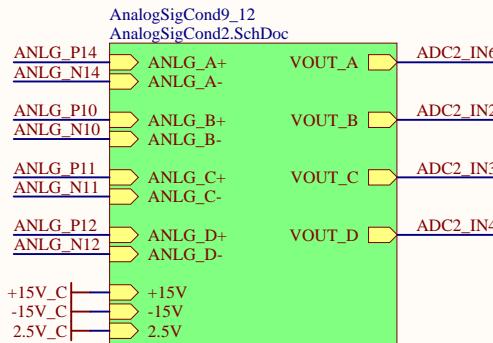
**SEVERSON
GROUP**

A



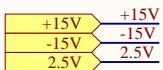
ANLG_P[1..16] ANLG_P[1..16]
ANLG_N[1..16] ANLG_N[1..16]

ADC1_IN[1..8] ADC1_IN[1..8]
ADC2_IN[1..8] ADC2_IN[1..8]



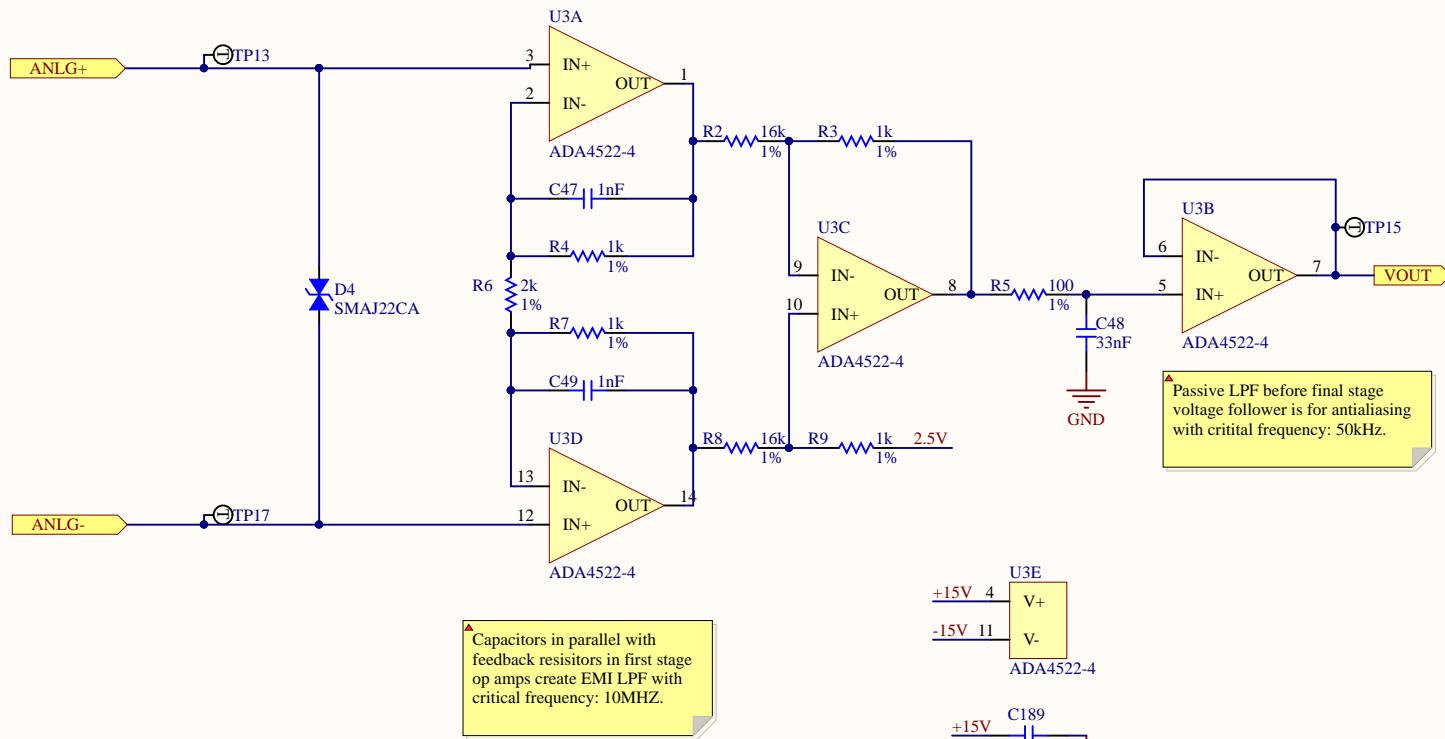
A

A



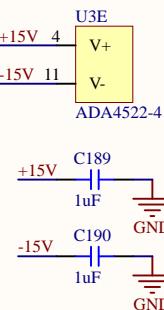
B

B



C

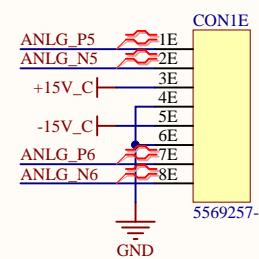
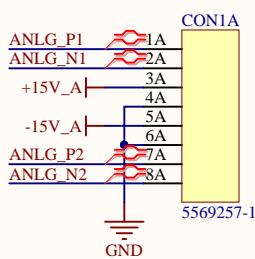
C



D

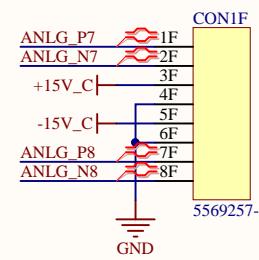
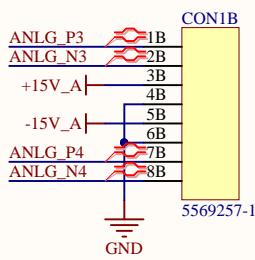
D

A

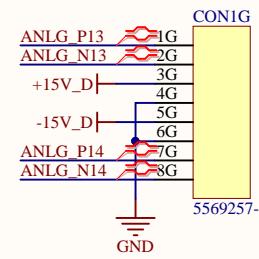
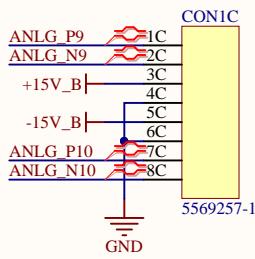


B

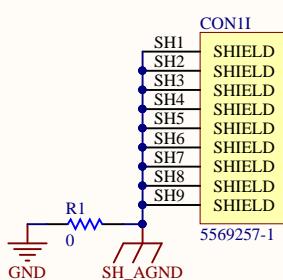
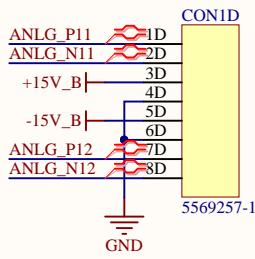
ANLG_P[1..16] — **ANLG_P[1..16]**
ANLG_N[1..16] — **ANLG_N[1..16]**



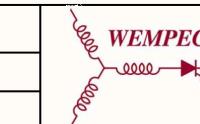
C



D

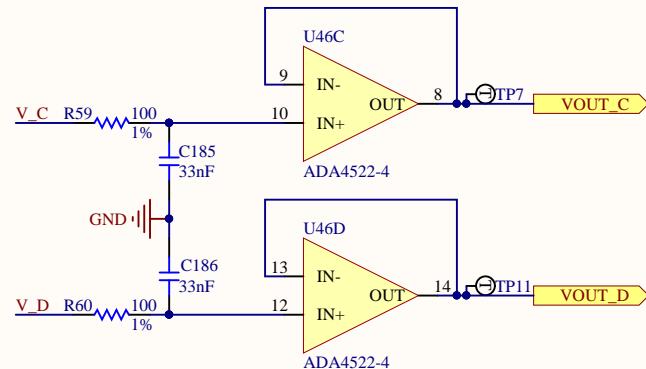
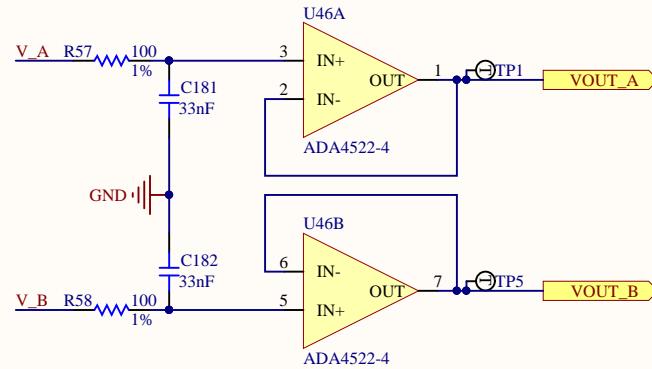
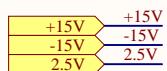
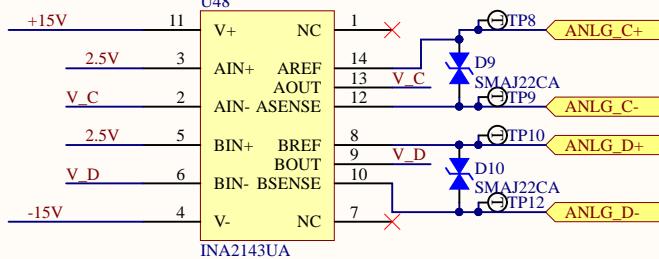
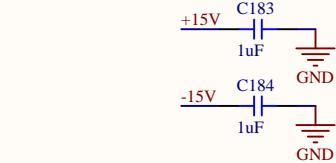
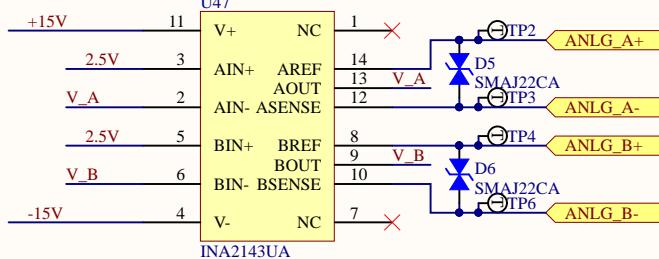
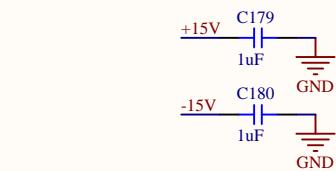


Title: Analog RJ45 Connectors	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 15 of 29



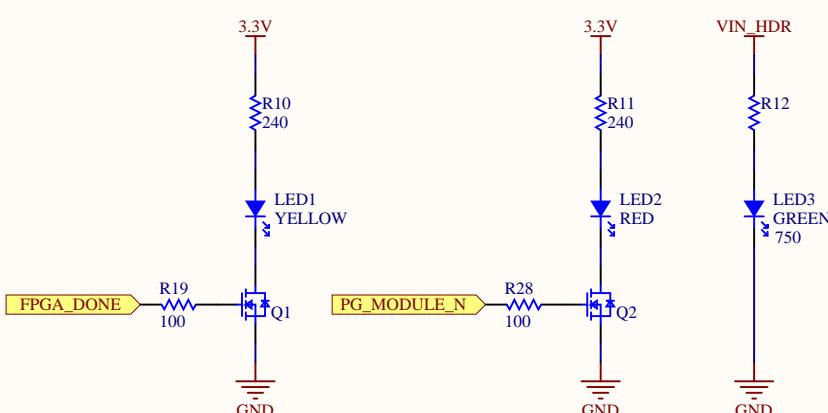
SEVERSON
GROUP

A

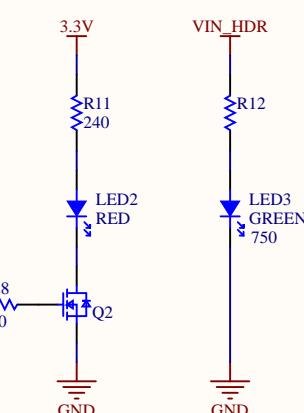


STATUS LEDS

FPGA DONE



PG MODULE

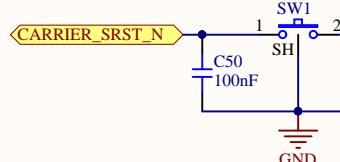


VIN_HDR

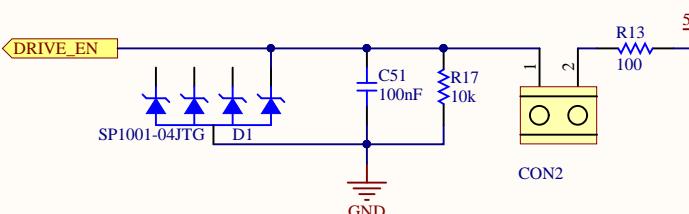


CONTROL BUTTON

CARRIER_SRST_N

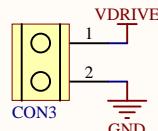


DRIVE ENABLE (ESTOP)

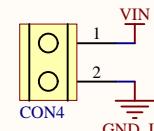


POWER CONNECTORS

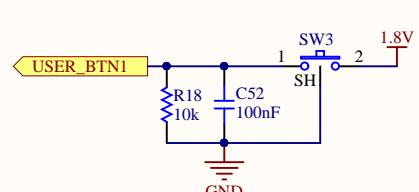
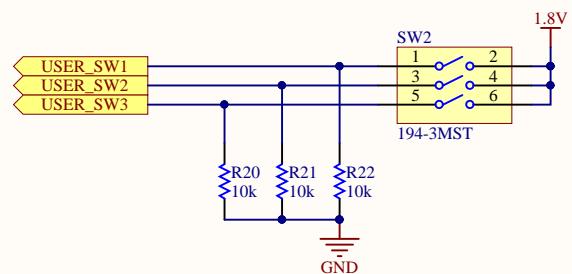
VDRIVE



VIN (assumed 24V DC)



USER INPUT

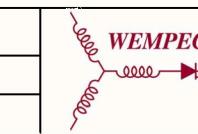


Title: Board I/O

REV: v1.2

Date: 7/20/2018

Engineer: Nathan Petersen



SEVERSON
GROUP

A

A

B

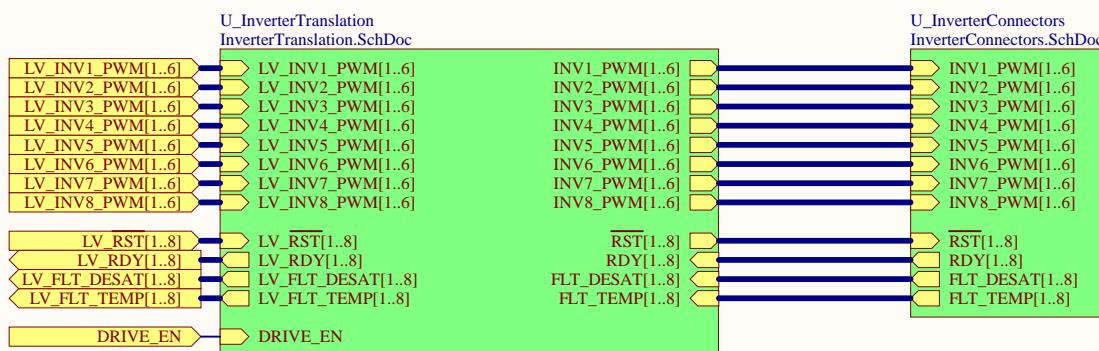
B

C

C

D

D

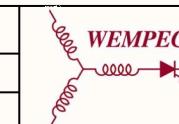


Title: Drive Interface

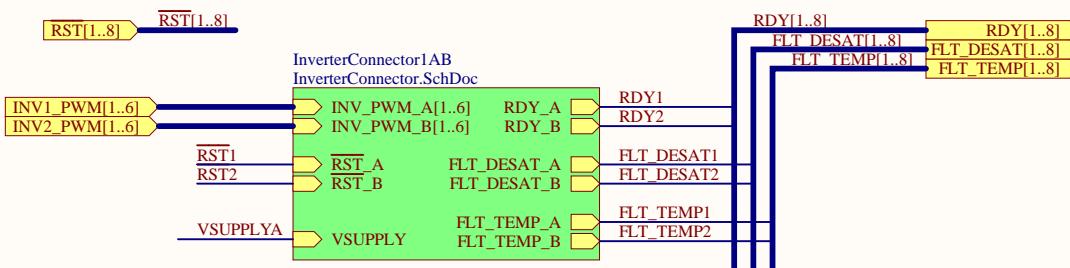
REV: v1.2

Date: 7/20/2018

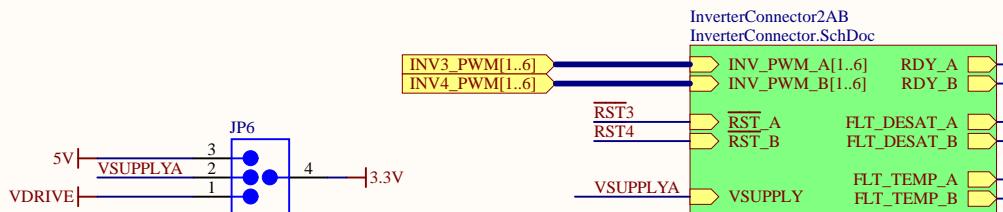
Engineer: Nathan Petersen


SEVERSON
GROUP

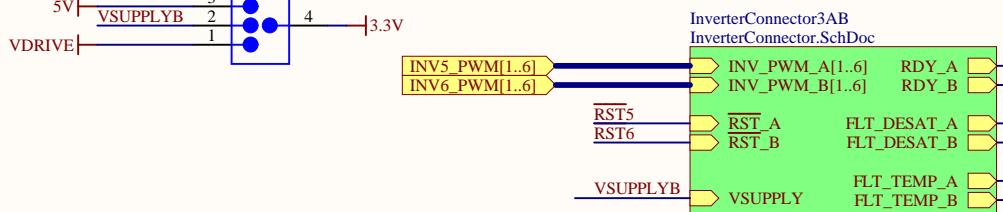
A



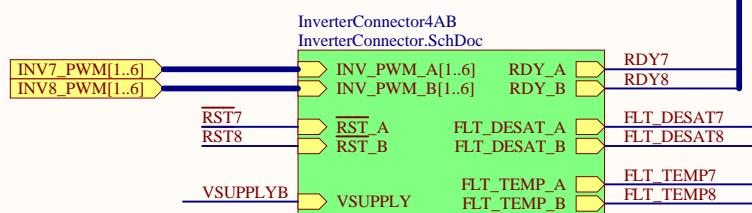
B



A



B



C

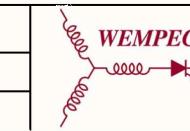
D

Title: Inverter Connectors

REV: v1.2

Date: 7/20/2018

Engineer: Nathan Petersen


SEVERSON
GROUP

A

A

VSUPPLY

INV_PWM_A[1..6]

INV_PWM_A1 1A
INV_PWM_A2 2A
INV_PWM_A3 3A
INV_PWM_A4 4A
INV_PWM_A5 5A
INV_PWM_A6 6A

GND || 7A
RST_A 8A
RDY_A 9A
FLT DESAT_A 10A
FLT TEMP_A 11A
VSUPPLY 13A
GND || 14A
GND || 15A

CON8A

178-015-513R571

INV_PWM_B[1..6]

INV_PWM_B1 1B
INV_PWM_B2 2B
INV_PWM_B3 3B
INV_PWM_B4 4B
INV_PWM_B5 5B
INV_PWM_B6 6B

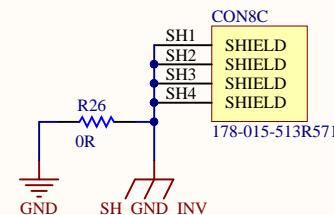
GND || 7B
RST_B 8B
RDY_B 9B
FLT DESAT_B 10B
FLT TEMP_B 11B
VSUPPLY 13B
GND || 14B
GND || 15B

CON8B

178-015-513R571

B

B



C

C

D

D

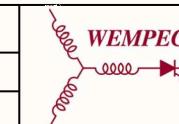
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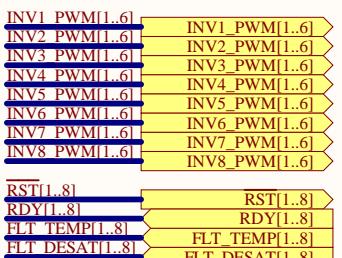
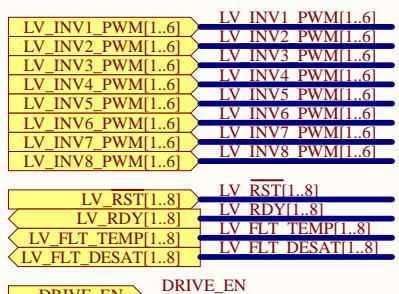
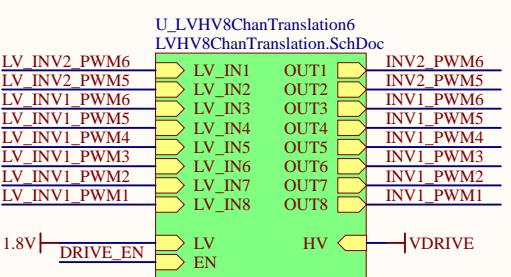
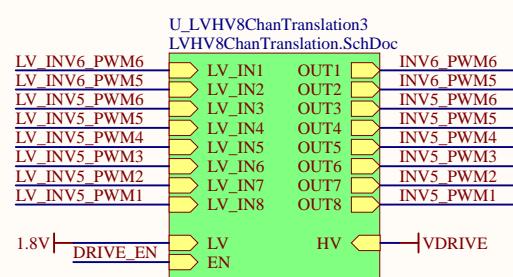
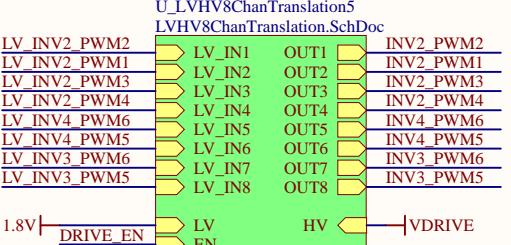
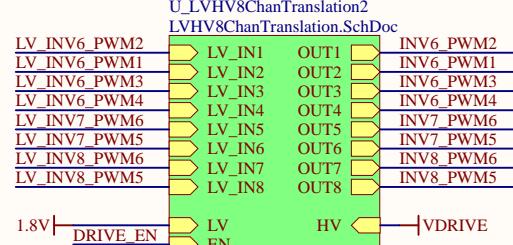
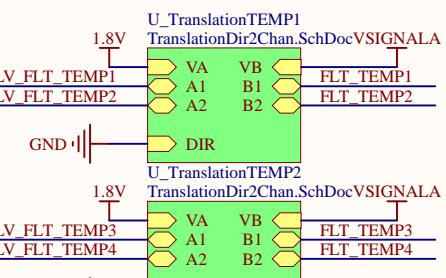
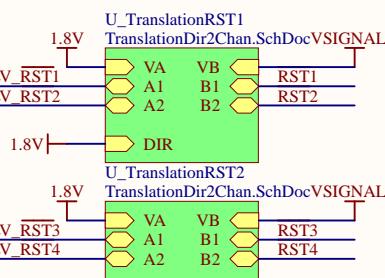
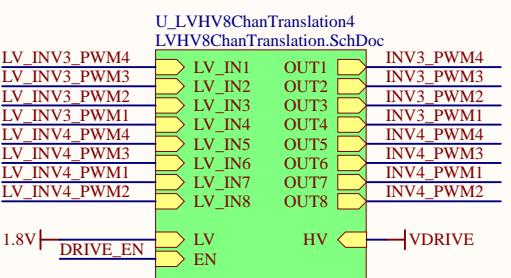
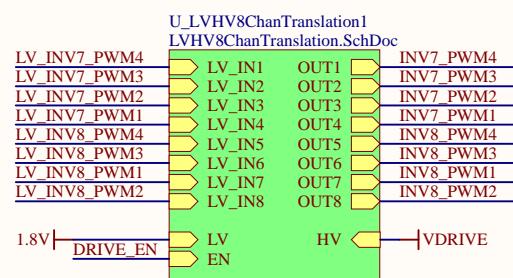
REV: v1.2

Date: 7/20/2018

Engineer: Nathan Petersen

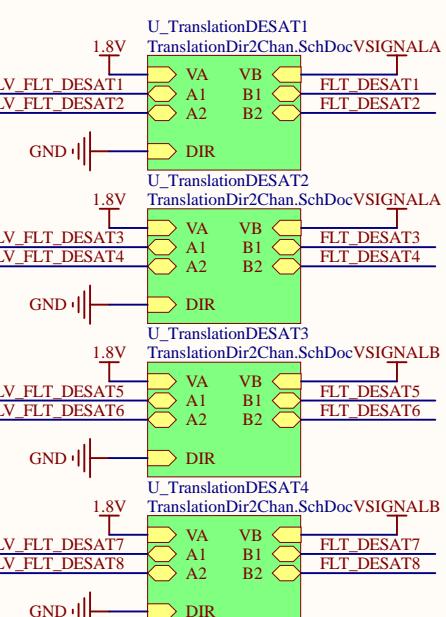
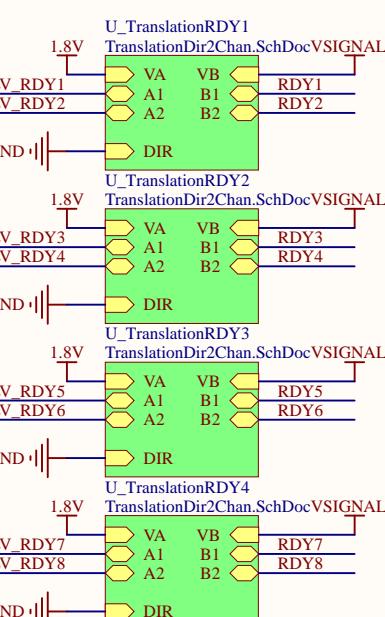
Sheet 20 of 29

SEVERSON
GROUP



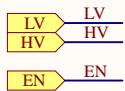
V SIGNALA
JP8

V SIGNALB
JP16



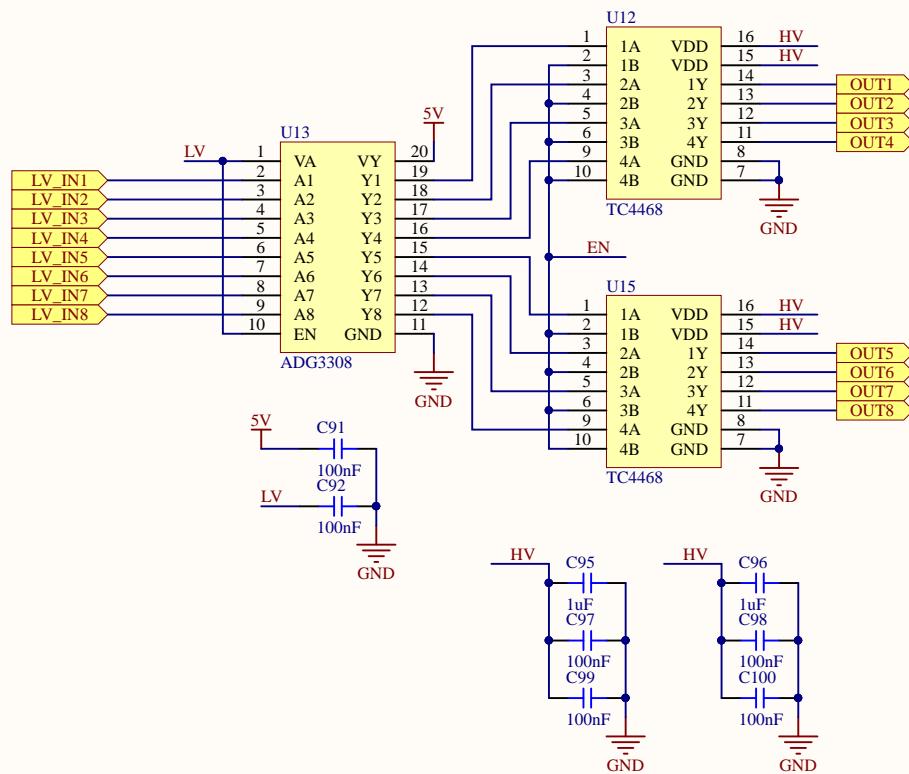
A

A



B

B



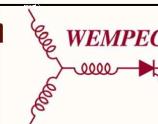
C

C

D

D

Title: 8-channel LV to HV Translation	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 22 of 29



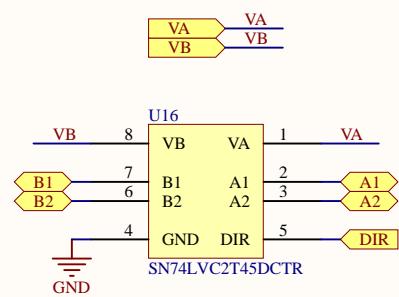
SEVERSON
GROUP

A

A

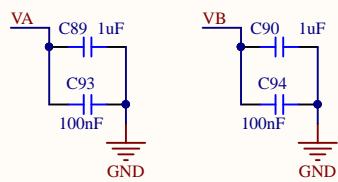
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B



C

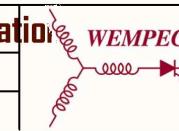
C



D

D

Title: 2-Channel Directional Translation	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 23 of 29



**SEVERSON
GROUP**

A

B

C

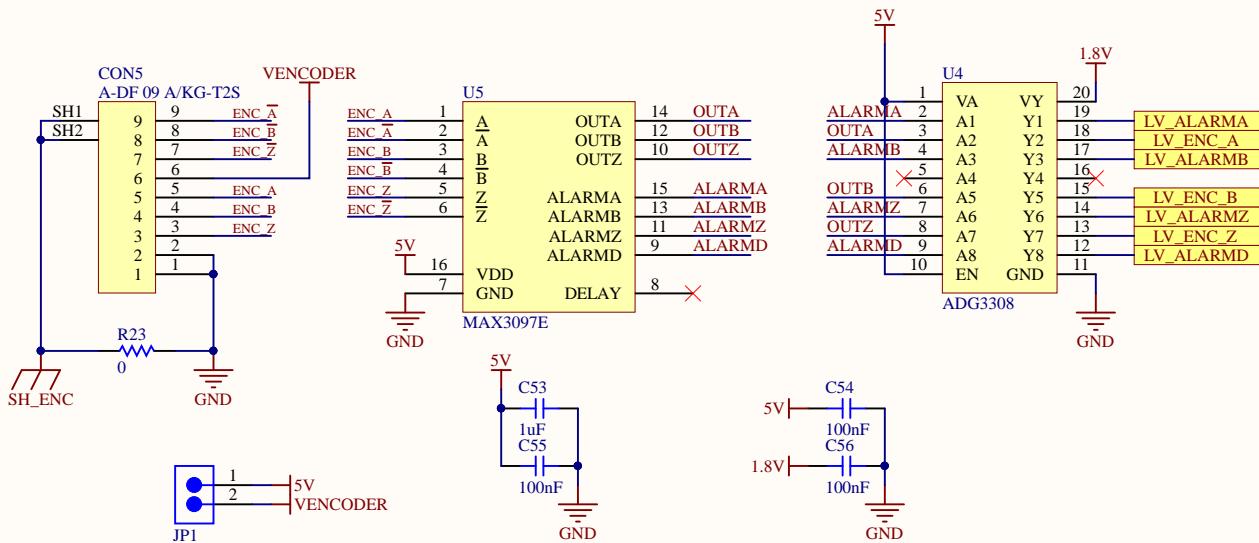
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A

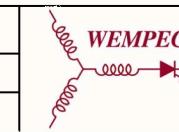
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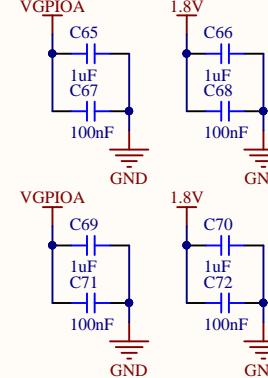
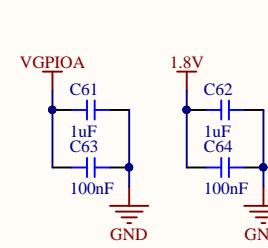
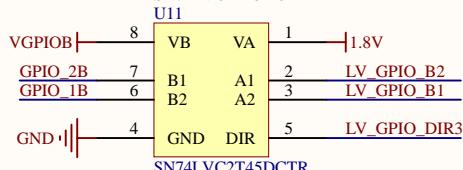
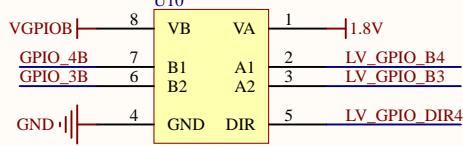
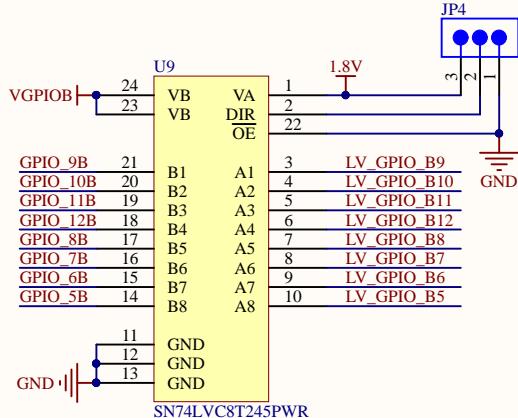
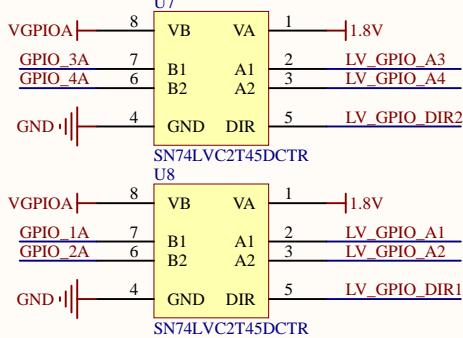
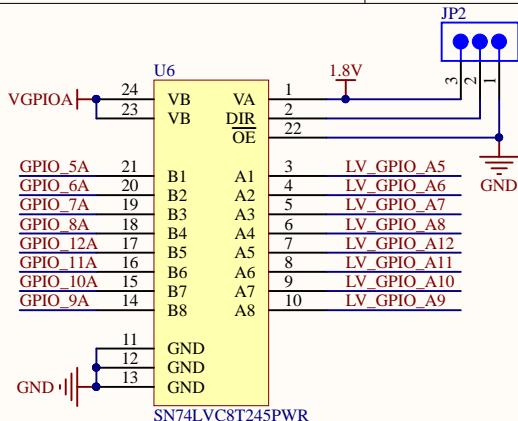
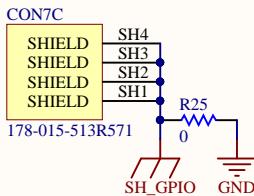
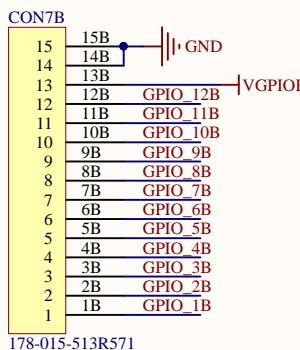
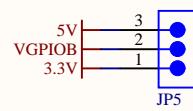
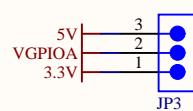
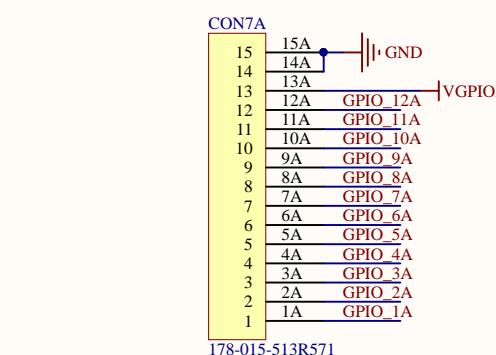
C

D

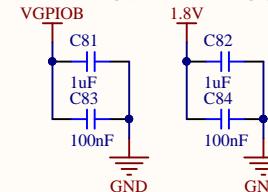
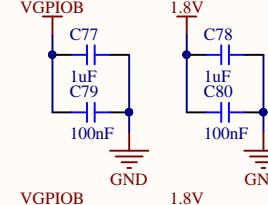
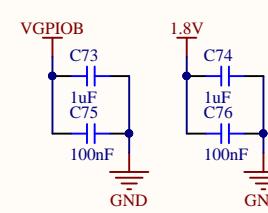


Title: Encoder	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 24 of 29


**SEVERSON
GROUP**



LV_GPIO_DIR[1..4] LV_GPIO_DIR[1..4]
LV_GPIO_A[1..12] LV_GPIO_A[1..12]
LV_GPIO_B[1..12] LV_GPIO_B[1..12]



4

Title: **GPIO**
Rev: **v1.2** Date: **7/20/2018**
Engineer: **Nathan Petersen** Sheet **25 of 29**

WEMPEC **SEVERSON GROUP**

A

A

B

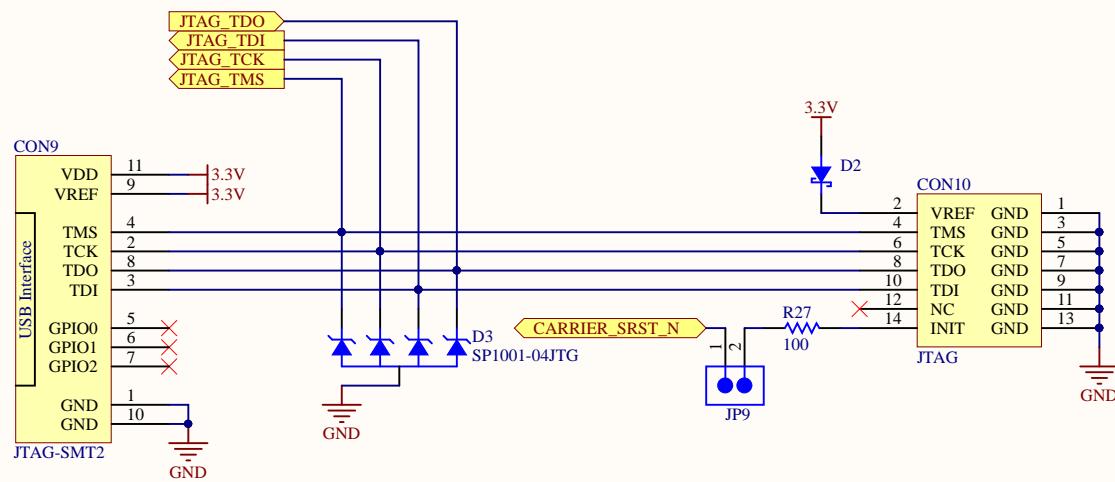
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C

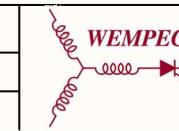
C

D

D



Title: JTAG	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 26 of 29


**SEVERSON
GROUP**

A

A

B

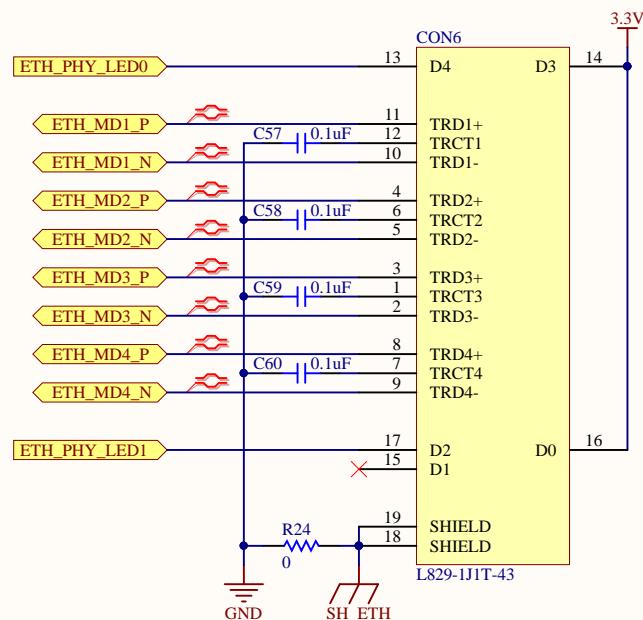
B

C

C

D

D



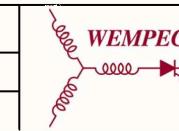
Title: SoM Gb Ethernet

REV: v1.2

Date: 7/20/2018

Engineer: Nathan Petersen

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SEVERSON
GROUP

A

A

B

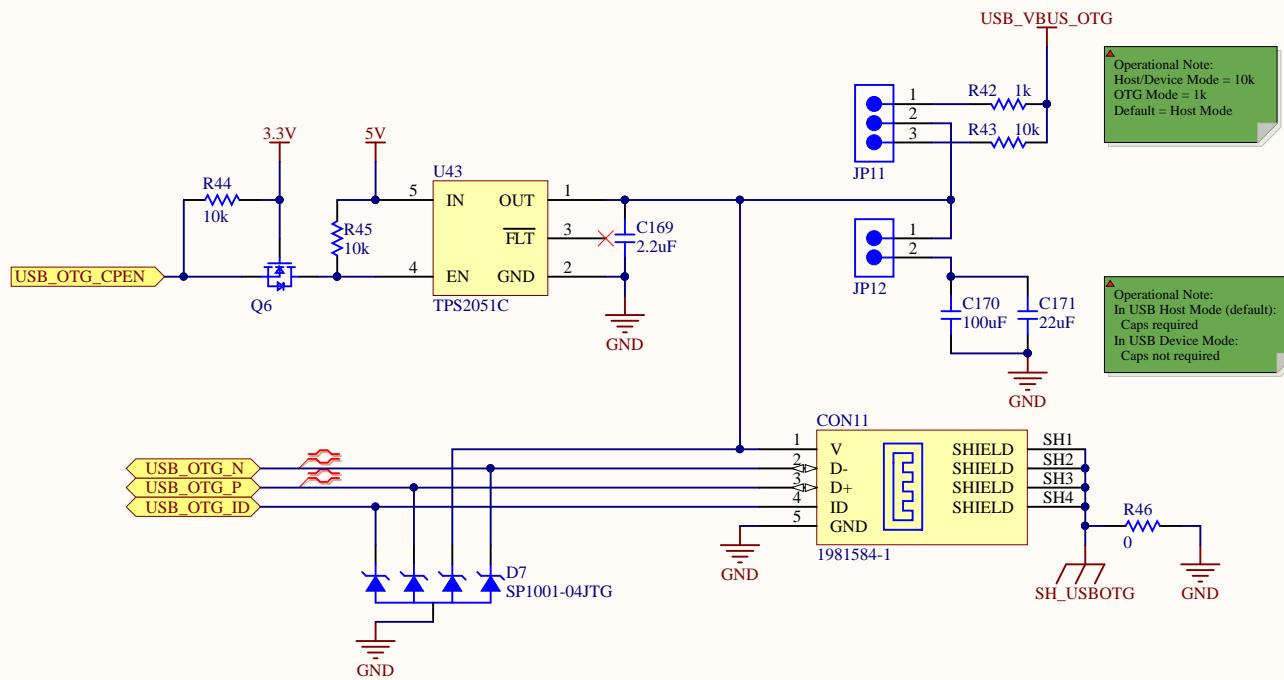
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C

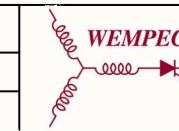
C

D

D



Title: USB OTG	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 28 of 29


**SEVERSON
GROUP**

A

A

B

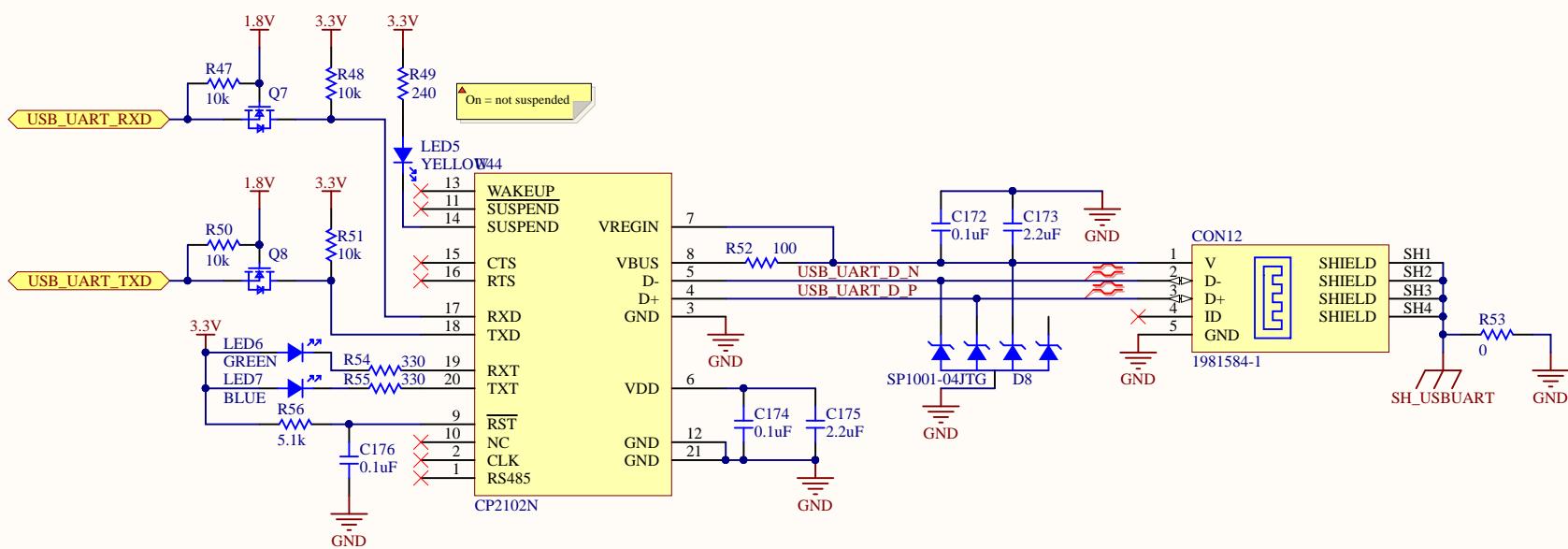
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C

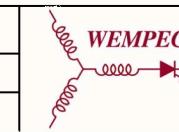
C

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D



Title: USB UART	
REV: v1.2	Date: 7/20/2018
Engineer: Nathan Petersen	Sheet 29 of 29


**SEVERSON
GROUP**