

4x RGB LEDs, E-STOP



BOARD I/O

4x GPIO ports
each with
3 diff inputs,
3 diff outputs

GPIO

8x channel
+/-10V diff.
pair inputs

ANALOG INPUTS

8x full 3-phase
2-level inverters

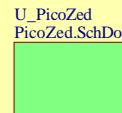
DRIVE OUTPUTS

2x quadrature
input (A,B,Z)

ENCODER

PicoZed

7030



JTAG / UART



ETHERNET



EEPROM

A

A

B

B

C

C

D

D

24V -15V +15V 5V 3.3V 2.048V 1.8V

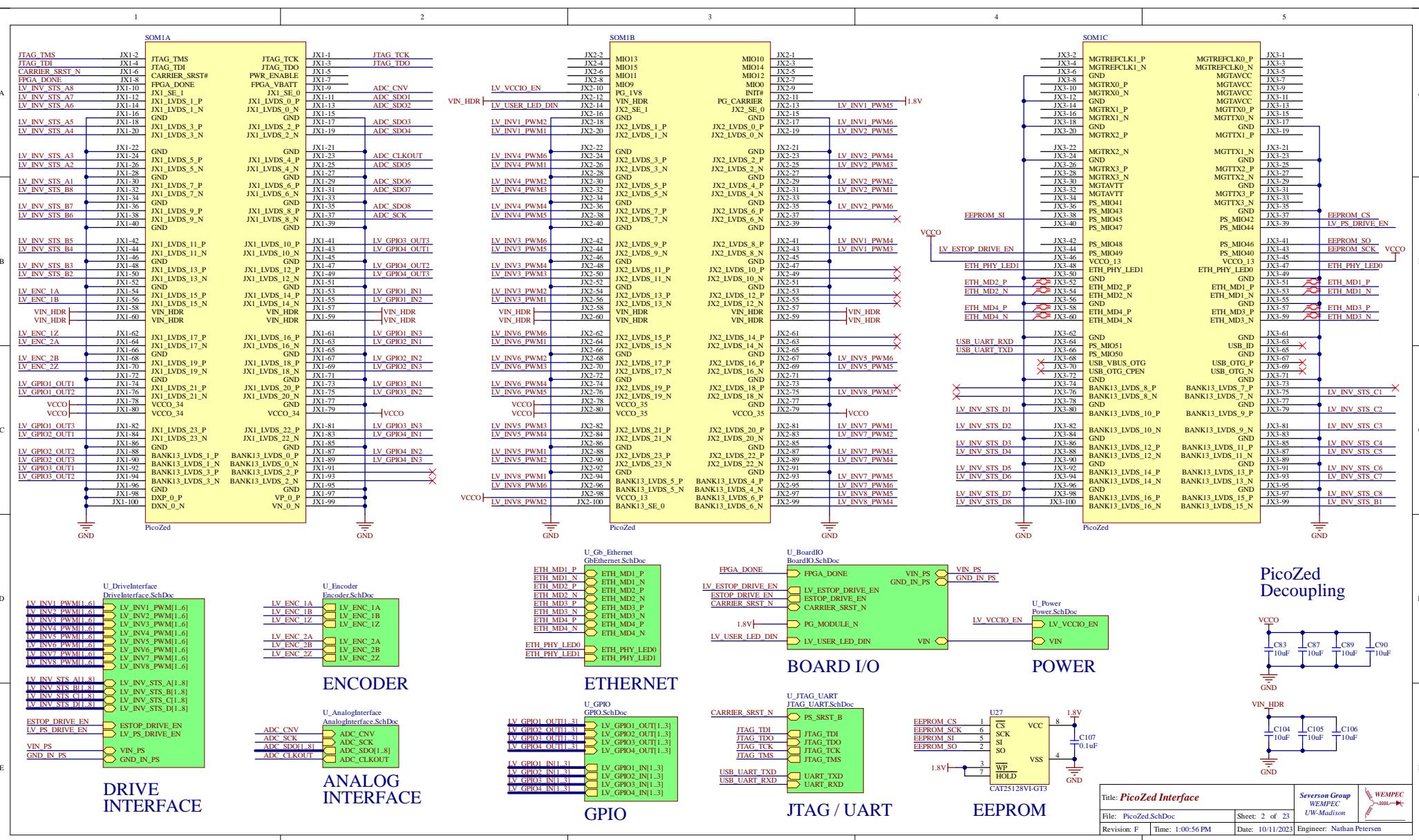
Power inputs to board

VINPS

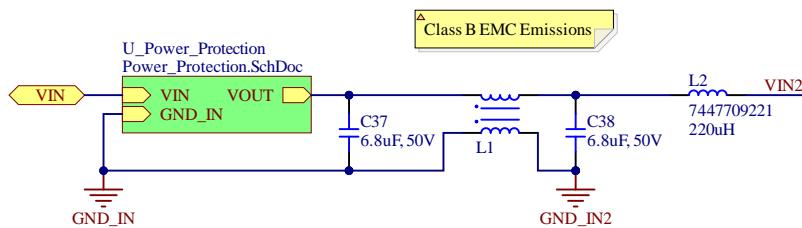
VDRIVE

POWER

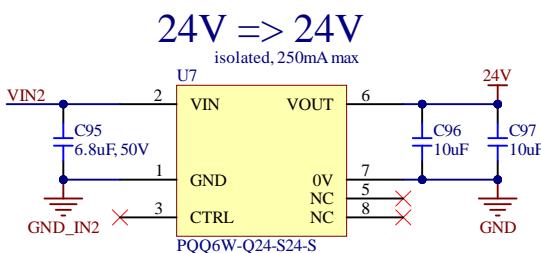
U_BackPage
BackPage.SchDocU_RevisionChanges
RevisionChanges.SchDocTitle: **Advanced Motor Drive Controller**File: **AMDC.SchDoc** Sheet: **1 of 23**Revision: **F** Time: **1:00:56 PM**Date: **10/11/2023**Severson Group
WEMPEC
UW-MadisonEngineer: **Nathan Petersen**



A



B



C

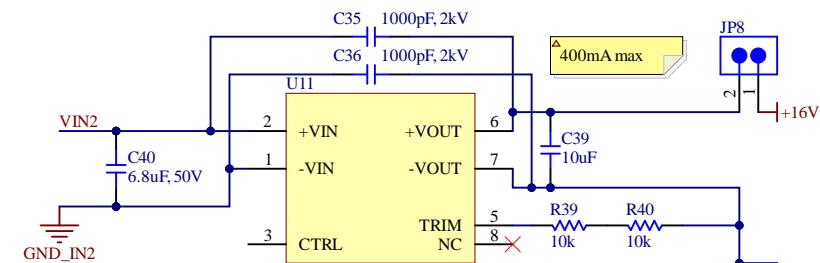
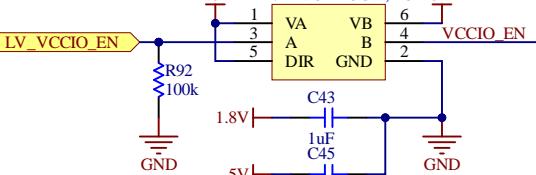
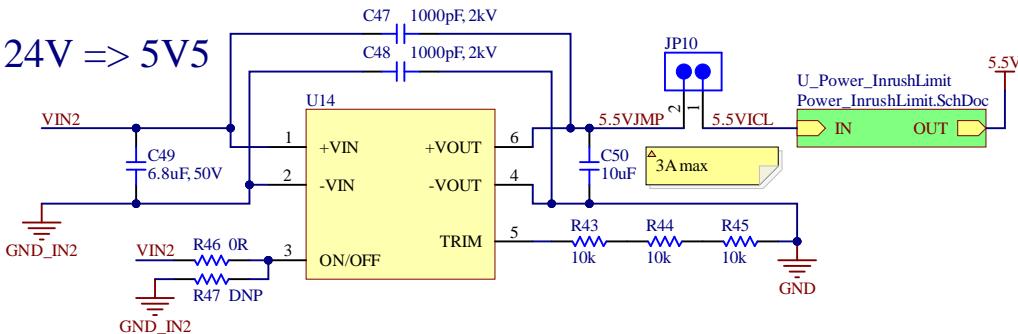
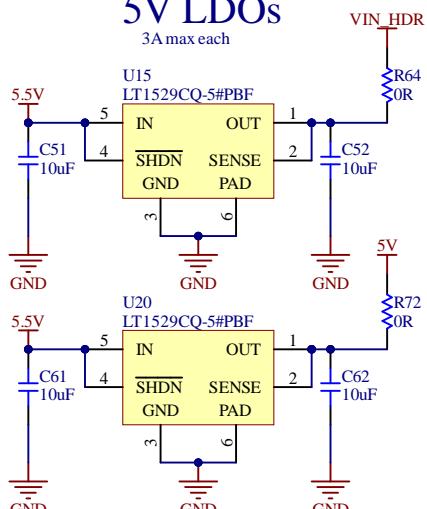
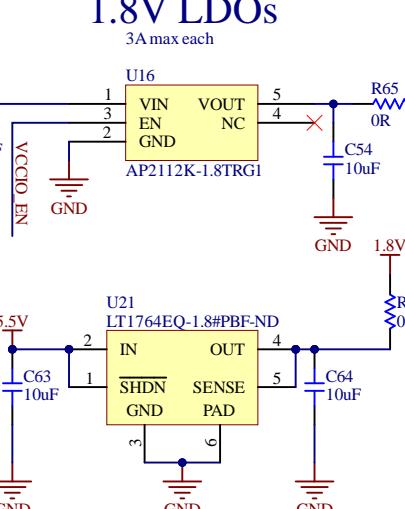
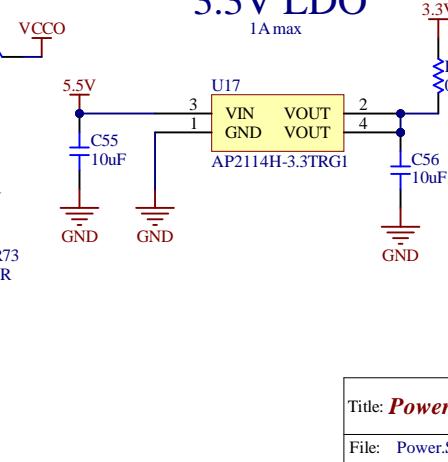
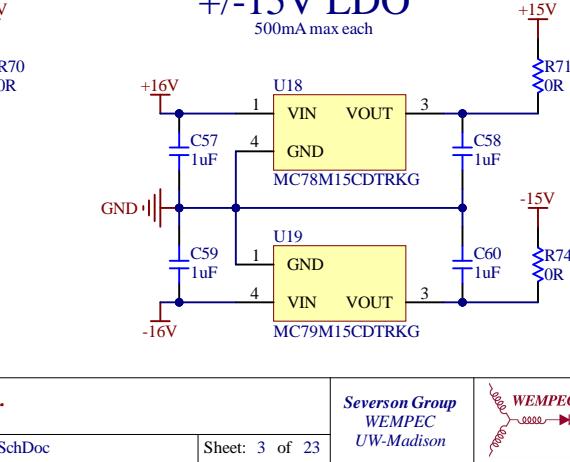
5V <=> General
VIN_HDR <=> PicoZed main power

3.3V <=> General

1.8V <=> General
VCCO <=> PicoZed VCCIO*

2.048VREF <=> ADC ref / SigCond1..8

+/-15V <=> Con1..4 / SigCond1..8

**24V => +16V****24V => -16V****24V => 5V5****5V LDOs****1.8V LDOs****3.3V LDO****+/-15V LDO**Title: **Power**

File: Power.SchDoc Sheet: 3 of 23

Revision: F Time: 1:00:56 PM Date: 10/11/2023

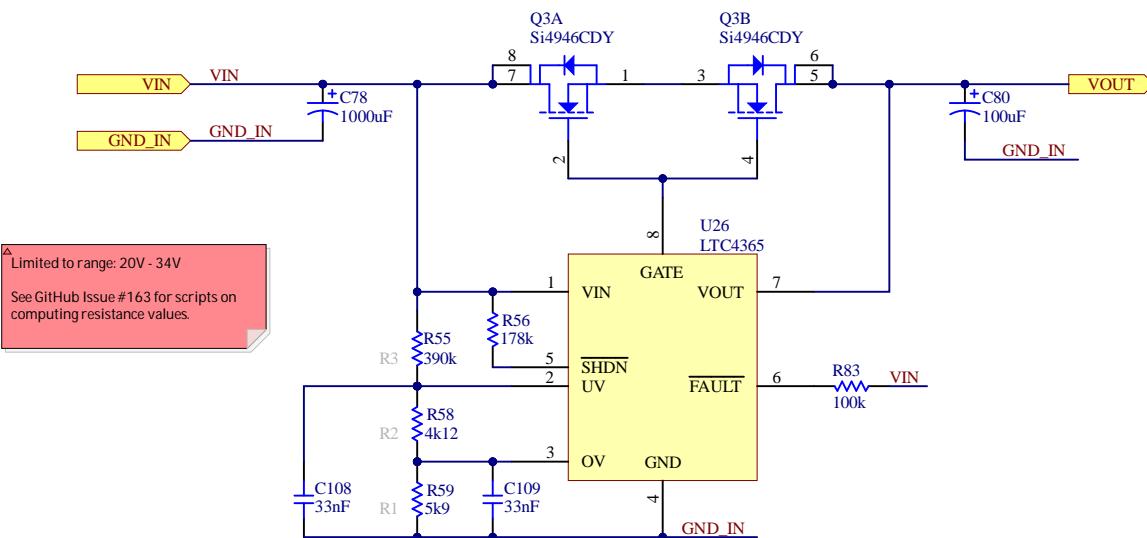
Severson Group
WEMPEC
UW-Madison

Engineer: Nathan Petersen



A

A



B

B

C

C

D

D

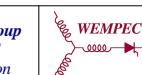
Title: **Power Protection**

File: Power_Protection.SchDoc

Revision: F

Sheet: 4 of 23

Time: 1:00:57 PM

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UW-Madison

Date: 10/11/2023

Engineer: Nathan Petersen

A

A

B

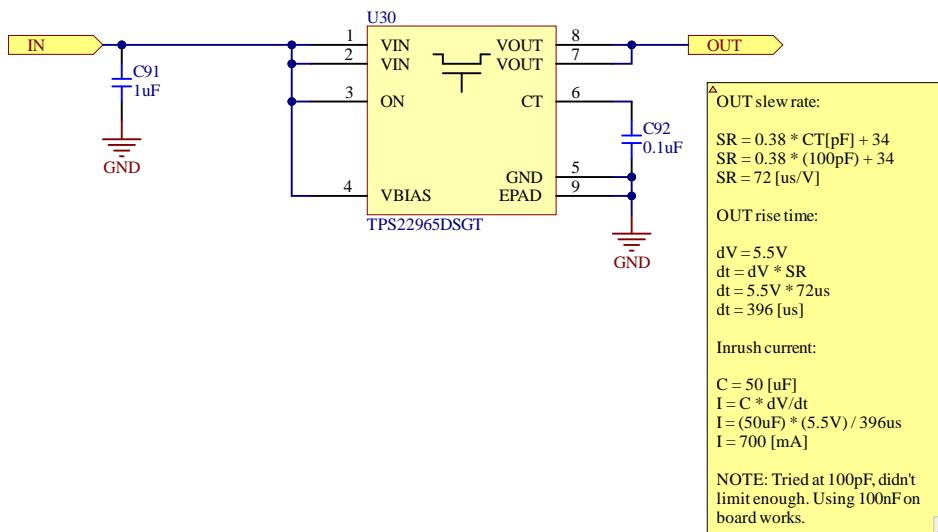
B

C

C

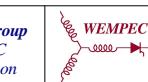
D

D

Title: **Inrush Current Limiter**

File: Power_InrushLimit.SchDoc | Sheet: 5 of 23

Revision: F | Time: 1:00:57 PM | Date: 10/11/2023

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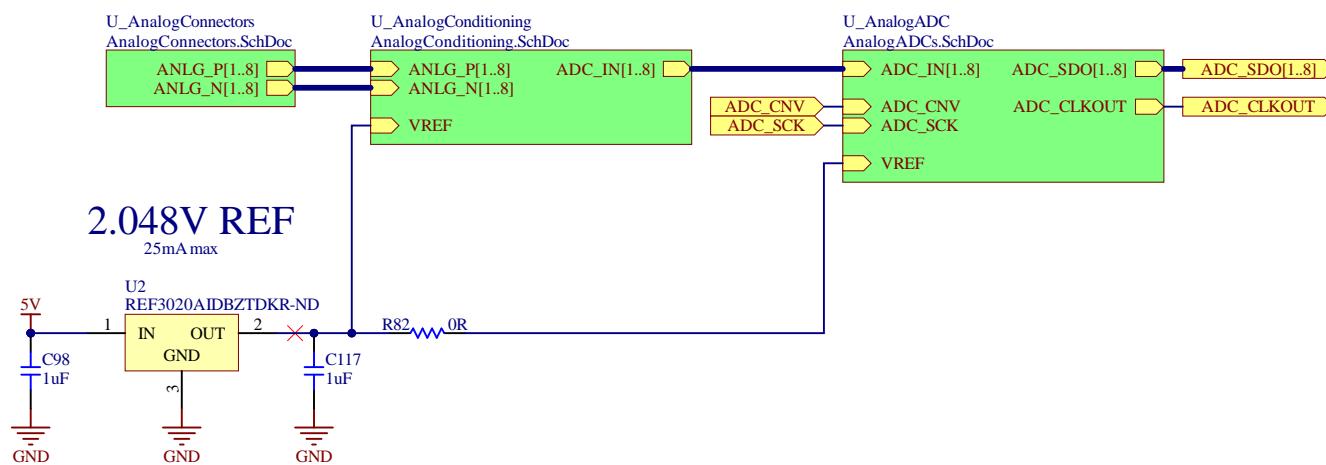
Engineer: Nathan Petersen

A

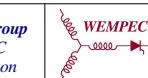
A

B

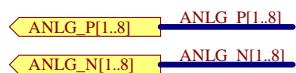
B

Title: *Analog Interface*File: *AnalogInterface.SchDoc*Sheet: *6 of 23*Revision: *F* Time: *1:00:57 PM*Date: *10/11/2023*

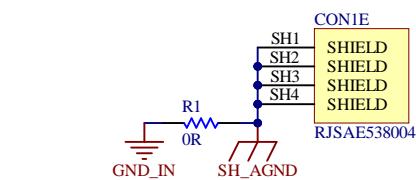
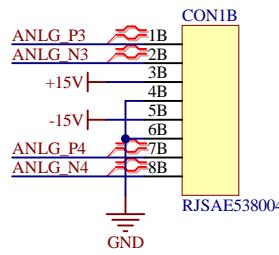
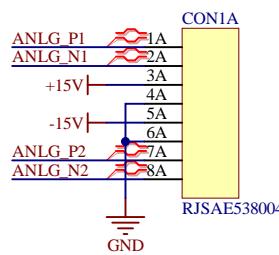
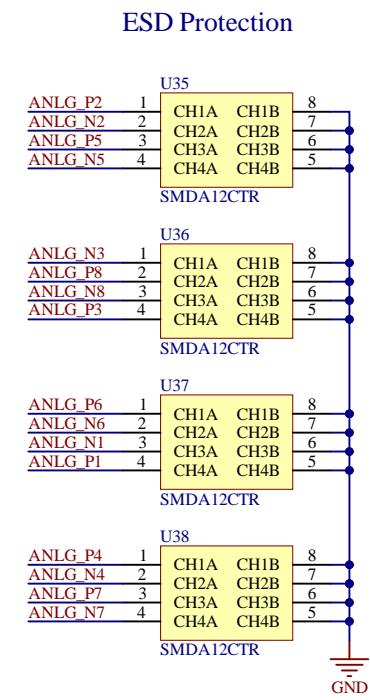
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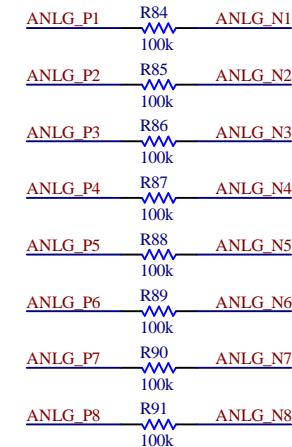
A



B



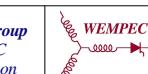
Force no input to 0V



D

Title: **Analog RJ45 Connectors**

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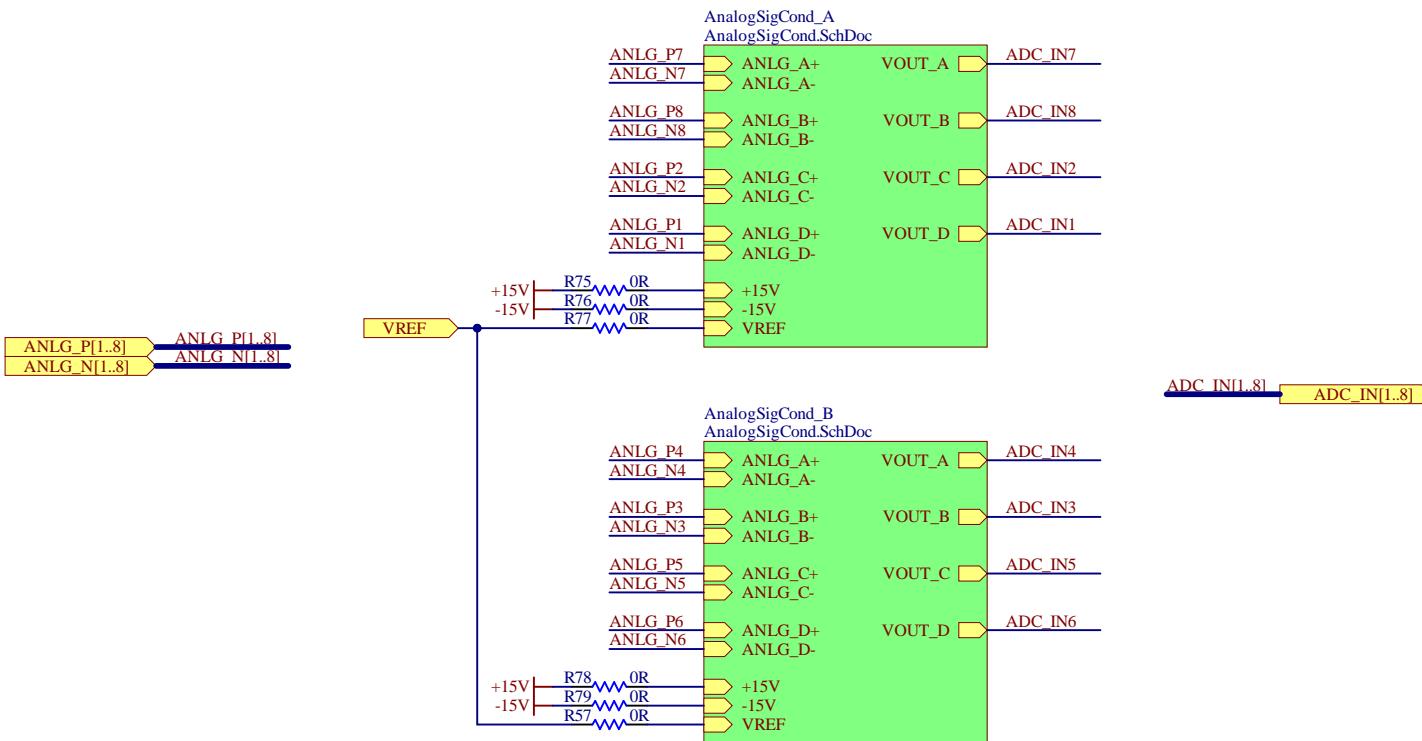
File: AnalogConnectors.SchDoc | Sheet: 7 of 23

Revision: F | Time: 1:00:57 PM | Date: 10/11/2023

Engineer: Nathan Petersen

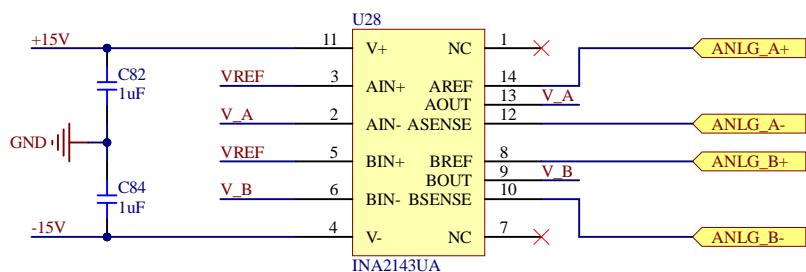
A

A

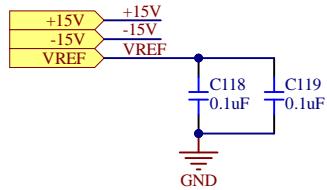
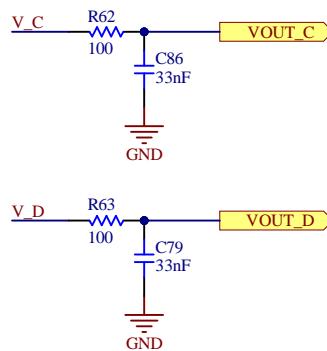
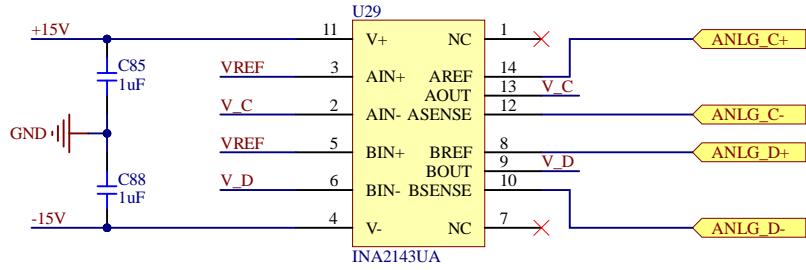
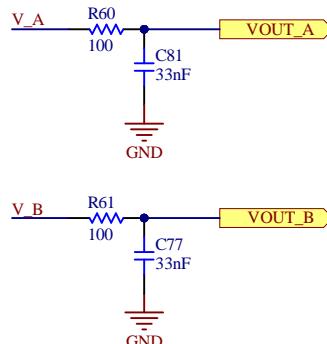


A

A



△ LPF: $f_c = 50\text{kHz}$



Title: **Analog Signal Front-End**

File: **AnalogSigCond.SchDoc**

Sheet: **9 of 23**

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Revision: **F** Time: **1:00:58 PM**

Date: **10/11/2023**

Engineer: **Nathan Petersen**

B

B

C

C

D

D

A



VREF
ADC_IN[1..8]

VREF
ADC_IN8 47
ADC_IN7 51
ADC_IN6 50
ADC_IN5 2
ADC_IN4 5
ADC_IN3 11
ADC_IN2 10
ADC_IN1 14
ADC_IN1 13
ADC_IN2 17
ADC_IN3 16
ADC_IN1 20
ADC_IN1 19

ADC_5V
ADC_1V8
44 52 21 15
VDD VDD VDD VDD
37 31

U1 LTC2320-14
CNV SCK CLKOUT
24 ADC_CNV
41 ADC_SCK
33 ADC_CLKOUT
27 ADC_SDO1
28 ADC_SDO2
29 ADC_SDO3
30 ADC_SDO4
35 ADC_SDO5
36 ADC_SDO6
39 ADC_SDO7
40 ADC_SDO8
25 23
34
42 DNC

ADC_SDO[1..8] ADC_SDO[1..8]

ADC Serial Interface Test Points

ADC_CNV TP1
ADC_SCK TP2
ADC_CLKOUT TP3
TP4
GND

B

VREF
C6 0.1uF C11 0.1uF C16 0.1uF C20 0.1uF
C7 0.1uF C12 0.1uF C17 0.1uF C21 0.1uF
C8 10uF C13 10uF C18 10uF C22 10uF
C9 0.1uF C14 0.1uF C19 0.1uF C23 0.1uF
C10 0.1uF C15 0.1uF
GND GND GND GND GND

REFBUFEN REF
REFOUT1 REFOUT2 REFOUT3 REFOUT4
3 7 12 18 26 32 38 46 49 53
GND GND GND GND GND GND GND GND GND
43 8 22 9 6 45
ADC_5V
C1 10uF C2 10uF C3 10uF C4 10uF C5 1uF
GND GND GND GND GND

C

D

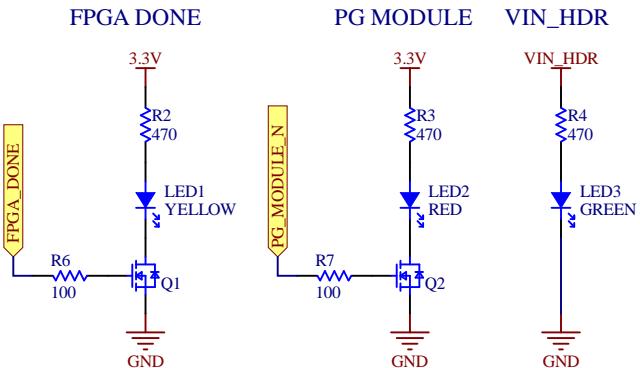
A

B

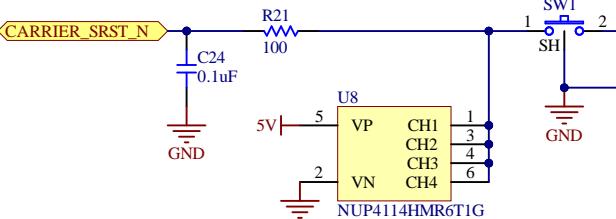
C

D

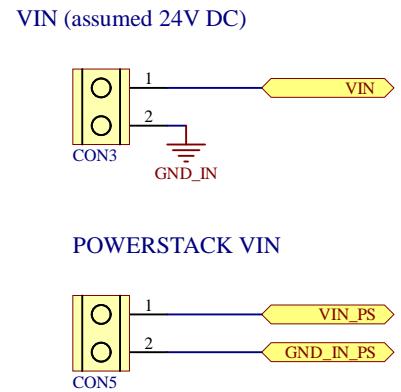
STATUS LEDS



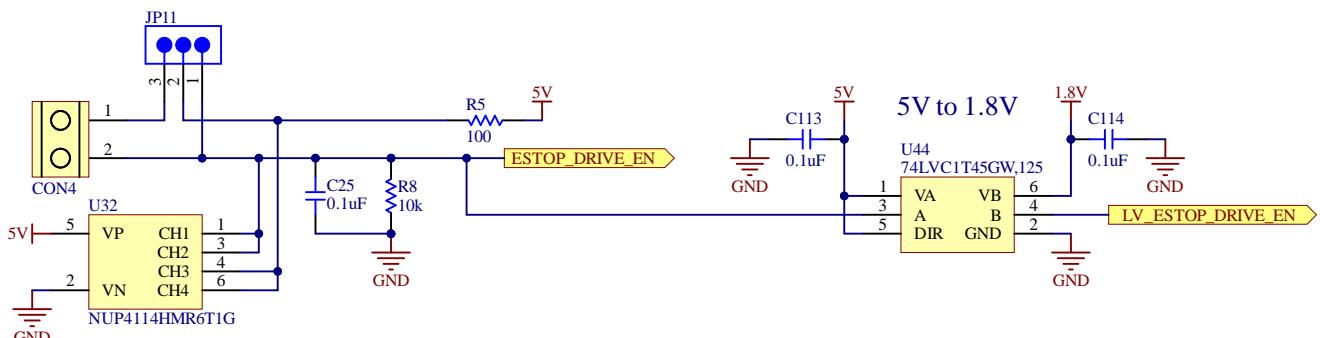
RESET BUTTON



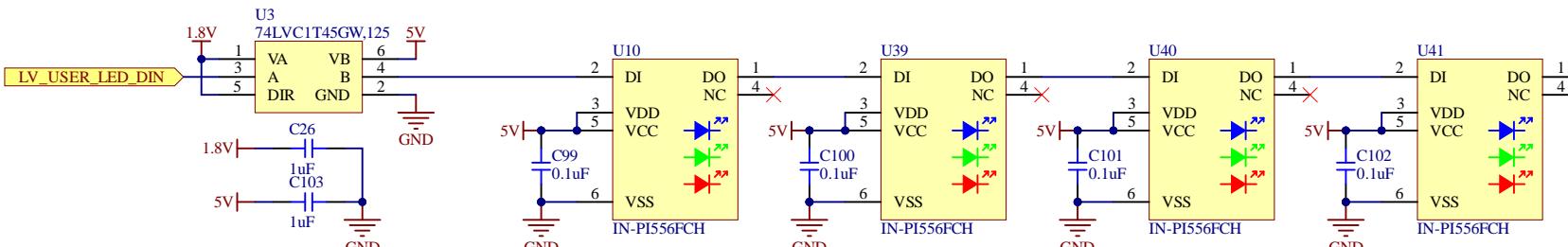
POWER CONNECTORS



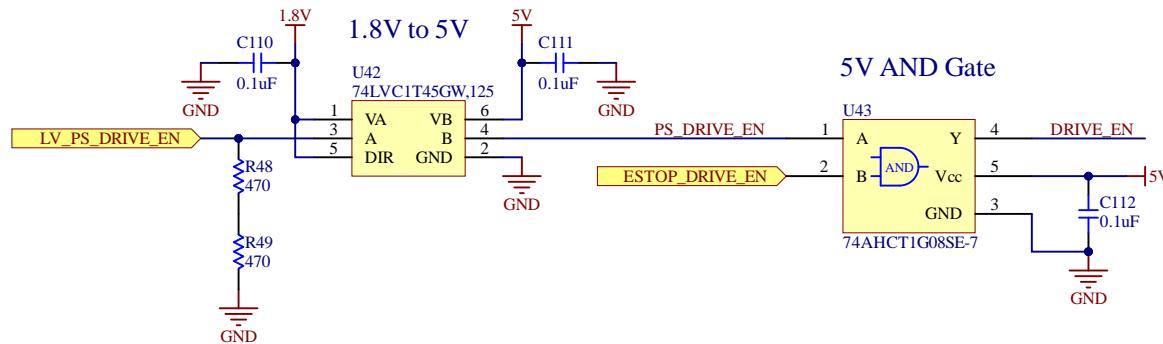
DRIVE ENABLE (ESTOP)



USER RGB LEDs

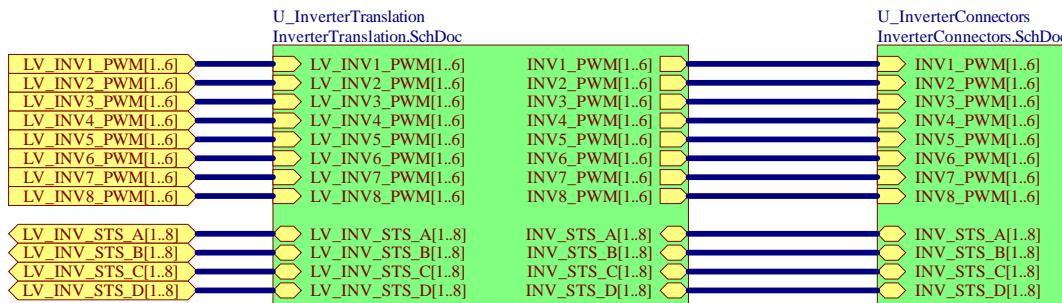


A



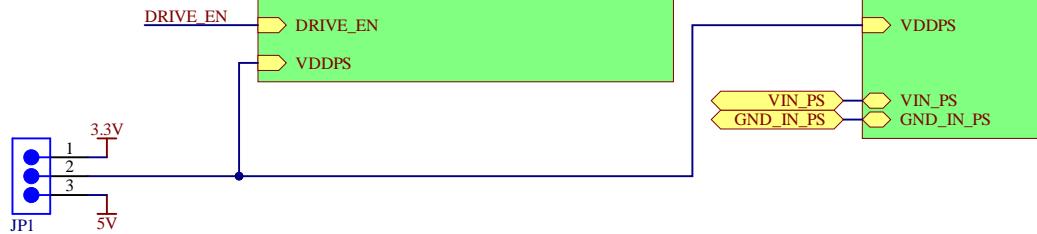
A

B



B

C



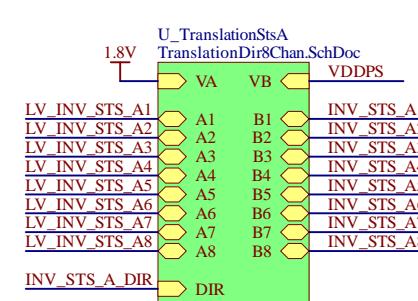
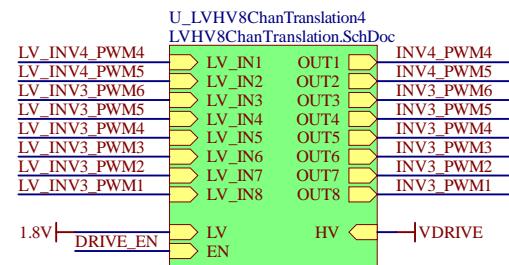
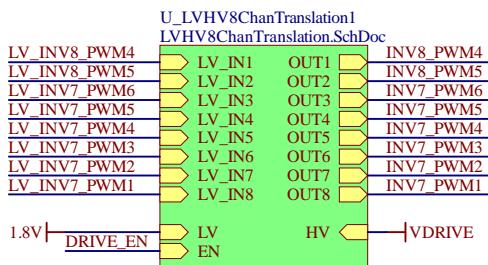
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D

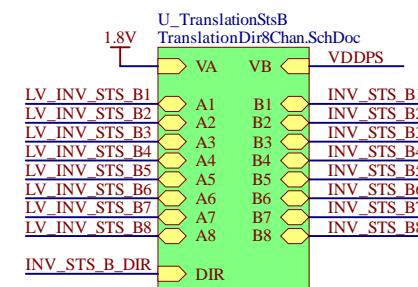
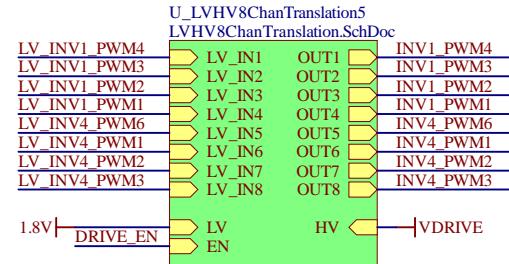
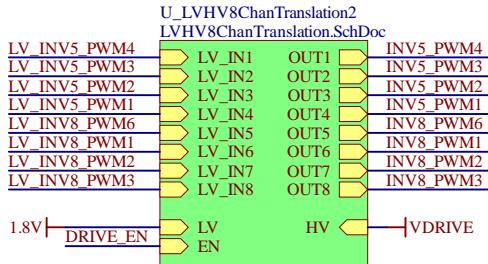
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File: DriveInterface.SchDoc				
Revision: F	Time: 1:00:58 PM	Date: 10/11/2023		

D

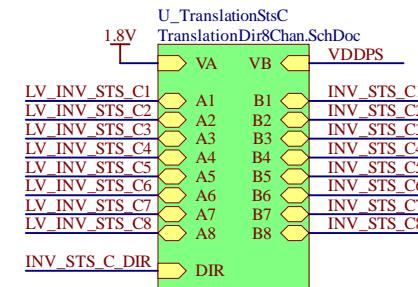
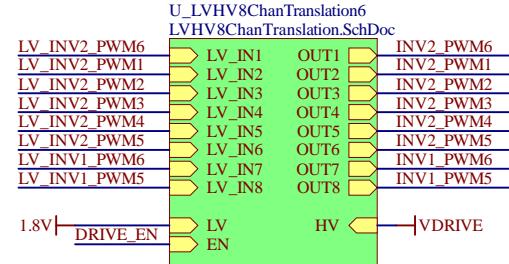
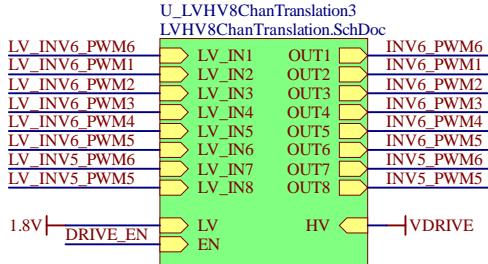
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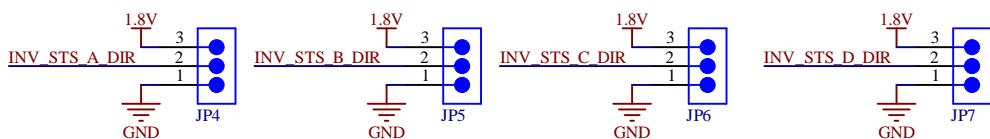
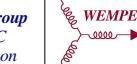
B



C



D

Title: **Inverter Level Translation**Severson Group
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UW-Madison

File: InverterTranslation.SchDoc | Sheet: 13 of 23

Revision: F | Time: 1:00:59 PM

Date: 10/11/2023 | Engineer: Nathan Petersen

A

A

B

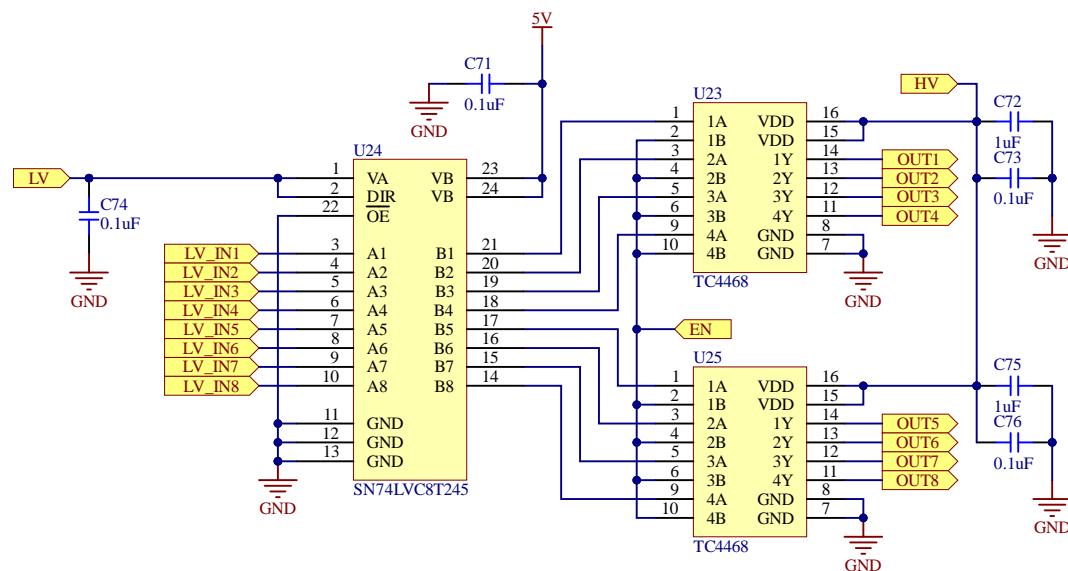
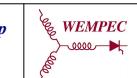
B

C

C

D

D

Title: **8-channel LV to HV Translation**File: **LVHV8ChanTranslation.SchDoc** | Sheet: **14 of 23**Revision: **F** | Time: **1:00:59 PM**Date: **10/11/2023****Severson Group**
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UW-MadisonEngineer: **Nathan Petersen**

A

A

B

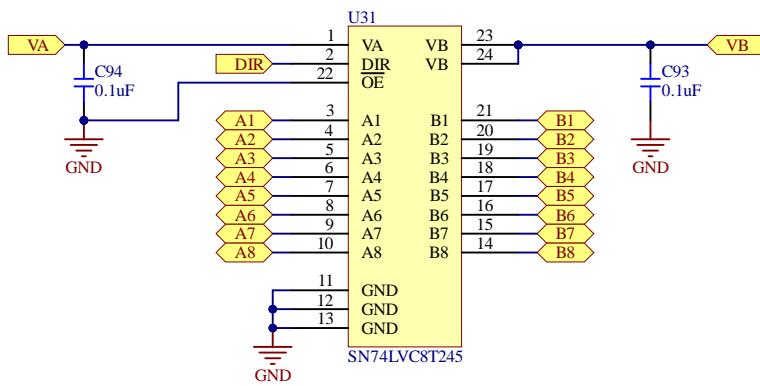
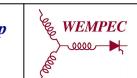
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C

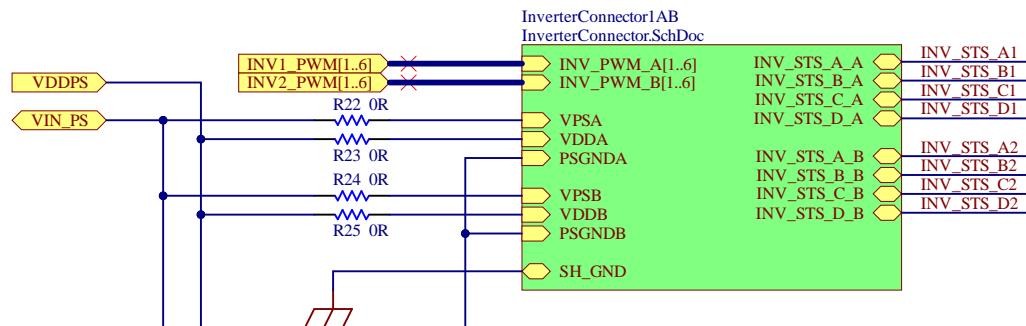
C

D

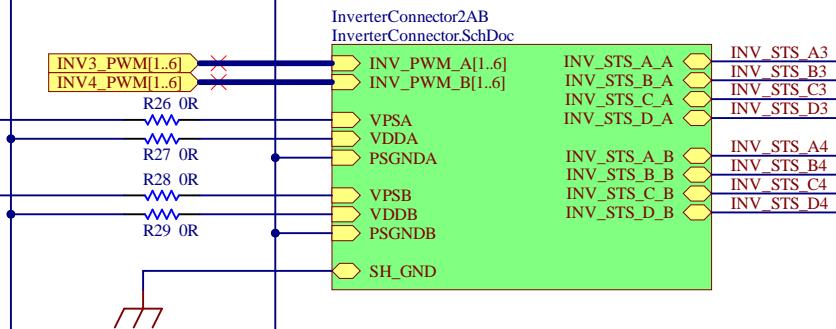
D

Title: **8-Channel Directional Translation**File: **TranslationDir8Chan.SchDoc** | Sheet: **15 of 23**Revision: **F** | Time: **1:00:59 PM**Date: **10/11/2023****Severson Group**
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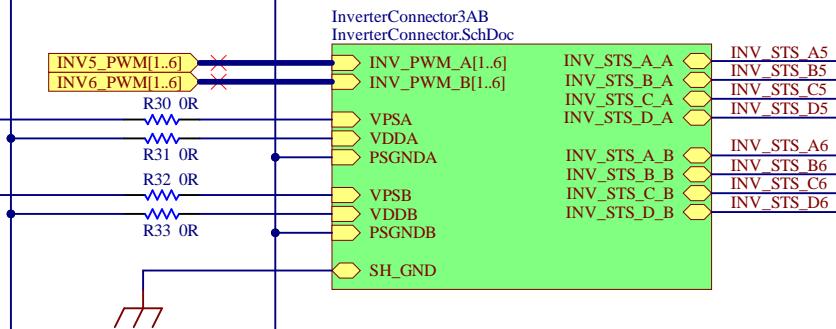
A



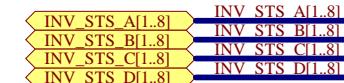
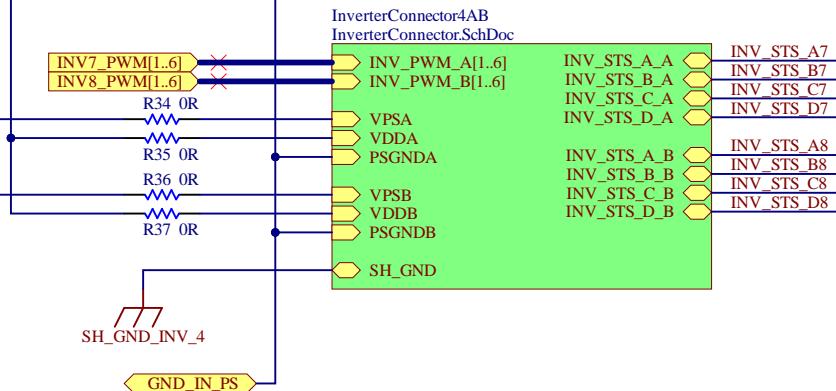
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C



D



Title: **Inverter Connectors**

File: InverterConnectors.SchDoc | Sheet: 16 of 23

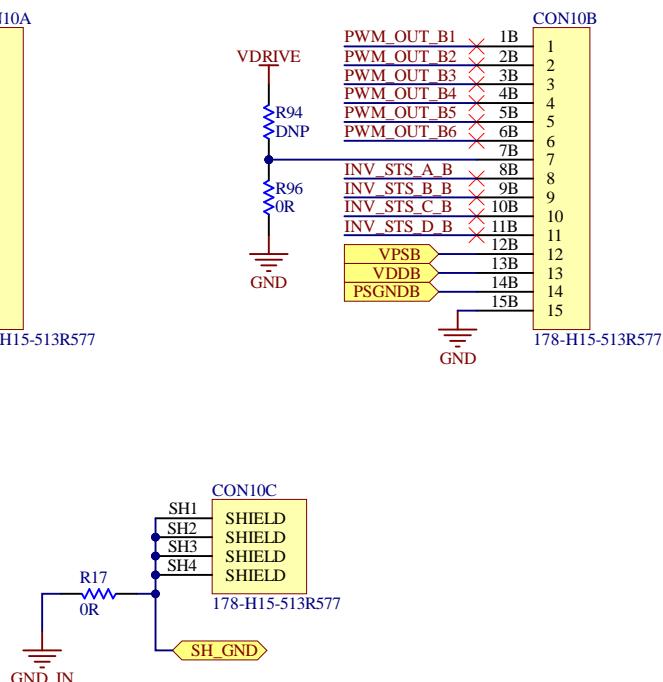
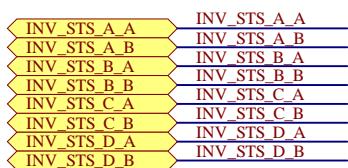
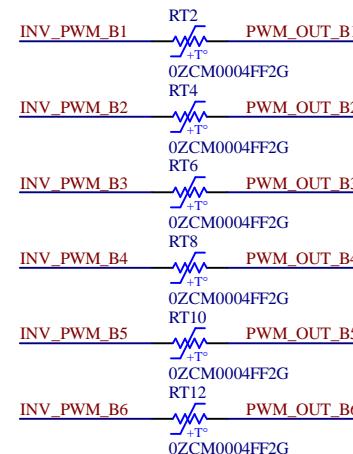
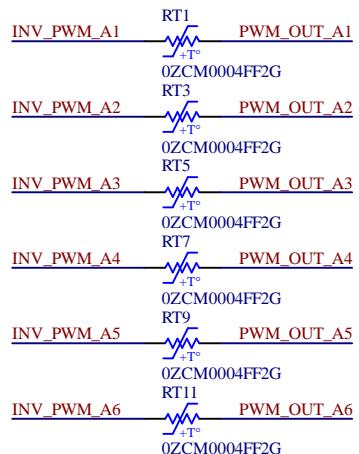
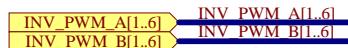
Revision: F | Time: 1:00:59 PM | Date: 10/11/2023

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Short Circuit Protection

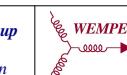


Title: **Inverter Connector**

File: InverterConnector.SchDoc | Sheet: 17 of 23

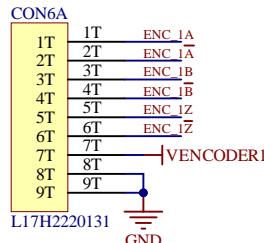
Revision: F | Time: 1:00:59 PM | Date: 10/11/2023

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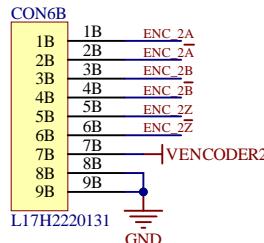


Engineer: Nathan Petersen

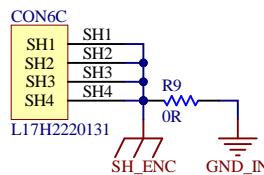
A



ENC_1A R11 ENC_1A
100
ENC_1B R12 ENC_1B
100
ENC_1Z R13 ENC_1Z
100

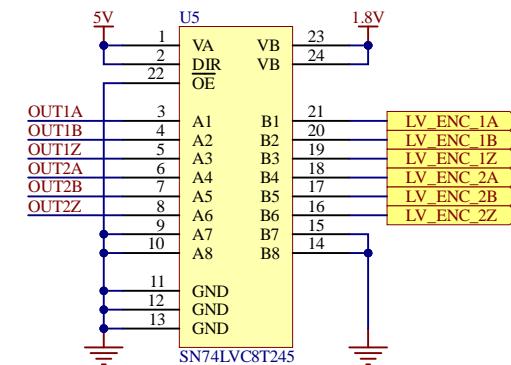
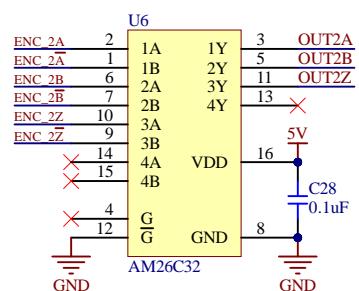
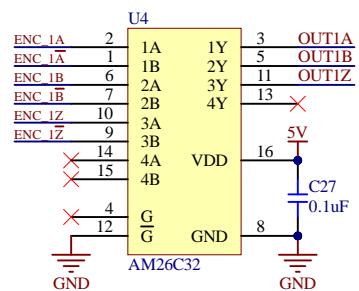


ENC_2A R14 ENC_2A
100
ENC_2B R15 ENC_2B
100
ENC_2Z R16 ENC_2Z
100



JP2 1 5V VENCODER1
2

JP3 1 5V VENCODER2
2

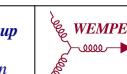


C29 5V 0.1uF C30 1.8V 0.1uF GND

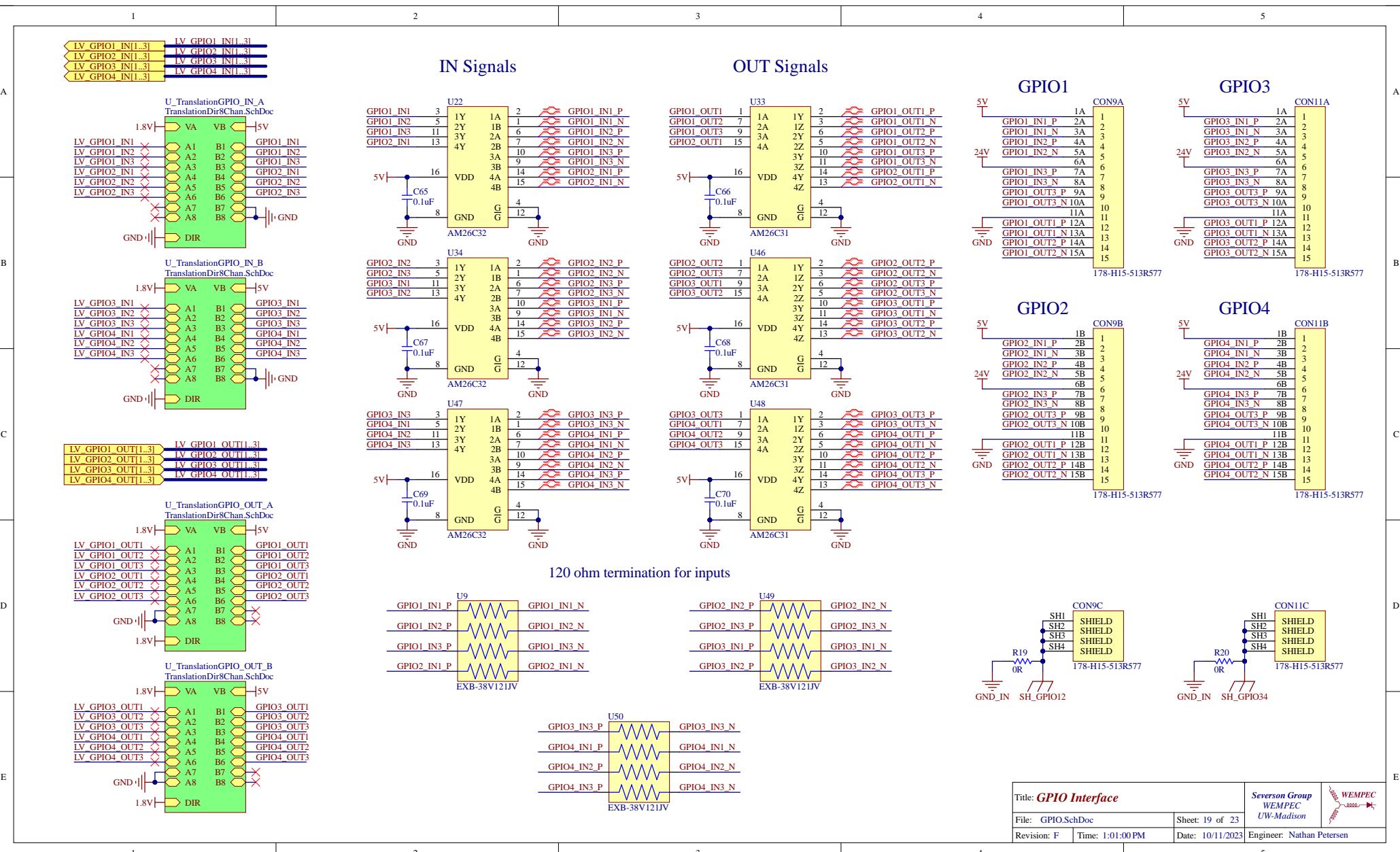
Title: **Encoders**

File: Encoder.SchDoc Sheet: 18 of 23

Revision: F Time: 1:01:00 PM Date: 10/11/2023

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A

A

B

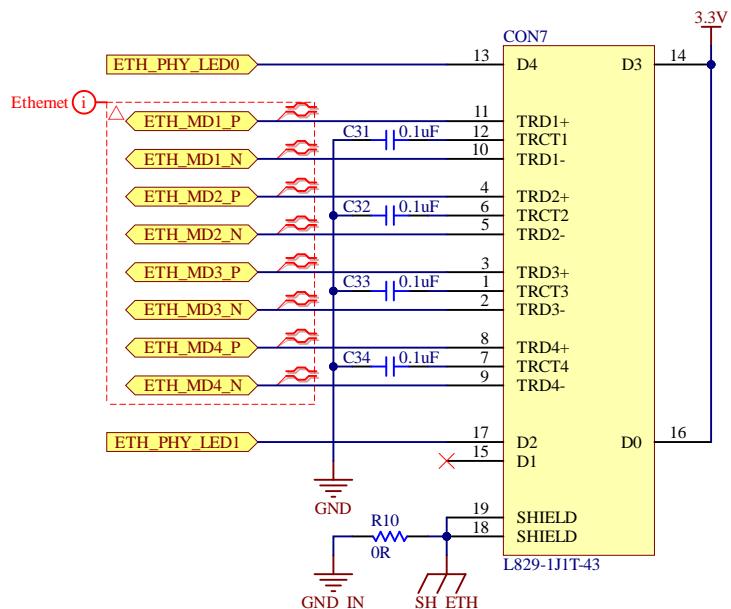
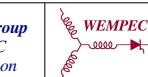
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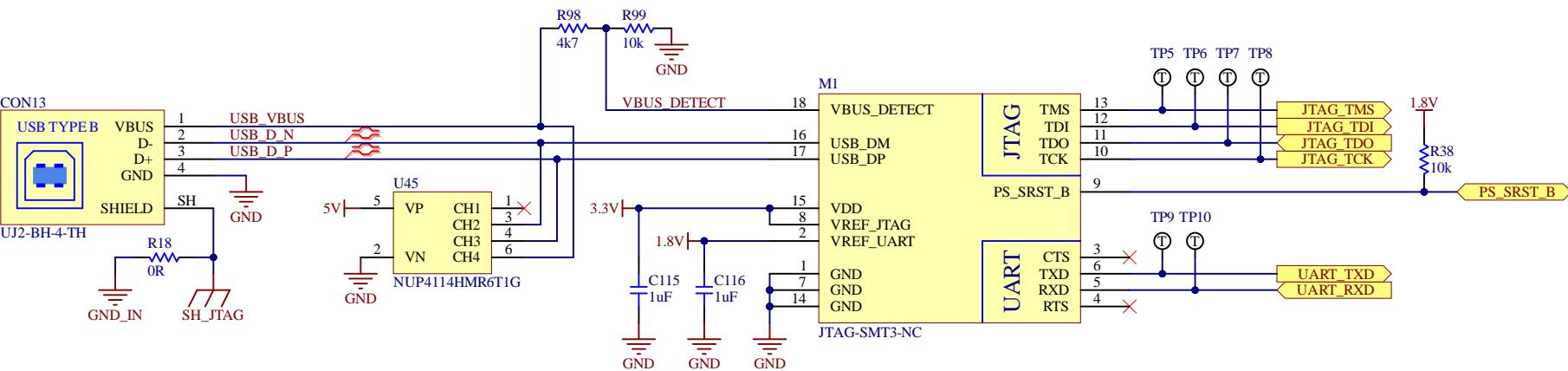
C

C

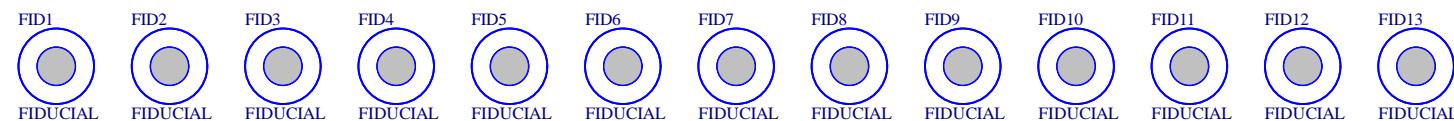
D

D

Title: **SoM Gb Ethernet**File: **GbEthernet.SchDoc** | Sheet: **20 of 23**Revision: **F** | Time: **1:01:00 PM** | Date: **10/11/2023**
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A

Fiducials:

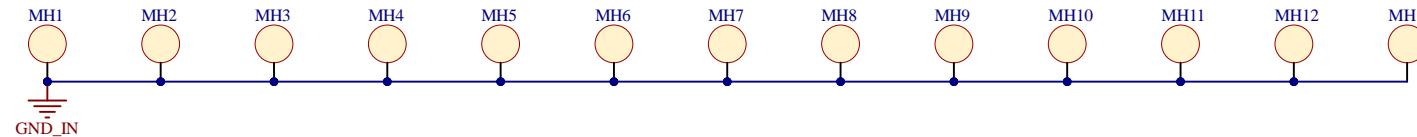
A

4-40 Screws:

B

4-40 Standoffs:

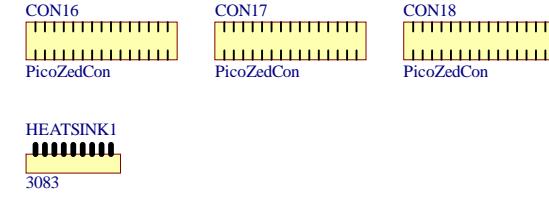
B

Mouting Holes:

C

PicoZed Module:

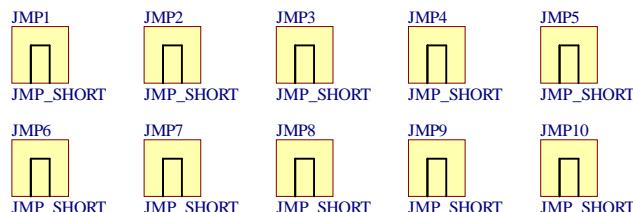
C

PicoZed hardware:

D

Jumpers:

Silkscreen marked with default locations

Title: ***Back Page***File: **BackPage.SchDoc** Sheet: **22 of 23**Revision: **F** Time: **1:01:01 PM** Date: **10/11/2023**
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A

REV A: design finalized 2018-05-25

- Initial design

REV B: design finalized 2018-07-17

- Add power input protection
- Add test points
- Add TVS to analog inputs
- Change power input DC/DC modules
- Fix BOM with correct part numbers
- Fix footprints

REV C: design finalized 2018-11-21

- Add inrush current limiting to 5V5 rail
- Add more silkscreen labels
- Add test points
- Change ADC reference from 2.5V to 2.048V
- Change trim resistors for +/-16V DC/DCs
- Swap UART Tx / Rx pins
- Separate power stack shields between connectors
- Fix footprints

REV D: design finalized 2020-01-29

- New PCB form factor (6" x 6.75", 6 layers)
- Add power stack supply rail distribution
- Add isoSPI ports
- Add extra encoder port
- Add 10R resistors to subsection power for debugging
- Add 100k resistors across analog inputs
- Add serially addressable RGB LEDs
- Add EEPROM
- Add fiducials to layout
- Remove user button / switch
- Remove discrete RGB LED
- Remove ADC2, now just one ADC
- Remove unity gain op-amp driving ADC inputs
- Reduce bulk input
- Reduce 24V power filter component current ratings
- Reduce 3V3 LDO current rating
- Change level-shifter IC for UART signals
- Change JTAG to NC module
- Change JTAG pin headers to pads
- Change values for inrush limiting circuitry
- Change FPGA driven MOSFETs to lower V_{th}
- Change FPGA pin-out mapping
- Change power stack connector I/O
- Change encoder input signal chain
- Change Ethernet routing to correct diff. impedance
- Fix footprints

REV E: design finalized 2021-03-25

- Remove isoSPI
- Add shared UART and JTAG interface
- Add more GPIO ports
- Add mechanical parts to BOM
- Add website to PCB silkscreen
- Add reset signal pull-up and ESD protection
- Add local decoupling to VREF
- Add local decoupling to 2.048V
- Add E-STOP logic signal to FPGA
- Add PTC resettable fuses to PWM outputs
- Add VDRIVE signal to PS interface
- Add jumpers for default VDRIVE and ESTOP
- Add pull-down to VCCIO_EN
- Change power wiring in schematics
- Change shield termination to VIN-
- Change mounting holes to VIN- from GND
- Change DB15 P/N to include screw posts
- Change to USB type B receptacle
- Update top-level block diagram
- Fix 24V supply to GPIO port
- Fix power protection circuitry
- Fix board start-up PWM issues
- Fix P/N for RC filter caps
- Fix BOM components for DFM
- Fix footprints

REV F: design finalized 2023-10-05

- Add termination on GPIO differential inputs
- Update pull-down resistor value for boot-up PWM output protection
- Update P/Ns and footprints for manufacturability

See www.github.com/Severson-Group/AMDC-Hardware/issues for more discussion on design changes

Title: Revision Changes		Severson Group WEMPEC UW-Madison
File: RevisionChanges.SchDoc	Sheet: 23 of 23	
Revision: F	Time: 1:01:02 PM	Date: 10/11/2023
Engineer: Nathan Petersen		

