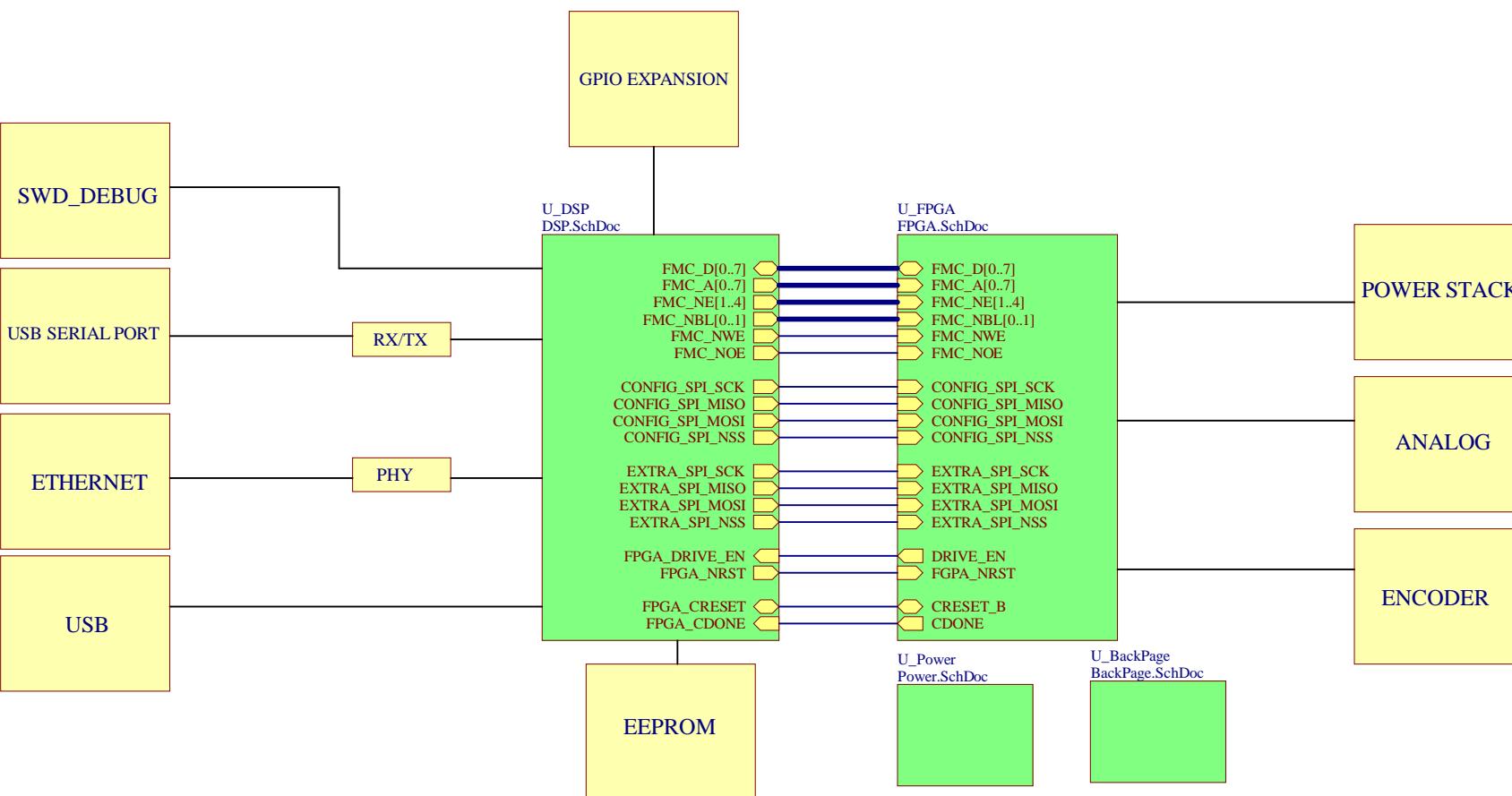


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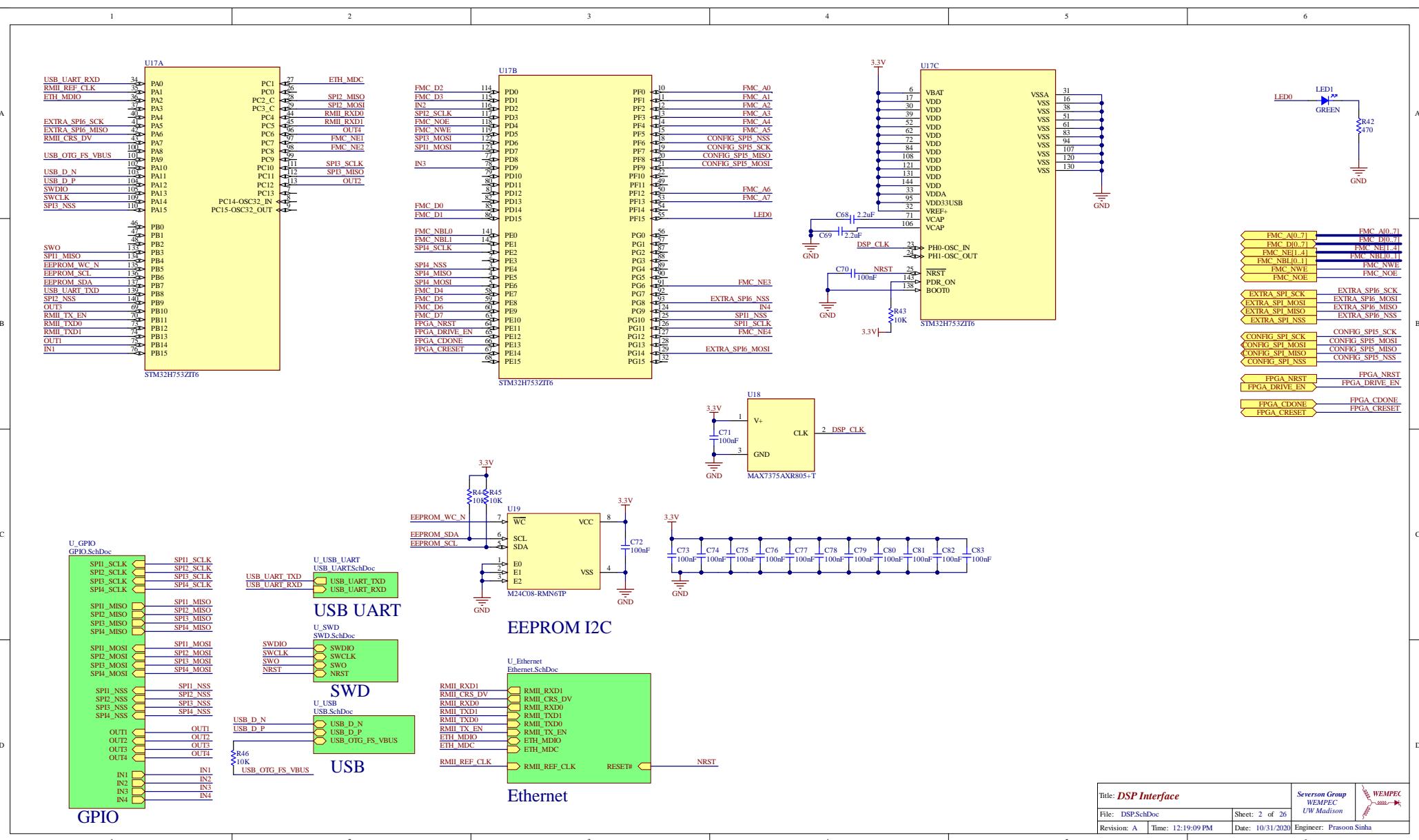
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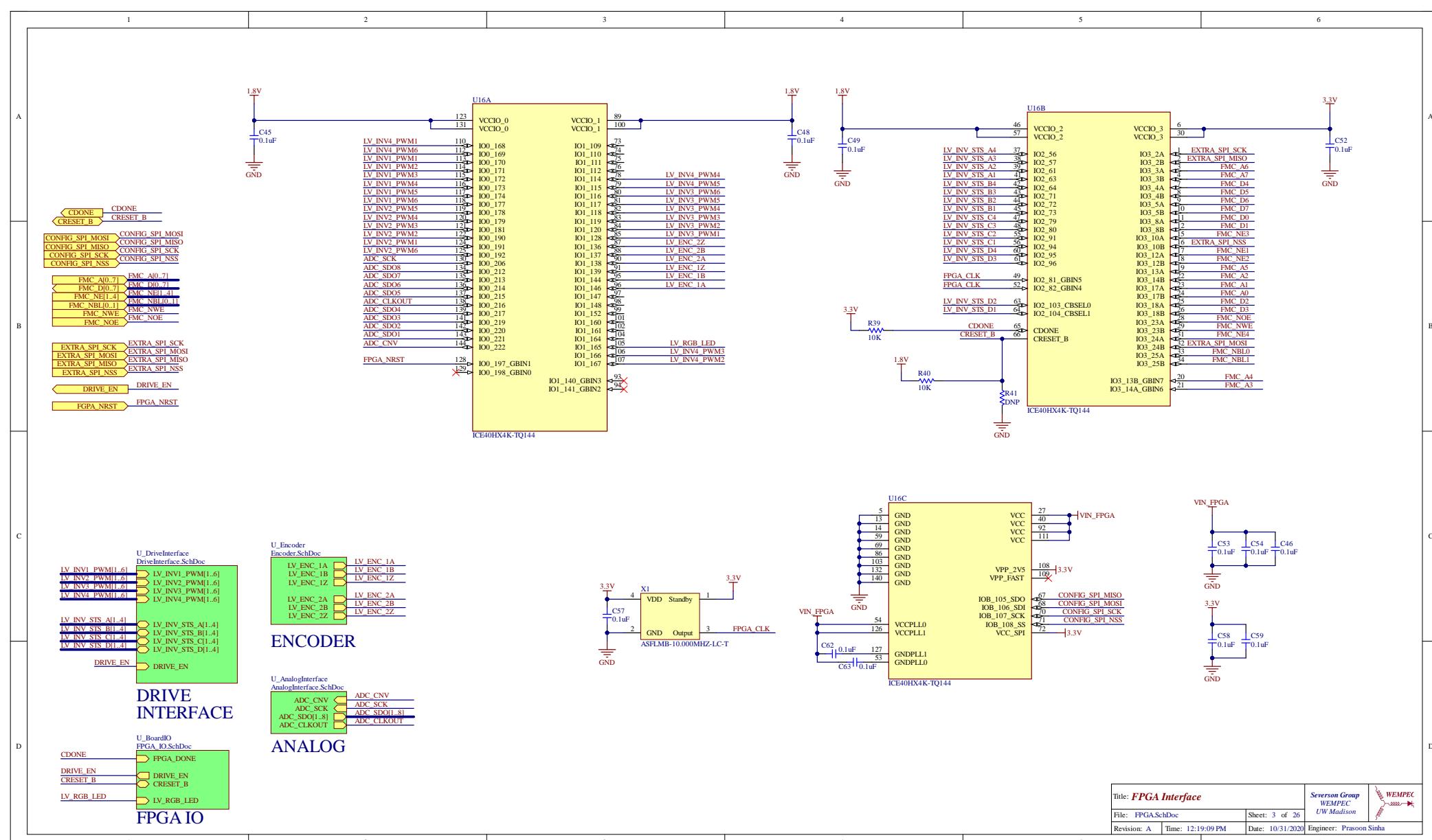
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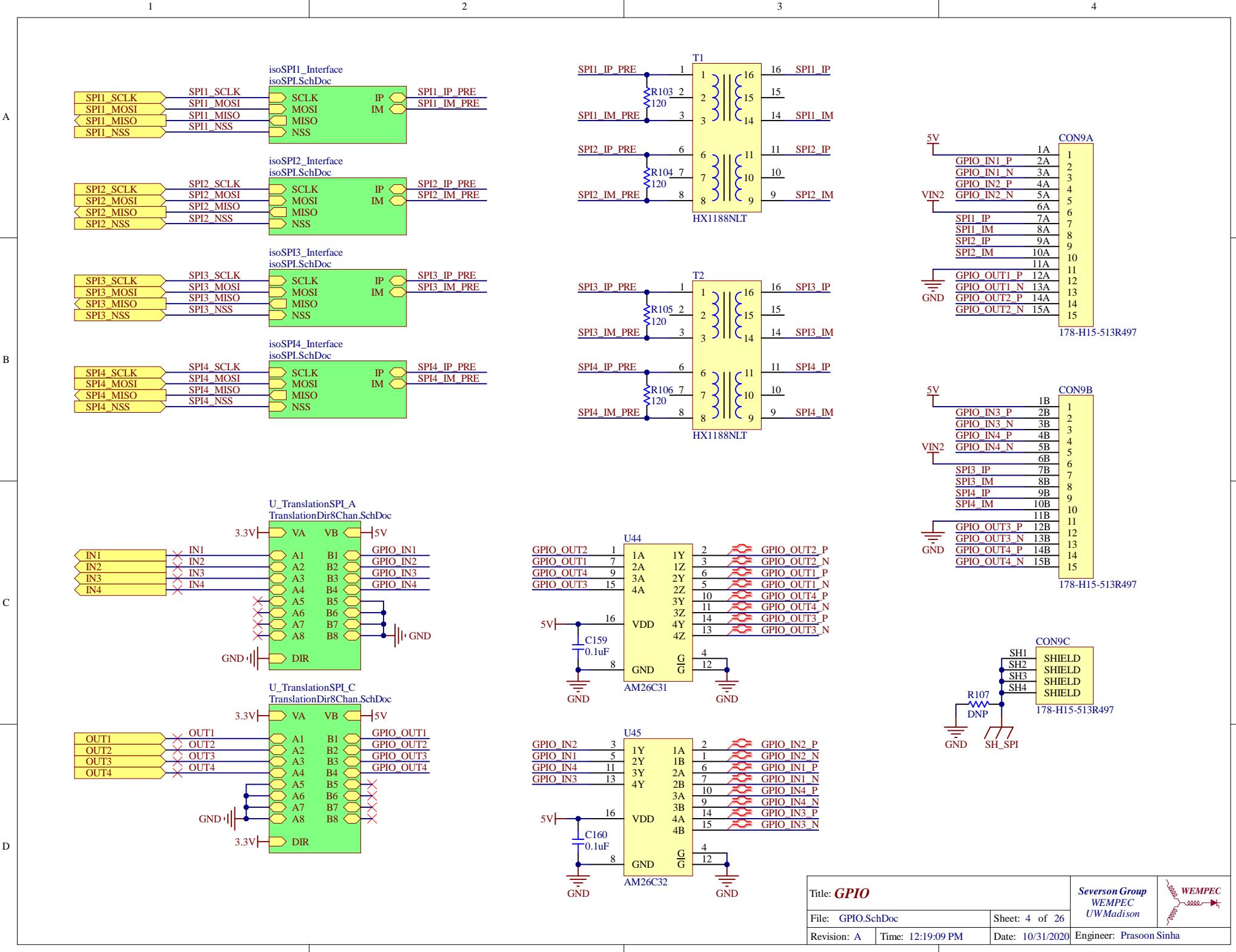
C

D

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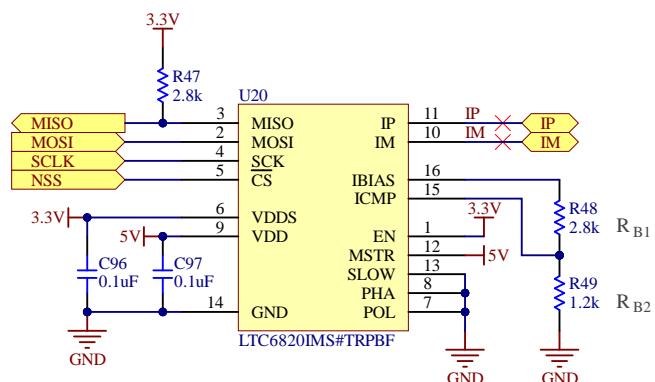
B

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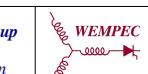
D

Title: *isoSPI Interface*

File: isoSPI.SchDoc | Sheet: 5 of 26

Revision: A | Time: 12:19:09 PM | Date: 10/31/2020

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UWMadison



Engineer: Nathan Petersen

A

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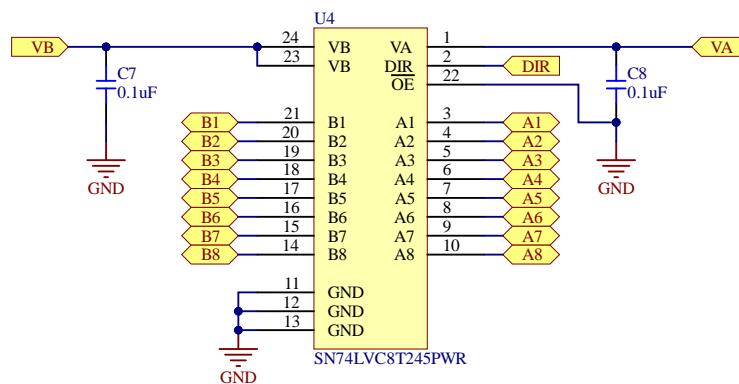
B

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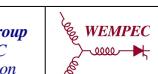
D

Title: **8-Channel Directional Translation**

File: TranslationDir8Chan.SchDoc | Sheet: 6 of 26

Revision: A | Time: 12:19:09 PM | Date: 10/31/2020

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Engineer: Nathan Petersen

A

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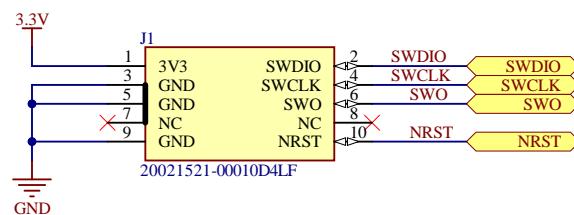
B

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Title: SWD		
File: SWD.SchDoc		Sheet: 7 of 26
Revision: A	Time: 12:19:09 PM	Date: 10/31/2020

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Engineer: Prasoon Sinha

A

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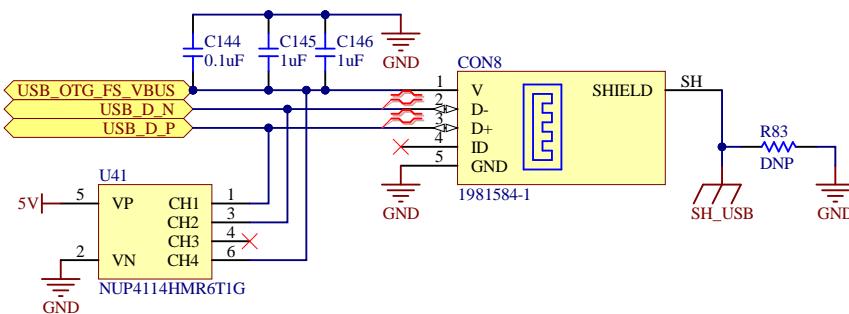
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C

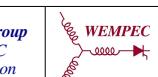
C

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Title: **USB**File: **USB.SchDoc**Sheet: **8 of 26**Revision: **A**Time: **12:19:09 PM**Date: **10/31/2020**

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Engineer: **Prasoon Sinha**

A

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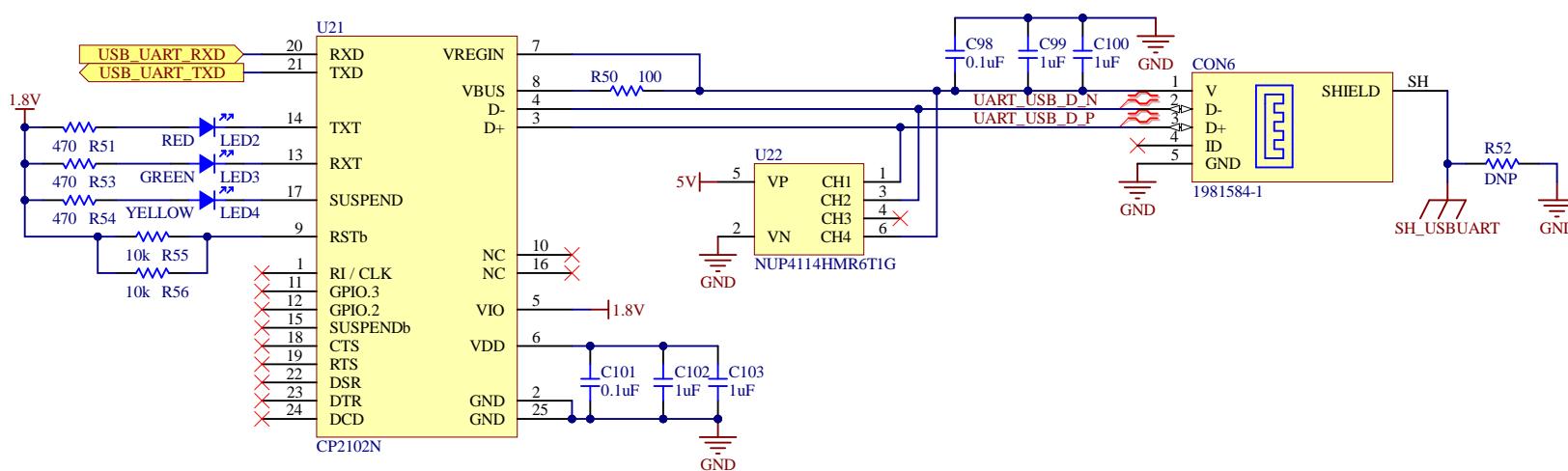
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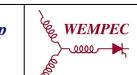
C

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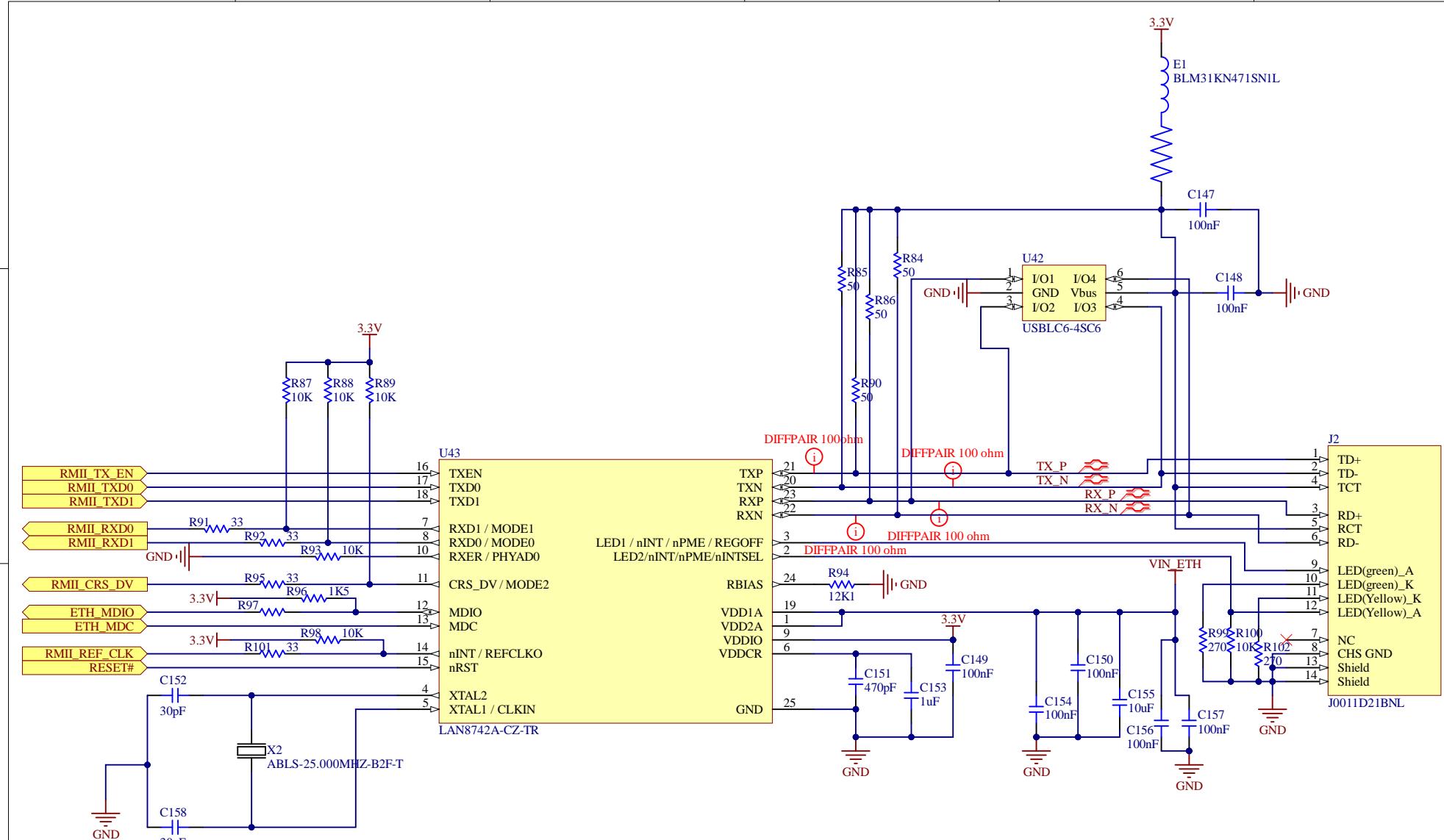
Title: **USB UART**File: **USB_UART.SchDoc**Sheet: **9 of 26**Revision: **A** Time: **12:19:10 PM**Date: **10/31/2020**

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Engineer: **Nathan Petersen**

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Title: *Ethernet*

File: Ethernet.SchDoc

Sheet: 10 of 26

Revision: A Time: 12:19:10 PM

Date: 10/31/2020

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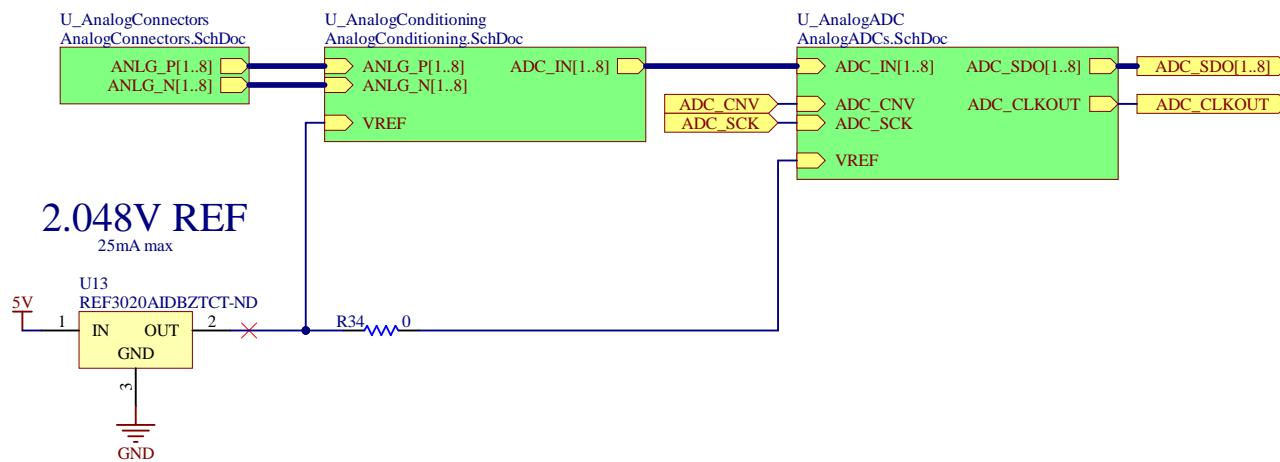
Engineer: Prasoon Sinha

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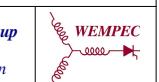
C

D

D

Title: **Analog Interface**File: **AnalogInterface.SchDoc**Sheet: **11 of 26**Revision: **A** Time: **12:19:10 PM**Date: **10/31/2020**

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Engineer: **Nathan Petersen**

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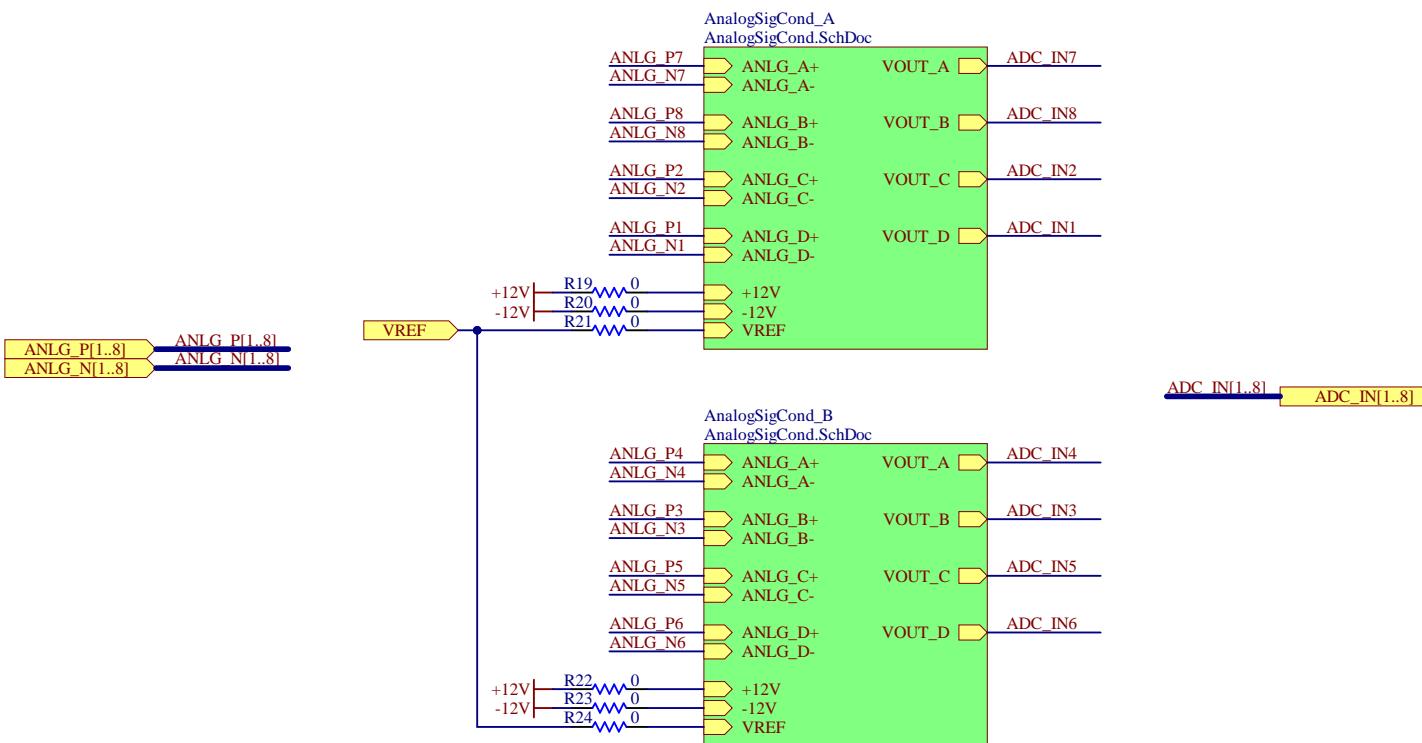
B

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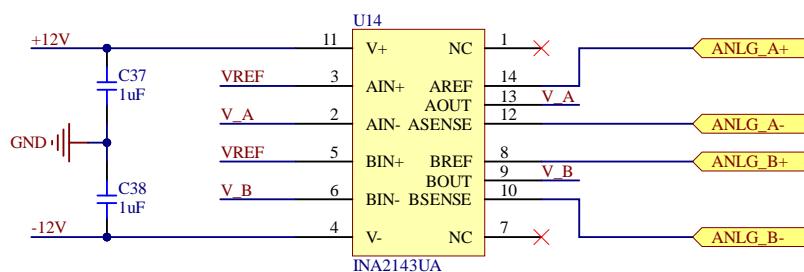
D

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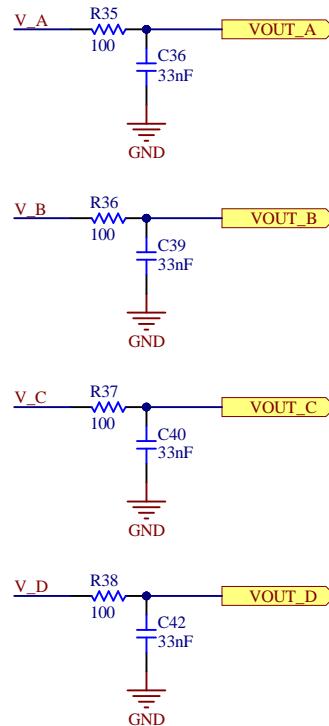


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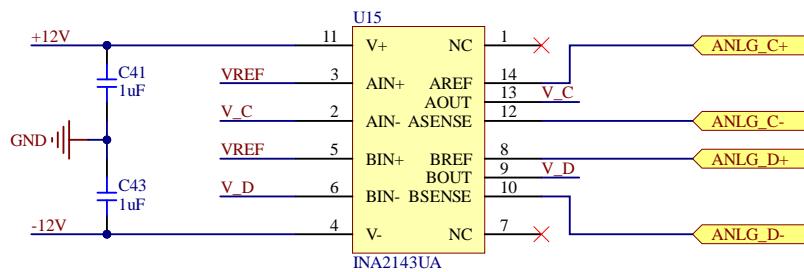


△ LPF: fc = 50kHz



B

B



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C



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Title: **Analog Signal Front-End**

File: **AnalogSigCond.SchDoc**

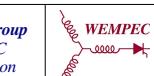
Sheet: **14 of 26**

Revision: **A**

Time: **12:19:10 PM**

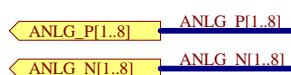
Date: **10/31/2020**

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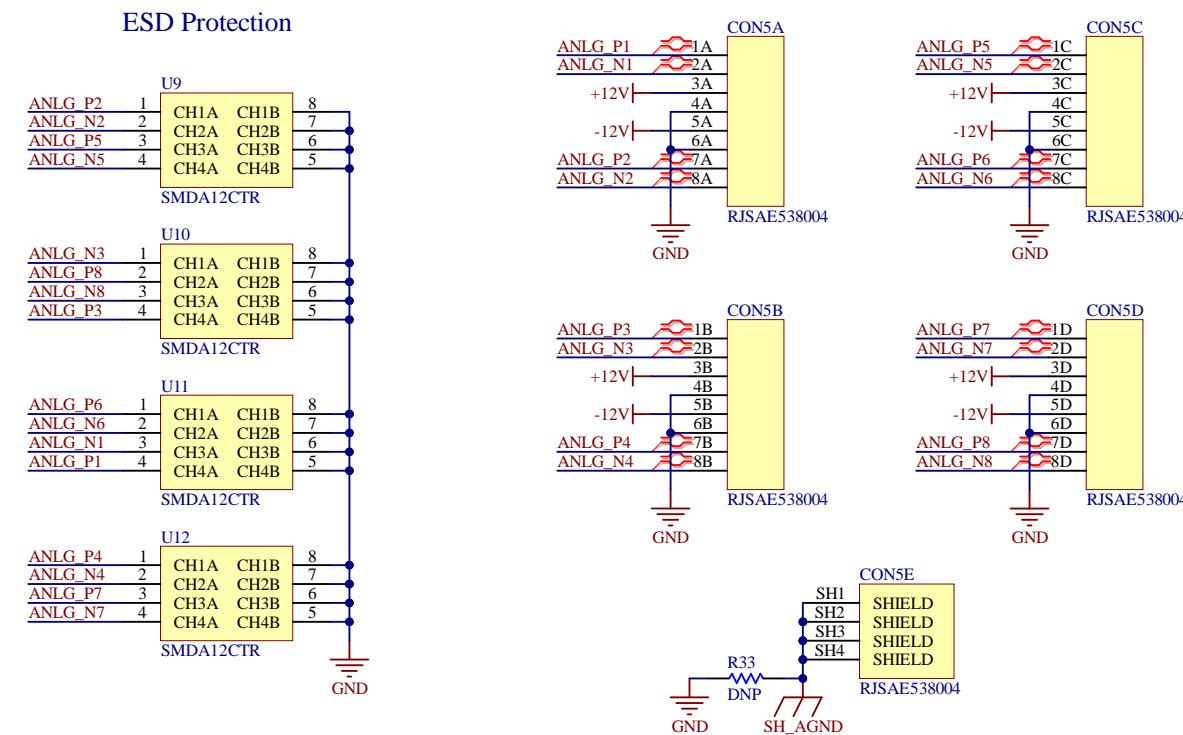
Engineer: **Nathan Petersen**

A



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Title: *Analog RJ45 Connectors*File: *AnalogConnectors.SchDoc*

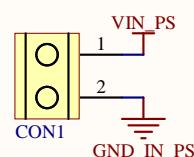
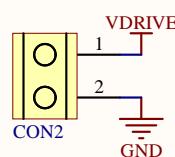
Revision: A Time: 12:19:10 PM

Sheet: 15 of 26 Date: 10/31/2020

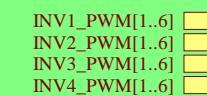
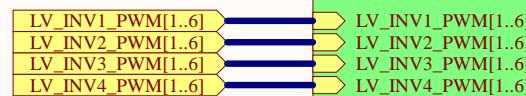
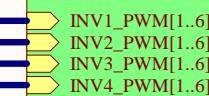
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Engineer: Nathan Petersen

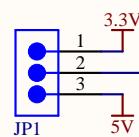
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POWERSTACK VIN**VDRIVE**

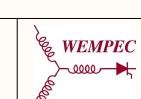
B

**U_InverterTranslation
InverterTranslation.SchDoc****U_InverterConnectors
InverterConnectors.SchDoc**

C

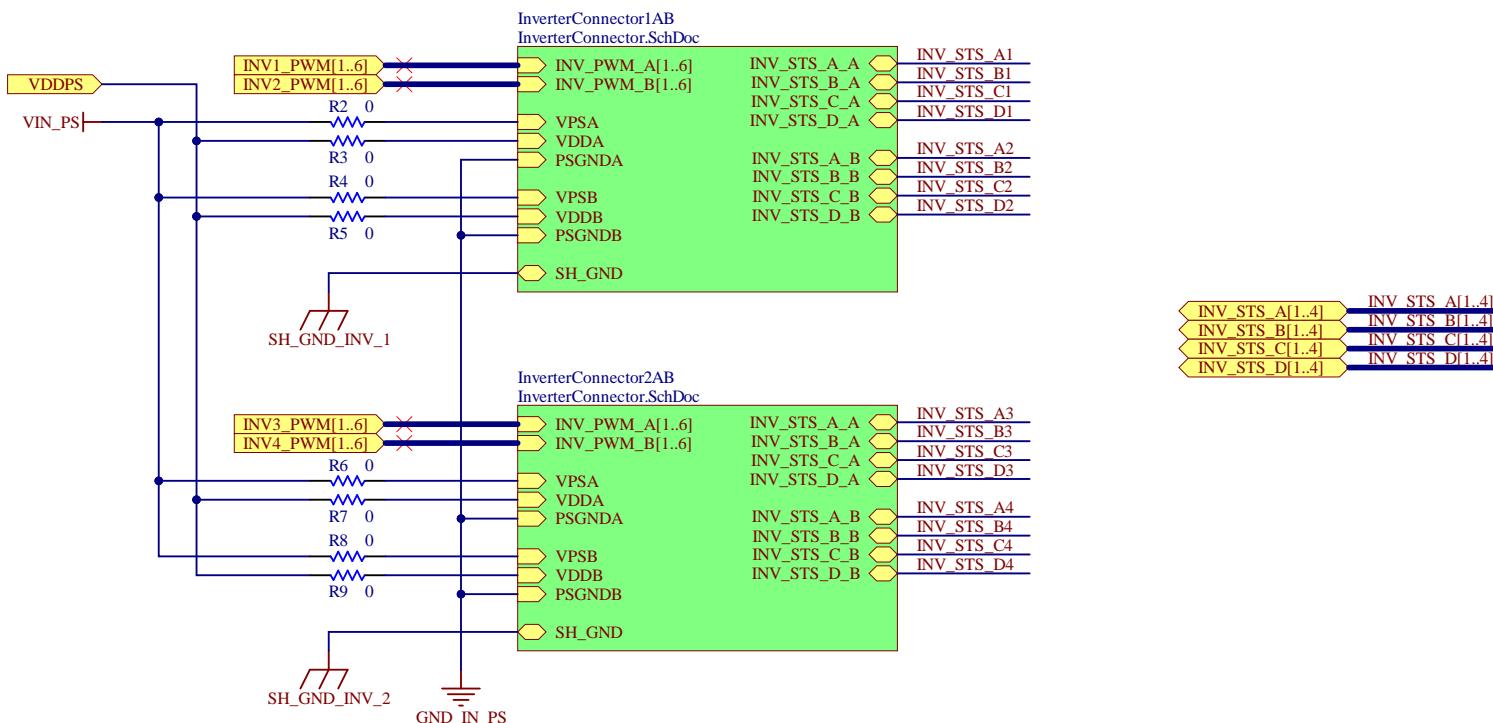


D

Title: **DriveInterface**File: **DriveInterface.SchDoc**Sheet: **16 of 26**Revision: **A** Time: **12:19:10 PM**Date: **10/31/2020** Engineer: **Prasoon Sinha****Severson Group
WEMPEC
UW Madison**

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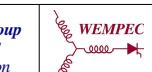
D

D

Title: **Inverter Connectors**

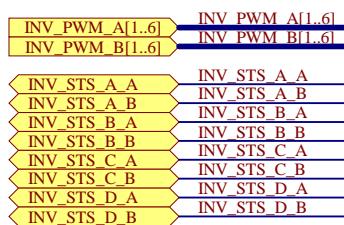
File: InverterConnectors.SchDoc | Sheet: 17 of 26

Revision: A | Time: 12:19:10 PM | Date: 10/31/2020

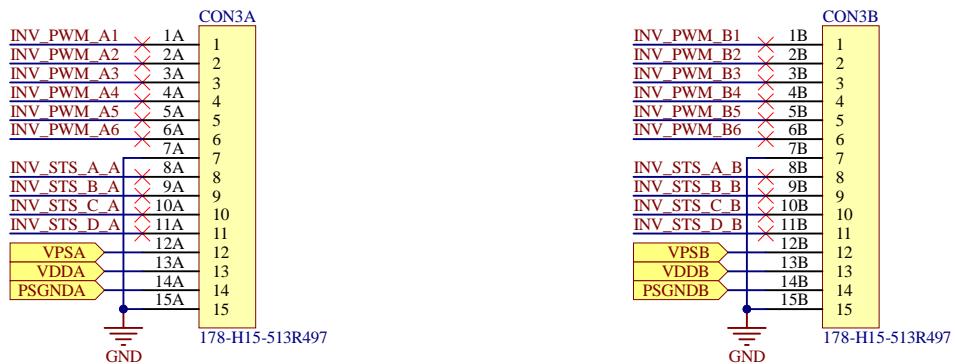
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Engineer: Nathan Petersen

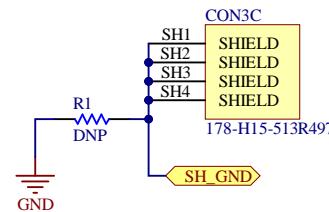
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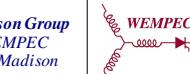
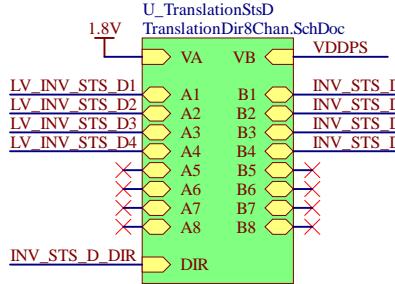
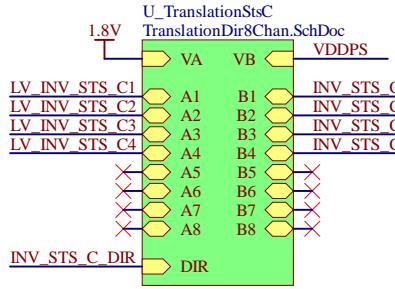
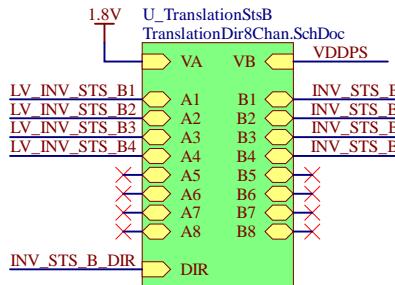
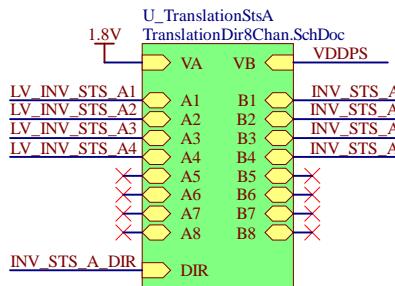
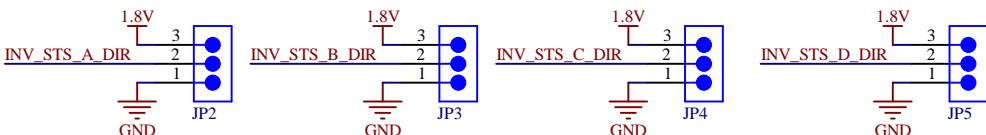
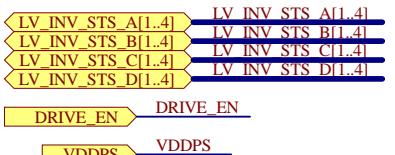
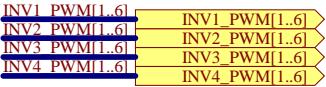
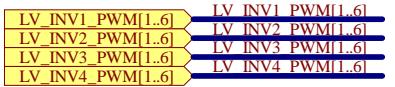
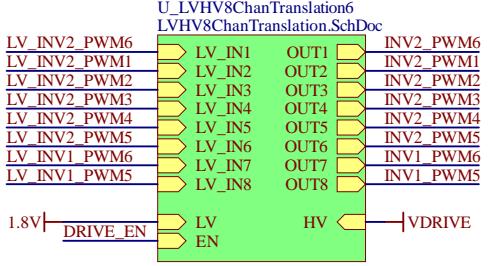
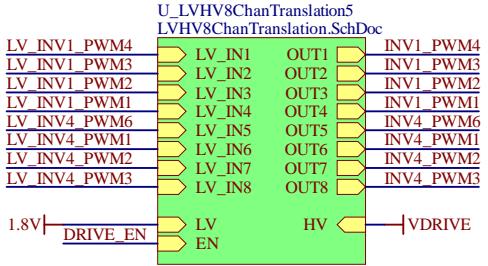
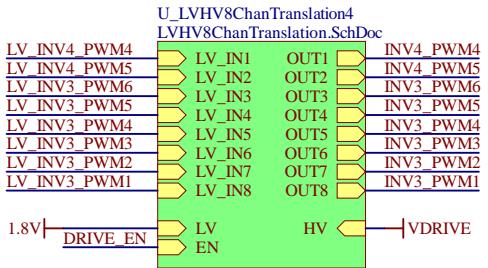
C



D

Title: Inverter Connector		Severson Group WEMPEC UWMadison
File: InverterConnector.SchDoc	Sheet: 18 of 26	
Revision: A	Time: 12:19:10 PM	
Date: 10/31/2020		Engineer: Nathan Petersen

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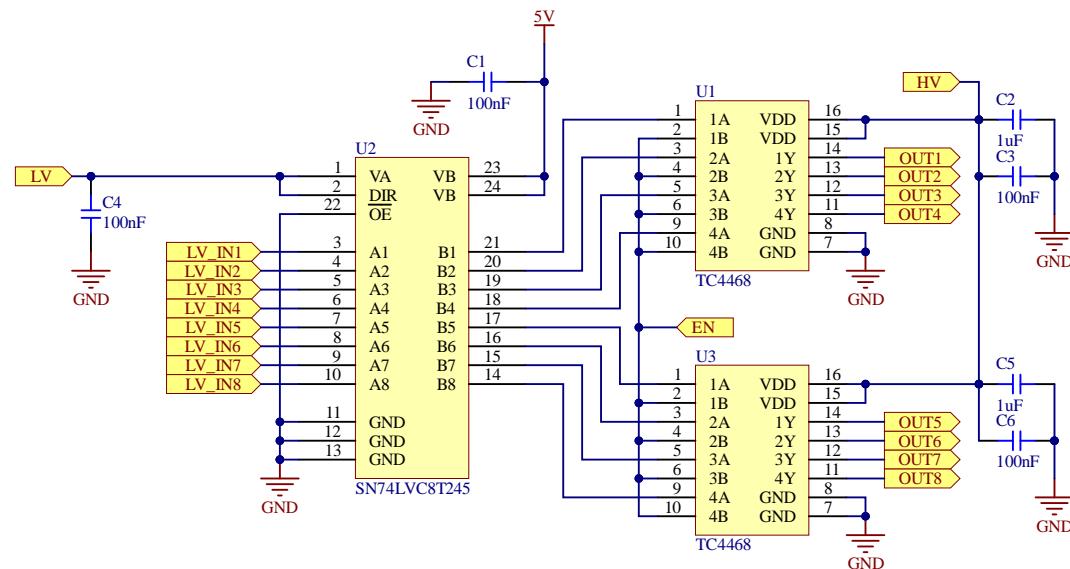
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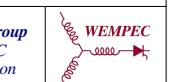
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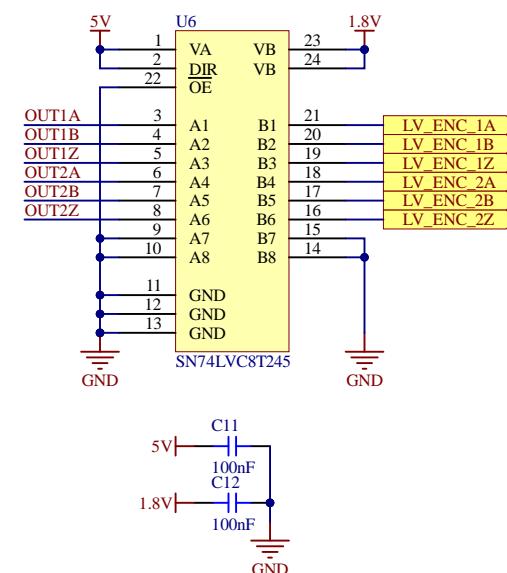
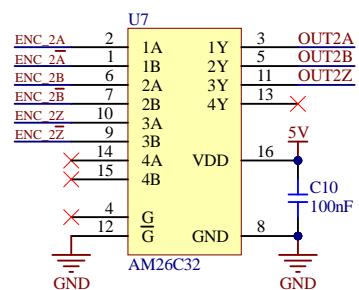
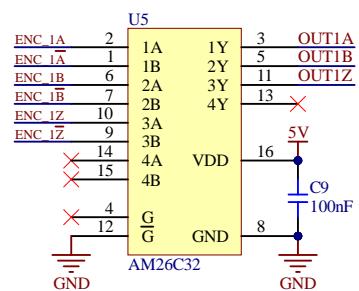
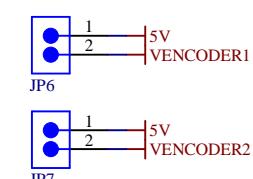
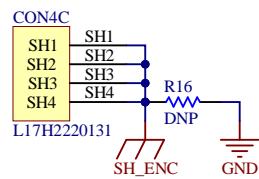
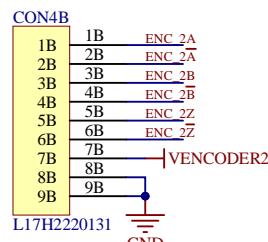
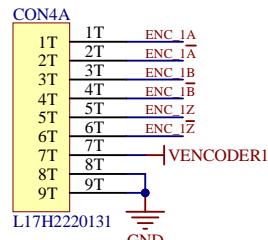
D

Title: **8-channel LV to HV Translation**File: **LVHV8ChanTranslation.SchDoc** | Sheet: **20 of 26**Revision: **A** | Time: **12:19:10 PM** | Date: **10/31/2020**

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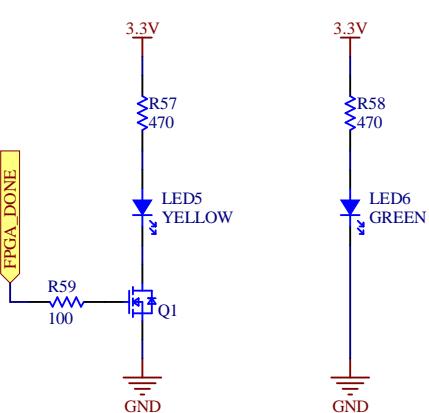
Engineer: **Prasoon Sinha**

A

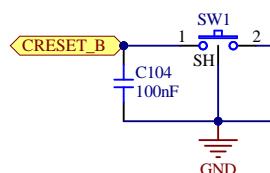


FPGA STATUS LEDS

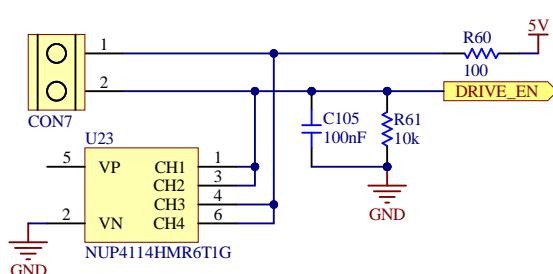
FPGA DONE



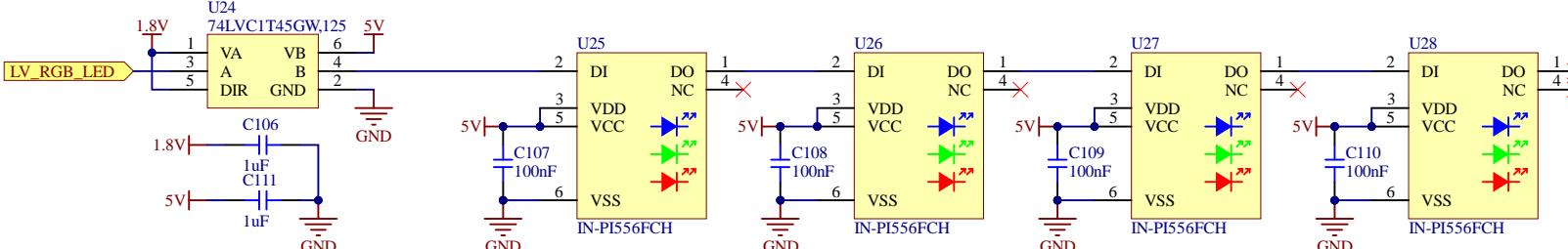
RESET BUTTON



DRIVE ENABLE (ESTOP)



FPGA RGB LEDs

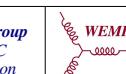


Title: **FPGA I/O Interface**

File: **FPGA_IO.SchDoc** Sheet: **22 of 26**

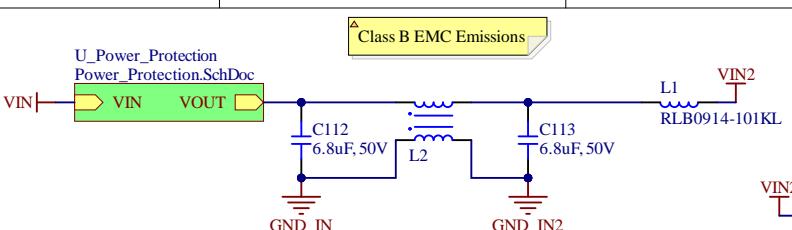
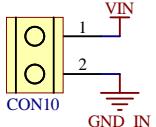
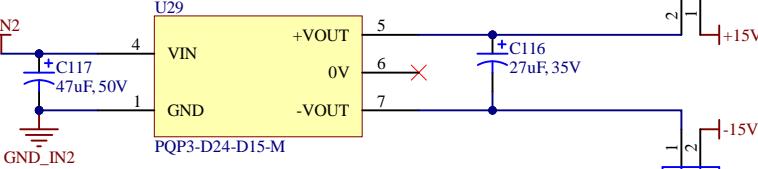
Revision: **A** Time: **12:19:10 PM** Date: **10/31/2020**

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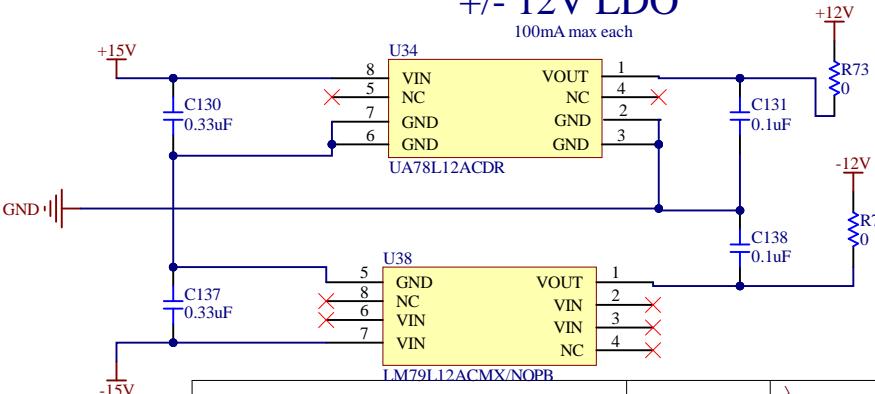
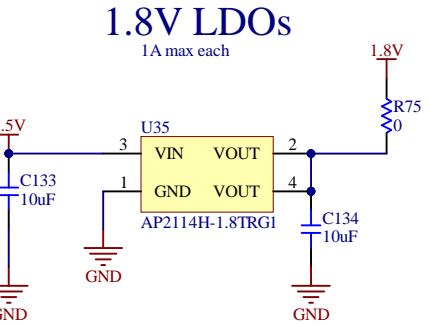
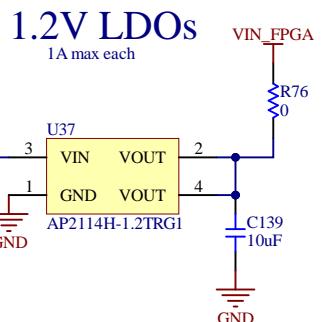
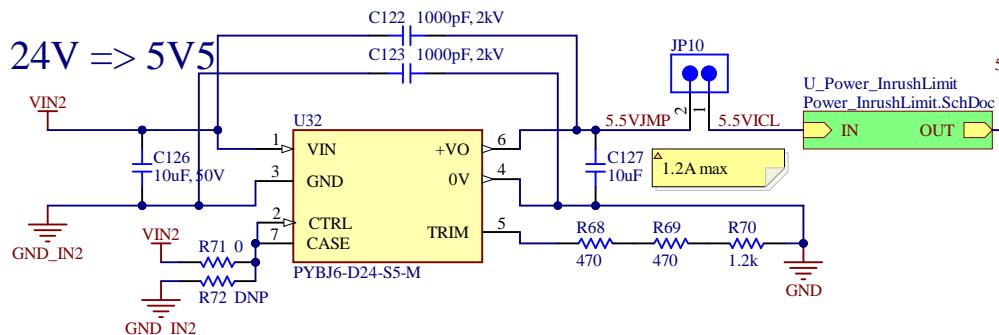
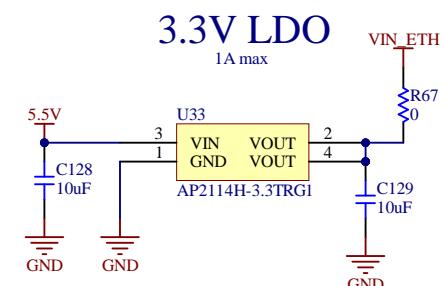
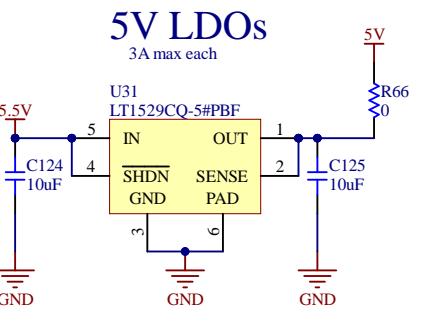


Engineer: **Prasoon Sinha**

VIN (assumed 24V DC)


 $24V \Rightarrow +15V$
 $24V \Rightarrow -15V$


A	<table border="1"> <tr><td>5V</td><td>VIN_FPGA</td><td><=> General</td></tr> <tr><td>3.3V</td><td></td><td><=> General</td></tr> <tr><td>1.8V</td><td></td><td><=> General</td></tr> <tr><td>2.048VREF</td><td></td><td><=> ADC ref / SigCond1..8</td></tr> <tr><td>+/-15V</td><td></td><td><=> Con1..4 / SigCond1..8</td></tr> <tr><td>VIN_ETH (3.3V)</td><td></td><td><=> Ethernet Power Supply</td></tr> </table>	5V	VIN_FPGA	<=> General	3.3V		<=> General	1.8V		<=> General	2.048VREF		<=> ADC ref / SigCond1..8	+/-15V		<=> Con1..4 / SigCond1..8	VIN_ETH (3.3V)		<=> Ethernet Power Supply
5V	VIN_FPGA	<=> General																	
3.3V		<=> General																	
1.8V		<=> General																	
2.048VREF		<=> ADC ref / SigCond1..8																	
+/-15V		<=> Con1..4 / SigCond1..8																	
VIN_ETH (3.3V)		<=> Ethernet Power Supply																	
B	<p>3.3V LDO 1A max</p> <p>U36</p> <p>VIN GND VOUT</p> <p>AP2114H-3.3TRGI</p> <p>3.3V</p> <p>R74</p> <p>C132 10uF</p> <p>GND</p> <p>C135 10uF</p> <p>GND</p>																		



A

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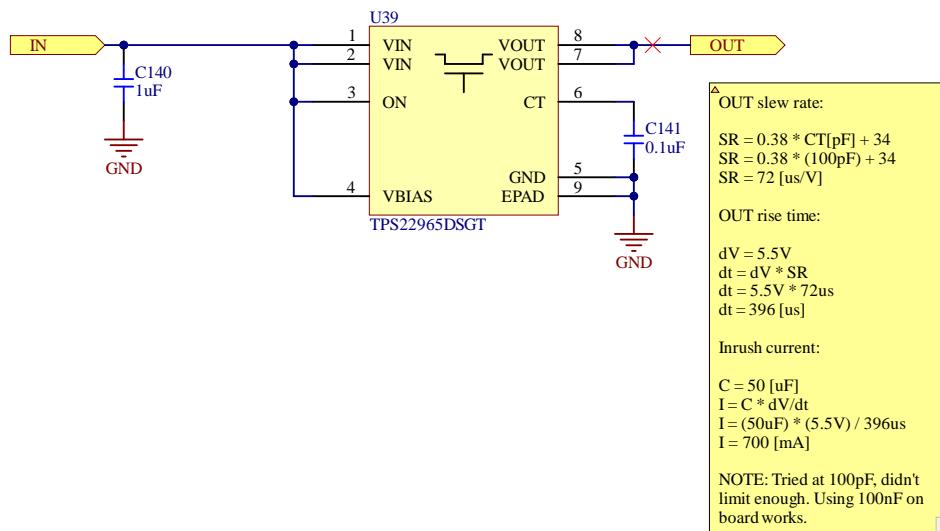
B

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C

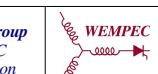
D

D

Title: **Inrush Current Limiter**

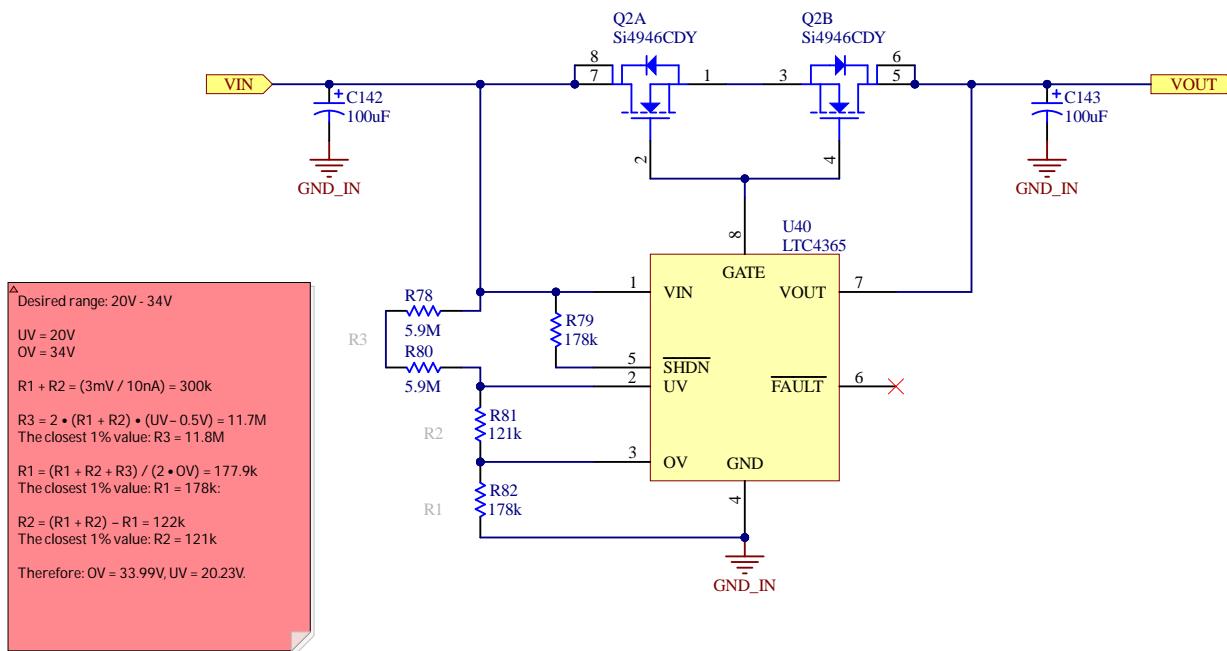
File: Power_InrushLimit.SchDoc | Sheet: 24 of 26

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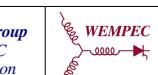
B

C

C

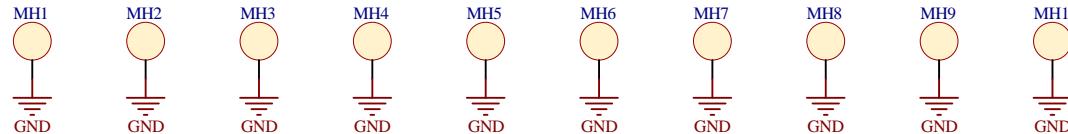
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Title: **Power Protection**File: **Power_Protection.SchDoc**Sheet: **25 of 26**Revision: **A** Time: **12:19:11 PM**Date: **10/31/2020**
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4-40 Screws:**4-40 Standoffs:****Mouting Holes:**

C

C

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D

Title: ***Back Page***File: **BackPage.SchDoc**Sheet: **26 of 26**Revision: **A** Time: **12:19:11 PM**Date: **10/31/2020** Engineer: **Nathan Petersen**

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