

4x RGB LEDs, E-STOP



## BOARD I/O

4x GPIO ports  
each with  
3 diff inputs,  
3 diff outputs

### GPIO

8x channel  
+/-10V diff.  
pair inputs

### ANALOG INPUTS

8x full 3-phase  
2-level inverters

### DRIVE OUTPUTS

2x quadrature  
input (A,B,Z)

### ENCODER

# PicoZed

7030

U\_PicoZed

PicoZed.SchDoc

### JTAG / UART



### ETHERNET



### EEPROM

A

A

B

B

C

C

D

D

24V -15V +15V 5V 3.3V 2.048V 1.8V

24V

VINPS

VDRIVE

## POWER

Power inputs  
to board

U\_BackPage

BackPage.SchDoc

U\_RevisionChanges

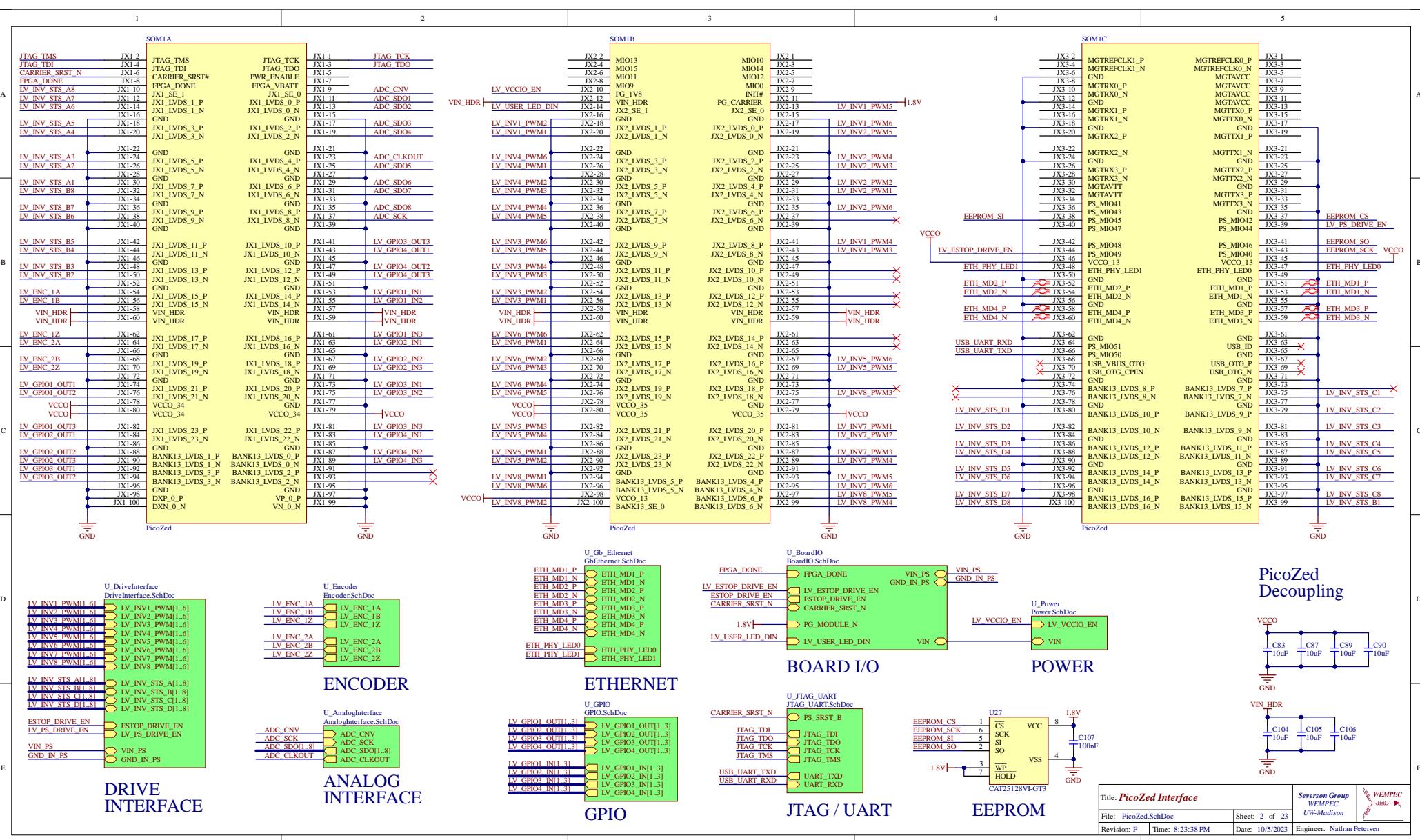
RevisionChanges.SchDoc

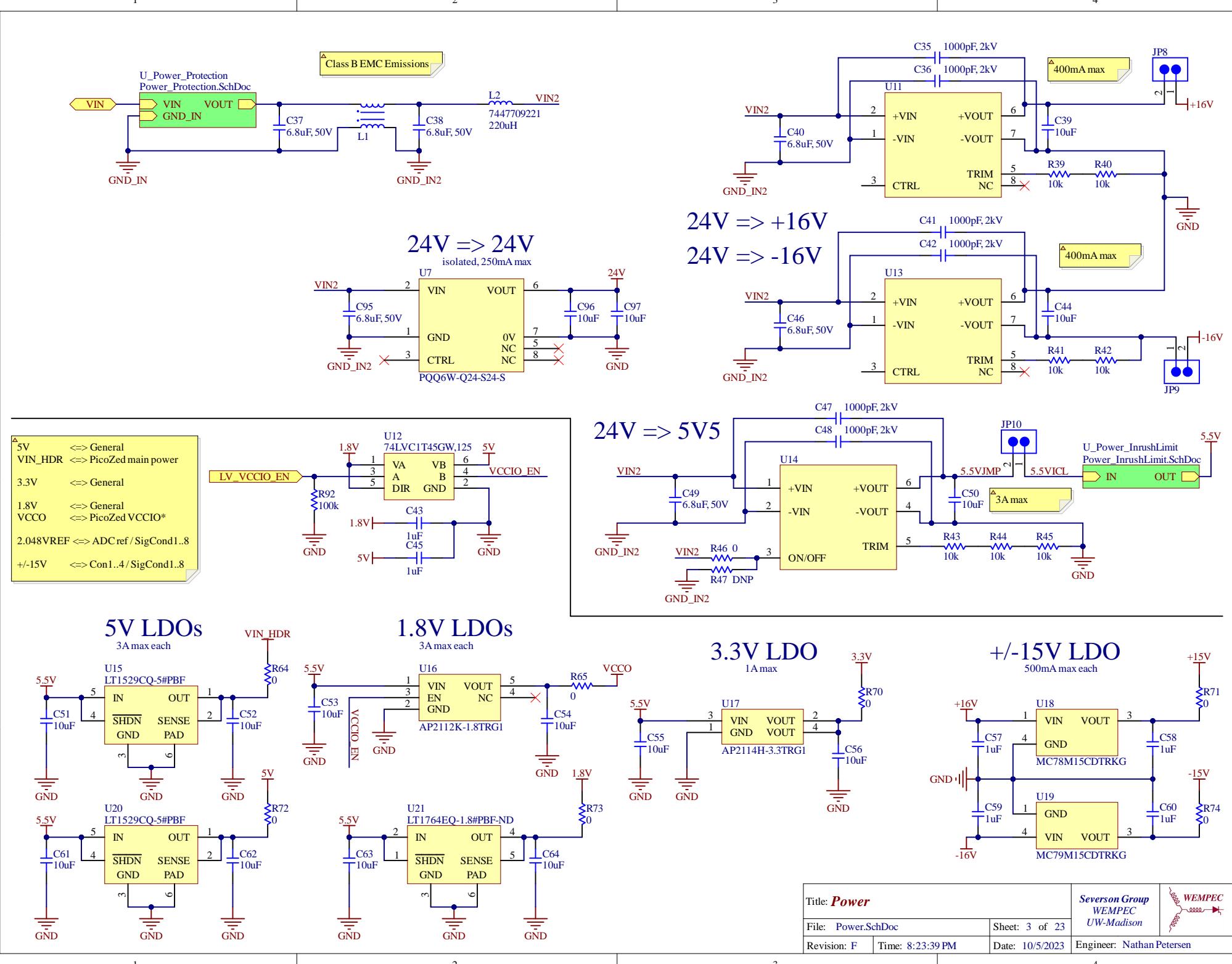
Title: *Advanced Motor Drive Controller*File: *AMDC.SchDoc* Sheet: 1 of 23

Revision: F Time: 8:23:38 PM Date: 10/5/2023

Severson Group  
WEMPEC  
UW-Madison

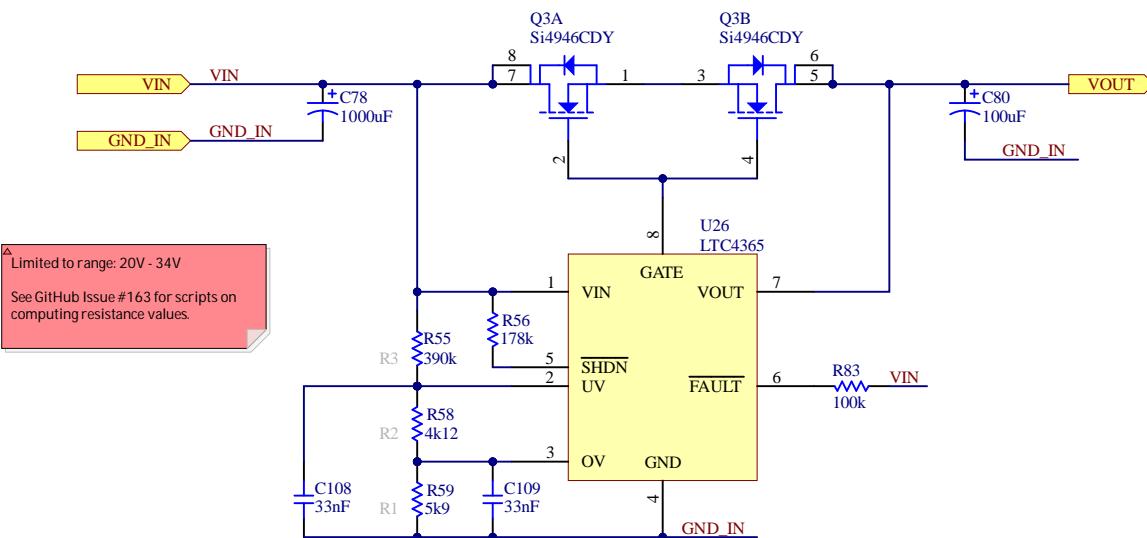
Engineer: Nathan Petersen





A

A



B

B

C

C

D

D

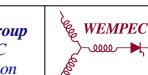
Title: **Power Protection**

File: Power\_Protection.SchDoc

Revision: F Time: 8:23:39 PM

Sheet: 4 of 23

Date: 10/5/2023

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**WEMPEC**  
**UW-Madison**


Engineer: Nathan Petersen

A

A

B

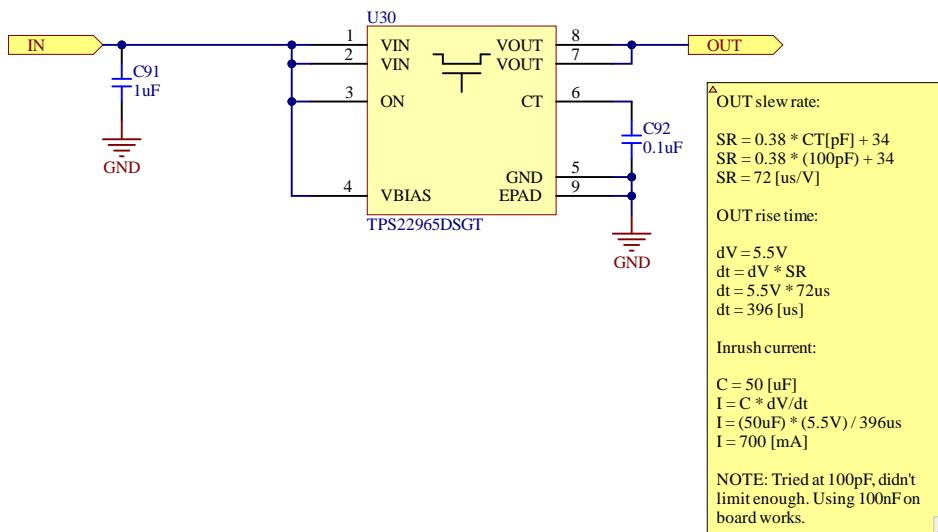
B

C

C

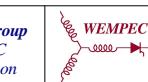
D

D

Title: **Inrush Current Limiter**

File: Power\_InrushLimit.SchDoc | Sheet: 5 of 23

Revision: F | Time: 8:23:39 PM | Date: 10/5/2023

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Engineer: Nathan Petersen

A

A

B

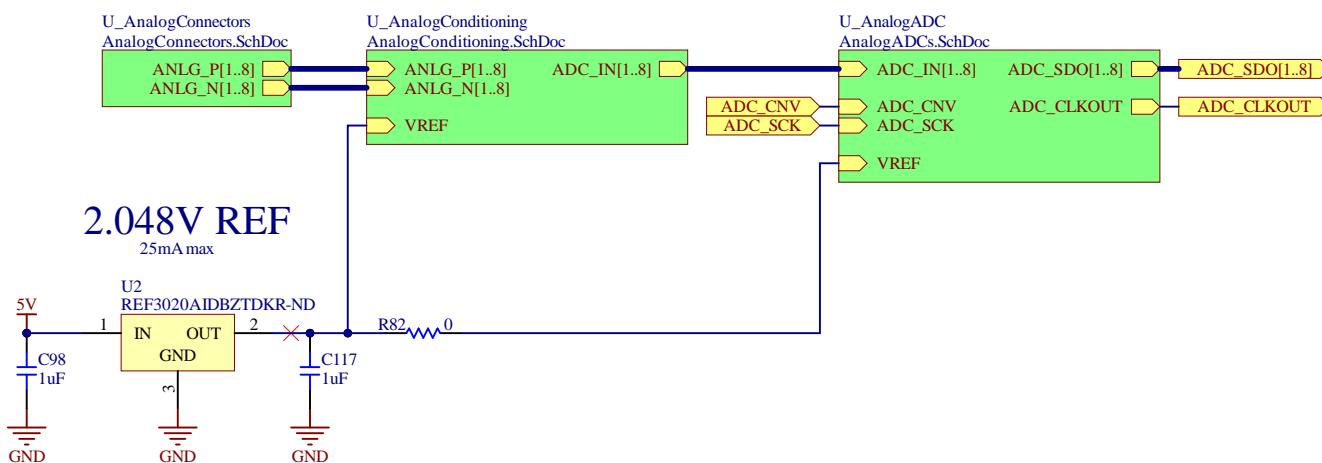
B

C

C

D

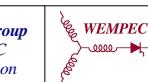
D

Title: *Analog Interface*File: *AnalogInterface.SchDoc*

Sheet: 6 of 23

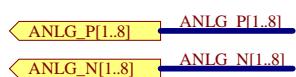
Revision: F Time: 8:23:39 PM Date: 10/5/2023

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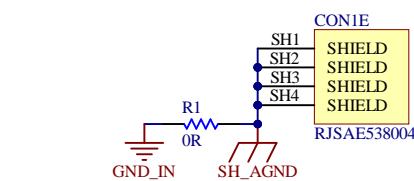
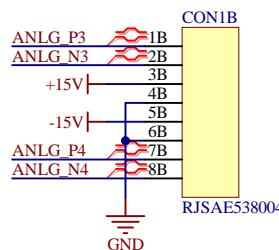
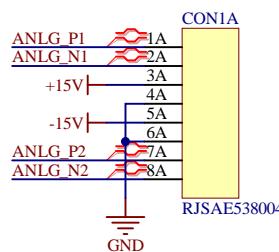
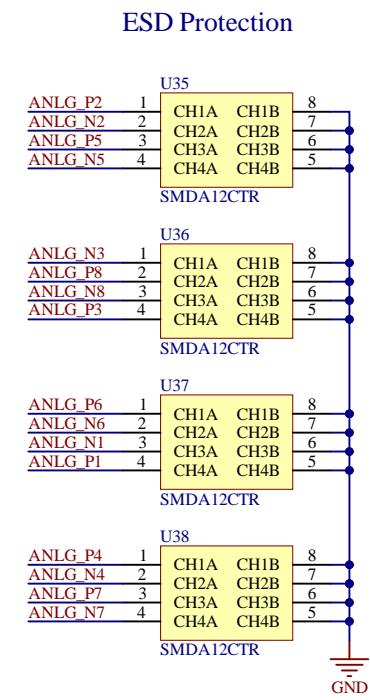


Engineer: Nathan Petersen

A



B



Force no input to 0V

ANLG_P1	R84 100k	ANLG_N1
ANLG_P2	R85 100k	ANLG_N2
ANLG_P3	R86 100k	ANLG_N3
ANLG_P4	R87 100k	ANLG_N4
ANLG_P5	R88 100k	ANLG_N5
ANLG_P6	R89 100k	ANLG_N6
ANLG_P7	R90 100k	ANLG_N7
ANLG_P8	R91 100k	ANLG_N8

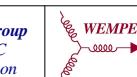
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Title: **Analog RJ45 Connectors**

File: **AnalogConnectors.SchDoc** | Sheet: **7 of 23**

Revision: **F** | Time: **8:23:39 PM** | Date: **10/5/2023**

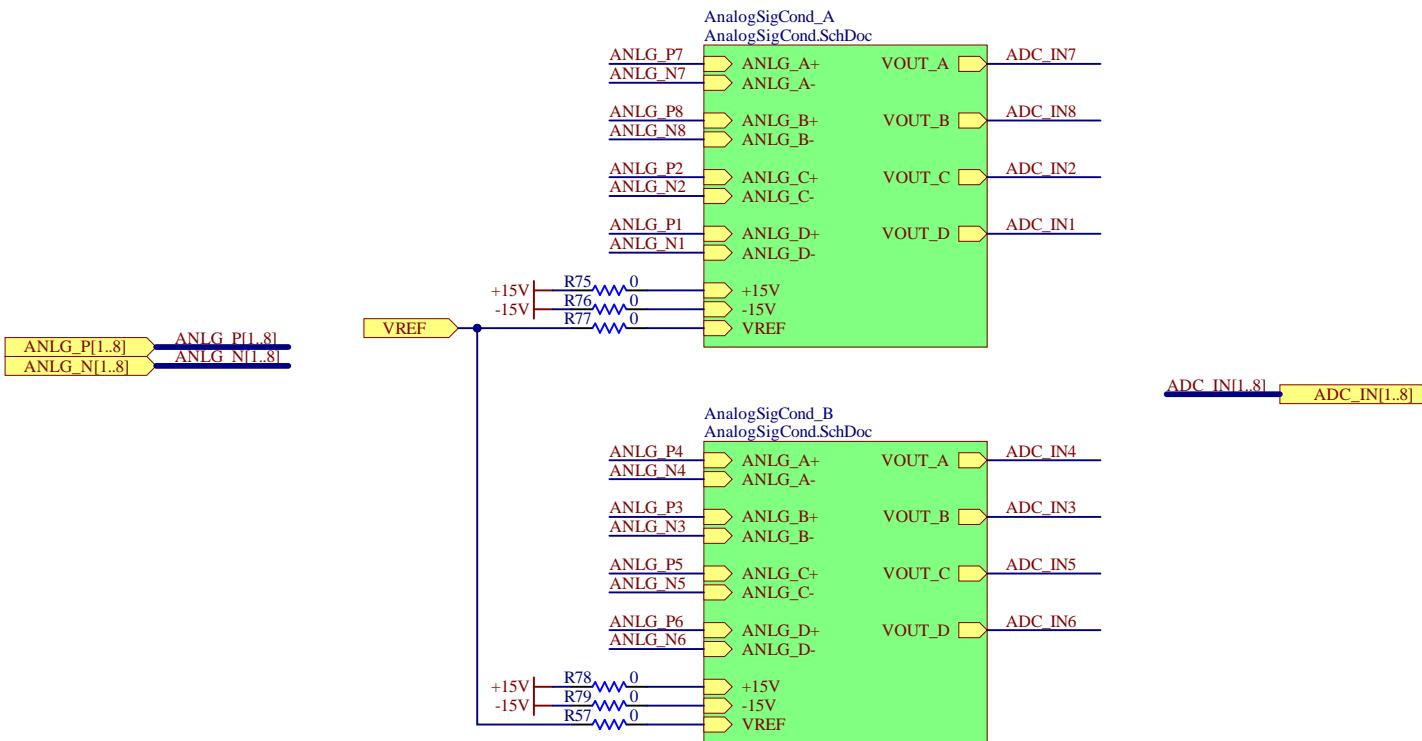
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**WEMPEC**  
**UW-Madison**



Engineer: **Nathan Petersen**

A

A



B

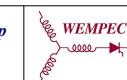
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C

C

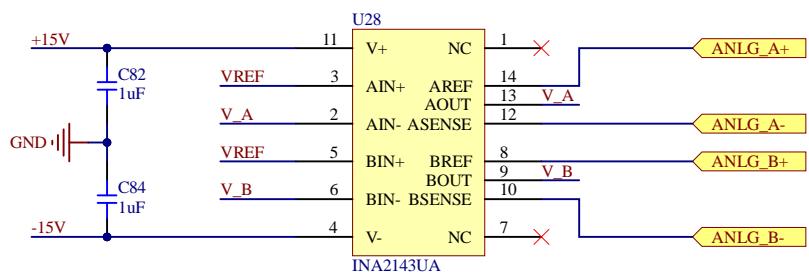
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D

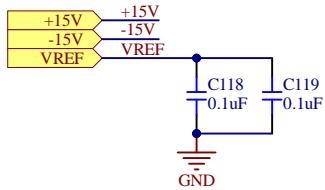
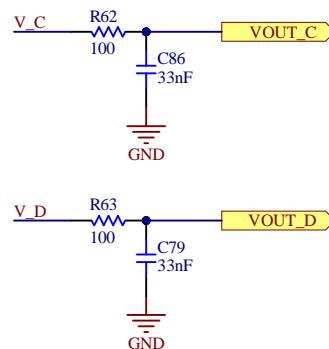
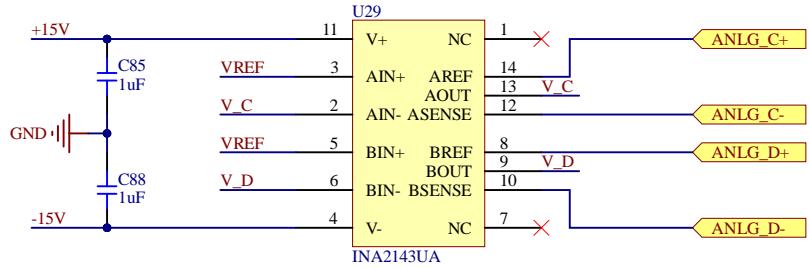
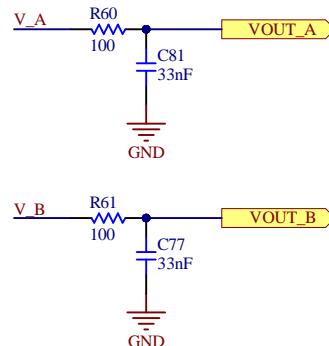
Title: **Analog Signal Conditioning**File: **AnalogConditioning.SchDoc** Sheet: **8 of 23**Revision: **F** Time: **8:23:39 PM**Date: **10/5/2023****Severson Group**  
**WEMPEC**  
**UW-Madison**Engineer: **Nathan Petersen**

A

A



△ LPF:  $f_c = 50\text{kHz}$



Title: *Analog Signal Front-End*

File: *AnalogSigCond.SchDoc*

Sheet: 9 of 23

Revision: F Time: 8:23:39 PM

Date: 10/5/2023

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B

B

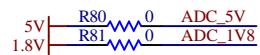
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C

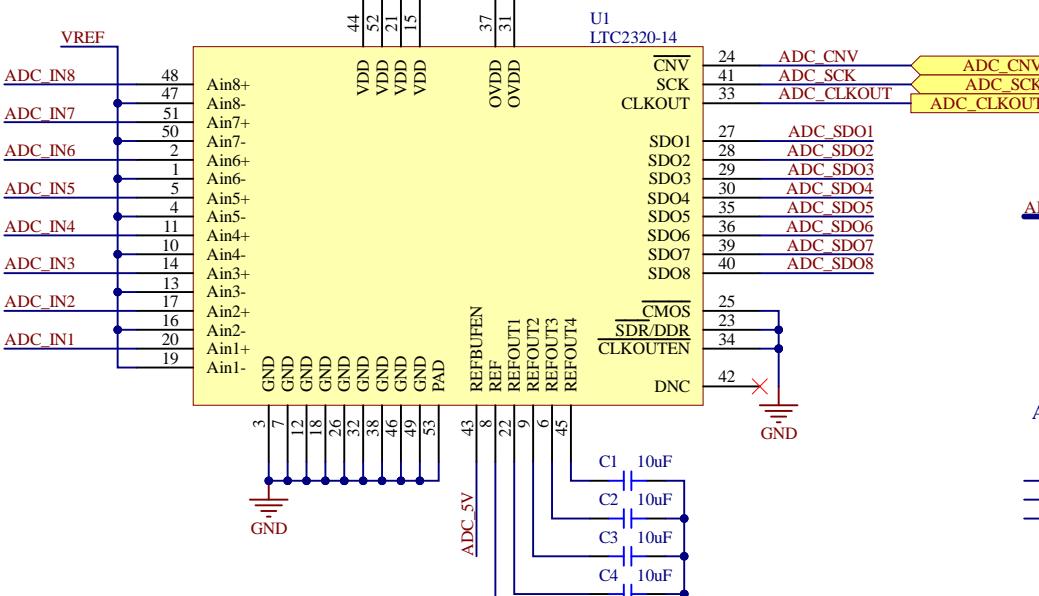
D

D

A

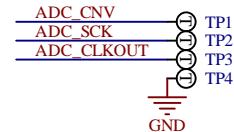


VREF  
ADC\_IN[1..8]

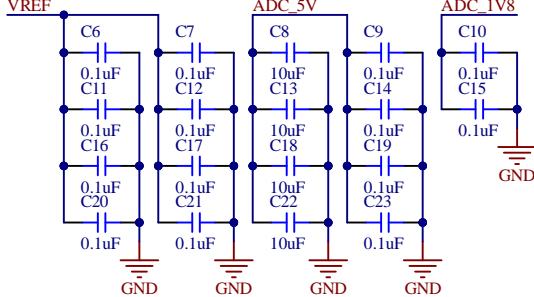


ADC\_SDO[1..8] → ADC\_SDO[1..8]

ADC Serial Interface Test Points



B



C

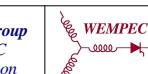
D

Title: **ADC**

File: AnalogADCs.SchDoc Sheet: 10 of 23

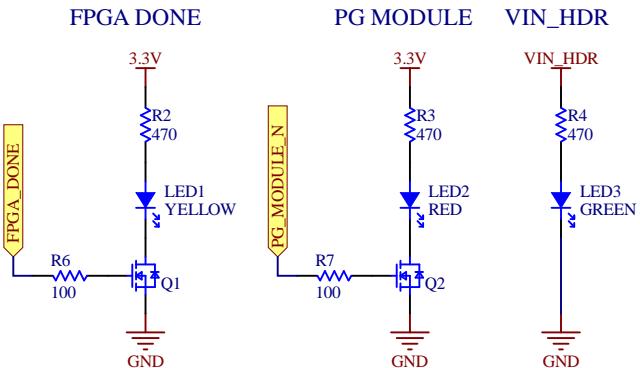
Revision: F Time: 8:23:40 PM Date: 10/5/2023

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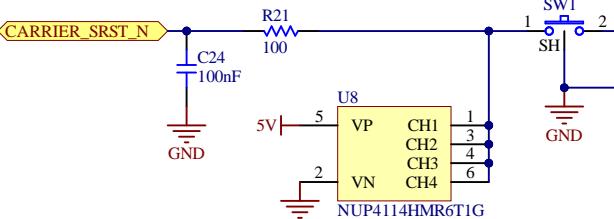


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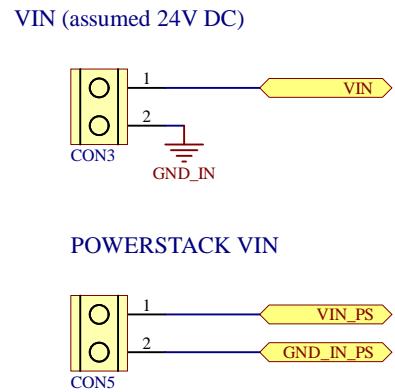
## STATUS LEDS



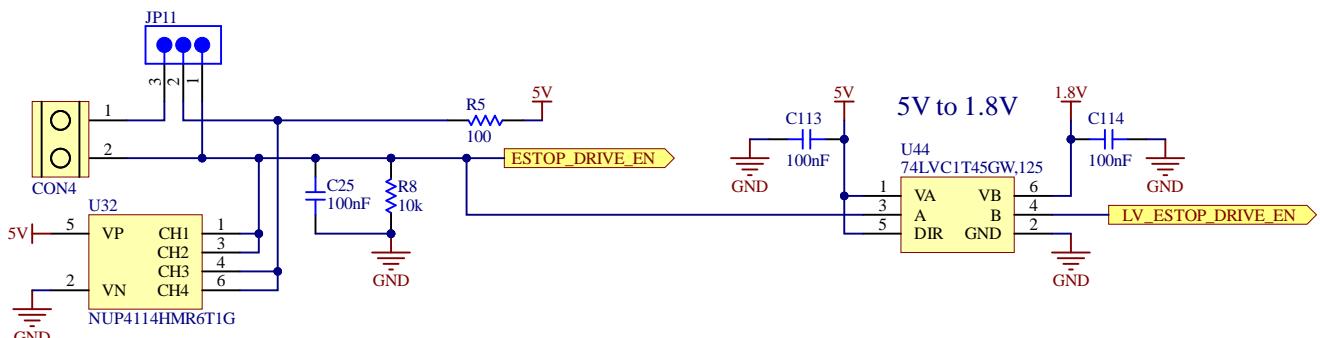
## RESET BUTTON



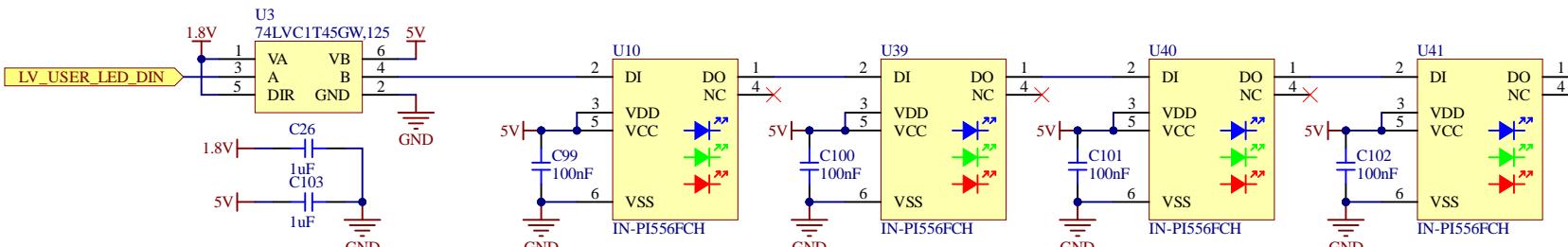
## POWER CONNECTORS



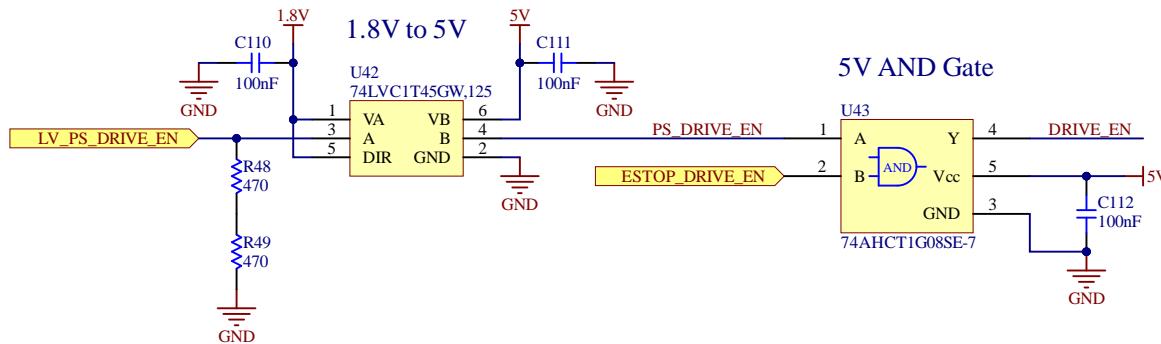
## DRIVE ENABLE (ESTOP)



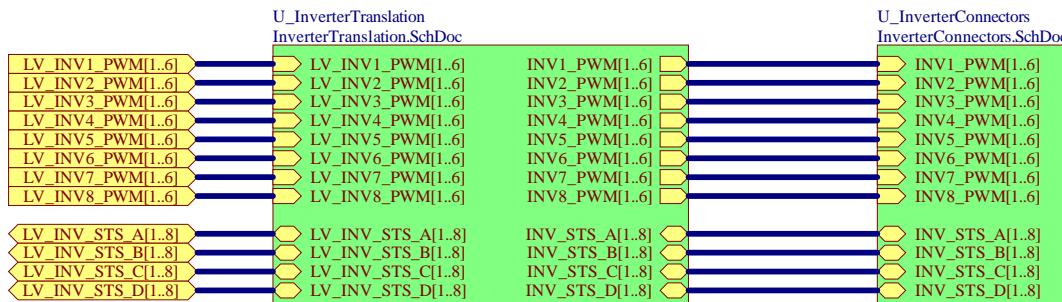
## USER RGB LEDs



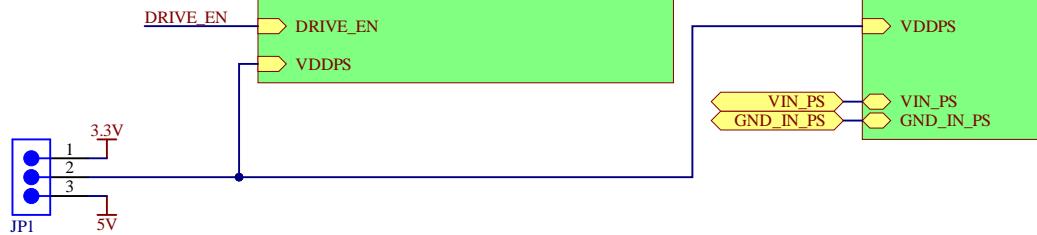
A



B



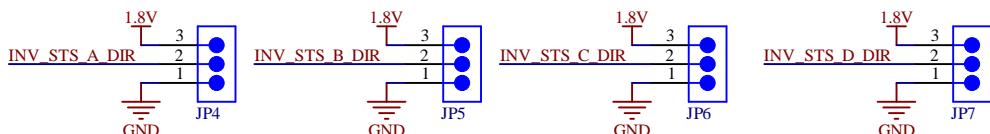
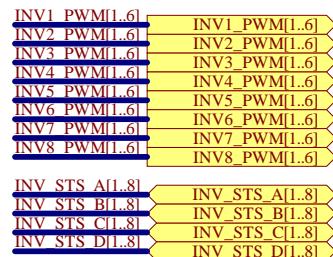
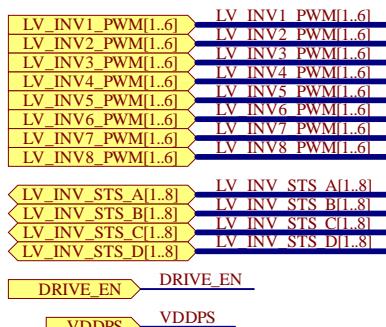
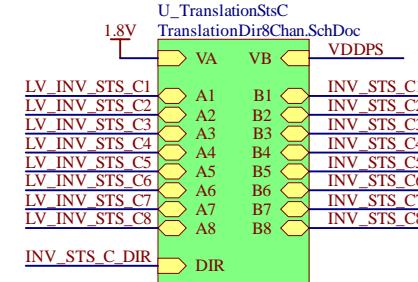
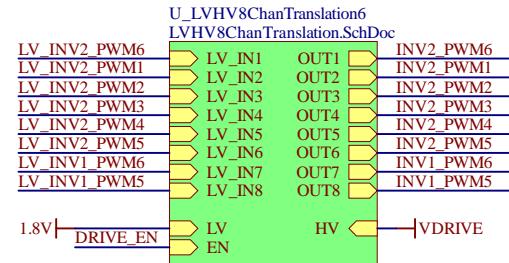
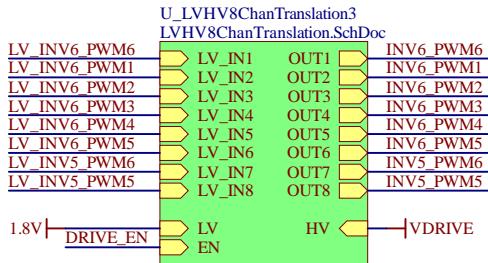
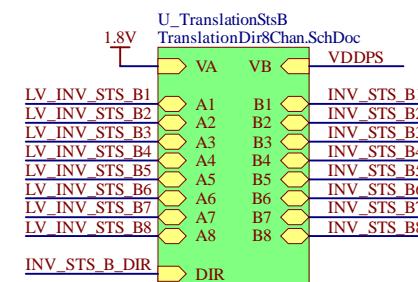
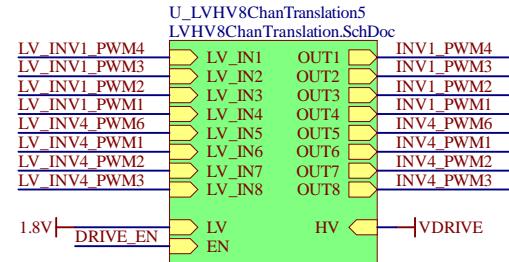
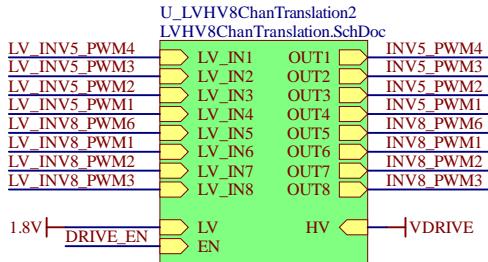
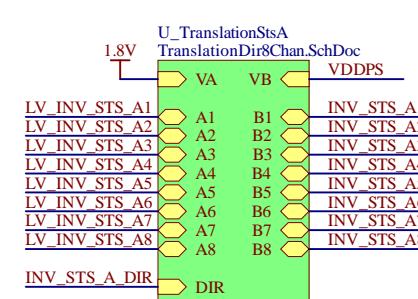
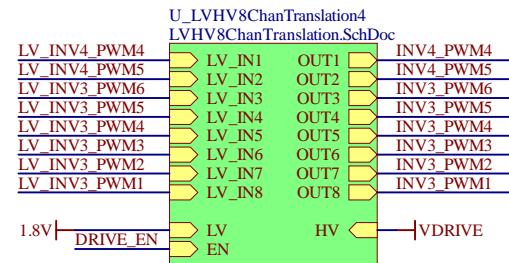
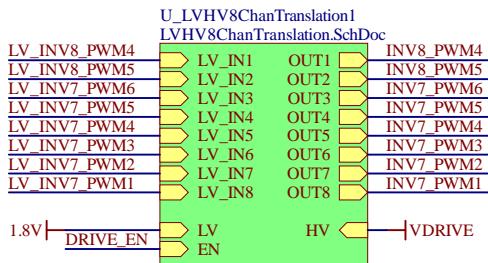
C



D

Title: <b>Drive Interface</b>			<b>Severson Group</b> WEMPEC UW-Madison
File: <b>DriveInterface.SchDoc</b>	Sheet: <b>12 of 23</b>	Revision: <b>F</b>	
Time: <b>8:23:40 PM</b>	Date: <b>10/5/2023</b>	Engineer: <b>Nathan Petersen</b>	

A

Title: **Inverter Level Translation**

File: InverterTranslation.SchDoc Sheet: 13 of 23

Revision: F Time: 8:23:40 PM Date: 10/5/2023

Severson Group  
WEMPEC  
UW-Madison

Engineer: Nathan Petersen

A

B

C

D

A

A

B

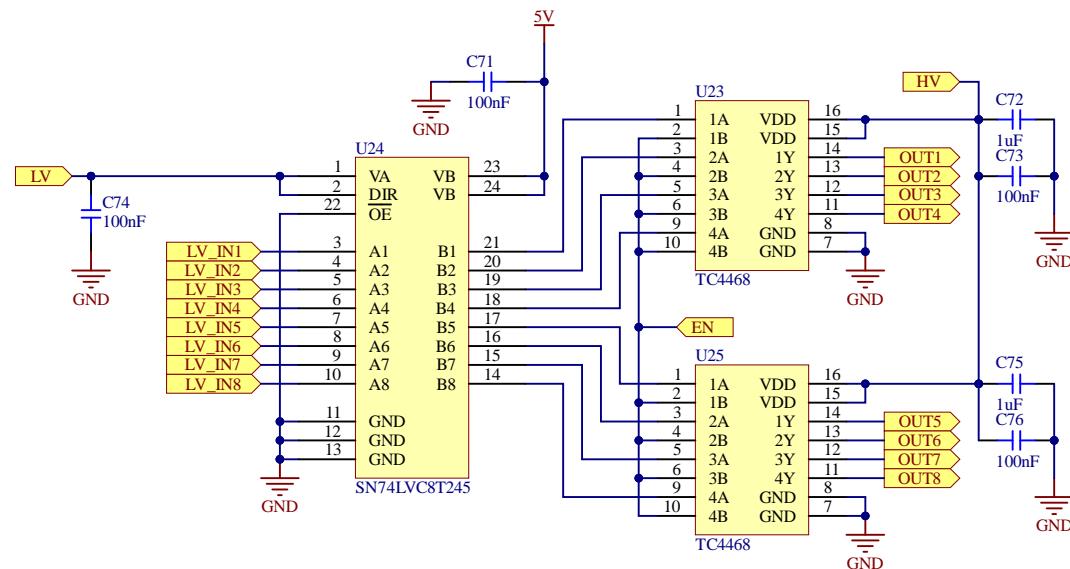
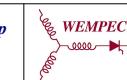
B

C

C

D

D

Title: **8-channel LV to HV Translation**File: **LVHV8ChanTranslation.SchDoc** | Sheet: **14 of 23**Revision: **F** | Time: **8:23:40 PM**Date: **10/5/2023**
**Severson Group**  
**WEMPEC**  
**UW-Madison**
Engineer: **Nathan Petersen**

A

A

B

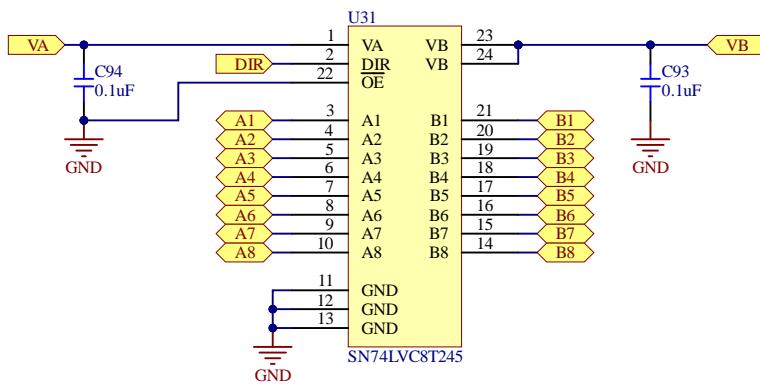
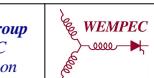
B

C

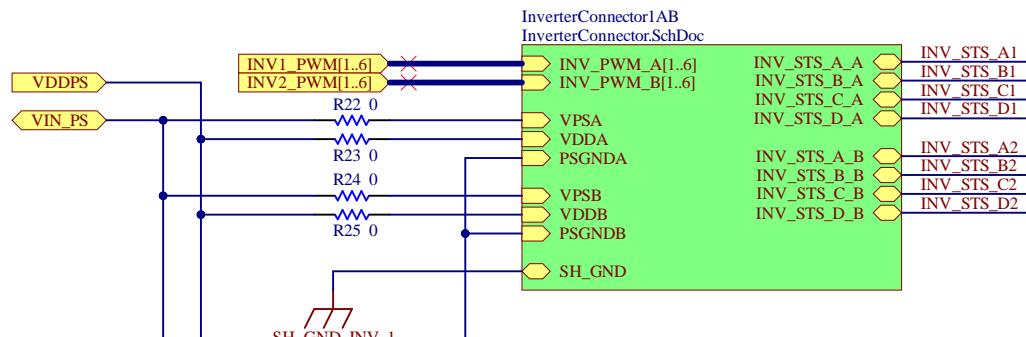
C

D

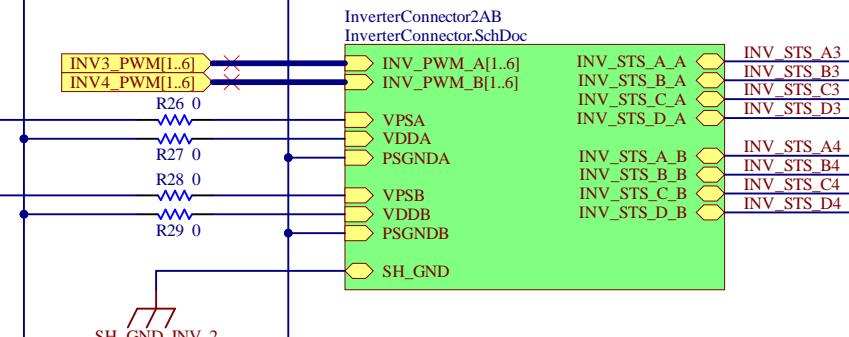
D

Title: **8-Channel Directional Translation**File: **TranslationDir8Chan.SchDoc** | Sheet: **15 of 23**Revision: **F** | Time: **8:23:40 PM** | Date: **10/5/2023**
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**UW-Madison**
Engineer: **Nathan Petersen**

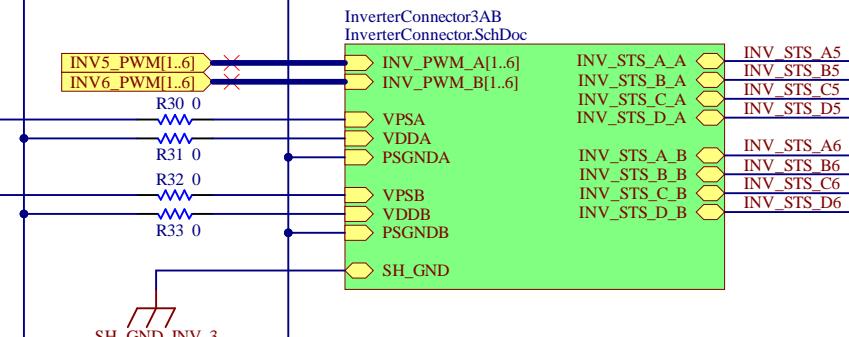
A



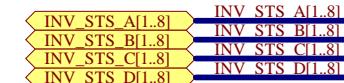
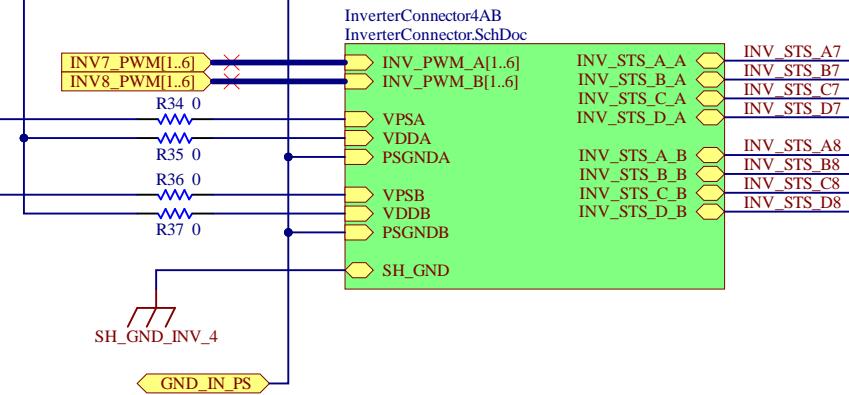
B



C



D



### Title: *Inverter Connectors*

File: InverterConnectors.SchDoc | Sheet: 16 of 23

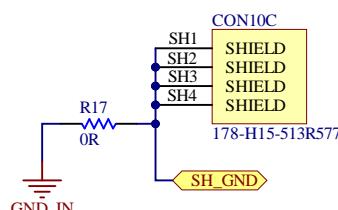
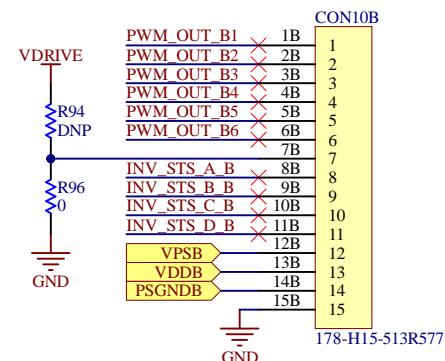
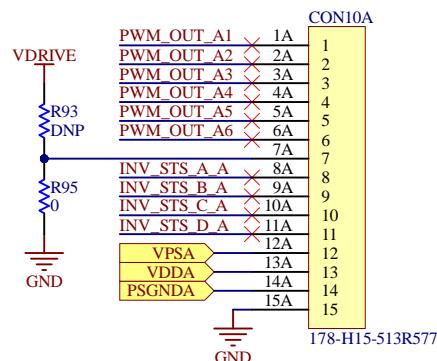
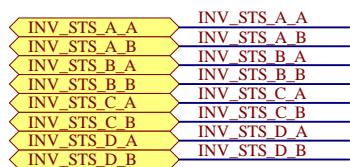
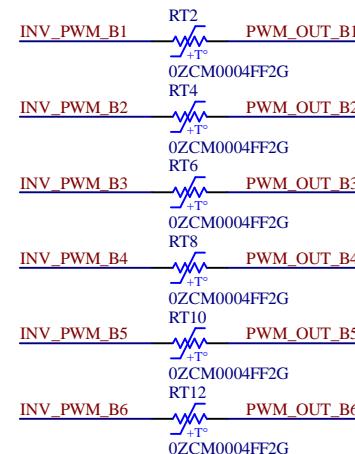
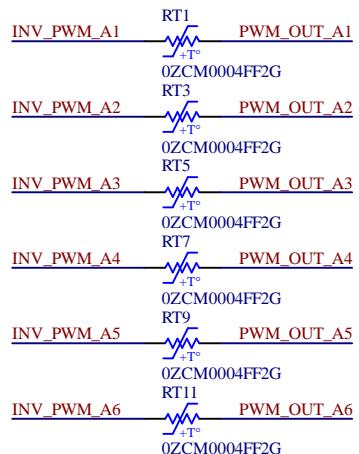
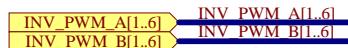
Revision: F | Time: 8:23:40 PM | Date: 10/5/2023

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UW-Madison



Engineer: Nathan Petersen

## Short Circuit Protection

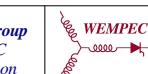


Title: **Inverter Connector**

File: InverterConnector.SchDoc | Sheet: 17 of 23

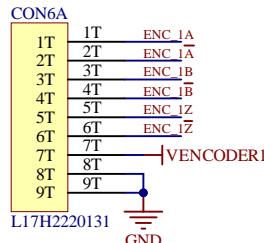
Revision: F | Time: 8:23:41 PM | Date: 10/5/2023

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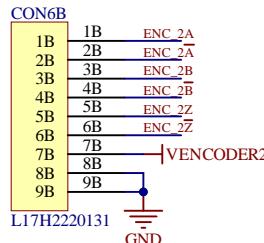
A



ENC\_1A R11 100

ENC\_1B R12 100

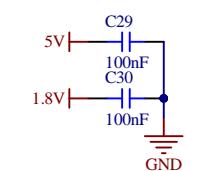
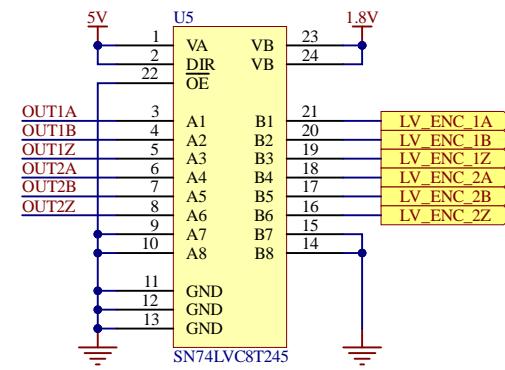
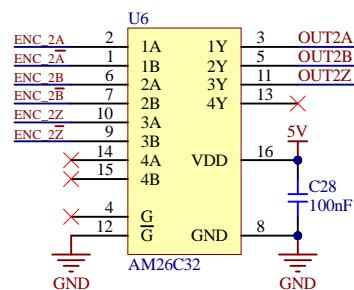
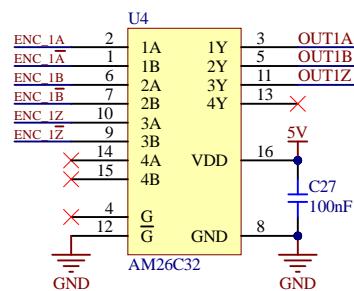
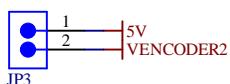
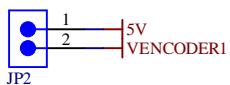
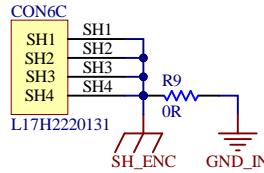
ENC\_1Z R13 100



ENC\_2A R14 100

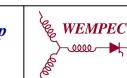
ENC\_2B R15 100

ENC\_2Z R16 100

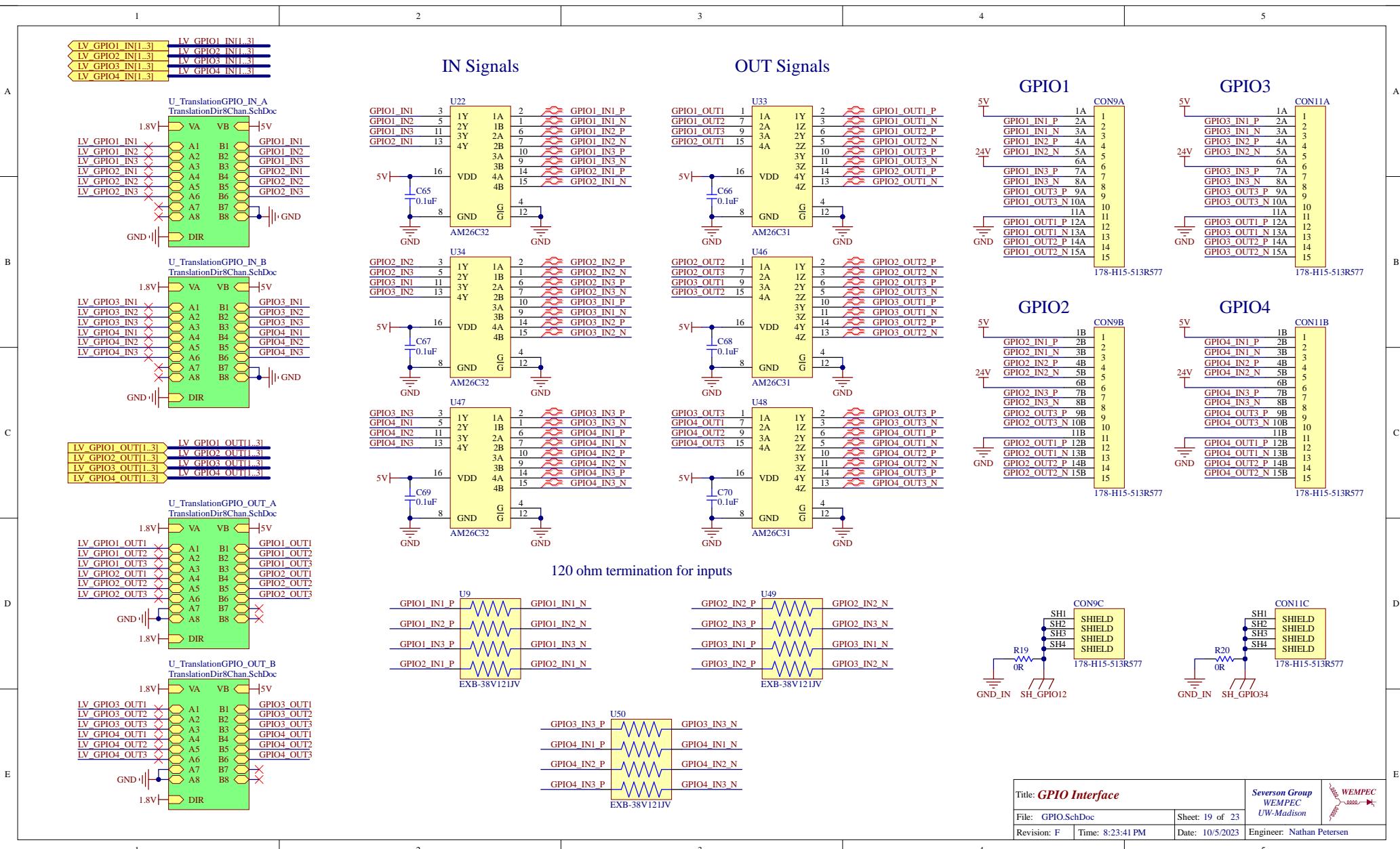
Title: **Encoders**

File: Encoder.SchDoc Sheet: 18 of 23

Revision: F Time: 8:23:41 PM Date: 10/5/2023

Severson Group  
WEMPEC  
UW-Madison

Engineer: Nathan Petersen



A

A

B

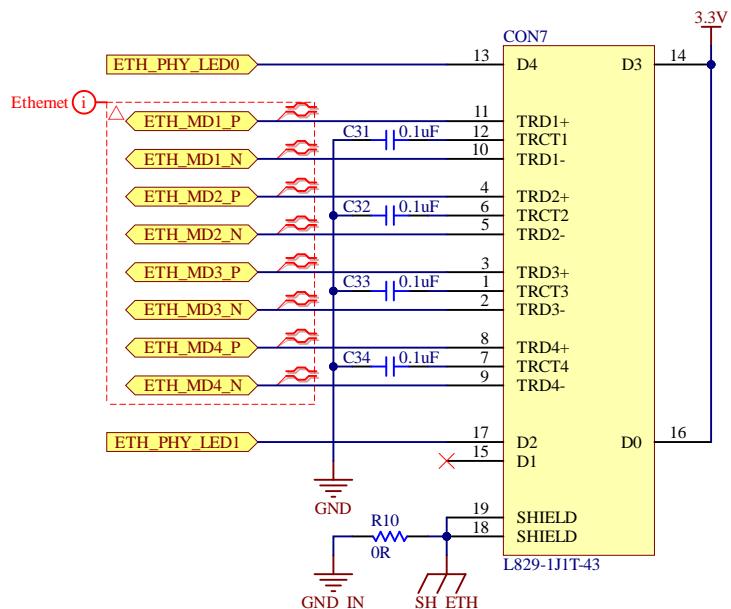
B

C

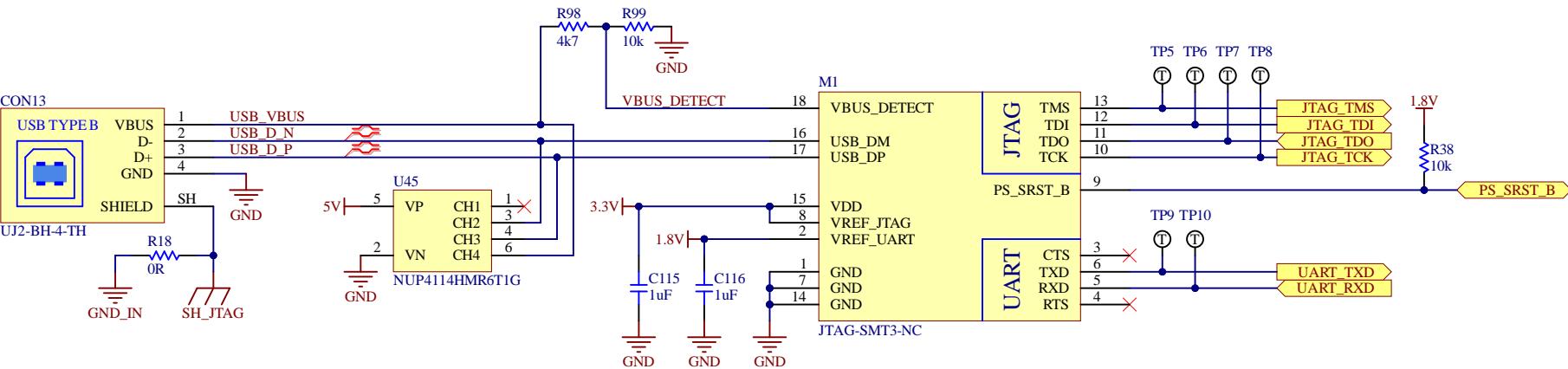
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D

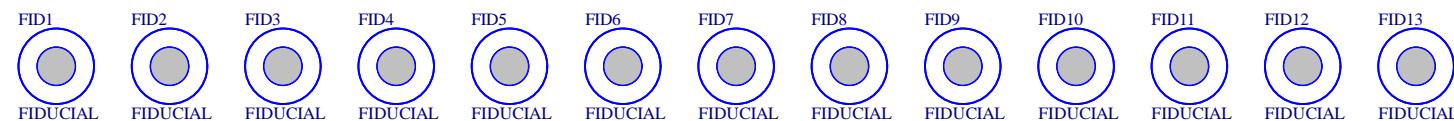
D



Title: <b>SoM Gb Ethernet</b>			Severson Group WEMPEC UW-Madison
File: GbEthernet.SchDoc			
Revision: F		Time: 8:23:41 PM	Date: 10/5/2023
Engineer: Nathan Petersen			WEMPEC



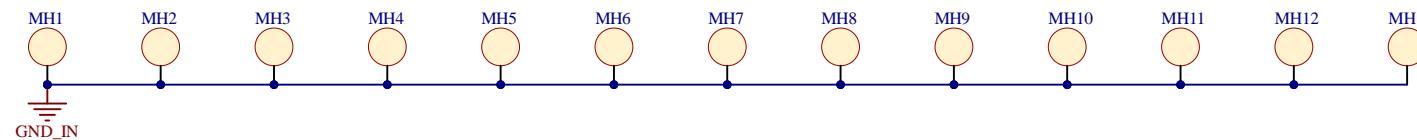
A

**Fiducials:**

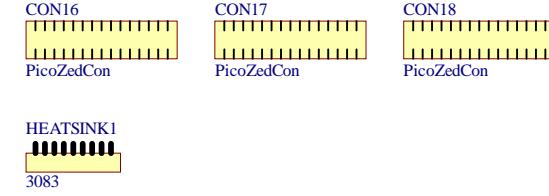
A

**4-40 Screws:**

B

**4-40 Standoffs:****Mouting Holes:**

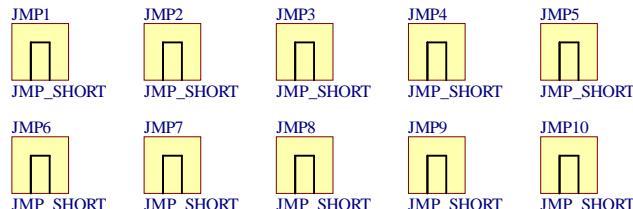
C

**PicoZed hardware:**

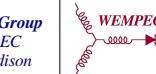
D

**Jumpers:**

Silkscreen marked with default locations

Title: ***Back Page***File: *BackPage.SchDoc* Sheet: 22 of 23

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Severson Group  
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UW-Madison

Engineer: Nathan Petersen

A

REV A: design finalized 2018-05-25

- Initial design

REV B: design finalized 2018-07-17

- Add power input protection
- Add test points
- Add TVS to analog inputs
- Change power input DC/DC modules
- Fix BOM with correct part numbers
- Fix footprints

REV C: design finalized 2018-11-21

- Add inrush current limiting to 5V5 rail
- Add more silkscreen labels
- Add test points
- Change ADC reference from 2.5V to 2.048V
- Change trim resistors for +/-16V DC/DCs
- Swap UART Tx / Rx pins
- Separate power stack shields between connectors
- Fix footprints

REV D: design finalized 2020-01-29

- New PCB form factor (6" x 6.75", 6 layers)
- Add power stack supply rail distribution
- Add isoSPI ports
- Add extra encoder port
- Add 10R resistors to subsection power for debugging
- Add 100k resistors across analog inputs
- Add serially addressable RGB LEDs
- Add EEPROM
- Add fiducials to layout
- Remove user button / switch
- Remove discrete RGB LED
- Remove ADC2, now just one ADC
- Remove unity gain op-amp driving ADC inputs
- Reduce bulk input
- Reduce 24V power filter component current ratings
- Reduce 3V3 LDO current rating
- Change level-shifter IC for UART signals
- Change JTAG to NC module
- Change JTAG pin headers to pads
- Change values for inrush limiting circuitry
- Change FPGA driven MOSFETs to lower V<sub>th</sub>
- Change FPGA pin-out mapping
- Change power stack connector I/O
- Change encoder input signal chain
- Change Ethernet routing to correct diff. impedance
- Fix footprints

REV E: design finalized 2021-03-25

- Remove isoSPI
- Add shared UART and JTAG interface
- Add more GPIO ports
- Add mechanical parts to BOM
- Add website to PCB silkscreen
- Add reset signal pull-up and ESD protection
- Add local decoupling to VREF
- Add local decoupling to 2.048V
- Add E-STOP logic signal to FPGA
- Add PTC resettable fuses to PWM outputs
- Add VDRIVE signal to PS interface
- Add jumpers for default VDRIVE and ESTOP
- Add pull-down to VCCIO\_EN
- Change power wiring in schematics
- Change shield termination to VIN-
- Change mounting holes to VIN- from GND
- Change DB15 P/N to include screw posts
- Change to USB type B receptacle
- Update top-level block diagram
- Fix 24V supply to GPIO port
- Fix power protection circuitry
- Fix board start-up PWM issues
- Fix P/N for RC filter caps
- Fix BOM components for DFM
- Fix footprints

REV F: design finalized 2023-10-05

- Add termination on GPIO differential inputs
- Update pull-down resistor value for boot-up PWM output protection
- Update P/Ns and footprints for manufacturability

See [www.github.com/Severson-Group/AMDC-Hardware/issues](http://www.github.com/Severson-Group/AMDC-Hardware/issues) for more discussion on design changes

Title: <b>Revision Changes</b>		Sheet: 23 of 23
File: RevisionChanges.SchDoc	Time: 8:23:43 PM	
Revision: F	Date: 10/5/2023	Engineer: Nathan Petersen

