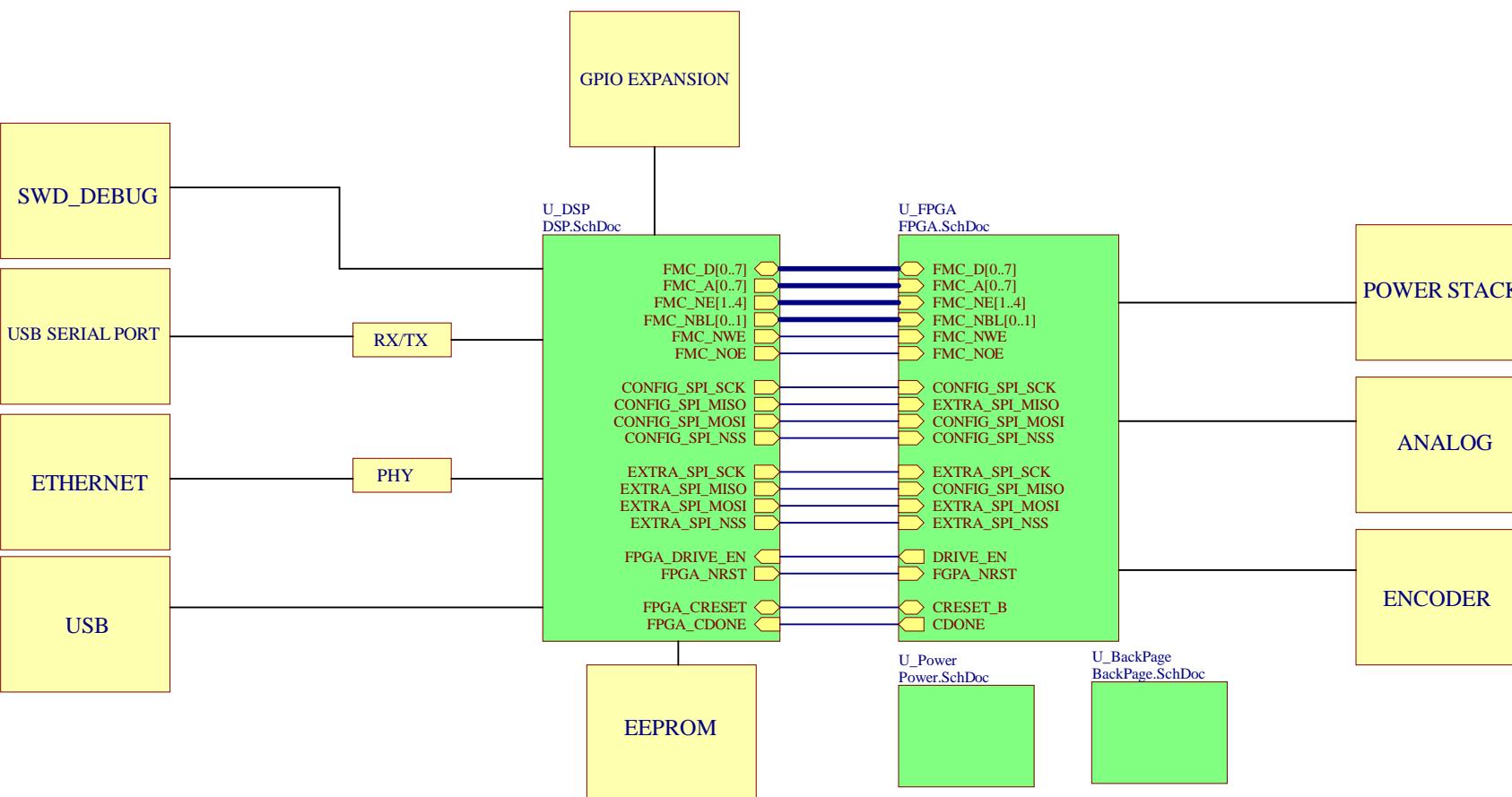


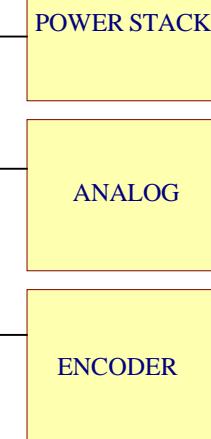
A

A



B

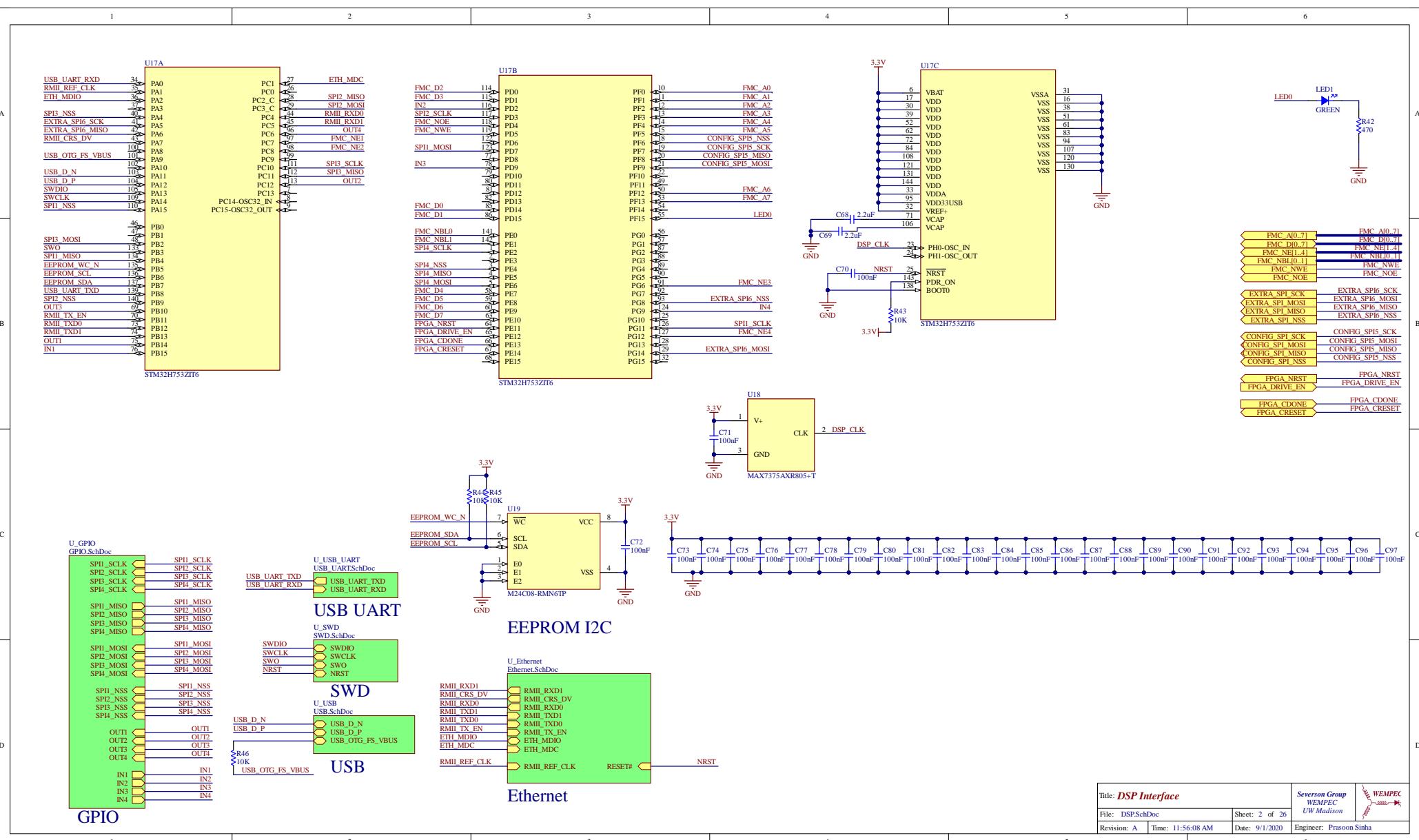
B

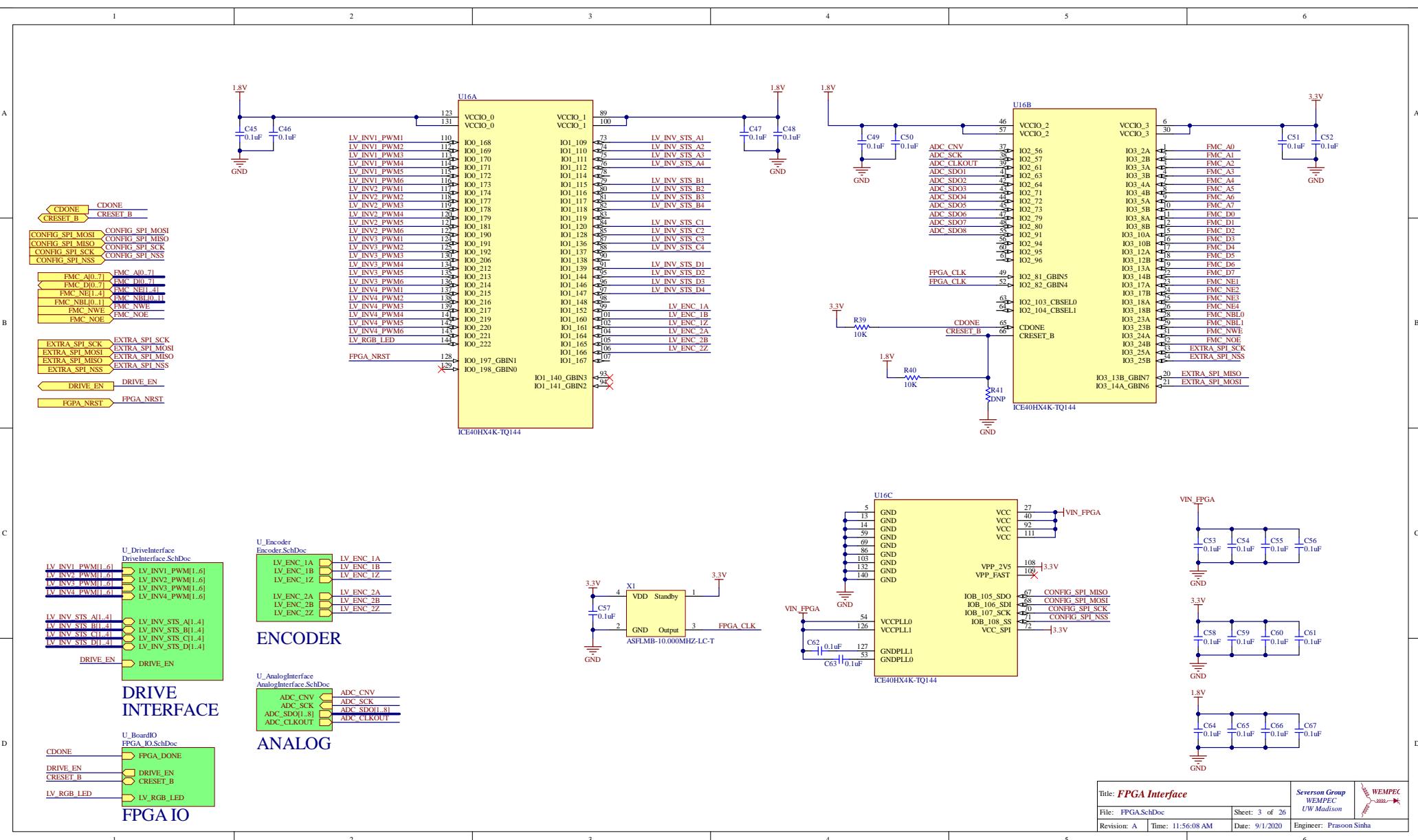


C

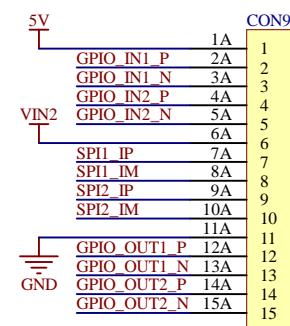
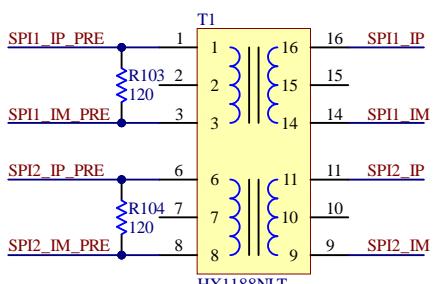
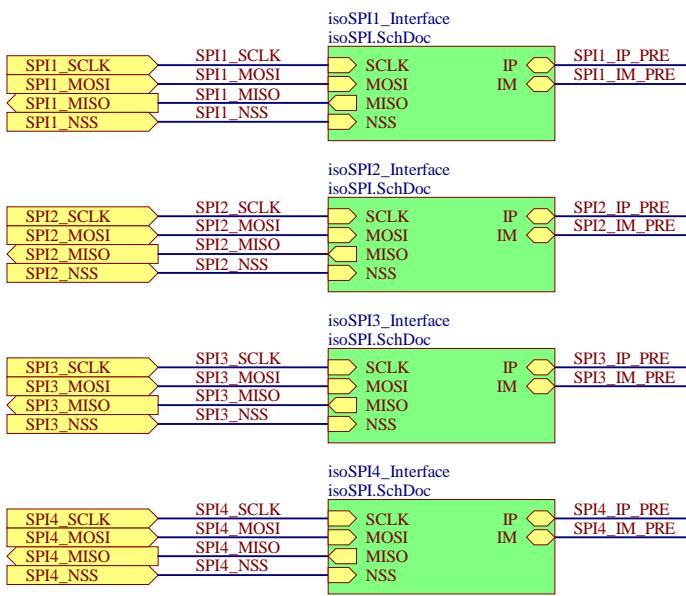
C

Title: uAMDC			Severson Group WEMPEC UWMadison
File: uAMDC.SchDoc	Sheet: 1 of 26		
Revision: A	Time: 11:56:07 AM	Date: 9/1/2020	
Engineer: Prasoon Sinha			

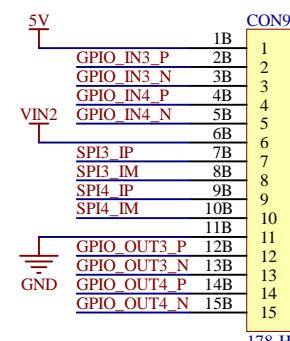
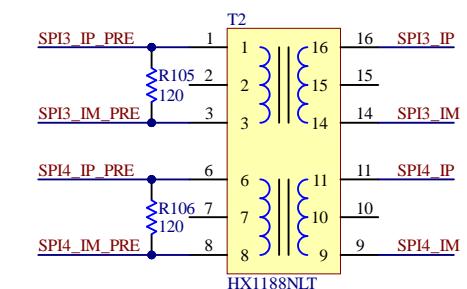
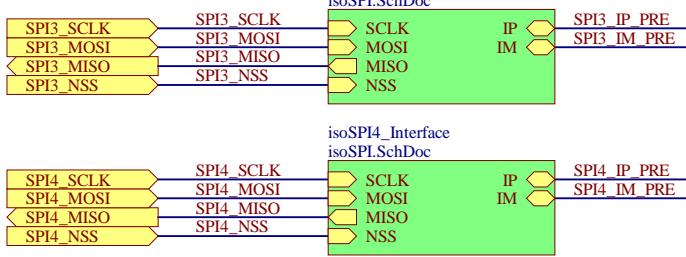




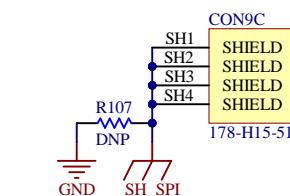
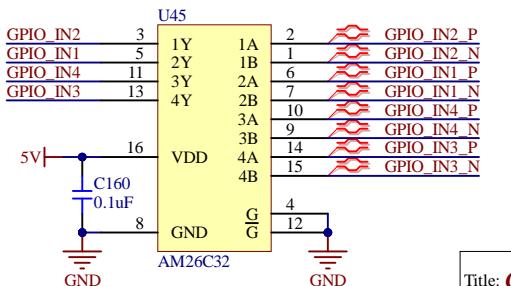
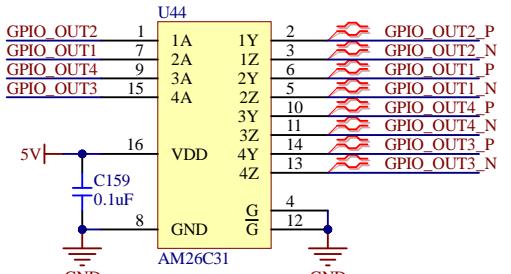
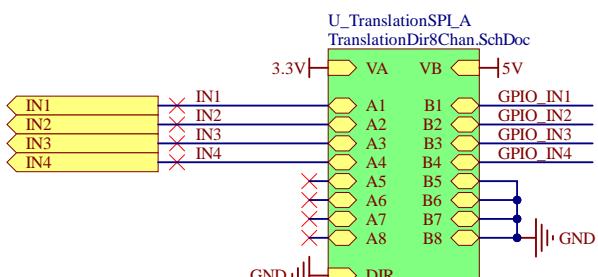
A



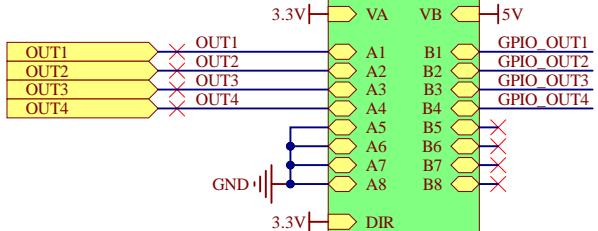
B



C



D



A

A

B

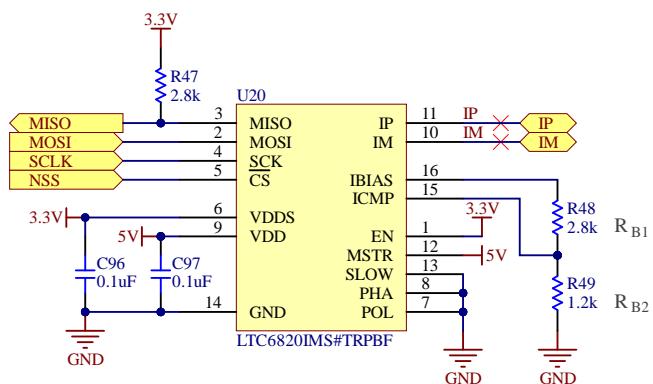
B

C

C

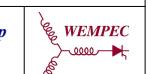
D

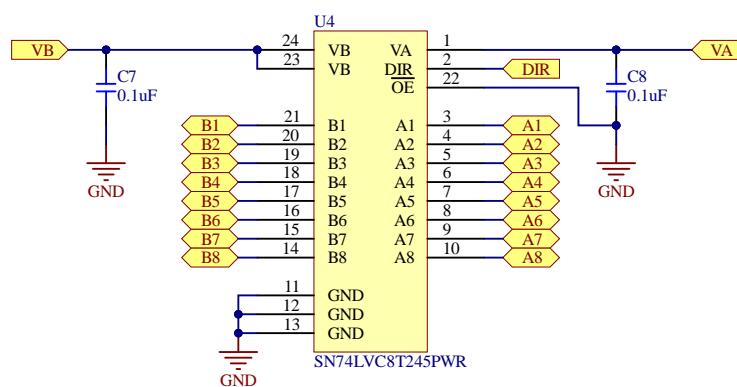
D

Title: *isoSPI Interface*

File: isoSPI.SchDoc Sheet: 5 of 26

Revision: A Time: 11:56:08 AM Date: 9/1/2020

Severson Group
WEMPEC
UWMadison

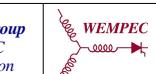


Title: **8-Channel Directional Translation**

File: **TranslationDir8Chan.SchDoc** Sheet: **6 of 26**

Revision: **A** Time: **11:56:08 AM** Date: **9/1/2020**

Severson Group
WEMPEC
UWMadison



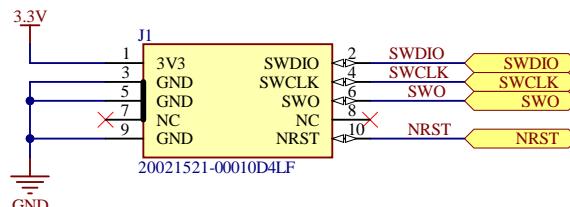
Engineer: Nathan Petersen

A

B

C

D



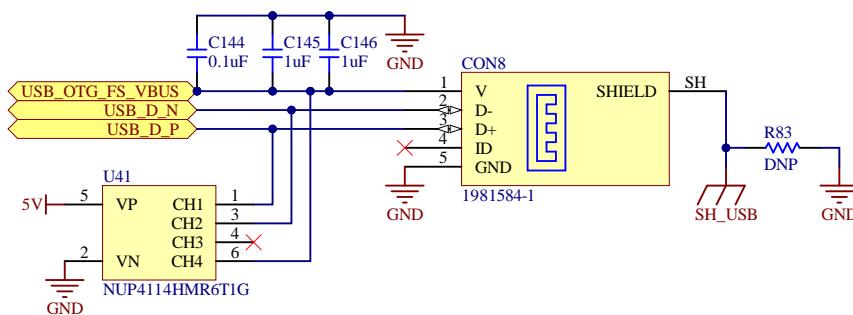
Title: SWD			Severson Group WEMPEC UWMadison
File: SWD.SchDoc		Sheet: 7 of 26	
Revision: A	Time: 11:56:08 AM	Date: 9/1/2020	Engineer: Prasoon Sinha

A

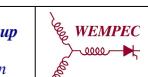
B

C

D

Title: **USB**File: **USB.SchDoc**Sheet: **8 of 26**Revision: **A** Time: **11:56:08 AM**Date: **9/1/2020**

Severson Group
WEMPEC
UWMadison

Engineer: **Prasoon Sinha**

A

A

B

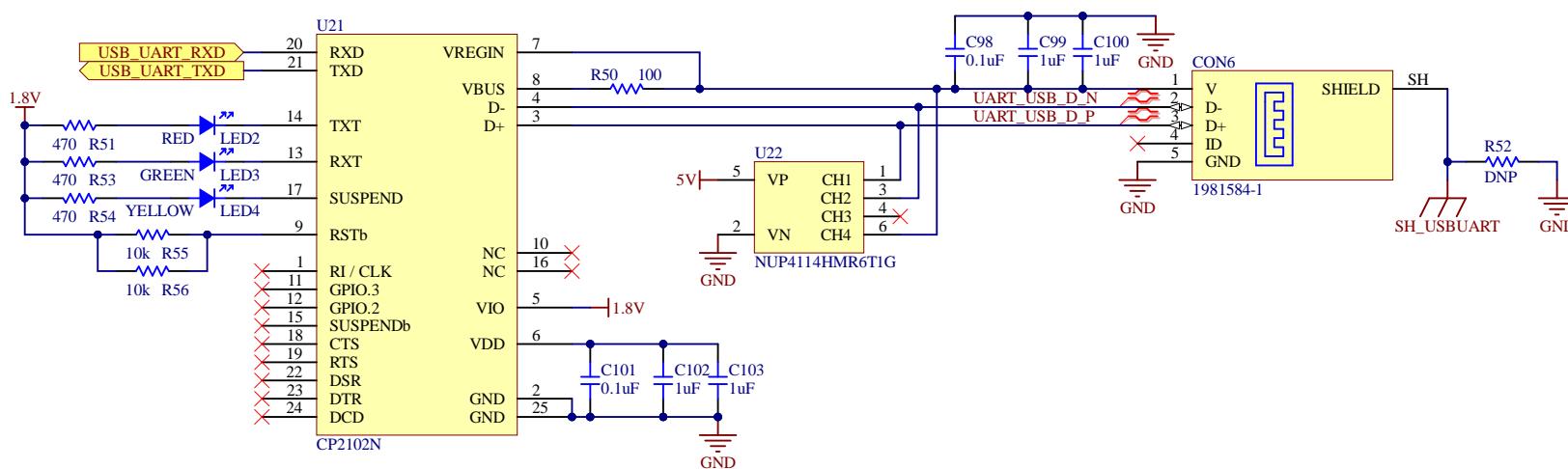
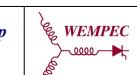
B

C

C

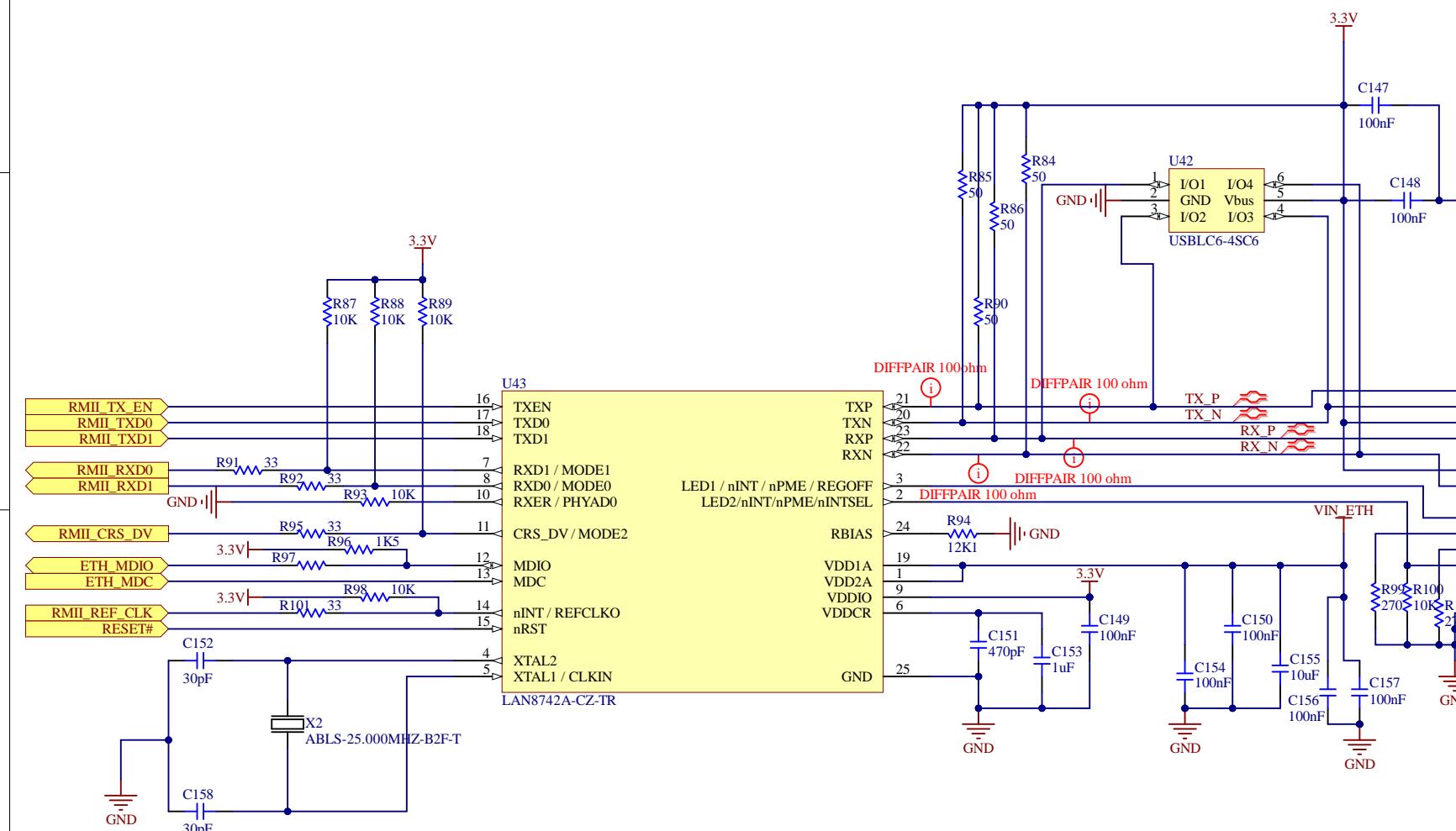
D

D

Title: **USB UART**File: **USB_UART.SchDoc**Sheet: **9 of 26**Revision: **A** Time: **11:56:08 AM**Date: **9/1/2020**
Severson Group
WEMPEC
UWMadison


A

A



B

B

C

C

D

D

Title: *Ethernet*

File: Ethernet.SchDoc

Sheet: 10 of 26

Revision: A Time: 11:56:08 AM

Date: 9/1/2020

Severson Group
WEMPEC
UWMadison

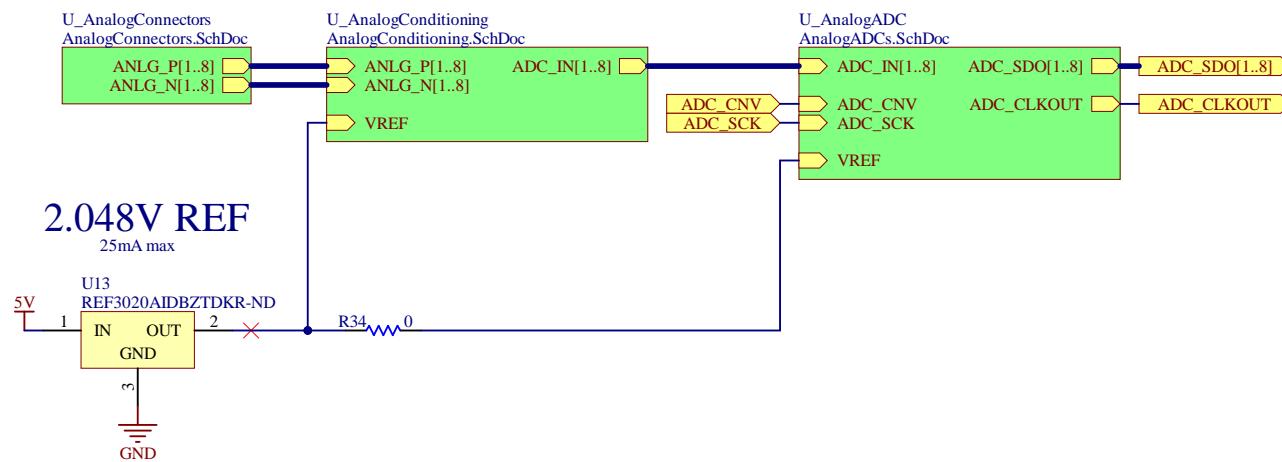


A

A

B

B



C

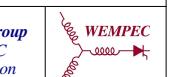
C

D

D

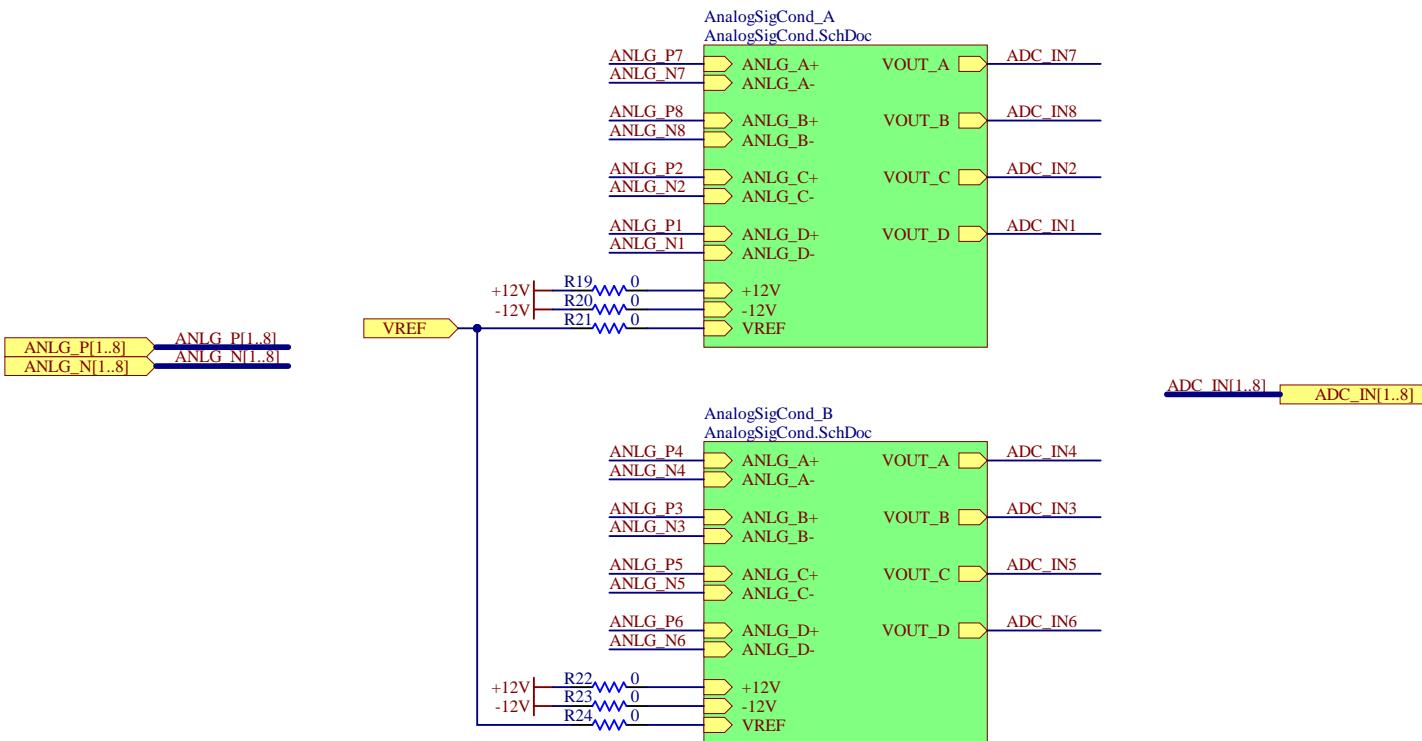
Title: **Analog Interface**File: **AnalogInterface.SchDoc**Sheet: **11 of 26**Revision: **A** Time: **11:56:09 AM**Date: **9/1/2020**

Severson Group
WEMPEC
UWMadison



A

A



B

B

C

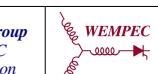
C

D

D

Title: **Analog Signal Conditioning**File: **AnalogConditioning.SchDoc** Sheet: **13 of 26**Revision: **A** Time: **11:56:09 AM** Date: **9/1/2020**

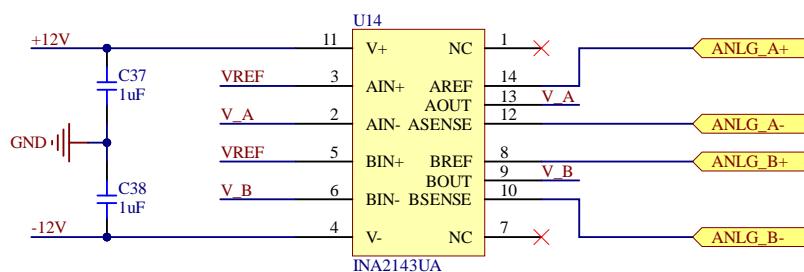
Severson Group
WEMPEC
UWMadison



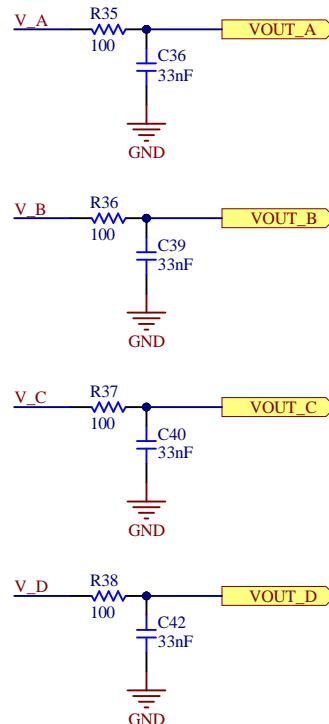
Engineer: Nathan Petersen

A

A

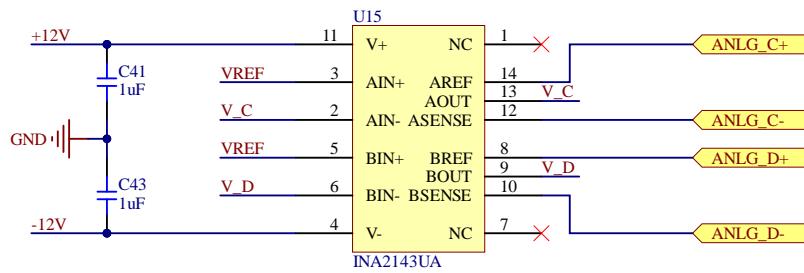


△ LPF: fc = 50kHz



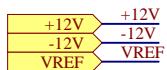
B

B



C

C



Title: **Analog Signal Front-End**

File: **AnalogSigCond.SchDoc**

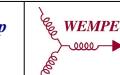
Sheet: **14 of 26**

Revision: **A**

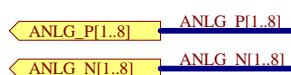
Time: **11:56:09 AM**

Date: **9/1/2020**

Severson Group
WEMPEC
UWMadison

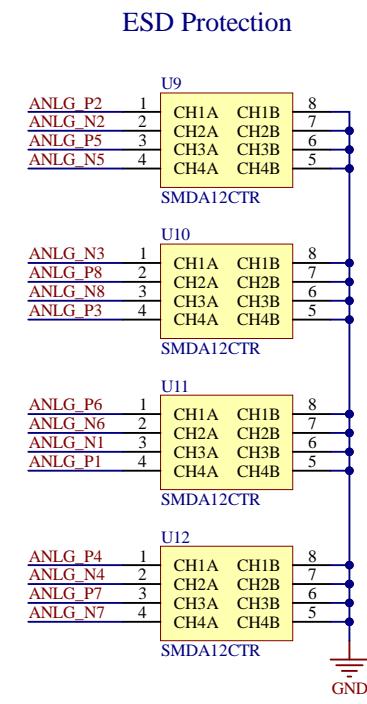


A

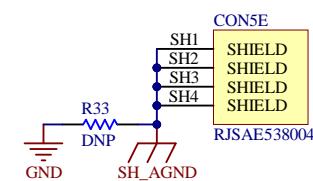
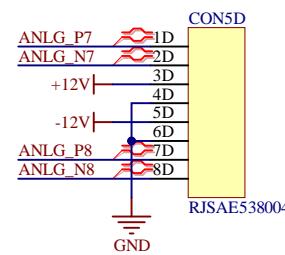
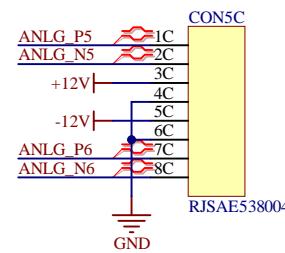
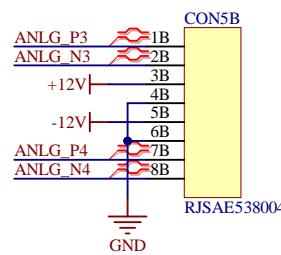
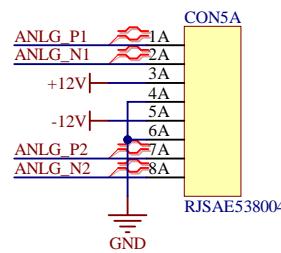


A

B



B



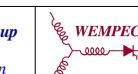
Force no input to 0V

ANLG_P1	R25 100k	ANLG_N1
ANLG_P2	R26 100k	ANLG_N2
ANLG_P3	R27 100k	ANLG_N3
ANLG_P4	R28 100k	ANLG_N4
ANLG_P5	R29 100k	ANLG_N5
ANLG_P6	R30 100k	ANLG_N6
ANLG_P7	R31 100k	ANLG_N7
ANLG_P8	R32 100k	ANLG_N8

C

Title: **Analog RJ45 Connectors**

Severson Group
WEMPEC
UWMadison

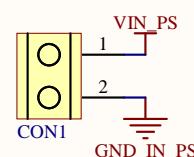
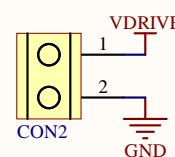


File: AnalogConnectors.SchDoc | Sheet: 15 of 26

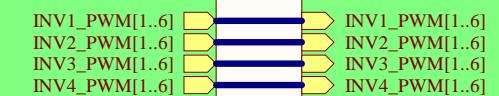
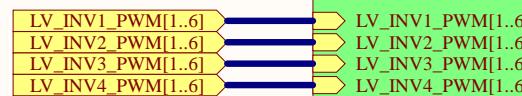
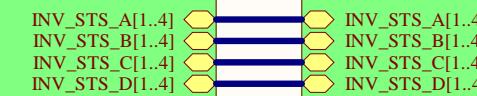
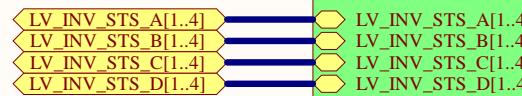
Revision: A | Time: 11:56:09 AM | Date: 9/1/2020

Engineer: Nathan Petersen

A

POWERSTACK VIN**VDRIVE**

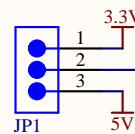
B

**U_InverterTranslation
InverterTranslation.SchDoc****U_InverterConnectors
InverterConnectors.SchDoc**

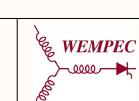
DRIVE_EN

VDDPS

C

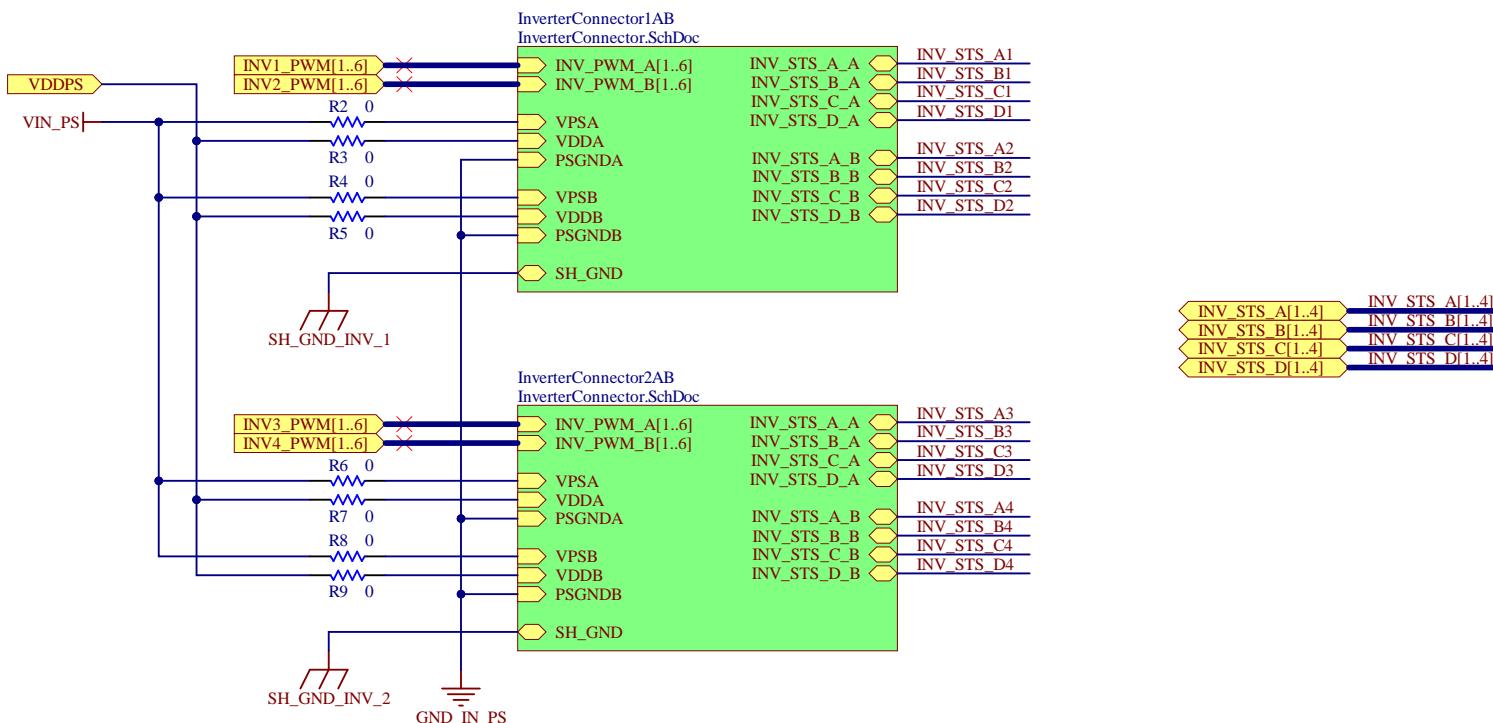


D

Title: **DriveInterface**File: **DriveInterface.SchDoc**Sheet: **16 of 26**Revision: **A** Time: **11:56:09 AM**Date: **9/1/2020****Severson Group
WEMPEC
UW Madison**

A

A



B

B

C

C

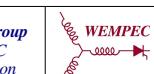
D

D

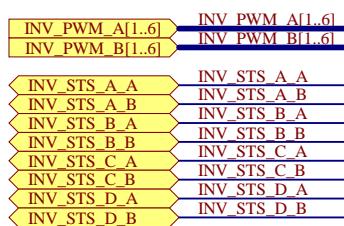
Title: **Inverter Connectors**

File: InverterConnectors.SchDoc | Sheet: 17 of 26

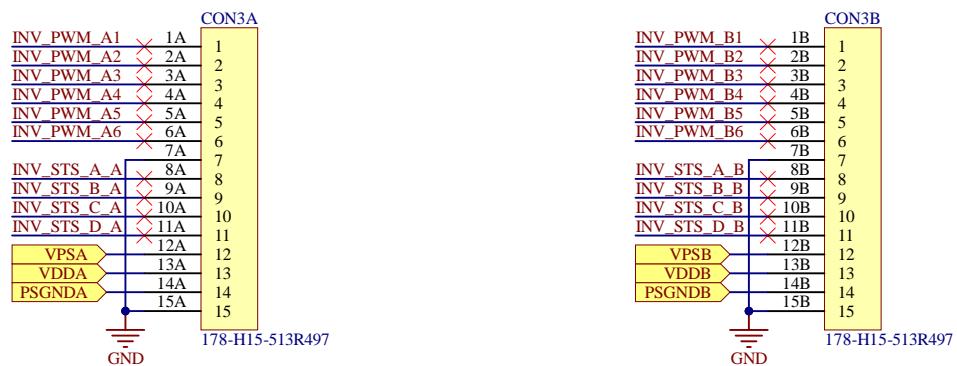
Revision: A | Time: 11:56:09 AM | Date: 9/1/2020

Severson Group
WEMPEC
UWMadison

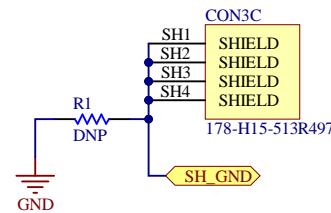
A



B



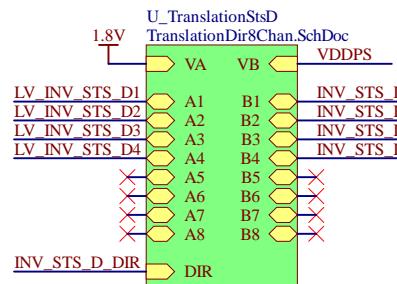
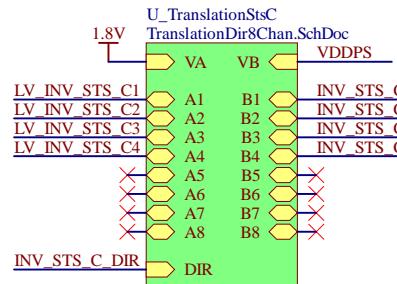
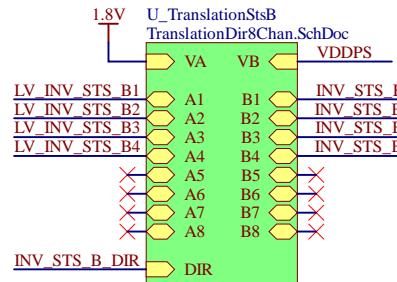
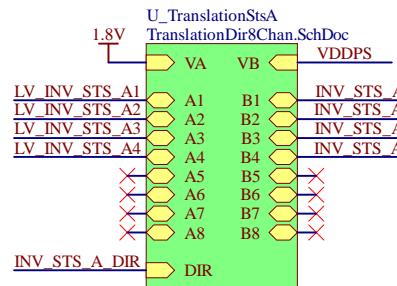
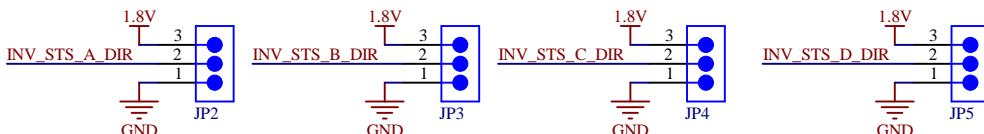
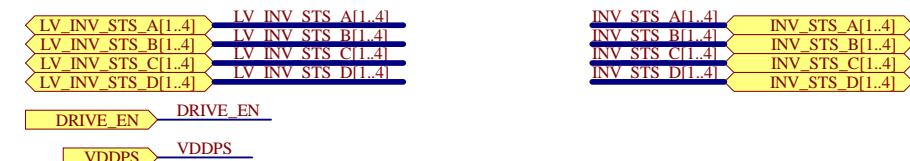
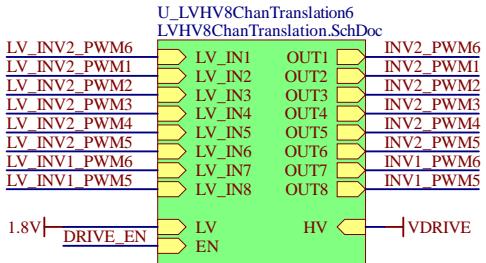
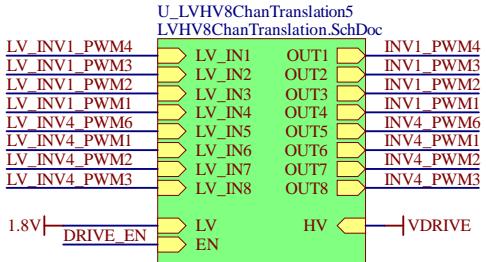
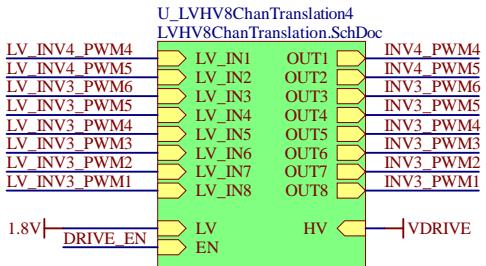
C



D

Title: Inverter Connector		Severson Group WEMPEC UWMadison
File: InverterConnector.SchDoc	Sheet: 18 of 26	
Revision: A	Time: 11:56:09 AM	
Date: 9/1/2020		Engineer: Nathan Petersen

A

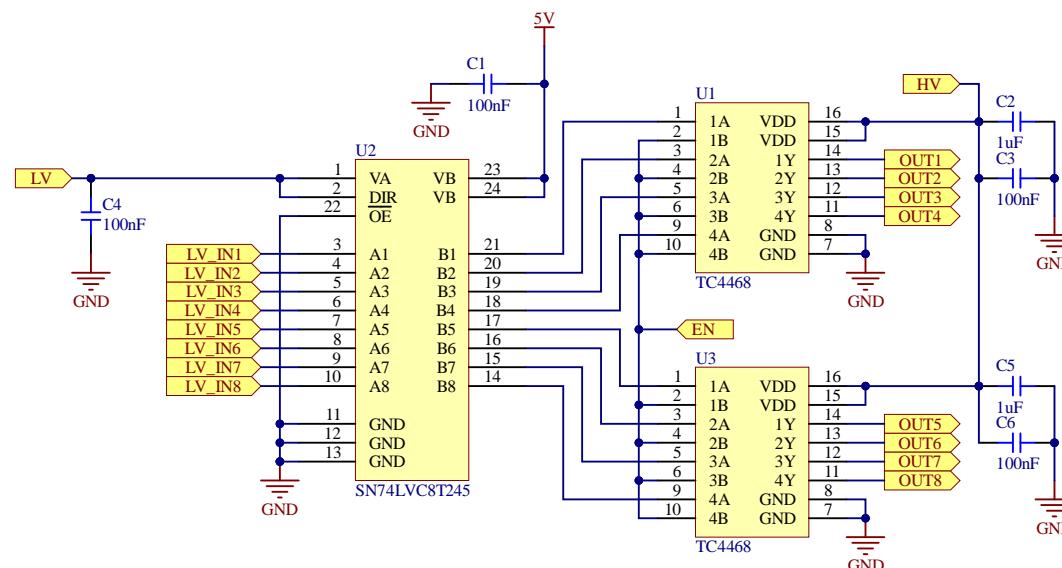


A

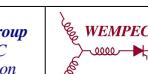
B

C

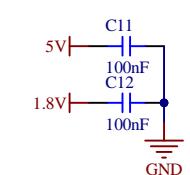
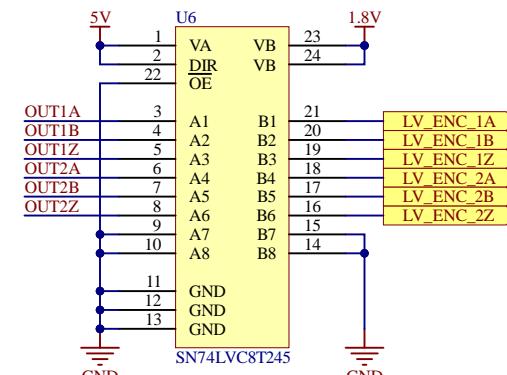
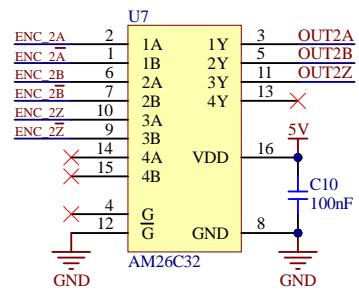
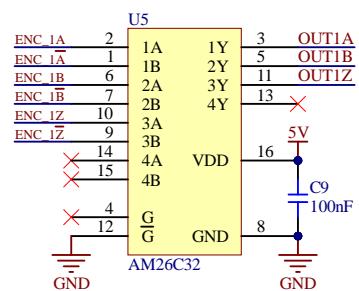
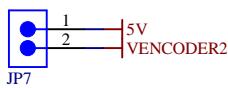
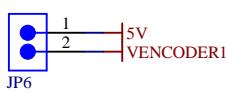
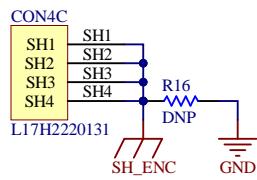
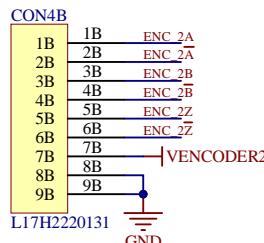
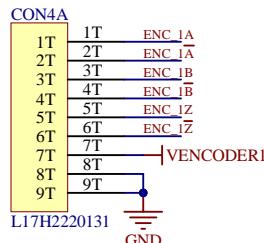
D

Title: **8-channel LV to HV Translation**File: **LVHV8ChanTranslation.SchDoc** | Sheet: **20 of 26**Revision: **A** | Time: **11:56:09 AM** | Date: **9/1/2020**

Severson Group
WEMPEC
UWMadison

Engineer: **Prasoon Sinha**

A



Title: Encoders			Severson Group WEMPEC UWMadison	
File: Encoder.SchDoc				
Sheet: 21 of 26				
Revision: A	Time: 11:56:09 AM	Date: 9/1/2020	Engineer: Nathan Petersen	

A

B

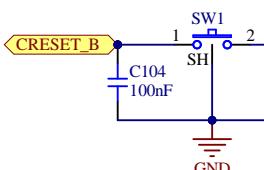
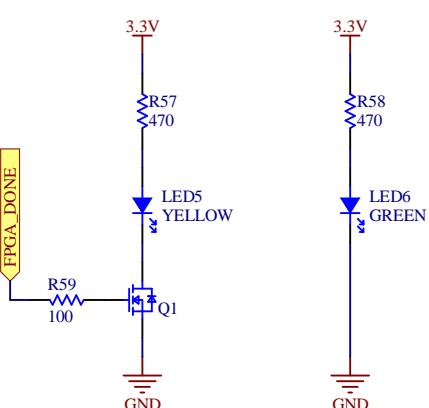
C

D

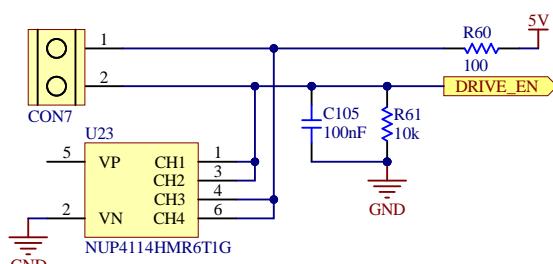
FPGA STATUS LEDS

RESET BUTTON

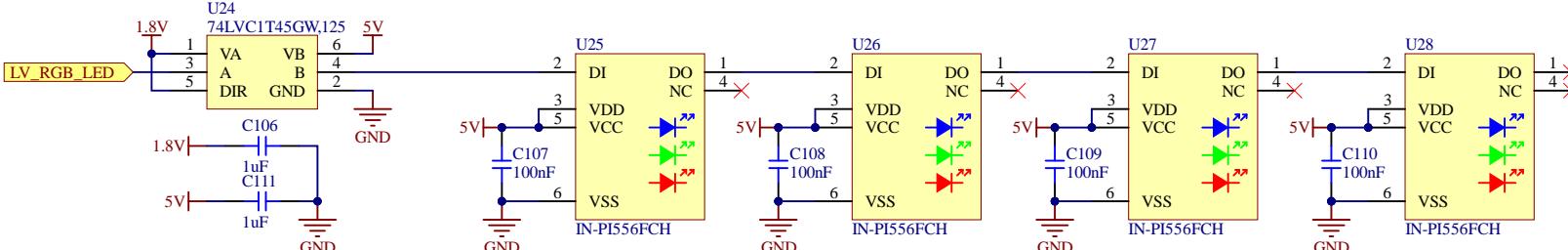
FPGA DONE



DRIVE ENABLE (ESTOP)

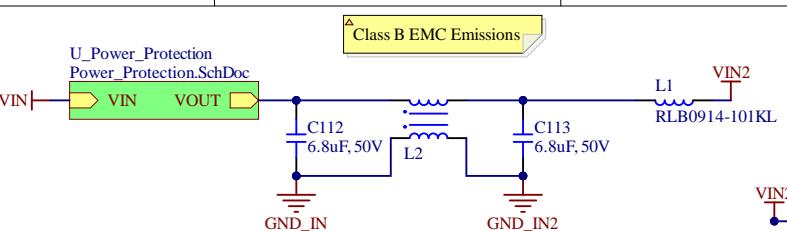
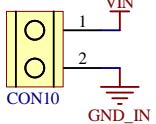
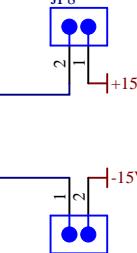
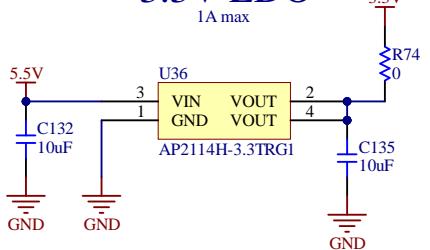
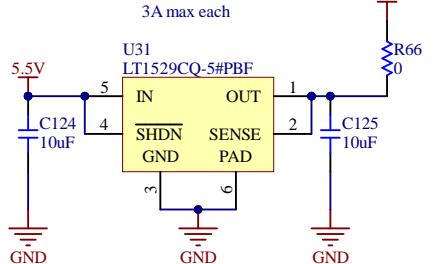
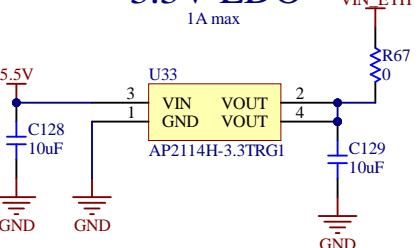
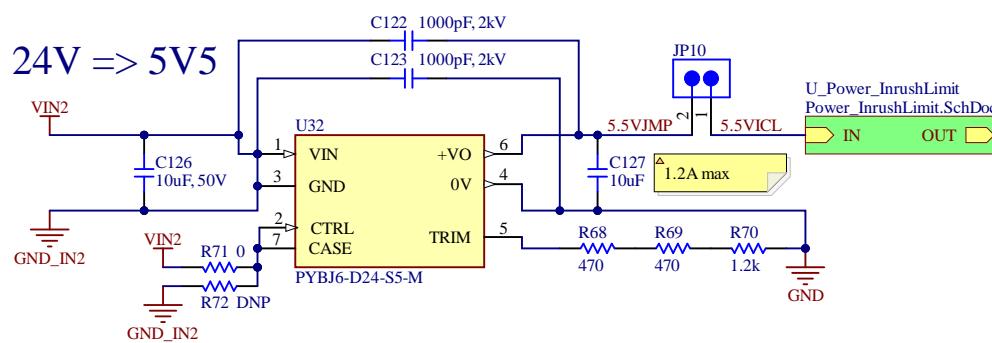
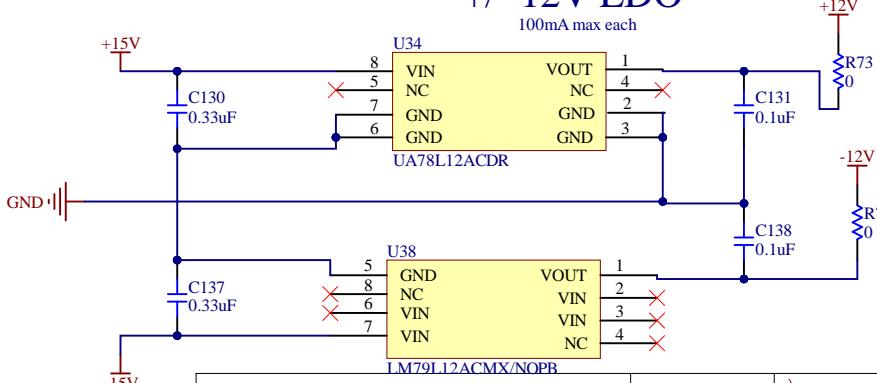
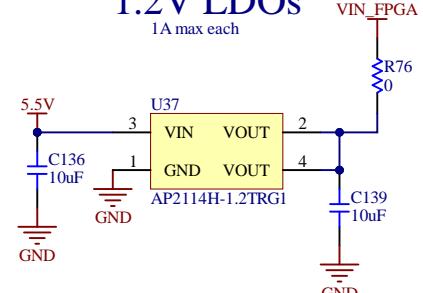
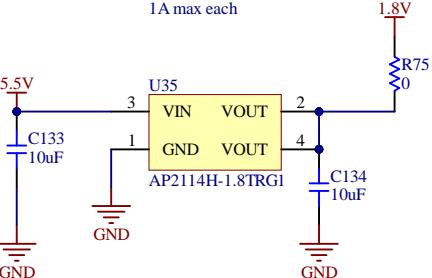


FPGA RGB LEDS



Title: FPGA I/O Interface			<i>Severson Group</i> WEMPEC UWMadison	
File: FPGA_IO.SchDoc		Sheet: 22 of 26		
Revision: A	Time: 11:56:09 AM	Date: 9/1/2020	Engineer:	Prasoon Sinha

VIN (assumed 24V DC)


 $24V \Rightarrow +15V$
 $24V \Rightarrow -15V$
**3.3V LDO****5V LDOs****3.3V LDO** $24V \Rightarrow 5V5$ **+/- 12V LDO****1.2V LDOs****1.8V LDOs**

Title: Power		Severson Group WEMPEC UWMadison
File: Power.SchDoc	Sheet: 23 of 26	WEMPEC
Revision: A	Time: 11:56:09 AM	Date: 9/1/2020
Engineer: Prasoon Sinha		

A

A

B

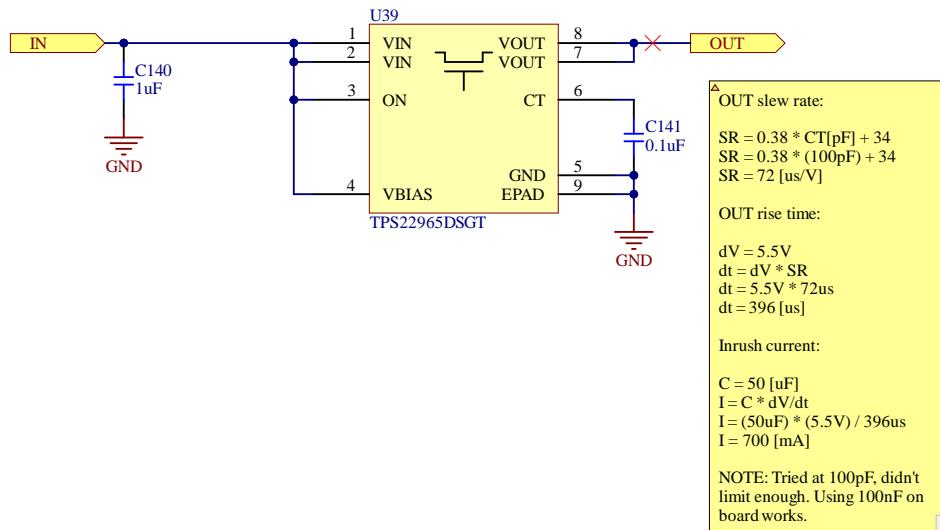
B

C

C

D

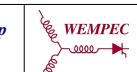
D

Title: **Inrush Current Limiter**

File: Power_InrushLimit.SchDoc | Sheet: 24 of 26

Revision: A | Time: 11:56:10 AM | Date: 9/1/2020 | Engineer: Nathan Petersen

Severson Group
WEMPEC
UWMadison



A

A

B

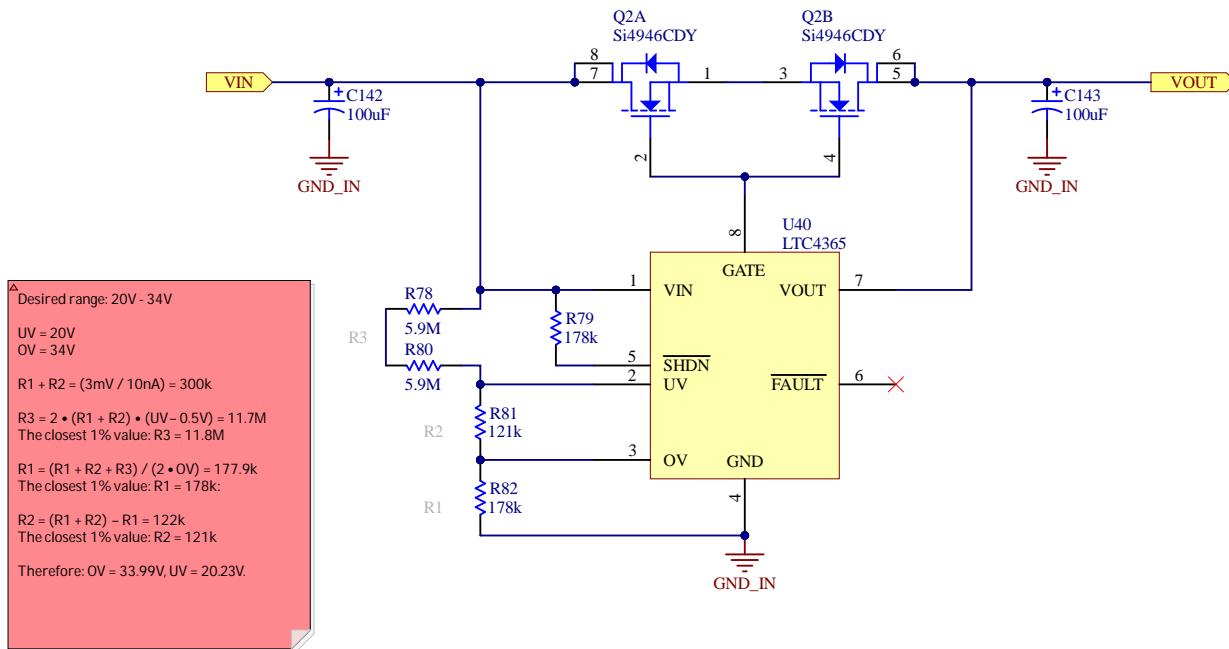
B

C

C

D

D



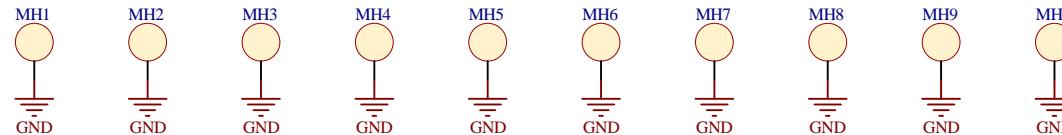
Title: Power Protection			<i>Severson Group WEMPEC UW Madison</i>	
File: Power_Protection.SchDoc		Sheet: 25 of 26		
Revision: A	Time: 11:56:10 AM	Date: 9/1/2020	Engineer: Nathan Petersen	

4-40 Screws:

SCREW1 SCREW2 SCREW3 SCREW4 SCREW5 SCREW6 SCREW7 SCREW8 SCREW9 SCREW10

4-40 Standoffs:

STANDOFF1 STANDOFF2 STANDOFF3 STANDOFF4 STANDOFF5 STANDOFF6 STANDOFF7 STANDOFF8 STANDOFF9 STANDOFF10

Mouting Holes:

Title: ***Back Page***

File: **BackPage.SchDoc**

Revision: **A**

Sheet: **26 of 26**

Date: **9/1/2020**

Severson Group
WEMPEC
UWMadison

