

RGB LED, 4x switches, 1x button, E-STOP



BOARD I/O

24 channels
5V/3.3V
I/O



GPIO

16 channels
+/-10V diff.
pair inputs



ANALOG INPUTS

48 channels
(8 full
inverters)



DRIVE OUTPUTS

Quadrature
input (A,B,Z)



ENCODER

PicoZed

7030

U_PicoZed
PicoZed.SchDoc

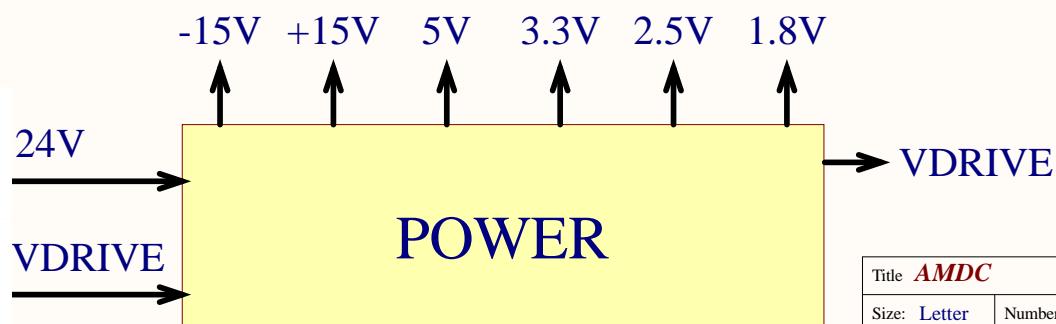
JTAG

ETHERNET

USB OTG

USB UART

Power inputs
to board

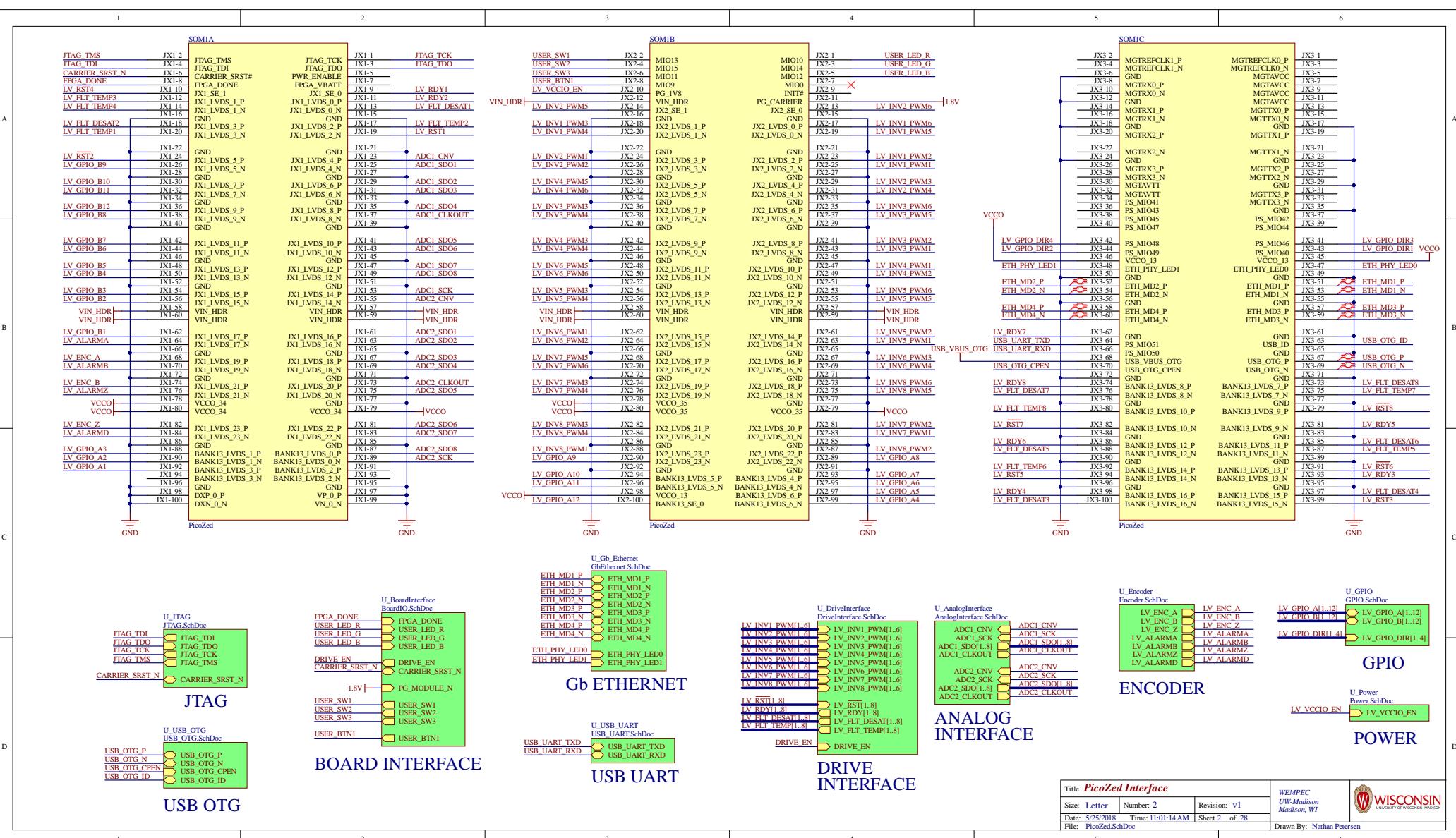


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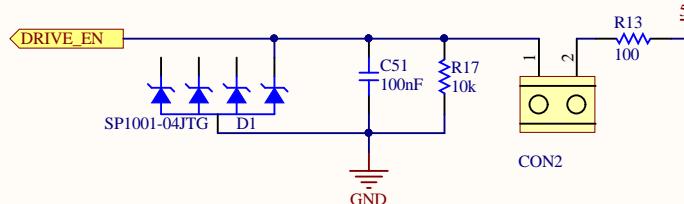
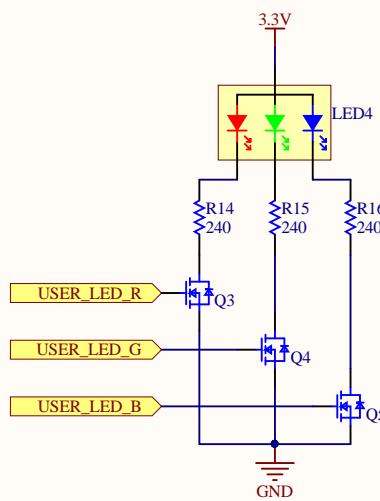
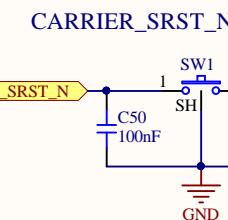
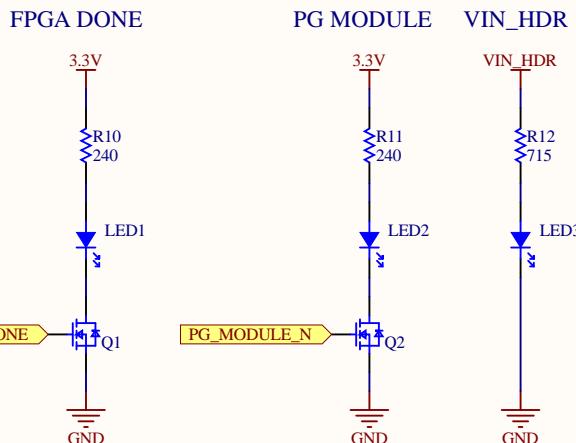
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Date: 5/25/2018	Time: 11:01:13 AM	Sheet 1 of 28
File: AMDC.SchDoc		Drawn By: Nathan Petersen

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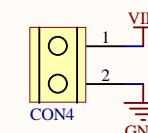
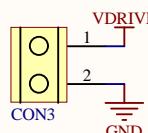
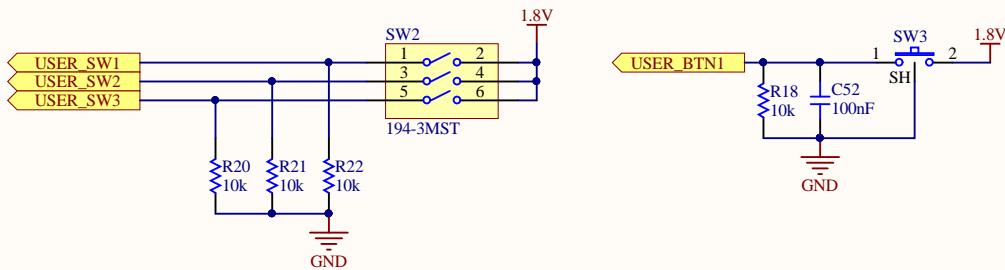




STATUS LEDS



USER INPUT



Title Board I/O			<i>WEMPEC</i> <i>UW-Madison</i> <i>Madison, WI</i>	 WISCONSIN <small>UNIVERSITY OF WISCONSIN-MADISON</small>
Size: Letter	Number: 3	Revision: v1		
Date: 5/25/2018	Time: 11:01:14 AM	Sheet 3 of 28	Drawn By:	Nathan Petersen
File: BoardIIO.SchDoc				

A

A

B

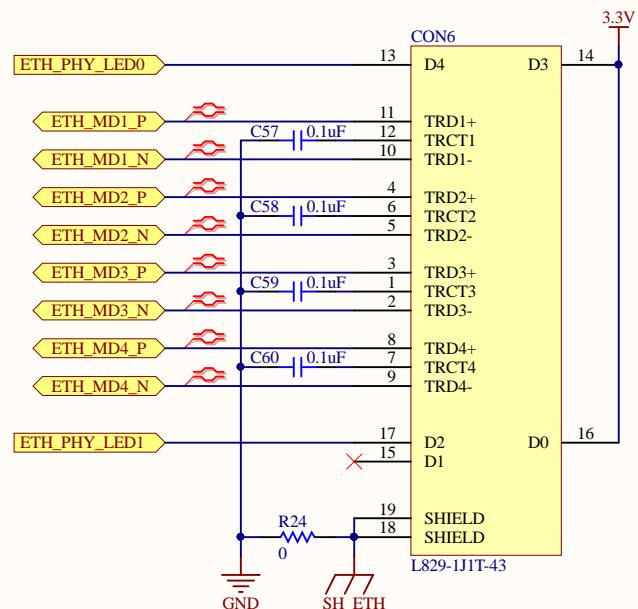
B

C

C

D

D



Title ***SoM Gb Ethernet***

Size: Letter	Number: 4	Revision: v1
Date: 5/25/2018	Time: 11:01:15 AM	Sheet 4 of 28
File: GbEthernet.SchDoc		Drawn By: Nathan Petersen

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A

A

B

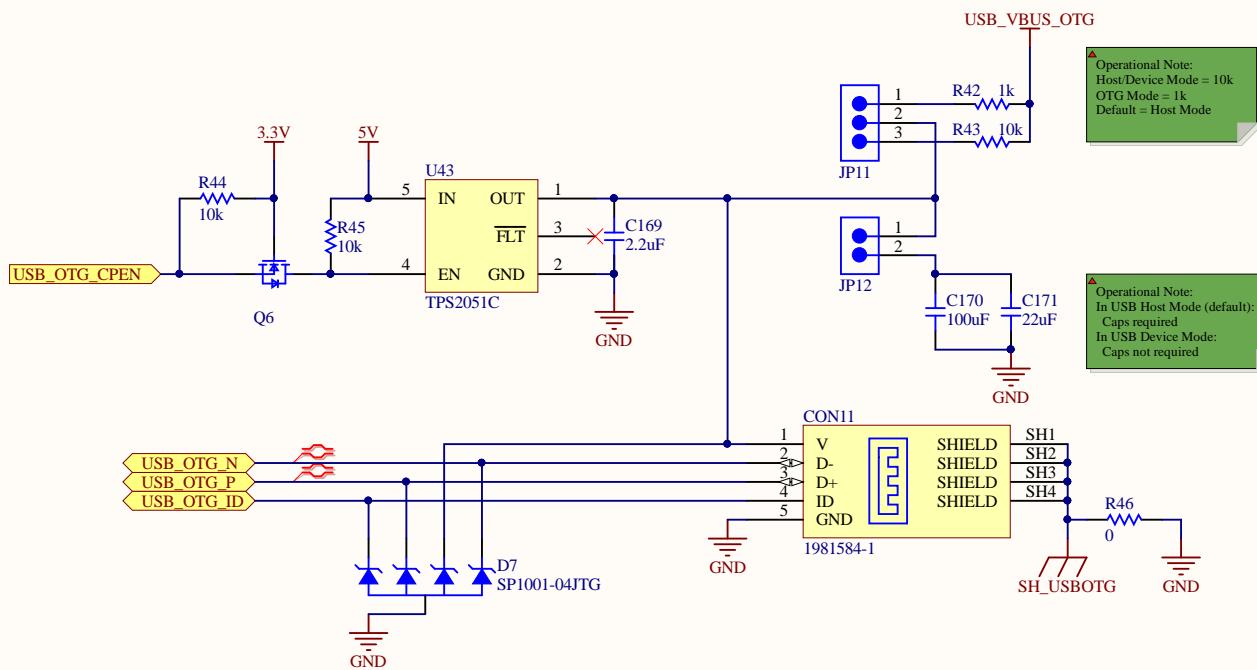
B

C

C

D

D


Title *USB OTG*

Size: Letter	Number: 5	Revision: v1
Date: 5/25/2018	Time: 11:01:15 AM	Sheet 5 of 28
File: USB_OTG.SchDoc		Drawn By: Nathan Petersen

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A

A

B

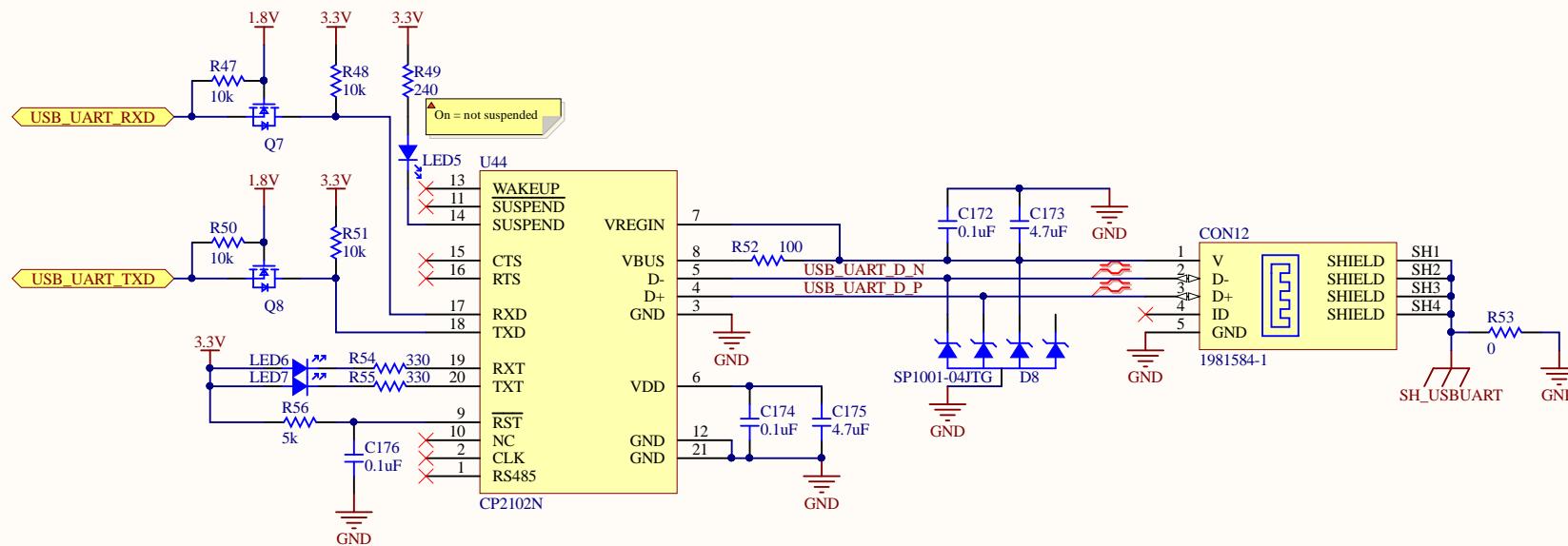
B

C

C

D

D

Title **USB UART**

Size: Letter Number: 6 Revision: v1

Date: 5/25/2018 Time: 11:01:15 AM Sheet 6 of 28

File: USB_UART.SchDoc

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Drawn By: Nathan Petersen

A

A

B

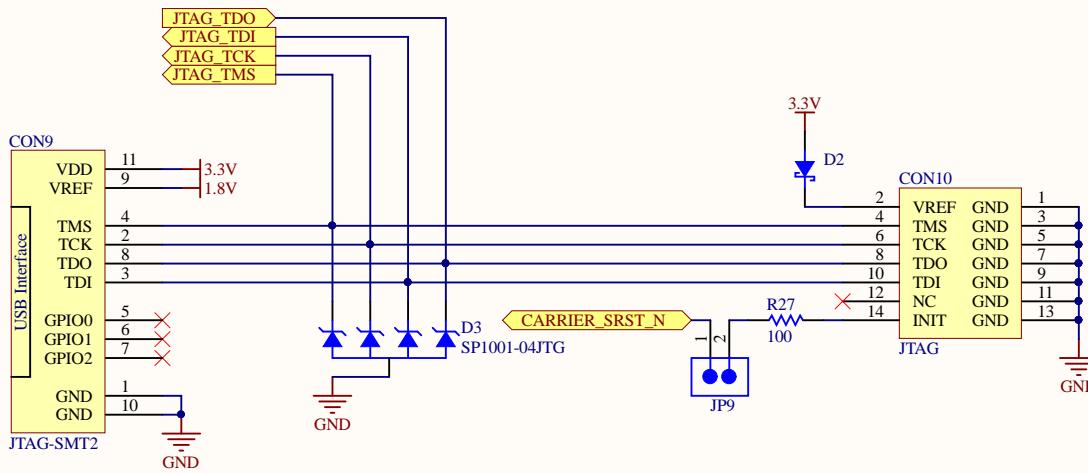
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C

C

D

D



Title JTAG			WEMPEC UW-Madison Madison, WI
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Date: 5/25/2018	Time: 11:01:15 AM	Sheet 7 of 28	
File: JTAG.SchDoc	Drawn By: Nathan Petersen		

A

A

B

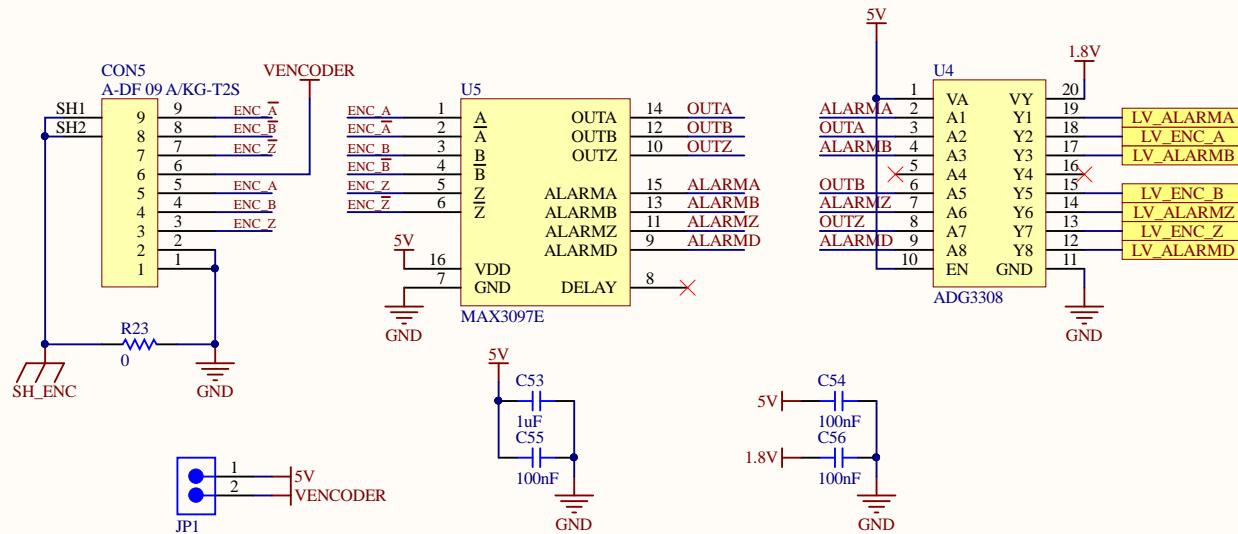
B

C

C

D

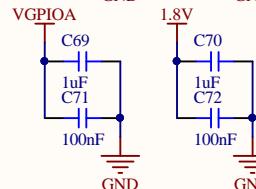
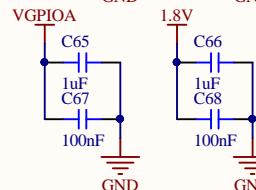
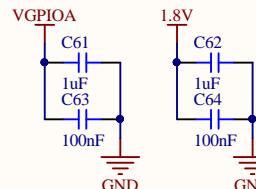
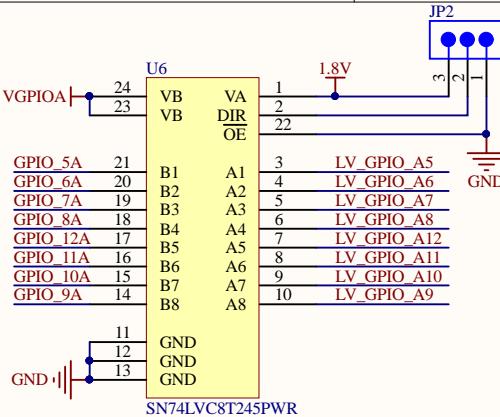
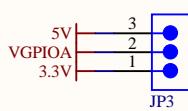
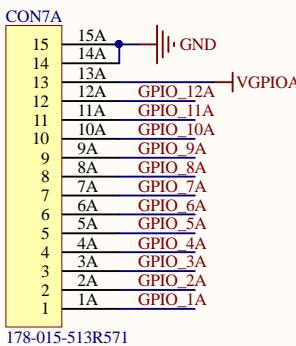
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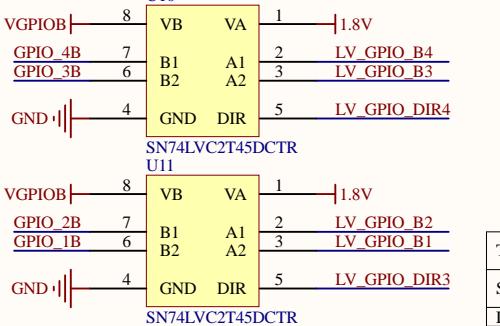
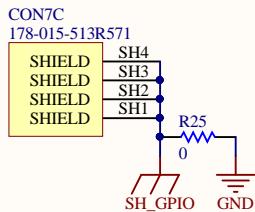
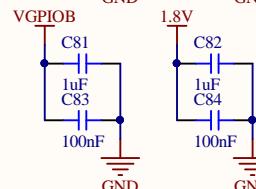
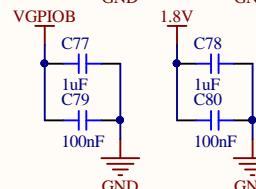
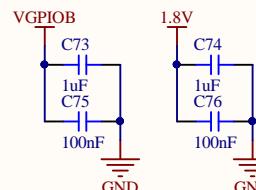
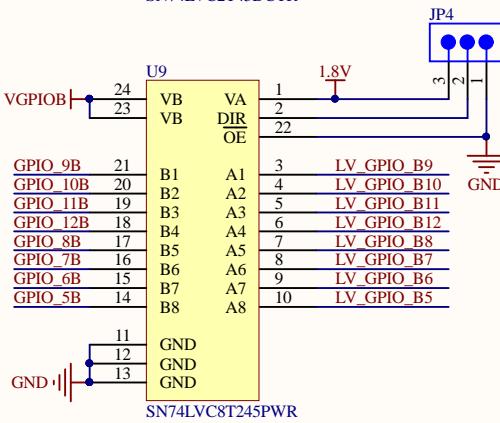
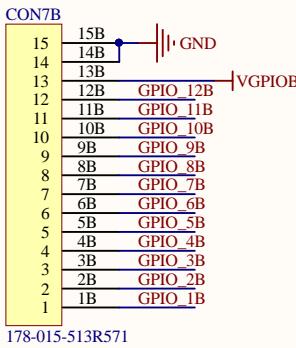
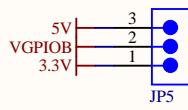
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Date: 5/25/2018	Time: 11:01:15 AM	Sheet 8 of 28
File: Encoder.SchDoc		Drawn By: Nathan Petersen



A



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 LV_GPIO_A[1..12] LV_GPIO_A[1..12]
 LV_GPIO_B[1..12] LV_GPIO_B[1..12]



Title **GPIO**

Size: Letter Number: 9 Revision: v1
 Date: 5/25/2018 Time: 11:01:15 AM Sheet 9 of 28
 File: GPIO.SchDoc

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A

A

B

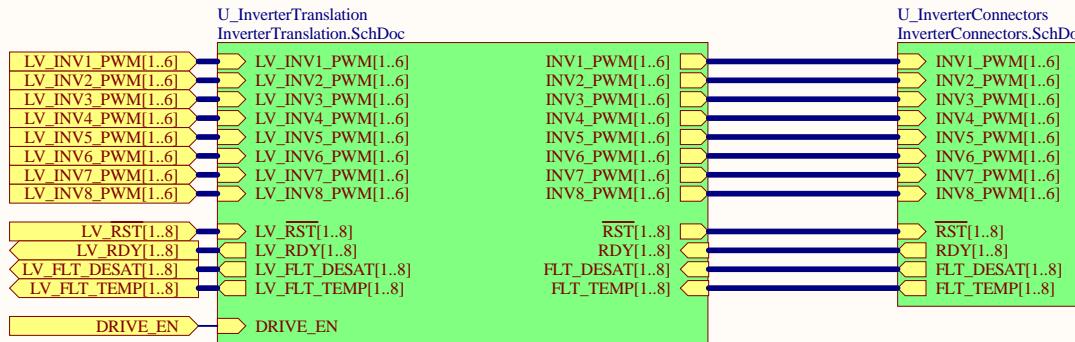
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C

C

D

D



Title Drive Interface		
Size: Letter	Number: 10	Revision: v1
Date: 5/25/2018	Time: 11:01:15 AM	Sheet 10 of 28
File: DriveInterface.SchDoc		
Drawn By: Nathan Petersen		

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1

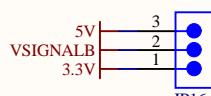
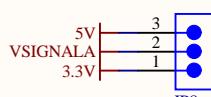
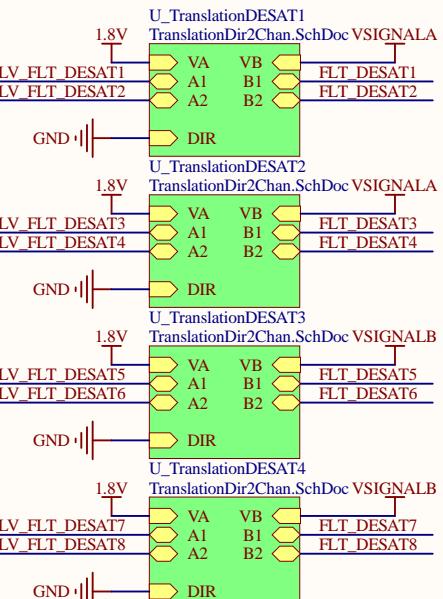
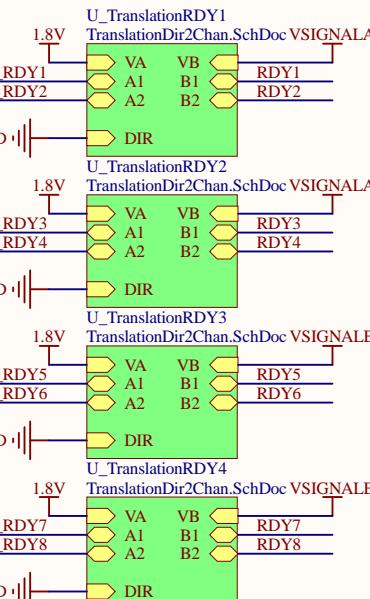
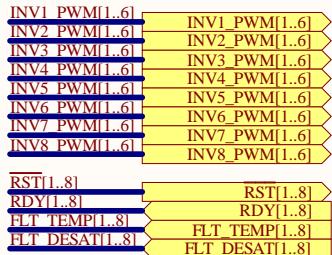
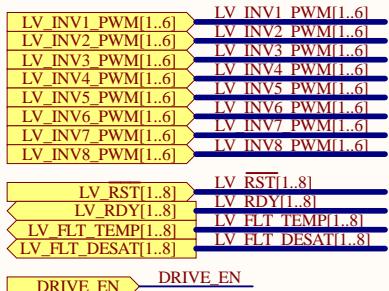
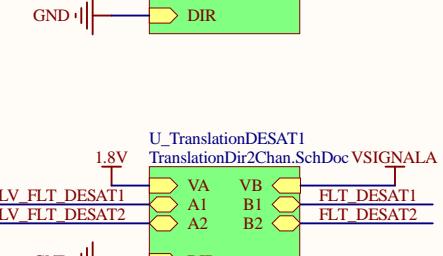
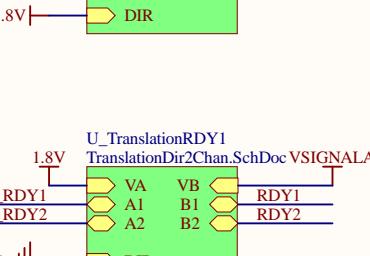
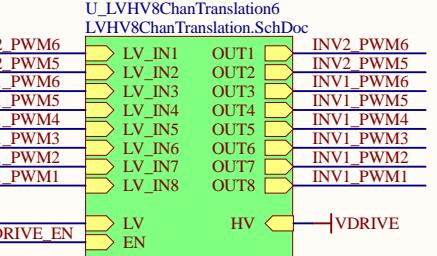
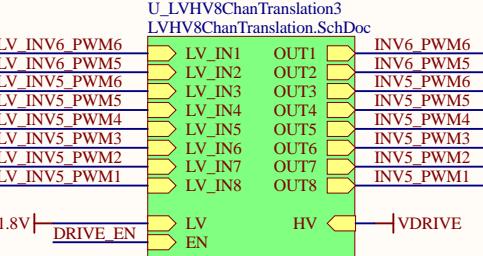
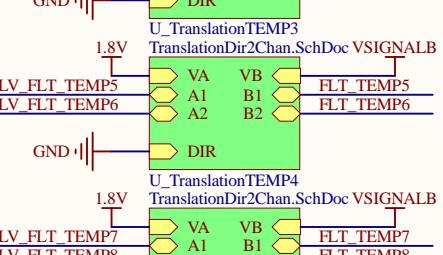
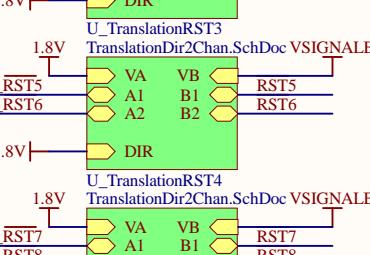
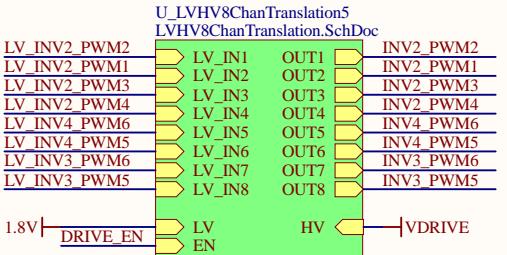
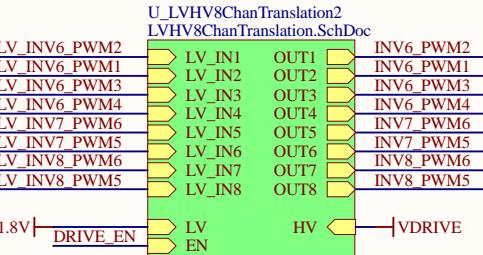
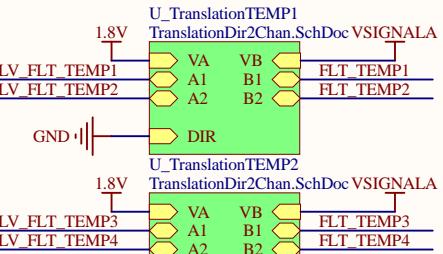
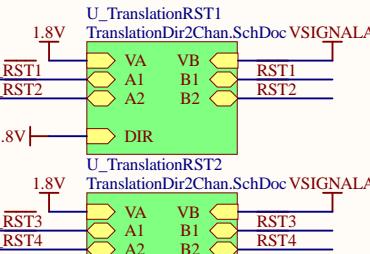
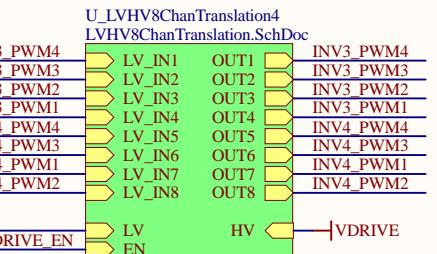
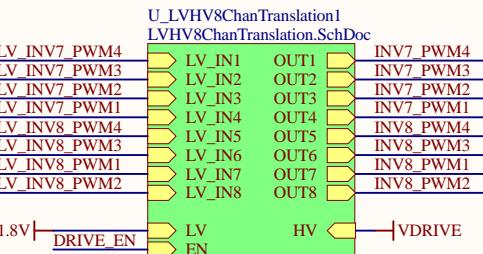
2

3

4

A

A



Title Inverter Level Translation

Size: Letter Number: 11 Revision: v1

Date: 5/25/2018 Time: 11:01:16 AM Sheet 11 of 28

File: InverterTranslation.SchDoc

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Drawn By: Nathan Petersen

1

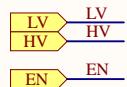
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3

4

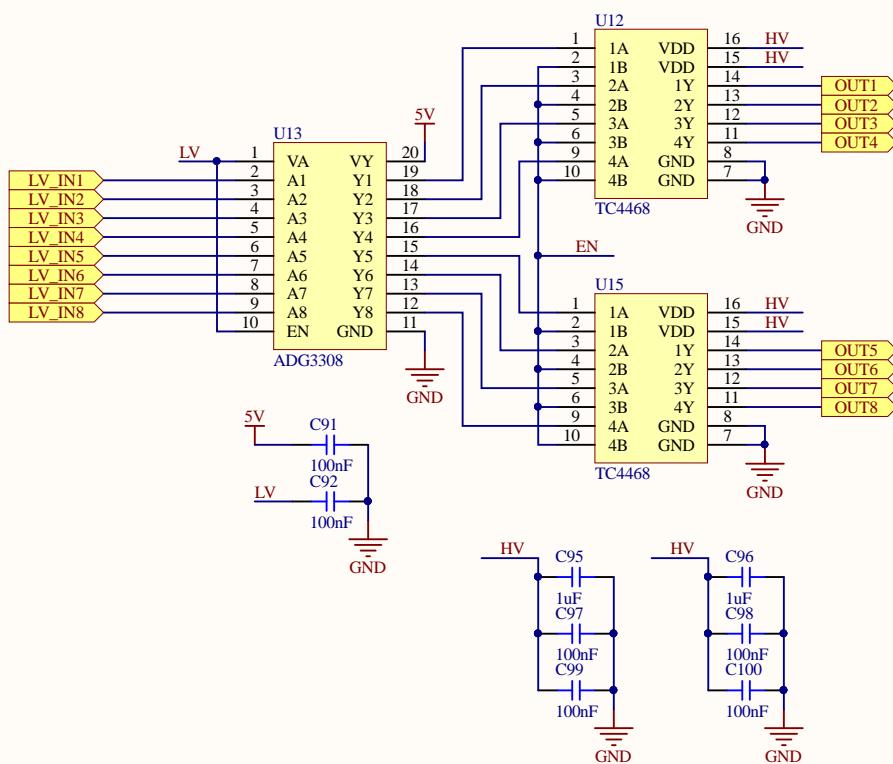
A

A



B

B



C

C

D

D

Title: **8-channel LV to HV Translation**

Size: Letter	Number: 12	Revision: v1
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Date: 5/25/2018	Time: 11:01:16 AM	Sheet 12 of 28
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File: LHV8ChanTranslation.SchDoc		
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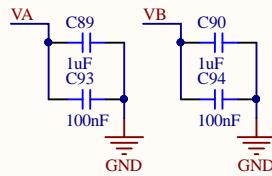
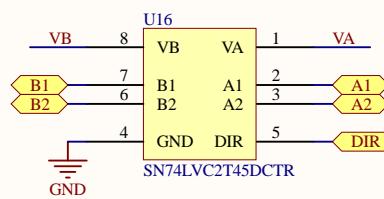
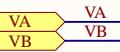
Drawn By: Nathan Petersen

A

B

C

D



Title 2-Channel Directional Translation

Size: Letter	Number: 13	Revision: v1
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Date: 5/25/2018	Time: 11:01:16 AM	Sheet 13 of 28
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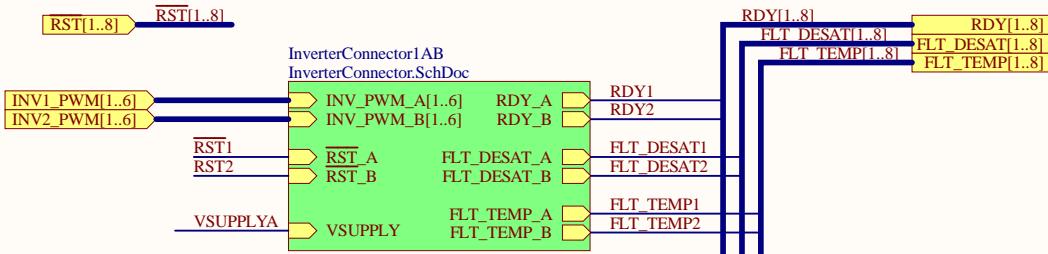
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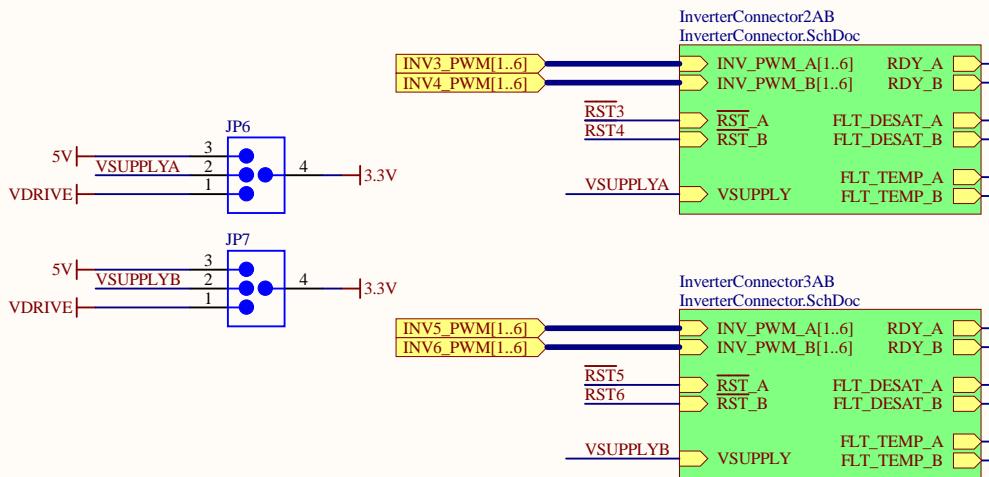


Drawn By: Nathan Petersen

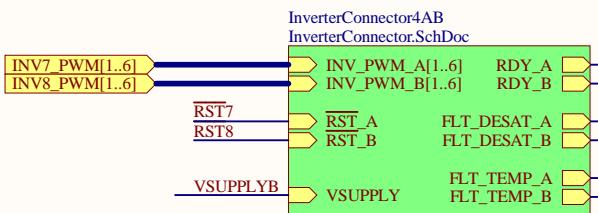
A



B



C



D

Title *Inverter Connectors*

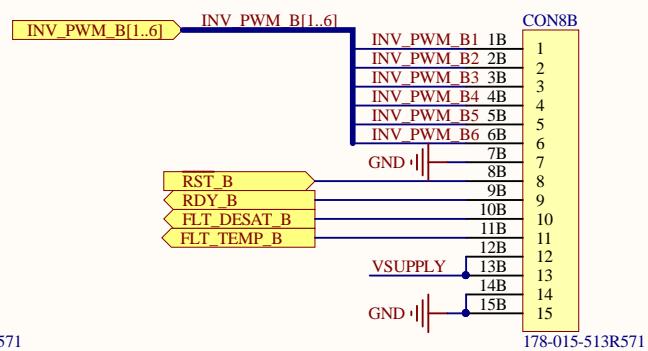
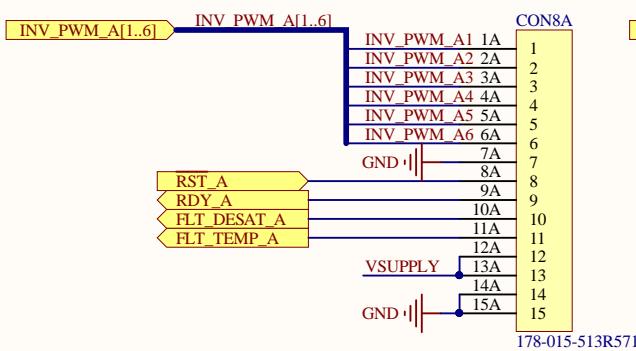
Size: Letter	Number: 14	Revision: v1
Date: 5/25/2018	Time: 11:01:16 AM	Sheet 14 of 28
File: InverterConnectors.SchDoc		Drawn By: Nathan Petersen



A

A

VSUPPLY



B

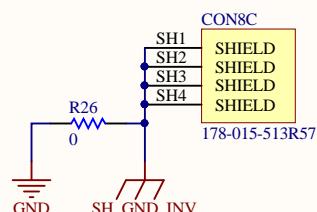
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C

C

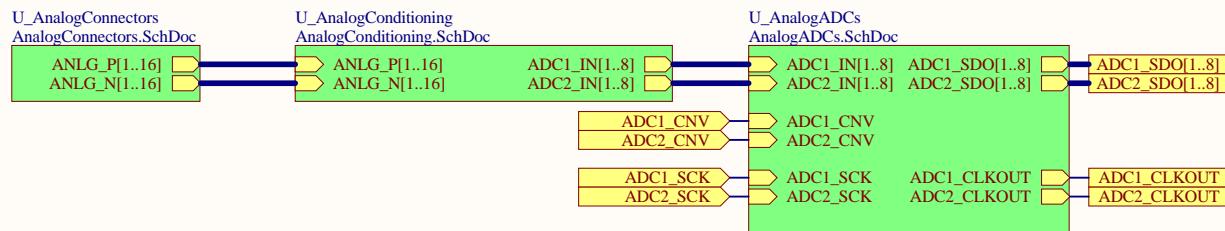
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D

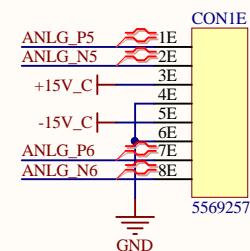
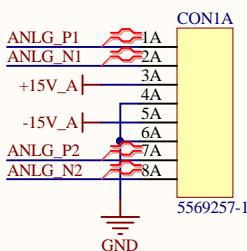

Title Inverter Connector

Size: Letter	Number: 15	Revision: v1
Date: 5/25/2018	Time: 11:01:16 AM	Sheet 15 of 28
File: InverterConnector.SchDoc		Drawn By: Nathan Petersen



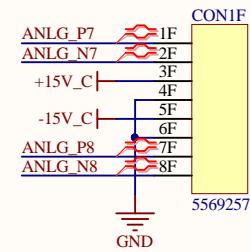
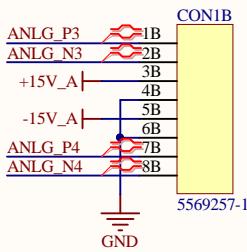


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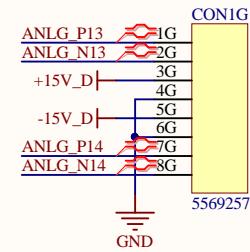
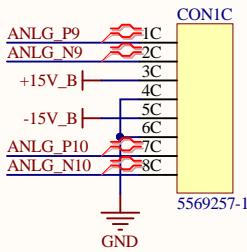


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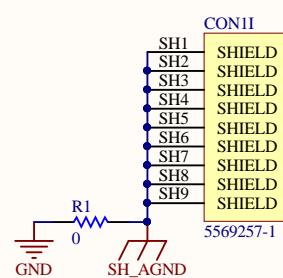
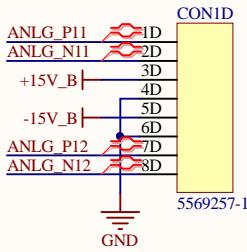
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C



D



Title Analog RJ45 Connectors

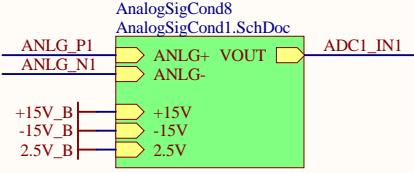
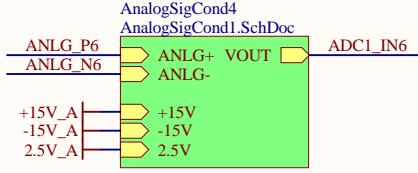
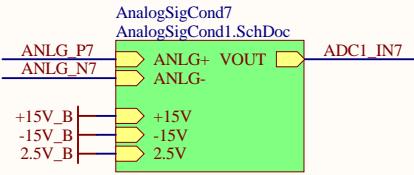
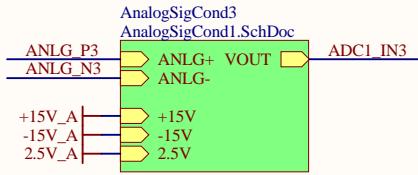
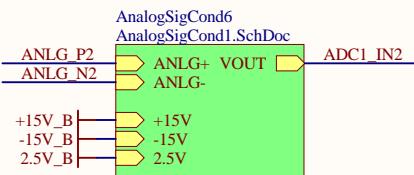
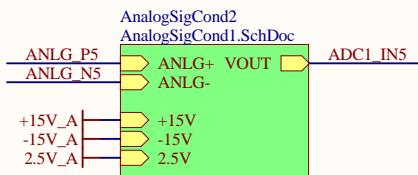
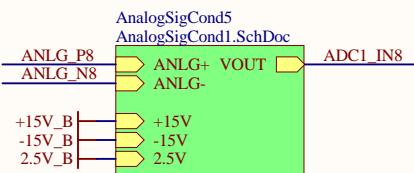
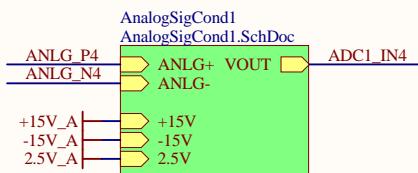
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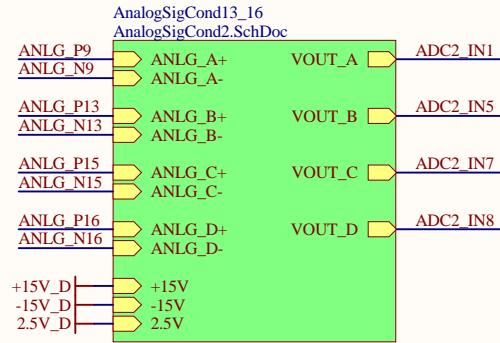
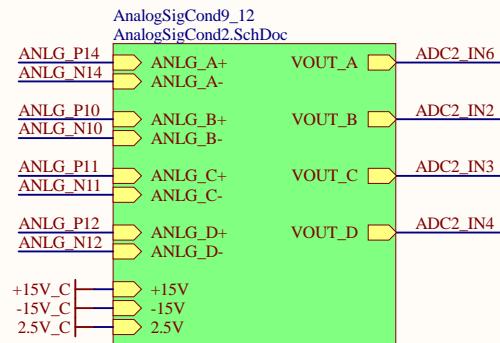
A

A



ANLG_P[1..16] ANLG_P[1..16]
ANLG_N[1..16] ANLG_N[1..16]

ADC1_IN[1..8] ADC1_IN[1..8]
ADC2_IN[1..8] ADC2_IN[1..8]



D

D

Title **Analog Signal Conditioning**

Size: Letter	Number: 18	Revision: v1
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Date: 5/25/2018	Time: 11:01:17 AM	Sheet 18 of 28
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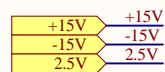
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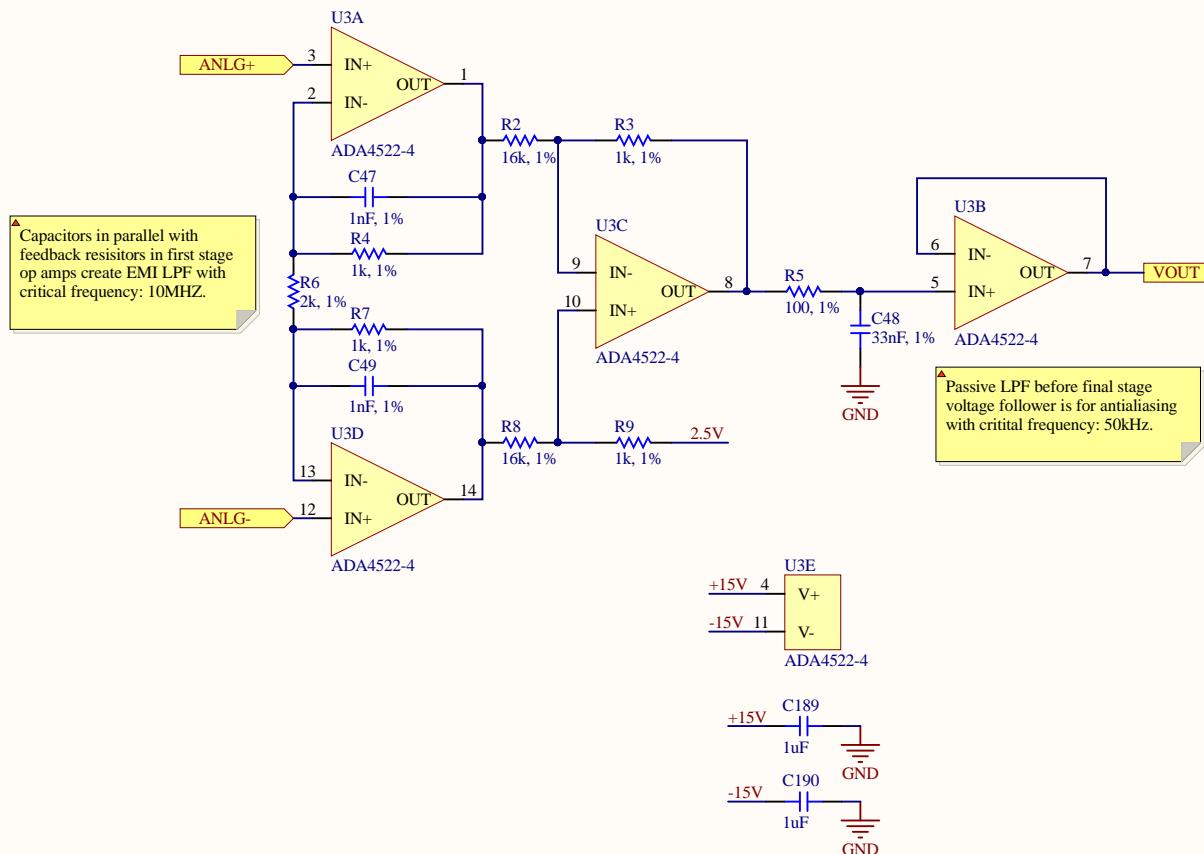


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A



B

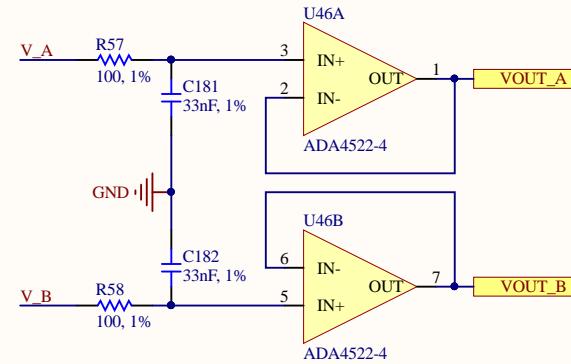
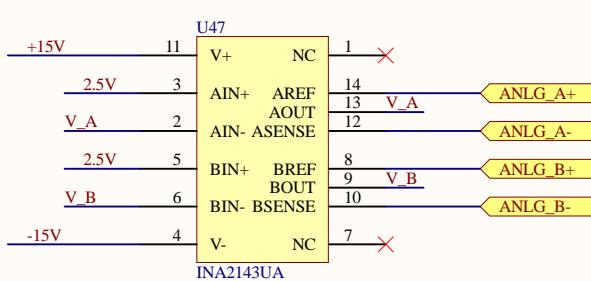
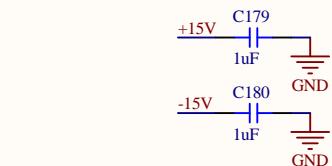


Title *Analog Signal Front-End 1*

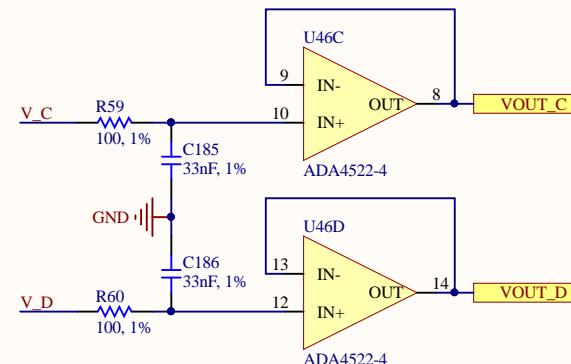
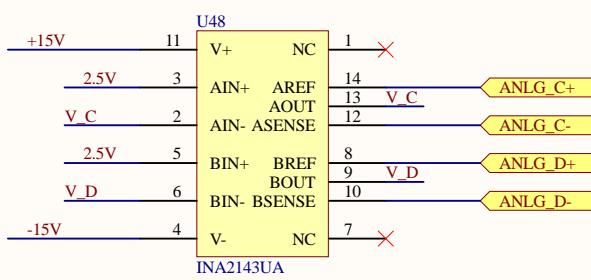
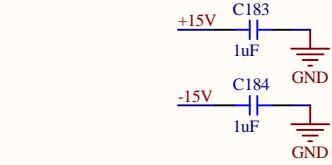
Size: Letter	Number: 19	Revision: v1
Date: 5/25/2018	Time: 11:01:17 AM	Sheet 19 of 28
File: AnalogSigCond1.SchDoc		Drawn By: Nathan Petersen



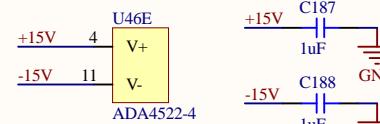
A



B



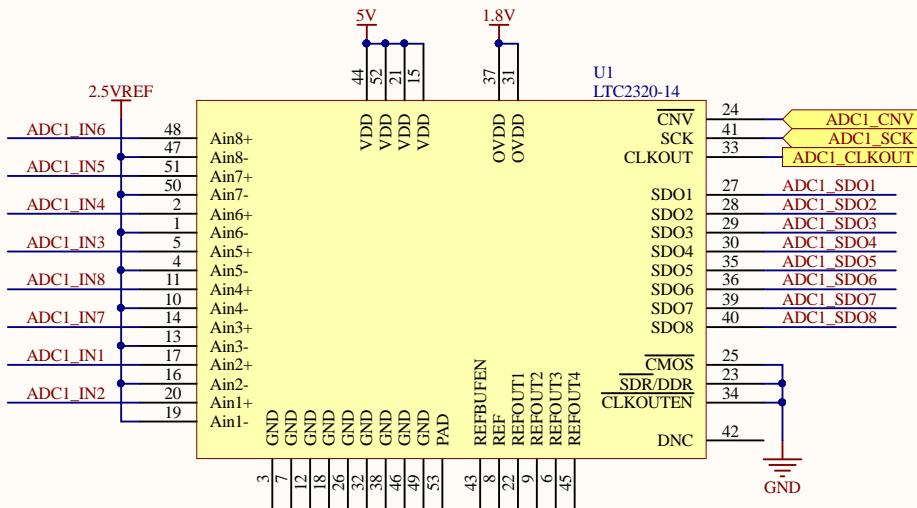
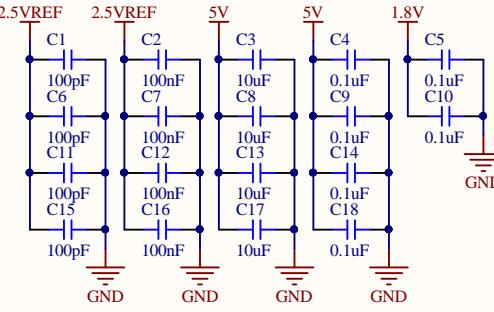
C



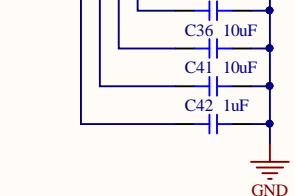
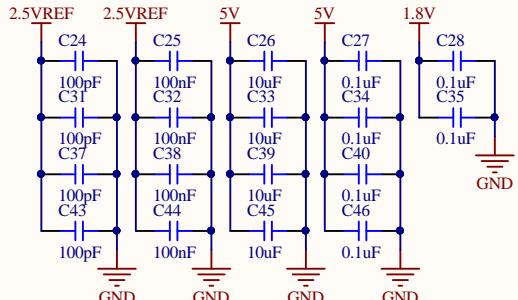
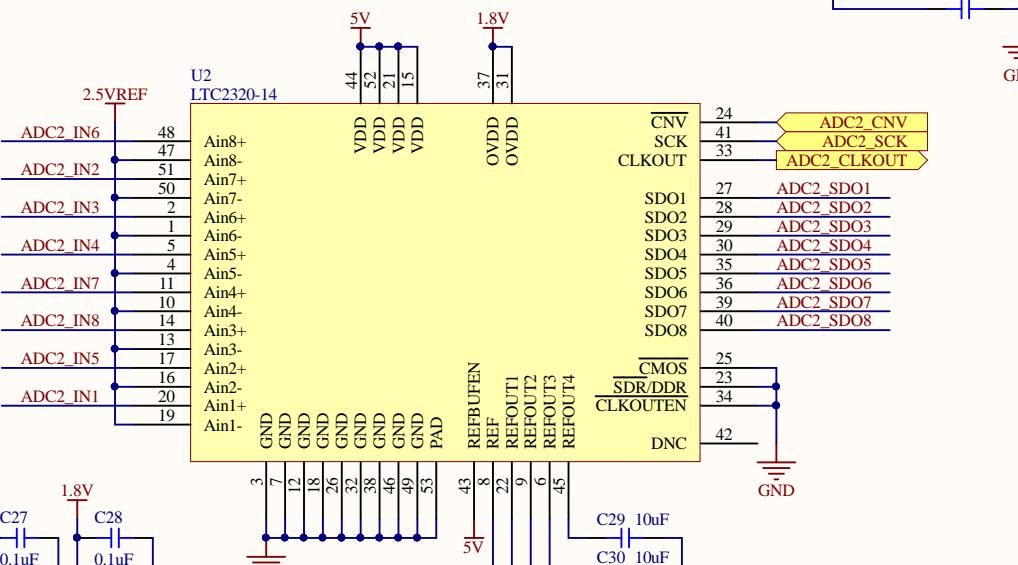
D

Title Analog Signal Front-End 2			WEMPEC UW-Madison Madison, WI	Drawn By: Nathan Petersen
Size: Letter	Number: 20	Revision: v1		
Date: 5/25/2018	Time: 11:01:17 AM	Sheet 20 of 28		
File: AnalogSigCond2.SchDoc				





The diagram illustrates two parallel signal paths. On the left, there are two orange trapezoidal boxes labeled "ADC1_IN[1..8]" and "ADC2_IN[1..8]". Each box has a horizontal line extending to the right, which then merges into a single blue horizontal line. This blue line continues across the page and ends at a central vertical node.

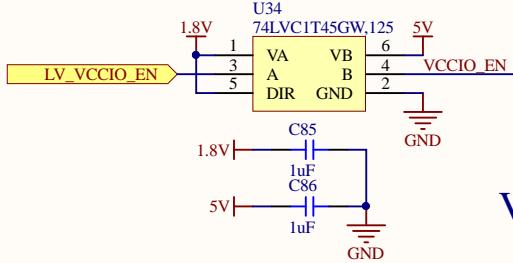


Title *ADCs*

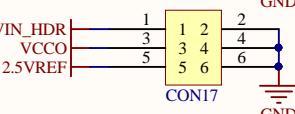
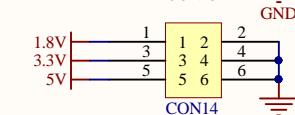
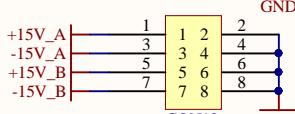
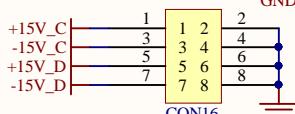
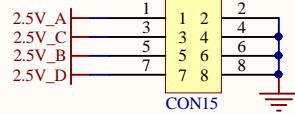
Size: Letter	Number: 21	Revision: v1
Date: 5/25/2018	Time: 11:01:17 AM	Sheet 21 of 28
File: AnalogADCs.SchDoc		

The diagram illustrates the merging of two parallel data paths. Two blue horizontal lines, each labeled "ADC1_SDO[1..8]" and "ADC2_SDO[1..8]", converge at a junction point. From this junction, a single yellow horizontal line continues, also labeled "ADC1_SDO[1..8]".



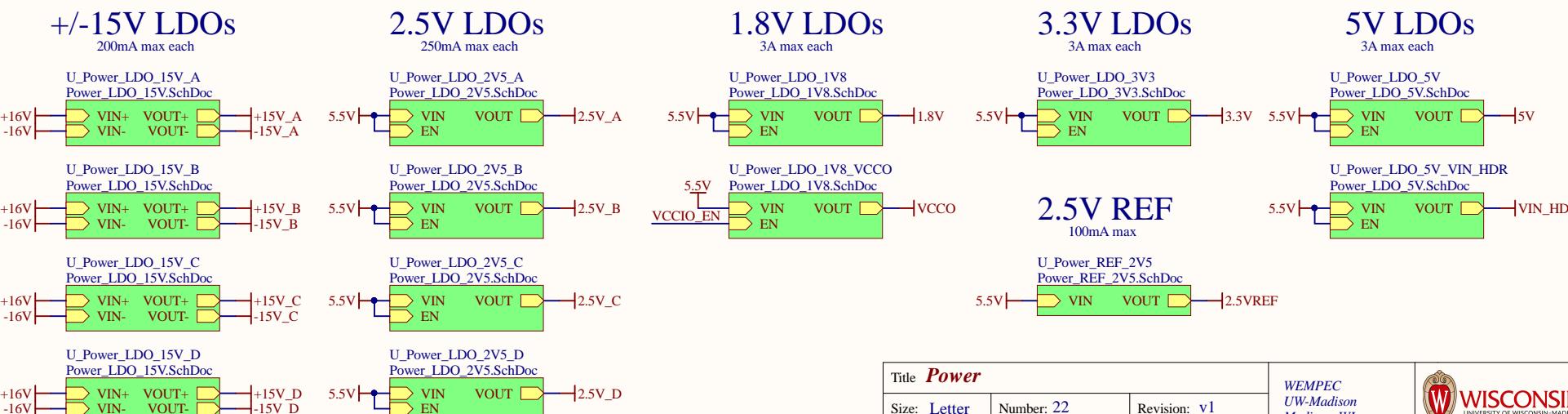
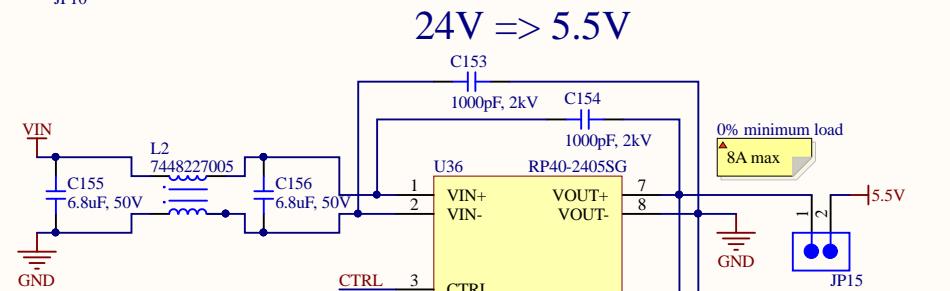
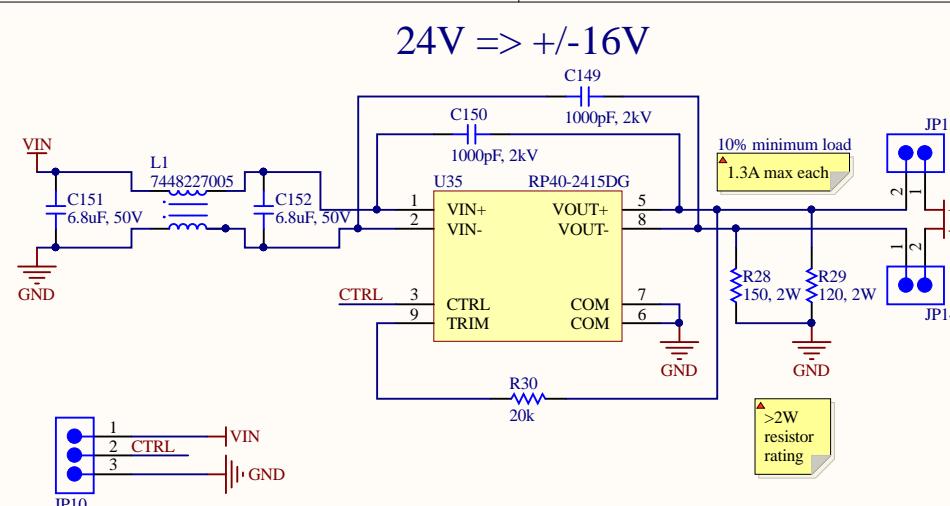


VOLTAGE HEADERS



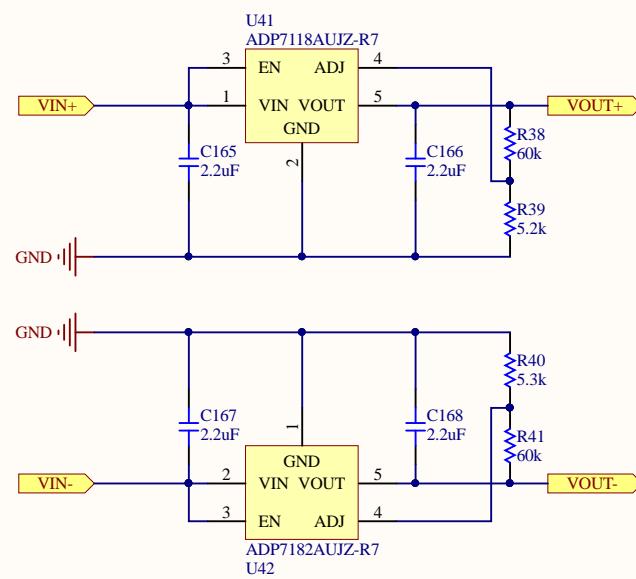
A
B
C
D

5V	<=> General
VIN_HDR	<=> PicoZed main power
3.3V	<=> General
1.8V	<=> General
VCCO	<=> PicoZed VCCIO*
2.5V_A	<=> SigCond1..4
2.5V_B	<=> SigCond5..8
2.5V_C	<=> SigCond9..12
2.5V_D	<=> SigCond13..16
2.5VREF	<=> ADCs input reference
+/-15V_A	<=> Con1..2 / SigCond1..4
+/-15V_B	<=> Con3..4 / SigCond5..8
+/-15V_C	<=> Con5..6 / SigCond9..12
+/-15V_D	<=> Con7..8 / SigCond13..16



Title Power			WEMPEC UW-Madison Madison, WI
Size: Letter	Number: 22	Revision: v1	
Date: 5/25/2018	Time: 11:01:18 AM	Sheet 22 of 28	
File: Power.SchDoc			Drawn By: Nathan Petersen



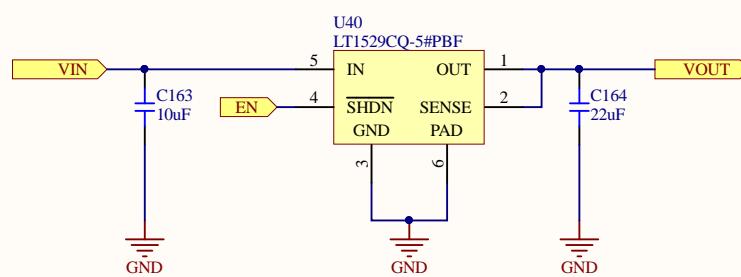


Title +/-15V LDO		
Size: Letter	Number: 23	Revision: v1
Date: 5/25/2018	Time: 11:01:18 AM	Sheet 23 of 28
File: Power_LDO_15V.SchDoc		

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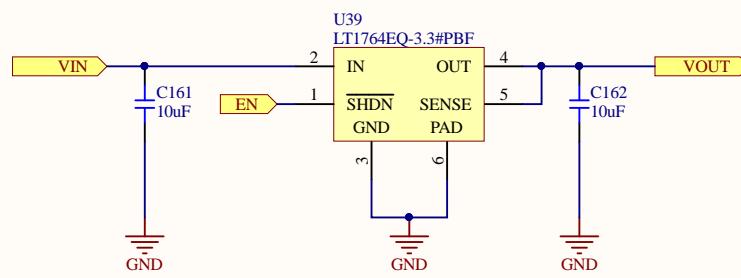


Title **5V LDO**

Size: Letter	Number: 24	Revision: v1
Date: 5/25/2018	Time: 11:01:18 AM	Sheet 24 of 28
File: Power_LDO_5V.SchDoc		Drawn By: Nathan Petersen

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Title **3.3V LDO**

Size: Letter	Number: 25	Revision: v1
Date: 5/25/2018	Time: 11:01:18 AM	Sheet 25 of 28
File: Power_LDO_3V3.SchDoc		Drawn By: Nathan Petersen

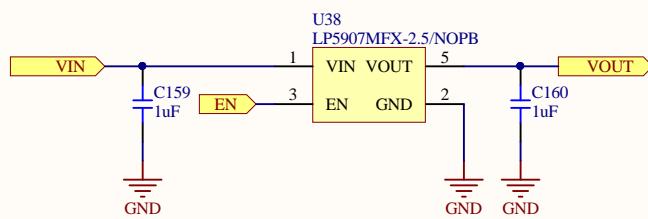


A

B

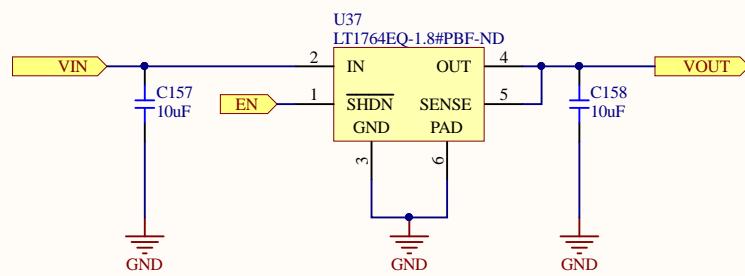
C

D


Title 2.5V LDO

Size: Letter	Number: 26	Revision: v1
Date: 5/25/2018	Time: 11:01:18 AM	Sheet 26 of 28
File: Power_LDO_2V5.SchDoc		Drawn By: Nathan Petersen

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Title ***1.8V LDO***

Size: Letter	Number: 27	Revision: v1
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Date: 5/25/2018	Time: 11:01:18 AM	Sheet 27 of 28
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File: Power_LDO_1V8.SchDoc

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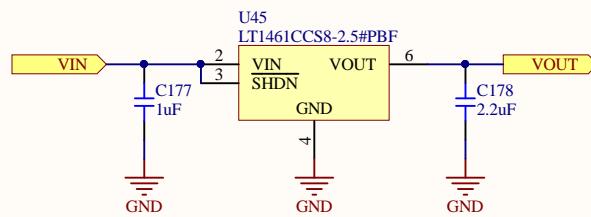
Drawn By: Nathan Petersen

A

B

C

D


Title *2.5V Reference*

Size: Letter	Number: 28	Revision: v1
Date: 5/25/2018	Time: 11:01:18 AM	Sheet 28 of 28
File: Power_REF_2V5.SchDoc		Drawn By: Nathan Petersen

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