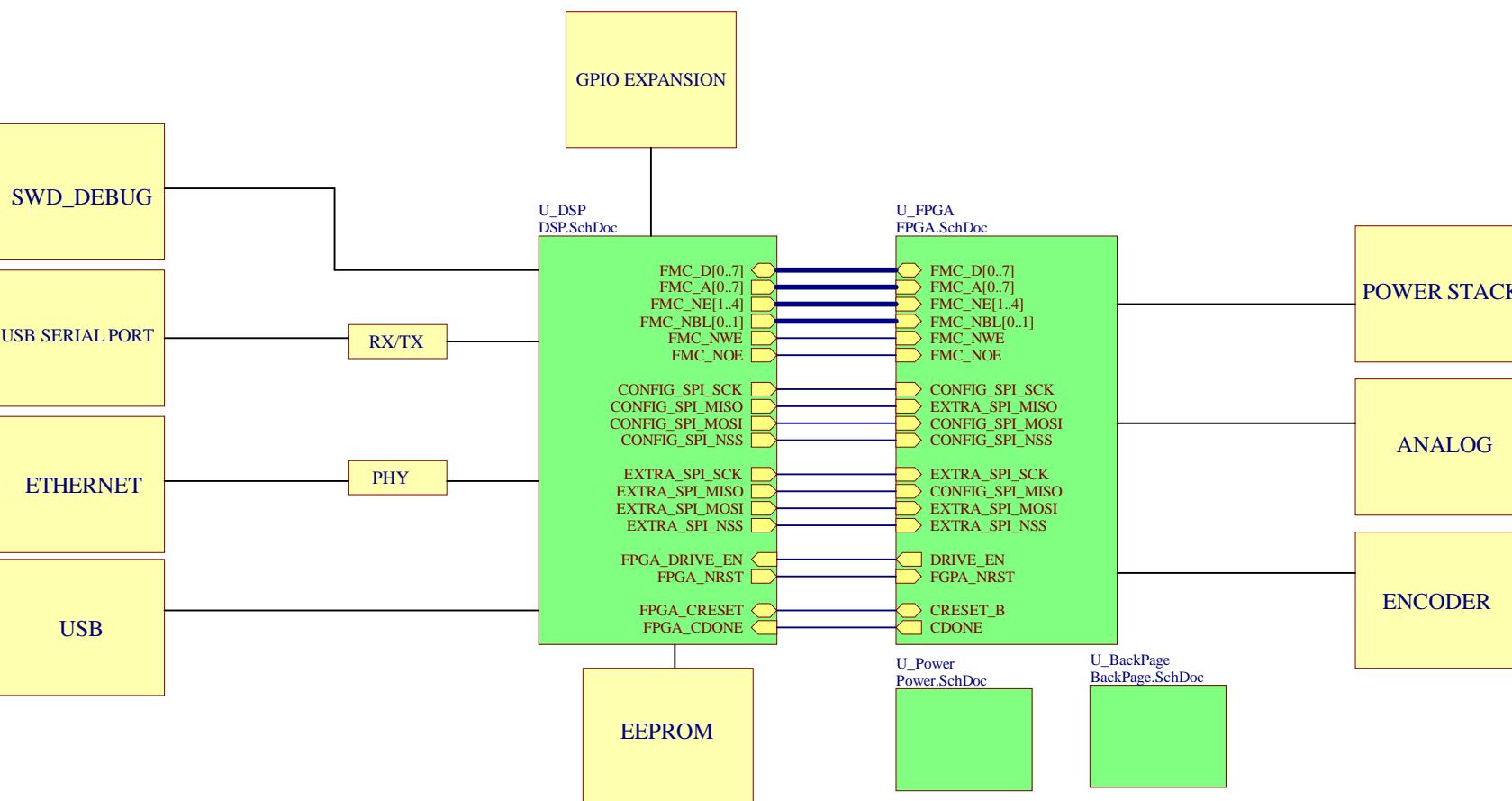


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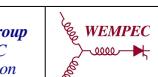
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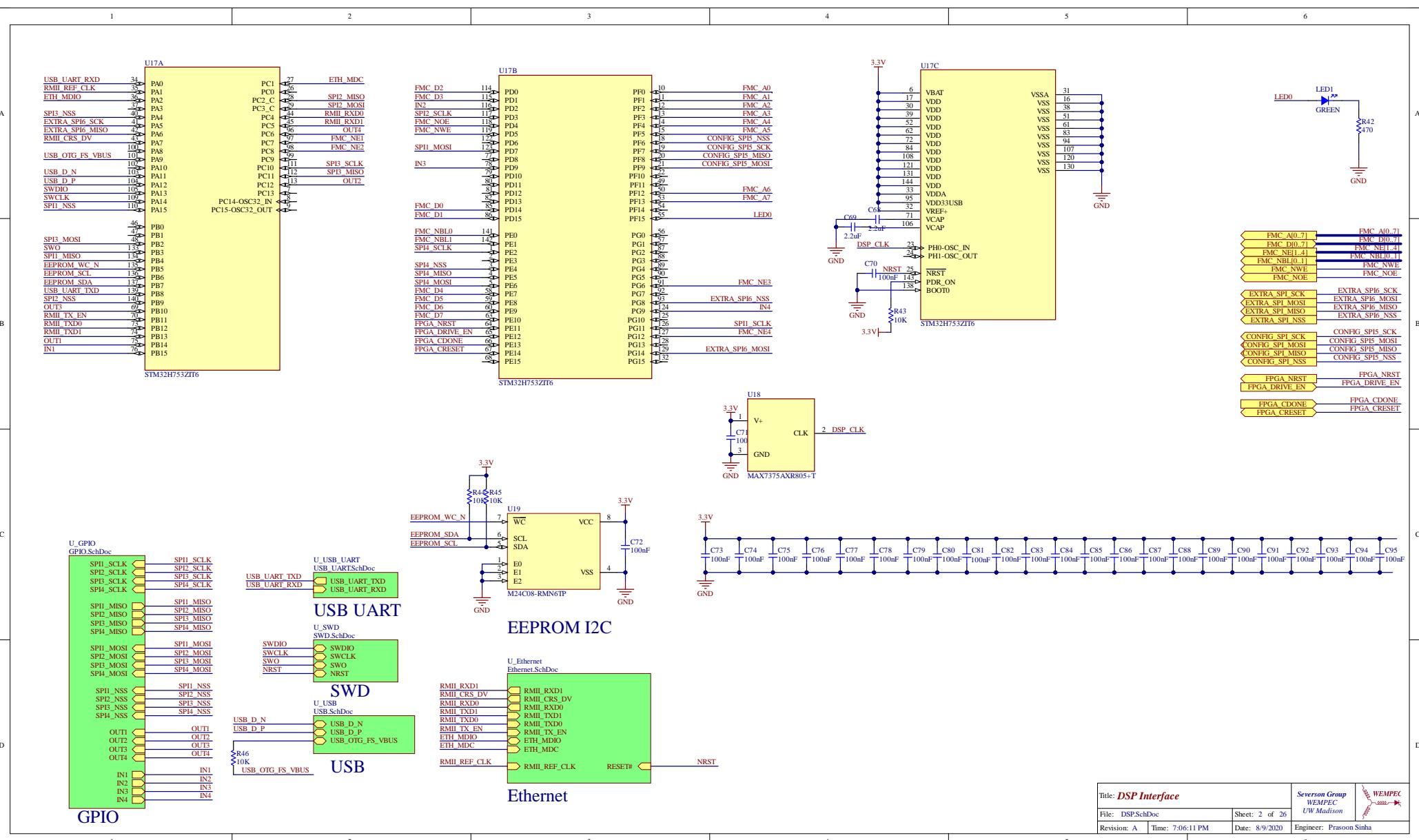
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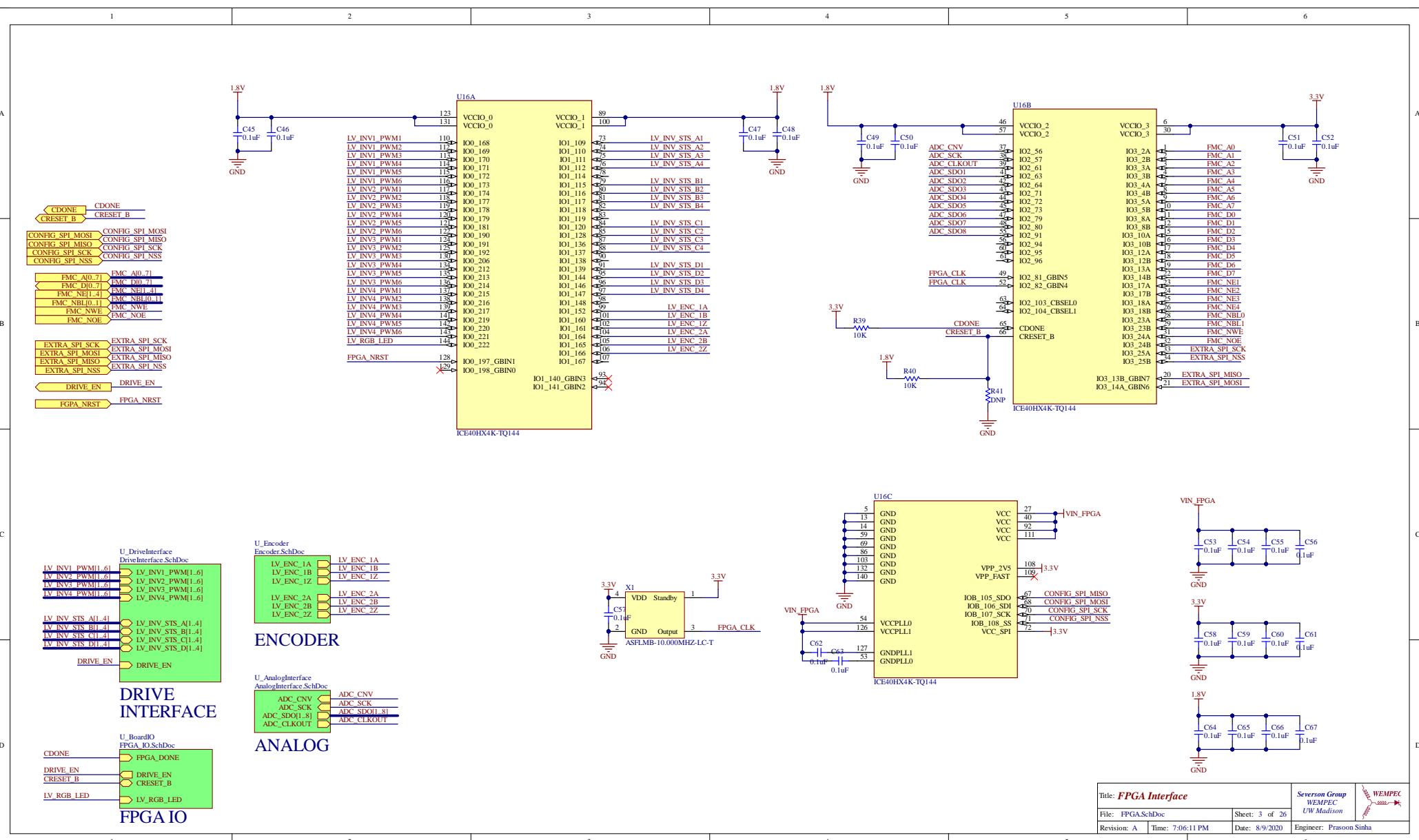
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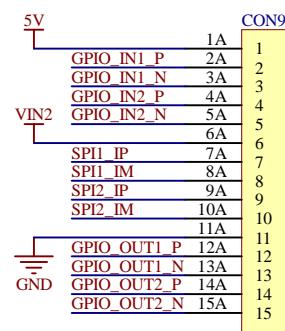
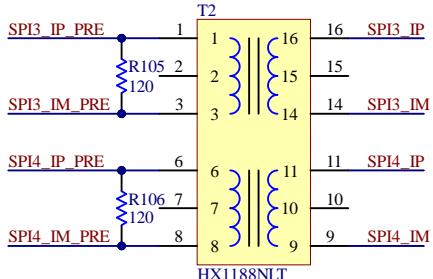
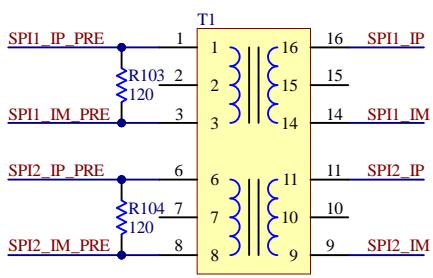
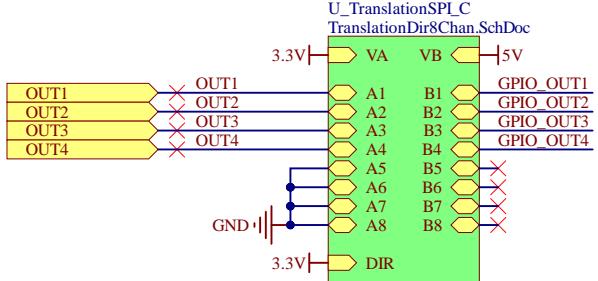
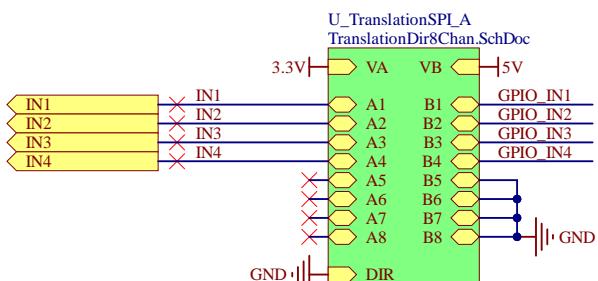
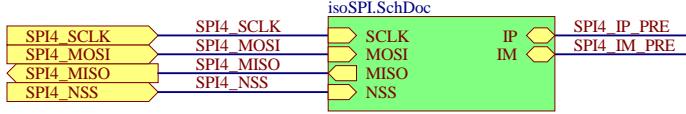
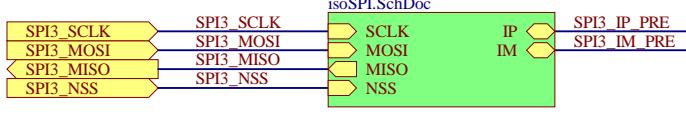
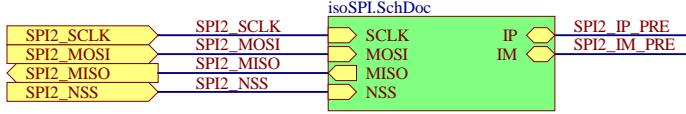
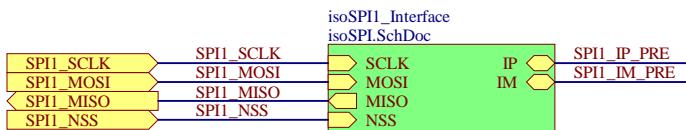
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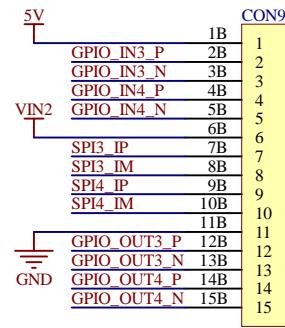
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Severson Group
 WEMPEC
 UWMadison




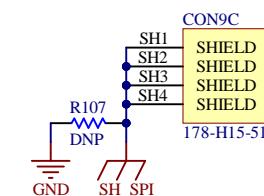




178-H15-513R49



178-H15-513R49



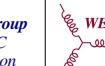
178-H15-513R497

Title: *GPIO*

File: GPIO.SchDoc

Revision: A Time: 7:06:11 PM Date: 8/9/2020

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9/2020 | Engineer: Prasoon Sinha

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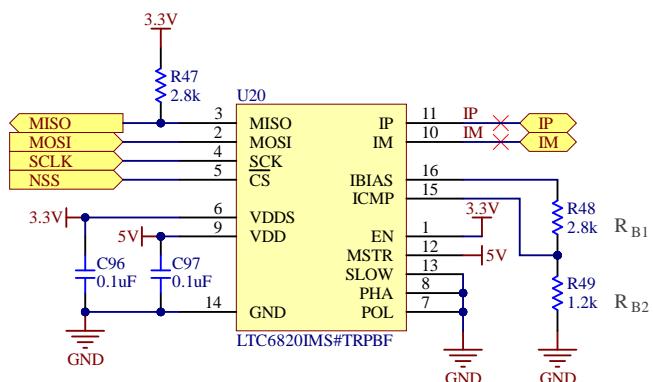
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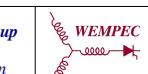
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Title: *isoSPI Interface*

File: isoSPI.SchDoc Sheet: 5 of 26

Revision: A Time: 7:06:11 PM Date: 8/9/2020

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Engineer: Nathan Petersen

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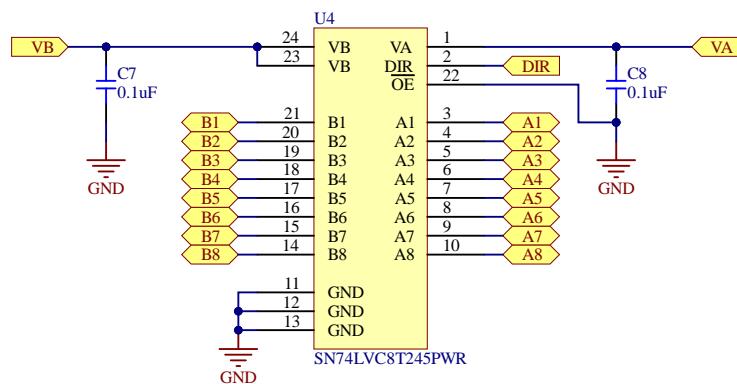
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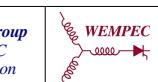
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Title: **8-Channel Directional Translation**File: **TranslationDir8Chan.SchDoc** Sheet: **6 of 26**Revision: **A** Time: **7:06:11 PM** Date: **8/9/2020**

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Engineer: Nathan Petersen

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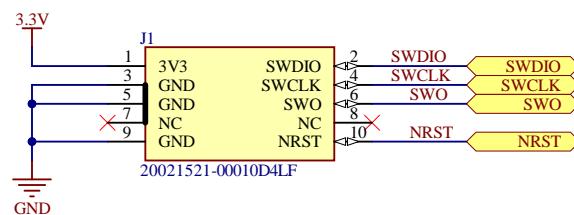
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Title: SWD			Severson Group WEMPEC UWMadison
File: SWD.SchDoc	Sheet: 7 of 26		
Revision: A	Time: 7:06:11 PM	Date: 8/9/2020	
Engineer: Prasoon Sinha			WEMPEC

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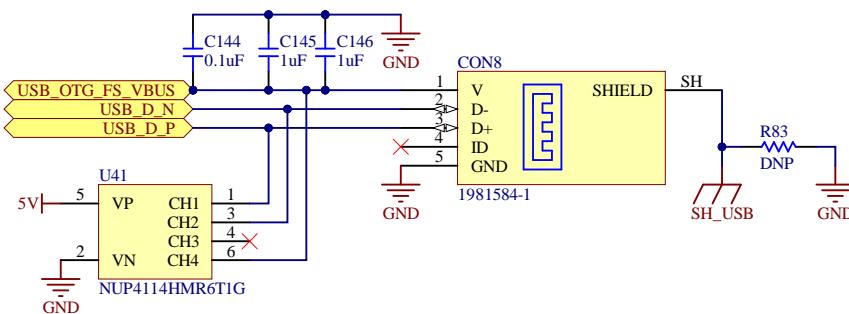
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Title: USB			Severon Group WEMPEC UWMadison
File: USB.SchDoc	Sheet: 8 of 26		
Revision: A	Time: 7:06:11 PM	Date: 8/9/2020	
Engineer: Prasoon Sinha			

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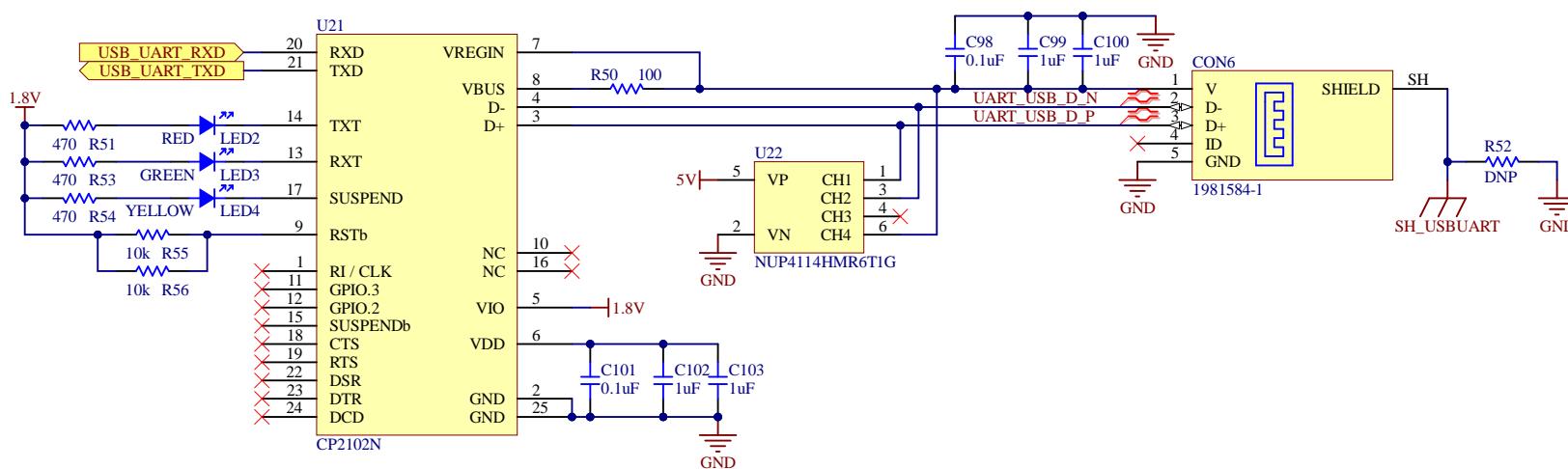
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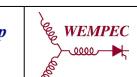
C

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Title: **USB UART**File: **USB_UART.SchDoc**Sheet: **9 of 26**Revision: **A** Time: **7:06:11 PM**Date: **8/9/2020**

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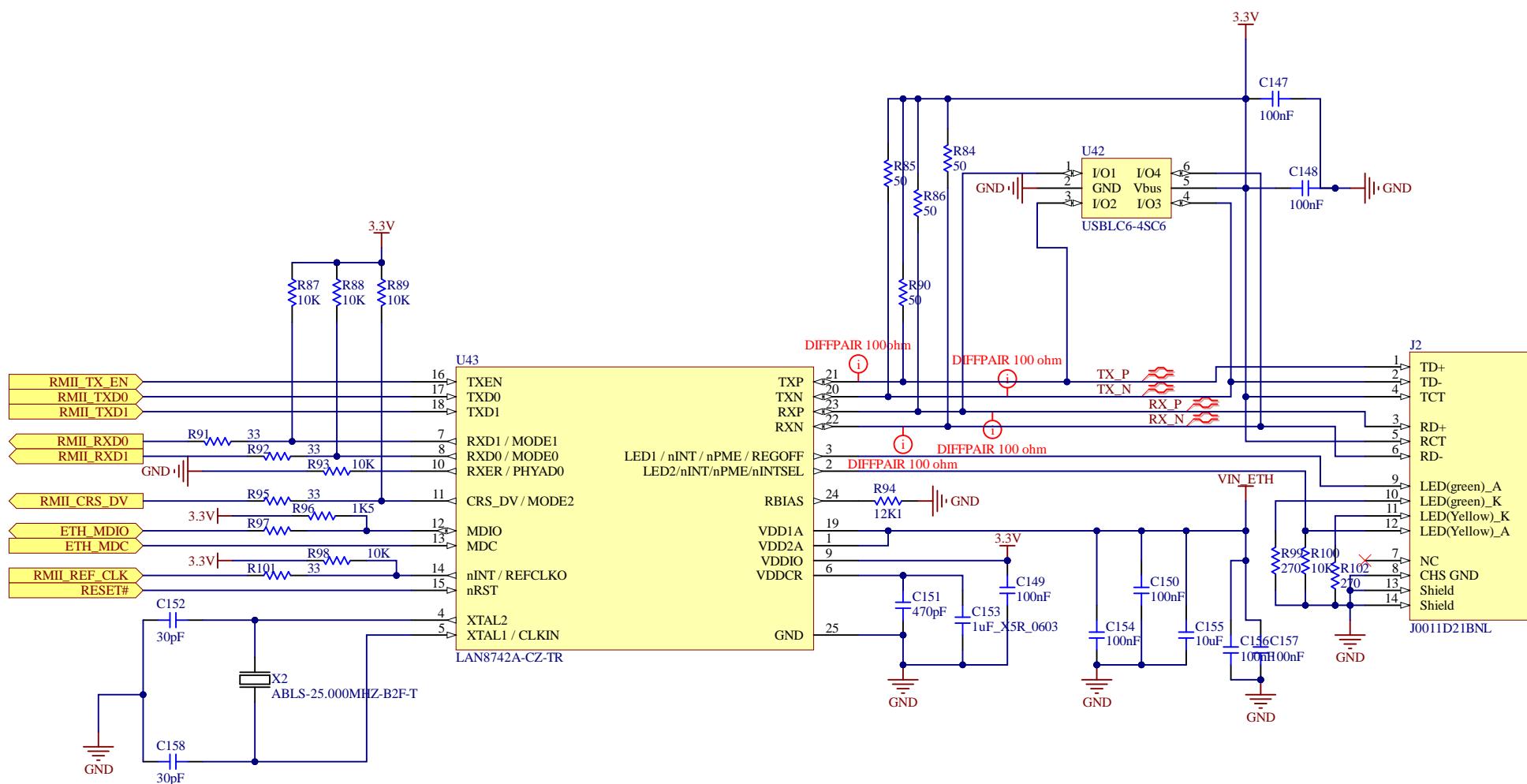
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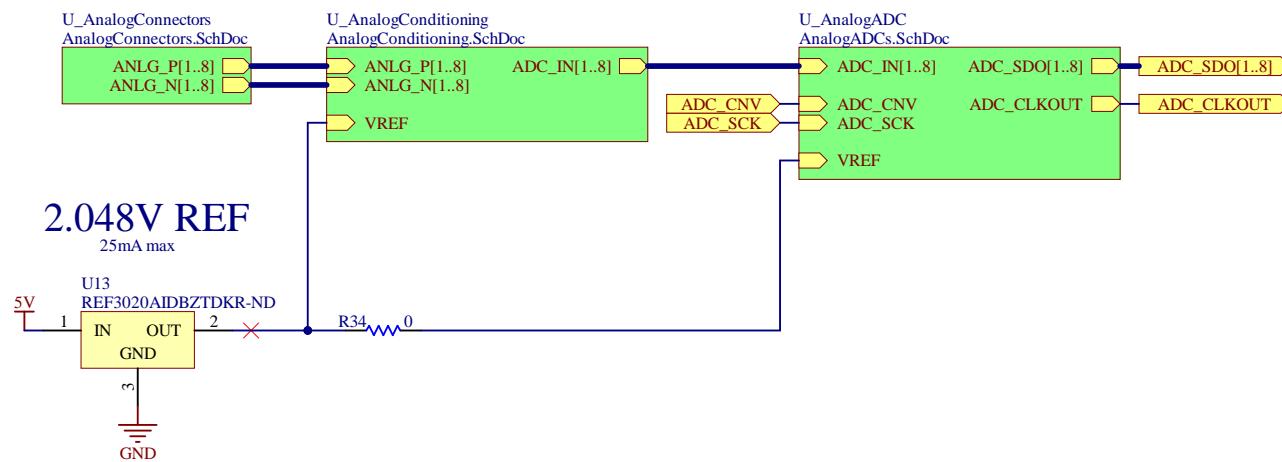
Title: Ethernet		<i>Severson Group WEMPEC UWMadison</i>	
File: Ethernet.SchDoc		Sheet: 10 of 26	
Revision: A	Time: 7:06:11 PM	Date: 8/9/2020	Engineer: Prasoon Sinha

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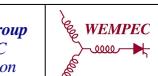
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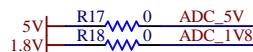
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Title: **Analog Interface**File: **AnalogInterface.SchDoc**Sheet: **11 of 26**Revision: **A** Time: **7:06:11 PM**Date: **8/9/2020**

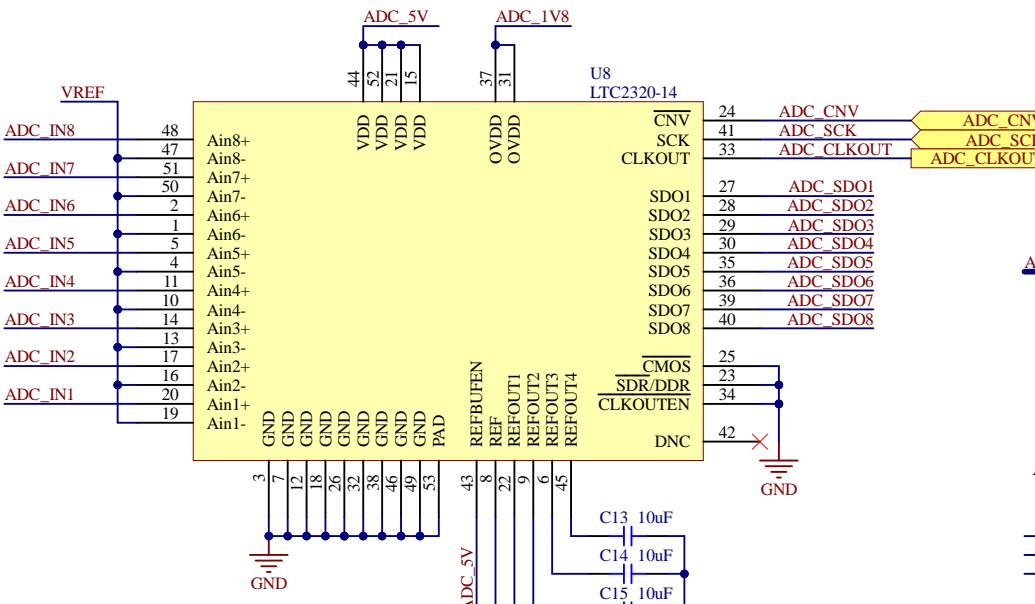
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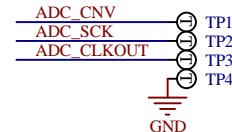


VREF
ADC_IN[1..8]

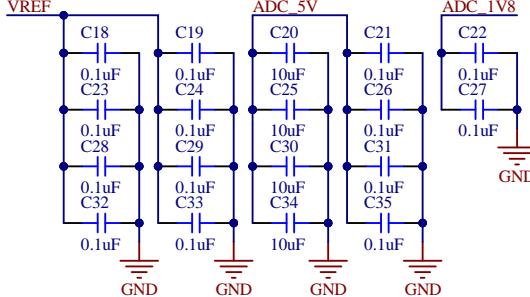


ADC_SDO[1..8] ADC_SDO[1..8]

ADC Serial Interface Test Points

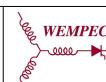


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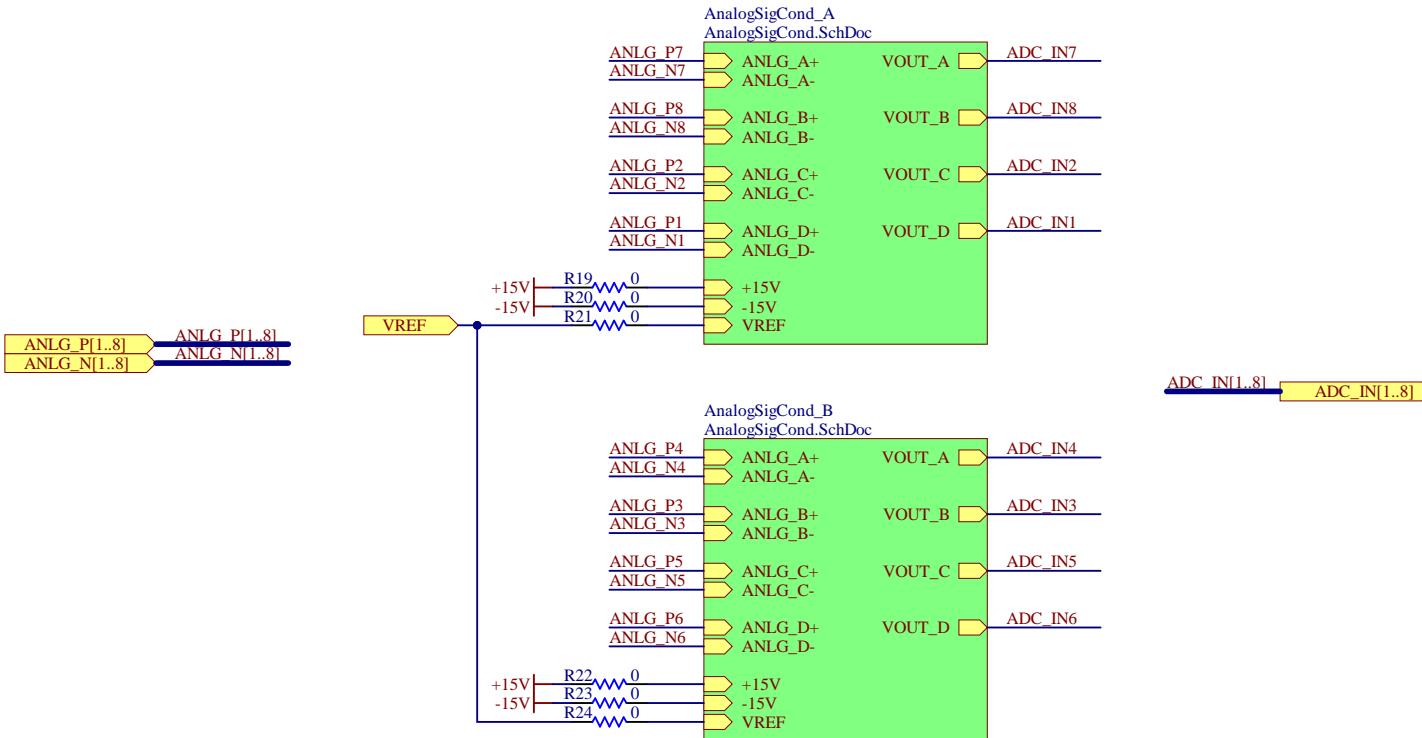
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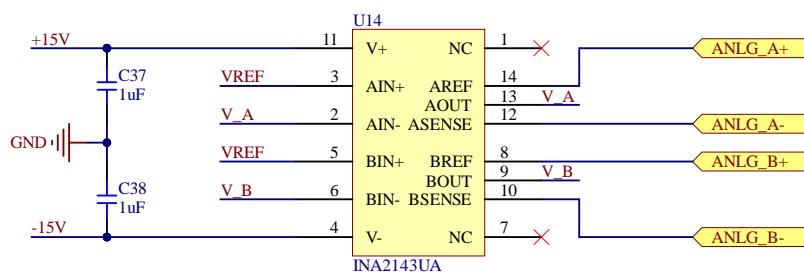
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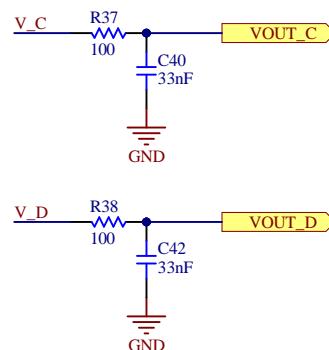
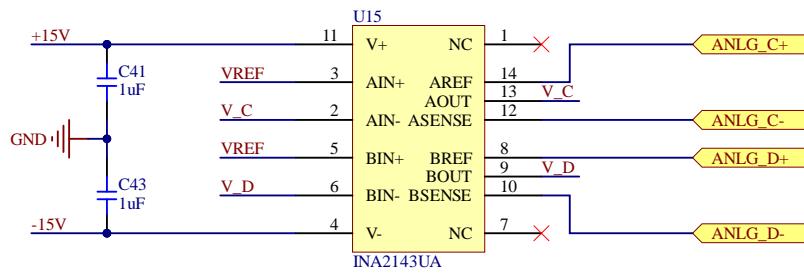
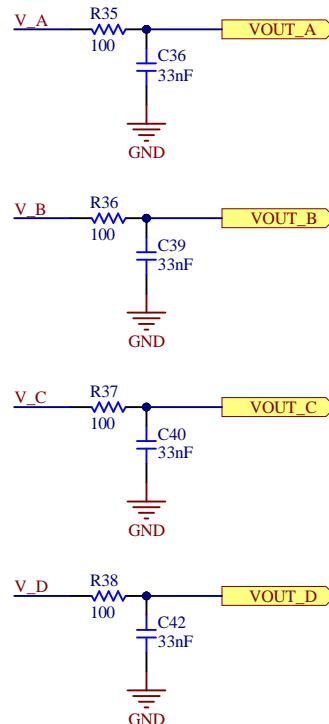


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△ LPF: fc = 50kHz



Title: **Analog Signal Front-End**

File: **AnalogSigCond.SchDoc**

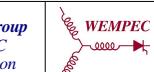
Sheet: **14 of 26**

Revision: **A**

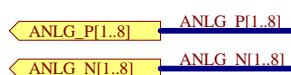
Time: **7:06:12 PM**

Date: **8/9/2020**

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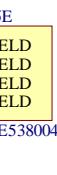
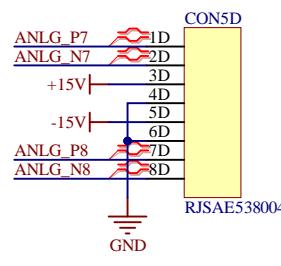
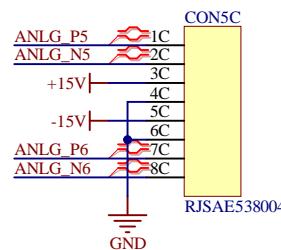
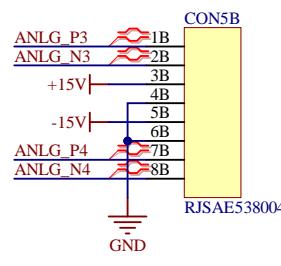
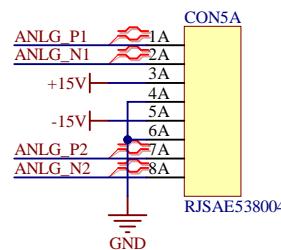
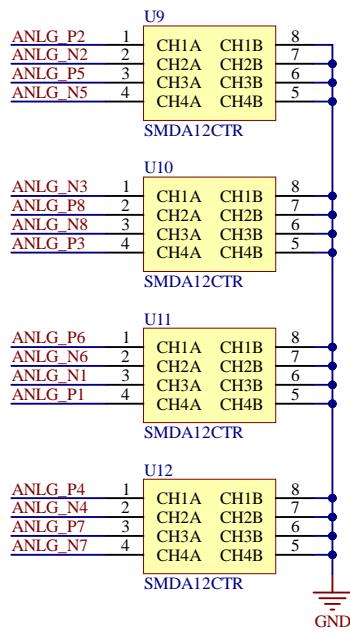


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ESD Protection



Force no input to 0V

ANLG_P1	R25 100k	ANLG_N1
ANLG_P2	R26 100k	ANLG_N2
ANLG_P3	R27 100k	ANLG_N3
ANLG_P4	R28 100k	ANLG_N4
ANLG_P5	R29 100k	ANLG_N5
ANLG_P6	R30 100k	ANLG_N6
ANLG_P7	R31 100k	ANLG_N7
ANLG_P8	R32 100k	ANLG_N8

D

Title: **Analog RJ45 Connectors**

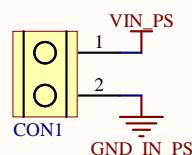
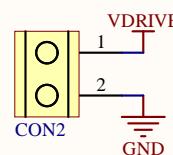
File: **AnalogConnectors.SchDoc** | Sheet: **15 of 26**

Revision: **A** | Time: **7:06:12 PM** | Date: **8/9/2020**

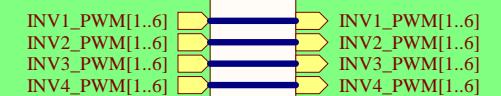
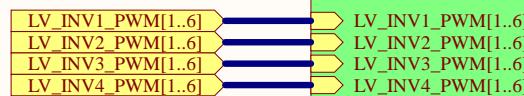
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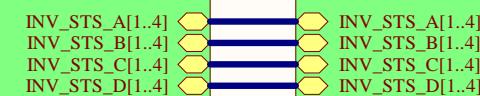
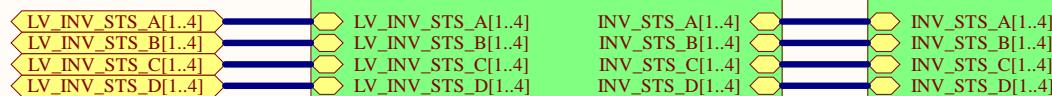
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POWERSTACK VIN**VDRIVE**

B

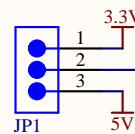
**U_InverterTranslation
InverterTranslation.SchDoc****U_InverterConnectors
InverterConnectors.SchDoc**

C

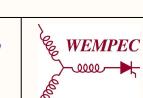


DRIVE_EN

VDDPS

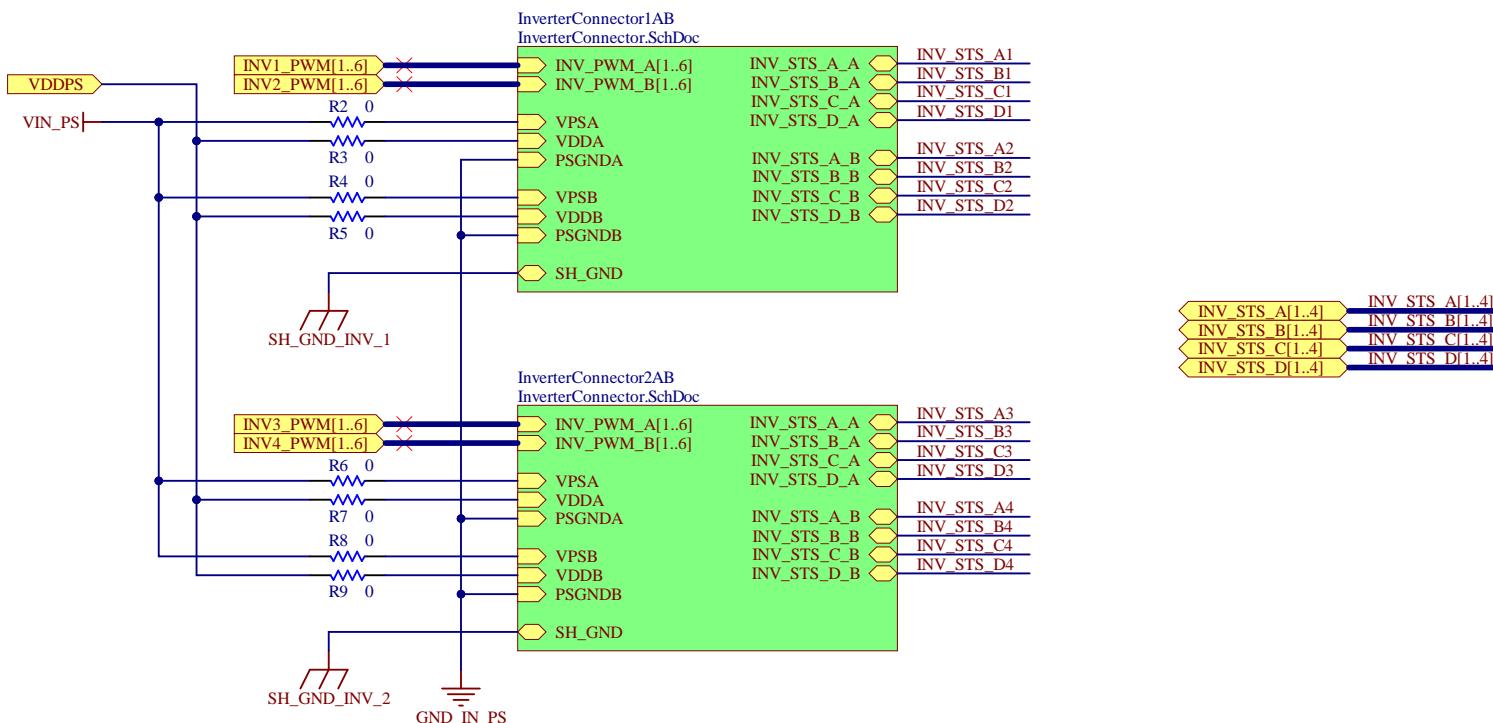


D

Title: **DriveInterface**File: **DriveInterface.SchDoc**Sheet: **16 of 26**Revision: **A** Time: **7:06:12 PM**Date: **8/9/2020****Severson Group
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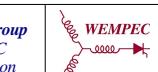
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D

Title: **Inverter Connectors**

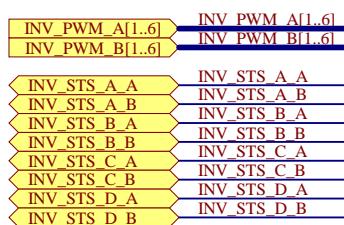
File: InverterConnectors.SchDoc | Sheet: 17 of 26

Revision: A | Time: 7:06:12 PM | Date: 8/9/2020

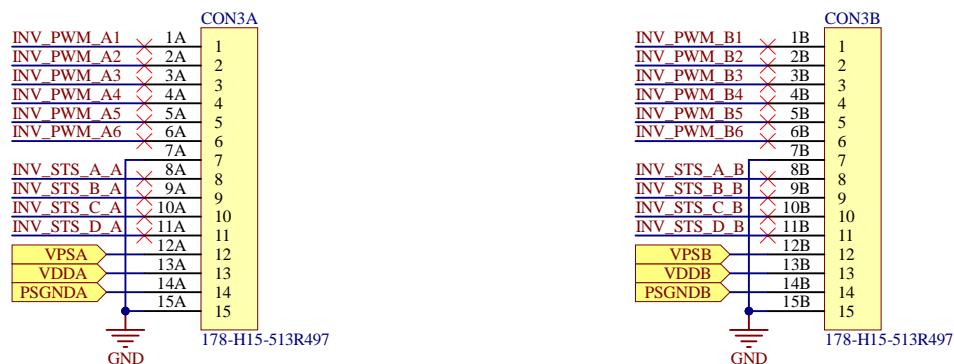
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Engineer: Nathan Petersen

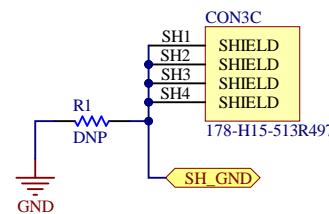
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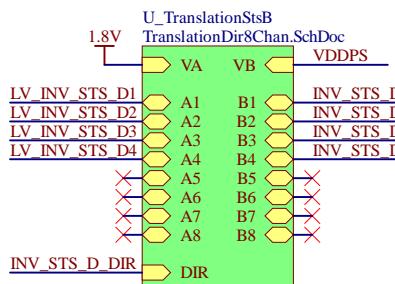
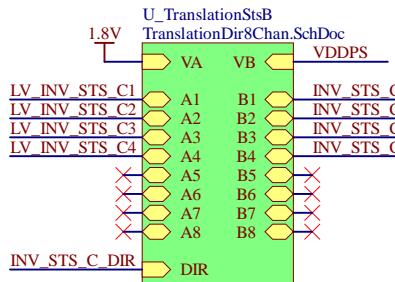
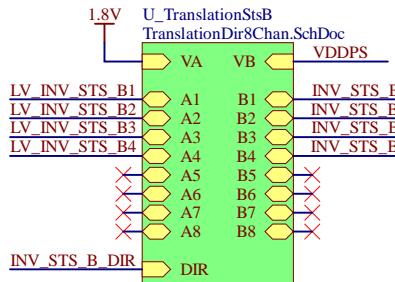
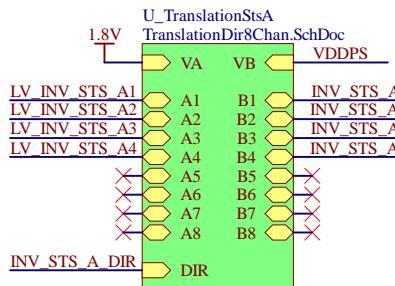
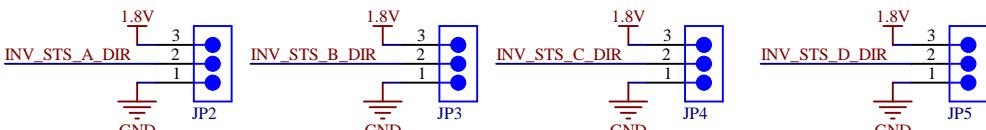
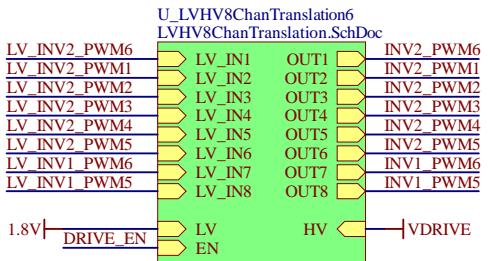
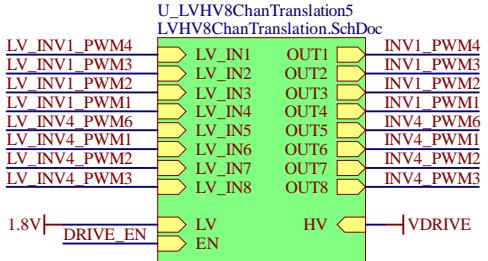
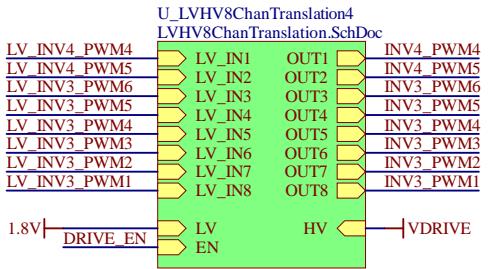
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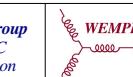
Title: Inverter Connector		Severson Group WEMPEC UWMadison
File: InverterConnector.SchDoc	Sheet: 18 of 26	
Revision: A	Time: 7:06:12 PM	
Date: 8/9/2020		Engineer: Nathan Petersen

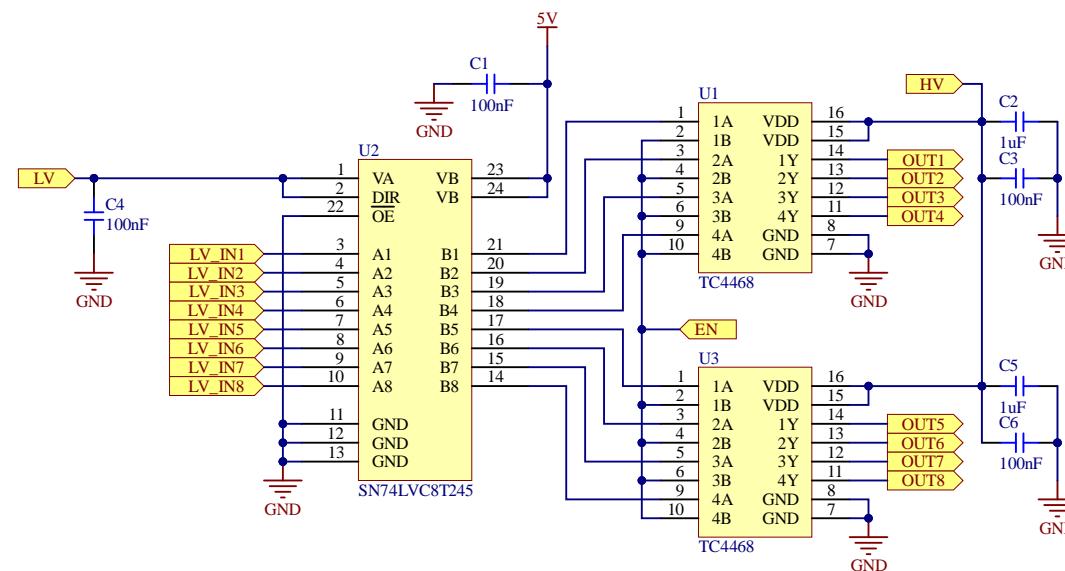
A

Title: **Inverter Level Translation**

File: InverterTranslation.SchDoc Sheet: 19 of 26

Revision: A Time: 7:06:12 PM Date: 8/9/2020

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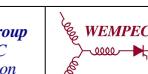
Title: **8-channel LV to HV Translation**

File: **LVHV8ChanTranslation.SchDoc** | Sheet: **20 of 26**

Revision: **A** | Time: **7:06:12 PM**

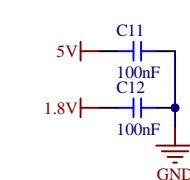
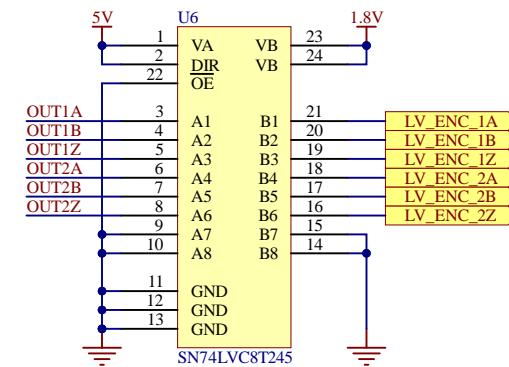
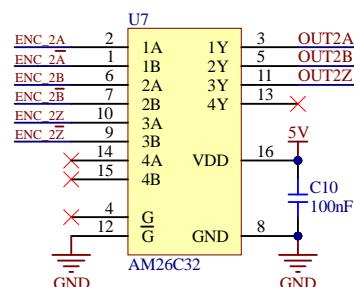
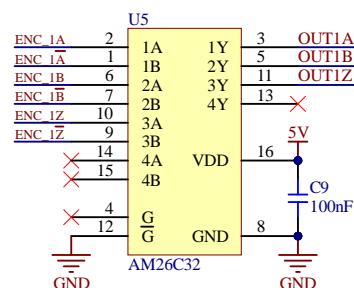
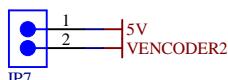
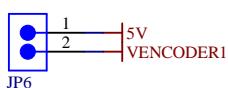
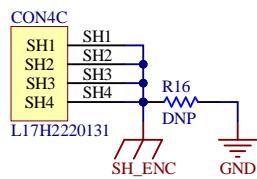
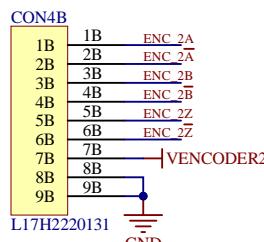
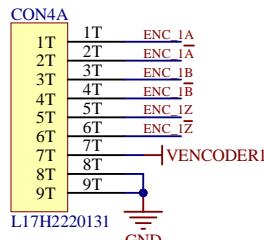
Date: **8/9/2020**

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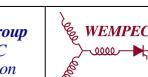
Engineer: **Prasoon Sinha**

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Title: **Encoders**

File: Encoder.SchDoc Sheet: 21 of 26

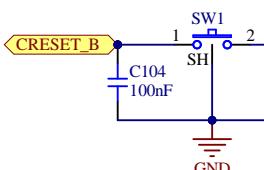
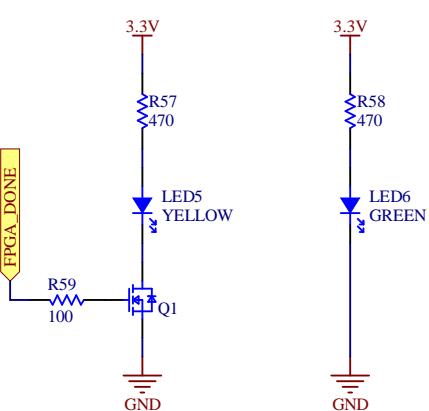
Revision: A Time: 7:06:12 PM Date: 8/9/2020

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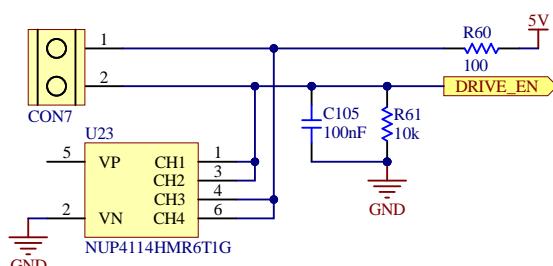
FPGA STATUS LEDS

RESET BUTTON

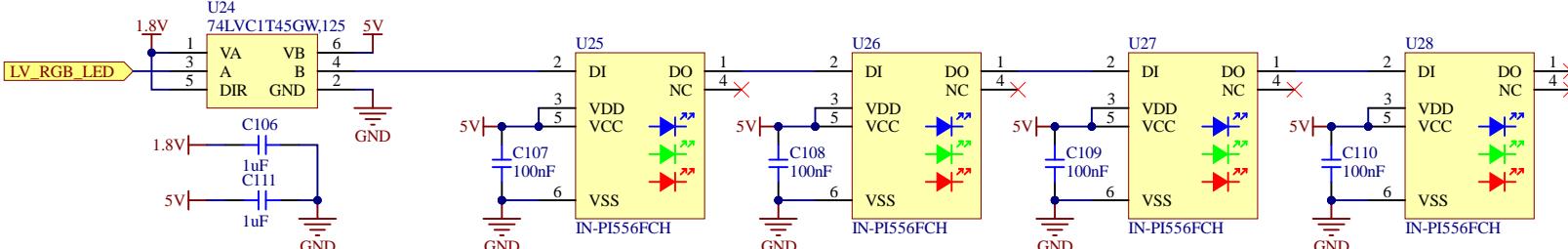
FPGA DONE



DRIVE ENABLE (ESTOP)



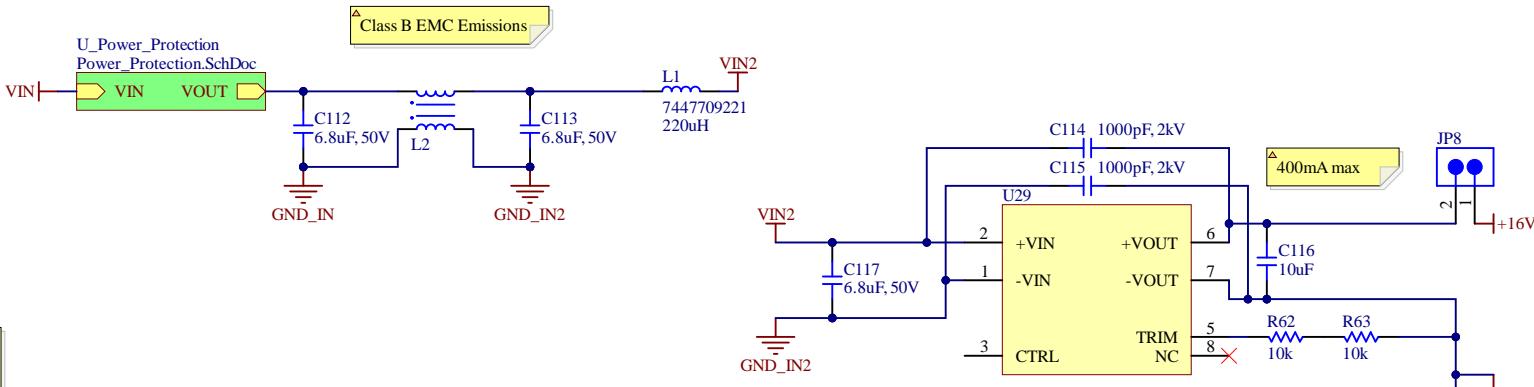
FPGA RGB LEDS



Title: FPGA I/O Interface			<i>Severson Group WEMPEC UWMadison</i>		
File: FPGA_IO.SchDoc					
Revision: A	Time: 7:06:12 PM	Date: 8/9/2020	Engineer: Prasoon Sinha		

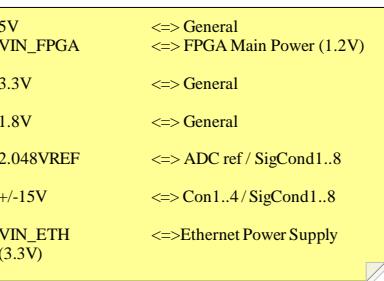
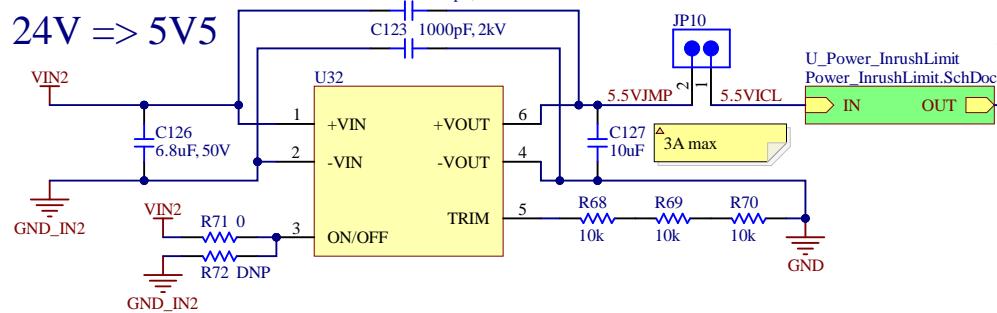
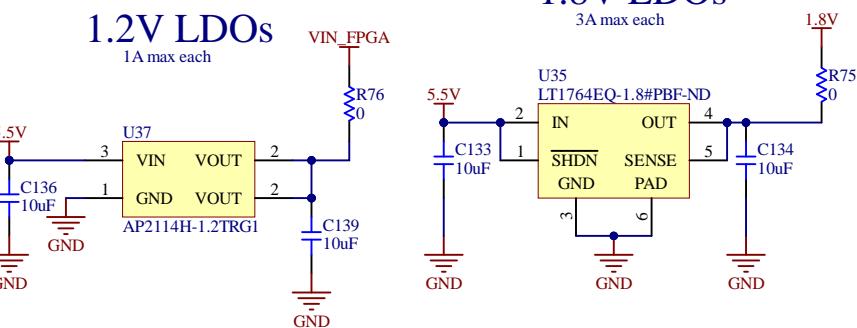
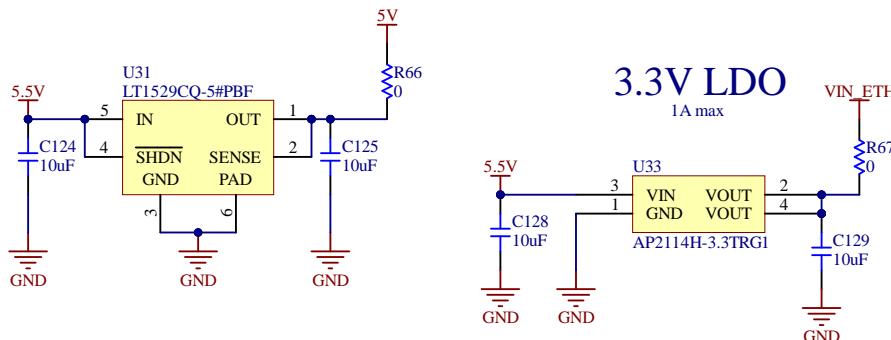
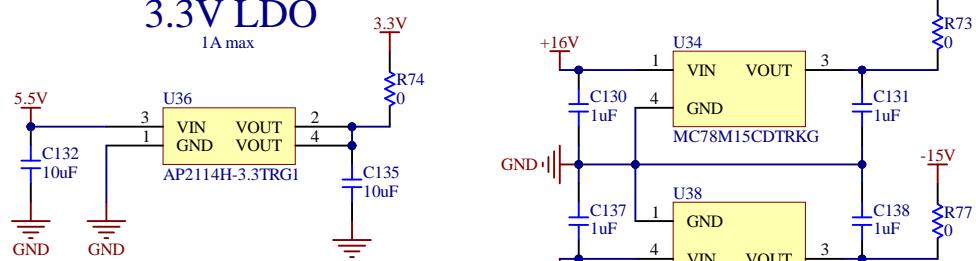
A

A



B

B

**24V => +16V****24V => -16V****+/-15V LDO 500mA max each**Title: **Power**File: **Power.SchDoc**Revision: **A**Time: **7:06:12 PM**Date: **8/9/2020**Sheet: **23 of 26**
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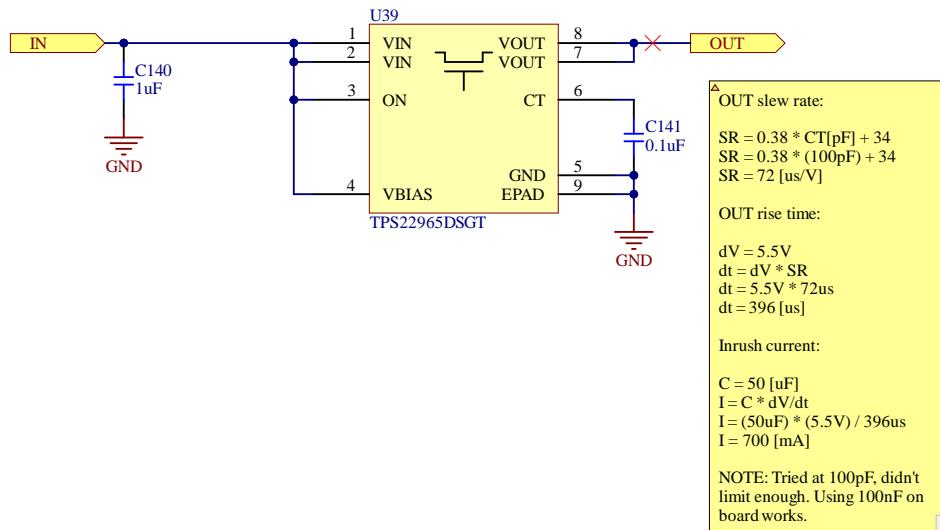
B

C

C

D

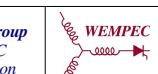
D

Title: **Inrush Current Limiter**

File: Power_InrushLimit.SchDoc | Sheet: 24 of 26

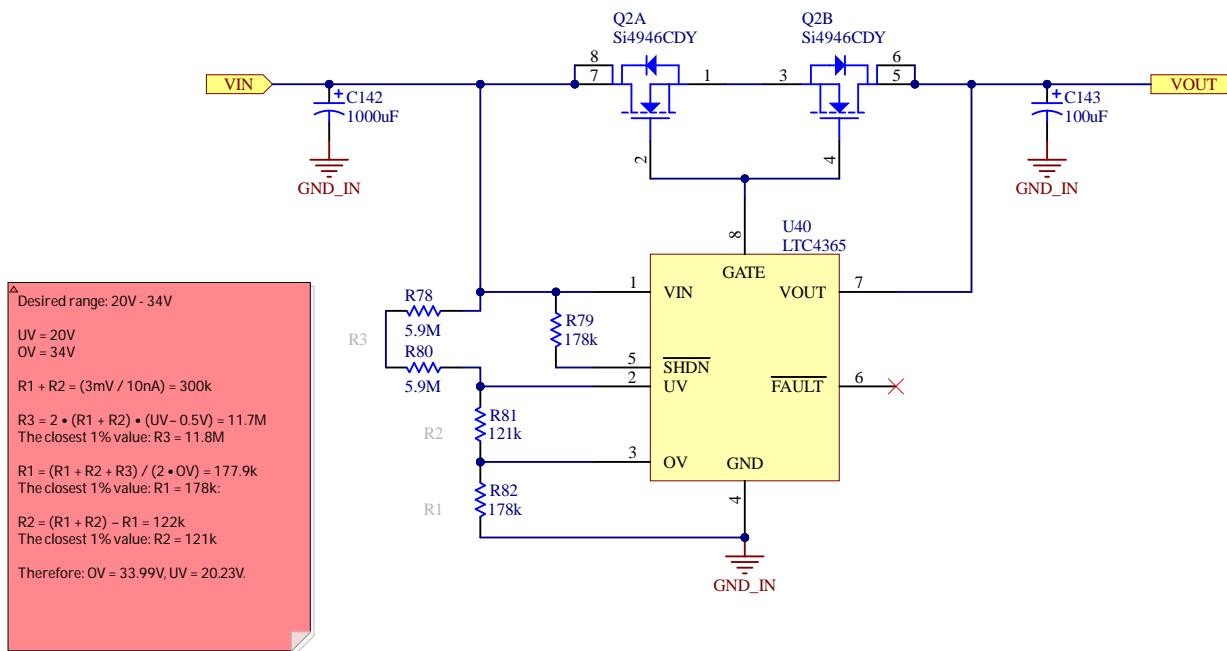
Revision: A | Time: 7:06:12 PM | Date: 8/9/2020

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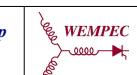
B

C

C

D

D

Title: **Power Protection**File: **Power_Protection.SchDoc**Sheet: **25 of 26**Revision: **A** Time: **7:06:12 PM**Date: **8/9/2020**
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4-40 Screws:**4-40 Standoffs:****Mouting Holes:**