Practice Problems on Main Memory and Virtual Memory

1. Given memory partitions of 200k, 150k, 80k and 350k (in order, top to bottom), apply first fit, best fit and worst fit algorithms to place processes with the space requirement of 170k, 120k, 185k and 125k (in order). Which algorithm makes the most effective use of memory?

   Answer: Worst fit is most effective for the scenario.

2. In a system there are 3 processes- P1 (10 bytes), P2 (6 bytes) and P3 (8 bytes) with page size of 2 bytes. Size of the main memory is 32 bytes. Page tables of processes are given below.

Page Tables					
Process P1		Process P2		Process P3	
p	f	p	f	p	f
0	7	0	15	0	2
1	12	1	13	1	6
2	1	2	9	2	3
3	5			3	8
4	4				

Find corresponding physical addresses of the following logical addresses:

a. Address 01001 of P1.
b. Address 00100 of P1.
c. Address 00111 of P1.
d. Address 00001 of P2.
e. Address 00100 of P2.
f. Address 10101 of P2.
g. Address 00010 of P3.
h. Address 11011 of P3.
i. Address 00110 of P3.

a) [9] 4*2+1 = 9
b) [4] 1*2+0 = 2
c) [7] 5*2+1 = 11
d) [1] 15*2+1 = 31
e) [4] 9*2+0 = 18
f) [21] Invalid Page Number
g) [2] 6*2+0 = 12
h) [27] Invalid Page Number
i) [6] 8*2+0 = 16

Answer:
a. 9 b. 2 c. 11 d. 31 e. 18 f. Invalid page number g. 12 h. Invalid page num. i. 16

3. Assume that, page size = 4 bytes and Physical Memory = 32 bytes. If the CPU generates logical addresses 6, 9, 19, 13 and 8 respectively then how can the users' view of memory be mapped into physical memory?

Logical Memory		PMT		Main Memory
P0	abc	P0	6	
P1	def	P1	3	
P2	ghi	P2	7	
P3	jkl	P3	1	
P4	mno	P4	0	

Answer:
Logical address=> Mapped physical address
6=> 14, 9=> 30, 19=> 3, 13=> 5, 8=> 28

4. Assume that page size = 4 bytes and Physical Memory = 16 bytes. If the CPU generates logical addresses 21, 7, 11, 6 and 3 respectively then how can the users' view of memory be mapped into physical memory?

Logical Memory		PMT		Main Memory
P0	abc	P0	2	
P1	def	P1	1	
P2	ghi	P2	7	
P3	jkl	P3	3	

Answer:
Logical address=> Mapped physical address
21=> invalid page number, 7=> 7, 11=> invalid memory address, 6=> 6, 3=> 11

5. During TLB search, the associative lookup time (ε) is 3ns and hit ratio (α) is 70%. For each time memory access, 80ns is needed. Calculate the effective access time.

Answer:
106.1ns (0.7*83)+(0.3*2*80)

6. During TLB search, the associative lookup time (ε) is 5ns and hit ratio (α) is 65.5%. For each time memory access, 200ns is needed. Calculate the effective access time.

   Answer:
   272.28ns

   (0.655*205)+(0.345*2*200)

7. In a system, there are 4 frames in the main memory. In a particular scenario main memory needs to accommodate 16 pages according to the order of the given reference string.

   [1 5 4 3 0 4 7 1 2 9 1 2 7 3 1 7]

   Apply FIFO, LRU and Optimal page replacement algorithms in order to accommodate the pages in the main memory and find out page hit ratio and page fault ratio of every algorithm. Lastly, logically explain which algorithm performs better for the given scenario.

   Answer:
   FIFO=> Hit ratio: 31.25%, Fault ratio: 68.75%
   LRU=> Hit ratio: 37.5%, Fault ratio: 62.5%
   Optimal=> Hit ratio: 43.75%, Fault ratio: 56.25%
   For this scenario, optimal performs better.

   (5/16)*100% = 32.25%