Low power OTA on 28nm CMOS technology

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***Abstract*—Operational transconductance amplifiers are widely used in various applications like BGRs, VCO, VGA etc. In this abstract a power efficient two staged OTA has been proposed on 28nm technology based on miller compensation. It is targeted to have at least a Gain of 50dB and Gain Bandwidth Product of 100kHz with maximum power consumption of 100µW .**

I. REFRENCE CIRCUIT DETAILS

This OTA is made on 28nm bulk CMOS technology. It's a double stage OTA with a differential amplifier at input followed by a common source amplifier as a second gain stage. The targeted design specs are as follows:

S.no	Design Specifications	Target value/range
1	DC Gain (dB)	~50dB
2	GBW	> 100KHz
3	Supply Voltage	~1V
4	Power consumption	< 100µW
5	Phase Margin	~60°
6	Slew Rate (SR)	>0.1 V/µs

II. REFRENCE CIRCUIT DESIGN

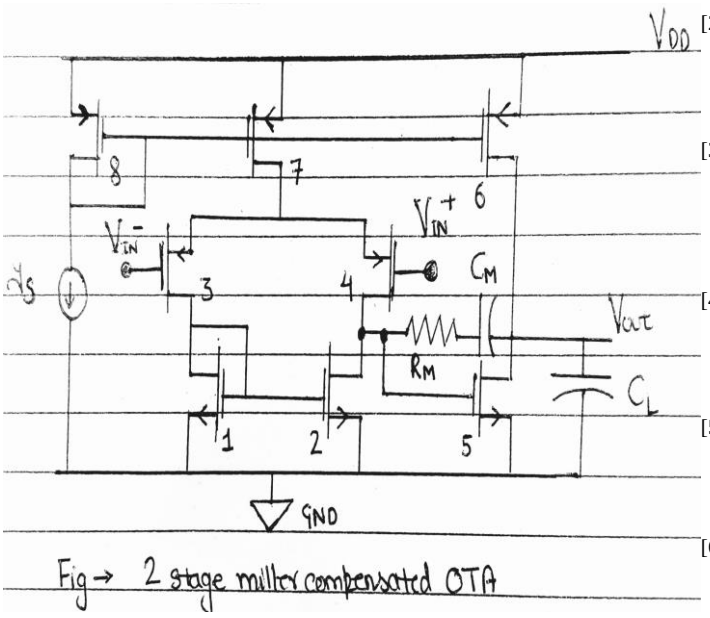

Fig 1: Reference circuit schematic

III. REFRENCE WAVEFORMS AND AREA ESTIMATE

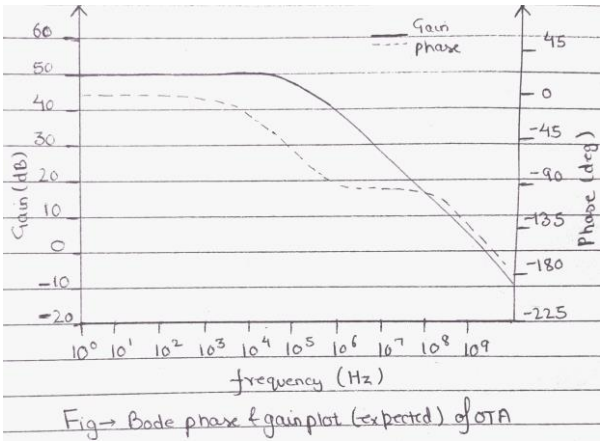

Fig 2: Reference design frequency response

Area Estimation:

Number of Transistors used: 9

Maximum area estimate: <100µm^2.

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