SlugSat Power Amplifier

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Abstract—For future UCSC SlugSat members to use a reference for the progress accomplished in Spring 2018 towards the Linear Transponder's Power Amplifier.

Keywords—Power Amplifier, Class AB PA, Crossover Distortion, Center-tapped Transformers, Operating Point, Power Gain, Efficiency, SlugSat, CubeSat .

1 Introduction

The primary discussion of this paper is a theoretical high-level introduction to SlugSat's Class AB Push-Pull Power Amplifier, its design constraints, design techniques, iterative design process, design results, and necessary design improvements. Overall, this PA design was a **successful** prototype design that met the Linear Transponder's output power requirement of +21 dBm, linearity requirement for CW/SSB communication, and power budget requirements.

2 Motivation

The reason we want to use a Class AB PA is due to our requirements for linearity, output power, power efficiency, and power consumption. For our transponder, the Power Amplifier is responsible for outputting a 19 dBm signal at 29.4 MHz, and only 29.4 MHz. 29.4 MHz is our downlink frequency, and we want to ensure the PA does not produce any other frequency components besides this one so it does not interfere with any other users operating at different frequencies. Therefore, we want this PA to be as linear as possible and not produce any harmonic content. Referring to our link budget, we need to transmit a +21 dBm signal back to the ground station on Earth, such that the ground station will be successfully receive the signal. Since the antenna used for the 29.4 MHz frequency provides around 2 dBi of gain, the PA only needs to output a signal power of 19 dBm. Similarly, the Class-AB topology was chosen to increase the power efficiency of the amplifier, where ideally a Class-AB PA has an Power Added Efficiency η of 50-78 %. According to our link budget, we would also ideally like the PA to consume less than 500 mW.

3 Class AB Push-Pull Power Amplifier

Class-AB Power Amplifiers can be used as either single-stage amplifiers or in a push-pull configuration. Single-stage Class AB PA's experience high distortion, since only the positive half-cycle of the input waveform is amplified and the negative half-cycle is absent. Thus, only half of the waveform is seen at the output. A way to alleviate this problem is to use the PA in a push-pull configuration, where there are now two, ideally identical, transistors instead of one. Their bases are tied to the secondary winding of the center-tapped transformer, their emitters are tied to ground, and their collectors are supplied V_{CC} through the primary winding of the output transformer:

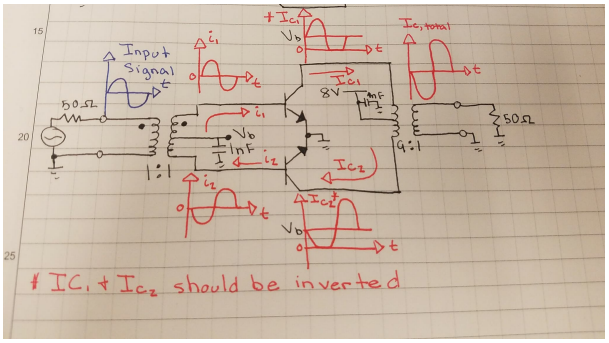

Fig. 1. Class AB Push-Pull Power Amplifier

This push-pull configuration offers high even-order harmonic suppression, minimal crossover distortion at the output, 50-78.5 % theoretical Power Added Efficiency, as well as twice the output power compared to the single-stage amplifier. It's called "push-pull" due to the alternating nature of the transistors, where one conducts for the positive half-cycle of the input waveform, while the other conducts for the negative half.

As seen in figure 1, the input current waveform enters the primary winding of the center-tapped transformer, which then causes a varying magnetic flux to appear in the core. According to Faraday's law of magnetic induction, a voltage is induced in a coil whenever its flux linkages are changing. Therefore, this flux induces a voltage in the N2-turn secondary winding, where according to Lenz's law, the polarity of the induced voltage is such that the voltage will produce a current (through an external resistance) that opposes the original change in flux linkages. Due to the nature of the center-tapped transformer, two current waveforms are produced by the secondary winding that ideally have the same amplitude, but are 180 ° out-of-phase, aka differential signals. These current waveforms then enter Q1 and Q2, which only conduct when the input waveform has a voltage greater than the base-emitter voltage of the transistor. Class AB PA's are biased slightly above each transistor's cut-off region, alleviating the problem of something called crossover distortion.

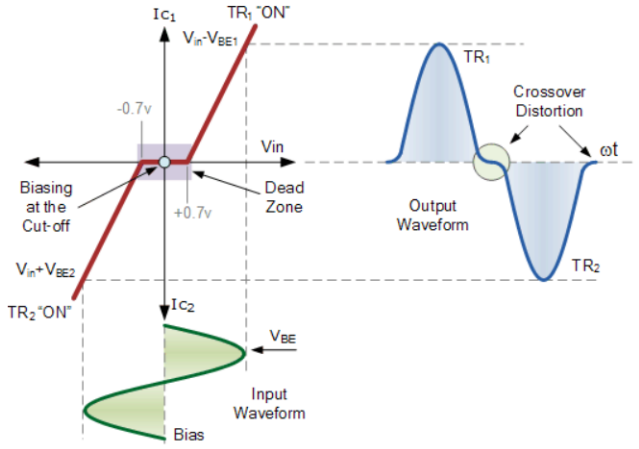

Fig. 2. Crossover Distortion

This crossover distortion seen in the output waveform leads it to becoming an odd-function, which consequently will contain odd-harmonics. Biasing each transistor slightly above cutoff decreases the amount of time that each transistor is off, allowing the output current waveform of the transistor to follow the full positive and negative cycle of the input waveform. This, therefore, reduces the "dead-zone" seen in output waveform leading to crossover distortion, reducing the odd-order harmonics.

Similarly, even-order harmonics should not be present in the output waveform due to the differential nature of the amplifier. Even-order harmonics are in-phase, and when these even-order harmonics produced by each transistor are combined in the output transformer, they should ideally cancel out.

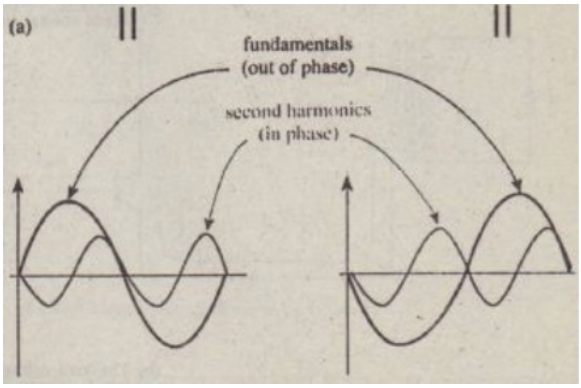

Fig. 3. Second-order harmonics

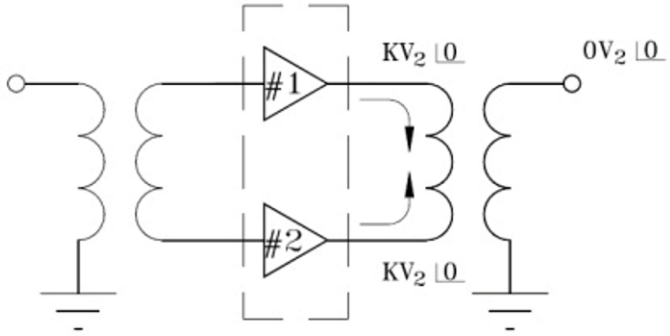

Figure 11 Even-order harmonics cancelled in push-pull amplifier

Fig. 4. Even-order harmonics canceling

4 TRANSFORMERS

The transformer used in this design was a center-tapped transformer:

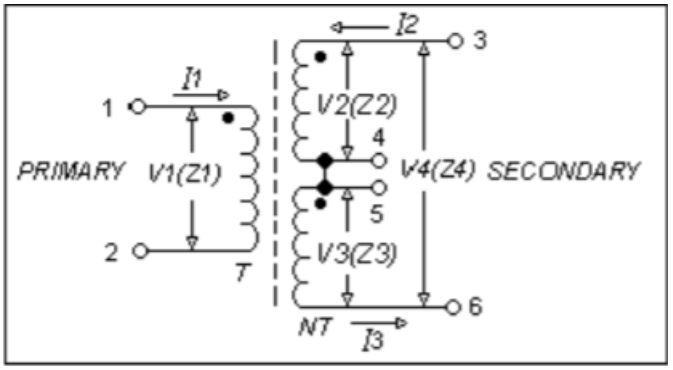

Fig. 5. Center-tapped transformer

These are very useful in transforming an unbalanced signal to balanced, providing excellent

amplitude and phase balance. In Figure 5, with a 1:1 turns ratio provided, signal V2 should have the same amplitude as V3, and they should be out-of-phase by 180 °. They are also useful in rejecting common-mode noise, as well as providing DC isolation between primary and secondary windings.

Similarly, the transformer can be used for impedance transformations:

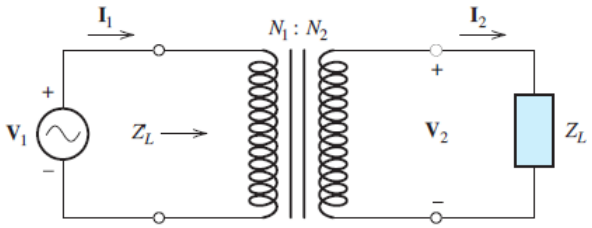

Fig. 6. Transformer Impedance Transformation

The phasor current and voltage in the secondary winding are related to the load impedance by:

$$\frac{\overrightarrow{V_2}}{\overrightarrow{I_2}} = Z_L$$

Rearranging V_2 and I_2 in terms of V_1 and I_1:

$$\frac{(\frac{N_2}{N_1})\overrightarrow{V_1}}{(\frac{N_1}{N_2})\overrightarrow{I_1}} = Z_L$$

Rearranging, we get:

$Z'_L = \frac{V_1}{I_1} = (\frac{N_1}{N_2})^2 Z_L$ in which Z'_L is the impedance seen by the source. We say that the load impedance is reflected to the primary side by the square of the turns ratio. Also, keep in mind that the turns ratio can be used to step up the voltage seen at the secondary winding, which consequently steps down the current, and vice-versa. What's important to note here is that all of the power delivered to an ideal transformer by the source is transferred to the load. Thus, an ideal transformer has a power efficiency of 100 % and neither generates or consumes power.

5 Parts

5.1 Components Used

1) **2N3904** General Purpose Transistor
2) **1N4148** Small Signal Fast Switching Diode
3) **FT 37-43 Toroid**
   a) Wideband Transformers: 5-400 MHz
   b) Power Transformers: 0.5-30 MHz
   c) RFI Suppression 5-500 MHz
   d) AL = 350 ± 20%
4) Remington Industries 28SNSP.25 28 AWG Magnet Wire, Enameled Copper Wire, 4 oz, 0.0135" Diameter, 507' Length, Red
5) Surface Mount Capacitors from Peterson
6) Surface Mount Resistors from Peterson
7) Maxmoral 2PCS SMA Female PCB Panel Edge Mount Plug with 4 Pins Stand Straight Connector RF Coax Coaxial Adapter

5.2 Equipment Used

1) VNA
2) Spectrum Analyzer
3) Signal Generator
4) Power Supply
5) DMM
6) Metcal MX-500S MX-500 Soldering Rework System

6 Design

This section focuses on the different techniques used to approach the final, **functioning prototype**, as well as the remaining work that needs to be completed to get this Power Amplifier out of the prototype phase and ready for integration within the finished Linear Transponder.

6.1 Class AB biasing techniques

6.1.1 Resistor Biasing

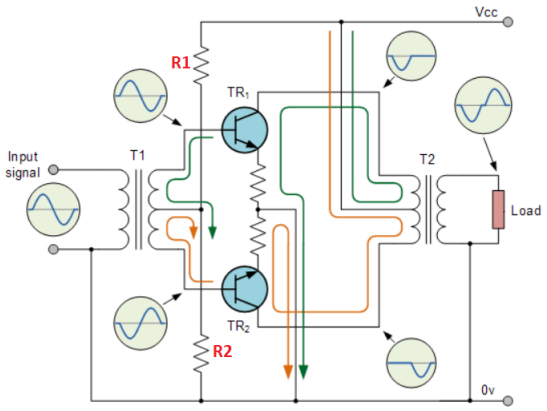

Fig. 7. PA resistor biasing

Biasing resistors R1 and R2 are used as a voltage divider to provide a specific voltage seen at the center-tap of the input transformer T1. Ideally, this should be slightly higher than the base-emitter voltage to ensure that each transistor is

biased above cutoff. This technique would work, but the main concern with this is the operating point's susceptibility to temperature variations. As the temperature rises, V_{BE} will begin to decrease, since the increase in carrier concentration leads to a lower bullt-in potential across the pn-junction. Since we are applying the same voltage at the base, but our built-in potential, V_{BE}, has decreased, our collector current will begin to rise. As the temperature keeps rising, V_{BE} will continue to decrease, and our collector current will continue to increase until it exceeds the maximum power ratings of the transistor and destroys it. This phenomena is called thermal runway, and must be avoided to ensure we have functioning transistors. Therefore, this resistor biasing technique should be avoided.

6.1.2 Diode Biasing

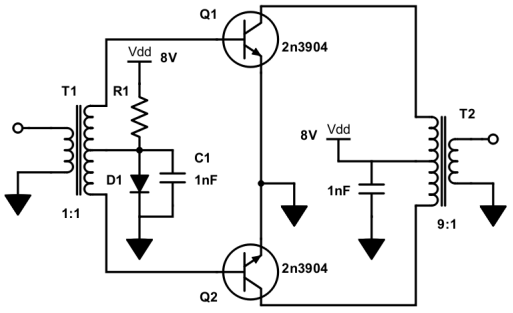

Fig. 8. PA diode Biasing

Depending on the forward current provided to bias the diode, which is dictated by the value of R1 and V_{CC}, the value of the forward voltage will vary from anywhere between 300mV to 900mV, across -40 to +65°C:

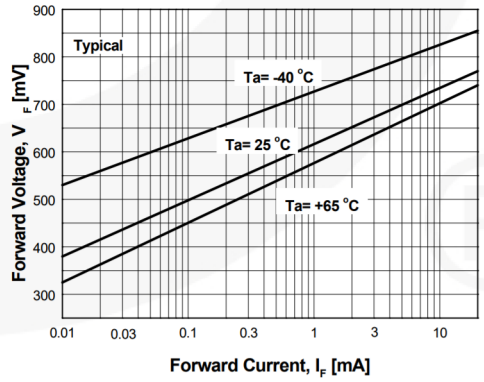

Fig. 9. Forward Voltage vs. Ambient Temperature

This may not seem helpful at first, but let us consider how this may remedy the problem of thermal runway. If we can somehow align this diode's I-V curve to match the V_{BE} - I_C curve of the transistor, then any change in temperature will properly compensate the bias voltage by the correct amount. This can be done by using something called compensating diodes, which can be mounted on the case of the transistors through a nonconductive adhesive that has good thermal transfer characteristics. This allows for each component to heat up similarly, and if the diode's I-V curve matches with the V_{BE} vs. I_C curve of the transistor, then our collector current will always stay constant.

6.1.3 External bias voltage

For debug purposes, both resistor and diode biasing were bypassed, and instead an external bias voltage was directly supplied to the base of each transistor through the center-tap of the transformer. The external voltage was produced using the Power Supply, and the voltage at the base was varied by using the Power Supply. Now, we could have also varied the voltage with the diode method by using a potentiometer as the resistor, but this method was recommended by Professor Peterson so I just stuck with this for my debug measurements. My rationale was that once I found a voltage that gave me the output power that I wanted, I would then revert back to my diode-biasing method and replicate this voltage.

6.1.4 Center-Tapped Transformer

Using either the resistor, diode biasing or external biasing technique, the bias voltage is sent to the base of each transistor through the center-tap on the secondary winding of the input transformer. This transformer was formed using a toroidal core, whose primary and secondary windings were created with magnet wire, which is made from electrolytically refined copper and coated with a flexible insulating surface; this is also known as enameled wire:

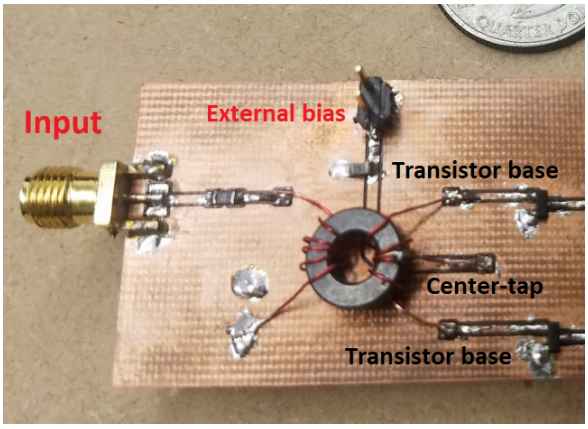

Fig. 10. Input Transformer

Similarly, the output transformer's center-tap was used to provide the voltage rail for each of the transistors, through each transistor's collector terminal:

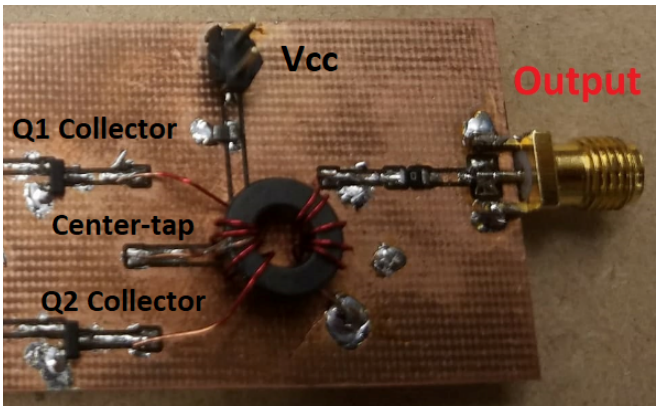

Fig. 11. Output Transformer

6.2 DC Bias of Transistor

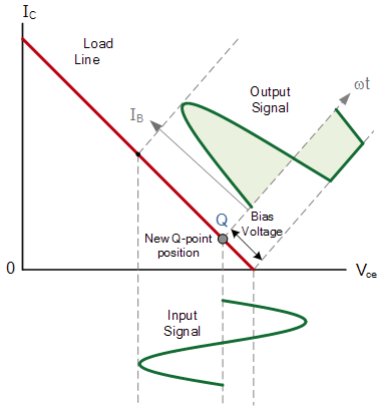

Fig. 12. Class AB AC Load Line

Since our PA is Class AB, we would like to choose a bias voltage such that each transistor is slightly conducting, leading to a small collector current as seen in Figure 13. This bias voltage is used to remove the crossover-distortion seen in Class-B amplifiers as mentioned earlier, achieving higher linearity due to the full positive and negative current waveform present at the output.

Similarly, we also have a power budget that we must keep in mind. Using an 8 volt rail, to ensure that the PA does not consume more than 500 mW, each transistor's collector current must not exceed 31.25 mA, which is a total of 62.50 mA: (8V)(62.5mA) = 500mW. When gauging what value to use for V_{BE} to ensure we do not exceed this 31.25 mA, we must refer to the exponential relationship between the collector current and V_{BE}:

$$I_C = I_s * e^{\frac{V_{BE}}{V_t}}$$

Now usually, when dealing in the small signal regime, you can calculate the transconductance, then depending on your input voltage signal you can determine how much your collector current will change, and then you can predict how much the output voltage will be across a known load, but you can't do that here. We are not dealing with a small-signal input. You begin to deal with large-signals when the peak-to-peak collector current is more than 10% of the quiescent collector current. When applying an input of -2 dBm, and assuming our quiescent collector current to be around 4mA (V_{BE} $\sim$ 700 mV), and the transistor's thermal voltage to be 26 mV, then the g_m is 0.153. The peak voltage of a -2 dBm signal is approximately 251 mV. G_m tells us how much our collector current varies with our V_{BE}, so with a peak voltage of 251 mV, and a g_m of 0.153, our collector current will change by:

$$\triangle I_C = g_m * V_{in}$$

$$\triangle I_C = (0.153)(251mV)$$

$$\triangle I_C = 38.4mA$$

This is most definitely more than 10% of our 4mA quiescent current, therefore we can no longer apply our small-signal performance techniques. And yes, you can may question whether this calculation is even valid since g_m is a small-signal characteristic, but I think it is still applicable because it still tells us how much our collector current will change, regards of the input being a small-signal or not.

Similarly, the best way I went about measuring the performance of the PA under large-signal behavior was measuring it experimentally. This is the main reason why I used an external bias voltage, so I could easily control the value of the base voltage, measure the collector current, calculate total power consumption, and measure the output power on the Spectrum Analyzer. I felt this was the fastest and efficient way, instead of staying stuck in simulation land for all of Spring Quarter.

6.3 PA with Emitter Degeneration

6.3.1 DC Analysis

I initially began my design by using the diode biasing technique, and noticed that the collector current was very sensitive to any changes in V_{BE} (obviously). I then pondered another way to control the collector current so that it would be more stable, and that led to my decision of adding the emitter resistor. If I chose to select the emitter voltage around 1V, for example, due to the built-in potential across the base to emitter, I would expect around 1.7 V seen at the base. If I place 1.7V at the base, then due to the voltage drop across the diode, there is around 1V left after the diode that is just tied to ground:

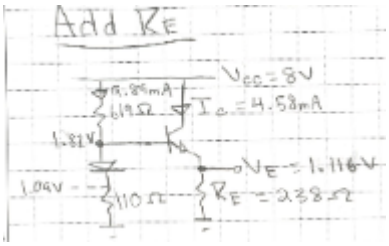

Fig. 13. PA with degeneration

Because there is no other voltage drop for KVL to be completed, this 1V tied to ground will cause a short which will spike the current used to bias the diode to dangerous levels. To prevent this, another resistor had to be added to complete the KVL loop:

Once this was taken care of, then the emitter resistor can be chosen to produce the selected collector current. However, since the emitters are tied together for both transistor, the emitter current must be twice the expected collector current. If I wanted my collector current to be around 4mA, then my emitter current must be 8mA; moreover, setting the emitter voltage to 1V, the exact resistor value can be found to produce this 8mA of emitter current by using Ohm's law.

Similarly, it is important to note that this is all possible because when we have a high DC current gain, which is β, the emitter current is approximately equal to the collector current:

$$I_E = I_C(1 + \frac{1}{\beta})$$

where β can be assumed to be 100.

6.3.2 Impedance Matching

Once I completed the DC analysis of my transistors, I then moved onto impedance matching the input and output to 50Ω, since as a team we agreed to 50Ω to perform modular testing in the future.

I first wound up both input and output transformers with about 5 turns on the primary and secondary, so that each transformer had a 1:1 ratio. I then began my first prototype using the dead-bug technique, and ensured that the power supply was on before I used the Vector Network Analyzer (VNA) to begin measuring the input/output impedance.

I also made sure that when measuring the input impedance, the output impedance was terminated with the proper 50Ω termination, and vice-versa with the output impedance:

My general approach to using the transformers as impedance transformations was to first measure the input/output impedance with a 1:1 turns ratio, and then begin to adjust the windings in the primary or secondary to bring the real part of the input/output impedance as close as possible to 50Ω. Once I had the real part of the input/output impedance down the 50Ω, I could then use either a capacitor or inductor to cancel out any stray reactance.

For example, through trial-and-error, using a 1:3 turns ratio at the input transformer, I was able to measure an input impedance of 45.7 - j62.5Ω. To cancel out this stray reactance, we can use an inductor which has a reactance value of +62.5Ω at 29.4 MHz:

$$X_L = j\omega L$$

$$L = \frac{X_L}{\omega} = \frac{62.5\Omega}{2\pi(29.4MHz)} = 338nH$$

Although I could not exactly find a 338 nH inductor, I found a 307 nH inductor, which was placed in the circuit as such:

This then lead to an input impedance of **50 - j7.254**Ω

A similar approach was taken with the output impedance, and using a 1:3 turns ratio again I was able to bring the output impedance to equal 54.1 + j25.4Ω. In this case, we need a capacitor that has a reactance of -j25.4Ω at 29.4 MHz, which was equal to 210 pF. Although a 210 pF cap wasn't found, a 220 pF cap was used an consequently led to the output impedance of **56 - j0.113**Ω

6.3.3 Performance

Now that both input and output impedances are matched to 50Ω, a CW tone of -9 dBm at 29.4 MHz was sent to the input of the PA, and the output power and power consumption were measured:

With this topology, I was seeing P_{out} **= 2.6 dBm**. This equates to a **total Power Gain = 11.6 dB**. This is not exactly what we desire...and the reason for such a low gain is mainly due to the emitter resistance being used, which lowers the overall gain of the PA. A more detailed explanation can be found in my engineering notes on page 9, but the conclusion that I drew from this was to remove the emitter resistance and move forward with a different topology to boost my overall power gain.

PA without Emitter Degeneration

Once the emitter resistance was removed, I saw a substantial increase in gain once both input and output impedances were matched to 50 Ohms, since I had to recalculate both impedances for the new topology. The iterative approach can be found in pages 10-25 in my Engineering Notebook.

By varying the base voltage from 680-722 mV, I was able to achieve a Total Power Gain of **16.6 - 22.4 dB** with an RF input of -9 dBm. This equates to a total output power varying from **7.6 - 13.4 dBm**. However, to keep the power consumption less than 200 mW, a conservative 710 mV needs to be applied to the base of the transistor (please see page 25 in Engineering Notebook). With 710 mV placed at the base, the output power is 12 dBm.

This, unfortunately, is not close to our desired 19 dBm output, and if we try to increase the base voltage to increase our output power, our collector current begins to rise exponentially and will cause damage to the transistor.

To mitigate this problem, we need to include a driver amplifier that will precede the PA, in order to boost the input power to the PA such that the PA will be capable of outputting the desired 19 dBm.

6.4 PA with Driver

The topology used for the Driver stage was our LNA block, since it consumes minimal power, and is capable to output a 0 dBm signal for the PA to achieve the required 19 dBm. Using the same topology as above, with an input signal of 0 dBm, and varying our base voltage from 690-710 mV, our total output power now varying from **19.2-20.1 dBm**. Using a base voltage of 706 mV, the total output power was 21 dBm with a total power consumption of 240 mW. This is superb since we anticipated that the PA was going to consume 500 mW, and this is half of that.

However,it seems that our transistor was compressing at this point because with in an increase in RF input, our output power would not go higher than 20 dBm. We need to back off away from this compression point, and I therefore decreased the requirement of the input power to the PA by 2 dB.

With an RF input of -2 dBm, our RF output was 18.7 dBm and there was a total power consumption of 240 mW:

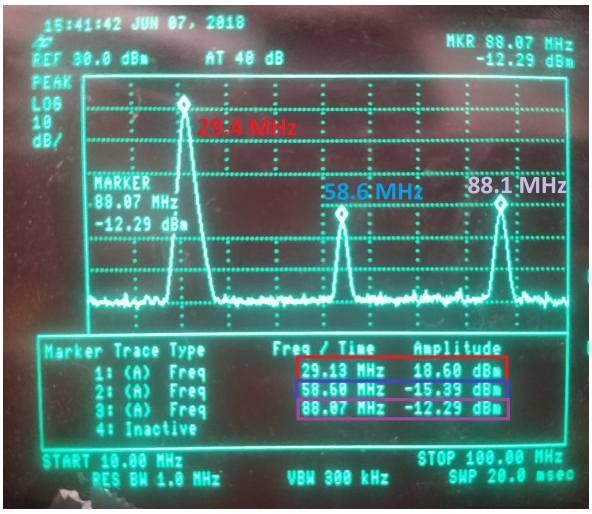

Fig. 14. PA with 18.6 dBm Output Power

6.5 PA Spectrum

Due to our linearity restraint, although our PA is able to produce the 19 dBm output power required according to our link budget, we must maintain minimal harmonic content. Looking at Figure 14, we can see that our second harmonic HD2 has a power of 37 dBc, and our third harmonic HD3 has a power of 32 dBc. We need these harmonics to ideally be non-existent, but as explained earlier

these harmonics will be inevitable due to the non-ideal characteristics of the transformers and our bias voltage being applied creating some crossover distortion.

To mitigate this problem, a filter must proceed our PA to clean up its spectrum. A 3-pole Chebyshev Low Pass Filter was used, mainly because it provided minimal insertion loss while still providing 16 dB and 29 dB of attenuation to both HD2 and HD3 respectively:

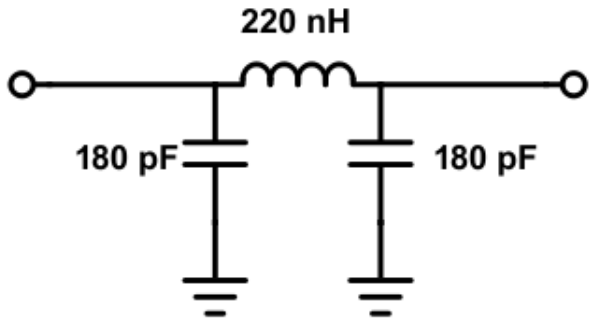

Fig. 15. 3-pole Chebyshev Low Pass Filter

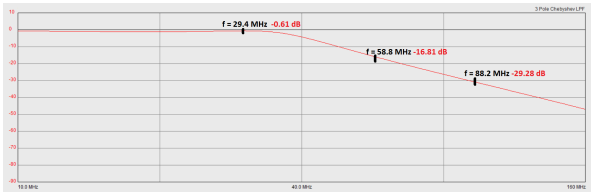

Fig. 16. Simulated Frequency Response of LPF

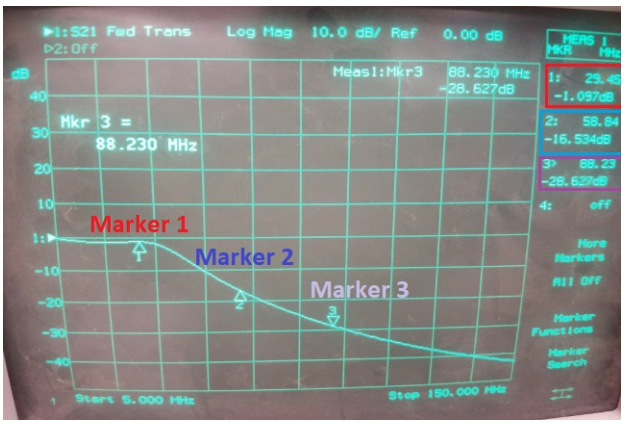

Fig. 17. Measured Frequency Response of LPF

Please see page 42 in my Engineering Notebook for better pictures.

Once this LPF was created, it was cascaded with the PA and the output spectrum looked like such:

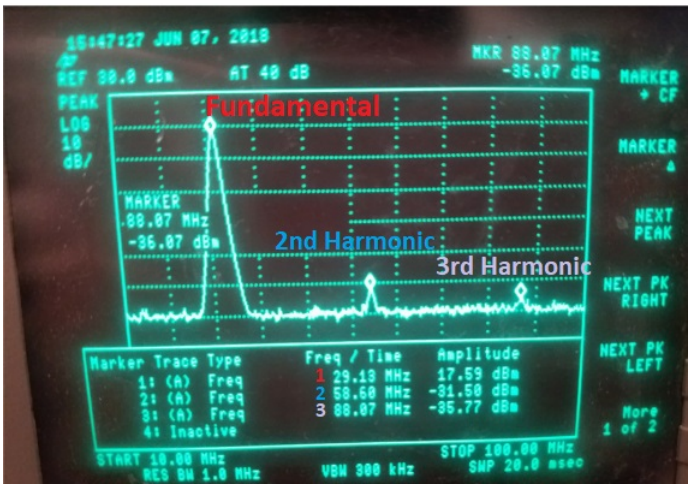

Fig. 18. Frequency Response of PA with LPF

For a table listing HD2 and HD3 powers please see page 48 in my Engineering notebook.

Conclusion

The next steps that need to be taken would be to replicated the design above but by using the diode biasing technique instead of using an external voltage supply, as I did for debugging purposes and proof-of-concept. Once this is done, a PCB with both PA and LPF needs to be created , since I had made two separate PCBs for these blocks and connected them together with male-to-male SMA connectors. Once the results of this board matches with figure 18, then the next thing would be to reduce the form factor of the PCB by buying all surface mount components, such as transformers and inductors, since these were not surface mount. Then, we can integrate each block of the linear transponder and measure its overall performance. Further debugging will be involved at this point since we have not yet integrated all blocks to measure the performance of our ”flatsat”.