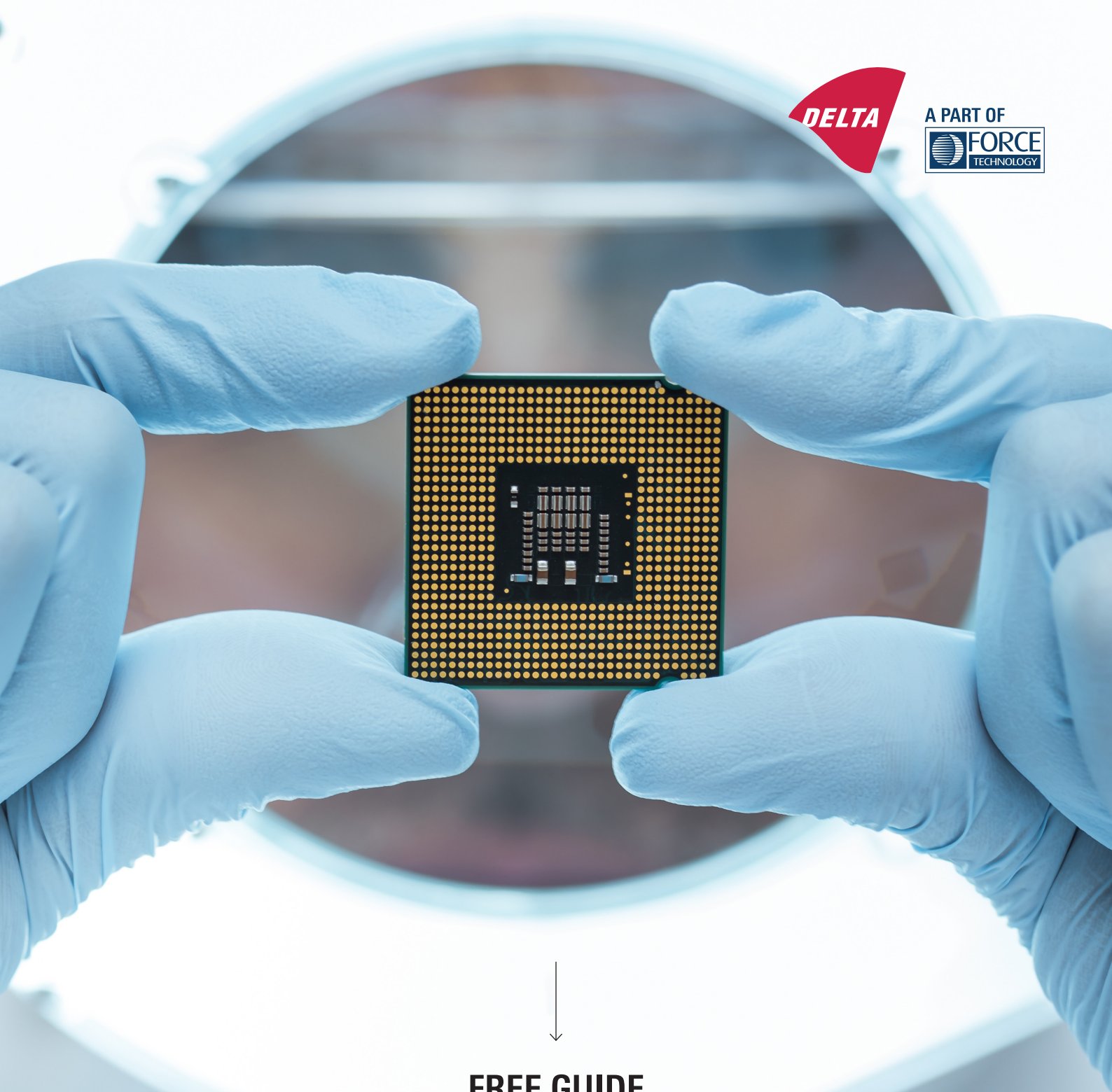

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FREE GUIDE

The Ultimate Guide for Selecting an ASIC Package

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Introduction

Semiconductor chip package technologies have evolved throughout the years to the point where hundreds of package types are available today.

Most applications will require the more general, single-element packaging for integrated circuits and the other components such as resistors, capacitators, antenna etc. However, as the semiconductor industry develops smaller and more powerful devices, a 'system in package' (SiP) type of solution is becoming the preferred choice, where all elements are placed into a single package or module.

While package types can be easily categorized into lead-frame, substrate or wafer-level packages, selecting a package that will suit all your requirements is a bit more complex and requires evaluating and balancing the application needs. To make the right choice, you must understand the effects of multiple parameters like thermal requirements, power, connectivity, environmental conditions, PCB assembly capability and of course, cost.

This paper presents seven different key requirements that need to be evaluated to enable the selection of a suitable packaging technology.

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Common Packaging Technologies

Package technologies have evolved throughout the years to the point where today there are a multitude of package types available, using different connections and assembly methods. This paper focuses on four of the most common packages used today: BGA, QFN, WLCSP and eWLB.

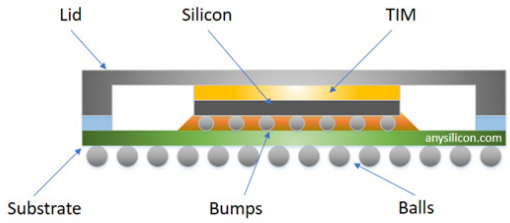


Image source: anysilicon.com

BGA (Ball Grid Array) is a packaging option that is popular for ICs that require a large number of I/O connections. BGA advantages include low inductance and good heat dissipation options. On the disadvantage side, inspection and fault detection is more difficult, and the cost may be higher compared to other packages such as QFN.

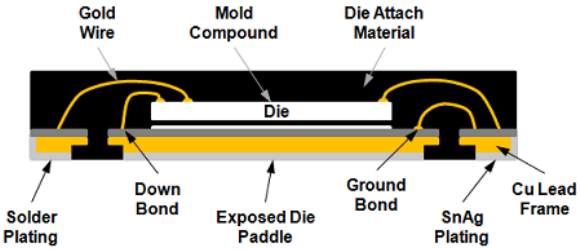


Image source: mentor.com

QFN (Quad Flat No Lead) is one of the most popular semiconductor packages today due to its low cost, small form factor and good electrical and thermal performance. The downsides of QFN include low pin count, potential oxidation problems and reliability in long-life, severe environments.

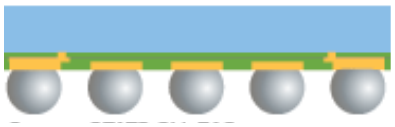
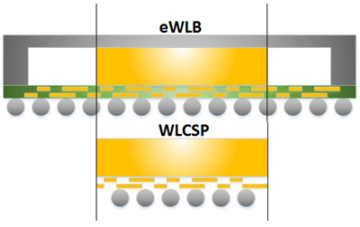


Image source: statschippac.com

WLCSP (Fan-in Wafer Level CSP) is essentially a bumped die, and therefore offers the smallest possible package size, as it will be the same size as the die. WLCSP offers reasonably low cost, small size, and good electrical performance but maybe less suitable for high-pin count applications.



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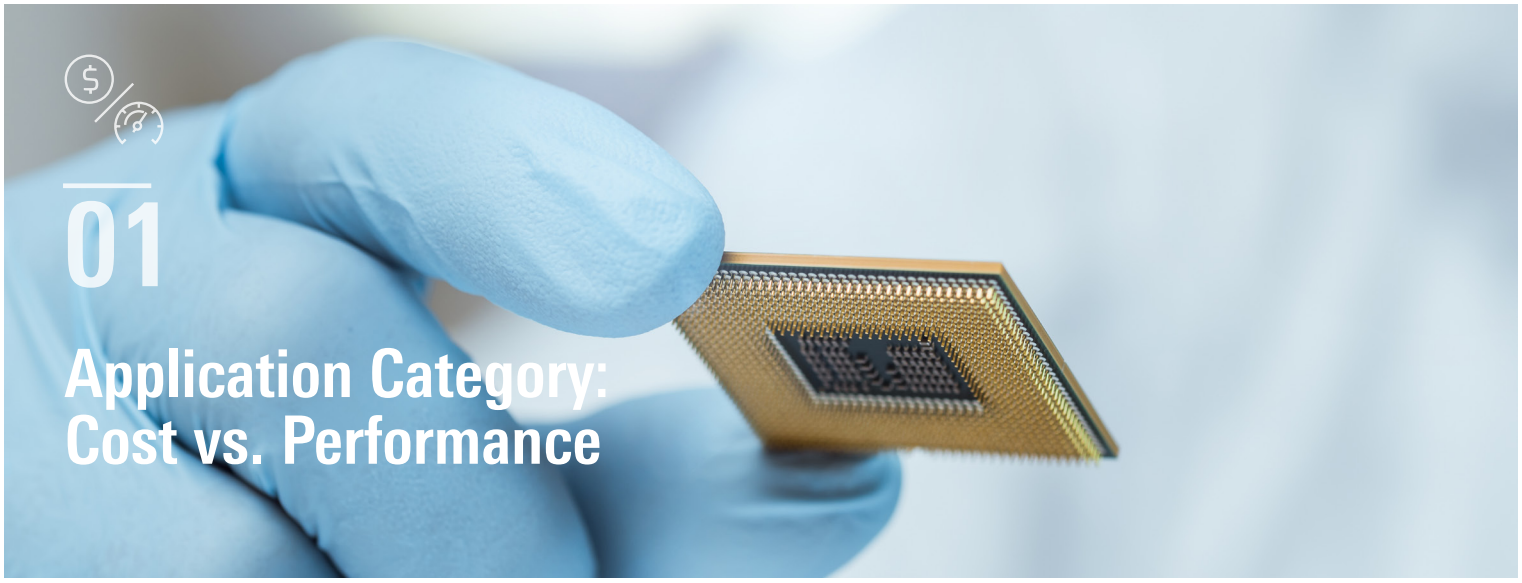
eWLB (Embedded Wafer Level Ball Grid Array) uses an interposer wafer under the original wafer to allow fan-out and more space for interconnect routing. This creates a larger die area and solves interconnect problems of WLCSP. eWLB is becoming the preferred choice when used with consumer and wireless ASICs.



01

Application Category: Cost vs. Performance

Your target application is the primary driver dictating your package selection. Is your application environment? Will you develop a System on Chip or will your ASIC be a key component within the system?

Such questions will help you decide on the type of packaging – whether you can you use wafer-level or chip-size package, or can standard, more readily available BGA or QFN type packaging be more relevant.

Application performance requirements and the corresponding packaging options can be broadly categorized into three groups:

High-end application requirements are often related to high-speed, high-power chips that have a large number of connections (high pin-out). These devices will require advanced packaging requirements to match the needs of small pad pitch, high-speed signals and decoupling, that can be achieved with the FC-BGA (flip chip BGA), or newer packaging like embedded Wafer Level Ball Grid Array (eWLB).

The **Mid-range** group typically require packaging that can address thermal enhancements and employ cost-effective plastic packaging technologies – often in the BGA and QFN type approach. At the higher end of this group are chip level and wafer level packaging, suitable for system in package and/ or multi-chip module packaging.

The **Entry level** group includes high-volume applications where cost is the main driver rather than performance. Devices for notebook and mobile applications, for example, will generally require small size wafer level and chip size packaging.

02

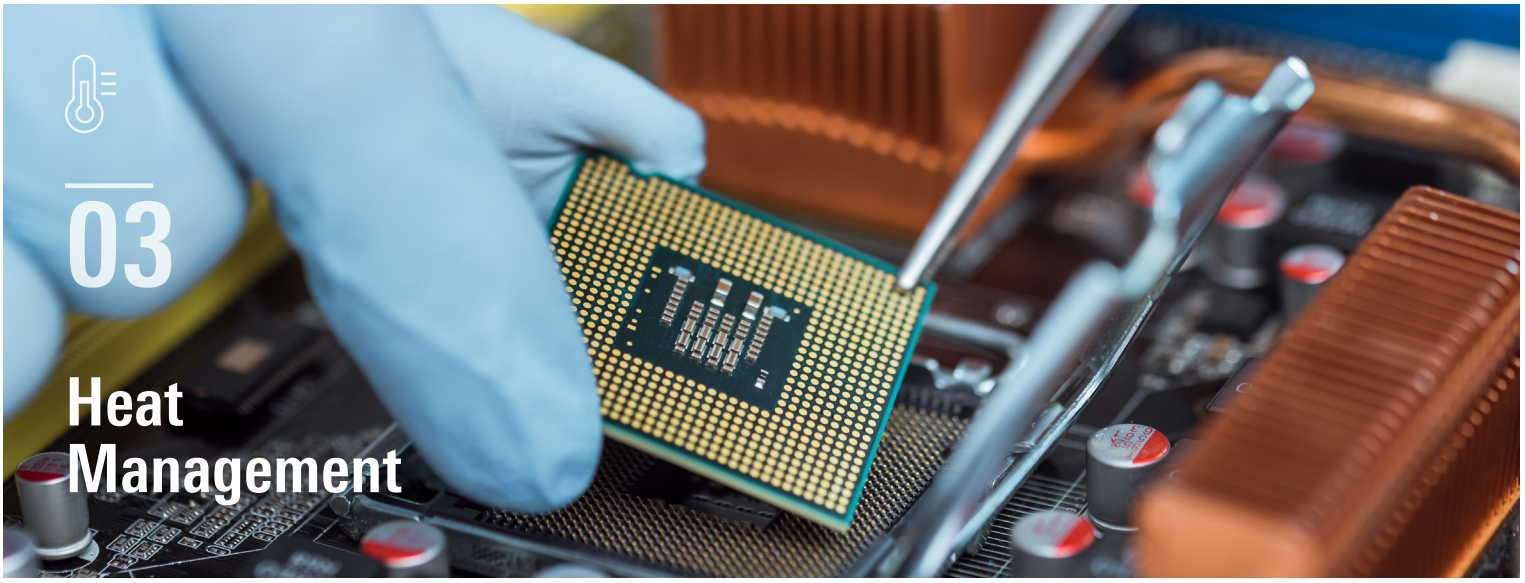
Number of Pins and I/Os

The number and location of input and output connections of any device are key factors to be considered when determining the package requirement. In addition the type of interconnect as in power connections, high speed data inputs and outputs, ground connections and control and monitoring signals need to be clearly identified and related to chip and package layouts.

High pin count. If you're looking at a very high pin-count, say 1000 pin package, then your best option may be a standard BGA package, which offers such I/O capability as overall package size can go up to 50-60 mm square.

Low pin count. For a low pint count, say 50 pins your choice would probably be a QFN or WLCSP package. However, a WLCSP will have limitations for heat dissipation within the package. In cases where there is heat generation (e.g., fast switching) or need for good signal grounding, then a QFN is the better package choice, due to the 'built-in' metal base pad.

Layout. Another parameter is the location of I/Os. If the I/Os are on the periphery around the die, then wire bonding is quick, easy and reliable provided there is enough surface area in the die and package pads for this. If the I/Os are spread across the surface of the chip in different areas, so that wire bonding out from the center of the chip is difficult, then flip chip packaging offers a direct attach approach onto the substrate of the package, which is usually a multi-layer PCB, and there would be no concerns about the die overlapping.



03

Heat Management

Advances in silicon technology are continually producing chips that are smaller and faster, which means they are also creating more heat. Consequently, thermal management is a key packaging factor for optimizing chip performance.

Heat management ensures the reliability and enduring operation of the chip. For example, interconnections - like the die attach material, wire bonds or Flip Chip balls – are far more reliable if temperatures are kept down. For example, if an ASIC chip is placed on a substrate using epoxy and then the temperatures run too high, the epoxy will soften and possibly melt, allowing the ASIC to physically move, causing the package to become unreliable. Excessive heat may also have a negative effect on RF frequencies and reduce device performance.

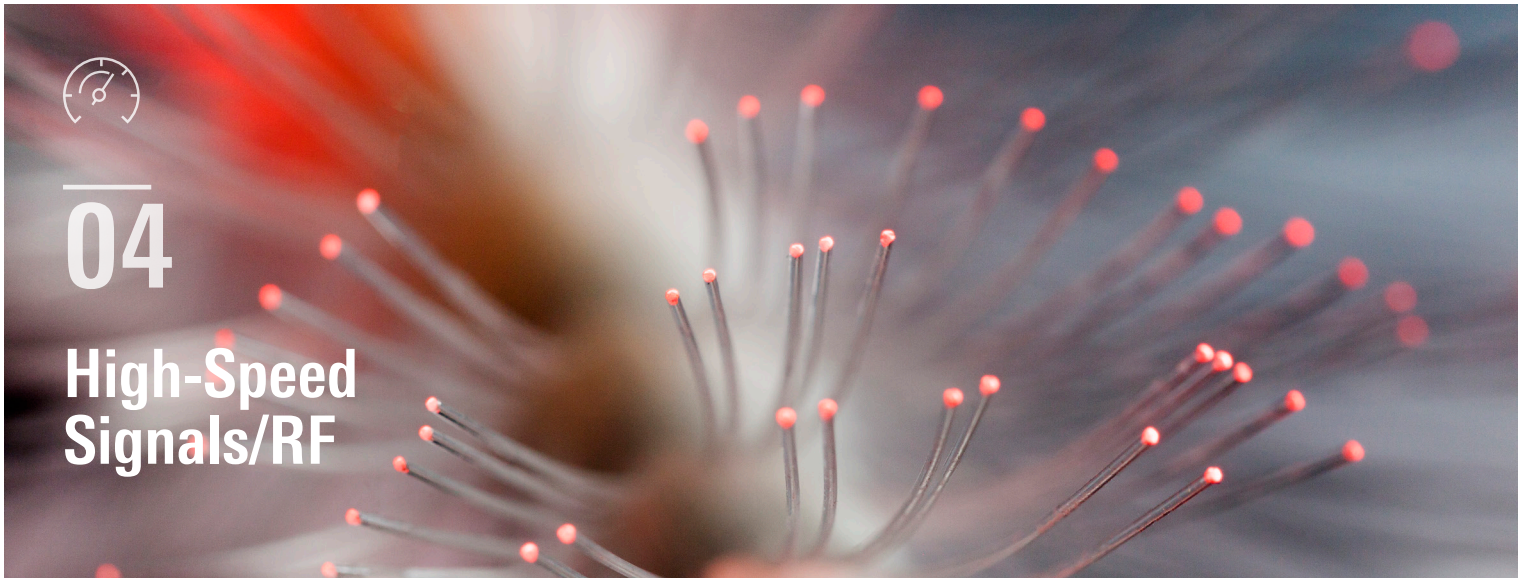
Heat management is also a cost factor – depending on the type of device and package selected. Various heat dissipation processes and methods are associated with different package types. A BGA package, for example, can often offer lower cost/improved thermal management solutions within the package because of its size, as it has a larger area available to dissipate the heat. The smaller real-estate chip tends to create a thermal environment that can be more expensive in terms of the thermal management solution, requiring an external heatsink or other cooling options.

BGA packages have options with both thermal pads, such as conductive vias or inbuilt metal base plates that can enable adequate heat management. Some options of thermally enhanced BGA packages can have a metal cap built onto them that establishes a thermal conduction path between the IC device and the metal cap, which provides good heat dissipation.

QFN packages are designed such that they have a solid metal die pad as the base of the package, to which the die is bonded. This enables very good heat dissipation from the silicon die through to the PCB.

Die attach materials. Bonding the chip to the substrate with a thermal conductive adhesive like Sliver filled Epoxy, rather than plain epoxy, will help remove the heat. In addition, newer technologies are available like Silver sinter technology – an interconnection method with high operating temperature, high thermal and electrical conductivity. These materials typically work well in QFN packages, but are not as effective in BGA packages, due to the package construction.

Chip size and wafer-level packaging. Thermal management in these packages is primarily done on the back of the chip, or in chip size package, on the exposed top-side of the chip.



04

High-Speed Signals/RF

RF, wireless and high-speed digital designs have specific requirements that affect package selection. The signal speed and the frequencies can be significantly degraded by the parametric effects of the interconnections within the package.

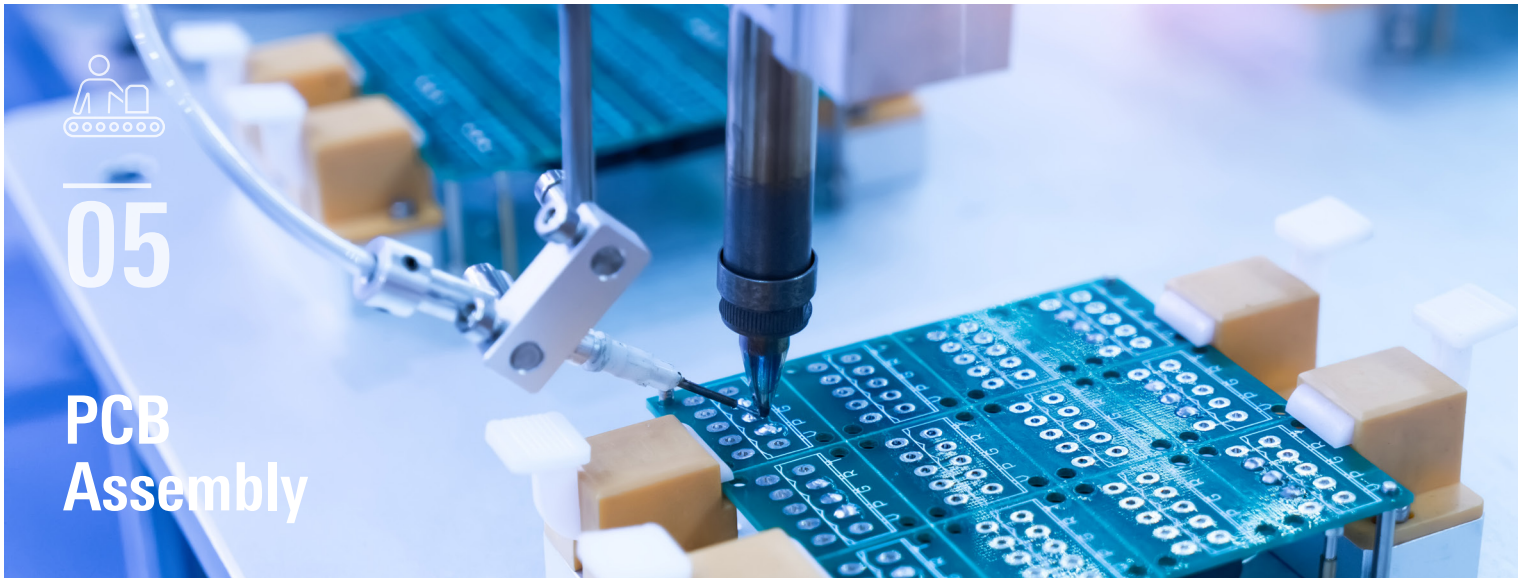
Wire bond vs. flip chip. In RF devices, key design considerations involve inductance, capacitance and resistance, which are affected by the speed of the signals travelling in and out of the device. These issues also impact package selection, primarily between flip chip and wire bond interconnections. Flip chip will provide better RF Performance and enable reaching higher frequencies with lower inductance. Wire bonds, on the other hand, can add a randomly-variable inductance at each RF input or output at higher frequencies.

Package layout. At RF frequencies, signals travel along the surface rather than in the conductor. Hence, the way in which the package is assembled has an important effect on the device. For example, high-speed amplifier chips, RF transistors, and diodes often cannot be put into a "standard" plastic package, as the encapsulation materials affect the speed in which the chip operates. Consequently, such chips should go into a cavity QFN or BGA package.

High frequency signals (1 GHz and above) are likely to require the layout of the interconnections to have isolated signal paths, known as "ground signal ground" interconnect. Here the requirement of two ground connections for every signal i/o will impact the package size and layout.

Additionally, with high-speed ASICs, the signal levels and timing will be affected by the length of the conductor that they travel along. For example, if you are using a BGA package and you have a longer lead to one point and a shorter lead to the next, you will have timing differences on the signal. This must be overcome by putting more consideration into the initial design of the package substrate to accommodate the high-speed RF devices.

BGA substrate dielectric materials are also a key factor in RF chips. For example, a high-performance liquid polymer substrate, like Rogers laminate, is better suited than the standard FR4 PCB material for use as the substrate for BGA packages used for RF designs.



05

PCB Assembly

PCB assembly and the method of connecting the packaged ASIC chip to the circuit board requires several processes that can impact reliability and should therefore be taken into consideration in advance when deciding on an ASIC package.

Depending upon package type chosen, you would need to ensure you find a provider with the right PCB assembly processes to ensure that your finished project is of the highest quality. Advanced package assemblies cannot be handled by just any electronic manufacturing service company. The choice should be one that is able to accommodate the fine pitch and both small and large package sizes.

For example, chip size packaging, wafer-level packaging and of course, bare die flip chip require a process of heat and pressure to attach them directly to the PCB. The assembler will therefore require the use of advanced PCB assembly capabilities to enable handling for accurate location and a suitably advanced process to ensure that these small size parts are reliably attached to the board.

If, on the other hand, the package is for example a high I/O Ball Grid Array (BGA) package with a small ball pitch (say, 0.5mm or smaller), the process will require a high-quality PCB assembly capability, with highly accurate alignment and specialized soldering processes in order to yield a reliable and robust outcome.

QFN packages provide many benefits, but they also pose several significant manufacturing and reliability concerns at PCB level, so they also require more specialist processes for the assembly. Due to the package having a metal "slug" base with peripheral contact pads, the assembly process is prone to create defects such as shorts, voids, opens, and fill deficiencies, and the issue of void formation becomes even more of a challenge when combined with a lead-free soldering process.

06

Environmental Considerations

Specific environmental or mechanical needs tend to determine the type of package required for the application. Consumer products have the simplest requirements (see table below) as the package tends to be driven by cost, rather than environment. Plastic package options are preferred but even here, shock and vibration resistance needs are a limiting factor for the types available.

However, if the application and the system chosen require protection from moisture or chemical effects, as in many medical and aerospace applications, the need for package hermeticity is the driver. In such cases, the only option may be to use a specific type of package, such as a hermetic metal or ceramic package, to protect the ASIC device.

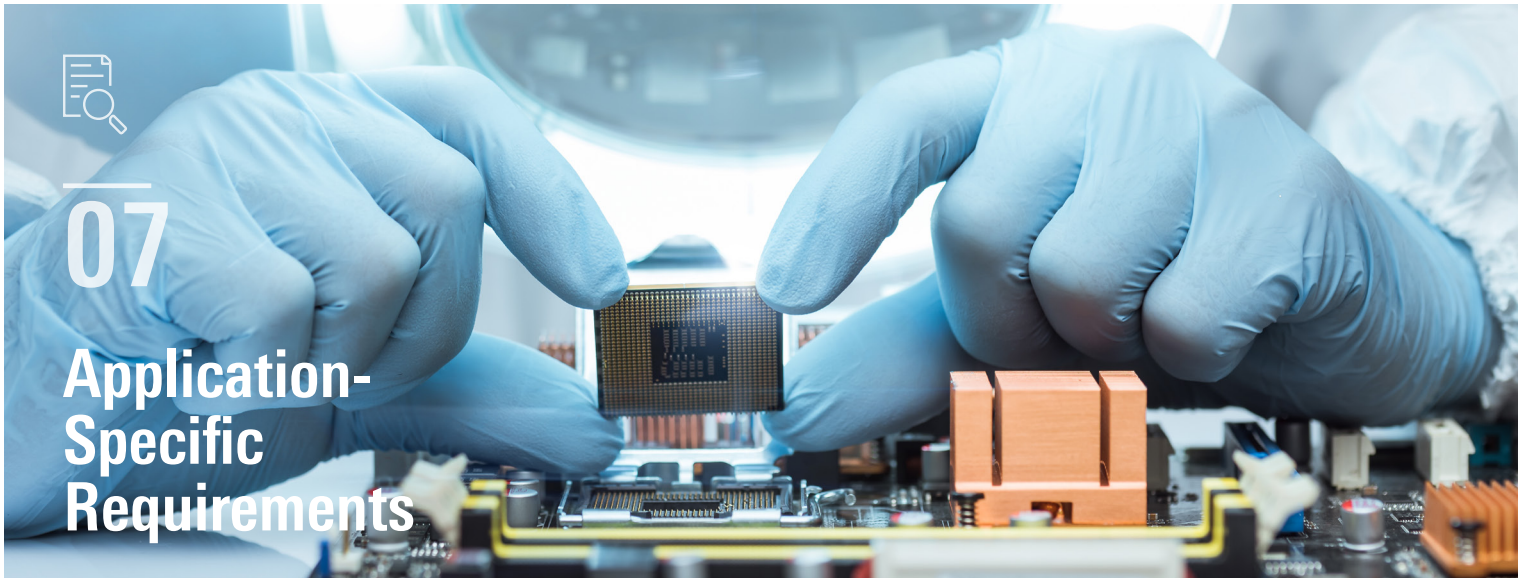
In Automotive applications packages need to withstand levels of temperature, vibration and shock which are now on a level with Defense and Aerospace requirements (See MIL Standards). Nevertheless, since cost is a key driver in Automotive, the industry has improved the performance of standard packages enabling the acceptance of QFN and certain BGA types of parts.

In the space industry, high-speed, low-cost ASIC devices are needed for next generation space capsules and satellites. Here, the applications require packaging that is low-cost and lightweight but can also withstand high G-force, mechanical shock, and pressure. A potential solution may be a plastic package, although these types are not hermetic. The need is driving these applications to look at new ways of sealing the complete systems to overcome the package deficiencies.

The table below provides examples of some environmental requirements in different industries and some potential packaging solutions.

	Consumer (Mobile device)	Automotive	Medical	Defense/aerospace
Temperature	-10° to +85°	-55° to +125°	-10° to +85°	High/rapid temperature shifts
Vibration & mechanical shock	•	•	•	••
Moisture ingress		•	•••	•
Hermeticity		•	••	•••
Thermal management	•	••		••
Chemical resistance		•	••	•
Radiation proof				••
Package options	QFN, BGA, WLCSP, eWLB	QFN, BGA, WLS+CSP	QFN, BGA, WLCSP, eWLB	QFN, BGA, eWLB

• Needed •• Important ••• Critical



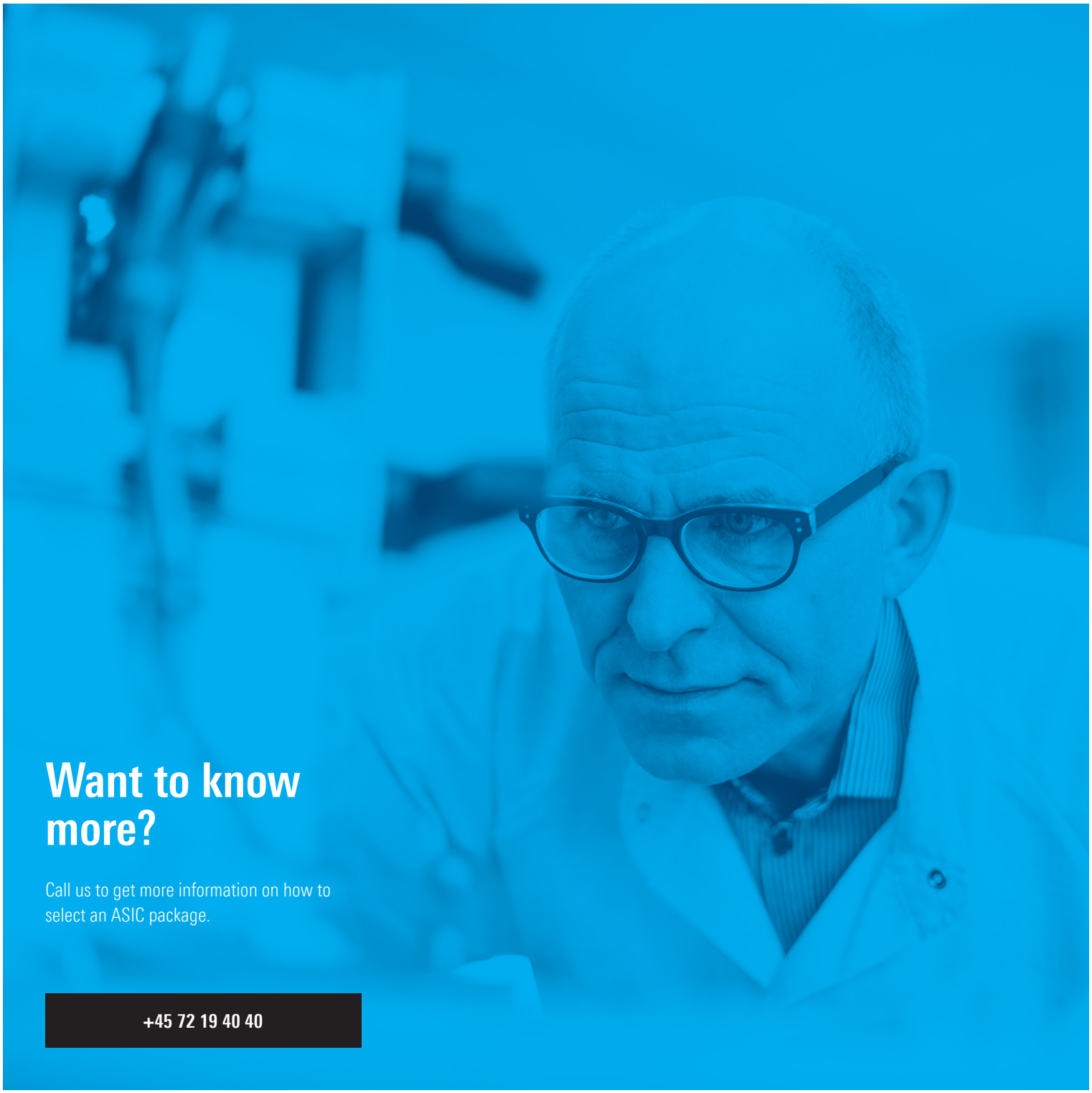
07 Application-Specific Requirements

In most cases, the specific application requirements will dictate the package type and form factors. Yet many new applications, such as hand-held devices, next generation ASIC devices with wafer level features such as Through Silicon Vias (TSV's) may make a package unnecessary. In such cases, a direct die attach/ flip chip process will be undertaken.

ASICs often support functional devices such as sensors and LEDs, where the package is not a standard of the type discussed above, but the package, or housing of the electronics must fit into a specific shape and space defined by the application. Typical applications in Automotive, Aerospace and Industry may adopt this approach. For example, the ASIC chip might need to fit into a specific space, such as a power module or into a sensor control system housing.

In other cases, such as when building an automotive module, a System in Package (SiP) may be used, bundling multiple ICs into one overall package along with peripheral devices. Here, custom ceramic package's such as Pin Grid Arrays or metal can module packages may be used.

Next generation SiP and emerging applications are now considering using three-dimensional package technologies such as Molded Interconnect Devices (3DMID) and 3D multistack units, which are all custom designs for application specific solutions.



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