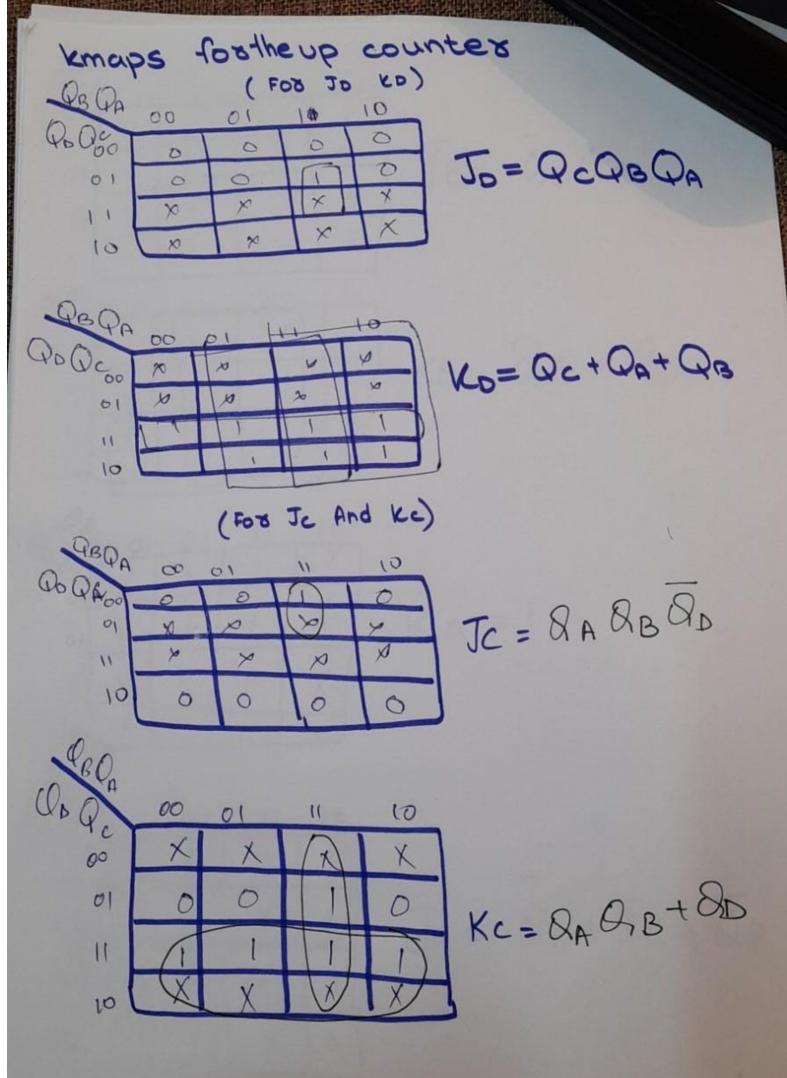
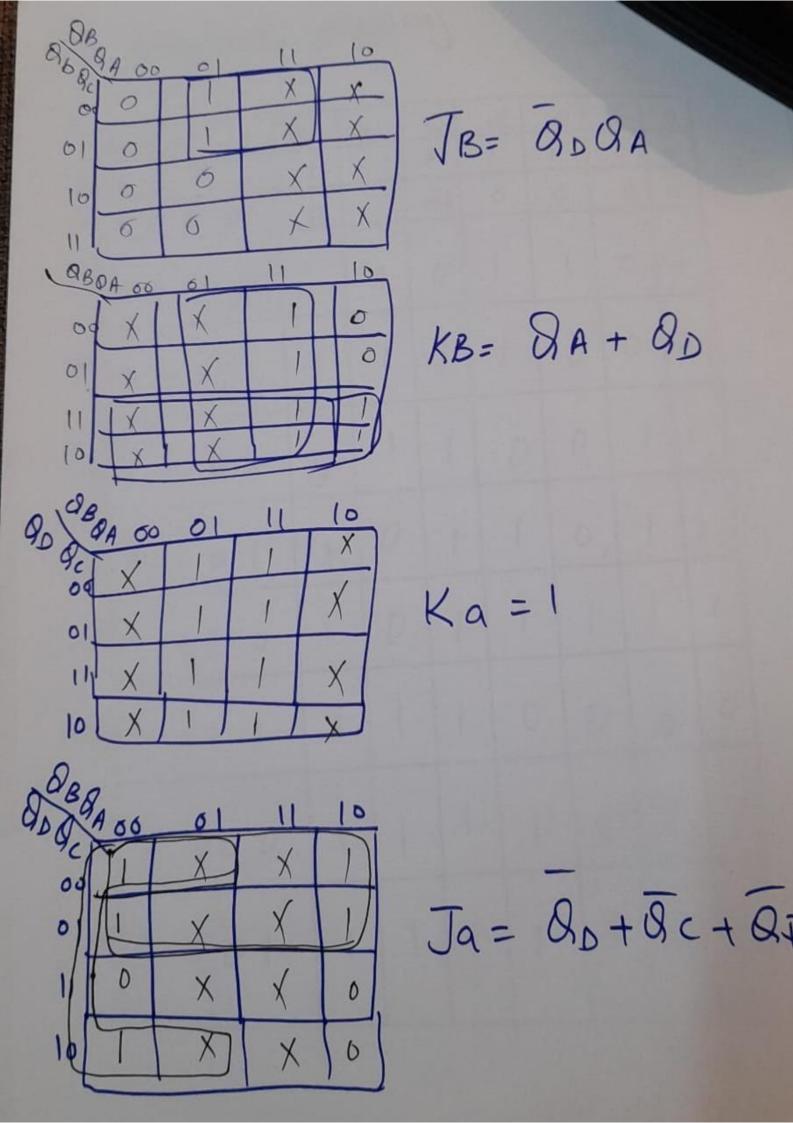
DLD Project Alasm Clock

4- bit up counter (synchronous) working for the clock

Present state, Next State, Jo Ko Jc Kc JB KB JA JA															
200	DA	c QB	QA	Q,	sext	- Ci	is Qa		X	0	×	0	X	,	X
0	C			0			0	0	×	0	×	1	×	×	1
0	0	1	0	0	0	1	١	0	×	0	×	X	0	1	1
0	0	1	(0	1	0	0	0	×	1	X	X	١	x	1
0	1	0	0	0	1	0	-\	0	X	×	O	0	X	1	×
0	1	0	1	0	1	١	0	0	X	X	0	١	X	X	-
0	1	1	0	0	1	1	١	0	X	X	0	×	0	1	X
0	1	1	1	1	0	0	0	1	X	X	١	X	1	X	1
1	0	0	0	1	0	0	1	×	0	0	X	6	X	1	X
1	0	0	1	0	0	0	0	X	١	0	×	6	×	X	1
1	0	1	0	0	0	0	0	X	١	0	X	X	١	0	X
1	0	1	1	0	9	0	0	X	\	0	X	×	1	×	1
1	1	0	0	0	0	0	0	X	1	X	\	0	X	0	X
1	1	0	١	0	0	0	0	X	1	X	1	0	X	X	1
	1		0	0	0	0	0	X	1	×	1	X	(0	X
1		(1	0	0 (0	0	X	1	X	١	X	(X	1





Logic diagram $Q = A + C + BD + \bar{B}\bar{D}$ e= BD+CD B+CD+CD f= A+cD+BD C= B+ Z + D 9=A+BC+BC+CD d = A + BD + CD + BC + BCD

7 segment display

6 r	ABCD	a	ь .	C.	d	e	f	19	1
(0)	ABCD	1	1	1	1	1	1	0	-
(1)	00000	0	1	01	0	6	0	0	
(2)	0010	1	1	0	1	1	C	1	_
(3)	0011	1	1	1	1	0	0	1	_
(4)	0100	0	1	1	0	0		1 1	
(5)	0 1 0 1	1	0	1	1	0		1	_
(6)	0 11 0	1	0	1	1	1		1	1
(7)	0 11 1	1	1	1	1) [0	0
(84	1000	1		1			1	1	1
(A)-	1001	1	1	1			0	1	1

