

Technical Reference Manual

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BUSLOGIC

MULTI-MASTER ULTRA
SCSI HOST ADAPTERS
FOR PCI SYSTEMS

Technical Reference Manual



MULTI-MASTER ULTRA SCSI HOST ADAPTERS FOR PCI SYSTEMS

Revision History

Revision	Change Activity	Date
A	Release	6/1/96

Compliance Statements

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operations.

Declaration of the Manufacturer/Importer

We hereby certify that the SCSI Host Adapter for PCI, VESA, EISA and ISA, in compliance with the requirements of BMPT Vfg 243/1991, is RFI suppressed. The normal operation of some equipment (e.g., signal generators) may be subject to specific restrictions. Please observe the notices in the user's manual.

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EN50082-1 GENERIC IMMUNITY STANDARD

- 1) IEC 801-2(1992) CRITERIA B; 2) IEC 801-3(1992) CRITERIA A
- 3) IEC 801-4(1988) CRITERIA B; 4) IEC 801-5(DRAFT 1993) CRITERIA B

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Preface

The BusLogic SCSI Host Adapter Technical Reference Manual is intended for system software programmers desiring to develop device driver software for BusLogic's family of SCSI adapter products.

This manual covers adapter architecture, hardware and software operation and includes electrical signaling information for each bus architecture.

Products covered in this document include:

- BT-948 PCI Ultra SCSI Host Adapter
- BT-958 PCI Ultra Wide SCSI Host Adapter
- BT-958D PCI Differential Ultra Wide SCSI Host Adapter

Contents

This manual is organized in the following manner:

Part 1: Adapter Operation

- Section 1 contains an overview to BusLogic's MultiMaster™ technology.
- Section 2 details adapter hardware components and operation.
- Section 3 discusses software operation between the host adapter and the host system.
- Section 4 describes the adapter's SCSI electrical interface.
- Section 5 details adapter internal diagnostics.
- Appendix A is a list of industry acronyms.

Part 2: PCI Host Adapters

- Section 1 includes descriptions and specifications for the BT-948, BT-958, and BT-958D host adapters.
- Section 2 describes the electrical interface for the BT-948, BT-958, and BT-958D host adapters.
- Section 3 contains the PCI bus timing diagrams.

Related Documentation

Refer to the user's guide provided with your BusLogic host adapter for details on host adapter installation and configuration.

Notational Conventions

The following conventions are used throughout this manual:

Convention	Description
UPPERCASE	Used to indicate the names of keys.
-	A hyphen indicates an active low signal.
+	A plus sign indicates an active high signal.

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BusLogic MultiMastering Technology

Introduction

Bus mastering data transfers are commonly used by intelligent I/O controllers to increase system performance by off-loading the low level control tasks to a dedicated micro-controller. BusLogic has created a unique technology for implementing a diverse family of high performance bus mastering SCSI host adapters while maintaining a high degree of compatibility among them. This technology is called MultiMaster™ and is implemented in a single ASIC. The MultiMaster technology is utilized on all BusLogic MultiMaster adapters allowing them to share common device drivers, firmware and BIOS. The following describes the key features, capabilities and benefits of BusLogic MultiMaster technology.

Bus Mastering Data Transfer

Bus mastering data transfer is a form of information transfer between two devices. The advantages of bus mastering in a PC environment are that it requires less host CPU time and offers high performance data transfers. An intelligent bus master device will use a micro-controller or micro-processor to perform complex I/O operations that would otherwise require interaction from the host system CPU. BusLogic intelligent SCSI controllers utilize a 16-bit micro-controller to off-load control of information transfers, thus freeing the system CPU for other tasks and increasing overall system performance as well as I/O performance.

BusLogic's MultiMaster technology allows the use of a single ASIC as the interface to our bus mastering adapters. The MultiMaster ASIC contains all the logic required to fully automate a bus master transfer on five different system buses: ISA, EISA (EMB), VL-Bus, MCA and PCI. This technology enables a common high performance microprocessor-based architecture to be applied to many system platforms. It allows the use of a single device driver per operating system to support all BusLogic MultiMaster SCSI host adapters.

Description

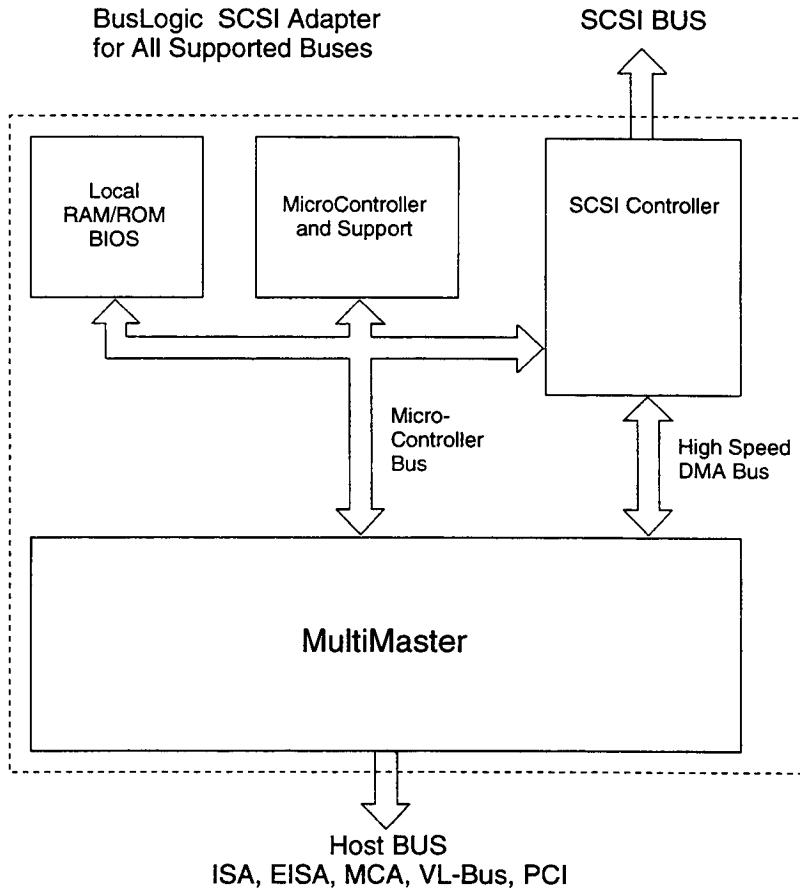


Figure 1-1. Typical MultiMaster SCSI Adapter

MultiMaster provides a complete register and interrupt interface between the host system and the host adapter microcontroller. SCSI command overhead is reduced by reading and updating mailboxes in host memory without intervention by the host adapter microcontroller. Data transfers between the SCSI controller and host system memory are under complete control of the MultiMaster ASIC, from system bus arbitration to the completion of data transfer.

Configuration

The MultiMaster ASIC is configured to interface with a particular system bus by hard wiring three mode select pins. Each host adapter has these pins tied to logic levels representing the host bus the adapter interfaces with. The ASIC contains the bus interface protocols required for each supported system bus. By embedding all the bus specific protocols in the MultiMaster ASIC the microcontroller and firmware design issues become independent of the target host platform.

Registers within the MultiMaster ASIC are configured at power-up to determine host adapter operating parameters.

In the PCI bus, the system BIOS will scan the system bus and assign I/O port address, BIOS memory address and interrupt level dynamically each time the system is powered up. This fully automatic initialization is also supported by the BusLogic MultiMaster ASIC.

The MultiMaster ASIC maintains a high level of isolation between the host environment and adapter firmware, allowing a common architecture to be applied to all BusLogic MultiMaster SCSI host adapters.

Bus Master Transfers

There are three basic phases of a bus master transfer: arbitration, where the bus master requests and gains access to the system bus; data transfer, in which the bus master has control of the bus and is actively transferring data across the bus. Data transfer is followed by bus release once all available data has been transferred or bus release is being forced to allow another device access or a system memory refresh cycle. Although signals and timing vary from one bus type to another, our MultiMaster technology fully automates the data transfer process.

Arbitration

Once a data transfer has been programmed into the MultiMaster by the local microprocessor, the resulting bus master transfer is completely automated by the MultiMaster ASIC. Bus arbitration is initiated by asserting the DMA request (for ISA systems) or bus request signal (for non-ISA systems) appropriate to the particular environment the MultiMaster is residing in. The host system then responds with an acknowledge signal granting access to the system bus. The MultiMaster then asserts a host bus signal to indicate it will be acting as a bus master. The host adapter is now the active bus master and has complete control over the system bus. In an ISA system the MultiMaster arbitrates for the system bus by asserting the DMA request line and waiting for a DMA acknowledge.

Data Transfer

Data transfer begins after the host system has granted the host adapter access to the system bus. The MASTER (or FRAME in a PCI system) signal is then asserted by the MultiMaster to inform the host system it is acting as a bus master device. The host adapter is now the active bus master and controls the system address, memory read and memory write signals to perform the current data transfer. This continues until one of three things happens: (1) the data transfer is complete, (2) the host adapter is unable to continue transferring due to an empty or full FIFO buffer or (3) the host system requires the bus to be released.

Bus Release

During the bus release phase the MultiMaster will relinquish control of the system bus through the appropriate protocol for the currently supported host bus.

Preempt

The MultiMaster will release the host system bus when preempted. Most advanced system bus architectures have provisions for preemption of the current bus master. This allows other bus masters to share the system bus. This also is required to allow the host system to perform system memory refresh cycles.

MultiMaster Advantages

MultiMaster technology offers several key advantages: performance, reliability and efficient product design cycles.

Performance

MultiMaster enhances the performance of BusLogic bus mastering SCSI products in several ways. The MultiMaster ASIC automatically retrieves mailbox entries and associated commands from the host system memory in a single operation. This greatly reduces the command overhead associated with maintaining the mailbox interface. Scatter/gather operations are streamlined under control of the MultiMaster. The microcontroller is able to pre-initialize the next segment of a scatter/gather transfer while the current segment is being transferred. This maintains the continuous flow of data during scatter/gather operations.

All BusLogic SCSI MultiMaster host adapters utilize the same mailbox structure interface. This mailbox interface allows the host system to perform multitasking I/O operations with minimum overhead. Mailboxes are located in system memory. The mailbox structure allows up to 255 independent I/O commands to be processed by the SCSI adapter simultaneously. The MultiMaster will automatically scan the mailboxes for a valid entry. Once a valid entry is found the MultiMaster will automatically read the mailbox and store the associated CCB (Command Control Block) in the host adapter local RAM and clears the mailbox semaphore. The advanced features of BusLogic MultiMaster ASIC coupled with a 16-bit microcontroller resident on all BusLogic bus mastering SCSI adapters provides high performance and reliability.

BusLogic MultiMaster host adapters are able to perform an entire I/O operation without intervention from the host CPU. By automating the data transfer between the system memory and utilizing a dedicated microcontroller to handle the high level control of the operation, BusLogic host adapters deliver superior performance over PIO types of interface cards. CPU utilization is much more efficient for adapters without dedicated microcontrollers.

All of these features combine to deliver the user the best possible I/O performance. The MultiMaster ASIC allows this high performance architecture to be implemented on five different host system buses without any significant design changes.

Common OS Drivers/BIOS/Firmware

The MultiMaster ASIC separates the SCSI, interface microcontroller, and firmware from the system bus allowing one design to be applied to all system platforms.

MultiMaster's common system interface allows a single device driver per operating system to support BusLogic's host adapters. Only one device driver needs to be tested, qualified and embedded into the operating system kernel to support all the BusLogic MultiMaster adapters. All BusLogic MultiMaster SCSI adapters are also supported by common BIOS source code.

MultiMaster provides the isolation from the host system required for a common architecture to be applied to many system platforms. This common architecture allows the use of common firmware across the entire MultiMaster host adapter product line.

Hardware Description

BusLogic host adapters are based on a BusLogic-designed, MultiMaster ASIC technology, offering high-performance interconnection between the bus architecture and Small Computer System Interface (SCSI) peripheral devices. A BusLogic-designed bus master controller ASIC, an advanced SCSI controller chip and a 16-bit microprocessor chip provide higher speed, lower power consumption, fewer parts and higher reliability.

Both internal and external connectors are included on the board for flexibility in attaching SCSI devices to the system.

This section describes the adapter's functional hardware operation. It covers the hardware control registers that are mapped into the system's I/O address space. It also describes command use, data flow and hardware management.

Adapter Architecture

The host adapter plugs into a host system and supports the attachment of internal SCSI drives or the connection to external SCSI peripheral devices in add-on enclosures. The system architecture is illustrated in Figure 1-2.

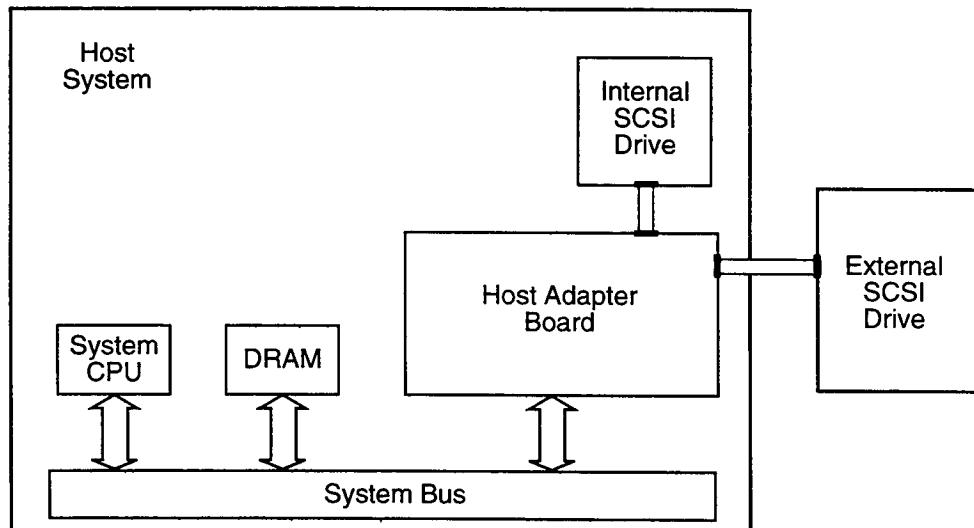
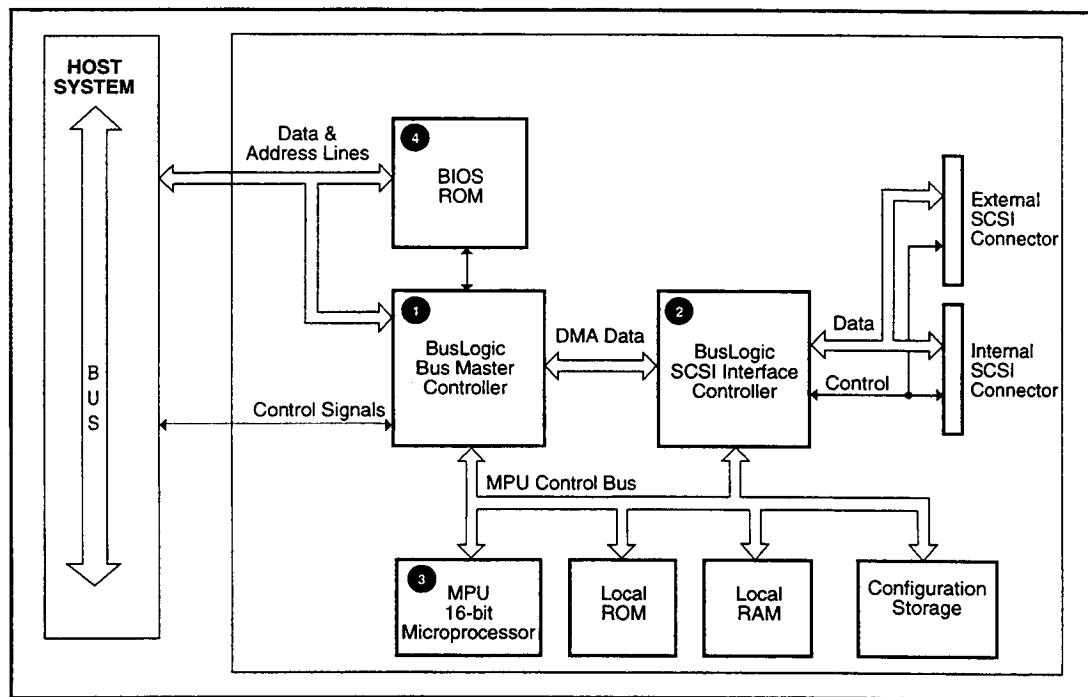


Figure 1-2. System Architecture

Figure 1-3 is a functional block diagram of the BusLogic adapter. The paragraphs that follow describe the numbered components in the figure.



Notes:

Configuration storage, local ROM, and BIOS ROM use the same flash memory devices in the host adapters.

Figure 1-3. Host Adapter Architecture

Bus Master Controller

All host bus interface logic is provided on the board by a BusLogic designed bus master ASIC ①. This chip provides bus master capabilities which greatly reduce the involvement of the host system's CPU in I/O control and data transfer activities. Under control of this chip, 32-bit bus master transfers at up to 132 MBytes/sec to and from the main system memory are possible with the use of its internal 128-byte FIFO. A true multitasking mailbox structure supports up to 255 tasks. This performance and improved bus utilization significantly enhances multitasking and multi-user applications.

Advanced SCSI Controller

On-board control of the interface to SCSI peripheral devices is provided by another ASIC, the BusLogic SCSI controller chip ②. Up to 20 MBytes/sec (Fast-20) synchronous and 7 MBytes/sec asynchronous data transfer for 8-bit SCSI, up to 40 MBytes/sec (Fast-40) synchronous, and 14 MBytes/sec asynchronous data transfer for 16-bit wide SCSI data transfers are supported by the SCSI interface controller. This low-power, high-performance CMOS component completely conforms to the ANSI standard, X3.131-1986 for the Small Computer System Interface. The chip reduces protocol overhead by performing common SCSI algorithms or sequences in response to a single host system command.

Microprocessor Unit (MPU)

An on-board, 16-bit Intel-based 8018X microprocessor unit (MPU) ③ coordinates all activity on the host adapter under the direction of the board's local ROM. Consequently, the on-board MPU orchestrates such activities as the initialization, command decoding, interrupt generation and the control of the data flow among the board's components.

Local BIOS ROM

The host adapter can be used in place of or in conjunction with a standard hard disk controller. The host adapter's on-board local BIOS ④ provides a compatible method of attaching a SCSI hard drive to a system just as any other type of hard disk is connected. The host adapter's BIOS intercepts each host software interrupt that requests a disk I/O service and manages these interrupts according to the address of the requested drive. If the designated drive is a disk assigned to the system's internal disk controller, the host adapter's BIOS passes the command on to that disk controller. If the designated disk is one of the SCSI disks attached to the host adapter, the host adapter's BIOS responds to the request and instructs the host adapter to execute the command.

Host Data Transfer Control for PCI Bus

The Bus Mastering control logic manages bus arbitration and data transfer coordination. The BusLogic host adapter operates as a PCI bus master during data transfers. The BusLogic host adapter arbitrates for PCI bus access and, once granted, it takes over control of the bus. It generates the PCI bus address and command strobes. The BusLogic host adapter supports both odd and even starting addresses, commonly known as aligned and unaligned transfers. If presented with an even transfer count beginning at an odd memory starting address, the BusLogic host adapter will first transfer a single byte (data bits D24-D31). The remaining data is then transferred as double words (32 bits) until the last byte, which is transferred as a single byte (data bits D0-D7). While odd byte transfers are fully supported, it is recommended that when possible, PCI host buffers be double-word aligned to gain better data transfer performance.

Hardware Registers

The host adapter's I/O interface consists of three hardware registers that are used by the host to issue start commands to the host adapter, to gain status information about the adapter's operation, and to manage interrupts generated by the host adapter. These registers are located in the I/O address space at three consecutive addresses. The beginning or base address is determined by the I/O base address assigned in the host adapter PCI configuration space by the system. Table 1-1 provides a summary of these 8-bit wide registers.

Table 1-1. Host Adapter Hardware Registers

Address	Type	Description
I/O Base Address + 0	W	Control Register
I/O Base Address + 0	R	Status Register
I/O Base Address + 1	W	Command/Parameter Register

Table 1-1. Host Adapter Hardware Registers (Continued)

Address	Type	Description
I/O Base Address + 1	R	Data In Register
I/O Base Address + 2	R	Interrupt Register

Control Register (Write Only) I/O Base Address + 0

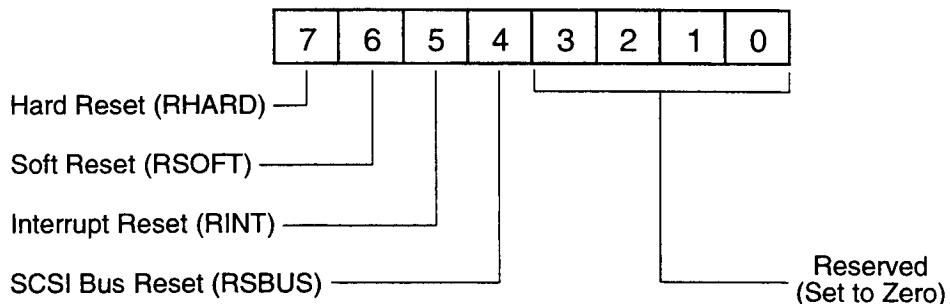


Figure 1-4. Control Register (Write)

The host system's CPU uses this register to specify programmable options within the host adapter (e.g., soft reset, hard reset, SCSI bus reset). For example, the host system's CPU can stop all host adapter activity immediately by setting this register's Bit 6, the Soft Reset bit (RSOFT). This is a write-only register.

Bits 0–3—These bits are reserved and must be set to zero.

Bit 4 Reset SCSI Bus (RSBUS)—When this bit is set to a one, the Reset signal on the SCSI bus is maintained true for at least 25 microseconds. This Reset condition immediately clears all SCSI devices from the bus. The assertion of the SCSI Reset condition supersedes all other activity on the SCSI bus. See the heading “Reset Operations” later in this section for additional details on the Reset operation.

Bit 5 Reset Interrupt (RINT)—The system’s CPU sets this bit to acknowledge a host adapter interrupt. When this bit is set to one by the CPU, the host adapter’s hardware-generated interrupt is reset and the Interrupt Register is cleared. Note that all bits in the Interrupt Register are cleared by setting this bit.

Bit 6 Soft Reset (RSOFT)—When this bit is set to one, it causes all host adapter activity to stop immediately. All mailboxes, command control blocks, and any pending commands are discarded by the host adapter. Previous mailbox pointers must be cleared by host processes. The primary difference between a hard and soft reset is that this bit does not effect a SCSI Bus Reset condition. Once the soft reset activity has been completed by the host adapter, the host adapter must be reinitialized for any future operation. This state is indicated by the setting of the Host Adapter Ready bit (HARDY) and the Initialization Required bit (INREQ) in the Status Register.

Bit 7 Hard Reset (RHARD)—The setting of this bit causes the host adapter to enter an initial condition power-on state. Any command in process is stopped and pending commands are abandoned. The host adapter will execute its internal diagnostic function and report any errors. During reset, the Diagnostic Active bit (DACT) is set. Once the hard reset activity has been completed by the host adapter, the host

adapter must be reinitialized for any future operation. This state is indicated by the setting of the Host Adapter Ready bit (HARDY) and the Initialization Required bit (INREQ) in the Status Register.

Specific operation bits in the Control Register are automatically reset by the host adapter when the specific operation is completed. The host-controlling software is not required to reset the operational control bit for a specific function.

Status Register (Read Only) I/O Base Address + 0

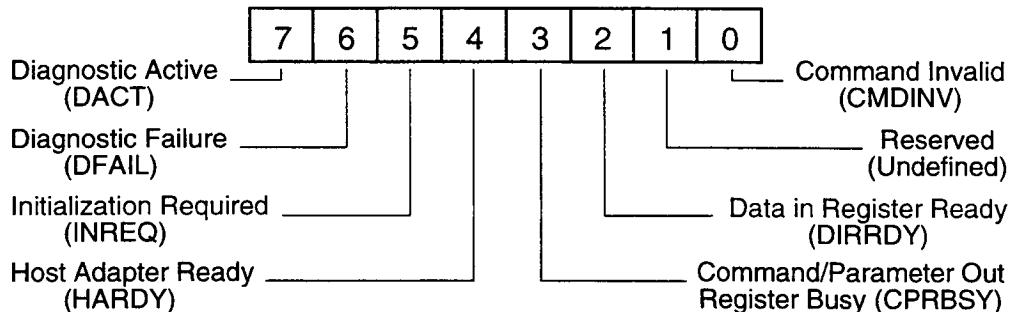


Figure 1-5. Status Register (Read)

The host adapter uses this register to report the status of its condition to the system's CPU. For example, the host adapter sets this register's Data In Register Ready bit (DIRRDY) when it has written data to its Data In Register. By setting this bit, the host adapter notifies the host system's CPU that there is fresh data in the Data In Register that should be read. As soon as the host system's CPU reads the Data In Register, the host adapter immediately resets the Data In Register Ready bit (DIRRDY). The host adapter resets this bit to zero to ensure that the host system's CPU does not reread the same data in the Data In Register. When the host adapter writes fresh data to its Data In Register, it will then set the Data In Register Ready bit (DIRRDY) to one again.

The host system's CPU can also read this register to check for error conditions. For example, the host adapter sets this register's Command Invalid bit (CMDINV) when it detects an invalid command or parameter byte in its Command/Parameter Register. Consequently, the host system's CPU can check the Command Invalid bit (CMDINV) to see if such an error condition currently exists. This is a read-only register.

Bit 0 Command Invalid (CMDINV)—The host adapter sets this bit immediately upon detection of an invalid command or parameter byte in the Command/Parameter Register. When the host is sending a single or multibyte command, the host adapter terminates the data transfer sequence by setting the Command Complete bit (CMDC) in the Interrupt Register and by generating a hardware interrupt. The host adapter terminates all commands (valid or invalid) by this method. Invalid commands are indicated by the setting of this bit. The condition of this bit is only meaningful while the Command Complete bit (CMDC) is true.

Bit 1 This bit is reserved and is set to zero.

Bit 2 Data In Register Ready (DIRRDY)—This status bit is used to synchronize the transfer of status information from the host adapter to the host system. The host adapter sets this bit to one when it has placed a byte of data in the Data In Reg-

ister. This condition notifies the host that it may read and process the data. When the host reads the data byte in the Data In Register, this bit is reset to zero by the host adapter. This sequence is repeated for multibyte data transfers.

Bit 3 Command/Parameter Register Busy (CPRBSY)—This status bit is used to synchronize the transfer of command and associated parameter bytes from the system host to the host adapter. When this bit is reset to zero the host may place a command or parameter byte in the Command/Parameter Register. When the host writes a byte to the Command/Parameter Register, the host adapter will set this bit to a one indicating a Busy condition. The host adapter will reset this bit when it has read and processed the command/parameter byte. This sequence is repeated for multibyte data transfers.

Bit 4 Host Adapter Ready (HARDY)—This bit indicates the ready or not ready internal command state of the host adapter. When this bit is set, the host adapter is ready for a new host adapter command. In general the host system's processor may only issue host adapter commands while this bit is set.

Note: The multitasking design of the host adapter's firmware permits the following commands to be issued regardless of the busy or not-busy state of the host adapter.

- Start SCSI (02) command
- Enable Outgoing Mailbox Ready Interrupt (05) command.

See Section 1-3, "Software Interface," for details on these commands

Bit 5 Initialization Required (INREQ)—When this bit is set to one, it indicates that the mailbox structures must be initialized. This bit is typically set immediately after the completion of self-diagnostic tests following a reset. This bit is not set if diagnostics fail (the Diagnostic Failure bit (DFAIL) is set). The host system must now issue an Initialize Mailbox command (01) to inform the host adapter of the base memory address of the mailbox structure area. The host adapter will reset this bit after successful completion of the Initialize Mailbox command.

Bit 6 Diagnostic Failure (DFAIL)—When this bit is set, it indicates that the host adapter's internal self diagnostic has detected an error. This bit may be reset only by a hard reset initiated either by hardware or by the host software. See Section 1-6, "Internal Diagnostics," for more details.

Bit 7 Diagnostic Active (DACT)—This bit is set when the host adapter begins its self-testing activity immediately after a power-on reset or a programmed hard reset (Control Register, Bit 7 is set). This bit is reset upon the successful completion of the self-test activity. If the diagnostics fail, this bit may not be reset indicating that the self-test programs could not be completed. In the case of most failures, the Diagnostic Failure bit (DFAIL) will also be set. See Section 1-6, "Internal Diagnostics," for more details.

Command/Parameter Register (Write Only) I/O Base Address + 1

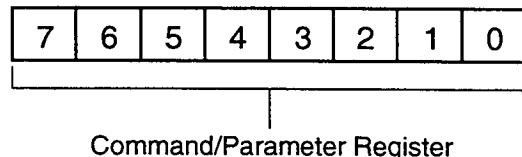


Figure 1-6. Command/Parameter Register (Write)

The Command/Parameter Register serves as the input port through which the host system software may issue commands and associated parameter bytes to the host adapter. The commands issued to the host adapter by this method provide initialization and establish control specifications for subsequent operations. SCSI-bus related commands are issued through a mailbox command structure (See Section 1-3, "Software Interface."). The host is responsible for issuing the correct number of command and parameter bytes for each operation. Otherwise, incorrect operation may occur along with the cessation of command acceptance by the host adapter. This condition is indicated by the setting of the Command Invalid bit (CMDINV) in the Status Register.

The coordination of command and parameter data byte transfers between the host adapter and the host system is governed by the Host Adapter Ready bit (HARDY), the Command/Parameter Register Busy bit (CPRBSY), and the Data In Register Ready bit (DIRRDY). All host adapter commands, with the exception of Enable OMCR Interrupt (05) and Start SCSI (02), require the Host Adapter Ready bit (HARDY) to be set. Parameter data bytes are written to the Command/Parameter Register. The host must first test the Command/Parameter Register Busy bit (CPRBSY) for a not set condition to determine if the host adapter is ready to accept a command parameter data byte. When the host writes a command or parameter byte to the Command/Parameter Register, the host adapter sets the Command/Parameter Register Busy bit (CPRBSY) to a one. When the local MPU has read the byte, the host adapter will reset the Command/Parameter Register Busy bit (CPRBSY) to indicate that the host can write another byte.

When all the bytes for a particular command have been transferred, and the command has been completed, the host adapter will set the Command Complete bit (CMDC) in the Interrupt Register. If an error is detected in the command, the Command Invalid bit (CMDINV) will be set in the Status Register.

Data In Register (Read Only) I/O Base Address + 1

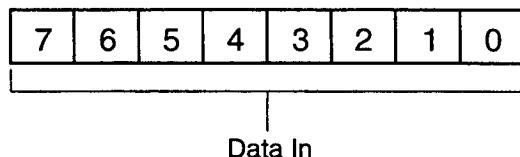


Figure 1-7. Data In Register (Read)

The host adapter uses this register to return information bytes to the host system. For commands that return information bytes to the host, the Data In Register Ready bit (DIRRDY) is used to synchronize data byte transfers. The host adapter sets the Data In Register Ready bit (DIRRDY) to a one when a data byte is available to be read by the host system. The Data In Register Ready bit (DIRRDY) is automatically reset to zero by the host adapter when the host system reads the data byte from the host adapter's Data In Register. For multiple data byte transfers, the host should wait for the Data In Register Ready bit (DIRRDY) to return to the set state before reading additional data. When the last byte of an information block (single or multiple byte) has been transferred, the host adapter will set the Command Complete bit (CMDC) in the Interrupt Register. This is a read-only register.

Interrupt Register (Read Only) I/O Base Address + 2

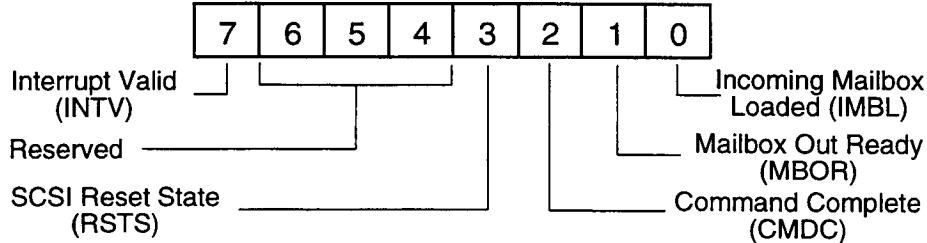


Figure 1-8. Interrupt Register (Read Only)

The host adapter uses this read-only register to tell the host system the reason why it generated a hardware interrupt signal. The following are the four conditions under which the host adapter can generate a hardware interrupt to the host system:

1. Incoming Mailbox Loaded interrupt (IMBL): the host adapter has made an entry in an incoming mailbox.
2. Mailbox Out Ready interrupt (MBOR): an outgoing mailbox location(s) is ready for the host system to use.
3. Command Complete interrupt (CMDC): the host adapter has completed a command.
4. SCSI Reset State interrupt (RSTS): the host adapter has detected a SCSI Bus Reset condition.

When the host adapter generates a hardware interrupt signal for one of the preceding four reasons, the host adapter sets bits in this register to provide the host system with more information about the interrupt. The host adapter completes the following actions:

1. It sets Bit 7, the Interrupt Valid bit (INTV), to indicate that the interrupt is valid.
2. It also sets one of the other unreserved bits to indicate why it generated a hardware interrupt signal to the host system. These bits (Bits 0-3) are collectively referred to as interrupt cause bits. This group of bits include the Incoming Mailbox Loaded bit (IMBL), the Mailbox Out Ready bit (MBOR), the Command Complete bit (CMDC), and the SCSI Reset State bit (RSTS).

In response to this interrupt request by the host adapter, the host system should execute the following sequence to service the interrupt:

1. Read the Interrupt Register. The host should maintain this value internally for further interrupt processing.
2. Clear the Interrupt Register. This is accomplished by setting the host adapter's Control Register's Reset Interrupt bit (RINT).
3. Determine the interrupt cause (from the saved Interrupt Register value in the preceding Step 1) and then execute the appropriate interrupt service routine.

Note: A hard reset, a soft reset, or initial board power-on condition will cause the Interrupt Register to be cleared, i.e., no interrupts pending.

The host adapter sets the priority of certain interrupt conditions. This topic will be discussed before describing the individual bits of the Interrupt Register. Refer to the following heading "Interrupt Timing and Synchronization."

Interrupt Timing and Synchronization. The host adapter sets the priority of certain interrupt conditions. The posting of a mailbox-related interrupt is withheld if a SCSI Reset State interrupt (RSTS) or a Command Complete interrupt (CMDC) is pending service from the host. Once the SCSI Reset State interrupt (RSTS) or the Command Complete interrupt (CMDC) is cleared, the host adapter will post the mailbox interrupt(s). Likewise, a SCSI Reset State interrupt (RSTS) or a Command Complete interrupt (CMDC) will only be presented if the Interrupt Register has been cleared, and the Data In Ready bit (DIRRDY) shows no additional data is pending.

Because all outbound host mailboxes are typically controlled by host-resident software, it is not necessary to enable the Outgoing Mailbox Ready interrupt (OMBR) unless all mailboxes are being utilized. This technique also lessens the possibility of missed interrupt notification for an Incoming Mailbox Loaded (IMBL) condition. If all outgoing mailboxes are in use, then the host could enable the Outgoing Mailboxes Ready interrupt (OMBR) to gain notification of a Mailbox Ready condition. See the Enable Outgoing Mailbox Ready command description in Section 1-3, "Software Interface," for instructions on how to enable the Outgoing Mailboxes interrupts (OMBR).

Bit 0 Incoming Mailbox Loaded (IMBL)—When this bit is set, it indicates that the host adapter has made an entry in an incoming mailbox location. This bit is qualified by the Interrupt Valid bit (INTV) also being set and by the generation of a bus interrupt signal. The host should service this interrupt as soon as possible to allow additional host adapter interrupts to be posted. The multitasking firmware of the host adapter continues to process outstanding SCSI commands after the posting of an Incoming Mailbox Loaded interrupt (IMBL). If additional outstanding commands are completed before the servicing of a previous Incoming Mailbox Loaded interrupt (IMBL), the status of completed commands will be placed in an available incoming mailbox location. The host should therefore scan all mailboxes to determine if additional data has been provided. The host adapter will use Incoming Mailbox locations in a round-robin order permitting the host to scan in the same manner. When a vacant mailbox is found the host may discontinue its scan.

Bit 1 Outgoing Mailbox Ready (OMBR)—When this bit is set to a one, it indicates that one or more of the outgoing mailbox locations is available for use by the host. This bit is qualified by the Interrupt Valid bit (INTV) also being set and by the generation of a bus interrupt signal. The Outgoing Mailboxes Ready interrupt (OMBR) is generated only when Outgoing Mailbox interrupts (OMBR) have been enabled and an outgoing mailbox entry is cleared by the host adapter. An Outgoing Mailbox Ready interrupt (OMBR) is suppressed if a SCSI Reset State (RSTS) or a Command Complete (CMDC) interrupt is pending service. When these previous interrupts are cleared by the host, the pending Outgoing Mailboxes Ready interrupt (OMBR) will be issued by the host adapter.

Application Note: It is recommended that the Outgoing Mailbox Ready interrupt (OMBR) not be enabled unless all outgoing mailbox locations are in use. For most applications, the host adapter will process command requests faster than a host will issue them. If the situation does occur where all outgoing mailbox locations are busy, the host may issue the Enable Outgoing Mailbox Ready Interrupt command without waiting for the status of the Host Adapter Ready bit (HARDY).

Bit 2 Command Complete (CMDC)—This bit is set to a one when the Command/Parameter Register is ready to accept a command. Any previous command will have been completed, either normally or abnormally. If a previous command completed with an error condition or was aborted for any reason, this bit will still be set along with the Command Invalid bit (CMDINV) in the Status Register. Normally completed commands are indicated by the setting of this bit without any accompanying error condition status bits. This bit is qualified by the Interrupt Valid bit (INTV) also being set and by the generation of a bus interrupt signal. A Command Complete interrupt (CMDC) is suppressed if an Interrupt Valid bit (INTV) is set (indicating an interrupt is pending service) or if the Data In Register Ready bit (DIRRDY) is set. When these previous interrupts are cleared by the host, the temporarily withheld Command Complete interrupt (CMDC) will be issued by the host adapter.

Bit 3 SCSI Reset State (RSTS)—When this bit is set, it indicates that a SCSI Bus Reset condition has been detected by the host adapter. This bit is qualified by the Interrupt Valid bit (INTV) also being set and by the generation of a bus hardware interrupt signal. In cooperation with host system driver software, the host adapter can implement the SCSI specification soft reset option. host adapter queued operations will resume once the SCSI bus has returned to the operational state. If a currently running command was aborted due to the SCSI Bus Reset condition, the host adapter may have to restart the command.

The host may convert the SCSI bus soft reset to a SCSI bus hard reset by setting the Soft Reset bit (RSOFT) in the host adapter's Control Register. In this case, all queued commands are abandoned and the host adapter must be reinitialized. See the heading "Reset Operations" later in this section for details on the reset conditions.

Bit 4 Reserved—Value read is zero.

Bit 5 Reserved—Value read is zero.

Bit 6 Reserved—Value read is zero.

Bit 7 Interrupt Valid (INTV)—When this bit is set, it indicates that a valid interrupt has been generated by the host adapter. This bit reflects the state of the host adapter generated interrupt signal on the bus. The specific reason for the interrupt condition is determined by Bits 0-3 of this register.

Reset Operations

Host adapter reset conditions are initiated from two different vantage points: the host system and the SCSI bus. A description of each follows.

Host-Initiated Reset Operations

The host system may reset the host adapter to an initial power-on condition through two different operations, one system and the other software.

System Reset—The host adapter is fully reset and initialized to a power-on initial condition when the Reset signal is true on the host system bus. The Reset signal is asserted to a true condition by the host (1) during power on, (2) host detected low-power conditions, or (3) a user-invoked reset switch reset. The Reset signal is applied universally to all installed host adapters in the system bus. A host adapter system reset causes a power-on initialization process which also results in a reset of all the devices on the SCSI bus.

Software Reset—The host adapter may be fully reset to an initial state by a software command, just the same as if a system reset had been received by setting the Hard Reset bit (RHARD). When RHARD is set to true, a Reset condition occurs immediately. However, this Reset condition will only affect *one* host adapter, unlike the system reset (described above) which resets *all* host adapters installed in the system bus. An RHARD reset may issue a subsequent reset to the SCSI device depending on the AutoSCSI utility configuration setting for the **Enable SCSI Bus Reset** option (see the manual for your host adapter for more information).

Either type of host-initiated reset will cause the following conditions on the host adapter.

- The control registers of all intelligent logic modules on the host adapter will be initialized to a known state.
- All pending operations are aborted and all data structures are initialized to a no operation pending state.
- The host adapter executes all internal diagnostic functions. While the diagnostic functions are in process, the host adapter will indicate this condition by setting the Diagnostic Active bit (DACT) to true in the Status Register.
- During a system reset, the host adapter places a SCSI Bus Reset condition on the SCSI bus. This may also occur during a software reset (using the RHARD bit), but depends on the AutoSCSI utility configuration setting for the **Enable SCSI Bus Reset** option. This will reset all peripheral devices, whether a target or initiator.
- After completion of a system reset, the host adapter indicates that it is now in an initial condition by asserting the Initialization Required bit (INREQ) in the host adapter's Status Register. This condition requires that all mailbox, command control blocks, and host adapter operation parameters be established before operations may begin.

Note: The host may initiate a soft reset by setting the RSOFT bit. This reset reinitializes the specific host adapter, but there is no subsequent SCSI bus reset.

SCSI Bus Reset Operations

The SCSI Bus Reset condition is used to clear all SCSI devices immediately from the SCSI bus. When the SCSI bus Reset signal is asserted, the SCSI Bus Reset condition takes precedence over all other bus phases. A SCSI Bus Reset condition may be forced by any device on the bus, whether a target or initiator. Whenever a SCSI Reset condition occurs, a Bus Free phase always follows the Reset condition.

The five ways in which a SCSI bus reset may be either asserted or sensed by the host adapter are as follows:

- R1 The SCSI Bus Reset condition is always asserted when the host adapter is reset by the host system (host system **system** reset only). This is described earlier in this section under the heading "Host-Initiated Reset Operation."
- R2 The SCSI Bus Reset condition may be asserted when the host adapter is **soft** reset by the host system when RHARD is set to true (depending on the AutoSCSI utility configuration setting for the **Enable SCSI Bus Reset** option). This is also described under the heading "Host-Initiated Reset Operations."
- R3 The SCSI Bus Reset condition is asserted if the Reset SCSI Bus bit (RSBUS) is set by the host system control software.

- R4 The host adapter may initiate a SCSI Bus Reset condition in reaction to a detected bus phase error. The host adapter constantly monitors the SCSI bus for invalid conditions. If an invalid phase is detected, the host adapter will perform a normal SCSI Bus Reset operation which includes the assertion of the SCSI bus Reset signal.
- R5 The host adapter will detect and respond to a SCSI Bus Reset condition that is asserted by another device on the bus. Other SCSI devices may normally assert the Reset signal during either initialization or certain error recovery states. The device driver requires an acknowledgment from the host adapter that a SCSI Reset operation has taken place, so the SCSI Reset State bit is set in the interrupt register.

While the SCSI specification defines two methods by which the SCSI bus may be reset, either by the hard reset option or the soft reset option, *BusLogic host adapters only support the hard reset option.*

The SCSI bus hard reset option restores ALL SCSI devices, target or initiator, to the initial power-on condition. All system activity is lost, and all devices must be completely reinitialized before normal operations may be restored. SCSI devices that implement the hard reset option perform the following operations:

- Clear all uncompleted commands.
- Release all SCSI device reservations.
- Return any SCSI device operating modes to their default condition.

Here is how the host adapter implements a SCSI hard reset:

- When the host adapter detects a SCSI reset, it issues an interrupt indicating a SCSI reset has occurred to the host system.
- The host adapter sets both the SCSI Reset State bit (RSTS) and the Interrupt Valid bit (INTV) in the host adapter's Interrupt Register.
- All host adapter command control blocks (CCBs) are abandoned and the host adapter readies itself to accept new initialization commands.
- BusLogic recommends that after the device driver receives the RSTS, it issue a RHARD or an RSOFT to ensure that the host adapter is re-initialized.
- All the mailbox and command control blocks must be reinitialized.

Software Interface

For the host adapter to operate properly, the host system must issue the correct command and associated parameters to the host adapter. The host adapter has its own set of executable instructions that the host system can issue to the host adapter. This command set can be subdivided into the following three groups:

1. Host adapter commands
2. Mailbox commands
3. BIOS commands

The host system uses the host adapter commands to initialize and to establish control specifications for subsequent operations of the host adapter. The host system uses the host adapter's Command/Parameter Register as an input port through which it issues any host adapter commands and associated parameter bytes to the host adapter. For more details on each of these host adapter commands refer to the heading "Host Adapter Commands" later in this section.

The second category of commands, mailbox commands, is issued to the host adapter when multithreaded operations are required. Mailboxes are reserved storage areas which reside at a fixed contiguous memory location in the host system's main memory. The mailboxes coordinate communications between the host system and the host adapter when the host adapter is operating in multithreaded mode. This software interface enables the host adapter to execute multiple commands concurrently for multiple targets with minimal intervention from the host system. For more details on these mailbox commands refer to the heading "Mailbox Commands" later in this section.

The third category of commands, BIOS commands, is issued to the host adapter when single-threaded operations are required. In this case the BIOS commands work with the host adapter's on-board BIOS. These commands in unison with the on-board BIOS function in a manner fully compatible with DOS and the standard BIOS interface as defined in the host system's technical reference manual. For more details on each of these BIOS commands refer to the heading "BIOS Command Interface" later in this section.

Before these commands are discussed in detail, a brief look at how the host adapter acts as bus master to transfer data on the memory bus and how it requests interrupt service from the host is presented.

Bus Master Data Transfer

The Bus Mastering control logic manages bus arbitration and data transfer coordination. The host adapter operates as a bus master during data transfers. The host adapter arbitrates for bus access and once granted, it takes over control of the bus. It generates the bus address and command strobes. The host adapter supports both odd and even starting addresses, commonly known respectively as aligned and unaligned transfers. If presented with an even transfer count beginning at odd memory starting address, the host adapter will first transfer a single byte (data bits D24-D31). The remaining data is then transferred as double words (32 bits) until the last byte which is transferred as a single byte (data bits D0-D7). While odd byte data transfers are fully supported, it is recommended that when possible host buffers be double-word aligned to gain better data transfer performance.

Interrupt Processing

Several interrupt channels are available to the host adapter. The channel to be used by each host adapter board is assigned by the system during power up or reboot. The PCI host adapter is capable of accepting from 1 to 254 channel assignments.

The host system contains a programmable interrupt controller which receives all interrupts and directs the host's CPU to a corresponding vector location which in turn contains a memory address for the software Interrupt Service routine which performs the necessary actions required by each interrupt. It also contains a Mask Register whose bits may be set to mask or cleared to permit corresponding interrupt channels to be acknowledged.

In order to respond correctly to host adapter interrupts during normal operation, the host interrupt controller must be programmed appropriately. The software driver will have to program the host's Interrupt Mask Register and interrupt vector before attempting to use interrupts from the host adapter. Programming the interrupt channel is host system dependent. User should refer to the specific system architecture for detail information.

The remainder of this section describes the structure and operation of the three categories of commands that the host can issue to the host adapter.

Host Adapter Commands

Host adapter command codes and associated parameter bytes are supplied to the host adapter's Control Register under the coordination of certain bits in the host adapter's Status Register. Table 1-2 provides a summary of these commands.

Table 1-2. Host Adapter Commands

Operation Code Hex Value	Host Adapter Command
00	Test CMDC interrupt
01	Initialize Mailbox 24-bit mode
02	Start Mailbox command
03	Execute BIOS command
04	Inquire Board ID
05	Enable OMCR interrupt

Table 1-2. Host Adapter Commands (Continued)

Operation Code Hex Value	Host Adapter Command
06	Set SCSI Selection Time-Out
07	Set Time On Bus
08	Set Time Off Bus
09	Set Bus Transfer Rate
0A	Inquire Installed Devices
0B	Inquire Configuration
0C	Target Mode Enable/disable
0D	Inquire Set-up Information
1A	Write Adapter Local RAM
1B	Read Adapter Local RAM
1C	Write Bus Master Chip FIFO
1D	Read Bus Master Chip FIFO
1F	Echo Data Byte
20	Host Adapter Diagnostic
21	Set Adapter Options
23	Inquire Installed Devices for Target ID 8-15
24	Inquire Target Devices
25	Disable Host HAC Interrupt
81	32-Bit Mode Initialize Mailbox
83	Execute SCSI Command
84	Inquire FW Version (Extended)
85	Inquire FW Version (Extended)
86	Inquire ISA compatible IO Address, IRQ Setting, and Generic I/O Port Setting
8B	Inquire Controller Model Number (Extended)
8C	Target Sync Information
8D	Inquire Extended Set-up Information
8F	Enable Strict Round Robin Mode
90	Store host Adapter Local RAM
91	Fetch Host Adapter Local RAM
92	Store Local Data in EEPROM or NOVRAM
94	Upload AutoSCSI Code
95	Modify PCI I/O Address
96	Set 64 LUN CCB format
97	Flash ROM Download
98	Enable/Disable Flash ROM Memory Write
9A	Write Inquiry Buffer
9B	Read Inquiry Buffer

Table 1-2. Host Adapter Commands (Continued)

Operation Code Hex Value	Host Adapter Command
A7	Flash ROM DownLoad or Flash ROM Upload
A8	Read SCAM data
A9	Write SCAM data

The host system can write a command to the Command/Parameter Register only after checking to see that the Host Adapter Ready bit (HARDY) is set to one, except that the Start Mailbox command and the Enable OMCR Interrupt command may be written at any time. After writing a command, the host may write a predetermined number of parameter bytes to the Command/Parameter Register after checking that the Command/Parameter Register Busy bit (CPRBSY) is zero, indicating that the Command/Parameter Register is not busy and can accept another parameter byte.

In response to some commands, the host adapter may transfer a predetermined number of parameter bytes back to the host. The host adapter places each byte into the Data In Register and then sets the Data In Register Ready bit (DIRRDY) to indicate to the host that the byte is ready to be read by the host. After the host has read the input data byte, the host adapter resets the Data In Register Ready bit (DIRRDY).

The following table lists each host adapter command code along with the associated number of parameter bytes coming into or being sent out from the host adapter and a brief description of the function performed.

Operation Code	Command	Parameter Byte Count	Direction
00	TEST CMDC INTERRUPT	None	None

Description. The host adapter's only response to this command is to set the Command Complete bit (CMDC) in the Interrupt Register. When this bit is set, the host can verify proper functioning of this bit.

Operation Code	Command	Parameter Byte Count	Direction
01	INITIALIZE MAILBOX 24-bit mode	4	Out

Description: This command specifies the number of mailboxes used by the host adapter, and the base memory location of the mailbox array to be used when executing 24-bit mode mailbox commands. Four parameter bytes follow the command byte to provide the following information:

Byte	Description
0	Number of mailboxes needed—must be greater than zero.
1–3	Base mailbox address—specifies the location of the first byte of the mailbox array. Byte 1 is the most significant byte (MSB).

Each mailbox location in memory will occupy four outgoing mailbox bytes and four incoming mailbox bytes. The Command Invalid bit (CMDINV) will be set with the Command Complete bit (CMDC) if the number of mailboxes is specified as zero. At command completion, the Command Complete bit (CMDC) is set to one and the Initialization Required bit (INREQ) is reset to zero to acknowledge that initialization is unnecessary. See the heading "Mailbox Commands" later in this section for more information on the mailbox structure.

Note: In 24-bit mode, the maximum accessible memory is 16 MBytes. In the 32-bit mode, accessible memory can be up to 4 GB. Refer to the host adapter command 81hex for 32-bit mode mailbox initialization.

Operation Code	Command	Parameter Byte Count	Direction
02	START MAILBOX COMMAND	None	None

Description. This command is normally issued every time the host makes an outgoing mailbox entry. Upon receipt of this command, the host adapter begins scanning for active outgoing mailbox entries and continues scanning until all outgoing mailbox entries have been serviced. This can be accomplished by either beginning the requested operations or queuing the commands and executing them later. To avoid unnecessary interrupt servicing by the host, the Command Complete bit (CMDC) is *not* set after receipt of this command. If this command is received before the Initialize Mailbox command, however, the host adapter will then set both the Command Invalid bit (CMDINV) and the Command Complete bit (CMDC) in the Status Register.

Operation Code	Command	Parameter Byte Count	Direction
03	START BIOS COMMAND	None	None

Warning: This command is reserved exclusively for the Host Adapter's BIOS and should NOT be used by application programs.

Description: This command is used exclusively by the host adapter's BIOS to communicate with the host adapter's firmware. No other HAC or mailbox commands can be running when this command is issued. Ten bytes follow the command byte and one is returned to provide the following info:

Out Byte	Description	
0	BIOS Command to execute (See BIOS Command table below)	
1	Drive Number	
	Bit	Meaning
	0-2	Logical Unit Number (LUN)
	3-4	Reserved
	5-7	Target SCSI ID
2	Cylinder number (MSB), 16-bit number	
3	Cylinder number (LSB)	
4	Head number, 4-bit number	
5	Sector number, 5-bit number (Logical block Address = Cylinder shifted left 9 times + Head shifted left 5 times + Sector)	
6	Transfer count in sectors	
7	Host DMA address (MSB)	
8	Host DMA address	
9	Host DMA address (LSB)	
IN Byte	Description	
0	Completion code (See Completion Code Table below)	

The BIOS Command table follows:

Code	Command	Description
00	Reset Disk System	This is a no operation command as the SCSI bus is reset when needed by the Host Adapter.
01	Read Status of Last Operation	The Host Adapter reports the status of the last operation performed by the specified disk. No SCSI activity occurs and the disk status is set to zero.

02	Read Desired Sectors into Memory	The requested sectors, calculated from the head/sector/cylinder parameters, are read from the specified disk to system memory. This function maps to a SCSI Read command (SCSI Opcode 28h).
03	Write Desired Sectors from Memory	The requested sectors, calculated from the head/sector/cylinder parameters, are written from system memory to the specified disk. This function maps to a SCSI Write command (SCSI Opcode 2Ah).
04	Verify Desired Sectors	The requested sectors, calculated from the head/sector/cylinder parameters, are verified to be written correctly on the SCSI disk. This function maps to a SCSI Verify command (SCSI Opcode 2Fh).
05	Format Track	This command is an invalid command as single tracks can not be accessed in SCSI.
06	Identify SCSI Devices	This is a no operation command as BIOS handles this without using the adapter.
07	Format Unit	The selected SCSI device formats its medium into addressable logical blocks. This function maps to a SCSI Format Unit command (SCSI Opcode 04h).
08	Read Drive Parameters	Returns stored Max LBA and block size for specified SCSI drive. (See Read Capacity below) as 6 bytes laid out as follows: 0 Max LBA (MSB) 1 Max LBA (MHI) 2 Max LBA (MLO) 3 Max LBA (LSB) 4 Size of drive block (LSB) 5 Size of drive block (MSB)
09	Initialize Drive Pair Characteristics	Because SCSI CCS drives are self-configuring, this is a no operation command.
0C	Seek	This function performs a Seek command (SCSI Opcode 2Bh) to the logical block address as calculated from the head, sector, and cylinder parameters. This command is not required for CCS commands nor for proper SCSI device operations. Because the Seek operation is performed automatically by the Read and Write operations, it is not necessary to generate a Seek command to access data.
0D	Alternate Disk Reset	This is a no operation command as SCSI devices are reset when needed by the Host Adapter.
10	Test Drive Ready	This function maps to a SCSI Test Unit Ready command (SCSI Opcode 00h). After executing a Reset function, the host adapter's BIOS issues this function internally until the target is no longer busy and the Unit Attention condition is cleared.
11	Recalibrate	This function maps to a Re-zero Unit command (SCSI Opcode 01h)
14	Controller Diagnostic	The Host Adapter will run an internal diagnostic.

15	Read DASD Type	This function returns the drive capacity found with the SCSI Read Capacity command (SCSI Opcode 25h) and the device type/RMB found with the SCSI Inquiry command (SCSI Opcode 12h). The data is returned as 6 bytes laid out as follows:
		0 Max LBA (MSB)
		1 Max LBA (MHI)
		2 Max LBA (MLO)
		3 Max LBA (LSB)
		4 Peripheral device type
		5 Removable Media Bit (RMB—bit 7)

The Completion Code table follows:

Status Reg	Meaning	SCSI Sense code
00	No error. Normal completion.	
01	Invalid Command Request.	
02	Address Mark Not Found	12—No Address Mark found on disk
03	Write Protect Error	21—Illegal Logical Block Address
04	Read Error	27—Write Protected
		14—No Record found
		16—Data Sync Error
10	Uncorrectable ECC Error	10—ID ECC Error
		11—Unrecoverable read error
11	ECC Corrected Data Error	17—Recovered Read Error w/o ECC
		18—Recovered Read Error w/ ECC
20	Controller Failure or one of and many Additional Sense Codes was returned from drive	01, 03, 05, 06, 07, 08, 09, 1B, 1C, 1D, 40 to 49
40	Seek Operation Failed	15—Seek Positioning Error
		02—No Seek Complete
80	Selection Time-Out	Drive did not respond to Host Adapter
AA	Device Not Ready	04—LUN Not Ready
		28—Medium Change
		29—Power On or Reset or Bus Device Reset occurred
BB	Unknown Target Sense Error	2A—Mode Select Parameter changed
		Unknown additional sense code from SCSI device
FF	Sense Operation Failed	No sense information from SCSI device

Operation Code	Command	Parameter Byte Count	Direction
04	INQUIRE BOARD ID	4	In

Description: Upon receipt of this command, the host adapter sends four bytes of data to the host which contain identification and revision information about itself. Refer to these byte contents:

Byte	Description	
0	BusLogic Board Type—value allows software support for PC/AT, PCI and Micro Channel BusLogic host adapters.	
	Hex Value	Meaning
	41	Board is a BT-54X, BT-74X, BT-44X, or BT-94X, BT-95X
	42	Board is a BT-640A with 64-head BIOS
	Other	Reserved

- 1 Custom Features—indicates what custom features may be supported by the host adapter.
- | Hex Value | Meaning |
|-----------|-----------------------|
| 41 | Standard host adapter |
| Other | Reserved |
- 2 Firmware Revision Level—a byte designating the revision level of the host adapter firmware. ASCII “0”–“9”
- 3 Firmware Version—2nd byte designating the revision level of the installed firmware
(2nd digit—also in HAC #8D byte 10).

Operation Code	Command	Parameter Byte Count	Direction
05	ENABLE OMBR INTERRUPT	1	Out

Description: This command specifies whether the Outgoing Mailbox Ready bit (OMBR) should be set when an outgoing mailbox entry is cleared by the host adapter. The single parameter byte from the host instructs the host adapter as follows:

Hex Value	Meaning
00	The Outgoing Mailbox Ready Interrupt bit (OMBR) is <i>not</i> to be set.
01	The Outgoing Mailbox Ready Interrupt bit (OMBR) is to be set once the outgoing mailbox has been cleared by the host adapter.

To avoid unnecessary interrupt servicing by the host, the Command Complete bit (CMDC) is not set after receipt of this command. If the parameter byte contains a value other than 00H or 01H, however, the Command Invalid bit (CMDINV) is set, as well as the Command Complete bit (CMDC), to indicate receipt of an invalid command.

Operation Code	Command	Parameter Byte Count	Direction
06	SET SCSI SELECTION TIME-OUT	4	Out

Description: This command specifies the wait time used to determine whether or not a SCSI selection was successful. If the SCSI Busy signal is *not* returned within the specified time-out period, the selection will be terminated and the appropriate error message recorded in the returned CCB. The contents of the four parameter bytes received with this command are as follows:

Byte	Description
0	Enable/Disable SCSI Selection Time-Out—specifies whether or not the SCSI Selection time-out is used. Refer to the following values.
Hex Value	Meaning
00	No time-out is performed.
01	The time specified in Bytes 02 and 03 is used as the SCSI time-out period.
1	Reserved—must be set to zero.
2–3	Time-Out Value—specifies the SCSI selection time-out period in milliseconds. The default value is 250 milliseconds. Byte 2 is the most significant byte.

After command completion, the Command Complete bit (CMDC) is set indicating normal command completion. The Command Invalid bit (CMDINV) is set only if data Byte 0 is invalid (neither 00H nor 01H) or data Byte 1 is not zero which indicates an invalid command.

Operation Code	Command	Parameter Byte Count	Direction
07	SET PREEEMPT TIME ON BUS	1	Out

Description: This command specifies the time the host adapter is allowed on the bus after being preempted. One parameter byte is sent to the host adapter indicating the length of time in microseconds. This time can be from 2 to 15 microseconds. The default value is 7 microseconds. After command completion, the Command Complete bit (CMDC) is set indicating normal command completion. If the data byte value is greater than 15, the Command Invalid bit (CMDINV) is set indicating that an invalid command was received.

This command is used for EISA bus (preempt time) or ISA, VL-Bus, or MCA (bus on time). It is not applicable to PCI bus. The PCI latency timer is assigned in the PCI configuration space during power up or system reboot.

Operation Code	Command	Parameter Byte Count	Direction
08	SET TIME OFF BUS	1	Out

Description: This command specifies the time the host adapter will spend off the bus. One parameter byte is sent to the host adapter indicating the length of time in microseconds. This command is treated as a no operation command. It is supported for software compatibility to ISA software.

Operation Code	Command	Parameter Byte Count	Direction
09	SET BUS TRANSFER RATE	1	Out

Description. This command is treated as a no operation command. It is supported for software compatibility to ISA software.

Note: Commands 07, 08, and 09 applied to non-PCI host adapters only.

Operation Code	Command	Parameter Byte Count	Direction
0A	INQUIRE INSTALLED DEVICES ID 0–7	8	In

Description: This command asks the host adapter to indicate the devices connected to the SCSI bus. The host adapter issues the SCSI Test Unit Ready command to each target/Logical Unit Number (LUN) combination and reports the results using eight bytes of data returned to the host through the Data In Register. Each byte has an associated target device; i.e., Byte 2 represents Target 2. If a bit has a value of one, the associated LU (Logical Unit) is installed. Each bit within a byte has an associated LU; i.e., Bit 3 represents LU 3, etc.

The byte associated with the host adapter will always be zero. Once all information has been transferred, the Command Complete bit (CMDC) is set to indicate normal command completion.

For target ID 8–15, refer to command 23h.

Operation Code	Command	Parameter Byte Count	Direction
0B	INQUIRE CONFIGURATION	3	In

Description: The host adapter returns three bytes of data describing the host DMA channel, the interrupt channel, and the SCSI ID values set during configuration set up.

Except for BusLogic ISA host adapters, BusLogic adapters do not use the ISA DMA channels but may still be required to support the ISA software command Inquire Configuration. This command requires the adapter to specify an ISA DMA channel which is used during host data transfers. ISA software programs the requested DMA channel to function in cascade mode and enables it to receive DMA requests. The adapter's response to the Inquire Configuration command is a configurable option described in the adapter user's guide. Most ISA software executes

properly when the adapter specifies no DMA channel in response to this command. Some ISA software, however, requires a specific DMA channel (DRQ5, DRQ6, or DRQ7) to be selected. Because the specification requires the host system hardware to pull down (deassert) the DRQ lines this option also functions properly. The ISA software believes 16-bit DMA transfers are taking place while the adapter performs 32-bit bus master transfers.

Byte	Description	Byte	Description	Byte	Description
0	Host DMA channel	1	Interrupt channel	2	SCSI ID
	Bit 0 = Reserved		Bit 0 = IRQ9		Bit 0-2 = SCSI ID, binary value
	Bit 1 = Reserved		Bit 1 = IRQ10		Bit 3-7 = Reserved, set to zero
	Bit 2 = Reserved		Bit 2 = IRQ11		
	Bit 3 = Reserved		Bit 3 = IRQ12		
	Bit 4 = Reserved		Bit 4 = Reserved		
	Bit 5 = DMA Channel 5		Bit 5 = IRQ14		
	Bit 6 = DMA Channel 6		Bit 6 = IRQ15		
	Bit 7 = DMA Channel 7		Bit 7 = Reserved		

Note: For PCI adapters, the IRQ may range from 1 to 254. If IRQ is not assigned from 9 to 15, it is recommended that the host software read the IRQ value directly from the PCI configuration space.

Operation Code	Command	Parameter Byte Count	Direction
0C	TARGET MODE ENABLE/ DISABLE	1	Out

Description: Some Host Adapters support initiator as well as target mode operation. By default, the target mode is disabled. The host system needs to send this command in order to enable the target mode operation. Host Adapters that do not have target mode support will return with illegal command error code.

Byte	Description
0	0: Disable Target mode 1: Enable Target mode
1	LUN for target mode

Note: This command is not supported for PCI adapters.

Operation Code	Command	Parameter Byte Count	Direction
0D	INQUIRE SETUP INFORMATION	1 Byte Count	Out In

Description: This command asks the host adapter to provide information on its the current set-up status. This command is followed by a parameter which specifies the number of bytes which the host adapter will send to the host.

Parameter Byte	
Byte	Description
0	Specifies the number of data bytes, from 0 to 255, to be sent to the host.

Data In Byte/Bit Assignments

Byte	Description	
0	SCSI synchronous negotiation and parity status.	
Byte	Bit	Meaning
	0	0: SCSI sync negotiation will NOT be initiated by the Host Adapter. 1: SCSI sync negotiation will be initiated by the Host Adapter when appropriate.
	1	0: Disable parity check on inbound SCSI transfer. 1: Enable parity check on inbound SCSI transfer.
	2–7	Reserved (zero).
1	BUS TRANSFER RATE—Returns the value set by the Set Bus Transfer Rate command. (not applicable to PCI adapters)	
2	TIME ON BUS—Returns the time set by the Set Time On Bus command. (not applicable to PCI adapters)	
3	TIME OFF BUS—Indicates the time set by the Set Time Off Bus command. (not applicable to PCI adapters)	
4	NUMBER OF MAILBOXES—Returns the number of mailboxes established by a previous Initialize Mailbox command. If the Initialize Mailbox command has not yet been completed successfully, the returned number will be 00H.	
5–7	Base Mailbox Address—Returns the base address of the mailbox array established by a previous Initialize Mailbox command. The MSB is Byte 5. If the Initialize Mailbox command has not been completed successfully, these bytes have no meaning.	
8	SYNCHRONOUS VALUES FOR TARGET 0—Contains information resulting from synchronous negotiation with Target 0. If the address is that of the host adapter or a non-existent target, this byte will contain 00H.	
Byte	Bit	Meaning
	0–3	Contain the negotiated offset value, normally between 1 and 15.
	4–6	Contain a value between 0 and 7 that defines the synchronous transfer period according to the following equation. $\text{Period} = 200 + 50 \text{ (value)} \text{ nanoseconds.}$
	7	Set (one) if synchronous transfer is negotiated. Reset (zero) if asynchronous transfers are used.

The following bytes have the same structure as Byte 8, but for Targets 1-7.

9	SYNCHRONOUS VALUES FOR TARGET 1—Same as byte 8 but for target 1.
10	SYNCHRONOUS VALUES FOR TARGET 2—Same as byte 8 but for target 2.
11	SYNCHRONOUS VALUES FOR TARGET 3—Same as byte 8 but for target 3.
12	SYNCHRONOUS VALUES FOR TARGET 4—Same as byte 8 but for target 4.
13	SYNCHRONOUS VALUES FOR TARGET 5—Same as byte 8 but for target 5.
14	SYNCHRONOUS VALUES FOR TARGET 6—Same as byte 8 but for target 6.
15	SYNCHRONOUS VALUES FOR TARGET 7—Same as byte 8 but for target 7.
16	State of SCSI Disconnection Option—Each bit corresponds to a SCSI device (e.g. Bit 0 represents the SCSI device assigned to SCSI address 0). When the bit is set, the Host Adapter will prevent the corresponding SCSI device from disconnecting. When the bit is reset, the Host Adapter will allow the corresponding SCSI device to disconnect. For setting, see byte 1 of the Set Adapter Options command (Byte 1, Opcode 21h) below.
17	BusLogic or Special Customer Signature “B”: BusLogic Generic Products “S”: Customized for SDI “D”: Customized for ADIC
18	ASCII Character “D”.

19	Host Bus Type
"A"	ISA
"B"	MCA
"C"	EISA
"D"	NUBUS
"E"	VESA
"F"	PCI
20	Reserved—set to zero
21	Reserved—set to zero
22	Synchronous Value for Target 8—Same as byte 8, but for target 8
23	Synchronous Value for Target 9—Same as byte 8, but for target 9
24	Synchronous Value for Target 10—Same as byte 8, but for target 10
25	Synchronous Value for Target 11—Same as byte 8, but for target 11
26	Synchronous Value for Target 12—Same as byte 8, but for target 12
27	Synchronous Value for Target 13—Same as byte 8, but for target 13
28	Synchronous Value for Target 14—Same as byte 8, but for target 14
29	Synchronous Value for Target 15—Same as byte 8, but for target 15
30	State of SCSI Disconnection Option for targets 8–15 (For setting, see Byte 3, Opcode 21h below)

Note: For Fast and Ultra SCSI devices, the synchronous transfer period is no longer valid. Use command (8C) to retrieve the exact value.

Operation Code	Command	Parameter Byte Count	Direction
1A	WRITE ADAPTER LOCAL RAM	3	Out

Description: The three parameter bytes contain a 24-bit address (first parameter byte is MSB) which points to a 64-byte area in the main system memory. Upon receipt of this command the host adapter performs a bus master data transfer of the designated 64 bytes from the host's main memory into its own local RAM memory. Once the 64 bytes have been successfully transferred to the host adapter, the Command Complete bit (CMDC) is set indicating that this command has been completed.

Operation Code	Command	Parameter Byte Count	Direction
1B	READ ADAPTER LOCAL RAM	3	Out

Description: The three parameter bytes contain a 24-bit address (first parameter byte is MSB) which points to a 64-byte area in the main system memory. Upon receipt of this command the host adapter performs a bus master data transfer of 64 bytes of data from its own local RAM into the designated 64 bytes in the host's main memory. Once the 64 bytes have been successfully transferred to the host's memory, the Command Complete bit (CMDC) is set indicating that this command has been completed.

Operation Code	Command	Parameter Byte Count	Direction
1C	WRITE BUS MASTER CHIP FIFO	3	Out

Description: The three parameter bytes contain a 24-bit address (first parameter byte is MSB) which points to a 64-byte area in main system memory. Upon receipt of this command the host adapter performs a bus master data transfer of the designated 64 bytes from the host's main memory into its own bus master chip FIFO. Once the 64 bytes have been successfully transferred to the host adapter, the Command Complete bit (CMDC) is set indicating that this command has been completed.

Operation Code	Command	Parameter Byte Count	Direction
1D	READ BUS MASTER CHIP FIFO	3	Out

Description: The three parameter bytes contain a 24-bit address (first parameter byte is MSB) which points to a 64-byte area in the main system memory. Upon receipt of this command the host adapter performs a bus master data transfer of 64 bytes of data from its bus master chip FIFO into the designated 64 bytes in the host's main memory. Once the 64 bytes have been successfully transferred to the host's memory, the Command Complete bit (CMDC) is set indicating that this command has been completed.

Operation Code	Command	Parameter Byte Count	Direction
1F	ECHO COMMAND DATA	1 1	Out In

Description: This command is used to test the Command/Parameter and Data In Registers and the associated control bits in the remaining I/O registers. The host adapter receives one parameter byte in the Command/Parameter Register and then instructs the host to read the same byte back from the Data In Register by setting the Data In Register Ready bit (DIRRDY). After the host has read the byte, the Command Complete bit (CMDC) is set indicating that this command has been completed.

Operation Code	Command	Parameter Byte Count	Direction
20	HOST ADAPTER DIAGNOSTIC	0 0	Out In

Description: This command instructs the host adapter to conduct its self-diagnostic tests. A hard reset of the host adapter will occur without issuing a SCSI bus reset. After this command is executed, the host adapter must be reinitialized before normal operation can continue. After issuing this command, the host should monitor the host adapter's Status Register to obtain this command's status. It should also wait until the Diagnostic Active bit (DACT) of the Status Register is reset indicating that the self-diagnostics have been completed successfully. It then should wait for one or more of the following bits to be set: the Diagnostic Failure bit (DFAIL), the Host Adapter Ready bit (HARDY), or the Data In Register Ready bit (DIRRDY). If the Host Adapter Ready bit (HARDY) is set and the Diagnostic Failure bit (DFAIL) is reset, then an error did not occur during the diagnostics.

If the Diagnostic Failure bit (DFAIL) or the Data In Register Ready bit (DIRRDY) is set, then an error did occur during the diagnostics. In this case, after the Data In Register Ready bit (DIRRDY) is set, then the Data In Register should be read for the error code that will equal the number of failed diagnostic tests. No data byte is returned if there is no error. When this command is completed, the Interrupt Register will be updated as follows: the Command Complete bit (CMDC) and the Interrupt Valid bit (INTV) will be set.

Operation Code	Command	Parameter Byte Count	Direction
21	SET ADAPTER OPTIONS	5	Out

Description: The host can use this command to specify certain configuration options for the host adapter. The host sends the specified configuration options to the host adapter via a parameter list. This five-byte parameter list follows the command opcode. The parameter list is as follows:

Parameter Byte

Byte Description

- | | |
|---|--|
| 0 | Specifies the number of bytes remaining in the parameter list. This specified length equals the total number of bytes in the parameter list minus one. |
|---|--|

- 1 Disables the SCSI disconnection option. Each bit corresponds to a SCSI device (e.g., Bit 0 represents the SCSI device assigned to SCSI address 0). When the bit is set, the host adapter will prevent the corresponding SCSI device from disconnecting. When the bit is reset, the host adapter will allow the corresponding SCSI device to disconnect. Byte 16 of the Inquire Setup command reflects the state of this byte.
- 2 Disables the SCSI Busy retry option. Each bit corresponds to a SCSI device (e.g., Bit 0 represents the SCSI device assigned to SCSI address 0). When the bit is set, the host adapter will prevent the corresponding SCSI device from being retried when the SCSI device returns a Busy status. When the bit is reset, the host adapter will allow the corresponding SCSI device to be retried when the SCSI device returns a Busy status.
- 3 Disables the SCSI disconnection option (Target IDs 8–15). Each bit corresponds to a SCSI device (e.g. Bit 0 represents the SCSI device assigned to SCSI address 8). When the bit is set, the Host Adapter will prevent the corresponding SCSI device from disconnecting. When the bit is reset, the Host Adapter will allow the corresponding SCSI device to disconnect. Byte 30 of the Inquire Setup command (Opcode 0Dh) above reflects the status of this byte.
- 4 Disables the SCSI Busy retry option (Target IDs 8–15). Each bit corresponds to a SCSI device (e.g. Bit 0 represents the SCSI device assigned to SCSI address 8). When the bit is set, the Host Adapter will prevent the corresponding SCSI device from being retried when the SCSI device returns a Busy status. When the bit is reset, the Host Adapter will allow the corresponding SCSI device to be retried when the SCSI device returns a Busy status.

Operation Code	Command	Parameter Byte Count	Direction
23	INQUIRE INSTALLED DEVICES ID 8–15	8	In

Description: The host adapter will check if any devices are attached at Target ID 8–15 on the SCSI bus. Each byte is associated with a Target ID; each bit is associated with a LUN. For example, if set to byte 0:bit 0, it indicates Target 8:LUN 0 is installed. If set to byte 7: bit7, it indicates that Target ID 15: LUN 7 is installed.

The byte associated with the host adapter will always be zero. Once all information has been transferred, the Command complete bit (CMDC) is set to indicate normal command completion.

For target ID 0–7, refer to command 0Ah.

Operation Code	Command	Parameter Byte Count	Direction
24	INQUIRE TARGET DEVICES	2	In

Description: This command asks the Host Adapter to indicate the target devices connected to the SCSI bus. Unlike command 0Ah and 23h, this command only inquires LUN 0 on the target ID. The Host Adapter reports the results using two bytes of data returned to the host through the Data In Register as follows:

Byte	Description
0	Targets 0–7 mapped to bits 0–7 (0 = unused, 1 = installed)
1	Targets 8–15 mapped to bits 0–7 (0 = unused, 1 = installed)

Operation Code	Command	Parameter Byte Count	Direction
25	DISABLE HOST HAC INTERRUPT 1	1	Out

Description: This command can turn host HAC interrupts on or off depending on the parameter byte. If the byte is zero, the interrupts are disabled. If the byte is non-zero, the interrupts are enabled.

Operation Code	Command	Parameter Byte Count	Direction
81	INITIALIZE EXTENDED MAILBOX 5 (EXTENDED)		Out

Description: Use the host adapter command 81H to send the host adapter a new command called **Initialize Extended Mailbox**. This command is just like the original Initialize Mailbox command except that it sends a one-byte mailbox count followed by a four-byte, 32-bit address pointing to the first mailbox that can be located anywhere within the 4 Gigabyte memory range. The description of the bytes is as follows:

Byte	Description
0	Mailbox count(Greater than 0)
1	Base Mailbox Address(LSB)
2	Base Mailbox Address
3	Base Mailbox Address
4	Base Mailbox Address(MSB)

The software driver may return the host adapter to the original 24-bit address mode using old data structures by issuing the Initialize Mailbox command (01H).

Operation Code	Command	Parameter Byte Count	Direction
83	Execute SCSI Command	11 + CDB Length 4	Out In

Warning: This command is reserved exclusively for the Host Adapter's BIOS and should NOT be used by application programs!

Description: This extended command is used by the Host Adapter's BIOS to issue single threaded SCSI commands via the host adapter's firmware.

Out	Byte	Description
	0	Data Buffer Length (LSB)
	1	Data Buffer Length (MLO)
	2	Data Buffer Length (MHI)
	3	Data Buffer Length (MSB)
	4	Host Data Buffer Address (LSB)
	5	Host Data Buffer Address (MLO)
	6	Host Data Buffer Address (MHI)
	7	Host Data Buffer Address (MSB)
	8	Target (SCSI address)
	9	LUN (Logical Unit Number)
	10	CCB Control
	Bit	Meaning
	0-2	Not used—set to zero
	3-4	Set to determine the direction of data transfer as follows: Initiator CCB
	Bit 3 Bit 4	Host Adapter Action
	0 0	Direction of data transfer determined by the SCSI command being executed.
	0 1	Data transferred from SCSI device to Host Adapter during Data In Phase and length will be checked.
	1 0	Data transferred from Host Adapter to SCSI device during Data Out Phase and length will be checked.
	5-7	Not used—set to zero
11		Number of bytes in CDB
12+		CDB

In	Byte	Description
0		Reserved
1		Reserved
2		Host Adapter Status
3		SCSI Device Status

Operation Code	Command	Parameter Byte Count	Direction
84	INQUIRE FW VERSION (Extended)	1	In

Description: This extended command returns the third ASCII digit of firmware revision.

Operation Code	Command	Parameter Byte Count	Direction
85	INQUIRE FW VERSION (Extended)	1	In

Description: This extended command returns the fourth ASCII digit of firmware revision.

Operation Code	Command	Parameter Byte Count	Direction
86	INQUIRE ISA COMPATIBLE I/O ADDRESS, IRQ SETTING, AND/GENERIC I/O PORT SETTING	4	In

Description: This command returns the ISA compatible I/O port address, the IRQ setting, and the generic I/O Port setting for PCI compliant products. Any non-PCI BusLogic Host Adapter will reject this command with an invalid command error. The ISA compatible I/O port address can be changed using HAC Opcode 95h.

Byte	Description	
0	ISA Compatible I/O port address index	
	Hex Value	Meaning
	00h	I/O port address 330H
	01h	I/O port address 334H
	02h	I/O port address 230H
	03h	I/O port address 234H
	04h	I/O port address 130H
	05h	I/O port address 134H
	06h	Reserved
	07h	Reserved
	FFh	I/O port address unknown
1	PCI assigned IRQ channel number (00h-FFh from Interrupt Line Register).	
2	Host Adapter Generic I/O Port Settings. If bytes 2 and 3 are not supported, bit 7 of this byte will be zero. This byte contains the current settings of the Host Adapter's generic I/O ports. This byte can be used by AutoSCSI or software utilities to monitor the settings of the Host Adapter.	
Bit	Meaning	
0	Low Byte termination status (0 = disabled, 1 = enabled)	
1	High Byte termination status (0 = disabled, 1 = enabled)	
2-3	Reserved (set to zero)	

4	JP1 jumper status (0 = open, 1 = close)
5	JP2 jumper status (0 = open, 1 = close)
6	JP3 jumper status (0 = open, 1 = close)
7	Bytes 2 and 3 Validity (0 = invalid, 1 = valid)
3	Reserved for Future Generic I/O Port Settings (set to zero).

Operation Code	Command	Parameter Byte Count	Direction
8B	INQUIRE CONTROLLER MODEL NUMBER (EXTENDED)	1 Byte Count	Out In

Description: This command returns the controller model number in ASCII. The command is followed by a parameter which specifies the number of bytes which the Host Adapter will send to the host.

Out	Byte	Description
	0	Byte count to be returned (normally 5).
In	Byte	Description
	0-4	Host Adapter model number in ASCII
	5-N	If byte count is greater than 5, then these bytes are set to zero (N is byte count minus one).

Operation Code	Command	Parameter Byte Count	Direction
8C	TARGET SYNC INFORMATION (EXTENDED)	1 Target Count	Out In

Description: This command returns each target's current SYNC period in 10 nanosecond increments. If no target or target not using synchronous data, a zero will be returned.

Out	Byte	Description
	0	Byte count to be returned.
In	Byte	Description
	0	SYNC period for target 0 in 10 ns units.
	1	SYNC period for target 1 in 10 ns units.
	2	SYNC period for target 2 in 10 ns units.
	3	SYNC period for target 3 in 10 ns units.
	:	
	:	
	N	SYNC period for target N in 10 ns units (where N = byte count - 1).

Operation Code	Command	Parameter Byte Count	Direction
8D	INQUIRE EXTENDED SETUP INFORMATION (Extended)	1 Byte Count	Out In

Description. This command returns information on the Host Adapter's current setup status. This command is followed by a parameter which specifies the number of bytes which the Host Adapter will send to the host.

Out	Byte	Description
	0	Byte count to be returned (0 to 255).

In	Byte	Description																						
	0	ASCII code specifying Host Adapter buss type <table> <thead> <tr> <th>Value</th><th>Meaning</th></tr> </thead> <tbody> <tr> <td>"A"</td><td>PC/AT or ISA</td></tr> <tr> <td>"E"</td><td>EISA or PCI</td></tr> <tr> <td>"M"</td><td>Micro channel</td></tr> </tbody> </table>	Value	Meaning	"A"	PC/AT or ISA	"E"	EISA or PCI	"M"	Micro channel														
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CCh	0CC000h																							
D0h	0D0000h																							
D4h	0D4000h																							
D8h	0D8000h																							
DCh	0DC000h																							
	2-3	Maximum number of segments permitted in the scatter-gather list for the Host Adapter (BusLogic presently defaults to 8192). Byte 2 is LSB Byte 3 is MSB																						
	4	Number of mailboxes allocated by the host.																						
	5-8	Mailbox base address with byte 5 LSB and byte 8 MSB.																						
	9	Configuration register: register D for EISA, trigger level for PCI, and reserved for all others. <table> <thead> <tr> <th>Bus</th><th>Usage</th></tr> </thead> <tbody> <tr> <td>EISA</td><td>Configuration register D as follows:</td></tr> <tr> <th>Bit</th><th>Meaning</th></tr> <tr> <td>1-0</td><td>Reserved</td></tr> <tr> <td>2</td><td>0: Sync negotiated start at 5 MB/s 1: Sync negotiated start at 10 MB/s</td></tr> <tr> <td>3</td><td>0: Floppy enabled 1: Floppy disabled</td></tr> <tr> <td>4</td><td>0: Floppy primary port (3F0h to 3F7h) 1: Floppy secondary port(370h to 377h)</td></tr> <tr> <td>5</td><td>0: EISA Buss burst mode disabled 1: EISA Buss burst mode enabled</td></tr> <tr> <td>6</td><td>0: Interrupt edge trigger 1: Interrupt level trigger</td></tr> <tr> <td>7</td><td>Reserved Bit 6 indicates interrupt trigger mode 0: edge trigger 1: level trigger all others Reserved (set to zero)</td></tr> <tr> <td>PCI</td><td></td></tr> </tbody> </table>	Bus	Usage	EISA	Configuration register D as follows:	Bit	Meaning	1-0	Reserved	2	0: Sync negotiated start at 5 MB/s 1: Sync negotiated start at 10 MB/s	3	0: Floppy enabled 1: Floppy disabled	4	0: Floppy primary port (3F0h to 3F7h) 1: Floppy secondary port(370h to 377h)	5	0: EISA Buss burst mode disabled 1: EISA Buss burst mode enabled	6	0: Interrupt edge trigger 1: Interrupt level trigger	7	Reserved Bit 6 indicates interrupt trigger mode 0: edge trigger 1: level trigger all others Reserved (set to zero)	PCI	
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PCI																								
	10-12	Firmware revision number in ASCII with byte 10 holding the 2nd digit, byte 11 holding the 3rd digit, and byte 12 holding the 4th digit. Note the redundancy for fetching the version number: the 1st and 2nd digits can be retrieved with HAC Opcode 04h, 3rd digit with Opcode 84h, and 4th digit with HAC Opcode 85h.																						
	13	Extended SCSI Options: <table> <thead> <tr> <th>Bit</th><th>Meaning</th></tr> </thead> <tbody> <tr> <td>0</td><td>0: Narrow SCSI Host Adapter 1: Wide SCSI Host Adapter</td></tr> <tr> <td>1</td><td>0: Single Ended Host Adapter 1: Differential Host Adapter</td></tr> <tr> <td>2</td><td>0: Hard configuration only 1: SCAM (SCSI Configured Automatically)</td></tr> <tr> <td>3</td><td>0: Fast SCSI 1: Ultra SCSI</td></tr> <tr> <td>4</td><td>0: Software controlled termination 1: Auto-detected termination (smart termination)</td></tr> <tr> <td>5-7</td><td>Reserved (set to zero)</td></tr> </tbody> </table>	Bit	Meaning	0	0: Narrow SCSI Host Adapter 1: Wide SCSI Host Adapter	1	0: Single Ended Host Adapter 1: Differential Host Adapter	2	0: Hard configuration only 1: SCAM (SCSI Configured Automatically)	3	0: Fast SCSI 1: Ultra SCSI	4	0: Software controlled termination 1: Auto-detected termination (smart termination)	5-7	Reserved (set to zero)								
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5-7	Reserved (set to zero)																							

Operation Code	Command	Parameter Byte Count	Direction
8F	ENABLE STRICT ROUND ROBIN MODE	1	Out

Description: BusLogic host adapters provide two modes for processing outgoing mailboxes.

Parameter Byte

Byte Description

- | | |
|---|---|
| 0 | 0=Strict Round Robin Mode. In this mode the host adapter firmware maintains a round robin outgoing mailbox pointer. During the outgoing mailbox scanning process, the host adapter only examines the mailbox pointed by the pointer. If that mailbox is active, then the firmware will process it and the pointer is advanced to the next mailbox address. This method guarantees that commands sent to the same target will be executed in the order sent by the host. |
| | 1=Aggressive Round Robin Mode. In this mode the host adapter firmware follows a round robin sequence to hunt for the outgoing mailbox. However, if the current outgoing mailbox pointed by the pointer is not active, the firmware will continue to advance the pointer to scan the next mailbox until the entire outgoing mailbox structure is tested. The mode is implemented because there are existing device drivers that do not use a strict round robin sequence to update outgoing mailboxes. This method does not guarantee that commands sent to the same target will be executed in the order they were written to the mailbox structure. Setting the mode for strict round robin where the device driver does not support it, also offers no guarantee that the commands will be processed in the order they are sent. |

Operation Code	Command	Parameter Byte Count	Direction
90	STORE HOST ADAPTER LOCAL RAM	2 + Data Bytes	Out

Description: This command stores data in the Host Adapter's Accessible Memory Map. This Accessible Memory Map includes BIOS scratch RAM (64 bytes) and AutoSCSI data (64 bytes). (See Accessible Memory Map at end of this section).

Byte Description

- | | |
|-----|--|
| 0 | Offset into Host Adapter local RAM. |
| 1 | Number of data bytes to store |
| 2 | Data byte 0 |
| 3 | Data byte 1 |
| : | |
| : | |
| N+2 | Data byte N (where N = number specified in byte 1 above) |

Note: To write AutoSCSI data, use this command to store the desired operating values in the AutoSCSI area of local RAM and then use HAC command 92h below with the parameter set to one (1) to save these values into EEPROM/Flash ROM.

Operation Code	Command	Parameter Byte Count	Direction
91	FETCH HOST ADAPTER LOCAL RAM	2 Byte Count	Out In

Description: This command fetches data from the Host Adapter's Accessible Memory Map in local RAM. This Accessible Memory Map includes BIOS scratch RAM (64 bytes) and AutoSCSI data (64 bytes). (See Accessible Memory Map at end of this section).

Out Byte Description

- | | |
|---|-------------------------------------|
| 0 | Offset into Host Adapter local RAM. |
| 1 | Number of data bytes to fetch |

In	Byte	Description
	0	Data byte 0
	1	Data byte 1
	:	
	:	
	N	Data byte N (where N = number of data bytes desired)

Operation Code	Command	Parameter Byte Count	Direction
92	STORE LOCAL DATA IN EEPROM OR FLASH ROM	1	Out

Description: This command will either store one of several sets of default values into the AutoSCSI area of the Host Adapter's local RAM (See Accessible Memory Map at end of this section) or program EEPROM or Flash ROM with the current operating values stored in the AutoSCSI area. To read EEPROM/Flash ROM, use HAC command 91h above. To write EEPROM/Flash ROM, use HAC command 90h above to store the desired operating values in local RAM and then use this command with the parameter set to one (1) to save in EEPROM/Flash ROM.

Byte	Description
0	0 = Load factory defaults into the current operating values in RAM
	1 = Burn current operating values in RAM into EEPROM or Flash ROM
	2 = Load optimum defaults into the current operating values in RAM
	3 = Load safe defaults into the current operating values in RAM

The 3 sets of default values vary from product to product. Firmware is responsible for choosing the right parameters for each default which are described below:

Factory defaults	Most used default values, i.e. sync/fast transfer, parity check, etc.
Optimum defaults:	Performance/Feature optimum default values, i.e. Ultra SCSI, SCAM, Wide SCSI, etc.
Safe defaults	Absolutely safe default values to avoid compatibility problems, i.e. Async, no parity check, no SCAM, no Wide negotiation, no INT13 extension, etc.

Operation Code	Command	Parameter Byte Count	Direction
94	UPLOAD AUTOSCSI CODE	3 Byte Count	Out In

Description: This command copies the AutoSCSI code to the host through the Data In Register byte by byte.

Out	Byte	Description
	0	Mode 0—Fetch AutoSCSI code 1+ —Illegal value
	1	Byte Count LSB
	2	Byte Count MSB
In	Byte	Description
	0-N	AutoSCSI code (where N = Byte Count - 1)

Note: The size of AutoSCSI program code could be 16K or 32K.

Operation Code	Command	Parameter Byte Count	Direction
95	MODIFY PCI I/O ADDRESS	1	Out

Description: This command is valid for PCI Host Adapters only. To be PCI compliant, the Host Adapter's registers are assigned addresses by the host system's BIOS. These addresses are not compatible with the old base addresses. So the Host Adapter allows the old base address to be configured in addition to PCI assigned address and the Host Adapter will recognize both sets of addresses. This command allows host software to re-assign the Host adapter's compatible register address as follows:

Byte	Description	
0	New I/O base address index	
	Value	Meaning
	00	Base address of 330h
	01	Base address of 334h
	02	Base address of 230h
	03	Base address of 234h
	04	Base address of 130h
	05	Base address of 134h
	06	Disable I/O address
	07	Disable I/O address
	08–255	Reserved

Note: No interrupt is generated at the completion of this command. The completion status will be reflected at the PCI compliant address and the new compatible I/O address. The presently used compatible I/O address can be fetched with HAC Opcode 86h.

Operation Code	Command	Parameter Byte Count	Direction
96	SET 64 LUN CCB Format	1	Out

Description. This command defines the two 32-bit Mode CCB formats. The main difference between these two formats is that format 0, the default format, addresses SCSI LUN devices up to LUN 7; while format 1, 64 LUN CCB format, can address the SCSI LUN devices from LUN 0 up to LUN 63. Refer to Table 1-6 for detailed 64 LUN CCB format (page 1-55).

Parameter Byte	
Byte	Description
0	0=Uses 8 LUN CCB Format
	1=Uses 64 LUN CCB Format

Note: This command only applies to 32-bit Mode CCB operation.

Operation Code	Command	Parameter Byte Count	Direction
97	Flash ROM Download	10 + Byte Count	Out

Description: This command is used to download Firmware, BIOS, or AutoSCSI, etc. to the Host Adapter's erasable/programmable memory. This command assumes that the write or read path to the programmable memory, such as flash ROM or NVRAM, is accessible to the Host Adapter's Firmware.

Command Block:

Byte	Meaning	Description
0	Command 3Bh 3Ch Reserved	Indicates direction of transfer. Commands are: Write to Host Adapter's buffer for downloading Only one mode is supported.
1	Mode bits 0–2 bits 3–7	Indicates command mode and data format. 010 binary, Vendor Unique Data Reserved (set to zero)
2	Buffer ID 43h	Identify a specific buffer in controller. Combination ROM (Firmware, AutoSCSI, BIOS) All other values are reserved
3–5	Buffer Offset	Byte offset from start of the selected buffer with byte 3 MSB and byte 5 LSB.
6–8	Allocation Length	Number of data bytes to transfer with byte 6 MSB and byte 8 LSB.
9		Reserved. Set to zero.

Data Block:

Out: Data direction and the number of bytes depend on the parameters set in the command block above. If multiple commands are needed to download or upload code data then each one needs to be preceded by the following header:

Byte	# of Bytes	Description
00–07	8	Vendor Identification "BusLogic"
08–23	16	Product Identification, e.g. BT-958, with zeros to pad the field
24–27	4	Product Revision Level, e.g. "1.00", with zeros to pad the field
28–31	4	Compatibility Group Code (Firmware vs. Hardware compatibility)
32–55	24	Reserved (set to zero)
56–59	4	Total Code Size in Bytes with byte 56 MSB and byte 59 LSB
60–63	4	Code Piece Checksum with byte 60 MSB and byte 63 LSB
64–N		Code Piece (where N = Allocation Length - 1)

Note: For 9x8 products, the host adapter will receive 128K of data, but only 112K of flash ROM is updated. The remaining 16K space (which is bootstrap + skeleton code and AutoSCSI/SCAM non-volatile data) remain intact. To update this 16K space, HAC command A7h should be used. After flash code is downloaded, the FW continue to be functional, the new code will not be run until a HDRST is received, then, the FW will copy the new code to the operating RAM and execute the new code.

HAC command 98h should be issued prior to this command to enable the Flash download.

Operation Code	Command	Parameter Byte Count	Direction
98	ENABLE/DISABLE FLASH ROM MEMORY WRITE	1	Out

Description: This command is used only by Host Adapters that allow the host to program the Firmware, BIOS and/or AutoSCSI Flash memory directly. If the Flash memory is accessible by the Firmware, e.g. 9x8 products, the host should follow with HAC command 97h instead.

Byte	Description
0	0: Disable Flash memory write 1: Enable Flash memory write

Note: The downloading utility should send this command to enable the write before programming the Flash memory. After the Flash memory is programmed, this command should be resent to disable the write, preventing inadvertent erasure or over-writing of the Flash memory.

Operation Code	Command	Parameter Byte Count	Direction
9A	WRITE INQUIRY BUFFER	4	Out

Description: This command is used to transfer 64 bytes from the host's main memory to the local inquiry buffer in the Host Adapter. Upon receipt of this command, the Host Adapter performs a bus master transfer of the designated 64 bytes. The four parameter bytes contain the 32-bit address in the host's main memory as follows:

Byte	Description
0	LSB
1	MLO
2	MHI
3	MSB

Operation Code	Command	Parameter Byte Count	Direction
9B	READ INQUIRY BUFFER	4	Out

Description: This command is used to transfer 64 bytes from the Host Adapter's local inquiry buffer to the host's main memory. Upon receipt of this command, the Host Adapter performs a bus master transfer of the designated 64 bytes. The four parameter bytes contain the 32-bit address in the host's main memory as follows:

Byte	Description
0	LSB
1	MLO
2	MHI
3	MSB

Operation Code	Command	Parameter Byte Count	Direction
A7 (9x8 specific)	FLASH ROM DOWNLOAD	10 + Byte Count	Out

Description: This host adapter command have the same definition of HAC 97h, except it will write out the whole 128K byte of data to the flash PROM, i.e. including AutoSCSI and SCAM data, Skeleton and BootStrip code. Please refer to HAC 97h for detailed information.

After flash code is downloaded, the FW continue to be functional, the new code will not be run until a HDRST is received, then, the FW will copy the new code to the operating RAM and execute the new code.

Operation Code	Command	Parameter Byte Count	Direction
A8 (9x8 specific)	READ SCAM DATA	4 Byte Count	Out In

Description: This command returns data from the Host Adapter's SCAM information stored in NVRAM, FlashROM or E2PROM. The SCAM data format follows:

00h-1Fh	32 bytes SCAM Initiator ID w/ Manufacturing S/N number
20h-FFh	Reserved for future SCAM Master
100h-2FFh	512 byte Target SCAM device ID string—32 bytes for each ID
300h-FFFFh	Reserved for future expansion

Out	Byte	Description
	0	LSB Offset into SCAM data
	1	MSB Offset into SCAM data
	2	LSB of Number of data bytes to return
	3	MSB of Number of data bytes to return
In	Byte	Description
	0	Data byte 0
	1	Data byte 1
	:	
	:	
	N	Data byte N (where N = Number of data bytes - 1)

Operation Code	Command	Parameter Byte Count	Direction
A9 (9x8 specific)	WRITE SCAM DATA	4 + Byte Count	Out

Description: This command stores data into the Host Adapter's SCAM information in NVRAM, FlashROM or E2PROM. The SCAM data format follows

00h-1Fh	32 bytes SCAM Initiator ID w/ Manufacturing S/N number
20h-FFh	Reserved for future SCAM Master
100h-2FFh	512 byte Target SCAM device ID string—32 bytes for each ID
300h-FFFFh	Reserved for future expansion

Byte	Description
0	LSB Offset into SCAM data
1	MSB Offset into SCAM data
2	LSB of Number of data bytes to return
3	MSB of Number of data bytes to return
4	Data byte 0
5	Data byte 1
:	
:	
N+4	Data byte N - 1 (where N=Number of data bytes)

Due to the block nature of the FlashPROM, E2PROM, the controller may need to retrieve data from the PROM, modified the bytes affected and write back to the PROM. If the offset and byte count fit in to the PROM block size, then one single write will do it. It is advised to do block write. For 9x8 products, a block is 128 bytes.

Addressing Mode

BusLogic adapters support both 24-bit and 32-bit addressing modes. 24-bit addressing support offers backward compatibility to early versions of BusLogic host adapter products as well as compatibility with products currently on the market.

However, 24-bit addressing offers limited memory access, allowing only up to 16 MBytes of memory. Current BusLogic adapters support 32-bit addressing, allowing the host adapter unrestricted access up to 4 Gigabytes of memory.

Under 24-bit mode addressing section below, you'll find a complete description of how 24-bit addressing is implemented by BusLogic host adapters. The description of 32-bit addressing that follows covers the differences between 24-bit and 32-bit addressing operation.

Mailbox Commands

With today's application requirements, sophisticated operating systems, and performance capabilities of the latest systems using faster CPUs and higher bus transfer rates, it is desirable to have several different tasks running simultaneously in support of many different users. These tasks require a wide variety of I/O peripheral devices such as hard disks, tape backup units and optical drives.

One advantage offered by the SCSI bus is that up to fifteen I/O devices may be connected to one host adapter. An effective method is needed to manage the processing of each separate task in a system where individual users make use of many different SCSI I/O devices. A method that takes advantage of the local microprocessor, bus master ASIC, and other intelligence features of the host adapter is needed. Otherwise, the main system CPU would be loaded down. One such method is the mailbox structure of communication between the host system and the host adapter.

Mailboxes are reserved storage areas which reside at a fixed contiguous memory location in the host system. The mailboxes coordinate communications between the host system and the host adapter. Outgoing mailboxes are used for sending command information to the host adapter and incoming mailboxes are used by the host adapter to return status information about completed commands to the host.

This interface architecture provides a means of passing SCSI device commands from a task, by means of a software driver, to the host adapter in a multi-tasking, multi-user environment with minimal host intervention. In this mode the host adapter can concurrently execute multiple commands for multiple targets. The host adapter's on-board intelligence allows it to complete bus master data transfers, to manage SCSI disconnects and reconnects and to perform other activities which reduce host intervention; thereby, increasing overall system I/O throughput. The following few pages describe the organization and operation of this approach.

When multiple mailboxes are established by the host driver, it is recommended that the outgoing mailbox be used in "round robin" fashion.

Mailbox Initialization

With most procedures in a computer system, some means of initialization must be performed to establish starting reference conditions. After power is applied to a system, many system initialization functions are carried out before any application programs are activated.

Similarly, before any mailbox commands can be supplied to the host adapter, another specific initialization process must be conducted.

First, the host system allocates storage space at a fixed contiguous location somewhere in the main system memory where the communication mailboxes will be placed. The host creates the required number of 4-bytes (for 24-bit mode) or 8 bytes (for 32-bit mode) outgoing mailboxes, followed immediately in memory by *an equal number* of incoming mailboxes. The host then sends an **Initialize Mailbox** command to the host adapter. This command tells the host adapter how many mailboxes will be used and the base address of the first outgoing mailbox in the main system memory as described in the heading "Host Adapter Commands" earlier in this section. There should typically be at least one set of Out/In mailboxes for each active and independent task. Figure 1-9 illustrates an array of four outgoing and four incoming mailboxes.

Before describing the use of outgoing and incoming mailboxes, their structure and contents will be defined.

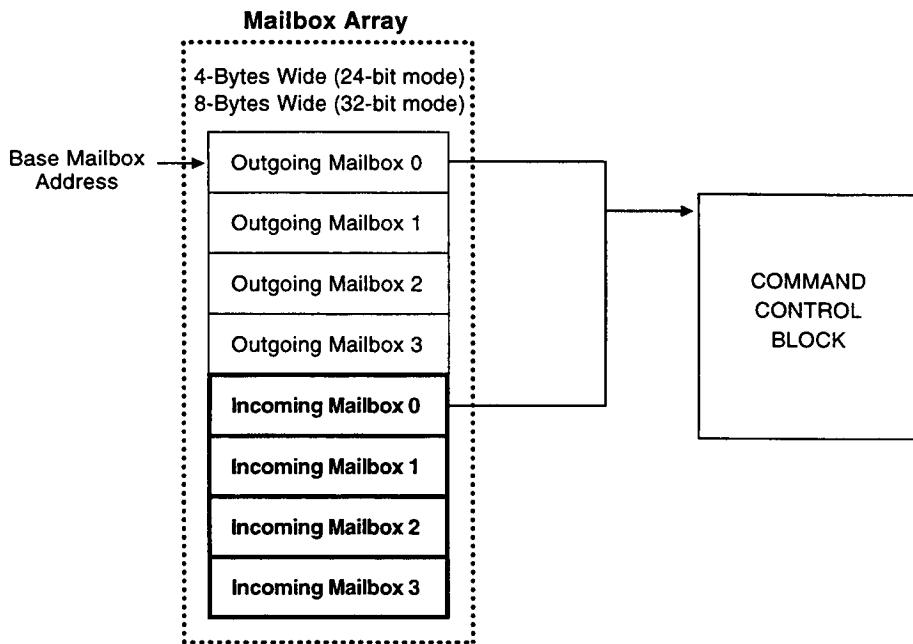


Figure 1-9. Mailbox Array

24-Bit Mode Outgoing Mailbox Structure

The following are the possible contents of the four bytes of each outgoing mailbox.

Byte	Function	
0	Action Code	
	Hex Value	Definition
	00	Outgoing Mailbox is not in use
	01	Start a Mailbox command
	02	Abort a Mailbox command
1-3	CCB Address (Byte 1 is MSB)	

The first byte of the outgoing mailbox is the “action” code. If the byte is zero in any particular outgoing mailbox, the host can place a CCB address in the last three bytes of that mailbox and set the first byte in the same mailbox to start or to abort the command contained in the designated CCB. After the host adapter has copied the information in an outgoing mailbox in the course of executing commands, it releases that mailbox by clearing its first byte so the host can use it again.

24-Bit Mode Incoming Mailbox Structure

When a CCB has been provided to the host adapter, the host adapter uses incoming mailboxes to provide information regarding the completion of the CCB to the host. The possible contents of the four bytes of each incoming mailbox of this type are as follows:

Byte	Function	
0	Completion Code	
	Hex Value	Definition
	00	Incoming Mailbox is not in use
	01	CCB completed without error
	02	CCB aborted at request of host
	03	Aborted CCB not found
	04	CCB completed with error
1-3	CCB Address (Byte 1 is MSB)	

If the first byte in an incoming mailbox is zero in any particular incoming mailbox, the host adapter can place the address of the completed CCB in the last three bytes of that mailbox and can set the first byte in the same mailbox to indicate the manner in which the command was completed.

Host Adapter as Initiator on the SCSI Bus

To establish communication between the host adapter and an attached SCSI device to execute some command, either the host adapter or the SCSI device can initiate the SCSI command. The other party in the communication is the target. The default case is for the host adapter to be the initiator.

Assuming that a task is running and that communication with a SCSI device is required the host system performs the following preparation to process the I/O request:

- Allocates an area in the main system memory for data storage or retrieval
- Creates a CCB which identifies the SCSI I/O device, provides an address which points to the data area in the main memory and specifies other detailed information about the SCSI command
- Places an address pointer to the CCB and an “action” code in an outgoing mailbox
- Sends a Start Mailbox command to the host adapter.

When the host adapter has received the Start Mailbox command, it performs the following activities:

- Begins scanning the outgoing mailboxes to find entries with action codes using a round-robin scheme
- Copies outgoing mailbox information into its local RAM and then releases the outgoing mailbox

- Copies the CCB pointed to by the outgoing mailbox into its local RAM
- Executes the SCSI command specified in the CCB as soon as the SCSI bus is not busy.

The action taken by the host adapter to release an outgoing mailbox once its information has been copied to local RAM depends on the host adapter command **Enable OMCR Interrupt**. If this command has been issued to the host adapter to enable the Outgoing Mailbox interrupt (OMBR), the host adapter will do one of the following:

- If no interrupt bits are set in the Interrupt Register, the host adapter will set the Outgoing Mailbox Ready (OMBR) and the Interrupt Valid (INTV) bits in the Interrupt Register, and then will assert the Interrupt Request signal on the bus.
- If the Outgoing Mailbox Ready bit (OMBR) is already set to indicate that a previous outgoing mailbox was released and the interrupt was not yet cleared by the host then no additional notification to the host is required.
- If interrupts other than Outgoing Mailbox Ready interrupt (OMBR) are pending, the host adapter will wait for all of them to be cleared before setting the Outgoing Mailbox Ready bit (OMBR).

After processing an outgoing mailbox, the host adapter will scan for another active entry beginning with the outgoing mailbox following the one just completed. The host can ensure that the host adapter will always find the next command with minimum overhead by placing commands in the outgoing mailboxes in consecutive, round-robin order. The host adapter will look for additional outgoing mailbox entries until it finds an empty outgoing mailbox, at which time it will stop scanning. It will start scanning again when the host issues a Start Mailbox command to indicate that another entry has been made. Active entries are transferred into local RAM and placed in a command queue. The local RAM has enough space to store up to 32 CCBs at any one time.

The commands are taken from the queue in a first-in first-out basis to be executed as soon as the SCSI bus is not busy. Commands will not necessarily be completed in the same order because the execution time of each command may be different.

If a Busy condition from the target device temporarily prevents the execution of a command, it is returned to the end of the queue and will be retried when queued up again. This process will continue until the Busy condition is resolved and the command can be completed.

When an outgoing mailbox is found to contain an abort code, the associated CCB pointer is used by the host adapter to locate the mailbox command to be aborted. The designated CCB may be active or queued. If the CCB can be found the command is terminated as soon as possible. The host adapter then makes an incoming mailbox entry to indicate that the command was terminated.

If the CCB can not be found, the command may have already been completed in a normal manner or may have been previously aborted. This situation will also be reported to the host in an incoming mailbox entry.

At the completion of each mailbox command, the target device can report that the completion was "GOOD" or that it has additional status which must be checked. In the latter case, the host adapter may automatically issue a Request Sense command to get the additional status data from the target device. This sense data is stored in a designated area at the end of the CCB in host memory.

At the completion of a mailbox command, the host adapter writes status information into the BTSTAT and SDSTAT fields in the CCB in the main system memory. The host adapter then writes into an incoming mailbox a completion status byte and a pointer to the completed CCB.

After placing an entry into an incoming mailbox, the host adapter will take one of the following actions:

- If no interrupt bits are set in the Interrupt Register, the host adapter will set the Incoming Mailbox Loaded (IMBL) and the Interrupt Valid (INTV) bits in the Interrupt Register and then will assert the Interrupt Request signal on the bus.
- If the Incoming Mailbox Loaded bit (IMBL) is already set to indicate that a previous incoming mailbox was loaded and the interrupt has not yet been cleared by the host then no additional notification to the host is required.
- If interrupts other than Incoming Mailbox Loaded interrupt (IMBL) are pending, the host adapter will wait for all of them to be cleared before setting the Incoming Mailbox Loaded bit (IMBL).

Whenever the host sees that the Incoming Mailbox Loaded bit (IMBL) is set, it begins to scan the incoming mailboxes for active entries. The host will read each active incoming mailbox to obtain status information and pointers to the completed CCBs and then will release the incoming mailboxes for future use. When all active incoming mailboxes have been processed, the host then clears the Incoming Mailbox Loaded bit (IMBL) and the Interrupt Invalid bit (INTV) in the host adapter's Interrupt Register.

The host adapter places **no** restrictions on the data segment address boundaries and lengths that are allowed. For maximum performance, however, it is recommended that all starting addresses (mailboxes, CCBs and data pointers) be on 32-bit (double-word) boundaries and all transfer byte counts be a multiple of four.

24-Bit Mode CCB Structure

A CCB contains detailed information about a SCSI command. The basic structure is presented in the following table. Detailed descriptions of each byte or field in the CCB follow this table.

Table 1-3. 24-Bit Mode CCB Structure

Byte	Description
0	CCB Operation Code
1	SCSI ID and Direction Control
2	Length of SCSI Command Descriptor Block
3	Request Sense Allocation Length
4	MSB
5	Data Length
6	LSB
7	MSB
8	Data Pointer
9	LSB
10–13	Reserved

Table 1-3. 24-Bit Mode CCB Structure (Continued)

Byte	Description
14	Host adapter Status (BTSTAT)
15	SCSI Device Status (SDSTAT)
16	Reserved and set to zero
17	Reserved and set to zero
18-n	SCSI Command Descriptor Block
n-m	Reserved For Request Sense Information Bytes (Length of reserved space is specified in Byte 3)

Table 1-4. Command Control Block Field Definitions

Byte	Field	Description
0	CCB Operation Code (Hex)	
	00	Initiator CCB. The host adapter acts as the initiator to issue the SCSI command specified in the target SCSI device. The Data Length field is the transfer count in bytes. The Data Pointer field is the transfer address.
	02	Initiator CCB with scatter-gather. The host adapter acts as the initiator to issue a command to the specified target device with scatter-gather data transfers. The data Length field is the byte count of the data segment list. The Data Pointer field is the pointer to the data segment list.
	03	Initiator CCB with residual data length returned. The host adapter acts as the initiator to issue a SCSI command to the specified target device with data transfer length checked. The Data Length field is the transfer count in bytes. The Data Pointer field is the transfer address.
	04	Initiator CCB with scatter-gather and residual data length returned. The host adapter acts as the initiator to issue a SCSI command to the specified target device with scatter-gather data transfers and transfer length check. The Data Length field is the byte count of the Data Segment list.
	81	SCSI bus reset. A BUS DEVICE RESET message is sent by the host adapter to the specified target. This forces the host adapter to abort all outstanding tasks against the selected target and to ignore all remaining CCB bytes.
1	Data Control	Identifies the address of the devices involved in the command and provides information about the expected direction of data flow.
	Bits 7-6-5	Specifies the target SCSI ID.
	Bits 4-3	Set to determine the direction of the data transfer as follows: Initiator CCB Bit Bit
	4 3	Host Adapter Action
	0 0	Direction of data transfer determined by the SCSI command being executed.

Table 1-4. Command Control Block Field Definitions (Continued)

Byte	Field	Description
	0 1	Data transferred from SCSI device to host adapter. Data transfer will be a Data In phase. Data length will be checked.
	1 0	Data transferred from host adapter to SCSI device. Data transfer will be a Data Out phase. Data length will be checked.
	1 1	No data transfer.
Bits 2-0		Target LUN. If the target accepts an IDENTIFY message out, these bits will be provided in the LUN field of the message byte. The LUN field in the SCSI CDB is expected to be zero. If the target does not accept an IDENTIFY message out, the LUN field in the SCSI CDB must contain the correct LUN address. All SCSI-II devices or devices supporting Common Command Set (CCS) accept the IDENTIFY message out. Any device not meeting these requirements should be examined individually to determine whether the LUN address should be placed in Byte 1 of the CCB or in the SCSI CDB.
2	Length of SCSI Command Descriptor Block	Specifies the number of bytes in the SCSI CDB beginning at Byte 18 of the CCB.
3	Request Sense Allocation Length	Indicates the number of bytes in the CCB following the CDB reserved for information that may be obtained by allocation length as its byte count in the CDB for the Request Sense command it issues in response to a Check Condition status received from a target SCSI device at the completion of a command. Sense information is placed in the specified request sense allocation area with a length not exceeding the request sense allocation length. This byte also provides a software method for disabling the Automatic Sense function to override the switch settings described in the adapter user's guide. The following values are defined for this byte:
Hex Value	Meaning	
00	Allocate 14 bytes for request sense data	
01	Disable automatic request sense	
02-07	Reserved	
08-FF	Valid allocation lengths for SCSI sense data	

Table 1-4. Command Control Block Field Definitions (Continued)

Byte	Field	Description
4–6	Data Length	<p>Specifies either the data transfer count or the Data Segment list length in bytes. Upon completion of a mailbox command, this field will report the residual count if specified by the CCB Opcode.,</p> <p>Note: for optimal performance, use residual count only when necessary.</p> <p>CCB Opcode 0: Specifies the data transfer count. It is not updated after a command is completed.</p> <p>CCD Opcode 2: Specifies the Data Segment List length. It is not updated after the command is completed.</p> <p>CCB Opcode 3: Specifies the data Segment list length. It contains the residual count after the command is completed. The residual count is the specified transfer count less the actual data transferred.</p> <p>CCB Opcode 4: Specifies the data Segment list length. It contains the residual count after the command is completed. The residual count is the accumulated transfer count of each data segment less the actual data transferred.</p> <p>CCB Opcode 81: This field is not used.</p>
7–9	Data Pointer	Specify the real address of the first byte of the data area to be used during the data phase of a SCSI command. If a scatter-gather operation is specified by the CCB, the Data Pointer field contains the pointer to the first byte in the Data Segment List.
10–13	Reserved	Not used
14	Btstat Hex Value	Host adapter status reported to the host.
	00	CCB completed normally with no errors.
	11	SCSI Selection time out. Initiator selection or target reselection did not complete within the set SCSI selection time-out period.
	12	Data over run/under run. The target attempted to transfer more or less data than was allocated by the Data Length field or the sum of the Scatter-Gather Data Length fields.
	13	Unexpected bus free.
	14	An invalid bus phase or sequence was requested by the target. The host adapter generated a SCSI Reset state, notifying the host with a SCSI Reset State interrupt (RSTS).
	15	Invalid action code in Byte 0 of the outgoing mailbox.
	16	Invalid operation code in Byte 0 of the CCB.
	17	Linked CCB does not have the same LUN as the first CCB.
	1A	Invalid parameter in CCB or segment list.
	1B	Auto request sense failed.
	1C	SCSI II Tagged Queueing message was rejected by the target.
	1D	Unsupported message received by the host adapter.
	20	The host adapter hardware failed.
	21	The target did not respond to SCSI ATN and the host adapter issued a SCSI RST to clear up the failure.
	22	The host adapter asserted a SCSI RST.

Table 1-4. Command Control Block Field Definitions (Continued)

Byte	Field	Description								
23		Other SCSI devices asserted a SCSI RST.								
24		The target device reconnected improperly (without tag). An abort message was issued.								
25		The host adapter issued BUS DEVICE RESET.								
26		Abort Queue generated.								
27		Host adapter software error.								
30		Host adapter hardware time-out error. Recommended recovery is to issue a hard reset to the host adapter								
34		SCSI parity error detected.								
15	SDSTAT	SCSI Device Status. If the host adapter is the initiator, the target will send a status byte to the host adapter at the termination of each SCSI command. The host adapter places that status code in this byte of the CCB to report it to the host. If a Busy status is returned in the SCSI command, the command is executed a second time. The host adapter requeues the command and automatically restarts it until the command completes with a status other than Busy. Status codes reported to the initiator by the target and reported to the host in this byte may have the following values:								
		<table> <thead> <tr> <th>Hex Value</th> <th>Status Meaning</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Good</td> </tr> <tr> <td>02</td> <td>Check Condition. See CCB Byte 3 discussion of Request Sense in response to Check Condition.</td> </tr> <tr> <td>08</td> <td>See SCSI specification.</td> </tr> </tbody> </table>	Hex Value	Status Meaning	00	Good	02	Check Condition. See CCB Byte 3 discussion of Request Sense in response to Check Condition.	08	See SCSI specification.
Hex Value	Status Meaning									
00	Good									
02	Check Condition. See CCB Byte 3 discussion of Request Sense in response to Check Condition.									
08	See SCSI specification.									
16–17	Reserved	Must be set to zero.								
18–n	SCSI Command Descriptor Block	Contains the SCSI CDB Its length is defined in CCB Byte 2. For initiator CCB's, the CDB provided by the host is transmitted to the target.								
n–m	Sense Data	If the host adapter detects a Check Condition status once an operation is completed on the SCSI bus, the host adapter automatically executes a Request Sense command with the number of bytes specified by the Request Sense Allocation Length in CCB Byte 3. The bytes returned, up to the maximum indicated by the Request Sense Allocation Length, are placed in this area.								

32-Bit Mode Mailbox Structure

Communication between the host and the host adapter is coordinated by the use of outgoing and incoming mailboxes. These mailboxes contain control and status information, and address pointers to CCBs that contain the details of each SCSI command to be processed. The mailbox structures have been changed to the following format:

OUTGOING MAILBOXES

Byte 0	Byte 1	Byte 2	Byte 3
LSB	32-Bit CCB	Pointer	MSB
Byte 4	Byte 5	Byte 6	Byte 7
Reserved	Reserved	Reserved	Action Code

Valid Action Codes are as follows:

Hex Value	Definition
00	Outgoing mailbox is not in use
01	Start a mailbox command
02	Abort a mailbox command.

INCOMING MAILBOXES

Byte 0	Byte 1	Byte 2	Byte 3
LSB	32-Bit CCB	Pointer	MSB
Byte 4	Byte 5	Byte 6	Byte 7
BTSTAT	SDSTAT	Reserved	Completion Code

Valid Completion Codes are as follows:

Hex Value	Definition
00	Incoming mailbox is not in use
01	CCB completed without error
02	CCB aborted at request of host
03	Aborted CCB not found
04	CCB completed with error.

32-Bit Mode CCB Structure

Byte	Description
0	Operation Code
1	Data Direction Control
2	Length of CDB
3	Length of Sense Area
4	LSB
5	Data
6	Length
7	MSB
8	LSB
9	Data
10	Pointer
11	MSB
12	Reserved
13	Reserved
14	BTSTAT
15	SDSTAT
16	Target ID
17	LUN & Tag
18-29	Command Descriptor Block (12 Bytes)

Byte	Description
30	Reserved
31–35	Reserved
36	LSB
37	Sense
38	Pointer
39	MSB

All reserved bytes and bits should always be set to zero.

32-Bit Mode CCB Description

Many fields of the 32-bit mode CCB are identical to the 24-bit CCB. Its data address fields expand to four-byte fields to contain full 32-bit address pointers. The byte order is reversed, with the LSB coming first rather than the MSB. To enhance symmetry, the Data Length field expands to four bytes as well.

Target ID and LUN numbers are given their own bytes rather than having to share a byte with specification of data direction and length checking in Byte 1 of the CCB.

A Sense Pointer is included. This offers the option of allocating a storage area anywhere in the main memory for the information returned in response to a Request Sense command. One option is to have the Sense Pointer point to the bytes immediately following itself at the end of the CCB. Refer to the following table for a description of 32-bit mode-specific CCB field definitions.

Table 1-5. 32-Bit Mode CCB Field Definitions

Byte	Field	Description
0	CCB Operation Code (Hex)	
	00	Initiator CCB. The host adapter acts as the initiator to issue the SCSI command specified in the target SCSI device. The Data Length field is the transfer count in bytes. The Data Pointer field is the transfer address.
	02	Initiator CCB with scatter-gather. The host adapter acts as the initiator to issue a command to the specified target device with scatter-gather data transfers. The data Length field is the byte count of the data segment list. The Data Pointer field is the pointer to the data segment list.
	03	Initiator CCB with residual data length returned. The host adapter acts as the initiator to issue a SCSI command to the specified target device with data transfer length checked. The Data Length field is the transfer count in bytes. The Data Pointer field is the transfer address.
	04	Initiator CCB with scatter-gather and residual data length returned. The host adapter acts as the initiator to issue a SCSI command to the specified target device with scatter-gather data transfers and transfer length check. The Data Length field is the byte count of the Data Segment list.
	81	SCSI bus reset. A BUS DEVICE RESET message is sent by the host adapter to the specified target. This forces the host adapter to abort all outstanding tasks against the selected target and to ignore all remaining CCB bytes.

Table 1-5. 32-Bit Mode CCB Field Definitions (Continued)

Byte	Field	Description										
1	Data Control	Identifies the address of the devices involved in the command and provides information about the expected direction of data flow.										
	Bits 7–5	Not used.										
	Bits 4–3	Set to determine the direction of the data transfer as follows:										
		Initiator CCB										
		Bit Bit										
		4 3 Host Adapter Action										
		0 0 Direction of data transfer determined by the SCSI command being executed.										
		0 1 Data transferred from SCSI device to host adapter. Data transfer will be a Data In phase. Data length will be checked.										
		1 0 Data transferred from host adapter to SCSI device. Data transfer will be a Data Out phase. Data length will be checked.										
		1 1 No data transfer.										
	Bits 2–0	Not used; reset to zero										
2	Length of SCSI Command Descriptor Block	Specifies the number of bytes in the SCSI CDB beginning at Byte 18 of the CCB.										
3	Request Sense Allocation Length	Indicates the number of bytes in the CCB following the CDB reserved for information that may be obtained by allocation length as its byte count in the CDB for the Request Sense command it issues in response to a Check Condition status received from a target SCSI device at the completion of a command. Sense information is placed in the specified request sense allocation area with a length not exceeding the request sense allocation length. This byte also provides a software method for disabling the Automatic Sense function to override the switch settings described in the adapter user's guide. The following values are defined for this byte:										
		<table><thead><tr><th>Hex Value</th><th>Meaning</th></tr></thead><tbody><tr><td>00</td><td>Allocate 14 bytes for request sense data</td></tr><tr><td>01</td><td>Disable automatic request sense</td></tr><tr><td>02–07</td><td>Reserved</td></tr><tr><td>08–FF</td><td>Valid allocation lengths for SCSI sense data</td></tr></tbody></table>	Hex Value	Meaning	00	Allocate 14 bytes for request sense data	01	Disable automatic request sense	02–07	Reserved	08–FF	Valid allocation lengths for SCSI sense data
Hex Value	Meaning											
00	Allocate 14 bytes for request sense data											
01	Disable automatic request sense											
02–07	Reserved											
08–FF	Valid allocation lengths for SCSI sense data											

Table 1-5. 32-Bit Mode CCB Field Definitions (Continued)

Byte	Field	Description
4–7	Data Length	<p>Specifies either the data transfer count or the Data Segment list length in bytes. Upon completion of a mailbox command, this field will report the residual count if specified by the CCB Opcode. Note: for optimal performance, use residual count only when necessary.</p> <p>CCB Opcode 0: Specifies the data transfer count. It is not updated after a command is completed.</p> <p>CCB Opcode 2: Specifies the Data Segment List length. It is not updated after the command is completed.</p> <p>CCB Opcode 3: Specifies the data Segment list length. It contains the residual count after the command is completed. The residual count is the specified transfer count less the actual data transferred.</p> <p>CCB Opcode 4: Specifies the data Segment list length. It contains the residual count after the command is completed. The residual count is the accumulated transfer count of each data segment less the actual data transferred.</p> <p>CCB Opcode 81: This field is not used.</p>
8–11	Data Pointer	Specify the physical address of the first byte of the data area to be used during the data phase of a SCSI command. If a scatter-gather operation is specified by the CCB, the Data Pointer field contains the pointer to the first byte in the Data Segment List.
12	Reserved	Not used; reset to zero
13	Reserved	Not used; reset to zero
14	Btstat Hex Value	Host adapter status reported to the host.
00		CCB completed normally with no errors.
11		SCSI Selection time out. Initiator selection or target reselection did not complete within the set SCSI selection time-out period.
12		Data over run/under run. The target attempted to transfer more or less data than was allocated by the Data Length field or the sum of the Scatter-Gather Data Length fields.
13		Unexpected bus free.
14		An invalid bus phase or sequence was requested by the target. The host adapter generated a SCSI Reset state, notifying the host with a SCSI Reset State interrupt (RSTS).
15		Invalid action code in Byte 0 of the outgoing mailbox.
16		Invalid operation code in Byte 0 of the CCB.
17		Linked CCB does not have the same LUN as the first CCB.
1A		Invalid parameter in CCB or segment list.
1B		Auto request sense failed.
1C		SCSI II Tagged Queueing message was rejected by the target.
1D		Unsupported message received by the host adapter.
20		The host adapter hardware failed.

Table 1-5. 32-Bit Mode CCB Field Definitions (Continued)

Byte	Field	Description															
21		The target did not respond to SCSI ATN and the host adapter issued a SCSI RST to clear up the failure.															
22		The host adapter asserted a SCSI RST.															
23		Other SCSI devices asserted a SCSI RST.															
24		The target device reconnected improperly (without tag). An abort message was issued.															
25		The host adapter issued BUS DEVICE RESET.															
26		Abort Queue generated.															
27		Host adapter software error.															
30		Host adapter hardware time-out error. Recommended recovery is to issue a hard reset to the host adapter															
34		SCSI parity error detected.															
15	SDSTAT	<p>SCSI Device Status. If the host adapter is the initiator, the target will send a status byte to the host adapter at the termination of each SCSI command. The host adapter places that status code in this byte of the CCB to report it to the host. If a Busy status is returned in the SCSI command, the command is executed a second time. The host adapter requeues the command and automatically restarts it until the command completes with a status other than Busy.</p> <p>Status codes reported to the initiator by the target and reported to the host in this byte may have the following values:</p> <table> <thead> <tr> <th>Hex Value</th> <th>Status Meaning</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Good</td> </tr> <tr> <td>02</td> <td>Check Condition. See CCB Byte 3 discussion of Request Sense in response to Check Condition.</td> </tr> <tr> <td>08</td> <td>Busy.</td> </tr> </tbody> </table>	Hex Value	Status Meaning	00	Good	02	Check Condition. See CCB Byte 3 discussion of Request Sense in response to Check Condition.	08	Busy.							
Hex Value	Status Meaning																
00	Good																
02	Check Condition. See CCB Byte 3 discussion of Request Sense in response to Check Condition.																
08	Busy.																
16		Specifies the target SCSI ID.															
17	Logical Unit Number (LUN) and Tag	<p>Bits 2–0</p> <p>Specifies the Logical Unit Number (LUN).</p> <p>Bits 4–3</p> <p>Reserved.</p> <p>Bit 5</p> <p>Tag enable. When this bit is set, the host adapter will support the tag queueing feature according to the SCSI-2 specifications. When this bit is reset, the host adapter will not support this feature.</p> <p>Bits 6,7</p> <p>Specifies the tag type. These two bits have no meaning if bit 5 (the Tag Enable bit) is not set. When bit 5 is set, bits 6 and 7 have the following meaning:</p> <table> <thead> <tr> <th>Bit 7</th> <th>Bit 6</th> <th>Message to be sent to the target after IDENTIFY</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Simple Queue Tag (20H) + Unique Tag ID</td> </tr> <tr> <td>0</td> <td>1</td> <td>Head of Queue Tag (21H) + Unique Tag ID</td> </tr> <tr> <td>1</td> <td>0</td> <td>Ordered Queue Tag (22H) + Unique Tag ID</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved (Do not use this value.)</td> </tr> </tbody> </table>	Bit 7	Bit 6	Message to be sent to the target after IDENTIFY	0	0	Simple Queue Tag (20H) + Unique Tag ID	0	1	Head of Queue Tag (21H) + Unique Tag ID	1	0	Ordered Queue Tag (22H) + Unique Tag ID	1	1	Reserved (Do not use this value.)
Bit 7	Bit 6	Message to be sent to the target after IDENTIFY															
0	0	Simple Queue Tag (20H) + Unique Tag ID															
0	1	Head of Queue Tag (21H) + Unique Tag ID															
1	0	Ordered Queue Tag (22H) + Unique Tag ID															
1	1	Reserved (Do not use this value.)															

Table 1-5. 32-Bit Mode CCB Field Definitions (Continued)

Byte	Field	Description
18– 29	SCSI Command Descriptor Block	Contains the SCSI CDB. Its length is defined in CCB Byte 2. For initiator CCB's, the CDB provided by the host is transmitted to the target.
30	Reserved	
31– 35	Reserved	Not used
36– 39	Sense Pointer	If the host adapter detects a Check Condition status once an operation is completed on the SCSI bus, the host adapter automatically executes a Request Sense command with the number of bytes specified by the Request Sense allocation length in CCB Byte 3. The bytes returned, up to the maximum indicated by the Request Sense allocation Length, are placed in this area.

64 LUN CCB Format

The SCSI product can support up to 64 (6 bit) LUNs. Its CCB structure is the same as the 32-bit mode structure, except that the 32-bit CCB's LUN and Tag field (Byte 17, described in the preceding table) can not address the expended 6-bit LUN field. the 64 LUN CCB has an expanded LUN ID field to support it. The default definition of the CCB is the "regular" 32-bit CCB. Enable 64 LUN CCB Format by calling host adapter command (96h) with the command parameter = 1; Set the CCB back to the normal 32-bit Mode CCB with command parameter = 0. (See page 1-37).

The 64 LUN CCB Format accommodates the 6-bit LUN by redefining two fields of the 32-bit CCB as follows:

Table 1-6. 64 LUN CCB Format Field Definitions

Byte	Field	Description
1	Data Direction and Tag	
Bits 6,7		Specifies the tag type. Thee two bits have no meaning if bit 5 (The Tag Enable bit) is not set. When bit 5 is set, bits 6 and 7 have the following meaning: Bit 7 Bit 6 Message to be sent to the target after IDENTIFY 0 0 Simple Queue Tag (20H) + Unique Tag ID 0 1 Head of Queue Tag (21H) + Unique Tag ID 1 0 Ordered Queue Tag (22H) + Unique Tag ID 1 1 Reserved (Do not use this value.)
Bit 5		Tab enable. when this bit is set, the host adapter will support the tag queueing feature according to the SCSI-2 specifications. when this bit is reset, the host adapter will not support this feature.

Table 1-6. 64 LUN CCB Format Field Definitions

Byte	Field	Description
	Bit 4–3	Set to determine the direction of the data transfer as follows:
Initiator CCB		
	Bit 4 Bit 3	
	4 3	Host Adapter Action
	0 0	Direction of data transfer determined by the SCSI command being executed.
	0 1	Data transferred from SCSI device to host adapter. Data transfer will be a Data In phase. Data length will be checked.
	1 0	Data transferred from host adapter to SCSI device. Data transfer will be a Data Out phase. Data length will be checked.
	1 1	No data transfer.
	Bits 2–0	Not used; reset to zero
17	Logical Unit Number (LUN) and Tag	
	Bits 7–6	Not used; reset to zero
	Bits 5–0	Specifies the LUN

Scatter-Gather Operations

Scatter-Gather Operation for 24-Bit Mode

In normal CCB operations using SCSI Initiator (00H) and SCSI Target (01H) codes, the CCB contains the pointer (CCB, Bytes 7–9) to the first byte of a contiguous area of data of a specified length (CCB, Bytes 4–6).

Unlike the preceding operation codes, the SCSI initiator with Scatter-Gather code (02H) uses CCB Bytes 7–9 as a pointer to a list of data segments to be transferred. Bytes 4–6 in the CCB specify the length of the Data Segment List. Each entry in the list contains a three-byte field specifying the length of a data segment and a second three-byte field containing a 24-bit address which points to the corresponding data segment in host memory. The Data Segment List is arranged in the order in which data is to be “gathered” or “scattered.” The first entry in the list, pointed to by the Data Segment List Pointer in CCB Bytes 7–9, will be used first. A Data Segment List can identify up to 8,192 separate segments of memory. An invalid Data Segment List error will be posted in the Btstat field (1AH) if a list contains zero or more than 8,192 segments.

The structure of the Data Segment List is as follows:

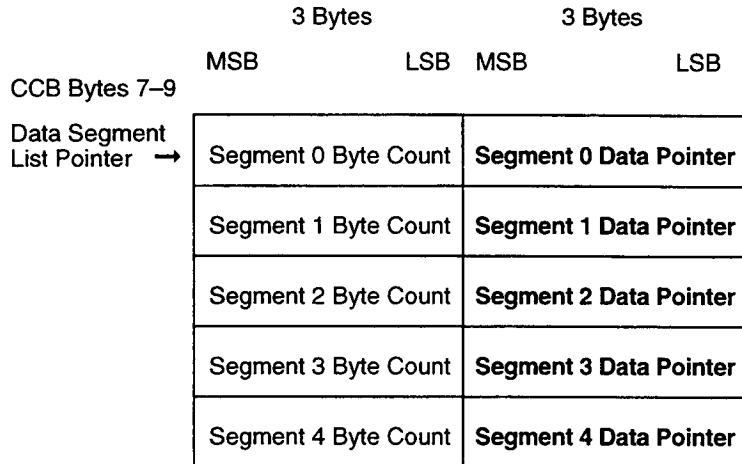


Figure 1-10. Scatter-Gather Data Segment List—CCB Bytes 7–9

The host adapter places **no** restrictions on the data segment address boundaries and lengths that are allowed.

Note: To enhance performance, it is recommended that all starting addresses (mailboxes, CCBs and data pointers) be on 32-bit (double-word) boundaries and that all transfer byte counts be a multiple of four. If an error occurs during execution of a Scatter-Gather command, the entire command must be retried. It is not possible to determine which segment produced the error.

Scatter-Gather Operation for 32-Bit Mode

Within 24-bit mode design when a scatter-gather data transfer is performed, the CCB points to a list of the separate data segments involved in the transfer. This list contains a three-byte field specifying the length of each individual data segment and a second three-byte field containing a 24-bit address that points to the corresponding data segment.

With 32-bit addressing, the scatter-gather list must be expanded to pairs of four-byte fields for each data segment in place of the present pairs of three-byte fields. These 32-bit addresses provide unrestricted access to any area of the 4 Gigabyte memory space.

The structure of the 32-bit data segment list is as follows:

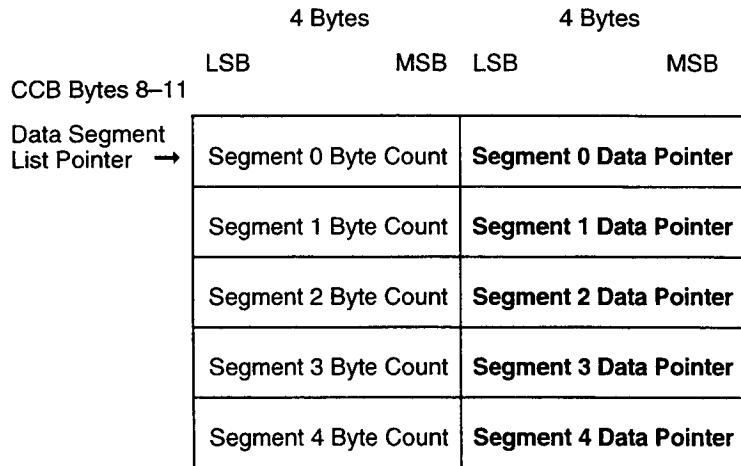


Figure 1-11. Scatter-Gather Data Segment List—CCB Bytes 8-11

In the BusLogic implementation of the host adapter, such a data segment list can have from 1 to 8192 segments.

32-Bit Mode Command Queueing

The host adapter supports command queuing in the 32-bit mode. The following are some device driver notes related to command queuing.

1. Once a device queues up Tag Queue commands, the Initiator should not issue a Non-Tag Queue command (with the exception of Contingent Allegiance condition) until all queued commands have been processed. Therefore, avoid mixing Tag Queue commands with Non-Tag Queue commands.
2. If a CCB is aborted in a Tag queue environment, the host adapter can no longer issue an Abort message to the target. It will have to wait until the Target reestablishes the I_T_L_Q NEXUS. Consequently, it is recommended that a CCB not be aborted in a Tag Queue environment.
3. When a Bus Device Reset is issued, the Target will flush all queued I/O commands. Consequently, the host adapter must return SCSI Reset status for all the CCBs sent to the Target.
4. When a SCSI Bus Reset is issued, all Targets will flush all queued I/O commands. Note that the host adapter will flush all existing TCB in the Disconnect TCB Link List and the Abort TCB Link List. Consequently, the host adapter must return SCSI Reset status for all the CCBs sent out.
5. If there are any outstanding Tag Queue commands and a Target attempts to reconnect without a Tag message, the host adapter will generate an Abort message. The host adapter will flush all outstanding CCBs sent to that Target. All these CCBs will be returned to the host with Host Adapter Status 24H. Refer to the description of the BTSTAT field for new host adapter status.

6. Because a Tag message must be sent right after an ID message, synchronous transfer negotiation initiated by the Initiator takes precedence over a Tag Queue message. This is because most devices that support Tag Queuing may not be able to handle an ID message, followed by a Tag Message, followed by a Synchronous Transfer Negotiations message.

Consequently, it is recommended that the first couple of commands be sent in Non-tag Queue fashion. This will allow the host adapter and Target to establish Synchronous Transfer mode after each Reset condition.

7. The Auto Sense capability is a useful feature that can be enabled or disabled. If Auto Sense is enabled and a Contingent Allegiance condition occurs, the host adapter will issue a Request Sense command. When a Request Sense command is issued, the Contingent Allegiance condition will be cleared and the Target can continue processing the queued commands.

When Auto Sense is disabled, the host can deal with the Contingent Allegiance condition itself and decide which recovery procedure to use. However, this may reduce adapter performance. For better performance BusLogic recommends that AutoSense be enabled when using tag queueing.

Implementation Requirements

Existing drivers must be modified to issue the Initialize Extended Mailbox command and to set up the new mailbox and CCB structures. To support scatter-gather transfers an expanded scatter-gather list structure must be provided.

Host adapter firmware will recognize the Initialize Extended Mailbox command to find the designated section of memory where the CCBs will be located. It will then recognize the specified 32-bit data pointer in each CCB when performing Bus Master data transfers and the expanded scatter-gather list.

Project Relationship

BusLogic will be pleased to work closely with the software supplier or customer in planning and implementing this extended addressing concept that will enhance SCSI data storage capacities on systems.

BIOS Command Interface

Bus compatible systems provide for a Basic Input/Output System (BIOS) interface in ROM on the system motherboard or on I/O option boards. These BIOS ROMs contain programs which control communication between the Disk Operating System (DOS) and the corresponding I/O peripheral device. Access to each BIOS occurs through a software interrupt of the host CPU. In the case of a hard disk, the software interrupt is Interrupt 13H.

On a standard system, the motherboard BIOS includes support for up to eight device-level interfaced hard disks. The BIOS on the host adapter provides equivalent support for up to eight SCSI hard disks by intercepting the Interrupt 13H call and by responding to its SCSI device IDs. Control of any additional hard disk drives requires the use of a software driver using mailbox commands.

If eight standard hard disks are present in a system, the host adapter's BIOS cannot support additional SCSI drives without a software driver. If no standard hard disks are installed, the host adapter's BIOS can support up to eight SCSI hard disks. For example, Drive 0 (C:) is Device 0, LUN0. Drive 1 (D:) is SCSI Device 1, LUN0, etc. Booting can only be done from first SCSI Device.

If one standard hard disk is installed, it is accessed as Drive 0 (C:). The system may be booted only from this internal hard disk. One SCSI hard disk may be concurrently supported by the host adapter.

Parameters required to execute commands associated with the control of the hard disks are transferred to and from the BIOS program routines with the use of the host CPU's general registers and segment registers. This interface is capable only with single-threaded operation.

The host adapter's BIOS can accept functions from the DOS operating system that are required for normal operation, system booting, basic maintenance and verification functions.

The host adapter is notified by its on-board BIOS when Interrupt 13H operations are in process by the Start BIOS host adapter command (03H). The host adapter might not respond properly to the Start BIOS command if it is issued by any other source than the on-board BIOS.

BIOS Commands and Input Parameters

The BIOS command code is passed to the host adapter through the CPU's Register AH. The drive number is provided to the host adapter through the CPU's Register DL. The drive number for each command will be 80H to 87H. Refer to the following table for a summary of valid BIOS disk functions. Other input parameters required by the host adapter to execute some of these commands will be described following the table.

Table 1-7. Valid Host Adapter BIOS Disk Functions

Command Code in AH Register (Hex Value)	Command	Description
00	Reset Disk System	The BIOS issues a reset to the SCSI bus. It then sends this command on to the standard BIOS so it can reset other floppy or hard disks in the system.
01	Read Status of Last Operation	The host adapter reports the status of the last operation performed by the specified disk. No SCSI activity occurs and the disk status is reset to zero.
02	Read Desired Sectors Into Memory	The requested sectors, defined by the input parameters, are read from the disk to the system memory. This function maps to a SCSI Read command (SCSI Opcode 08).
03	Write Desired Sectors From Memory	The requested sectors, defined by the input parameters, are written from the system memory to the indicated disk. This function maps to a SCSI Write command (SCSI Opcode 0A).

Table 1-7. Valid Host Adapter BIOS Disk Functions (Continued)

Command Code in AH Register (Hex Value)	Command	Description
04	Verify Desired Sectors	The requested sectors, defined by the input parameters, are verified to be written correctly on the SCSI disk. This function maps to a SCSI Verify Command (SCSI Opcode 2F). In some special cases, for targets that do not support the 2F command, this function maps to a SCSI Read command (SCSI Opcode 08) and discards the received data.
06	Identify SCSI Devices	This command is used to determine the number of the first SCSI drive attached to the host adapter.
08	Read Drive Parameters	This function maps to a SCSI Read Capacity command (SCSI Opcode 25). The total logical capacity is then converted to pseudo-physical parameters.
09	Initialize Drive Pair Characteristics	Because SCSI CCS drives are self-configuring, this command performs no operation.
0C	Seek	This function performs a Seek command (SCSI Opcode 0B) to the logical block address as defined by the physical parameters. This command is not required for CCS commands nor for proper SCSI device operations. Because the Seek operation is performed automatically by the Read and Write operations, it is not necessary to generate a Seek command to access data.
0D	Alternate Disk Reset	The BIOS sends a SCSI bus reset to the target specified in the DL Register. A reset function request is also passed to the system's BIOS so that any internally installed hard or floppy disk(s) can be reset.
10	Test Drive Ready	This function maps to a SCSI Test Unit Ready command (SCSI Opcode 00). After executing a Reset function, the host adapter's BIOS issues this function internally until the Target is no longer busy and the Unit Attention condition is cleared.
11	Recalibrate	This function maps to a Re-zero Unit command (SCSI Opcode 01).
15	Read DASD Type	The BIOS of the host adapter checks the Peripheral Device Type Qualifier (returned by the SCSI Inquiry command) to verify that the device is a Direct Access Device. The BIOS then returns the logical capacity reported by the SCSI Read Capacity command in the CX and DX Registers.

Additional input parameters are required by the Read (02H), Write (03H) and Verify (04H) BIOS commands and are supplied in the following registers:

CPU Register	Input Parameter
AL	Number of Sectors
CH	Low-Order Byte of the Cylinder Number
CL	Cylinder and Sector Numbers Bits 7 and 6: High-Order Cylinder Bits Bits 5 to 0: Sector Number
DH	Head number
DL	Drive Number
ES:BX	Address of Data Buffer Area

The Seek BIOS command (0C) requires only the cylinder and head numbers from Registers CL, CH and DH. In this case, the sector number bits in Register CL are zero.

The physical starting disk address provided in the preceding registers is converted by the host adapter's BIOS into a logical block address before being sent to the designated SCSI device. The physical address consists of 10 bits to specify up to 1024 cylinders, 8 bits to specify up to 255 heads and 6 bits to specify up to 63 sectors. These bits are combined to form a logical block address for the SCSI drive as follows:

Physical Cylinder Number	Physical Head Number	Physical Sector Number—1
10 bits	8 bits	6 bits
Logical Block Address		

BIOS Command Completion Status

When the host adapter has completed the BIOS command, control is returned to the requesting program at the next instruction after the software Interrupt 13H.

The host adapter's BIOS places a completion code in the Carry Flag (CF). If CF is zero, the BIOS command was completed normally and there is no additional status to report. If CF is set to one, normal command completion did not occur and a non-zero status byte will be placed into the CPU's Register AH by the host adapter. This status byte is to be interpreted as follows:

Completion Status Byte Hex Value	Meaning	Hex Sense Code Returned to the Host Adapter from the Request Sense Command
00	No error. Normal Completion.	
01	Invalid Command Request	
02	Address Mark Not Found	12—No AM Found on Disk 21—Illegal Logical Block Address
03	Write Protect Error	27—Write Protected
04	Read Error	14—No Record Found 16—Data Sync Error
10	Uncorrectable ECC Error	10—ID ECC Error 11—Unrecovered Read Error

Completion Status Byte Hex Value	Meaning	Hex Sense Code Returned to the Host Adapter from the Request Sense Command
11	ECC Corrected Data Error	17—Recovered Read Error w/o ECC 18—Recovered Read Error w/ ECC
20	Controller Failure or one of many Additional Sense Codes was returned	01 03 05 06 07 08 09 1B 1C 1D 40–49
40	Seek Operation Failed	15—Seek Positioning Error 02—No Seek Complete
80	Selection Time-Out	Drive did not respond to Host Adapter
AA	Device Not Ready	04—LUN Not Ready 28—Medium Changed 29—Power On or Reset or Bus Device Reset Occurred 2A—Mode Select Parameter Changed
BB	Unknown Target Sense Error	Unknown Additional Sense Code from SCSI Device
FF	Sense Operation Failed	No sense information from

Additional output parameters are required by three BIOS commands and are supplied in the following CPU registers:

Command (HEX)	CPU Register	Output Parameter
06	AL	Drive Number of First SCSI Drive Attached
Identify SCSI Devices		80 if no standard hard disk 81 if one standard hard disk
08	DL	Number of SCSI Drives Attached
Read Drive Parameters	DH	Max value for head number (3F)
	CH	Max value for Cylinder Range (Low Byte)
	CL	Max value for Sector and Cylinder Bits 7–6 High Order Cylinder Bits Bits 5–0 Max Sector Number (20)
15	AH	Status of Operation
Read DASD		00 Drive not present or DL invalid 01 Reserved 02 Reserved 03 Fixed Disk installed
	CX,DX	Number of 512 byte blocks available on disk

BIOS Disk Commands

The host adapter's BIOS can accept functions from the DOS operating system that are required for normal operation, system booting, and normal disk operation, basic maintenance and verification functions. Refer to the following table for a summary of valid BIOS disk functions. Detailed explanations of the operation of each BIOS command follow the table.

Table 1-8. Valid BIOS Disk Functions

Command Value in AH Register (Hex Value)	Description
00	Reset Disk System
01	Read Status of Last Operation
02	Read Desired Sectors to Memory
03	Write Desired Sectors from Memory
04	Verify Desired Sectors
06	Identify SCSI Devices
08	Read Drive Parameters
09	Initialize Drive Pair Characteristics
0C	Seek
0D	Alternate Disk Reset
10	Test Drive Ready
11	Recalibrate
15	Read DASD Type

In the following descriptions, all references to the SCSI operation codes or parameters input from the host and output back to the host through the various CPU registers are stated in their Hex value for each BIOS command.

00—Reset Disk System. The BIOS issues a reset to the SCSI bus. It then sends this command on to the standard BIOS so it can reset other floppy or hard disks in the system.

Input Parameters: AH=00H
DL=Drive Number (80H to 87H)

Output Parameters: AH=Status of Operation
CF=Return Code

01—Read Status of Last Operation. The host adapter reports the status of the last operation performed by the specified disk. No SCSI activity occurs and the disk status is reset to zero.

Input Parameters: AH=01
DL=Drive Number (80H to 87H)

Output Parameters: AH=Status of Operation
CF=Completion Code

02—Read Desired Sectors to Memory. The requested sectors, defined by the input parameters, are read from the disk to the system memory. This function maps to a SCSI Read command (SCSI Opcode 08).

Input Parameters: AH=02H
DL=Drive Number (80H to 87H)
DH=Head Number
CH=Low-order Byte of Cylinder Number
CL=High-cylinder Bit and Sector Numbers
AL=Number of Sectors to Read
ES:BX=Address of Data Buffer Area

Output Parameters: AH=Status of Operation
CF=Completion Code

03—Write Desired Sectors from Memory. The requested sectors, defined by the input parameters, are written from the system memory to the indicated disk. This function maps to a SCSI Write command (SCSI Opcode 0A).

Input Parameters: AH=03H
DL=Drive Number (80H to 87H)
DH=Head
CH=Low-order Byte of Cylinder Number
CL=High-cylinder Bit and Sector Numbers
AL=Number of Sectors to Write
ES:BX=Address of Buffer Area

Output Parameters: AH=Status of Operation
CF=Return Code

04—Verify Desired Sectors. The requested sectors, defined by the input parameters, are verified to be written correctly on the SCSI disk. This function maps to a SCSI Verify command (SCSI Opcode 2F). In some special cases, for targets that do not support the SCSI Verify command, this function maps to a SCSI Read command (SCSI Opcode 08) and discards the received data.

Input Parameters: AH=04H
DL=Drive Number (80H to 87H)
DH=Head
CH=Low-order Byte of Cylinder Number
CL=High-cylinder Bit and Sector Numbers
AL=Number of Sectors to Verify
ES:BX=Address of Buffer Area

Output Parameters: AH=Status of Operation
CF=Completion Code

06—Identify SCSI Devices. This command is used to determine the number of the first SCSI drive attached to the host adapter.

Input Parameters: AH=06

Output Parameters: AH=Status of Operation
AL= Drive Number of First SCSI Drive Attached
80H if no standard hard disk
81H if one standard hard disk
CF=Completion Code

08—Read Drive Parameters. This function maps to a SCSI Read Capacity command (SCSI Opcode 25). The total logical capacity is then converted to pseudo-physical parameters.

Input Parameters: AH=08H
DL=Drive Number (80H to 87H)

Output Parameters: AH=Status of Operation
DL=Number of SCSI Drives Attached
DH=Max value for head number (3Fh)
CH=Max value for Cylinder Range (Low Byte)
CL=Max value for Sector and Cylinder
 Bits 7–6 High-order Cylinder Bits
 Bits 5–0 Max Sector Number (20h)
CF=Completion Code

09—Initialize Drive Pair Characteristics. Because SCSI CCS drives are self-configuring, this command performs no operation.

Input Parameters: AH=09H
DL=Drive Number (80H to 87H)

Output Parameters: AH=Status of Operation
CF=Completion Code

0C—Seek. This function performs a Seek operation (SCSI Opcode 0B) to the logical block address as defined by the physical parameters. This command is not required for CCS commands nor for proper SCSI device operations. Because the Seek operation is performed automatically by the Read and Write operations, it is not necessary to generate a Seek command to access data. If the addressed device reports that the Extended Seek command is not supported, the BIOS command will be completed as normal.

Input Parameters: AH=0CH
DL=Drive Number (80H to 87H)
DH=Head
CH=Cylinder
CL=High Cylinder (Sector bits=0)

Output Parameters: AH=Status of Operation
CF=Completion Code

0D—Alternate Disk Reset. The BIOS sends a SCSI bus reset to the target specified in the DL Register. A reset function request is also passed to the system's BIOS so that any internally installed hard or floppy disk(s) can be reset.

Input Parameters: AH=0DH
DL=Drive Number (80H to 87H)

Output Parameters: AH=Status of Operation
CF=Completion Code

10—Test Unit Ready. This function maps to a SCSI Test Unit Ready command (SCSI Opcode 00). After executing a Reset function, the host adapter's BIOS issues this function internally until the target is no longer busy and the Unit Attention condition is cleared.

Input Parameters: AH=10H
DL=Drive Number (80H to 87H)

Output Parameters: AH=Status of Operation
CF=Completion Code

11—Recalibrate. This function maps to a Re-zero Unit command (SCSI Opcode 01).

Input Parameters: AH=11H
DL=Drive Number (80H to 87H)

Output Parameters: AH=Status of Operation
CF=Completion Code

15—Read DASD. The BIOS of the host adapter checks the Peripheral Device Type Qualifier (returned by the SCSI Inquiry command) to verify that the device is a Direct Access Device. The BIOS then returns the logical capacity reported by the SCSI Read Capacity command in the CX and DX Registers.

Input Parameters: AH=15H
DL=Drive Number (80H to 87H)

Output Parameters: AH=Status of Operation
00 Drive not present or DL invalid
01 Reserved
02 Reserved
03 Fixed Disk installed
CX,DX= Number of 512 byte blocks available on disk
CF=Completion Code

Accessible Memory Map in Host Adapter

The Host Adapters reserve 128 bytes of data that is accessible by the host. These bytes are located in the Host Adapter's local RAM and are defined as two separate areas as shown below. The BIOS, Auto Configure Utilities (AutoSCSI) and I/O drivers can read 128 bytes by using HAC commands 91h. Finally, the host can store any changes to the 2nd area in nonvolatile memory by using HAC command 92h.

Bytes 00–63 These 64 bytes are used by BIOS as scratch ram usage. Their definition is solely controlled by BIOS. Firmware doesn't interpret any byte from this area.

Bytes 64–127 These 64 bytes are used by BIOS, AutoSCSI, and Firmware. They are used to setup the operating configuration of the Host Adapter. The BIOS or AutoSCSI or system utility can direct the controller firmware to store this data to a permanent area, such as EEPROM or Flash ROM. The BIOS and controller firmware use this data as operating parameters. For loading one of several sets of default values into this area or for storing the present values into nonvolatile memory, see HAC command 92h.

Expanded BIOS Area Definitions

These 64 bytes are used by BIOS as Scratch RAM. Information in these bytes are not stored permanently.

Expanded AutoSCSI Area Definitions

Byte	F/W	HOST	Description																																
0–1	r/w	r	Firmware internal factory setting signature (default is “FA”).																																
2	r	r/w	The number of information bytes (2-64, default is 64) stored in EEPROM starting at byte 0 of this area.																																
3–8	r/w	r	Adapter type stored as 6 byte ASCII string (e.g. “ ”, “9”, “4”, “8”, “ ”, and “ ”).																																
9	r/w	r	Adapter I/O Port Address (reserved)																																
10	r	r/w	System Configuration <table border="1"><thead><tr><th>Bit</th><th>Meaning</th></tr></thead><tbody><tr><td>0</td><td>Floppy enable (0 = disable, 1 = enable)</td></tr><tr><td>1</td><td>Floppy secondary (0 = primary, 1 = secondary)</td></tr><tr><td>2</td><td>Level trigger (0 = edge, 1 = level)</td></tr><tr><td>3</td><td>Reserved</td></tr><tr><td>4</td><td>Reserved</td></tr><tr><td>5–7</td><td>System RAM area for BIOS</td></tr></tbody></table> <table border="1"><thead><tr><th>Value</th><th>Address</th></tr></thead><tbody><tr><td>0</td><td>200h</td></tr><tr><td>1</td><td>220h</td></tr><tr><td>2</td><td>240h</td></tr><tr><td>3</td><td>300h</td></tr><tr><td>4</td><td>320h</td></tr><tr><td>5</td><td>340h</td></tr><tr><td>6</td><td>4D8h for non PCI, None for PCI</td></tr><tr><td>7</td><td>Reserved</td></tr></tbody></table>	Bit	Meaning	0	Floppy enable (0 = disable, 1 = enable)	1	Floppy secondary (0 = primary, 1 = secondary)	2	Level trigger (0 = edge, 1 = level)	3	Reserved	4	Reserved	5–7	System RAM area for BIOS	Value	Address	0	200h	1	220h	2	240h	3	300h	4	320h	5	340h	6	4D8h for non PCI, None for PCI	7	Reserved
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7	Reserved																																		
11	r	r/w	DMA Channel (default is 81h) (N/A for PCI Adapter) <table border="1"><thead><tr><th>Bit</th><th>Meaning</th></tr></thead><tbody><tr><td>0–6</td><td>Channel number</td></tr></tbody></table> <table border="1"><thead><tr><th>Value</th><th>Channel</th></tr></thead><tbody><tr><td>0</td><td>None</td></tr><tr><td>1</td><td>5</td></tr><tr><td>2</td><td>6</td></tr><tr><td>3</td><td>7</td></tr><tr><td>7</td><td>Enable auto configuration if set</td></tr></tbody></table>	Bit	Meaning	0–6	Channel number	Value	Channel	0	None	1	5	2	6	3	7	7	Enable auto configuration if set																
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7	Enable auto configuration if set																																		
12	r	r/w	Adapter Interrupt Channel (default is 83h) (N/A for PCI Adapter) <table border="1"><thead><tr><th>Bit</th><th>Meaning</th></tr></thead><tbody><tr><td>0–6</td><td>Interrupt channel number</td></tr></tbody></table> <table border="1"><thead><tr><th>Value</th><th>Channel</th></tr></thead><tbody><tr><td>0</td><td>None</td></tr><tr><td>1</td><td>9</td></tr><tr><td>2</td><td>10</td></tr><tr><td>3</td><td>11</td></tr><tr><td>4</td><td>12</td></tr><tr><td>5</td><td>14</td></tr><tr><td>6</td><td>15</td></tr><tr><td>7</td><td>Enable auto configuration if set</td></tr></tbody></table>	Bit	Meaning	0–6	Interrupt channel number	Value	Channel	0	None	1	9	2	10	3	11	4	12	5	14	6	15	7	Enable auto configuration if set										
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3	11																																		
4	12																																		
5	14																																		
6	15																																		
7	Enable auto configuration if set																																		

13	r	r/w	DMA Transfer Rate (default is 1 for ISA, 0 for others) (N/A for PCI Adapter)
			Value Meaning
			0 None
			1 5.0 MBytes/sec
			2 5.7 MBytes/sec
			3 6.7 MBytes/sec
			4 8.0 MBytes/sec
			5 10.0 MBytes/sec
			6 3.3 MBytes/sec
14	r	r/w	Adapter SCSI ID (default is 7)
15			SCSI Configuration (default is 3Fh for wide, 3Bh for narrow)
			Bit Meaning
	r	r/w	0 For non-smart termination Host Adapters: SCSI termination (Low) (0 = Off, 1 = On)
			For smart termination Host Adapters: SCSI termination (Low)
			0 Off
			1 Enable Smart Termination
			Bit Meaning
	r	r/w	1 SCSI Parity (0 = disable, 1 = enable)
	r	r/w	2 High byte SCSI termination for wide Host Adapters
			For non-smart termination Host Adapters: SCSI termination (High) (0 = Off, 1 = On)
			For smart termination Host Adapters: SCSI termination (High)
			0 Off
			1 Enable Smart Termination
	r	r/w	3 Long SCSI cable & Noisy cabling environment (0 = disable, 1 = enable)
	r	r/w	4 Maximum Sync Negotiation Transfer Rate (0 = 5 MBytes, 1 = 10 MBytes)
	r	r/w	5 SCSI bus reset (0 = disable, 1 = enable)
	-	r/w	6 Reserved
	r	r	7 SCSI Active negation (0 = disable, 1 = enable)
16	r	r/w	Bus On Delay (2–15 microseconds, default is 7) (N/A for PCI Adapter)
17	r	r/w	Bus Off Delay (1–64 microseconds, default is 4) (N/A for PCI Adapter)
18	-	r/w	BIOS Configuration (default is 32h)
			Bit Meaning
			0 Host Adapter BIOS (0 = disable, 1 = enable)
			1 BIOS redirection of INT 19 vector (0 = disable, 1 = enable)
			2 BIOS translation for greater than 1 GByte drives (0 = disable, 1 = enable)
			3 Map removable disks as fixed disks (0 = disable, 1 = enable)
			4 Reserved
			5 BIOS support for more than 2 drives (0 = disable, 1 = enable)
			6 BIOS interrupt mode (0 = disable, 1 = enable)
			7 Floptical support (0 = disable, 1 = enable)

19	r	r/w	Enable SCSI Device, Targets 0 to 7 map to bits 0 to 7 (default is FFh, all targets enabled)
20	r	r/w	Enable SCSI Device, Targets 8 to 15 map to bits 0 to 7 (default is FFh, all targets enabled)
21	r	r/w	Enable Wide SCSI Negotiation, Targets 0 to 7 map to bits 0 to 7 (default is FFh if adapter is wide, else default is 0)
22	r	r/w	Enable Wide SCSI Negotiation, Targets 8 to 15 map to bits 0 to 7 (default is FFh if adapter is wide, else default is 0)
23	r	r/w	Enable fast transfer (0 = 5 MBytes/sec, 1 = 10 MBytes/sec), Targets 0 to 7 map to bits 0 to 7 (default is FFh)
24	r	r/w	Enable fast transfer (0 = 5 MBytes/sec, 1 = 10 MBytes/sec), Targets 8 to 15 map to bits 0 to 7 (default is FFh)
25	r	r/w	Enable Sync Negotiation, Targets 0 to 7 map to bits 0 to 7 (default is FFh)
26	r	r/w	Enable Sync Negotiation, Targets 8 to 15 map to bits 0 to 7 (default is FFh)
27	r	r/w	Enable Disconnect, Targets 0 to 7 map to bits 0 to 7 (default is FFh)
28	r	r/w	Enable Disconnect, Targets 8 to 15 map to bits 0 to 7 (default is FFh)
29		r/w	Send Start Unit Command, Targets 0 to 7 map to bits 0 to 7 (default is 0)
30		r/w	Send Start Unit Command, Targets 8 to 15 map to bits 0 to 7 (default is 0)
31		r/w	Ignore BIOS Scan, Targets 0 to 7 map to bits 0 to 7 (default is 0)
32		r/w	Ignore BIOS Scan, Targets 8 to 15 map to bits 0 to 7 (default is 0)
33	r	r/w	PCI Interrupt Pin assignments, Round Robin, and VESA configuration (default is 20h)
			Bit Meaning
			0–1 PCI Interrupt Pin assignments (0 = A, 1 = B, 2 = C, & 3 = D)
			2–3 Host Adapter I/O port address
			3 2 Meaning
			0 0 Primary
			0 1 Alternate
			1 0 Disable
			1 1 Reserved
			4 Round Robin Scheme (0 = disable, 1 = enable)
			5 VESA bus speed (0 = 33 MHz or less, 1 = greater than 33 MHz)
			6 VESA burst write (0= disable, 1 = enable)
			7 VESA burst read (0=disable, 1 = enable)
34	r	r/w	Enable Ultra SCSI Negotiation, Targets 0 to 7 map to bits 0 to 7 (default is Host Adapter dependent)
35	r	r/w	Enable Ultra SCSI Negotiation, Targets 8 to 15 map to bits 0 to 7 (default is Host Adapter dependent)
36–39	r	-	Reserved (set to zero)
40	r	r/w	Reserved
41	r	r/w	Maximum LUN support in AutoSCSI.

42	r	r/w	SCAM support																												
			<table border="1"> <thead> <tr> <th>Bit</th><th>Meaning</th></tr> </thead> <tbody> <tr> <td>0–1</td><td>SCAM mode.</td></tr> <tr> <td>1 0</td><td>Mode</td></tr> <tr> <td>0 0</td><td>Reserved</td></tr> <tr> <td>0 1</td><td>Not Dominant</td></tr> <tr> <td>1 0</td><td>Reserved</td></tr> <tr> <td>1 1</td><td>Dominant</td></tr> <tr> <td>2</td><td>SCAM (0 = disable, 1 = enable)</td></tr> <tr> <td>3–4</td><td>SCAM Level</td></tr> <tr> <td>4 3</td><td>Level</td></tr> <tr> <td>0 0</td><td>Level 1</td></tr> <tr> <td>0 1</td><td>Level 2</td></tr> <tr> <td>1 x</td><td>Reserved</td></tr> <tr> <td>5–7</td><td>Reserved</td></tr> </tbody> </table>	Bit	Meaning	0–1	SCAM mode.	1 0	Mode	0 0	Reserved	0 1	Not Dominant	1 0	Reserved	1 1	Dominant	2	SCAM (0 = disable, 1 = enable)	3–4	SCAM Level	4 3	Level	0 0	Level 1	0 1	Level 2	1 x	Reserved	5–7	Reserved
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43	r	r/w	Multi-Boot option/CDROM boot/INT 13 extension																												
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44	r	r/w	Boot Device ID: Channel # and ID number For SCSI Host Adapters:																												
			<table border="1"> <thead> <tr> <th>Bit</th><th>Meaning</th></tr> </thead> <tbody> <tr> <td>0–3</td><td>SCSI device ID</td></tr> <tr> <td>4–7</td><td>Channel number for multiple channel card</td></tr> </tbody> </table>	Bit	Meaning	0–3	SCSI device ID	4–7	Channel number for multiple channel card																						
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45	r	r/w	<table border="1"> <tr> <td>Bit 7–1</td><td>Reserved (To be used by Power Saving Mode)</td></tr> <tr> <td>Bit 0</td><td>0: PCI Scanning sequence depends on BIOS INT 1A returned sequence 1: PCI Scanning sequence depends on PCI Bus # and Device #. Start with Bus # from 0 to 255, then Device # from 0 to 31.</td></tr> </table>	Bit 7–1	Reserved (To be used by Power Saving Mode)	Bit 0	0: PCI Scanning sequence depends on BIOS INT 1A returned sequence 1: PCI Scanning sequence depends on PCI Bus # and Device #. Start with Bus # from 0 to 255, then Device # from 0 to 31.																								
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Bit 0	0: PCI Scanning sequence depends on BIOS INT 1A returned sequence 1: PCI Scanning sequence depends on PCI Bus # and Device #. Start with Bus # from 0 to 255, then Device # from 0 to 31.																														
46	r	r/w	Enable SCSI T-L-Q Nexus support, Targets 0 to 7 map to bits 0 to 7. (default is Host Adapter dependent)																												
			<table border="1"> <thead> <tr> <th>Bit</th><th>Meaning</th></tr> </thead> <tbody> <tr> <td>0</td><td>Blocks non-tag command to different LUN in the same target ID.</td></tr> <tr> <td>1</td><td>Allows non-tag command to different LUN in the same target ID.</td></tr> </tbody> </table>	Bit	Meaning	0	Blocks non-tag command to different LUN in the same target ID.	1	Allows non-tag command to different LUN in the same target ID.																						
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48	r	r/w	Enable H/A to renegotiate the sync rate after check condition. Target 0 to 7 map to bit 0 to 7. (default is disable)						
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50–59	-	-	Reserved						
60–61	r/w	-	Reserved for manufacturing diagnostic purpose <table border="1"> <thead> <tr> <th>Byte Value</th><th>60 61</th></tr> </thead> <tbody> <tr> <td>00 00</td><td>Normal operating condition</td></tr> <tr> <td>'C' 'D'</td><td>Manufacturing Test in process.</td></tr> </tbody> </table>	Byte Value	60 61	00 00	Normal operating condition	'C' 'D'	Manufacturing Test in process.
Byte Value	60 61								
00 00	Normal operating condition								
'C' 'D'	Manufacturing Test in process.								
62–63	r/w	-	These two bytes are used by the manufacturing test program. Under normal operation, they are cleared to 0. During testing, these two bytes are written with 'C', 'D' to indicate testing in progress.						
			Firmware internal usage only (Checksum)						

SCSI Electrical Interface

The host adapter interfaces the host system bus to a SCSI general purpose 16-bit bidirectional bus. The SCSI port is controlled by a SCSI interface chip which supports arbitration, selection, and reselection with a minimum need for processor attention. The SCSI interface controller supports target mode and synchronous SCSI transfers. BusLogic Wide SCSI host adapters (non-differential) include single-ended drivers and receivers (built into the SCSI interface chip) which allow a maximum cable length of six meters. BusLogic Wide SCSI host adapters with differential include differential drivers and receivers which allow a maximum cable length of 25 meters.

A minimum conductor size of 28 AWG should be employed to minimize noise effects and ensure proper distribution of terminator power.

There are three SCSI connectors:

- An internal 50-pin, non-shielded SCSI device connector consisting of two rows of 25 male pins with adjacent pins 2.54 mm (0.1 in) apart.
- An internal 68-pin Wide SCSI device connector consisting of 4 rows of 17 pins.
- An external 68-pin Wide SCSI shielded SCSI device connector.

BusLogic Wide SCSI host adapters (non-differential) use active termination. Termination is software selectable. All assigned signals are terminated with 110 ohms to the 2.85 volts voltage regulator. All signals must use open-collector or three-state drivers.

For BusLogic Wide SCSI host adapters with differential, all signals are terminated with 330 ohms from the differential nodes to +5 volts and ground, respectively, and with 150 ohms between each differential pair. Termination is configured using on-board terminator resistor packs.

Single-Ended Output Characteristics. Each signal driven has the following output characteristics when measured at the connector:

Signal assertion	= 0.0 volts dc to 0.4 volts
Minimum driver output capability	= 48 milliamps (sinking) at 0.5 volts dc (7438 or equivalent)
Signal negation	= 2.5 volts dc to 5.25 volts dc.

Devices receiving the host adapter's output should be of the SCHMITT trigger type to improve noise immunity, 74LS14, 74LS240, or the equivalent. The device should not load the bus with more than two standard low-power Shottky (LS) input loads per line, and should terminate the controller output signals with active 110 ohm terminators or passive 220/330 ohm terminators.

Single-Ended Input Characteristics. Each signal received by the controller should have the following input characteristics when measured at the SCSI device's connector:

Signal true	= 0.0 volts dc to 0.8 volts dc
Maximum total input load	= -0.4 millamps at 0.4 volts dc
Signal false	= 2.0 volts dc to 5.25 volts dc
Minimum input hysteresis	= 0.2 volts dc.

Differential Output Characteristics. Each signal driven should have the following output characteristics when measured at the connector:

Signal true	= when +SIGNAL is more positive than -SIGNAL
Maximum low-level output current	= 55 millamps at 1.7 volts dc maximum
Maximum high-level output current	= -55 millamps at 2.7 volts dc maximum

Differential Input Characteristics. Each signal received by the controller should have the following input characteristics when measured at the SCSI device's connector:

Signal true	= when +SIGNAL is more positive than -SIGNAL
Maximum input load	= <u>±</u> 2.0 millamps
Maximum input capacitance	= 25 pF
Minimum input hysteresis	= 35 millivolts

Terminator Power (Pin 26). BusLogic recommends that the two devices at each end of the cable provide termination.

VTerm. =	4.25 volts dc to 5.25 volts dc
	1.0 amp minimum source drive capability
	1.0 millamp maximum sink capability

Refer to Figure 1-12 for a schematic representation of how terminator power is provided on the host adapter.

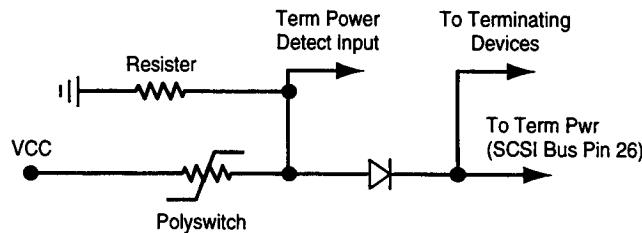


Figure 1-12. Terminator Power Schematic

Terminators. Terminators are required for reliable operation of the SCSI bus. The first and last SCSI devices connected together on a SCSI bus must have terminators installed or enabled. Terminators can be connected to either the SCSI device itself or affixed to the SCSI cable ends.

Termination settings on your Wide SCSI host adapter are as follows:

- **Low Byte** terminates data bits 0–7.
- **High Byte** terminates data bits 8–15.
- **Low Byte and High Byte together (default)** terminate all signals.

The following table indicates what your **Low Byte** and **High Byte** settings should be based on the connector and the attached devices (8-bit or 16-bit).

Table 1-9. Termination Options

External 68-Pin Connector	Internal 68-Pin Connector	Internal 50-Pin Connector	Low Byte	High Byte	Notes
-	-	8-bit	On	On	Select if the adapter is configured at the end of the SCSI chain using only one of the connectors.
8/16-bit	-	-	On	On	
-	16-bit	-	On	On	
8/16-bit	-	8-bit	Off	On	Select if the adapter is in the middle of a SCSI chain, but is configured with one 50-pin and one 68-pin connector. Termination is required on the cable ends or on the devices at the ends of the cable.
-	16-bit	8-bit	Off	On	
16-bit	16-bit	-	Off	Off	No termination is required if the adapter is in the middle of the SCSI chain using two 68-pin connectors with 16-bit devices.
8-bit	16-bit	-	Off	On	High Byte must be On if the adapter is in the middle of the SCSI chain using two 68-pin connectors with one attached to 8-bit devices only .

Note the following:

- This table assumes that you would use the 50-pin connector to connect internal 8-bit devices and, therefore, does not include settings for 8-bit devices on the internal 68-pin connector.
- When 8-bit and 16-bit devices are mixed on the cable attached to a 68-pin connector, you still need to terminate all signals.

SCSI Signal Interface for the 50-Pin Connector

The host adapter's single-ended SCSI interface signals for the internal 50-pin SCSI connector is shown in Table 1-13. A plus sign (+) denotes an active high signal. A hyphen (-) denotes an active low signal.

Table 1-10. Single-Ended SCSI Interface Signal Pin Assignments

Signal Pin	Signal Name	Signal Pin	Signal Name	Direction (Initiator)
1	Ground	2	-DB0	I/O
3	Ground	4	-DB1	I/O
5	Ground	6	-DB2	I/O
7	Ground	8	-DB3	I/O
9	Ground	10	-DB4	I/O
11	Ground	12	-DB5	I/O
13	Ground	14	-DB6	I/O

Table 1-10. Single-Ended SCSI Interface Signal Pin Assignments (Continued)

Signal Pin	Signal Name	Signal Pin	Signal Name	Direction (Initiator)
15	Ground	16	-DB7	I/O
17	Ground	18	-DBP	
19	Ground	20	Ground	
21	Ground	22	Ground	
23	Reserved	24	Reserved	
25	Open	26	TERMPWR	
27	Reserved	28	Reserved	
29	Ground	30	Ground	
31	Ground	32	-ATN	Output
33	Ground	34	Ground	
35	Ground	36	-BSY	I/O
37	Ground	38	-ACK	Output
39	Ground	40	-RST	I/O
41	Ground	42	-MSG	Input
43	Ground	44	-SEL	I/O
45	Ground	46	-C/D	Input
47	Ground	48	-REQ	Input
49	Ground	50	-I/O	Input

The following table shows the pin assignments for the 50-pin differential SCSI connector. A plus sign (+) denotes an active high signal. A hyphen (-) denotes an active low signal.

Table 1-11. 50-Pin Differential SCSI Interface Signal Pin Assignments

Signal Pin	Signal Name	Signal Pin	Signal Name	Direction (Initiator)
1	Ground	2	Ground	
3	+DB0	4	-DB0	I/O
5	+DB1	6	-DB1	I/O
7	+DB2	8	-DB2	I/O
9	+DB3	10	-DB3	I/O
11	+DB4	12	-DB4	I/O
13	+DB5	14	-DB5	I/O
15	+DB6	16	-DB6	I/O
17	+DB7	18	-DB7	I/O
19	+DBP	20	_DBP	
21	+DIFFSENS	22	Ground	
23	Reserved	24	Reserved	
25	TERMPWR	26	TERMPWR	
27	Reserved	28	Reserved	
29	+ATN	30	-ATN	Output

Table 1-11. 50-Pin Differential SCSI Interface Signal Pin Assignments (Continued)

Signal Pin	Signal Name	Signal Pin	Signal Name	Direction (Initiator)
31	Ground	32	Ground	
33	+BSY	34	-BSY	
35	+ACK	36	-ACK	Output
37	+RST	38	-RST	Output
39	+MSG	40	-MSG	Output
41	+SEL	42	-SEL	Input
43	+C/D	44	-C/D	I/O
45	+REQ	46	-REQ	Input
47	+I/O	48	-I/O	Input
49	Ground	50	Ground	

SCSI Signal Interface for the 68-Pin Connectors

The host adapter's SCSI interface signals for the 68-pin internal and external SCSI connectors are shown in Table 1-13. A plus sign (+) denotes an active high signal. A hyphen (-) denotes an active low signal.

Table 1-12. Single-Ended 68-Pin SCSI Interface Signal Pin Assignments

Signal Pin	Signal Name	Signal Pin	Signal Name	Direction (Initiator)
1	Ground	2	-DB12	I/O
3	Ground	4	-DB13	I/O
5	Ground	6	-DB14	I/O
7	Ground	8	-DB15	I/O
9	Ground	10	-DBP1	I/O
11	Ground	12	-DB0	I/O
13	Ground	14	-DB1	I/O
15	Ground	16	-DB2	I/O
17	Ground	18	-DB3	I/O
19	Ground	20	-DB4	I/O
21	Ground	22	-DB5	I/O
23	Ground	24	-DB6	I/O
25	Ground	26	-DB7	I/O
27	Ground	28	-DBP	I/O
29	Ground	30	Ground	
31	Ground	32	Ground	
33	TERMPWR	34	TERMPWR	Output
35	TERMPWR	36	TERMPWR	Output
37	Reserved	38	Reserved	
39	Ground	40	Ground	
41	Ground	42	-ATN	Output

Table 1-12. Single-Ended 68-Pin SCSI Interface Signal Pin Assignments (Continued)

Signal Pin	Signal Name	Signal Pin	Signal Name	Direction (Initiator)
43	Ground	44	Ground	
45	Ground	46	-BSY	I/O
47	Ground	48	-ACK	Output
49	Ground	50	-RST	I/O
51	Ground	52	-MSG	Input
53	Ground	54	-SEL	I/O
55	Ground	56	-C/D	Input
57	Ground	58	--REQ	Input
59	Ground	60	-I/O	Input
61	Ground	62	-DB8	I/O
63	Ground	64	-DB9	I/O
65	Ground	66	-DB10	I/O
67	Ground	68	-DB11	I/O

The following table shows the pin assignments for the 68-pin differential SCSI connector. A plus sign (+) denotes an active high signal. A hyphen (-) denotes an active low signal.

Table 1-13. 68-Pin Differential SCSI Interface Signal Pin Assignments

Signal Pin	Signal Name	Signal Pin	Signal Name	Direction (Initiator)
1	+DB12	2	-DB12	I/O
3	+DB13	4	-DB13	I/O
5	+DB14	6	-DB14	I/O
7	+DB15	8	-DB15	I/O
9	+DBP1	10	-DBP1	I/O
11	Ground	12	Ground	
13	+DB0	14	-DB0	I/O
15	+DB1	16	-DB1	I/O
17	+DB2	18	-DB2	I/O
19	+DB3	20	-DB3	I/O
21	+DB4	22	-DB4	I/O
23	+DB5	24	-DB5	I/O
25	+DB6	26	-DB6	I/O
27	+DB7	28	-DB7	I/O
29	+DBP	30	-DBP	I/O
31	DIFFSENS	32	Ground	
33	TERMPWR	34	TERMPWR	Output
35	TERMPWR	36	TERMPWR	Output
37	Reserved	38	Reserved	
39	+ATN	40	-ATN	Output

Table 1-13. 68-Pin Differential SCSI Interface Signal Pin Assignments (Continued)

Signal Pin	Signal Name	Signal Pin	Signal Name	Direction (Initiator)
41	Ground	42	Ground	
43	+BSY	44	-BSY	I/O
45	+ACK	46	-ACK	Output
47	+RST	48	-RST	I/O
49	+MSG	50	-MSG	Input
51	-SEL	52	-SEL	I/O
53	+C/D	54	-C/D	Input
55	+REQ	56	--REQ	Input
57	+I/O	58	-I/O	Input
59	Ground	60	Ground	
61	+DB8	62	-DB8	I/O
63	+DB9	64	-DB9	I/O
65	+DB10	66	-DB10	I/O
67	+DB11	68	-DB11	I/O

SCSI Signal Definitions

The definitions for SCSI interface signals are shown in Table 1-14.

Table 1-14. SCSI Interface Signal Descriptions

Differential Signal	Single-Ended Signal	Definition
-RST +RST	-RST	Reset: This “OR Tied” signal, which is asserted by the initiator, causes the SCSI bus to cease all operations and return to the Idle condition. This signal is normally used during a power-up sequence. A reset during a Write operation would cause incorrect data to be written on the disk.
-SEL +SEL	-SEL	Select: When this signal is asserted by the initiator, along with an initiator ID and target ID data bit (0–7 for eight-bit devices, 0–15 for 16-bit devices), it causes the addressed target to be selected. This signal must be deasserted by the initiator after the target asserts the Busy (-BSY) signal in response to a proper selection.
-BSY +BSY	-BSY	Busy: When this “OR Tied” signal is asserted, it indicates that the bus is being used.
-C/D +C/D	-C/D	Control/Data: When this signal is asserted by the target, it indicates that control information is to be transferred on the data bus. Deassertion of this signal indicates that data information is to be transferred on the data bus.
-I/O +I/O	-I/O	Input/Output: When this signal is asserted by the target, it indicates that information will be transferred to the initiator from the target. Deassertion indicates that information will be transferred to the target from the initiator. This signal is also used to distinguish between the Selection and Reselection phases.

Table 1-14. SCSI Interface Signal Descriptions (Continued)

Differential Signal	Single-Ended Signal	Definition
-REQ +REQ	-REQ	Request: When this signal is asserted by the target, it indicates that a 16-bit byte is to be transferred on the data bus. The Request (REQ) signal is deasserted following the assertion of the Acknowledge (ACK) signal from the host. The Request (REQ) and Acknowledge (ACK) signals control the handshaking.
-ACK +ACK	-ACK	Acknowledge: When this signal is asserted by the initiator, it indicates data has been accepted by the initiator or that data is ready to be transferred from the initiator to the target.
-ATN +ATN	-ATN	Attention: This signal is driven by the initiator to indicate the Attention condition.
-MSG +MSG	-MSG	Message: When this signal is asserted by the target, it indicates the Message phase. The state of the Input/Output (-I/O) signal when it is asserted indicates MESSAGE IN or MESSAGE OUT.
-DB0-7 -DBP +DB0-7 +DBP	-DB0-7 & -DBP	Data Bits & Parity: These eight bidirectional data lines and one odd parity signal are used to transfer 8-bit parallel data over the SCSI bus. Bit 7 is the MSB and has highest priority during the Arbitration phase. Parity is not valid during the Arbitration phase. The use of the parity bit is an option. See the adapter's user's guide to determine how to enable or disable SCSI parity on your adapter.

Internal Diagnostics

When the host adapter is powered up, an onboard diagnostic routine is run to verify that the major functional components of the board are operating correctly. The bus master chip, the SCSI controller chip, the firmware PROM, the local RAM and internal data buses are tested. Results of the tests are indicated by an LED on the board.

The LED will first turn on when power is applied. If the diagnostics find no malfunctions, the LED will then go off. In normal operation, the LED will be illuminated when command or SCSI bus activity occurs on the board.

If an error is detected by the diagnostics, the LED will repeatedly flash a specific number of times, with a long pause between flashes, to indicate the board function which failed. This will continue until the board is powered down or reset. Failure interpretation from the number of flashes is as follows:

Number of LED Flashes	Interpretation of Failure
Always On	host adapter is not operating
1	Firmware ROM checksum failure
2	Local RAM test failure
3	SCSI controller chip or SCSI interface failure
4	Internal data bus failure
5	Internal address bus failure
6	Bus master chip failure
Constantly Flashing	Term power failure

List of Acronyms

BIOS	Basic Input/Output System
CCB	Command Control Block
CCS	Common Command Set
CDB	Command Descriptor Block
CPU	Central Processing Unit
DMA	Direct Memory Access
DRAM	Dynamic Random-Access Memory
EISA	Extended Industry Standard Architecture
FCC	Federal Communications Commission
FIFO	First-In First-Out
I/O	Input/Output
ISA	Industry Standard Architecture
LSB	Least Significant Bit
LU	Logical Unit
LUN	Logical Unit Number
MPU	Microprocessor Unit
MSB	Most Significant Bit
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
POS	Programmable Option Select
PROM	Programmable Read-Only Memory
RAM	Random-Access Memory
RFI/EMI	Radio Frequency Interference/Electromagnetic Interference
ROM	Read-Only Memory
SCSI ID	Small Computer System Interface Identification
VL-BUS	VESA (Video Electronics Standards Association) Local Bus

Part 2: Contents

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Introduction

The BusLogic BT-948, BT-958 and BT-958D PCI Ultra/Fast SCSI Host Adapters are intelligent PCI to SCSI bus master host adapters based on BusLogic-designed, universal ASIC technology. Each provides a high-performance interconnection between the Peripheral Component Interconnect (PCI) bus and Small Computer System Interface (SCSI) peripheral devices. The BT-948 supports up to 7 SCSI devices. The BT-958 and BT-958D support up to 15 SCSI devices.

The BT-948, BT-958, and BT-958D are designed for multitasking environments such as Windows NT, Windows95, NetWare, OS/2 and UNIX. They support a full 32-bit data path with 32-bit addressing which can access up to four gigabytes of system memory.

The BT-948, BT-958 and BT-958D adapters comply with PCI Specification Rev. 2.0 and Rev. 2.1, operating at the maximum PCI local bus rate of 133 MBytes/sec in 32-bit data burst mode. BusLogic host adapters offer exceptionally high product reliability due to reduced component count and lower power consumption. Minimized command overhead results in faster command execution. Adapter BIOS supports disks with over 8 GBytes capacity.

BT-948 Host Adapter

The BT-948 adapter is shown in Figure 2-1. It is an 8-bit Parallel Single-Ended SCSI host adapter with smart detection controlled active termination.

The BT-948, supports up to 7 SCSI devices with asynchronous data rates of up to 7 MBytes/sec and synchronous data rates of up to 20 MBytes/sec in Fast-20 Mode (UltraSCSI) with proper termination and cabling.

The BT-948 has one internal 50-pin connector (J2) and one external 50-pin connector (J1).

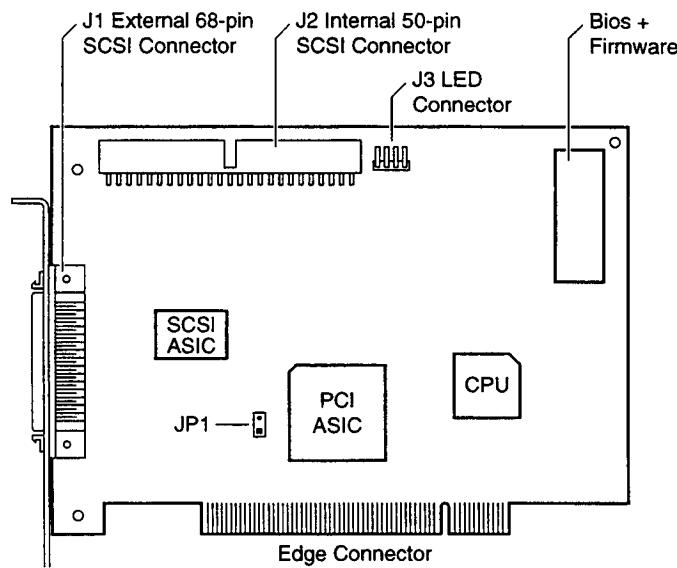


Figure 2-1. The BT-948 Host Adapter

BT-958 Host Adapter

The BT-958 is shown in Figure 2-2. It is a 16-bit parallel single-ended SCSI host adapter with software controlled active termination.

The BT-958 supports up to 15 SCSI devices with asynchronous data rates of up to 14 MBytes/sec and synchronous data rates of up to 40 MBytes/sec in Fast-40 Mode (UltraSCSI) with proper termination and cabling.

The BT-958 has one internal 50-pin connector (J2) and one internal 68-pin connector (J4) and one 68-pin external connector (J1).

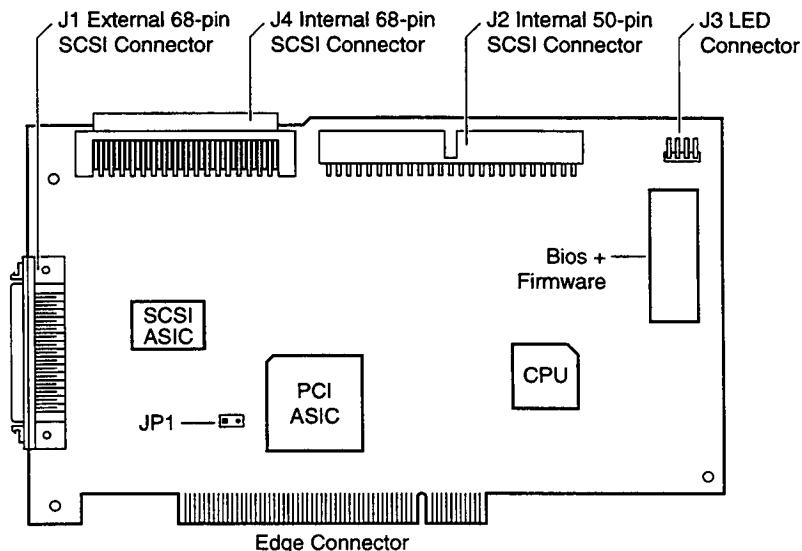


Figure 2-2. The BT-958 Host Adapter

BT-958D Host Adapter

The BT-958D is shown in Figure 2-3. It is a 16-bit parallel differential SCSI host adapter with standard differential termination. The BT-958D supports up to 15 SCSI devices with asynchronous data transfer rates of up to 14 MBytes/sec on synchronous data rates of up to 40 MBytes/sec in Fast-40 Mode (UltraSCSI) with proper termination and cabling. The BT-958D has one 50-pin internal connector (J2) and one 68-pin internal connector (J4) and one 68-pin external connector (J1).

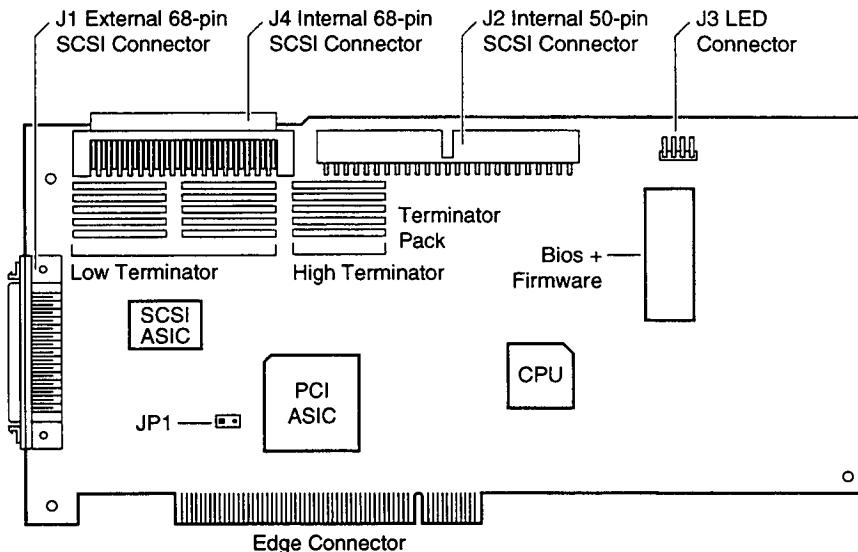


Figure 2-3. The BT-958D Host Adapter

Configuration

Plug and Play Operation. BT-948, BT-958 and BT-958D configuration is handled by the PCI motherboard. Operating parameters can be adjusted using AutoSCSI™, a menu-driven utility residing in the adapter's Read Only Memory (ROM).

Features

- SCAM Support

The BT-948, BT-958, and BT-958D adapters support the SCSI-3 SCAM Level-I protocol for SCSI ID assignment. SCAM devices do not require manual SCSI ID assignment. The BT-948, BT-958, and BT-958D adapters assign a SCSI ID to the device as required. See the owner's manual for your SCSI devices to determine whether or not they support SCAM.

- Fast data transfer rates

The BT-948, BT-958 and BT-958D adapters support standard data transfer rates including Fast SCSI-2 at 10 megabytes per second, the Ultra SCSI (Fast-20) rates at 20 megabytes per second, Fast/Wide at 20 megabytes per second, and Ultra SCSI (Fast-40) rate at 40 megabytes per second.

- SmartTerm™
The BT-948 and BT-958 adapters have no onboard jumpers for termination. With SmartTerm, the BT-948 and BT-958 adapters determine the configuration of the daisy chained devices, and self terminate as required. See the owner's manual for your SCSI devices to determine how they support termination.
- SeqEngine™
The combination of the local processor and the SeqEngine provide automated SCSI command processing which reduces SCSI command overhead by minimizing the need to interface with the host processor. This results in improved performance.
- Local Processor
A high-speed local processor offloads the host CPU I/O task maintenance and monitor improving overall system CPU utilization especially in multitasking systems.

Hardware Requirements

Your PCI computer needs:

- One available PCI Busmaster slot for each adapter being installed
- At least one 3.5" floppy drive
- DC power for an internal 3.5" SCSI drive or an external subsystem

You'll need the following cables:

- A 50-pin cable to connect the BT-948 to external devices.
- A 68-pin cable to connect the BT-958 or BT-958D to Wide SCSI external devices
- A 68-pin, flat ribbon cable to connect internal Wide SCSI devices to the BT-958 or BT-958D
- A 50-pin, flat ribbon cable to connect internal Narrow SCSI devices to the BT-948, BT-958 or BT-958D
- An optional four-pin (or two-pin) cable to connect the drive activity LED on the host front panel to the BT-948, BT-958, and BT-958D

Note: The device activity LED cable is usually supplied with the host system.

The peripherals you are attaching to the BT-948, BT-958, or BT-958D should be SCSI-2 or SCSI-3 Common Command Set (CCS) compatible.

Software Requirements

You may need the following software:

- Software for hard drive set-up to perform partitioning and high-level formatting
- Operating system software for hard drives being installed
- Device drivers if not already embedded in the operating system

Device Driver Needs

BusLogic has embedded (built-in) driver support in most popular operating systems. No additional drivers are needed for most standard installations.

If support for the kind of device (or the number of devices) you are installing is not embedded in your operating system, you will need additional drivers. These may be available with the device. Consult your device documentation for more information.

BusLogic also offers drivers where embedded support is not available (e.g., older operating system versions, etc.). Drivers available in the BusLogic SCSI Host Adapter Software Kit allow:

- Multiple BusLogic host adapters
- Up to seven (for narrow host adapters) and fifteen (for wide host adapters) SCSI peripheral devices (hard drives, etc.) per adapter
- Connectivity to SCSI tape drives, magneto optical (MO) disk drives and CD-ROM drives and other devices

See the *BusLogic SCSI Host Adapter Software Installation Guide* if you are installing BusLogic drivers.

Supported Operating System/Driver Support

BusLogic SCSI adapter driver support is provided for the following operating systems:

- PC/MS DOS 5.0 or above
- IBM OS/2 2.1x and Warp
- Windows 95
- Windows 3.x
- Windows NT 3.1, 3.5x
- NetWare 3.1x, 4.x
- Solaris (for X86)
- SCO UNIX
- Interactive UNIX
- UNIXWare

PC-DOS, MS-DOS and Windows. Your host adapter's onboard BIOS allows you to attach up to seven SCSI disk drives (BT-948 adapter), or eight (limited by DOS) SCSI disk drives (BT-958 or BT-958D adapters) without additional software under PC or MS-DOS 5.0 and above. Earlier versions of DOS only allow support for up to two hard disk drives.

BusLogic offers device drivers that support ASPI (Advanced SCSI Program Interface) for configurations where more hard drives are needed than your version of DOS can support. BusLogic also offers CD-ROM drivers for DOS and Windows.

If you are installing other types of devices under DOS and Windows, such as a tape backup device or a scanner, you will need to install additional drivers that support the ASPI interface to operate those devices. Those drivers are usually available packaged with the device or from third party sources.

Note: You can obtain the latest BusLogic driver updates from the BusLogic Bulletin Board System (BBS) via modem at 408-492-1984. (up to 14.4K, 8,1,N), FTP site at <ftp://buslogic.com>, World Wide Web site at <http://www.buslogic.com>.

Reference Documents

You should have the following documents on hand during installation:

- The installation and set-up guide for your computer
- The installation guide for your SCSI peripherals (e.g., hard drive, CD-ROM or tape drive)
- Operating system installation and user's guide
- Installation guide for BusLogic or third-party device drivers

Specifications

Dimensions:	BT-948 6" x 4.2" BT-958 6.5" x 4.2" BT-958D 7.8" x 4.2"
Electrical:	
Operating Voltage	5±0.25V
Operating Current	.5A Max.
Max. Ripple/Noise	100 mV
Environmental:	
Temperature	0°C to 60°C (32°F to 126°F)
Relative Humidity	10% to 95% non-condensing
Altitude	0 to 10,000 ft. operating 0 to 15,000 ft. non-operating
Interface Connections:	
SCSI Internal	68-pin Wide SCSI connector (BT-958 and BT-958D only) 50-pin double-row connector
SCSI External	68-pin Wide shielded SCSI connector (BT-958 and BT-958D only) 50-pin shielded SCSI connector (BT-948 only)
To/From System	PCI standard edge connector
MTBF:	90,000 hours

Electrical Interface

This section provides the user with a complete description of the name, function, and applicable logic level of all signals between the BusLogic PCI host adapter and the PCI host system.

PCI System Bus Electrical Interface

The PCI host adapter is electrically and mechanically compatible with the Input/Output (I/O) bus used in PCI computers. Physically, this Input/Output bus is contained on the card edge connector. The bus master control logic on the PCI host adapter controls the PCI system bus arbitration and data transfer operations. During bus master data transfers, the PCI host adapter takes control of the system bus and transfers data directly to and from the main system memory. Both odd and even starting addresses are supported by the PCI host adapter.

The PCI system I/O bus provides the necessary hardware interface to the host Central Processing Unit (CPU) to allow it to communicate with the PCI host adapter. Figure 2-4 identifies the positions of connector rows on the PCI host adapter's board edge.

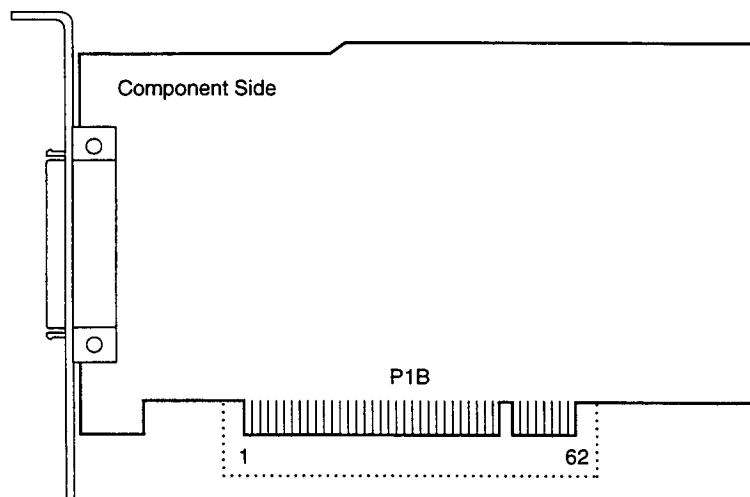


Figure 2-4. Connector Rows on the PCI Host Adapter's Board Edge

Summary of PCI Signals

Tables 2-1 and 2-2 summarize the pin assignments for the PCI board's 124-pin edge connector. Following are the signal type definitions used in the tables:

in	Input is a standard input-only signal.
out	Totem Pole Output is a standard active driver.
t/s	Tri-State® is a bi-directional, tri-state input/output pin.
s/t/s	Sustained Tri-State is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives an s/t/s pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving an s/t/s signal any sooner than one clock after the previous owner tri-states it. A pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
o/d	Open Drain allows multiple devices to share as a wire-OR.

Table 2-1. PCI Board Pin-outs for Side A (Solder Side)

Pin #	Signal Name	Type
1	TRST#	in
2	+12V	Power
3	TMS	in
4	TDI	in
5	+5V	Power
6	INTA#	o/d
7	INTC#	o/d
8	+5V	Power
9	Reserved	Not Used
10	+5V	Power
11	Reserved	Not Used
12	Ground	Ground
13	Ground	Ground
14	Reserved	Not Used
15	RST#	In
16	+5V	Power
17	GNT#	t/s
18	Ground	Ground
19	Reserved	Not Used
20	AD[30]	t/s
21	+3.3V	Power
22	AD[28]	t/s
23	AD[26]	t/s
24	Ground	Ground
25	AD[24]	t/s
26	IDSEL	in

Table 2-1. PCI Board Pin-outs for Side A (Solder Side) (Continued)

Pin #	Signal Name	Type
27	+3.3V	Power
28	AD[22]	t/s
29	AD[20]	t/s
30	Ground	Ground
31	AD[18]	t/s
32	AD[16]	t/s
33	+3.3V	Power
34	FRAME#	s/t/s
35	Ground	Ground
36	TRDY#	s/t/s
37	Ground	Ground
38	STOP#	s/t/s
39	+3.3V	Power
40	SDONE	in/out
41	SBO#	in/out
42	Ground	Ground
43	PAR	t/s
44	AD[15]	t/s
45	+3.3V	t/s
46	AD[13]	t/s
47	AD[11]	t/s
48	Ground	Ground
49	AD[09]	t/s
50	Keyway	Keyway
51	Keyway	Keyway
52	C/BE[0]#	t/s
53	+3.3V	Power
54	AD[06]	t/s
55	AD[04]	t/s
56	Ground	Ground
57	AD[02]	t/s
58	AD[00]	t/s
59	+5V	Power
60	REQ64#	s/t/s
61	+5V	Power
62	+5V	Power

Table 2-2. PCI Board Pin-outs for Side B (Component Side)

Pin #	Signal Name	Type
1	-12V	Power
2	TCK	in
3	Ground	Ground
4	TDO	out
5	+5V	Power
6	+5V	Power
7	INTB#	o/d
8	INTD#	o/d
9	PRSNT1#	?
10	Reserved	Not Used
11	PRSNT2#	?
12	Ground	Ground
13	Ground	Ground
14	Reserved	Not Used
15	Ground	Ground
16	CLK	in
17	Ground	Ground
18	REQ#	t/s
19	+5V	Power
20	AD[31]	t/s
21	AD[29]	t/s
22	Ground	Ground
23	AD[27]	t/s
24	AD[25]	t/s
25	+3.3V	Power
26	C/BE[3]#	t/s
27	AD[23]	t/s
28	Ground	Ground
29	AD[21]	t/s
30	AD[19]	t/s
31	+3.3V	Power
32	AD[17]	t/s
33	C/BE[2]#	t/s
34	Ground	Ground
35	IRDY#	s/t/s
36	+3.3V	Power
37	DEVSEL#	s/t/s
38	Ground	Ground

Table 2-2. PCI Board Pin-outs for Side B (Component Side) (Continued)

Pin #	Signal Name	Type
39	LOCK#	s/t/s
40	PERR#	s/t/s
41	+3.3V	Power
42	SERR#	o/d
43	+3.3V	Power
44	C/BE[1]#	t/s
45	AD[14]	t/s
46	Ground	Ground
47	AD[12]	t/s
48	AD[10]	t/s
49	Ground	Ground
50	Keyway	Keyway
51	Keyway	Keyway
52	AD[08]	t/s
53	AD[07]	t/s
54	+3.3V	Power
55	AD[05]	t/s
56	AD[03]	t/s
57	Ground	Ground
58	AD[01]	t/s
59	+5V	Power
60	ACK64#	s/t/s
61	+5V	Power
62	+5V	Power

PCI Edge Connector Signal Descriptions

This section lists the PCI signal descriptions.

Table 2-3. Signal Descriptions

Signal	Definition
AD[31::00]	<p><i>Address and Data</i> are multiplexed on the same PCI pins. A bus transaction consists of an address¹ phase followed by one or more data phases. PCI supports both read and write bursts.</p> <p>The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted, and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.</p>

Table 2-3. Signal Descriptions (Continued)

Signal	Definition
C/BE[3::0]#	<i>Bus Command and Byte Enables</i> are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
CLK	<i>Clock</i> provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, IRQA#, IRQB#, IRQC#, and IRQD#, are sampled on the rising edge of CLK, and all other timing parameters are defined with respect to this edge. PCI operates up to 33 MHz, and in general, the minimum frequency is DC (0 Hz).
DEVSEL#	<i>Device Select</i> , when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
FRAME#	<i>Cycle Frame</i> is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase.
GNT#	<i>Grant</i> indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT#.
IDSEL	<i>Initialization Device Select</i> is used as a chip select during configuration read and write transactions.
INTA# INTB# INTC# INTD#	<p>Interrupts on PCI are optional and are defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function (i.e., a single device into which several independent functions have been integrated. Each function on a multi-function device has its own configuration space.) device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.</p> <p><i>Interrupt A</i> is used to request an interrupt. <i>Interrupt B</i> is used to request an interrupt and only has meaning on a multi-function device. <i>Interrupt C</i> is used to request an interrupt and only has meaning on a multi-function device. <i>Interrupt D</i> is used to request an interrupt and only has meaning on a multi-function device.</p>
IRDY#	<i>Initiator Ready</i> indicates the initiating agent’s (bus master’s) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::0]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
LOCK#	<i>Lock</i> indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it must also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them must also implement LOCK#.
PAR	<i>Parity</i> is even ² parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00] but delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.

Table 2-3. Signal Descriptions (Continued)

Signal	Definition
PERR#	<i>Parity Error</i> is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# and completed a data phase.
REQ#	<i>Request</i> indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# .
RST#	<i>Reset</i> is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be tri-stated. SERR# (open drain) is floated. SBO# and SDONE ³ may optionally be driven to a logic low level if tri-state outputs are not provided here. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD , C/BE# , and PAR signals from floating during reset, the central device may drive these lines during reset (bus parking) but only to a logic low level—they may not be driven high. REQ64# has meaning at the end of reset. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
SERR#	<i>System Error</i> is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. The pullup may take two to three clock periods to fully restore SERR# . The agent that reports SERR# s to the operating system does so anytime SERR# is sampled asserted.
STOP#	<i>Stop</i> indicates the current target is requesting the master to stop the current transaction.
TRDY#	<i>Target Ready</i> indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY# . A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00] . During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.

1. The DAC uses two address phases to transfer a 64-bit address.
2. The number of “1”s on **AD[31::00]**, **C/BE[3::0]#**, and **PAR** equal an even number.
3. **SDONE** and **SBO#** have no meaning until **FRAME#** is asserted indicating the start of a transaction.

PCI Bus Master Transaction Diagrams

Read Transactions

Figure 2-5 illustrates a read transaction and starts with an address phase which occurs when **FRAME#** is asserted for the first time and occurs on clock 2. During the address phase **AD[31:00]** contain a valid address and **C/BE[3:0]#** contain a valid bus command.

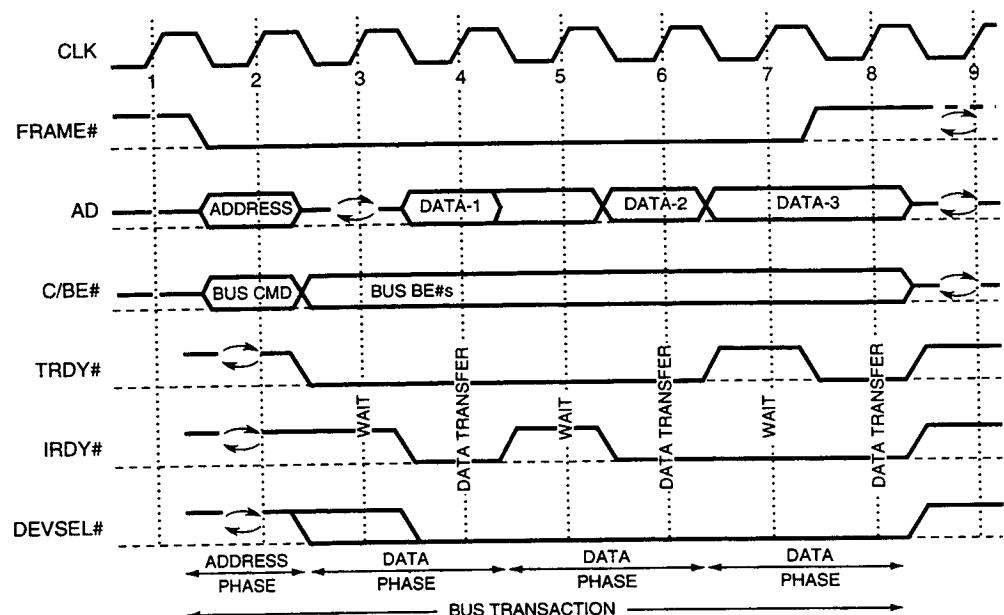


Figure 2-5. Basic Read Operation

The first clock of the first data phase is clock 3. During the data phase **C/BE#** indicate which byte lanes are involved in the current data phase. A data phase may consist of a data transfer and wait cycles. The **C/BE#** output buffers must remain enabled (for both read and writes) from the first clock of the data phase through the end of the transaction. This ensures **C/BE#** are not left floating for long intervals.

The first data phase on a read transaction requires a turnaround cycle (enforced by the target via **TRDY#**). In this case the address is valid on clock 2 and then the master stops driving **AD**. The earliest the target can provide valid data is clock 4. The target must drive the **AD** lines following the turnaround cycle when **DEVSEL#** is asserted. Once enabled, the output buffers must stay enabled through the end of the transaction. (This ensures **AD** are not left floating for long intervals.)

A data phase completes when data is transferred, which occurs when both **IRDY#** and **TRDY#** are asserted on the same clock edge. (**TRDY#** cannot be driven until **DEVSEL#** is asserted.) When either is deasserted, a wait cycle is inserted and no data is transferred. As noted in the diagram, data is successfully transferred on clocks 4, 6, and 8, and wait cycles are inserted on clocks 3, 5, and 7. The first data phase completes in the minimum time for a read transaction. The second data phase is extended on clock 5 because **TRDY#** is deasserted. The last data phase is extended because **IRDY#** was deasserted on clock 7.

The master knows at clock 7 that the next data phase is the last. However, because the master is not ready to complete the last transfer (**IRDY#** is deasserted on clock 7), **FRAME#** stays asserted. Only when **IRDY#** is asserted can **FRAME#** be deasserted, which occurs on clock 8.

Write Transaction

Figure 2-6 illustrates a write transaction. The transaction starts when **FRAME#** is asserted for the first time which occurs on clock 2. A write transaction is similar to a read transaction except no turnaround cycle is required following the address phase because the master provides both address and data. Data phases work the same for both read and write transactions.

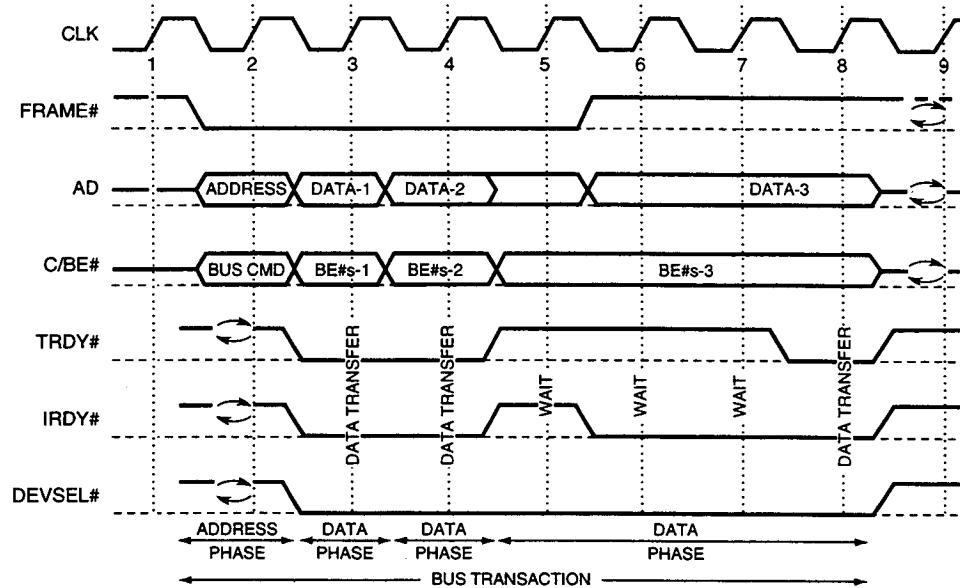


Figure 2-6. Basic Write Operation

In Figure 2-6, the first and second data phases complete with zero wait cycles. However, the third data phase has three wait cycles inserted by the target. Notice both agents insert a wait cycle on clock 5. **IRDY#** must be asserted when **FRAME#** is deasserted indicating the last data phase.

The data transfer was delayed by the master on clock 5 because **IRDY#** was deasserted. Although this allowed the master to delay data, it did not allow the byte enables to be delayed. The last data phase is signaled by the master on clock 6, but does not complete until clock 8.

Arbitration Signaling Protocol

An agent requests the bus by asserting its **REQ#**. Agents must only use **REQ#** to signal a true need to use the bus. An agent must never use **REQ#** to “park” itself on the bus. If bus parking is implemented, it is the arbiter that designates the default owner. When the arbiter determines an agent may use the bus, it asserts the agent’s **GNT#**.

The arbiter may deassert an agent’s **GNT#** on any clock. An agent must ensure its **GNT#** is asserted on the clock edge it wants to start a transaction. If **GNT#** is deasserted, the transaction must not proceed. Once asserted, **GNT#** may be deasserted according to the following rules.

1. If **GNT#** is deasserted and **FRAME#** is asserted, the bus transaction is valid and will continue.
2. One **GNT#** can be deasserted coincident with another **GNT#** being asserted if the bus is not in the IDLE state. Otherwise, a one clock delay is required between the deassertion of a **GNT#** and the assertion of the next **GNT#**, or else there may be contention on the **AD** lines and **PAR**.
3. While **FRAME#** is deasserted, **GNT#** may be deasserted at any time in order to service a higher priority¹ master, or in response to the associated **REQ#** being deasserted.

Figure 2-7 illustrates basic arbitration. Two agents are used to illustrate how an arbiter may alternate bus access.

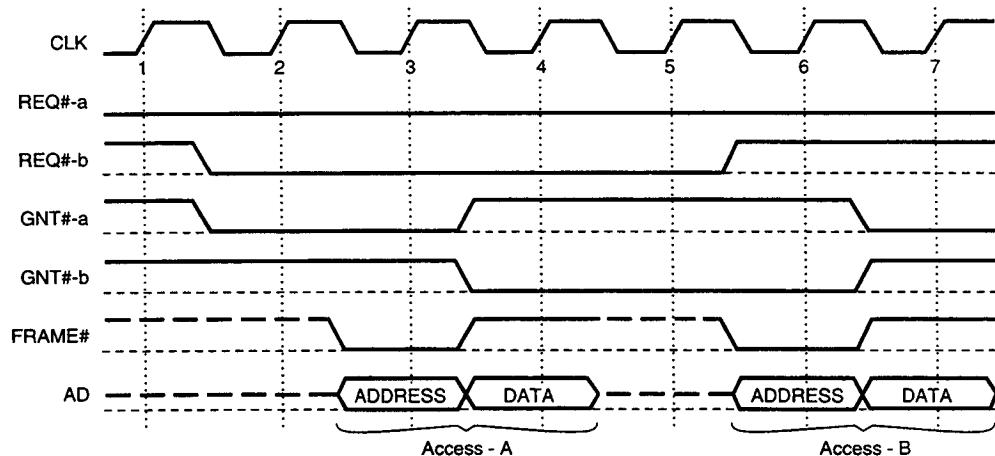


Figure 2-7. Basic Arbitration

REQ#-a is asserted prior to or at clock 1 to request use of the interface. Agent A is granted access to the bus because **GNT#-a** is asserted at clock 2. Agent A may start a transaction at clock 2 because **FRAME#** and **IRDY#** are deasserted and **GNT#-a** is asserted. Agent A’s transaction starts when **FRAME#** is asserted on clock 3. Since agent A desires to perform another transaction, it leaves **REQ#-a** asserted.

When **FRAME#** is asserted on clock 3, the arbiter determines agent B should go next and asserts **GNT#-b** and deasserts **GNT#-a** on clock 4.

¹ Higher priority here does not imply a fixed priority arbitration, but refers to the agent that would win arbitration at a given instant in time.

When agent A completes its transaction on clock 4, it relinquishes the bus. All PCI agents can determine the end of the current transaction when both **FRAME#** and **IRDY#** are deasserted. Agent B becomes the owner on clock 5 (because **FRAME#** and **IRDY#** are deasserted) and completes its transaction on clock 7.

Notice that **REQ-b** is deasserted and **FRAME#** is asserted on clock 6 indicating agent B requires only a single transaction. The arbiter grants the next transaction to agent A because its **REQ#** is still asserted.

The current owner of the bus keeps **REQ#** asserted when it requires additional transactions. If no other requests are asserted or the current master has highest priority, the arbiter continues to grant the bus to the current master.

GNT# gives an agent access to the bus for a single transaction. If an agent desires another access, it should continue to assert **REQ#**. An agent may deassert **REQ#** anytime, but the arbiter may interpret this to mean the agent no longer requires use of the bus and may deassert its **GNT#**. An agent should deassert **REQ#** in the same clock **FRAME#** is asserted if it only wants to do a single transaction. When a transaction is terminated by a target (**STOP#** asserted), the master must deassert its **REQ#** for a minimum of two PCI clocks, one being when the bus goes to the **IDLE** state (at the end of the transaction where **STOP#** was asserted) and either the clock before or the clock after the **IDLE** state. If the master intends to complete the transaction, it must reassert its **REQ#** following the deassertion of **REQ#** or a potential starvation condition may occur. If the master does not intend to complete (because it was prefetching or a higher priority internal request needs to be serviced), the agent asserts **REQ#** whenever it needs to use the interface again. This allows another agent to use the interface while the previous target prepares for the next access.

The arbiter can assume the current master is “broken” if it has not started an access after its **GNT#** has been asserted (its **REQ#** is also asserted), and the bus is **IDLE** for 16 PCI clocks. However, the arbiter may remove **GNT#** at any time to service a higher priority agent.

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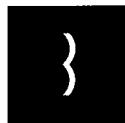
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