

EE 109 Homework 6 State Machine Design

Name: _____

Due: See Blackboard

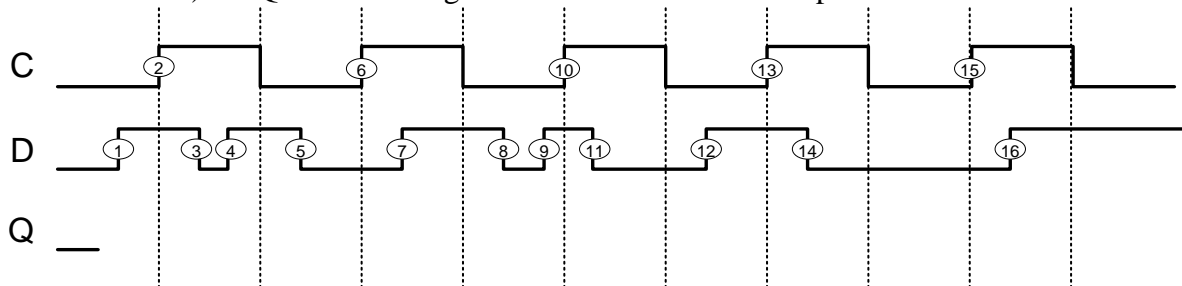
Score: _____

Blackboard ONLY Submission.

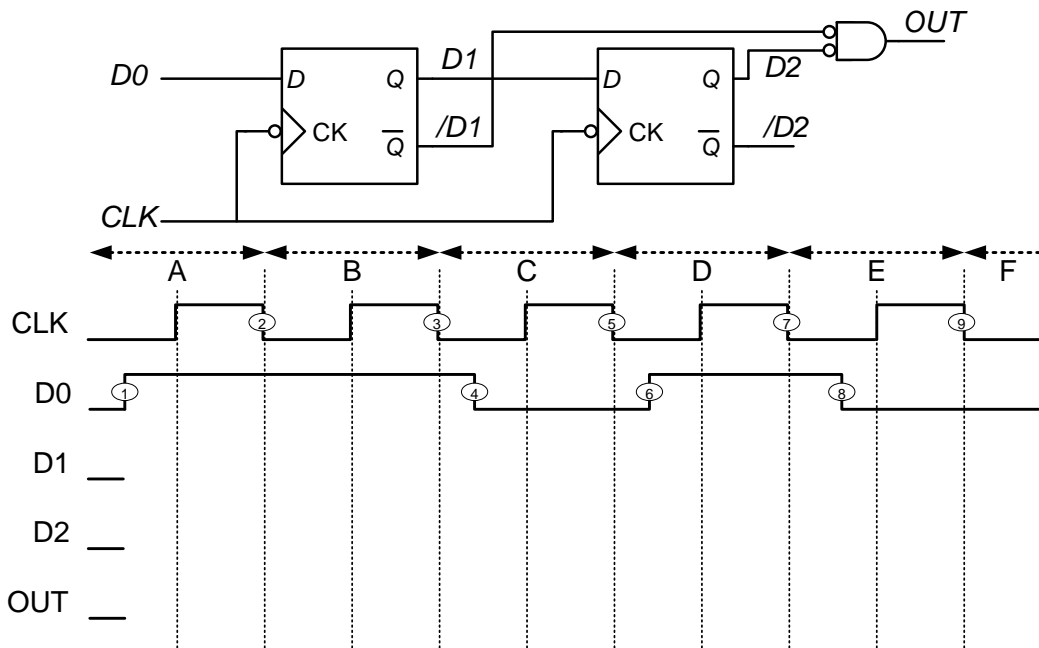
While the Blackboard submission may not require you to go through all the design steps (such as drawing out state diagrams or circuits, you should make sure to go through all the steps on your own.

HW 6a Blackboard Form

1. [BB] (8 pts.) Complete the following waveform for a D-Latch with active-high clock (Remember latches are level sensitive). To enter your answer online, select which transitions of the clock, C, or the D-input (indicated by a timestamp) will cause Q to toggle (i.e. change from 0 to 1 or 1 to 0). If Q doesn't change do not enter that timestamp as an answer.

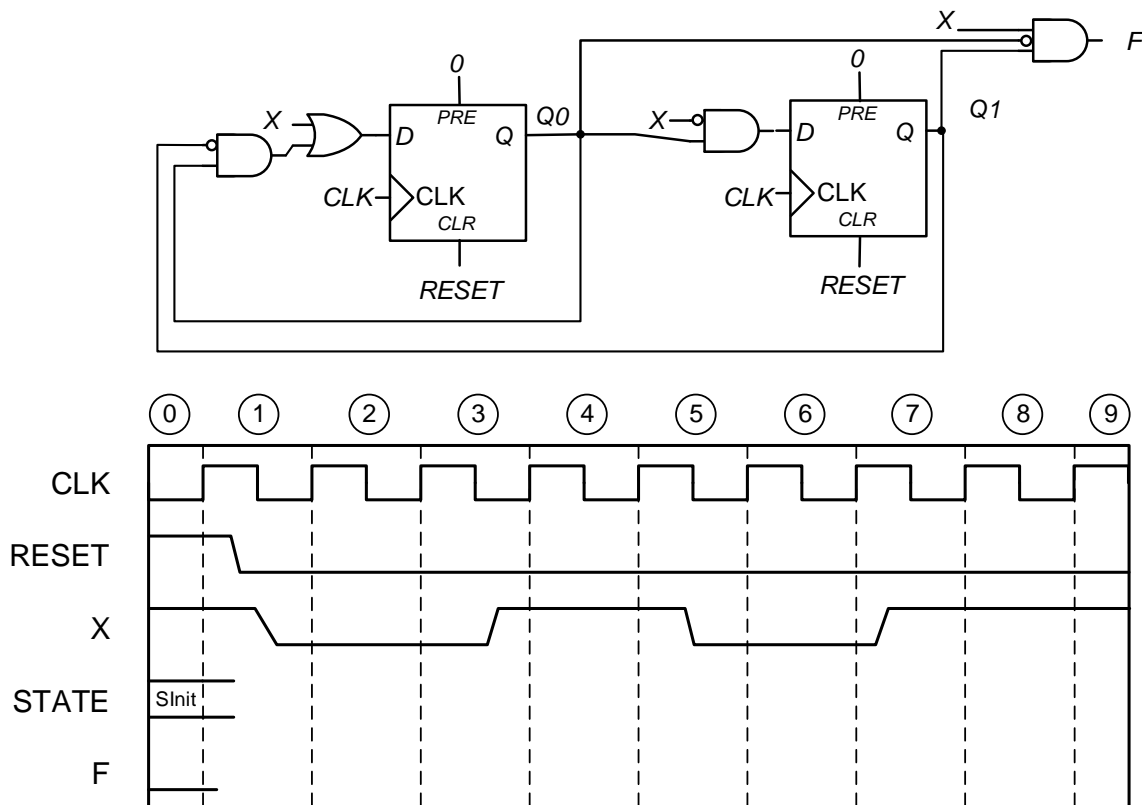


2. [BB] (15 pts.) Complete the waveform for the following design involving two negative edge-triggered D flip-flops. Note: OUT is a combinational logic function of the FF outputs. Note: Combinational logic gates are UNAFFECTED by the clock (only FF's use the clock signal). Thus, a change in the inputs to logic gates causes an immediate change (after a small propagation delay) in the outputs. For D1 and D2 indicate their value during the middle of clock cycles A through F. For OUT indicate which timestamps of D or CLK will cause (either directly or via D1 and D2) OUT to toggle (from 0 to 1 or 1 to 0)



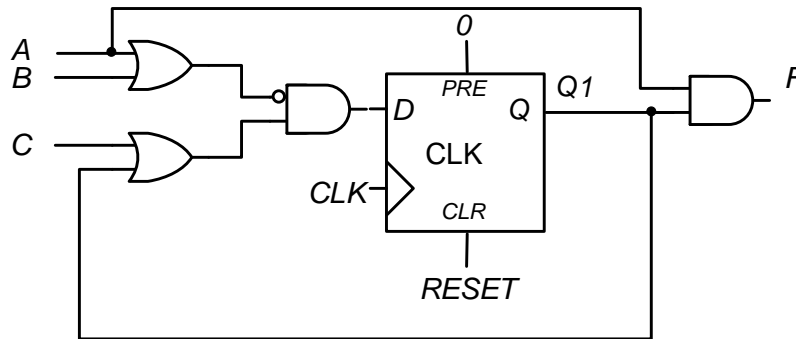
3. **[BB] (12 pts.)** Analyze the sequential circuit below that implements a 4-bit sequence checker. Find and identify what sequence this circuit is checking for (i.e. the shortest sequence of X that will make $F=1$) by complete the waveform (Notice the state machine is in reset at the first clock edge and will not respond to X). **Enter the sequence being checked and waveform values in the Blackboard submission.**

Q1,Q0	State Name
00	SInit
01	SA
10	SC
11	SB



Look at the state transitions and what input sequence leads to the output being true, we can say this circuit is checking for the sequence: _____

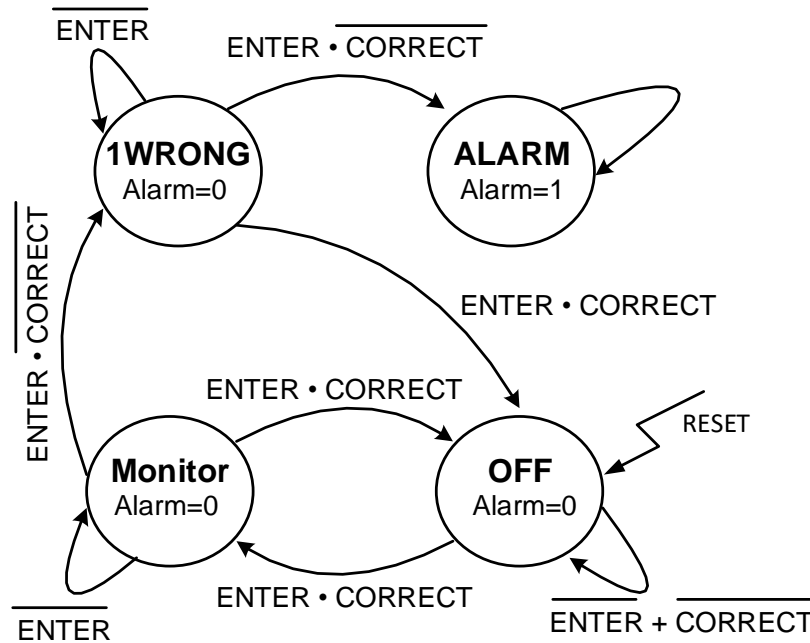
4. [BB] (5 pts.) Study the following sequential circuit and answer the questions below.



- How many states will there be in the state diagram for this circuit?
- Is this a Mealy or Moore Machine.
- When we found the state diagram, what would be the maximum number of transition arrows originating from a state?
- If A is held constant at '1' for more than one clock, can the output, F, be 1?

HW 6b Blackboard Form

5. [BB] (20 pts.) Below is a state diagram for a simple, home alarm system. To turn the alarm system on or off, the user has to enter a code correctly and then hit the enter key. If the alarm system is on (in the monitor state), the user can deactivate it by entering the code correctly. If, however, they enter it incorrectly two times in a row, then the user may actually be an intruder, so the system should enter the alarm state and stay there forever (until reset). Design a state machine to implement this diagram. Use D flip-flops and for state assignment OFF = 00, MONITOR = 01, 1WRONG = 10, and ALARM = 11. Be sure to implement the initial state using the /RESET signal.
- Enter your excitation (D-input) equations on Blackboard
 - Enter your output equations on Blackboard
 - Show the initial state (RESET) configuration on Blackboard.



6. [BB] (20 pts.) Design a state machine that compares two unsigned binary numbers, A and B, input serially (1-bit at a time for each of A and B) starting with the LSB and working up to more significant bits. You need not worry about how many bits the numbers are, just keeping checking the A and B inputs. You should have three states: EQ, LT, and GT with three corresponding outputs: EQ, LT, GT which should be asserted when in the corresponding state.

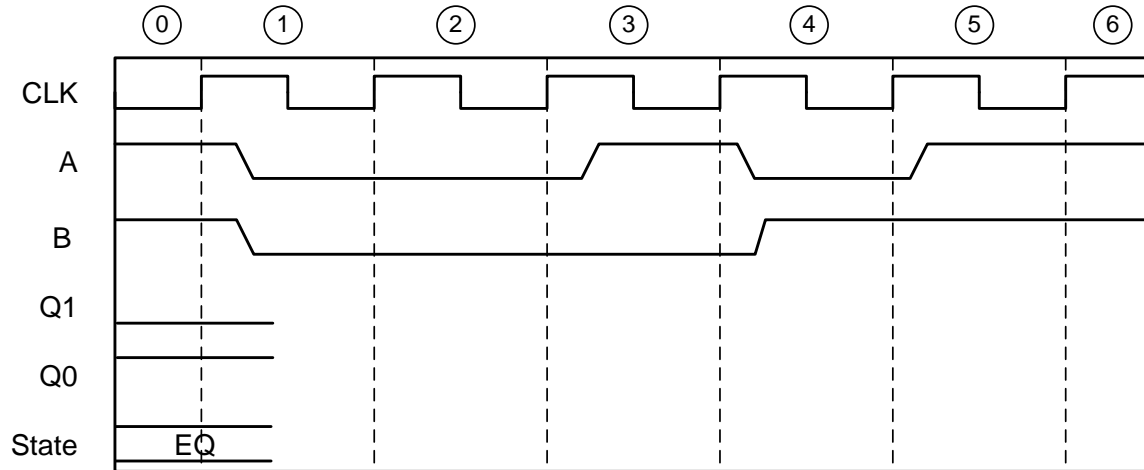
Hint: As an example, think about the numbers: $A=1010$ and $B=1100$. If you started at the LSB's (0 and 0) you would say they are equal. Once you looked at the second bit 1 and 0 you would say $A > B$, but when you looked at the next bit (0 and 1), what would you say is the relationship?

Design the system using positive-edge triggered D Flip-flops (w/ preset and clear inputs). Use two state variables, Q1 and Q0, with the state assignment GT=00, EQ=01, LT=11, (10 = Don't-care).

Enter your excitation (D-input) equations and output equations on Blackboard. Use the preset and clear inputs along with the signal RESET to initialize the state machine to the initial state EQ and enter your configuration on Blackboard.

- Enter your (D-input) excitation equations on Blackboard
- Enter your output equations on Blackboard
- Show the initial state (RESET) configuration on Blackboard.
- Show the waveform of the operation of Q[2:0] on Blackboard.

Waveform for problem 0 (Note: Q1 is LOW and Q0 is HIGH initially)



7. **[BB] (20 pts.)** Design a 3-bit Down Counter (i.e. counting down: 111,110,101,100,011,010,001,000,111...). This counter has one input DOWN. The circuit should not count (it should stay at it's current value) if DOWN=0. The circuit should count down if DOWN=1. In this case, the outputs are just the state values: Q2, Q1, Q0 which form the 3-bit count value.

Draw a state diagram of this machine. On power on (reset) the counter should start at Q2,Q1,Q0 = 111

Using positive-edge triggered D-Flip-Flops implement the circuit (show all steps.) Find the next-state equations for the flip-flop inputs (excitation variables). Use the state variables Q2, Q1 and Q0.

- Enter your excitation (D-input) equations on Blackboard
- Show the initial state (RESET) configuration on Blackboard.
- Show the waveform of the operation of Q[2:0] on Blackboard.

Waveform for problem 7. (Note: Q2, Q1, and Q0 are HIGH initially)

