Shenzhen Youritech Technology Co.,Ltd.

AMOLED MODULE SPECIFICATION

Customer: _____

Module No.: ET055FH06-GT

For Customer's Acceptance:

Approved by	Comment

Approved by	Checked by	Prepared by
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Table of Contents

Record of Revision

Rev.	Date	Description	Editor
1.0	2022-5-04	First release	Kanglin.Zhong

1 General Specifications

No.	Item	Specification	Remark
1	OLED Size	5.44 inch (Diagonal)	
2	Driver Element	AMOLED active matrix	
3	Resolution	1080 (RGB) ×1920	
4	Display Mode	AMOLED	
5	Pixel Pitch(mm)	0.0314(H) × 0.0628 (V)	
6	Display Colors	16.7M	
7	Surface Treatment	--	
8	Color Arrangement	Rendering	
9	Interface	MIPI	
10	Viewing Direction	All	
11	Gray Scale Inversion Direction	/	Note 1
12	Outline Dimension (mm)	81.0 (W) ×138.2 (H) × 1.67 (T)	
13	Active Area (mm)	67.824 (W) × 120.58 (H)	
14	Touch Screen	On-cell with Cover Lens	
15	Display Driver IC	RM67199	
16	Touch Driver IC	GT9886	

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180°shift.

Note 2: RoHS compliant.

2 Pin Assignment

2.1 OLED Pin assignment

PIN	Symbol	I/O	Description	Remark
1	GND1	P	Ground	
2	GND2	P	Ground	
3	GND3	P	Ground	
4	VBAT1	P	power supply (4.2V)	
5	VBAT2	P	power supply (4.2V)	
6	VBAT3	P	power supply (4.2V)	
7	VBAT4	P	power supply (4.2V)	
8	VBAT5	P	power supply (4.2V)	
9	GND4	P	Ground	
10	VPP	--	Power supply for OTP. Float it for normal operation.	
11	NC1	--	NC	
12	GND5	P	Ground	
13	D3P	I	MIPI DSI differential data pair (Data lane 3)	
14	D3N	I	MIPI DSI differential data pair (Data lane 3)	
15	GND6	P	Ground	
16	D0P	I/O	MIPI DSI differential data pair (Data lane 0)	
17	D0N	I/O	MIPI DSI differential data pair (Data lane 0)	
18	GND7	P	Ground	
19	CLKP	I	MIPI DSI differential clock pair	
20	CLKN	I	MIPI DSI differential clock pair	
21	GND8	P	Ground	
22	D1P	I	MIPI DSI differential data pair (Data lane 1)	
23	D1N	I	MIPI DSI differential data pair (Data lane 1)	
24	GND9	P	Ground	
25	D2P	I	MIPI DSI differential data pair (Data lane 2)	
26	D2N	I	MIPI DSI differential data pair (Data lane 2)	
27	GND10	P	Ground	
28	RESX	I	Reset Signal ,Active Low.	
29	VDDIO	P	Digital circuit I/O power supply	
30	VCI	P	Power supply for Analog circuit.	
31	TE	O	Tearing effect.	

32	GND11	P	Ground	
33	TSP_AVDD_3.3V	P	Touch IC analog power supply (3.3V)	
34	TSP_DVDD_1.8V	P	Touch IC Digital circuit I/O power supply	
35	TSP_SDA	I/O	Touch IIC Data signal	
36	TSP_SCL	I	Touch IIC Clock signal	
37	TSP_RESET	I	Touch Reset Signal	
38	TSP_ATTN	I	Touch Interrupt(1.8V)	
39	ID	--	ID Signal. (not connect)	

I---Input, O---Output, P--- Power/Ground

3 Absolute Maximum Ratings

Ta = 25℃

Item	Symbol	Min.	Max.	Unit	Remark
Power Voltage	VBAT	2.5	5.0	V	
	VCI	-0.30	+5.5	V	
	VDDIO	-0.30	+5.5	V	
	TSP_AVDD_3.3V	-0.30	+4.2	V	
	TSP_DVDD_1.8V	-0.30	+4.2	V	
Operating Temperature	Top	-20.0	70.0	℃	
Storage Temperature	T_{st}	-30.0	80.0	℃	
Operating and Storage Humidity	H_{stg}	10%	90%	%(RH)	

4. Electrical Characteristics

4.1 Recommended Operating Condition

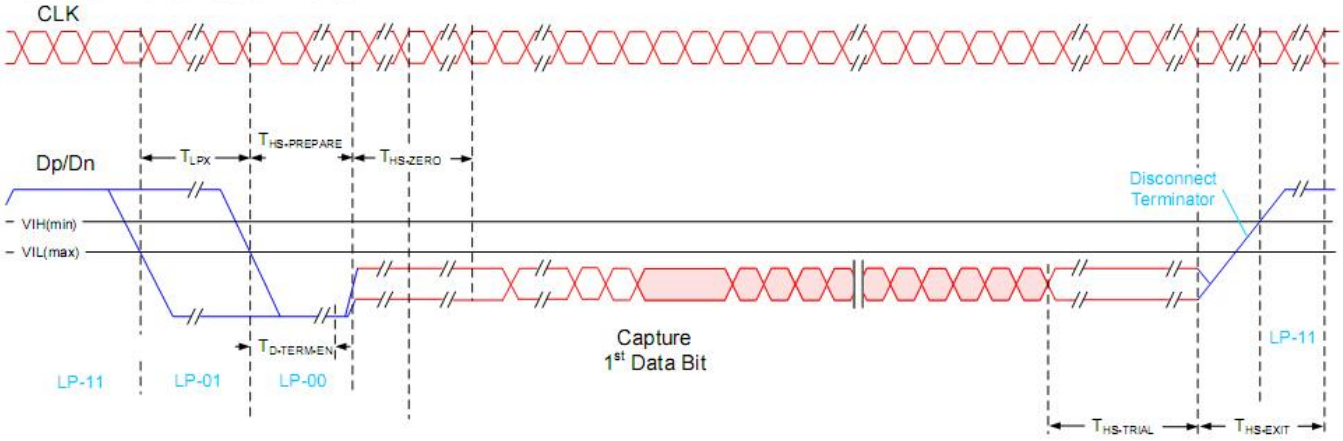
VCI=3.3V，GND=0V，Ta = 25℃

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Voltage		VBAT	2.9	4.2	4.5	V	
Digital supply Voltage		VDDIO	1.65	1.8	3.3	V	
Analog supply Voltage		VCI	2.5	2.8	3.3	V	
TP Power		TSP_AVDD_3.3	2.7	3.0	3.4	V	
		TSP_DVDD_1.8V	1.65	1.8	3.3	V	
Input Signal Voltage	Low Level	V_{IL}	0	-	0.3 x VDDIO	V	
	High Level	V_{IH}	0.7 x VDDIO	-	VDDIO	V	
Current of Power Voltage		VBAT	-	205	380	mA	350 nits @Gray 255
Current of digital supply voltage		I_{VDDIO}	-	-	10	mA	
Current of analog supply voltage		I_{VCI}	-	50	60	mA	VCI=3.3V, @Gray 255

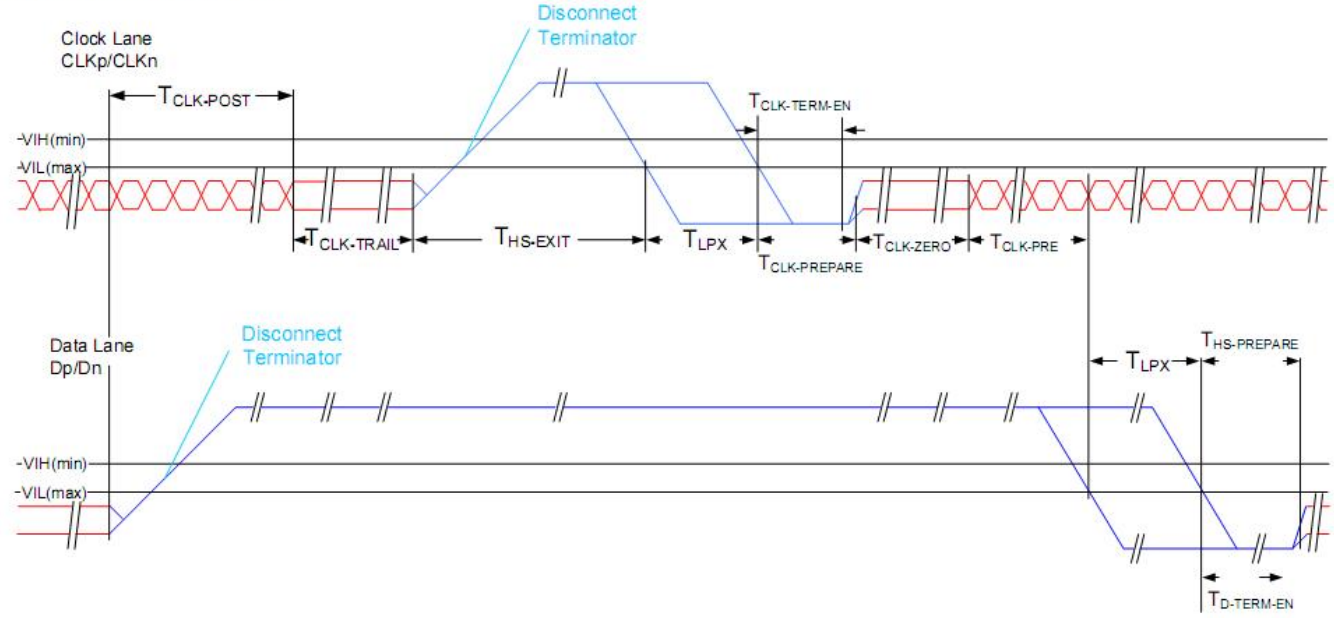
5 Timing Chart

5.1 DSI Interface Timing Characteristics

HS Data Transmission Burst

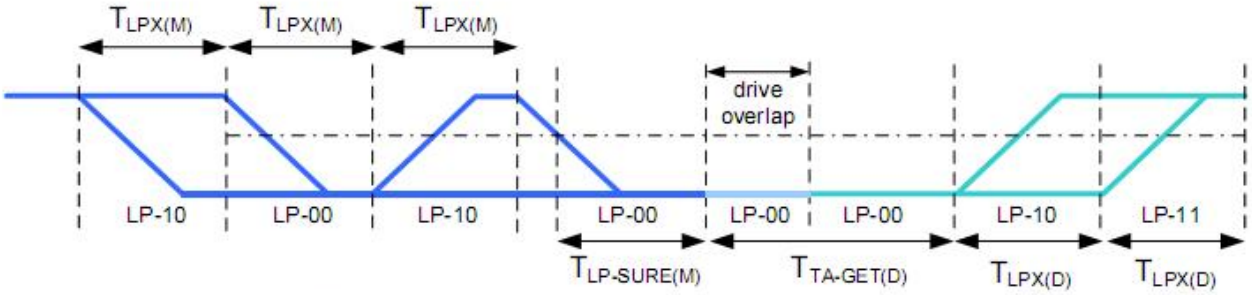


HS clock transmission

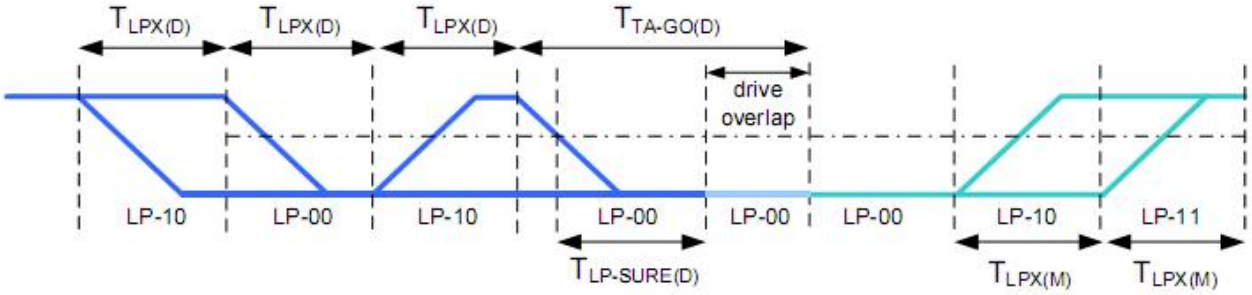


Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	**300**			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	**$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.**	**145ns + 10*UI**			**ns**
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns



Bus turnaround (BAT) from MPU to display module timing



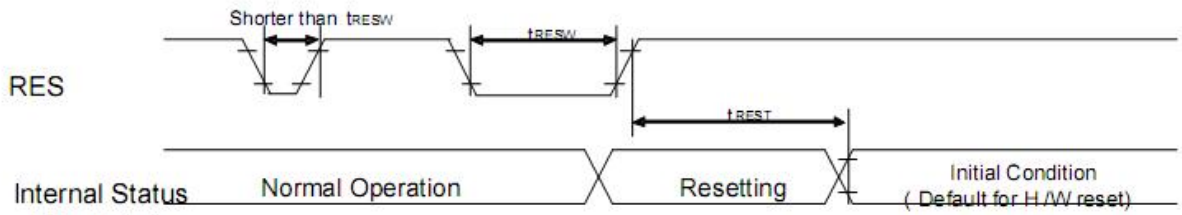
Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

NOTE:
1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

5.2 Reset Input timing



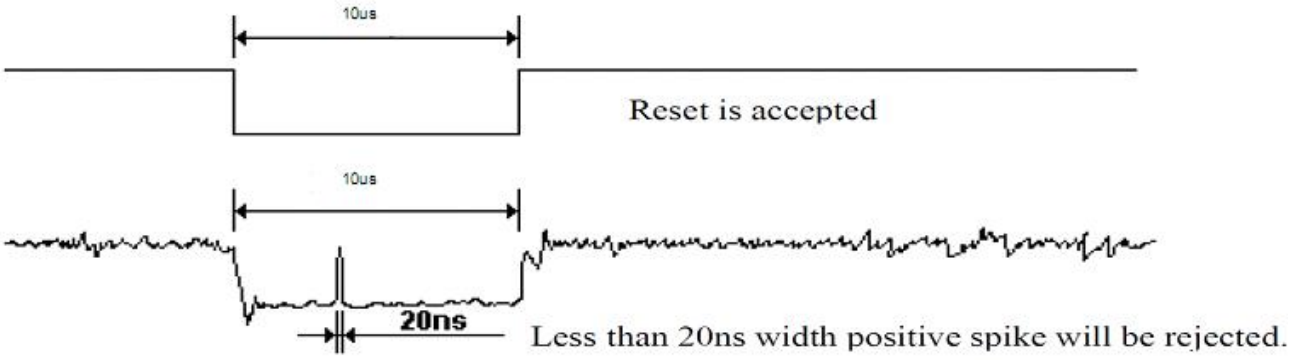
Reset input timing:
IOVCC=1.65 to 3.6V, VDD=2.5 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

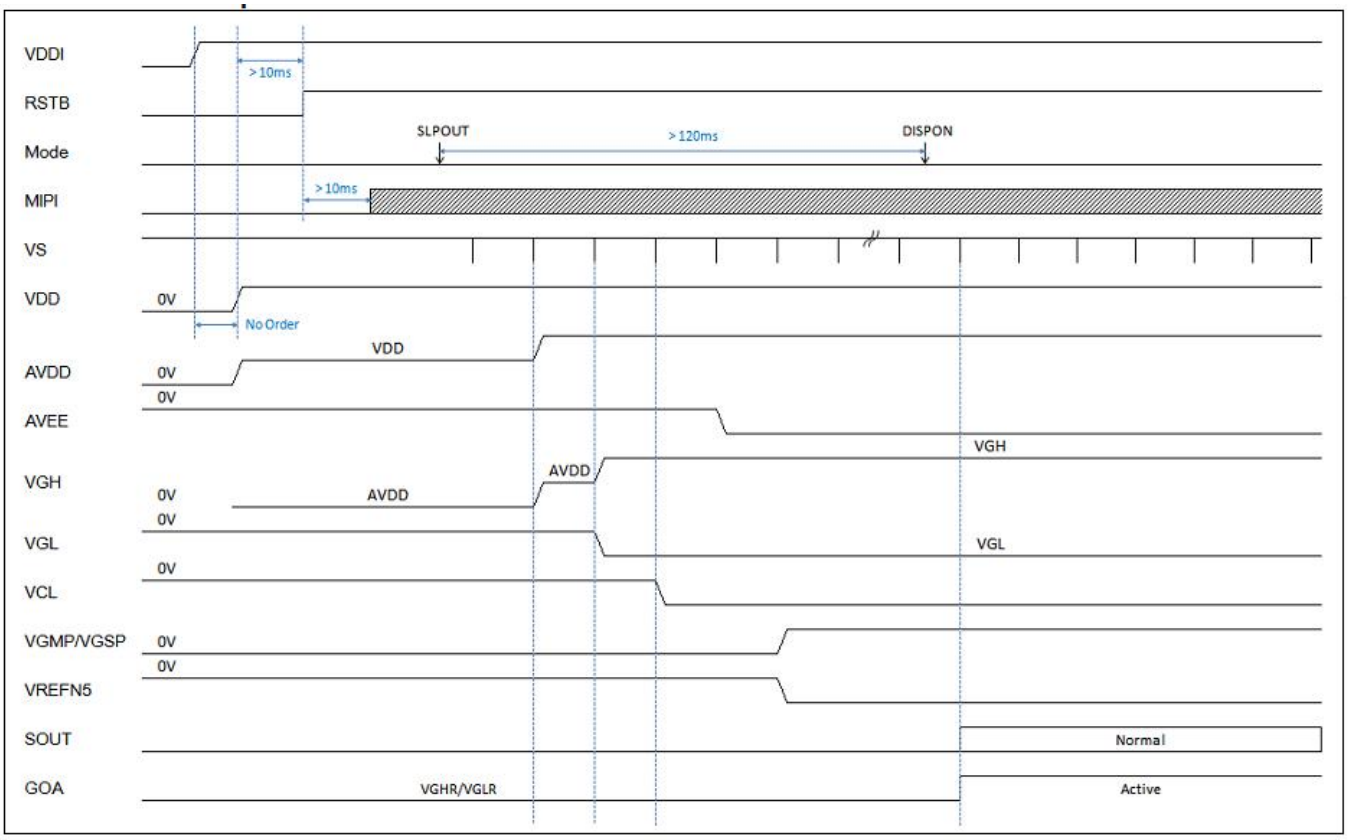
RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

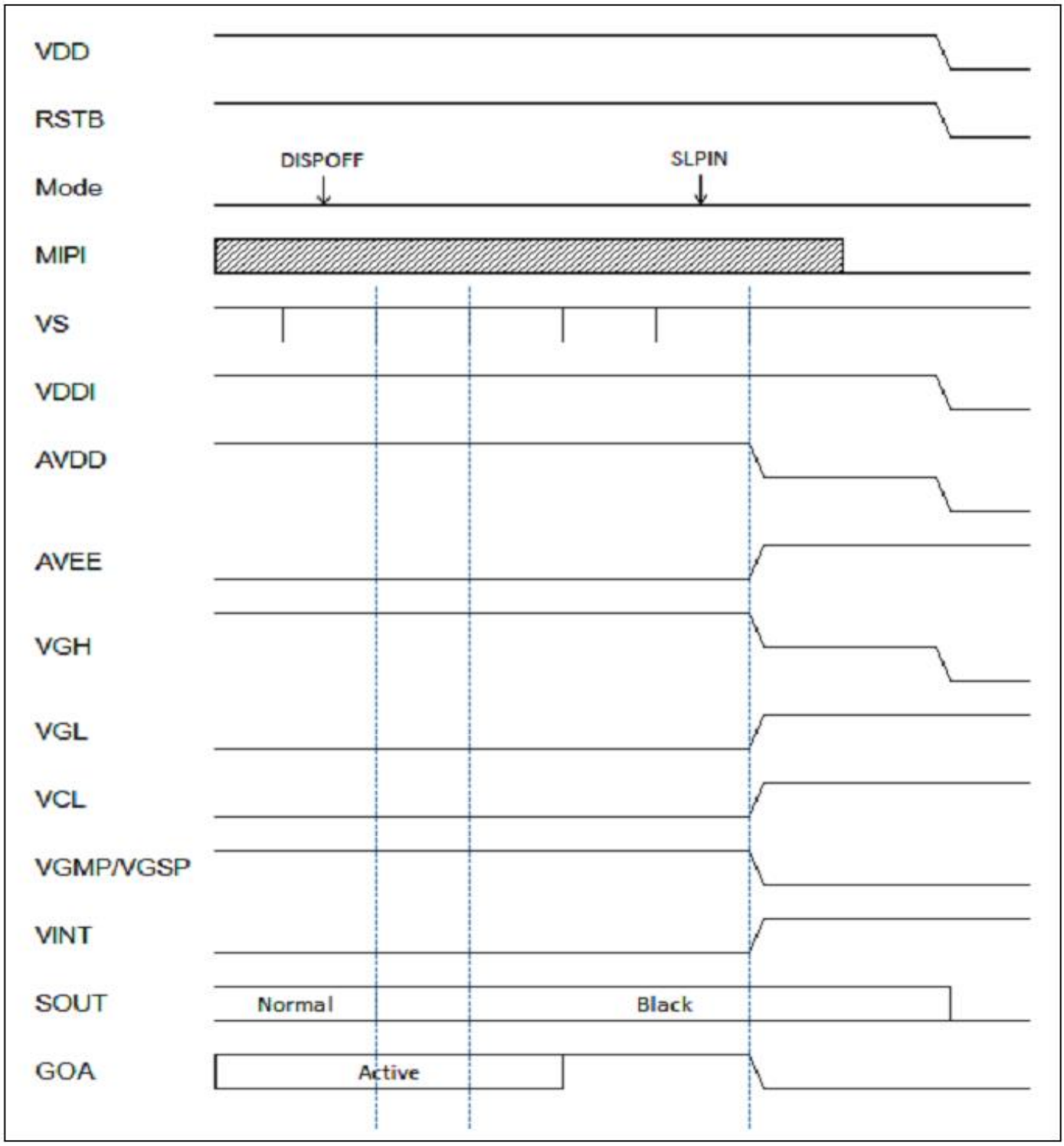


Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.3 Power On Timing



5.4 Power Off Timing



6 Optical Characteristics

Ta=25℃

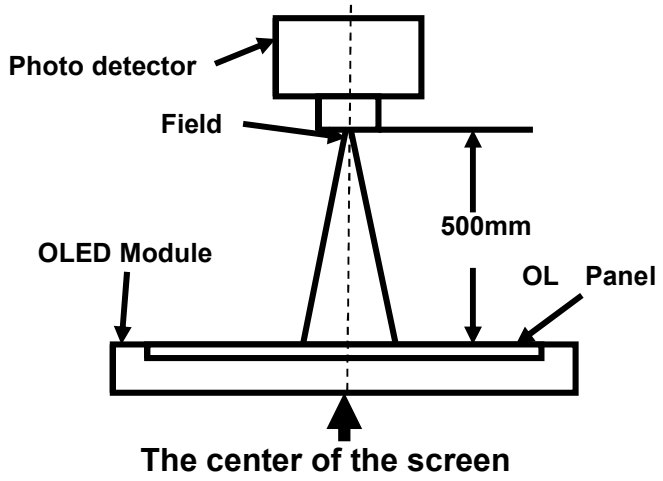
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
View Angles		θT	CR≧1000	80	-	-	Degree	Note 2
		θB		80	-	-		
		θL		80	-	-		
		θR		80	-	-		
Contrast Ratio		CR	θ=0°	60000	-	-		Note1 Note3
Response Time		T_{ON}	25℃	-	-	2	ms	Note1 Note4
		T_{OFF}						
Chromaticity	White	x	Backlight is on	0.275	0.295	0.315		Note1 Note5
		y		0.285	0.305	0.325		
	Red	x		0.66	0.69	0.72		
		y		0.28	0.31	0.34		
	Green	x		0.195	0.235	0.275		
		y		0.68	0.72	0.760		
	Blue	x		0.113	0.143	0.173		
		y		0.014	0.044	0.074		
Uniformity		U		75	-	-	%	Note1 Note6
NTSC				90	109	-	%	Note 5
Luminance		L		315	350	385	cd/m^2	Note1 Note7

Test Conditions:

1. The ambient temperature is 25±3℃.humidity is 65±20%RH, Dark Room.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

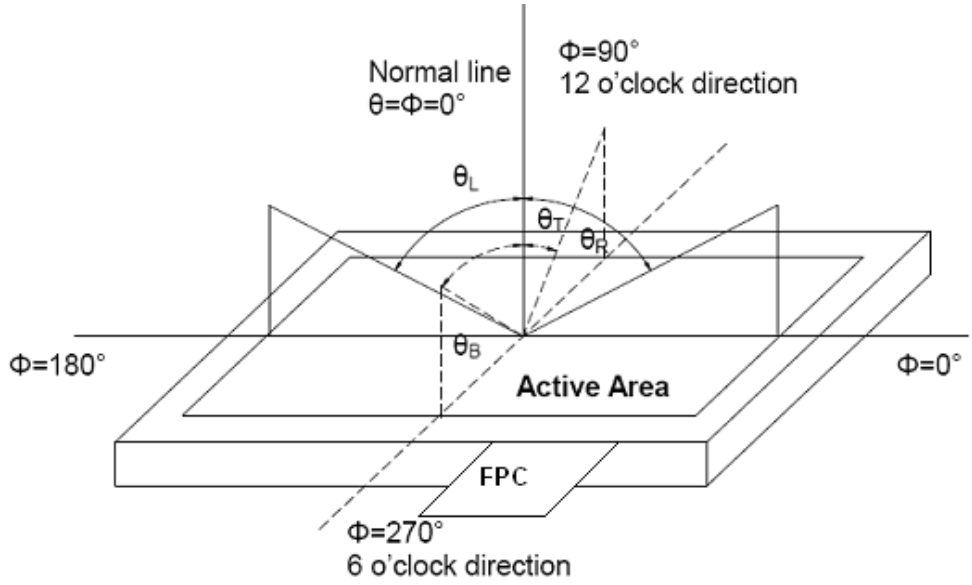
Properties are measured at the center point of the OLED screen. All input terminals OLED panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.

Viewing angle is measured at the center point of the OLED by CONOSCOPE(ergo-80)。



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when OLED is on the "White" state}}{\text{Luminance measured when OLED is on the "Black" state}}$$

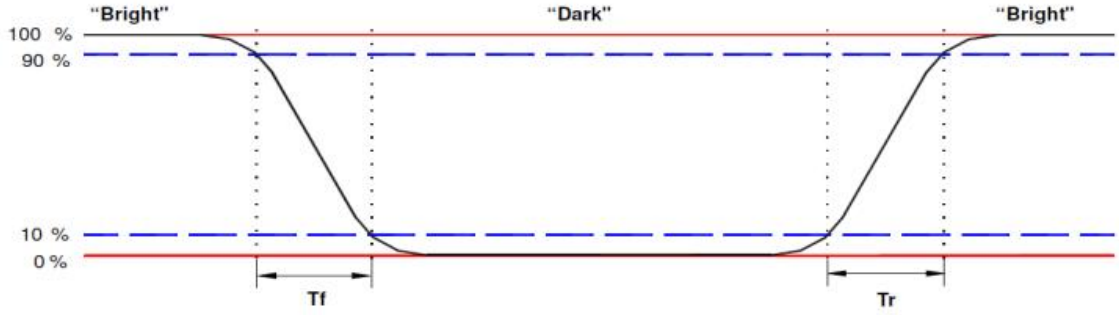
"White state ": The state is that the OLED should drive by Vwhite.

"Black state": The state is that the OLED should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of response time

The response time is defined as the OLED optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

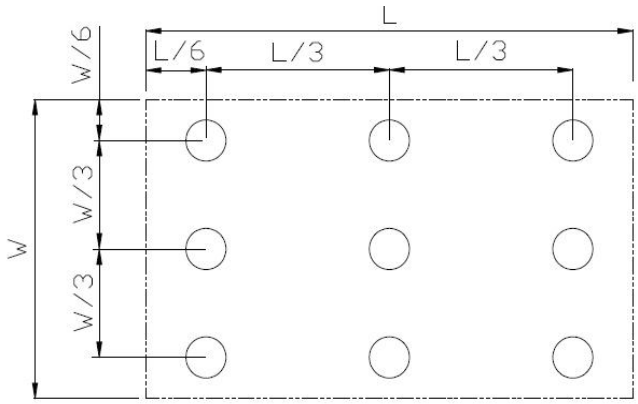
Color coordinates measured at center point of OLED.

Note 6: Definition of luminance uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of luminance:

Measure the luminance of white state at center point.

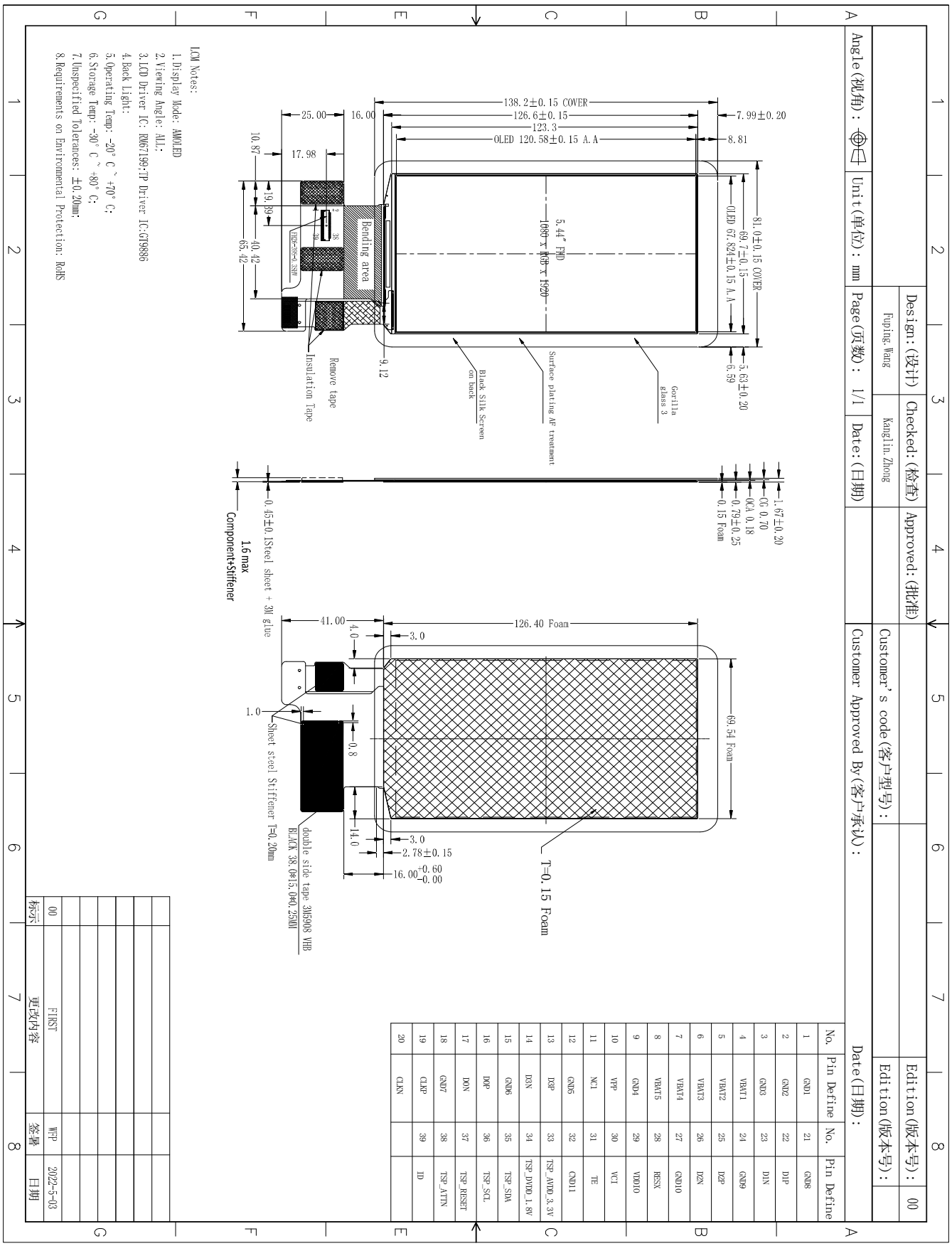
7 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts = +70℃, 120 hours	No abnormalities in functions
2	Low Temperature Operation	Ta = -20℃, 120 hours	No abnormalities in functions
3	High Temperature Storage	Ta = +85℃, 120 hours	No abnormalities in functions
4	Low Temperature Storage	Ta = -40℃, 120 hours	No abnormalities in functions
5	Storage at High Temperature and Humidity	Ta = +60℃, 93% RH max,120hours	No abnormalities in functions
6	Thermal Shock (non-operating)	-40℃ 30 min~ +85℃ 30 min, Change time: 0.5 hour □ 5 min □ 0.5 hour.32 Cycle	Start with cold temperature, End with high temperature,
7	ESD	C=150pF, R=330Ω,5point/panel Air: ±6Kv, 20times; Contact:±4Kv,20times (Environment:15℃~35℃, 30%~60%.86Kpa~106Kpa)	No abnormalities in functions

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of samples.

8 Mechanical Drawing



9 Precautions for Use of OLED Modules

Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.3 The polarizer covering the display surface of the OLED module is soft and easily scratched. Handle this polarizer carefully.

9.1.4 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

9.1.6 Do not attempt to disassemble the OLED Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

9.1.8.1 Be sure to ground the body when handling the OLED Modules.

9.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

9.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

9.1.8.4 The OLED Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

Storage Precautions

9.2.1 When storing the OLED modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The OLED modules should be stored under the storage temperature range. If the OLED modules will be stored for a long time, the recommend condition is: Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

9.2.3 The OLED modules should be stored in the room without acid, alkali and harmful gas.

Transportation Precautions

9.3.1 The OLED modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.