Radxa CM5 Connectors x 3

CONNECTOR1

DF40C-100DS-0.4V(51)

CONNECTOR2

DF40C-100DS-0.4V(51)

DF40C-100DS-0.4V(51)
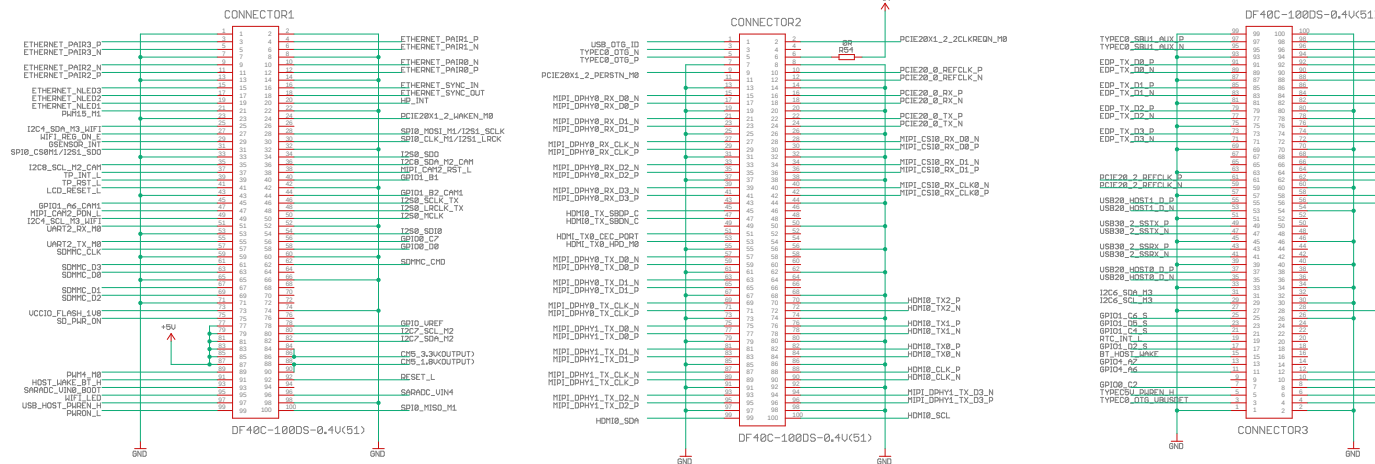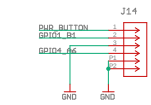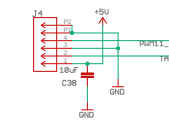
CONNECTOR3

Check SuperSpeed USB 3.0 functionality. Dimensions of 3rd connector measured & OK.
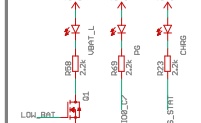
VOL/PWR Switch

J14

Self explanatory, really.

Fan

J4

TACH (PWM15_M1) and PWM pins to respective PWM pins.

LEDs

Indicates successful FET switch, charge status & low VBAT.

Schmitt Trigger/Buffers/Shifters

U8 — UP3204QQFN14_3.5X3.5_UM3204_USC-L

U9 — UP3204QQFN14_3.5X3.5_UM3204_USC-L

U10 — UP3204QQFN14_3.5X3.5_UM3204_USC-L

U13 — UP3204QQFN14_3.5X3.5_UM3204_USC-L

Real-Time-Clock (RTC)

ECS-.327-12.5-12R-TR
32.768 kHz

TSIC_306_SOP-8

Checked battery polarity. OK
I2C pins already have pull-ups on CM5 board.

J11

I2S Audio – WM8960

WM8960

ECS-3225MV-240-BN-TR
24MHz

I2S1

I2S Logic 3V3 - GROUNDED 3V3
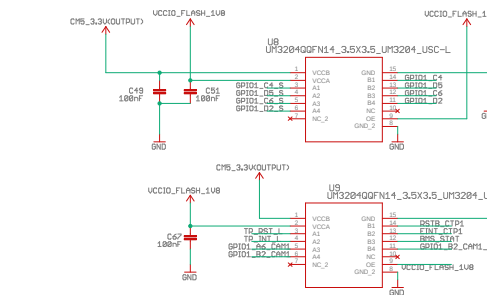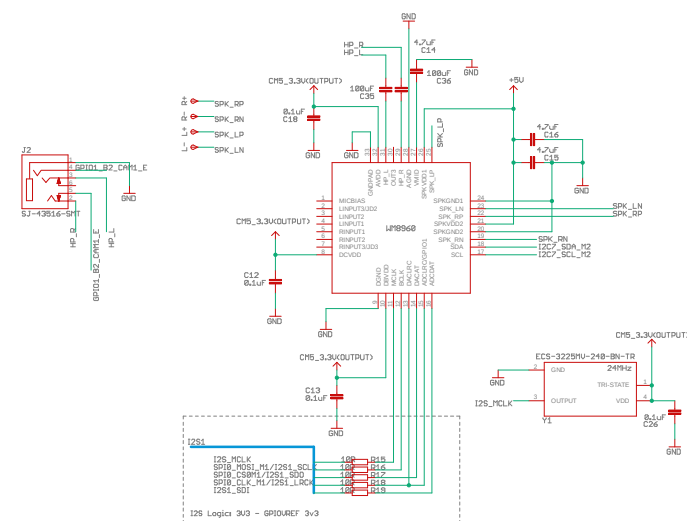
To check I2S bus pins runs on 3V3 logic on CM5.

Testpads
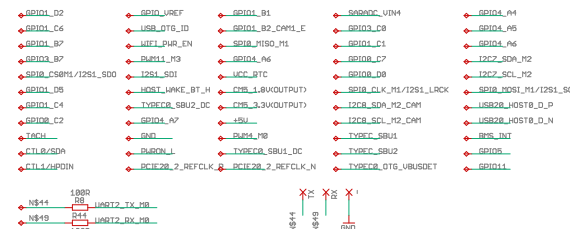
Make sure all pins are connected to the CM5 Radxa B2B mezzanines.

SD Interface

SDIO1

Note:
GPIO4_D0 to D5
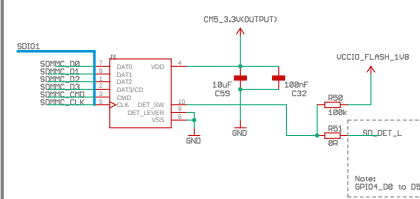
No need for logic switch. OK!

ATtiny84/SysCon

ATtiny84 Programming Pins
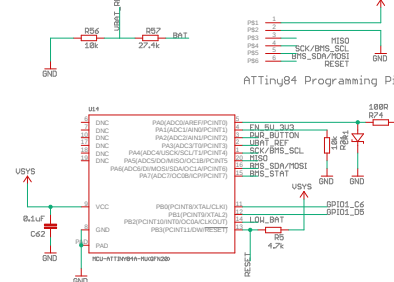
Boots up system and drives various GPIOs to shutdown, sleep and wake.

RP2040 Passthrough FFCs

J6

J12
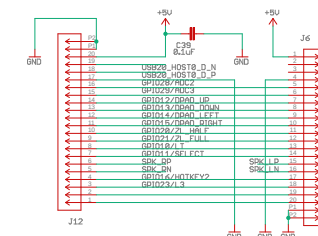
Working. To hope analog speakers don't cause any intereference.
Kept away from USB data.

>CNAME
RetroLiteCM5IOFinal_v2
10/06/2025 5:56 PM
Sheet: 1/2   Rev:>CREVISION

USB-C DRP Connector

rockchip,dp-lane-mux = < 3 2 0 1 >;

TUSB546 High Speed Mux

Note: Ensure jumper is correctly populated for I2C/GPIO mode.

Ben to check if USB 3.0 functionality correctly works with Radxa CM5 IO board.

TUSB546-DCIRNQT

U23

CTL1: Controls whether DP is enabled or not. High is enabled, low is disabled.

CTL0: Controls whether USB 3.1 is enabled (high). If CTL0 low and CTL1 is high, then 4 lanes of DisplayPort are enabled. If CTL0 is high and CTL1 is also high, then USB 3.1 and 2-lane DP is enabled.

```
&usbdp_phy0 {
    status = "okay";
    rockchip,dp-lane-mux = < 3 2 0 1 >;
};
```

HDMI 2.1

HDMI Type-C Mini Port

ESD Protection

DDC/CEC/HPD

Radxa have removed logic shifting on I2C EDID pins since X2.2. What is pin 14 used for? HEAC+

TPS65987D USB Type-C Controller

ADCIN1 BP_Nakid/Safe
ADCIN2 8180 I2C Address

U21

TPS65987DDHRSHR

W25X05 Programming Pins

W25X05 SPI Mode

Complete & verified (negotiating both a USB-C PD source/sink contract & works with DisplayPort Alternate Mode.

MIPI 5.5 Inch Display

KD055HDFIA001-C001A FFC Connector   J9

TPS61160A Backlight Driver

U16 TPS61160ADRVT

Inverse PWM polarity

GT911 FFC Connector   J10

Display KD055HDFIA001-C001A   MIPI_DSI

Done!

PCIe 2.0 (WiFi M.2 E-Slot)

J8

MDT320DC1001

For WiFi only (will not work with M.2 SSDs!)

Power Path Management

VBUS Max Input 17V

BQ24292i

Mates with J13. Check battery polarity!

5V 3A Boost Regulator (TPS61235)

3V3 Buck Regulator (WiFi)

U12 SY8089AAAC SY8089AAAC_SGY-L

I2C Only Fuel Gauge (MAX17055)

U11 MAX17055ETB+T

BQ24292i controls VBUS power path and charges lithium ion cells. MAX17055 is used for battery management. 5V 3A boost regulator to power CM5. 3v3 buck is to power the WiFi PCIe card. Check GPIO int pin for MAX17055 & also I2C logic.

Order Notes

- Order with JLC06081H-2116 (Standard) Stackup
- 0.8mm thickness
- ENIG plating
- Thanks to GinKage for all of his hard work :)

Imped	Signal Layer	Top Ref	Bot Ref	Width	Spacing
100Ω	L1	–	L2	0.1422mm	0.2032mm
100Ω	L4	L3	L5	0.1128mm	0.2032mm
100Ω	L6	L5	–	0.1422mm	0.2032mm
90Ω	L1	–	L2	0.1245mm	0.1016mm
90Ω	L4	L3	L5	0.1064mm	0.1016mm
90Ω	L6	L5	–	0.1245mm	0.1016mm

Checklist

- Change volume GPIOs
- Check USB3.0 pinouts w/ multimeter
- Check DP pinouts w/ multimeter
- Check USB-C MUX pins for DP
- Wait for GinKage on sleep modes

Bus	Imped	Signal Layer
MIPI_DSI	100Ω	L1
HDMI2.0	100Ω	L4
USB2.0	90Ω	L4 & L1
USB3.0	90Ω	L4 & L1
DP1.4	100Ω	L4 & L1
PCIE2.0	90Ω	L6