

# Voltage Integrator Calculation

## Definitions and Equations - Multislope Continuous Runup with periodic ADC measurements

```
In[1]:= voutIn = -  $\frac{1}{r_{Mes} * C_{int}}$  * vin * Δtint;  
In[2]:= voutRefPos = -  $\frac{1}{r_{RefPos} * C_{int}}$  * vrefPos * ΔtrefPos;  
In[3]:= voutRefNeg = -  $\frac{1}{r_{RefNeg} * C_{int}}$  * vrefNeg * ΔtrefNeg;  
In[4]:= ΔtrefPos = tPos * nPos;  
In[5]:= ΔtrefNeg = tNeg * nNeg;
```

Solve for the unkown input voltage  $V_{in}$  we want to measure:

```
In[6]:= Solve[voutIn + voutRefPos + voutRefNeg == ΔvADC, vin] // FullSimplify  
Out[6]= { {vin → - (rMes (nNeg rRefPos tNeg vrefNeg + rRefNeg (nPos tPos vrefPos + Cint rRefPos ΔvADC)) ) / (rRefNeg rRefPos Δtint) } }
```

## Component value calculations and some error calculation

Design choices:

```
In[7]:= iinFS = 0.0005; vinFS = 2.5; vrefPos = 5.0; vrefNeg = -5.0; vsat = 13;  
In[8]:= irefFS = iinFS * 1.25;  
In[9]:= trunup = 0.0001; vrunupFS = -2000;
```

Assuming equally long times for the reference voltages - this will very likely not be the case in the final design

```
In[10]:= nPos = 5; nNeg = 5; {tPos =  $\frac{t_{runup}}{n_{Pos}}$ , tNeg =  $\frac{t_{runup}}{n_{Neg}}$ }  
Out[10]= {0.00002, 0.00002}
```

Design choice: At least 100 clock cycles for the shortest time interval (might later be much shorter than  $t_{pos}/t_{neg}$  due to 3458A switch operation).

All operations on the FPGA must complete within one clock cycle.

```
In[11]:= fmin =  $\frac{100}{\text{Max}[\text{t}_{\text{Pos}}, \text{t}_{\text{Neg}}]} * 0.5$ 
Out[11]=  $1. \times 10^7$ 
```

## Compute the component values and constraints

```
In[12]:= {rMes =  $\frac{v_{inFS}}{i_{inFS}}$ , rRefPos =  $\frac{v_{refPos}}{i_{refFS}}$ , rRefNeg =  $\frac{-v_{refNeg}}{i_{refFS}}$ }
```

Integration Capacitor: With the maximum slope ( $V_{in}$  positive and negative reference switched in), the integrator shall rise to 70%  $V_{sat}$  within 3/4 of the time the reference is switched in:

```
In[13]:= capacitor = NSolve[
  1/(rMes * Cint) * vInFS * (tPos * 3/4) + 1/(rRefPos * Cint) * vRefPos * (tPos * 3/4) == (0.70 * vSat), Cint]
Out[13]= {{Cint -> 1.8544*10^-9}}
```

Calculate the slew rate of the rising signal with fullscale input and corresponding reference:

```
In[24]:= slewrateVusMin =
  
$$\frac{1}{r_{Mes} * C_{int}} * v_{inFS} * 0.000001 + \frac{1}{r_{RefPos} * C_{int}} * v_{refPos} * 0.000001 / . capacitor$$

Out[24]= {0.606667}
```

Design choice: The maximum current leakage into the opamp should be less than 5 least significant counts (drift of bias current might become relevant with temperature):

```
In[15]:= ierrorOpAmpMax = iinfS * 0.0000005  
Out[15]= 2.5 × 10-10
```

Compute the maximum acceptable timing jitter to not affect the measurement more than 0.75 of a least significant digit on a full-scale input:

```
In[16]:= VerrJitter[tJitter_, ΔvADC_] :=
- 
$$\left( r_{\text{Mes}} \left( n_{\text{Neg}} r_{\text{RefPos}} \left( t_{\text{Neg}} + \frac{t_{\text{Jitter}}}{n_{\text{Neg}}} \right) v_{\text{refNeg}} + r_{\text{RefNeg}} \left( n_{\text{Pos}} \left( t_{\text{Pos}} + \frac{t_{\text{Jitter}}}{n_{\text{Pos}}} \right) v_{\text{refPos}} + c_{\text{int}} r_{\text{RefPos}} \Delta v_{\text{ADC}} \right) \right) \right) / \left( r_{\text{RefNeg}} r_{\text{RefPos}} (t_{\text{runup}} + t_{\text{Jitter}}) \right) +$$


$$\frac{r_{\text{Mes}} \left( n_{\text{Neg}} r_{\text{RefPos}} t_{\text{Neg}} v_{\text{refNeg}} + r_{\text{RefNeg}} (n_{\text{Pos}} t_{\text{Pos}} v_{\text{refPos}} + c_{\text{int}} r_{\text{RefPos}} \Delta v_{\text{ADC}}) \right)}{r_{\text{RefNeg}} r_{\text{RefPos}} t_{\text{runup}}} .$$

capacitor;
```