

# Voltage Integrator Calculation

## Definitions and Equations - Multislope Continuous Runup with periodic ADC measurements

```
In[1]:= voutIn = -  $\frac{1}{r_{Mes} * C_{int}}$  * vin * Δtint;  
In[2]:= voutRefPos = -  $\frac{1}{r_{RefPos} * C_{int}}$  * vrefPos * tPos;  
In[3]:= voutRefNeg = -  $\frac{1}{r_{RefNeg} * C_{int}}$  * vrefNeg * tNeg;
```

Solve for the unkown input voltage  $V_{in}$  we want to measure:

```
In[4]:= Solve[voutIn + voutRefPos + voutRefNeg == ΔvADC, vin] // FullSimplify  
Out[4]=  $\left\{ \left\{ V_{in} \rightarrow - \frac{r_{Mes} (r_{RefNeg} t_{Pos} v_{refPos} + r_{RefPos} (t_{Neg} v_{refNeg} + C_{int} r_{RefNeg} \Delta v_{ADC}))}{r_{RefNeg} r_{RefPos} \Delta t_{int}} \right\} \right\}$ 
```

## Component value calculations and some error calculation

Design choices:

```
In[5]:= iinFS = 0.0005; vinFS = 2.5; vrefPos = 5.0; vrefNeg = -5.0; vsat = 11;  
In[6]:= irefFS = iinFS * 1.25;  
In[7]:=  $\left\{ r_{Mes} = \frac{v_{inFS}}{i_{inFS}}, r_{RefPos} = \frac{v_{refPos}}{i_{refFS}}, r_{RefNeg} = \frac{-v_{refNeg}}{i_{refFS}} \right\}$   
Out[7]= {5000., 8000., 8000.}
```

```
In[8]:= trunup = 0.001; vrunupFS = -2000; nPatterns = 100;
```

Calculate the mean time a reference is swichted in, with the 3458A patterns. 10% at each end is without any  $v_{ref}$  activated, so only use 80% of the pattern time

```
In[9]:=  $\left\{ t_{Pattern} = \frac{t_{runup}}{n_{Patterns}}, t_{Pos} = \frac{t_{runup}}{n_{Patterns}} * 0.8, t_{Neg} = \frac{t_{runup}}{n_{Patterns}} * 0.8 \right\}$   
Out[9]= {0.00001, 8. × 10-6, 8. × 10-6}
```

Design choice: At least 100 clock cycles for the shortest time interval, wich is 10% of a pattern time with the 3458A patterns:

All operations on the FPGA must complete within one clock cycle.

$$\text{In[10]:= } \mathbf{f}_{\min} = \frac{10}{\frac{\mathbf{t}_{\text{runup}}}{n_{\text{Patterns}}} * 0.10}$$

$$\text{Out[10]= } 1. \times 10^7$$

Compute the required ADC resolution in noise-free counts to resolve the virtual runup signal to the desired digit counts.

$$\text{In[11]:= } \mathbf{adc}_{\text{volts}} = \frac{-\mathbf{v}_{\text{runupFS}}}{2500000}$$

$$\text{Out[11]= } \frac{1}{1250}$$

$$\text{In[12]:= } \mathbf{adc}_{\text{counts}} = \frac{2 * \mathbf{v}_{\text{sat}}}{\mathbf{adc}_{\text{volts}}}$$

$$\text{Out[12]= } 27500$$

Add some margin

$$\text{In[13]:= } \mathbf{adc}_{\text{realcounts}} = \mathbf{adc}_{\text{counts}} * 1.5$$

$$\text{Out[13]= } 41250.$$

$$\text{In[14]:= } \{2^{14}, 2^{16}, 2^{18}\}$$

$$\text{Out[14]= } \{16384, 65536, 262144\}$$

## Compute the component values and constraints

Integration Capacitor: With the maximum slope ( $V_{in}$  positive and negative reference switched in), the integrator shall rise to 70%  $V_{sat}$  within 45% of the time the reference is switched in:  
old and wrong:

$$\text{capacitor} = \text{NSolve} \left[ \frac{1}{r_{\text{Mes}} * C_{\text{int}}} * V_{inFS} * (t_{\text{Pos}} * 0.45) + \frac{1}{r_{\text{RefPos}} * C_{\text{int}}} * V_{refPos} * (t_{\text{Pos}} * 0.45) == (0.70 * v_{\text{sat}}), C_{\text{int}} \right]$$

$$\text{In[15]:= } \text{capacitor} = \text{NSolve} \left[ \frac{1}{r_{\text{Mes}} * C_{\text{int}}} * V_{inFS} * t_{\text{runup}} == -V_{runupFS}, C_{\text{int}} \right]$$

$$\text{Out[15]= } \{C_{\text{int}} \rightarrow 2.5 \times 10^{-10}\}$$

Calculate the slew rate of the rising signal with fullscale input and corresponding reference:

$$\text{In[16]:= } \mathbf{slewrateV\mu s} = \frac{1}{r_{\text{Mes}} * C_{\text{int}}} * V_{inFS} * 0.000001 + \frac{1}{r_{\text{RefPos}} * C_{\text{int}}} * V_{refPos} * 0.000001 /. \text{capacitor}$$

$$\text{Out[16]= } \{4.5\}$$

Calculate the settling time - since we measure the second voltage for  $\Delta V_{\text{adc}}$  at the end of the last pattern, the opamp has to settle to less than 0.1 least significant digits after the last switch within:

$$\text{In[17]:= } \mathbf{t}_{\text{settle}} = \mathbf{t}_{\text{Pattern}} * 0.1$$

$$\text{Out[17]= } 1. \times 10^{-6}$$

```
In[18]:= vsettle = adcvolts * 0.1
Out[18]= 0.00008
```

Design choice: The maximum current leakage into the opamp should be less than 5 least significant counts (drift of bias current might become relevant with temperature):

```
In[19]:= ierrorOpAmpMax = iinFS * 0.0000005
Out[19]= 2.5 × 10-10
```

Compute the maximum acceptable phase noise / timing jitter to not affect the measurement more than 0.75 of a least significant digit on a full-scale input:

First, define the voltage error as a function of the jitter/phase noise and the  $\Delta V_{ADC}$

```
In[20]:= VerrJitter[tJitter_, ΔvADC_] :=
  (- (rMes ((tNeg + tJitter) rRefPos vrefNeg + rRefNeg ((tNeg + tJitter) vrefPos +
    Cint rRefPos ΔvADC)))) / (rRefNeg rRefPos (trunup + tJitter)) +
  (rMes (tNeg rRefPos vrefNeg + rRefNeg (tPos vrefPos + Cint rRefPos ΔvADC))) /
  (rRefNeg rRefPos trunup)) /. capacitor;

In[21]:= {NSolve[VerrJitter[tJitter, 13] == 0.00000075, tJitter],
  NSolve[VerrJitter[tJitter, 13] == 0.0000001, tJitter]}
Out[21]= {{tJitter → 4.6156 × 10-8}, {{tJitter → 6.15388 × 10-9}}}
```