

Voltage Integrator Calculation

Definitions and Equations - Multislope Continuous Runup with periodic ADC measurements

```
In[1]:= voutIn = -  $\frac{1}{r_{Mes} * C_{int}}$  * vin * Δtint;  
In[2]:= voutRefPos = -  $\frac{1}{r_{RefPos} * C_{int}}$  * vrefPos * ΔtrefPos;  
In[3]:= voutRefNeg = -  $\frac{1}{r_{RefNeg} * C_{int}}$  * vrefNeg * ΔtrefNeg;  
In[4]:= ΔtrefPos = tPos * nPos;  
In[5]:= ΔtrefNeg = tNeg * nNeg;
```

Solve for the unkown input voltage V_{in} we want to measure:

```
In[6]:= Solve[voutIn + voutRefPos + voutRefNeg == ΔvADC, vin] // FullSimplify  
Out[6]= { {vin → - (rMes (nNeg rRefPos tNeg vrefNeg + rRefNeg (nPos tPos vrefPos + Cint rRefPos ΔvADC)) ) / (rRefNeg rRefPos Δtint) } }
```

Component value calculations and some error calculation

Design choices:

```
In[7]:= iinFS = 0.0005; vinFS = 2.5; vrefPos = 5.0; vrefNeg = -5.0; vsat = 13;  
In[8]:= irefFS = iinFS * 1.25;  
In[9]:= trunup = 0.0001; vrunupFS = -2000;
```

Assuming equally long times for the reference voltages - this will very likely not be the case in the final design

```
In[10]:= nPos = 5; nNeg = 5; {tPos =  $\frac{t_{runup}}{n_{Pos}}$ , tNeg =  $\frac{t_{runup}}{n_{Neg}}$ }  
Out[10]= {0.00002, 0.00002}
```

Design choice: At least 100 clock cycles for the shortest time interval (might later be much shorter than t_{pos}/t_{neg} due to 3458A switch operation).

All operations on the FPGA must complete within one clock cycle.

```
In[11]:=  $f_{\min} = \frac{100}{\text{Max}[t_{\text{Pos}}, t_{\text{Neg}}] * 0.5}$ 
Out[11]=  $1. \times 10^7$ 
```

Compute the component values and constraints

```
In[12]:=  $\left\{ r_{\text{Mes}} = \frac{V_{\text{inFS}}}{i_{\text{inFS}}}, r_{\text{RefPos}} = \frac{V_{\text{refPos}}}{i_{\text{refFS}}}, r_{\text{RefNeg}} = \frac{-V_{\text{refNeg}}}{i_{\text{refFS}}} \right\}$ 
Out[12]= {5000., 8000., 8000.}
```

Integration Capacitor: With the maximum slope (V_{in} positive and negative reference switched in), the integrator shall rise to 70% V_{sat} within 3/4 of the time the reference is switched in:

```
In[13]:= capacitor = NSolve[
   $\frac{1}{r_{\text{Mes}} * C_{\text{int}}} * V_{\text{inFS}} * \left(t_{\text{Pos}} * \frac{3}{4}\right) + \frac{1}{r_{\text{RefPos}} * C_{\text{int}}} * V_{\text{refPos}} * \left(t_{\text{Pos}} * \frac{3}{4}\right) = (0.70 * V_{\text{sat}}), C_{\text{int}}]$ 
Out[13]= { $C_{\text{int}} \rightarrow 1.8544 \times 10^{-9}$ }
```

Calculate the slew rate of the rising signal with fullscale input and corresponding reference:

```
In[14]:= slewrateVusMin =
   $\frac{1}{r_{\text{Mes}} * C_{\text{int}}} * V_{\text{inFS}} * 0.000001 + \frac{1}{r_{\text{RefPos}} * C_{\text{int}}} * V_{\text{refPos}} * 0.000001 /. \text{capacitor}$ 
Out[14]= {0.606667}
```

Design choice: The maximum current leakage into the opamp should be less than 5 least significant counts (drift of bias current might become relevant with temperature):

```
In[15]:= i_errorOpAmpMax = i_inFS * 0.0000005
Out[15]=  $2.5 \times 10^{-10}$ 
```

Compute the maximum acceptable phase noise / timing jitter to not affect the measurement more than 0.75 of a least significant digit on a full-scale input:

First, define the voltage error as a function of the jitter/phase noise and the ΔV_{ADC}

```
In[22]:= VerrJitter[tJitter_,  $\Delta V_{\text{ADC}}_$ ] :=
   $(-(r_{\text{Mes}} (n_{\text{Neg}} (t_{\text{Neg}} + t_{\text{Jitter}}) r_{\text{RefPos}} V_{\text{refNeg}} + r_{\text{RefNeg}} (n_{\text{Neg}} (t_{\text{Neg}} + t_{\text{Jitter}}) V_{\text{refPos}} + C_{\text{int}} r_{\text{RefPos}} \Delta V_{\text{ADC}}))) / (r_{\text{RefNeg}} r_{\text{RefPos}} (t_{\text{runup}} + t_{\text{Jitter}} * (1 + n_{\text{Neg}} + n_{\text{Pos}}))) +$ 
   $r_{\text{Mes}} (n_{\text{Neg}} t_{\text{Neg}} r_{\text{RefPos}} V_{\text{refNeg}} + r_{\text{RefNeg}} (n_{\text{Pos}} t_{\text{Pos}} V_{\text{refPos}} + C_{\text{int}} r_{\text{RefPos}} \Delta V_{\text{ADC}})) / r_{\text{RefNeg}} r_{\text{RefPos}} t_{\text{runup}}$ 
  capacitor;

In[25]:= {NSolve[VerrJitter[tJitter, 13] == 0.00000075, tJitter],
  NSolve[VerrJitter[tJitter, 13] == 0.0000001, tJitter]}

Out[25]= {{ $t_{\text{Jitter}} \rightarrow 5.65657 \times 10^{-12}$ }}, {{ $t_{\text{Jitter}} \rightarrow 7.54209 \times 10^{-13}$ }}}
```

Compute the required ADC resolution in noise-free counts to resolve the virtual runup signal to the desired digit counts.

$$\text{In[18]:= } \text{adc}_{\text{volts}} = \frac{-\text{vrunupFS}}{2\ 500\ 000}$$

$$\text{Out[18]= } \frac{1}{1250}$$

$$\text{In[19]:= } \text{adc}_{\text{counts}} = \frac{2 * \text{vsat}}{\text{adc}_{\text{volts}}}$$

$$\text{Out[19]= } 32\ 500$$

Add some margin

$$\text{In[20]:= } \text{adc}_{\text{realcounts}} = \text{adc}_{\text{counts}} * 1.5$$

$$\text{Out[20]= } 48\ 750.$$

$$\text{In[21]:= } \{2^{14}, 2^{16}, 2^{18}\}$$

$$\text{Out[21]= } \{16\ 384, 65\ 536, 262\ 144\}$$