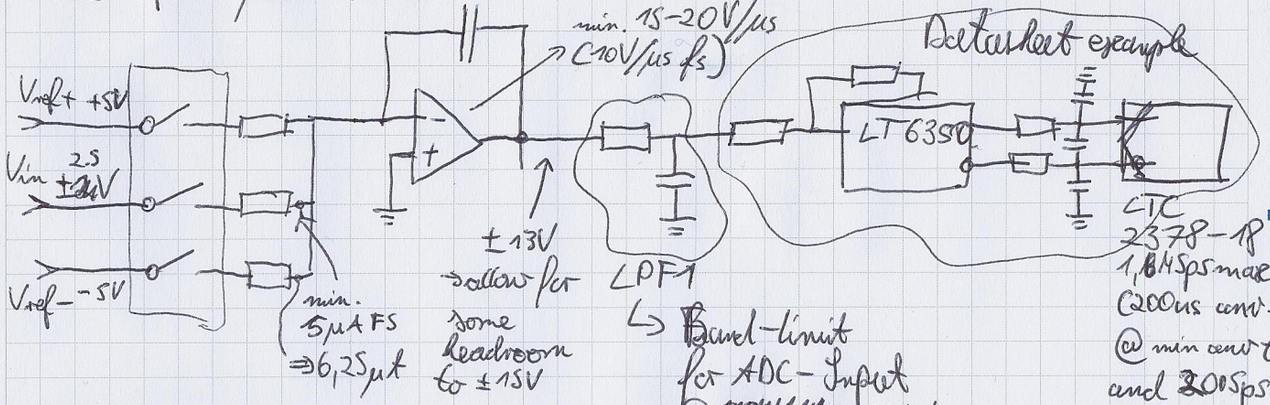
FS = Fs = full-scale



Operation:

- Use 3458A switing cycles for ramup
- Vref stages are 25% stronger than $V_{in,max}$

@ Ram-Up to 1kV virtual integration:

⇒ 1kV / 2500000 = 0,0004V = 0,4mV required resolution of ADC

↳ @ ±13V_{fs} ⇒ 32 500 cuts of ADC (noise free)
⇒ 18 bit ADC

Ramup Time: 1kV-FS ⇒ 10V/µs
⇒ 100µs

Theoretical Speed (with delays and switing) ⇒ 4kSps (estimate)

Limit the final speed to 100Sps!