

Voltage Integrator Calculation

Definitions and Equations - Multislope Continuous Runup with periodic ADC measurements

```
In[1]:= voutIn = -  $\frac{1}{r_{Mes} * C_{int}}$  * vin * Δtint;  
In[2]:= voutRefPos = -  $\frac{1}{r_{RefPos} * C_{int}}$  * vrefPos * tPos;  
In[3]:= voutRefNeg = -  $\frac{1}{r_{RefNeg} * C_{int}}$  * vrefNeg * tNeg;
```

Solve for the unkown input voltage V_{in} we want to measure:

```
In[5]:= Solve[voutIn + voutRefPos + voutRefNeg == ΔvADC, vin] // FullSimplify  
Out[5]= { {vin → - (rMes (rRefNeg tPos vrefPos + rRefPos (tNeg vrefNeg + Cint rRefNeg ΔvADC))) / (rRefNeg rRefPos Δtint) } }
```

Component value calculations and some error calculation

Design choices:

```
In[39]:= iinFS = 0.0005; vinFS = 2.5; vrefPos = 5.0; vrefNeg = -5.0; vsat = 11;  
In[40]:= irefFS = iinFS * 1.25;  
In[41]:= trunup = 0.001; vrunupFS = -2000;
```

Calculate the mean time a reference is swichted in, with the 3458A patterns. 10% at each end is without any v_{ref} activated, so only use 80% of the pattern time

```
In[42]:= nPatters = 10; {tPos =  $\frac{t_{runup}}{n_{Patters}} * 0.8$ , tNeg =  $\frac{t_{runup}}{n_{Patters}} * 0.8$ }  
Out[42]= {0.00008, 0.00008}
```

Design choice: At least 100 clock cycles for the shortest time interval, wich is 10% of a pattern time with the 3458A patterns:

All operations on the FPGA must complete within one clock cycle.

```
In[43]:= fmin =  $\frac{100}{\text{Max}[t_{Pos}, t_{Neg}] * 0.1}$   
Out[43]= 1.25 × 107
```

Compute the component values and constraints

$$\text{In[44]} = \left\{ r_{\text{Mes}} = \frac{V_{\text{inFS}}}{i_{\text{inFS}}}, r_{\text{RefPos}} = \frac{V_{\text{refPos}}}{i_{\text{refFS}}}, r_{\text{RefNeg}} = \frac{-V_{\text{refNeg}}}{i_{\text{refFS}}} \right\}$$

Out[44]= {5000., 8000., 8000.}

Integration Capacitor: With the maximum slope (V_{in} positive and negative reference switched in), the integrator shall rise to 70% V_{sat} within 45% of the time the reference is switched in:

$$\begin{aligned} \text{In[45]} = & \text{capacitor} = \text{NSolve} \left[\frac{1}{r_{\text{Mes}} * c_{\text{int}}} * v_{\text{inFS}} * (t_{\text{Pos}} * 0.45) + \right. \\ & \left. \frac{1}{r_{\text{RefPos}} * c_{\text{int}}} * v_{\text{refPos}} * (t_{\text{Pos}} * 0.45) = (0.70 * v_{\text{sat}}), c_{\text{int}} \right] \\ \text{Out[45]} = & \{ \{c_{\text{int}} \rightarrow 5.25974 \times 10^{-9}\} \} \end{aligned}$$

Calculate the slew rate of the rising signal with fullscale input and corresponding reference:

$$\begin{aligned} \text{In[46]} = & \text{slewrateVusMin} = \\ & \frac{1}{r_{\text{Mes}} * c_{\text{int}}} * v_{\text{inFS}} * 0.000001 + \frac{1}{r_{\text{RefPos}} * c_{\text{int}}} * v_{\text{refPos}} * 0.000001 /. \text{capacitor} \\ \text{Out[46]} = & \{0.213889\} \end{aligned}$$

Design choice: The maximum current leakage into the opamp should be less than 5 least significant counts (drift of bias current might become relevant with temperature):

$$\begin{aligned} \text{In[15]} = & i_{\text{errorOpAmpMax}} = i_{\text{inFS}} * 0.000005 \\ \text{Out[15]} = & 2.5 \times 10^{-10} \end{aligned}$$

Compute the maximum acceptable phase noise / timing jitter to not affect the measurement more than 0.75 of a least significant digit on a full-scale input:

First, define the voltage error as a function of the jitter/phase noise and the ΔV_{ADC}

$$\begin{aligned} \text{In[47]} = & \text{VerrJitter}[t_{\text{Jitter}}, \Delta V_{\text{ADC}}] := \\ & (- (r_{\text{Mes}} ((t_{\text{Neg}} + t_{\text{Jitter}}) r_{\text{RefPos}} v_{\text{refNeg}} + r_{\text{RefNeg}} ((t_{\text{Neg}} + t_{\text{Jitter}}) v_{\text{refPos}} + \\ & c_{\text{int}} r_{\text{RefPos}} \Delta V_{\text{ADC}}))) / (r_{\text{RefNeg}} r_{\text{RefPos}} (t_{\text{runup}} + t_{\text{Jitter}})) + \\ & (r_{\text{Mes}} (t_{\text{Neg}} r_{\text{RefPos}} v_{\text{refNeg}} + r_{\text{RefNeg}} (t_{\text{Pos}} v_{\text{refPos}} + c_{\text{int}} r_{\text{RefPos}} \Delta V_{\text{ADC}}))) / \\ & (r_{\text{RefNeg}} r_{\text{RefPos}} t_{\text{runup}}) /. \text{capacitor}; \\ \text{In[48]} = & \{\text{NSolve}[\text{VerrJitter}[t_{\text{Jitter}}, 13] == 0.00000075, t_{\text{Jitter}}], \\ & \text{NSolve}[\text{VerrJitter}[t_{\text{Jitter}}, 13] == 0.0000001, t_{\text{Jitter}}]\} \\ \text{Out[48]} = & \{\{t_{\text{Jitter}} \rightarrow 2.19374 \times 10^{-9}\}, \{t_{\text{Jitter}} \rightarrow 2.92498 \times 10^{-10}\}\} \end{aligned}$$

Compute the required ADC resolution in noise-free counts to resolve the virtual runup signal to the desired digit counts.

$$\begin{aligned} \text{In[49]} = & \text{adcVolts} = \frac{-v_{\text{runupFS}}}{2500000} \\ \text{Out[49]} = & \frac{1}{1250} \end{aligned}$$

$$\text{In[50]:= } \text{adc}_{\text{counts}} = \frac{2 * \text{vsat}}{\text{adc}_{\text{volts}}}$$

Out[50]= 27 500

Add some margin

$$\text{In[51]:= } \text{adc}_{\text{realcounts}} = \text{adc}_{\text{counts}} * 1.5$$

Out[51]= 41 250.

$$\text{In[38]:= } \{2^{14}, 2^{16}, 2^{18}\}$$

Out[38]= {16 384, 65 536, 262 144}