

Voltage Integrator Calculation

Definitions and Equations - Multislope Continuous Runup with periodic ADC measurements

```
In[1]:= voutIn = -  $\frac{1}{r_{Mes} * C_{int}}$  * vin * Δtint;  
In[2]:= voutRefPos = -  $\frac{1}{r_{RefPos} * C_{int}}$  * vrefPos * tPos;  
In[3]:= voutRefNeg = -  $\frac{1}{r_{RefNeg} * C_{int}}$  * vrefNeg * tNeg;
```

Solve for the unkown input voltage V_{in} we want to measure:

```
In[4]:= Solve[voutIn + voutRefPos + voutRefNeg == ΔvADC, vin] // FullSimplify  
Out[4]= {vin → 0. -  $\frac{1 \cdot C_{int} V_{inFS} \Delta v_{ADC}}{i_{inFS} \Delta t_{int}}$ }
```

Component value calculations and some error calculation

Design Choices:

```
In[5]:= iinFS = 0.0005; vinFS = 2.5; vrefPos = 5.0; vrefNeg = -5.0;  
vsat = 11; vth = 5; trunup = 0.001; vrunupFS = -2750;  
In[6]:= irefFS = iinFS * 1.25;
```

Resistor Values:

```
In[7]:= Dynamic[{rMes =  $\frac{V_{inFS}}{i_{inFS}}$ , rRefPos =  $\frac{V_{refPos}}{i_{refFS}}$ , rRefNeg =  $\frac{-V_{refNeg}}{i_{refFS}}$ }]  
Out[7]= {5000., 8000., 8000.}  
{5000., 8000., 8000.}
```

Integration Capacitor:

```
In[8]:= Dynamic[capacitor = NSolve[ $\frac{1}{r_{Mes} * C_{int}} * v_{inFS} * t_{runup} == -v_{runupFS}$ , Cint]]  
Out[8]= {Cint → 1.81818 × 10-10}
```

Timing

Calculate the maximum allowable pattern time, to stay below V_{th} by 0.1V (we want the integrator to stabilize around the zero position):

```
In[9]:= Dynamic[pTime = NSolve[-(1/(rMes * Cint) * vInFS * tPattern) - (1/(rRefNeg * Cint) * vRefNeg * 0.8 * tPattern) - (1/(rRefPos * Cint) * vRefPos * 0.1 * tPattern) == -2 * vTh - 1 + 0.1, tPattern] /. capacitor]
Out[9]= {{tPattern -> 0.0000317091}}
```

Compute the minimum allowable number of patterns, due to the pattern time:

```
In[10]:= Dynamic[nPatterns = Ceiling[tRunup / pTime]]
Out[10]= {32}
```

```
In[11]:= Dynamic[{tPos = tRunup/nPatterns * 0.8, tNeg = tRunup/nPatterns * 0.8, tMin = tRunup/nPatterns * 0.1} /. pTime]
Out[11]= {{{{0.000025}}, {{0.000025}}, {{3.125*10^-6}}}}
```

Design choice: At least 10 clock cycles for the shortest time interval, which is 10% of a pattern time with the 3458A patterns:

All operations on the FPGA must complete within one clock cycle. The minimum required **Clock frequency** is:

```
In[12]:= Dynamic[{fMin = 10 / tRunup * 0.10 /. pTime, TFreq = 1/fMin}]
Out[12]= {{{{3.2*10^6}}}, {{{{3.125*10^-7}}}}}
```

Required ADC resolution

```
In[13]:= Dynamic[adcVolts = -vRunupFS / 2500000]
Out[13]= 11 / 10000
```

Compute the minimum required number of **ADC counts**

```
In[14]:= Dynamic[Ceiling[adcCounts = 2 * vSat / adcVolts]]
Out[14]= 20000
```

Add some margin

```
In[15]:= Dynamic[adcRealCounts = adcCounts * 1.25]
Out[15]= 25000.
```

```
In[16]:= {2^12, 2^14, 2^16, 2^18}
Out[16]= {4096, 16384, 65536, 262144}
```

Calculate the maximum number of adc samples possible with our 1.6MSPS ADC @ 625ns per Sample:

$$\text{In[17]:= Dynamic} \left[\text{adc}_{\text{Samples}} = \frac{\text{t}_{\text{min}}}{0.000000625} \right]$$

Out[17]= { {5.} }

Theoretically gained resolution in bit and reduction in noise power / increase in SNR by a factor of:

$$\text{In[40]:= Dynamic} \left[\left\{ \text{resgained} = \frac{\text{Log}[\text{adc}_{\text{Samples}}]}{2 \text{Log}[2]}, \text{noise}_{\text{power}} = \frac{1}{\text{adc}_{\text{Samples}}} \right\} \right]$$

Out[40]= { {{1.16096}}, {{0.2}} }

Compute the component values and constraints

Calculate the **slew rate** of the rising signal with fullscale input and corresponding reference:

$$\text{In[18]:= Dynamic} \left[\text{slewrateVus} = \frac{1}{\text{r}_{\text{Mes}} * \text{c}_{\text{int}}} * \text{v}_{\text{inFS}} * 0.000001 + \frac{1}{\text{r}_{\text{RefPos}} * \text{c}_{\text{int}}} * \text{v}_{\text{refPos}} * 0.000001 /. \text{capacitor} \right]$$

Out[18]= {6.1875}

Calculate the **settling time** - since we measure the second voltage for ΔV_{adc} at the end of the last pattern, the opamp has to settle to less than 0.1 least significant digits after the last switch within:

$$\text{In[19]:= Dynamic} \left[\text{t}_{\text{settle}} = \frac{\text{t}_{\text{runup}}}{\text{n}_{\text{Patters}}} * 0.1 \right] /. \text{ptime}$$

Out[19]= { {{ {3.125 \times 10^{-6}}} } }

$$\text{In[20]:= Dynamic} [\text{v}_{\text{settle}} = \text{adc}_{\text{volts}} * 0.1] /. \text{ptime}$$

Out[20]= { {0.00011} }

Design choice: The maximum **current leakage** into the opamp should be less than 5 least significant counts (drift of bias current might become relevant with temperature):

$$\text{In[21]:= Dynamic} [\text{i}_{\text{errorOpAmpMax}} = \text{i}_{\text{inFS}} * 0.000005]$$

Out[21]= 2.5×10^{-10}

Compute the maximum acceptable phase noise / **timing uncertainty** to not affect the measurement more than 0.75 of a least significant digit on a full-scale input:

First, define the voltage error as a function of the jitter/phase noise and the ΔV_{ADC}

$$\begin{aligned} \text{In[22]:= VerrJitter} [\text{tJitter}_-, \Delta \text{vADC}_-] := & (- (\text{r}_{\text{Mes}} ((\text{t}_{\text{Neg}} + \text{tJitter}) \text{r}_{\text{RefPos}} \text{v}_{\text{refNeg}} + \text{r}_{\text{RefNeg}} ((\text{t}_{\text{Neg}} + \text{tJitter}) \text{v}_{\text{refPos}} + \\ & \text{c}_{\text{int}} \text{r}_{\text{RefPos}} \Delta \text{vADC}))) / (\text{r}_{\text{RefNeg}} \text{r}_{\text{RefPos}} (\text{t}_{\text{runup}} + \text{tJitter})) + \\ & (\text{r}_{\text{Mes}} (\text{t}_{\text{Neg}} \text{r}_{\text{RefPos}} \text{v}_{\text{refNeg}} + \text{r}_{\text{RefNeg}} (\text{t}_{\text{Pos}} \text{v}_{\text{refPos}} + \text{c}_{\text{int}} \text{r}_{\text{RefPos}} \Delta \text{vADC}))) / \\ & (\text{r}_{\text{RefNeg}} \text{r}_{\text{RefPos}} \text{t}_{\text{runup}}) /. \text{capacitor}; \end{aligned}$$

$$\text{In[23]:= Dynamic} [\{\text{NSolve}[\text{VerrJitter}[\text{tJitter}, 13] == 0.00000075, \text{tJitter}], \\ \text{NSolve}[\text{VerrJitter}[\text{tJitter}, 13] == 0.0000001, \text{tJitter}]\}]$$

Out[23]= { {{tJitter \rightarrow 6.34656 \times 10^{-8}}}, {{tJitter \rightarrow 8.46161 \times 10^{-9}}}}