

Voltage Integrator Calculation

Definitions and Equations - Multislope Continuous Runup with periodic ADC measurements

```
In[1]:= voutIn = -  $\frac{1}{r_{Mes} * C_{int}}$  * vin * Δtint;  
In[2]:= voutRefPos = -  $\frac{1}{r_{RefPos} * C_{int}}$  * vrefPos * tPos;  
In[3]:= voutRefNeg = -  $\frac{1}{r_{RefNeg} * C_{int}}$  * vrefNeg * tNeg;
```

Solve for the unkown input voltage V_{in} we want to measure:

```
In[4]:= Solve[voutIn + voutRefPos + voutRefNeg == ΔvADC, vin] // FullSimplify  
Out[4]= { {vin → - (rMes (rRefNeg tPos vrefPos + rRefPos (tNeg vrefNeg + Cint rRefNeg ΔvADC))) / (rRefNeg rRefPos Δtint) } }
```

Component value calculations and some error calculation

Design choices:

```
In[5]:= iinFS = 0.0005; vinFS = 2.5; vrefPos = 5.0; vrefNeg = -5.0; vsat = 11;  
In[6]:= irefFS = iinFS * 1.25;
```

Resistor Values:

```
In[7]:= Dynamic[ {rMes =  $\frac{v_{inFS}}{i_{inFS}}$ , rRefPos =  $\frac{v_{refPos}}{i_{refFS}}$ , rRefNeg =  $\frac{-v_{refNeg}}{i_{refFS}}$  } ]  
Out[7]= {5000., 8000., 8000.}
```

```
In[23]:= trunup = 0.001; vrunupFS = -5000; nPatters = 100;
```

Calculate the mean time a reference is swichted in, with the 3458A patterns. 10% at each end is without any v_{ref} activated, so only use 80% of the **pattern time**

```
In[9]:= Dynamic[ {tPattern =  $\frac{t_{runup}}{n_{Patters}}$ , tPos =  $\frac{t_{runup}}{n_{Patters}} * 0.8$ , tNeg =  $\frac{t_{runup}}{n_{Patters}} * 0.8$  } ]  
Out[9]= {0.00001, 8. × 10-6, 8. × 10-6}
```

Design choice: At least 100 clock cycles for the shortest time interval, wich is 10% of a pattern time with the 3458A patterns:

All operations on the FPGA must complete within one clock cycle. The minimum required **Clock frequency** is:

$$\text{In[10]:= Dynamic} \left[f_{\min} = \frac{10}{\frac{t_{\text{runup}}}{n_{\text{Patters}}} * 0.10} \right]$$

Out[10]= $1. \times 10^7$

Compute the required ADC resolution in noise-free counts to resolve the virtual runup signal to the desired digit counts.

$$\text{In[11]:= Dynamic} \left[\text{adc}_{\text{volts}} = \frac{-v_{\text{runupFS}}}{2500000} \right]$$

Out[11]= $\frac{1}{500}$

Compute the minimum required number of **ADC counts**

$$\text{In[12]:= Dynamic} \left[\text{adc}_{\text{counts}} = \frac{2 * v_{\text{sat}}}{\text{adc}_{\text{volts}}} \right]$$

Out[12]= 11 000

Add some margin

$$\text{In[13]:= Dynamic} [\text{adc}_{\text{realcounts}} = \text{adc}_{\text{counts}} * 1.25]$$

Out[13]= 13 750.

$$\text{In[14]:= } \{2^{14}, 2^{16}, 2^{18}\}$$

Out[14]= {16 384, 65 536, 262 144}

Compute the component values and constraints

Integration Capacitor: With the maximum slope (V_{in} positive and negative reference switched in), the integrator shall rise to 70% V_{sat} within 45% of the time the reference is switched in:
old and wrong:

$$\text{capacitor} = \text{NSolve} \left[\frac{1}{r_{\text{Mes}} * c_{\text{int}}} * v_{\text{inFS}} * (t_{\text{Pos}} * 0.45) + \frac{1}{r_{\text{RefPos}} * c_{\text{int}}} * v_{\text{refPos}} * (t_{\text{Pos}} * 0.45) == (0.70 * v_{\text{sat}}), c_{\text{int}} \right]$$

$$\text{In[15]:= Dynamic} \left[\text{capacitor} = \text{NSolve} \left[\frac{1}{r_{\text{Mes}} * c_{\text{int}}} * v_{\text{inFS}} * t_{\text{runup}} == -v_{\text{runupFS}}, c_{\text{int}} \right] \right]$$

Out[15]= $\{c_{\text{int}} \rightarrow 1. \times 10^{-10}\}$

Calculate the **slew rate** of the rising signal with fullscale input and corresponding reference:

$$\text{In[16]:= Dynamic} [\text{slewrateV}\mu\text{s} = \frac{1}{r_{\text{Mes}} * c_{\text{int}}} * v_{\text{inFS}} * 0.000001 + \frac{1}{r_{\text{RefPos}} * c_{\text{int}}} * v_{\text{refPos}} * 0.000001 /. \text{capacitor}]$$

Out[16]= {11.25}

Calculate the **settling time** - since we measure the second voltage for ΔV_{adc} at the end of the last pattern, the opamp has to settle to less than 0.1 least significant digits after the last switch within:

```
In[17]:= Dynamic[t_settle = t_Pattern * 0.1]
```

```
Out[17]= 1. × 10-6
```

```
In[18]:= Dynamic[v_settle = adc_volts * 0.1]
```

```
Out[18]= 0.0002
```

Design choice: The maximum **current leakage** into the opamp should be less than 5 least significant counts (drift of bias current might become relevant with temperature):

```
In[19]:= Dynamic[i_errorOpAmpMax = i_inFS * 0.0000005]
```

```
Out[19]= 2.5 × 10-10
```

Compute the maximum acceptable phase noise / **timing uncertainty** to not affect the measurement more than 0.75 of a least significant digit on a full-scale input:

First, define the voltage error as a function of the jitter/phase noise and the ΔV_{ADC}

```
In[20]:= VerrJitter[tJitter_, ΔvADC_] :=
  (- (rMes ((tNeg + tJitter) rRefPos vRefNeg + rRefNeg ((tNeg + tJitter) vRefPos +
    cint rRefPos ΔvADC)))) / (rRefNeg rRefPos (tRunup + tJitter)) +
  (rMes (tNeg rRefPos vRefNeg + rRefNeg (tPos vRefPos + cint rRefPos ΔvADC))) /(
  rRefNeg rRefPos tRunup) /. capacitor;
```

```
In[21]:= Dynamic[{NSolve[VerrJitter[tJitter, 13] == 0.00000075, tJitter],
  NSolve[VerrJitter[tJitter, 13] == 0.0000001, tJitter]}]
```

```
Out[21]= {{tJitter → 1.15398 × 10-7}, {tJitter → 1.53849 × 10-8}}
```