

# Voltage Integrator Calculation

## Definitions and Equations - Multislope Continuous Runup with periodic ADC measurements

```
In[1]:= voutIn = -  $\frac{1}{r_{Mes} * C_{int}}$  * vin * Δtint;  
In[2]:= voutRefPos = -  $\frac{1}{r_{RefPos} * C_{int}}$  * vrefPos * tPos;  
In[3]:= voutRefNeg = -  $\frac{1}{r_{RefNeg} * C_{int}}$  * vrefNeg * tNeg;
```

Solve for the unkown input voltage  $V_{in}$  we want to measure:

```
In[5]:= Solve[voutIn + voutRefPos + voutRefNeg == ΔvADC, vin] // FullSimplify  
Out[5]= { {vin → - (rMes (rRefNeg tPos vrefPos + rRefPos (tNeg vrefNeg + Cint rRefNeg ΔvADC))) / (rRefNeg rRefPos Δtint) } }
```

## Component value calculations and some error calculation

Design choices:

```
In[39]:= iinFS = 0.0005; vinFS = 2.5; vrefPos = 5.0; vrefNeg = -5.0; vsat = 11;  
In[40]:= irefFS = iinFS * 1.25;  
In[41]:= trunup = 0.001; vrunupFS = -2000;
```

Calculate the mean time a reference is swichted in, with the 3458A patterns. 10% at each end is without any  $v_{ref}$  activated, so only use 80% of the pattern time

```
In[59]:= nPatters = 10; {tPattern =  $\frac{t_{runup}}{n_{Patters}}$ , tPos =  $\frac{t_{runup}}{n_{Patters}} * 0.8$ , tNeg =  $\frac{t_{runup}}{n_{Patters}} * 0.8$ }  
Out[59]= {0.0001, 0.00008, 0.00008}
```

Design choice: At least 100 clock cycles for the shortest time interval, wich is 10% of a pattern time with the 3458A patterns:

All operations on the FPGA must complete within one clock cycle.

```
In[58]:= fmin =  $\frac{100}{\frac{t_{runup}}{n_{Patters}} * 0.10}$   
Out[58]= 1. × 107
```

Compute the required ADC resolution in noise-free counts to resolve the virtual runup signal to the desired digit counts.

$$\text{In[49]:= } \text{adc\_volts} = \frac{-v_{\text{runupFS}}}{2500000}$$

$$\text{Out[49]= } \frac{1}{1250}$$

$$\text{In[50]:= } \text{adc\_counts} = \frac{2 * v_{\text{sat}}}{\text{adc\_volts}}$$

$$\text{Out[50]= } 27500$$

Add some margin

$$\text{In[51]:= } \text{adc\_realcounts} = \text{adc\_counts} * 1.5$$

$$\text{Out[51]= } 41250.$$

$$\text{In[38]:= } \{2^{14}, 2^{16}, 2^{18}\}$$

$$\text{Out[38]= } \{16384, 65536, 262144\}$$

Compute the component values and constraints

$$\text{In[44]:= } \left\{ r_{\text{Mes}} = \frac{v_{\text{inFS}}}{i_{\text{inFS}}}, r_{\text{RefPos}} = \frac{v_{\text{refPos}}}{i_{\text{refFS}}}, r_{\text{RefNeg}} = \frac{-v_{\text{refNeg}}}{i_{\text{refFS}}} \right\}$$

$$\text{Out[44]= } \{5000., 8000., 8000.\}$$

Integration Capacitor: With the maximum slope ( $V_{\text{in}}$  positive and negative reference switched in), the integrator shall rise to 70%  $V_{\text{sat}}$  within 45% of the time the reference is switched in:

$$\text{In[45]:= } \text{capacitor} = \text{NSolve} \left[ \frac{1}{r_{\text{Mes}} * c_{\text{int}}} * v_{\text{inFS}} * (t_{\text{pos}} * 0.45) + \frac{1}{r_{\text{RefPos}} * c_{\text{int}}} * v_{\text{refPos}} * (t_{\text{pos}} * 0.45) = (0.70 * v_{\text{sat}}), c_{\text{int}} \right]$$

$$\text{Out[45]= } \{c_{\text{int}} \rightarrow 5.25974 \times 10^{-9}\}$$

Calculate the slew rate of the rising signal with fullscale input and corresponding reference:

$$\text{In[46]:= } \text{slewrateVusMin} = \frac{1}{r_{\text{Mes}} * c_{\text{int}}} * v_{\text{inFS}} * 0.000001 + \frac{1}{r_{\text{RefPos}} * c_{\text{int}}} * v_{\text{refPos}} * 0.000001 /. \text{capacitor}$$

$$\text{Out[46]= } 0.213889$$

Calculate the settling time - since we measure the second voltage for  $\Delta V_{\text{adc}}$  at the end of the last pattern, the opamp has to settle to less than 0.1 least significant digits after the last switch within:

$$\text{In[60]:= } t_{\text{settle}} = t_{\text{Pattern}} * 0.1$$

$$\text{Out[60]= } 0.00001$$

$$\text{In[61]:= } v_{\text{settle}} = \text{adc\_volts} * 0.1$$

$$\text{Out[61]= } 0.00008$$

Design choice: The maximum current leakage into the opamp should be less than 5 least significant counts (drift of bias current might become relevant with temperature):

```
In[15]:= i_errorOpAmpMax = i_inFS * 0.0000005
```

```
Out[15]= 2.5 × 10-10
```

Compute the maximum acceptable phase noise / timing jitter to not affect the measurement more than 0.75 of a least significant digit on a full-scale input:

First, define the voltage error as a function of the jitter/phase noise and the  $\Delta V_{ADC}$

```
In[47]:= VerrJitter[tJitter_, ΔvADC_] :=
  (- (rMes ((tNeg + tJitter) rRefPos vrefNeg + rRefNeg ((tNeg + tJitter) vrefPos +
    cint rRefPos ΔvADC)))) / (rRefNeg rRefPos (trunup + tJitter)) +
  (rMes (tNeg rRefPos vrefNeg + rRefNeg (tPos vrefPos + cint rRefPos ΔvADC))) /
  (rRefNeg rRefPos trunup) /. capacitor;
```

```
In[48]:= {NSolve[VerrJitter[tJitter, 13] == 0.00000075, tJitter],
  NSolve[VerrJitter[tJitter, 13] == 0.0000001, tJitter]}
```

```
Out[48]= {{tJitter → 2.19374 × 10-9}}, {{tJitter → 2.92498 × 10-10}}
```