

# Voltage Integrator Calculation

## Definitions and Equations - Multislope Continuous Runup with periodic ADC measurements

$$\begin{aligned} v_{outIn} &= -\frac{1}{r_{Mes} * c_{int}} * v_{in} * \Delta t_{int}; \\ v_{outRefPos} &= -\frac{1}{r_{RefPos} * c_{int}} * v_{refPos} * \Delta t_{refPos}; \\ v_{outRefNeg} &= -\frac{1}{r_{RefNeg} * c_{int}} * v_{refNeg} * \Delta t_{refNeg}; \\ \Delta t_{refPos} &= t_{Pos} * n_{Pos}; \\ \Delta t_{refNeg} &= t_{Neg} * n_{Neg}; \end{aligned}$$

Solve for the unkown input voltage  $V_{in}$  we want to measure:

$$\begin{aligned} \text{Solve}[v_{outIn} + v_{outRefPos} + v_{outRefNeg} == \Delta v_{ADC}, v_{in}] // \text{FullSimplify} \\ \left\{ \left\{ v_{in} \rightarrow - \left( r_{Mes} (n_{Neg} r_{RefPos} t_{Neg} v_{refNeg} + r_{RefNeg} (n_{Pos} t_{Pos} v_{refPos} + c_{int} r_{RefPos} \Delta v_{ADC})) \right) / (r_{RefNeg} r_{RefPos} \Delta t_{int}) \right\} \right\} \end{aligned}$$

## Component value calculations and some error calculation

Design choices:

$$\begin{aligned} i_{inFS} &= 0.0005; v_{inFS} = 2.5; v_{refPos} = 5.0; v_{refNeg} = -5.0; v_{sat} = 13; \\ i_{refFS} &= i_{inFS} * 1.25; \\ t_{runup} &= 0.0001; v_{runupFS} = -2000; \end{aligned}$$

Assuming equally long times for the reference voltages - this will very likely not be the case in the final design

$$\begin{aligned} n_{Pos} &= 5; n_{Neg} = 5; \left\{ t_{Pos} = \frac{t_{runup}}{n_{Pos}}, t_{Neg} = \frac{t_{runup}}{n_{Neg}} \right\} \\ &\{0.00002, 0.00002\} \end{aligned}$$

Design choice: At least 100 clock cycles for the shortest time interval (might later be much shorter than  $t_{pos}/t_{neg}$  due to 3458A switch operation).

All operations on the FPGA must complete within one clock cycle.

$$f_{\min} = \frac{100}{\text{Max}[t_{\text{Pos}}, t_{\text{Neg}}] * 0.5}$$

$$1. \times 10^7$$

## Compute the component values and constraints

$$\left\{ r_{\text{Mes}} = \frac{V_{\text{inFS}}}{i_{\text{inFS}}}, r_{\text{RefPos}} = \frac{V_{\text{refPos}}}{i_{\text{refFS}}}, r_{\text{RefNeg}} = \frac{-V_{\text{refNeg}}}{i_{\text{refFS}}} \right\}$$

$$\{5000., 8000., 8000.\}$$

Integration Capacitor: With the maximum slope ( $V_{\text{in}}$  positive and negative reference switched in), the integrator shall rise to 70%  $V_{\text{sat}}$  within 3/4 of the time the reference is switched in:

$$\begin{aligned} \text{capacitor} = \text{NSolve} [ & \\ & \frac{1}{r_{\text{Mes}} * C_{\text{int}}} * V_{\text{inFS}} * \left( t_{\text{Pos}} * \frac{3}{4} \right) + \frac{1}{r_{\text{RefPos}} * C_{\text{int}}} * V_{\text{refPos}} * \left( t_{\text{Pos}} * \frac{3}{4} \right) = (0.70 * V_{\text{sat}}), C_{\text{int}} ] \\ & \{C_{\text{int}} \rightarrow 1.8544 \times 10^{-9}\} \end{aligned}$$

Calculate the slew rate of the rising signal with fullscale input and corresponding reference:

$$\begin{aligned} \text{slewrateVusMin} = & \\ & \frac{1}{r_{\text{Mes}} * C_{\text{int}}} * V_{\text{inFS}} * 0.000001 + \frac{1}{r_{\text{RefPos}} * C_{\text{int}}} * V_{\text{refPos}} * 0.000001 /. \text{capacitor} \\ & \{0.606667\} \end{aligned}$$

Design choice: The maximum current leakage into the opamp should be less than 5 least significant counts (drift of bias current might become relevant with temperature):

$$i_{\text{errorOpAmpMax}} = i_{\text{inFS}} * 0.0000005$$

$$2.5 \times 10^{-10}$$

Compute the maximum acceptable timing jitter to not affect the measurement more than 0.75 of a least significant digit on a full-scale input:

$$\begin{aligned} \text{VerrJitter}[t_{\text{Jitter}}, \Delta v_{\text{ADC}}] := & \\ & - \left( r_{\text{Mes}} \left( n_{\text{Neg}} r_{\text{RefPos}} \left( t_{\text{Neg}} + \frac{t_{\text{Jitter}}}{n_{\text{Neg}}} \right) V_{\text{refNeg}} + r_{\text{RefNeg}} \left( n_{\text{Pos}} \left( t_{\text{Pos}} + \frac{t_{\text{Jitter}}}{n_{\text{Pos}}} \right) V_{\text{refPos}} + \right. \right. \right. \right. \\ & \left. \left. \left. \left. c_{\text{int}} r_{\text{RefPos}} \Delta v_{\text{ADC}} \right) \right) \right) / (r_{\text{RefNeg}} r_{\text{RefPos}} (t_{\text{runup}} + t_{\text{Jitter}})) + \\ & \frac{r_{\text{Mes}} (n_{\text{Neg}} r_{\text{RefPos}} t_{\text{Neg}} V_{\text{refNeg}} + r_{\text{RefNeg}} (n_{\text{Pos}} t_{\text{Pos}} V_{\text{refPos}} + c_{\text{int}} r_{\text{RefPos}} \Delta v_{\text{ADC}})))}{r_{\text{RefNeg}} r_{\text{RefPos}} t_{\text{runup}}} /. \\ & \text{capacitor}; \\ & \{\text{NSolve}[\text{VerrJitter}[t_{\text{Jitter}}, 13] == 0.00000075, t_{\text{Jitter}}], \\ & \text{NSolve}[\text{VerrJitter}[t_{\text{Jitter}}, 13] == 0.0000001, t_{\text{Jitter}}]\} \\ & \{\{t_{\text{Jitter}} \rightarrow 6.22223 \times 10^{-11}\}, \{t_{\text{Jitter}} \rightarrow 8.2963 \times 10^{-12}\}\} \end{aligned}$$

Compute the required ADC resolution in noise-free counts to resolve the virtual runup signal to the desired digit counts.

$$\text{In[28]:= } \text{adc}_{\text{volts}} = \frac{-\text{vrunupFS}}{2\ 500\ 000}$$

$$\text{Out[28]= } \frac{1}{1250}$$

$$\text{In[29]:= } \text{adc}_{\text{counts}} = \frac{2 * \text{vsat}}{\text{adc}_{\text{volts}}}$$

$$\text{Out[29]= } 32\ 500$$

Add some margin

$$\text{In[31]:= } \text{adc}_{\text{realcounts}} = \text{adc}_{\text{counts}} * 1.5$$

$$\text{Out[31]= } 48\ 750.$$

$$\text{In[33]:= } \{2^{14}, 2^{16}, 2^{18}\}$$

$$\text{Out[33]= } \{16\ 384, 65\ 536, 262\ 144\}$$