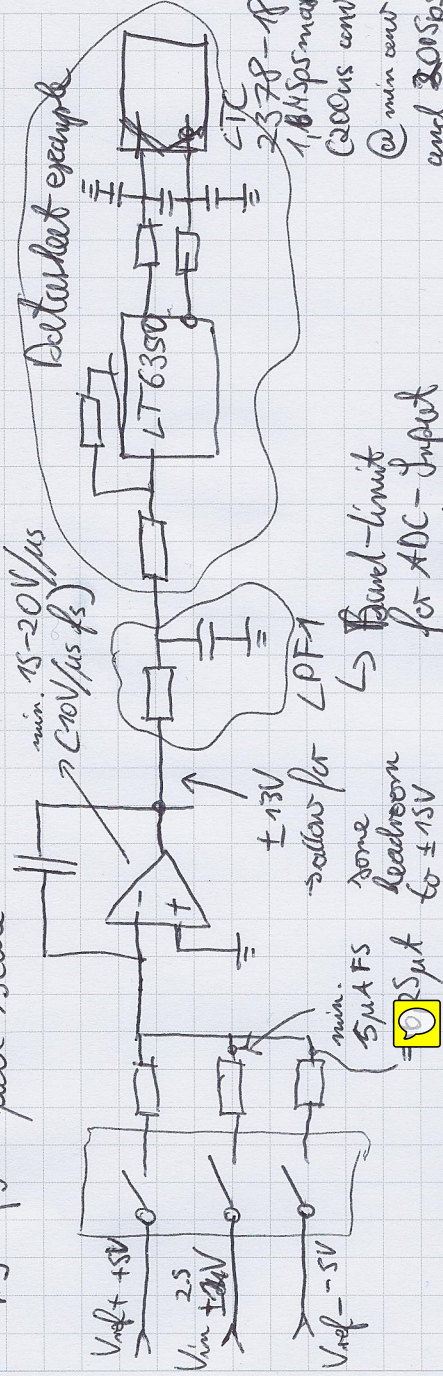


$F_S = F_S = \text{full-scale}$



### Operation:

- Use 34584 switching cycles for rampup

-  $V_{ref}$  slopes are 25% stronger than  $V_{in, max}$

@ Ramp-up to 1kV virtual integration:

$$\rightarrow 1kV / 2500000 = 0.0004V = 0.4\mu V \text{ required resolution of ADC}$$

$$\text{Rampup Time: } 1kV - FS \Rightarrow 10V/\mu s \Rightarrow 100\mu s$$

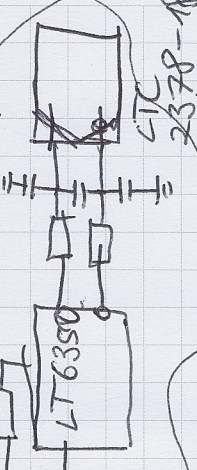
Theoretical Speed  $\Rightarrow 4kSps$  (estimate)

$$\hookrightarrow @ \pm 13V_{FS} \Rightarrow 32500 \text{ counts of ADC (noise free)} \Rightarrow 18 \text{ bit ADC}$$

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Disturbance example



LTC2378-18  
1.8kSps max.  
(2000us conv. time)  
@ min conv time  
and 200Sps  
 $\Rightarrow 100Sps$

Band-limit  
for ADC-Input  
@ 50kHz  
 $\Rightarrow$  Optional, if timing  
errors occur

Limit the final speed to 100Sps!