Utkarsh Upadhyaya | **183079019**
Electrical Engineering | **M.Tech.**
Indian Institute of Technology, Bombay | **Gender: Male**
Specialization: Microelectronics and VLSI | **DOB: 02-05-1995**

Examination	University	Institute	Year	CPI / %
Post Graduation	IIT Bombay	IIT Bombay	2021	9.49
Graduation	IIIT Delhi	Indraprastha Institute of Information Technology, Delhi	2017	7.89
Graduation Specialization: Electronics and Communication				

SCHOLASTIC ACHIEVEMENTS

- Achieved **99.46** percentile in EC-GATE examination, 2018 among **1,25,870** candidates. (*Feb'18*)
- Secured **AA** grade in all the courses in the first semester. (*Aug'18 - Nov'18*)

AREAS OF INTEREST

CMOS Analog VLSI Design, RF VLSI Design, Mixed Signal VLSI Design, Digital VLSI Design.

MAJOR PROJECT AND SEMINAR

- **M.Tech. RA work + M.Tech. thesis work:**
  A half-rate, 8-16 Gbps, 10:1 serializing transmitter in a SerDes system (*Dec'18 - Present*)
  Guide: *Prof. Shalabh Gupta, Electrical Engineering, IIT Bombay*
  Objectives:
  - Design an **8-16 Gbps**, NRZ 10:1 serializing transmitter (Tx) in CMOS 65 nm technology.
  - Achieve good channel performance of the Tx, with low jitter and discernible eye-opening at the output.

  Completed work:
  - Designed, laid-out different circuit blocks, and hence the serializing Tx.
  - Performed simulations across the PVT variants with the parasitics back-extracted.
  - Proposed an active inductive-peaking CTLE that obviates the need for an FFE for the targeted channel losses.
  - Simulation results articulated the good performance of the Tx with **0.36 UI**$_{PP}$ timing margin and **3.3 ps** rms jitter, at the bit error rate (BER) of $\mathbf{10^{-12}}$ for the channel loss of **17 dB** at the $f_{Nyquist}$ of **8 GHz**.
  - Contributed to the final integration of all the blocks, after which the chip was sent to the foundry for fabrication.

  Ongoing and future work:
  - Designing the PCBs, ensued by the test of the ICs.
  - Power reduction of the transmitter and optimization of the performance.

  A linear, quarter-rate PAM4 transmitter for high data rates (*Jun'20 - Present*)
  Guide: *Prof. Shalabh Gupta, Electrical Engineering, IIT Bombay*
  Objectives:
  - Target the data-rates from **50-112 Gbps**.
  - Achieve **RLM** $>$ **95** % and perform equalization for the channel losses up to **10 dB** at Nyquist frequency.
  - Achieve energy efficiency in compliance with the standards.
  - Avoid data corruption, clocks' duty-cycle, and quadrature-phase mismatches, using the delay calibration blocks.

  Completed work:
  - Reviewed the literature for various techniques to achieve the aforementioned targets.
  - Characterized the CMOS FDSOI 28 nm technology.

  Ongoing and future work:
  - Designing and simulating the circuits at the schematic level across the PVT variants.
  - Lay the design out and perform the post-layout simulations across the PVT variants.

  Testing of the procured 5 Gbps SerDes ICs (*Jun'20 - Present*)
  Guide: *Prof. Shalabh Gupta, Electrical Engineering, IIT Bombay*
  Completed work:
  - Designed PCBs using Altium to test the procured **5 Gbps** SerDes ICs, fabricated in CMOS 180 nm technology.

  Ongoing and future work:
  - DC characterization of the ICs.
  - Test the ICs to validate their performance.

- **M.Tech Seminar:**
  High-speed Pulse Amplitude Modulation-4 (PAM4) transmitter architectures (*Aug'19 - Nov'19*)
  Guide: *Prof. Shalabh Gupta, Electrical Engineering, IIT Bombay*
  - Reviewed state-of-the-art linear PAM4 Tx architectures that achieve high data-rates with equalization.
  - Explored different circuit techniques to achieve high linearity (better **RLM**) and equalization techniques.
  - The Tx with hybrid current-mode (CM)-voltage-mode (VM) driver based 4-tap FFE achieves appreciable linearity with RLM $>$ **94**%, and FoM of **2.6 pJ/bit**, operating at **45 Gbps**. (JSSC by Matteo Bassi).

PUBLICATIONS

- Utkarsh Upadhyaya, Souradip Sen, Sandeep Goyal, and Shalabh Gupta, "**A 16 Gbps 10:1 Serializer with Active Inductor Based CTLE for High Frequency Boosting**", submitted for review in **27^{th} IEEE International Conference on Electronics Circuits and Systems (ICECS'20)**.
- Souradip Sen, Utkarsh Upadhyaya, Krishna Reddy Kondreddy, Arun Goyal, Sandeep Goyal, and Shalabh Gupta, "**A Low Jitter Digital loop CDR Based 8-16 Gbps SerDes in 65 nm CMOS Technology**", submitted for review in **34^{th} International Conference on VLSI Design & the 20^{th} International Conference on Embedded Systems (VLSID'21)**.

KEY COURSE PROJECTS AND ASSIGNMENTS

- **A two-stage, Operational Transconductance Amplifier (OTA)** | *Prof. Rajesh Zele* (*Oct'18*)
  - Designed and laid-out a two-stage, miller compensated, OTA with single-ended output in CMOS 180 nm technology for the targeted specifications. The common-centroid technique was used for the layout.
  - Improved the ICMR by including a circuit that would not disturb the operating point of the OTA. Post-layout simulations were performed over the PVT variants to validate the performance.
- **A wide-band Low Noise Amplifier (LNA) with Noise and Distortion cancellation in CMOS 65 nm technology** | *Prof. Rajesh Zele* (*Feb'19*)
  - Optimized the design to achieve the targeted specs of voltage gain, S_{11}, Noise Figure (NF), and P_{DC}.
  - Evaluated the performance of the LNA at the schematic level and reported the results.
- **A double-balanced direct down conversion mixer in CMOS 65 nm technology** | *Prof. Rajesh Zele* (*Mar'19*)
  - Optimized the design to meet the target specifications of conversion gain, NF, IIP_3, P_{1dB}, and P_{DC}.
- **An narrow-band CS cascode LNA in CMOS 65 nm technology** | *Prof. Rajesh Zele* (*Mar'19*)
  - Optimized the design of a CS cascode LNA with **inductive degeneration**, to achieve the target specs of voltage gain, S_{11}, NF, IIP_3, P_{1dB}, and P_{DC} at the schematic level.
  - The LNA was laid-out, and the post-layout simulations were performed over the PVT variants.
- **A current-reuse LC-Voltage Controlled Oscillator (LC-VCO) and integration with a Phase Locked Loop (PLL) in CMOS 65 nm technology** | *Prof. Rajesh Zele* (*Apr'19*)
  - Optimized the VCO design to meet the target specs of the tuning range, phase noise, VCO gain, and peak-to-peak swing with discrete coarse-fine tuning. Post-layout simulations were performed over the PVT.
  - Implemented a system-level integer-N, type-2 PLL using the LC-VCO designed.
- **A 6-bit, first-order discrete-time Delta-Sigma Modulator (DSM) in CMOS 45 nm technology** | *Prof. Maryam S. Baghini* (*Feb'20*)
  - Designed the forward-euler SC integrator, an MSB comparator, and the whole DSM loop, maintaining stability.
  - Passed the DSM output through a moving average filter implemented in MATLAB for further calculations.
  - Optimized the design for the Over-Sampling Ratio (OSR) of **64**, the sampling frequency of **640 MHz**, and achieved the resolution (ENOB) $>$ **6 bits**, SQNR of **48.96 dB**, SINAD of **42.96 dB**, and THD of **-44.2 dB**.
- **A digital Low Dropout Regulator (LDO) in CMOS 45 nm technology** | *Prof. Maryam S. Baghini* (*Mar'20*)
  - Designed a comparator, shift register, transistor array, and the whole LDO.
  - Optimized the design for the voltage conversion from **0.65 V to 0.6 V** with output ripples $<$ the max of **5 mV**$_{PP}$, for an I_{LOAD} of **200 μA**, f_{clock} of **10 MHz**, and C_L of **100 nF**, while evaluating for different $I_{LOAD}s$.

SELF PROJECT

A 3-bit, mod-3, CIFB continuous-time $\Delta - \Sigma$ modulator in CMOS 45 nm technology (*Aug'20*)

- Designed a comparator, Flash ADC, thermometer coded current-steering DAC for the final mod-3, CIFB CT-DSM, followed by optimization, and performed the simulations.

RELEVANT COURSES

- CMOS Analog VLSI Design
- RF Microelectronics Chip Design
- Mixed Signal VLSI Design
- VLSI Design
- VLSI Design Lab
- Processor Design
- Delta Sigma Data Converters
- Solid State Devices
- Microelectronics Simulation Lab

TECHNICAL SKILLS

Languages : Python, MATLAB, VHDL, Verilog, VerilogA.
Tools : Cadence Virtuoso, Sentarus TCAD, Altera Quartus II, ModelSim.

POSITIONS OF RESPONSIBILITY

- **Research Assistant, Communication Lab, IIT Bombay** (*Jul'18 - Present*)
  - Work as a team player in carrying out research in the lab.
  - Responsible for maintaining a record of the experimental components in the lab and scheduling experiments.
- **Volunteering in International Microwave and RF Conference (IMaRC), 2019 at IIT Bombay** (*Dec'19*)
  - Assisted the participants and ensured the smooth conduction of the three-day-long conference.
- **Academic Unit Representative of Academic Affairs (AURAA), Dept. of EE** (*Jul'20 - Present*)
  - Deal with the M.Tech. students' academic and non-academic issues.
  - Organize workshops, seminars, outreach programs, and talks by the researchers, professors, and alumni at the departmental and institute level to foster great learning.

CO & EXTRA CURRICULAR ACTIVITIES

- Participated in National Science, Cyber, and Maths Olympiads at various levels in school. (*2006-07*)
- Community work at Udayan Care. (*2015*)
- Hobbies: Cooking, Badminton, Swimming, Reading books.

Scholastic achievements and extracurricular activities are not verified by the Placement Cell