孙永帅

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教育经历

上海交通大学 上海
微电子科学与工程 本科 电子信息与电气工程学院 2015年9月 - 2019年6月

- GPA： 3.8 / 4.3（前15%）
- 奖项：国家励志奖学金、全国电子设计大赛上海赛区三等奖、上海交通大学优秀奖学金
- 荣誉：上海市优秀毕业生、上海交通大学三好学生、上海交通大学优秀团员

专业技能

- 操作系统：熟练使用**Linux**系统，基于Linux开发
- 程序设计：熟练使用**C**语言，可使用**C++**完成应用开发
- 脚本工具：熟练使用**Python**，熟悉**Make/Bash**脚本
- 版本控制：熟练使用**Git**版本控制
- FPGA：熟悉**FPGA**的设计，基于**Vivado**工具开发
- 硬件设计：熟练使用**Verilog HDL**，熟练使用**Modelsim**, 熟悉**Synopsys DC/ICC**等工具
- 计算机结构：熟悉**MIPS/RISC-V**等指令集
- 机器学习：熟悉**CNN**基本流程，掌握**Matlab/TensorFlow**等工具和框架

科研经历

基于CNN的肺结节识别 上海
上海交通大学 2018年6月 - 2018年7月

- 基于MATLAB，使用DeepLearningToolBox完成图片数据的处理和基本CNN结构的搭建
- 基于TensorFlow，使用Keras框架完成CNN结构，并基于数据集完成训练
- 尝试不同结构CNN，达到识别正确率的要求

全国电子设计大赛 上海
组长 2017年6月 - 2017年9月

- 带领小组完成四旋翼飞行器的搭建和自主控制
- OV摄像头、2.4G通讯模组、陀螺仪等的开发使用
- 基于MCU实现PID控制算法的移植和优化
- 图像识别轨迹算法实现和优化

基于FPGA的UART通讯接口实现 上海
上海交通大学 2017年2月 - 2017年7月

- 使用Verilog实现UART通讯的接收与发送，包括时序、缓存、控制模块等
- 在Altera FPGA Cyclone IV平台完成验证
- 实现与计算机串口的9600/115200波特率通讯

开源项目及作品

SunSpice-电路仿真工具设计实现
2018年3月 - 2018年7月
项目简介：基于Python设计，实现文本电路的解析和DC\AC\Tran仿真，并完成时域\频域的仿真图形
项目地址：https://github.com/SunicYosen/SunSpice

2D-IDCT Design for HEVC
2018年2月 - 2018年4月
项目简介：基于Verilog HDL设计实现面向HEVC的IDCT计算单元，实现4*4/8*8兼容，并使用DC/ICC综合实现
项目地址：https://github.com/SunicYosen/IDCT

Linux下基于ELF病毒的键盘输入窃取
2017年9月 - 2017年12月
项目简介：基于Linux操作系统，通过实现root权限获取、ELF感染实现键盘输入的窃取和发送，并完成窃取程序进程的隐藏
项目地址：https://github.com/SunicYosen/Rotanimret

其他

- **证书** 电子商务师三级(高级)
- **兴趣爱好：** 乒乓球、足球

Yongshuai Sun

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EDUCATION

Shanghai Jiao Tong University *Sep 2015 - Jun 2019*
B.E. School of Electronic Information and Electrical Engineering *Shanghai*

- GPA: 3.8 / 4.3 (top 15%)
- Award: National Inspirational Scholarship, Third Prize of National Students Electronic Design Competition in Shanghai, Shanghai Jiaotong University Excellent Scholarship
- Honor: Shanghai Outstanding Graduates, Three Good Students of Shanghai Jiaotong University

SKILLS LIST

- Operating system: Skilled in using **Linux** system, based on Linux development
- Programming: Skilled in **C** language, and use **C++** to complete application development
- Scripting Tools: Familiar with **Python**, familiar with **Make/Bash** scripts
- Version Control: Skilled in using **Git** version control
- FPGA: Familiar with **FPGA** design, based on **Vivado** tool development
- Hardware design: Familiar with **Verilog HDL**, familiar with **Modelsim**, familiar with **Synopsys DC/ICC** tools
- Computer structure: Familiar with instruction set such as **MIPS/RISC-V**
- Machine Learning: Get familiar with the basic process of **CNN** and master tools and frameworks like **Matlab/TensorFlow**

RESEARCH EXPERIENCE

CNN-based lung nodule recognition *Jun 2018 - Jul 2018*
Shanghai Jiaotong University *Shanghai*

- Based on MATLAB, use DeepLearningToolBox to complete image data processing and basic CNN structure construction
- Based on TensorFlow, use the Keras framework to complete the CNN structure and complete training based on the data set
- Try different structures of CNN to meet the requirements for identifying correct rates

National Student Electronic Design Competition *Jun 2017 - Sep 2017*
Team leader *Shanghai*

- Lead the team to complete the construction and autonomous control of the quadrotor
- Development of OV camera, 2.4G communication module, gyroscope, etc.
- Transplant and optimization of PID control algorithm based on MCU
- Image recognition trajectory algorithm implementation and optimization

FPGA-based UART communication interface implementation *Feb 2017 - Jul 2017*
Shanghai Jiaotong University *Shanghai*

- Using Verilog to receive and send UART communication, including timing, buffer, control module, etc.
- Verification on Altera FPGA Cyclone IV Platform
- Communicate with the 9200/115200 baud rate of the computer serial port

PROJECT EXPERIENCE

SunSpice-Circuit Simulation Tool Design Implementation *Mar 2018 - Jul 2018*

Project Description: Based on Python design, realize text circuit parsing and DC\AC\Tran simulation, and complete time domain\frequency domain simulation graphics

Project address: https://github.com/SunicYosen/SunSpice

Electronic ELF virus-based keyboard input stealing *Sep 2017 - Dec 2017*

Project Description: Based on the Linux operating system, realize the stealing and sending of keyboard input by implementing root access and ELF infection, and complete the hidden process of stealing programs

Project address: https://github.com/SunicYosen/Rotanimret

2D-IDCT Design for HEVC *Sep 2017 - Dec 2017*

Project Description: Designed to implement HEVC-based IDCT computing unit based on Verilog HDL, 4*4/8*8 compatible, and integrated using DC/ICC

Project address: https://github.com/SunicYosen/IDCT

MISCELLANEOUS

- **CERTIFICATE** E-Commerce Level 3 (Advanced)