National University of Computer & Emerging Sciences, Karachi
FAST School of Computing
Spring 2022

Course Code: CS2006	Course Name: Operating Systems
Instructor Name: Anaum Hamid	Issue Date: 16th May 2022
Assignment no. 03	Due Date: 20th May 2022

Instructions:

- Assignment should be solved handwritten on paper and their scanned soft copies are to be submitted on GCR.
- Must write your NU id on the top of each page of the assignment.
- Rought work must be solved for the clarification of the answer.
- Prints of Soft copy documented assignment cost direct zero.

All questions have equal marks (5 Each) - Total Marks-40 Marks

Memory Management

1. A paging scheme uses a Translation Lookaside Buffer (TLB). The effective memory access takes 150 ns, and the main memory access takes 100 ns. What is the **TLB access time** (in ns) if the TLB hit ratio is 70% and there is no page fault?
2. Consider a **two-level paging scheme** with a TLB. Assume no page fault occurs. It takes 25 ns to search the TLB and 100 ns to access the physical memory. If TLB hit ratio is 75%, What will be its **EAT**??
3. Consider a **three-level paging scheme** with a TLB. Assume no page fault occurs. It takes 30 ns to search the TLB and 100 ns to access the physical memory. If TLB hit ratio is 70%, What will be its **EAT**??
4. Consider a demand-paging system with a paging disk that has average access and transfer time of 25 milliseconds. Addresses are translated through a page table in the main memory, with an access time of 1 microsecond per memory access. Thus, each memory reference through the page table takes two accesses. To improve this time, we have added an associative memory that reduces access time to one memory reference if the page-table entry is in the associative memory. Assume that 80 percent of the accesses are in the associative memory and that, of those remaining, 10 percent (or 2 percent of the total) cause page faults. What is the effective memory access time in milliseconds?

Paging

1. Calculate the size of memory if its address consists of 22 bits and the memory is 2-byte addressable.
2. Calculate the number of bits required in the address for a memory having a size of 16 GB. Assume the memory is 4-byte addressable.
3. Consider a system with byte-addressable memory, 32-bit logical addresses, 4-kilobyte page size, and page table entries of 4 bytes each. Calculate the page table size in the system.

Page Replacement Algorithm

Consider the following page reference string:

5, 0, 1, 2, 9, 0, 5, 0, 4, 2, 5, 0, 5, 0, 5, 2, 1, 2, 0, 1, 9, 0, 1

Assuming demand paging with three frames and all frames are initially empty. Hence, allocation of the first unique pages will cost one fault each. Calculate fault ratio by Second Chance Algorithm?

**********End**********