ORDER NO. AVS9602118C8

Service Manual

Digital AV Mixer WJ-AVE55



SPECIFICATIONS

Source Input: x4 (SOURCE 1/4)

Video Input : $1.0 \text{ Vp-p/75}\Omega \text{ PAL composite signal, pin-jack}$

Y/C input: Y signal : 1.0 V[p-p]/75Ω, C signal : 0.3 V[p-p]/75Ω Mini Din 4-pin connector

Audio Input : $-6 \text{ dBs } 20 \text{ k}\Omega \text{ pin jack (L/R)}$

Character Input: x1 (TITLE); 10-pin connector for optional Character Generator WJ-TTL7

Recording Output: x1 (REC OUT)

Video Output : 1.0 Vp-p/75Ω PAL Composite signal, pin-jacks

Y/C Output: Y signal; 1.0 V[p-p]/75Ω, C signal; 0.3 V[p-p]/75Ω Mini Din 4-pin connector

Audio Output : $-6 \text{ dBV/1 k}\Omega$, pin jacks (L/R)

Preview Output:

Video Output : 1.0 Vp-p/75Ω PAL Composite signal, pin-jacks

Back Colour : White, Yellow, Cyan, Green, Magenta, Red, Blue, Black and Useable

Wipe Patterns: 157 patterns

Video Gain: Unity

S/N (typical): Video 50 dB (composite), 50 dB (Y/C)

Audio; 60 dB

Power Source : 220 - 240V AC, 50 Hz

Power Consumption : Approx 19W

Ambient Operating Temperature: 0°C - 40°C (32°F - 104°F)

Ambient Operating Humidity: Less than 90%

Dimensions: 420 (W) x 300 (H) x 88 (D) mm

Weight: 2.5 kg

Weight and dimensions indicated above are approximate. Specifications are subject to change without notice.

Panasonic

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⚠ WARNING

This service information is designed for experienced repair technicians only and is not designed for use by the general public.

It does not contain warnings or cautions to advise non-technical individuals of potential dangers in attempting to service a product.

Products powered by electricity should be serviced or repaired only by experienced professional technicians. Any attempt to service or repair the product or products dealt with in this service information by anyone else could result in serious injury or death.



PERSONNEL.



This symbol warns the user that uninsulated voltage within the unit may have sufficient magnitude to cause electric shock. Therefore, it is dangerous to make any kind of contact with any inside part of this unit.



This symbol alerts the user that impotant literature concerning the operation and maintenance of this has been included. Therefore, it should be read carefully in order to avoid any problems.

IMPORTANT SAFETY NOTICE

There are special components used in this equipment which are important for safety. These parts are indicated by the "\Delta" mark on the schematic diagram and the replacement parts list. It is essential that these critical parts should be replaced with manufacturer's specified parts to prevent shock, fire, or other hazards.

Do not modify the original design without permission of manufacture.

Standard Accessory

Optional Accessory

Power Cord 1 pc.

Character Generator

WJ-TTL7

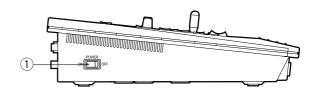
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MAJOR OPERATING CONTROLS AND THEIR FUNCTIONS

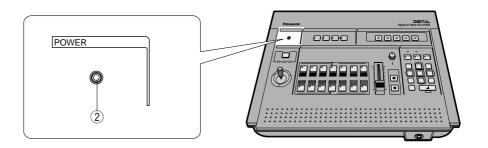
■ Side View ¬

(1) Power Switch (POWER ON/OFF)

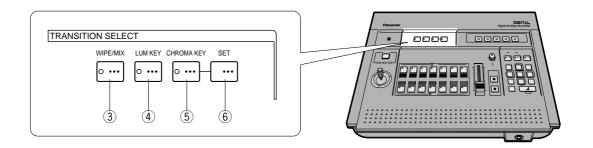


■ POWER Section

(2) Power Indicator



■ TRANSITION SELECT Section



(3) Wipe / Mix Selection Button (WIPE/MIX)

Used to select either the Wipe or Mix Effect.

Lighting: shows the Wipe selection

Blinking: shows the Mix selection

(4) Luminance Key Button

Used to replace certain luminance of one picture with a second picture.

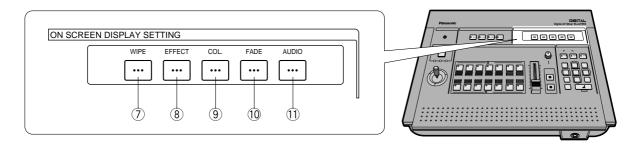
(5) Chroma Key Button

Used to replace certain colour of one picture with a second picture.

(6) Set Button

Used to select the position for the chroma function.

■ ON SCREEN DISPLAY SETTING Section



(7) Wipe Button (WIPE)

Used to display the Wipe menu on the preview monitor.

(8) Effect Button (EFFECT)

Used to display the Effect Setting menu on the preview monitor.

(9) Colour Button (COL.)

Used to select the colour for the back screen or wipe edge.

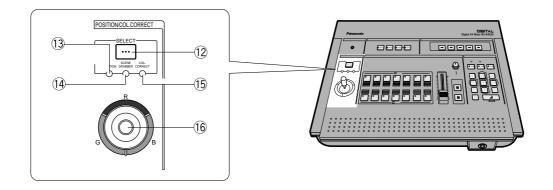
(10) Fade Button (FADE)

Used to display the Fade Setting menu on the preview monitor.

(11) Audio Button (AUDIO)

Used to display the Audio Setting menu on the preview monitor.

■ POSITION/COL. CORRECT Section



(12) Select Button (SELECT)

Used to select the POSITION, SCENE GRABBER or COL CORRECT.

Notes:

- 1. Scene Grabber is available in pattern.
- 2. When selecting the CHROMA ON mode and press the desired Effect Output Button, colour correction is available.

(13) Position Indicator (POSITION)

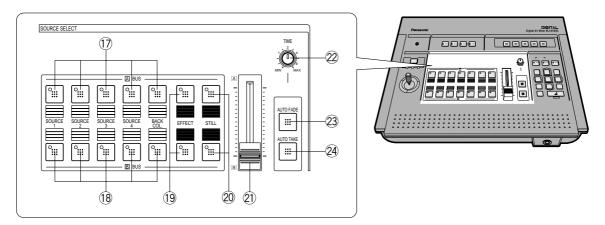
(14) Scene Grabber Indicator (SCENE. GRA.)

(15) Colour Correct Indicator (COL CORRECT)

(16) Joystick Control

This joystick Control has two functions - setting the position of the specified wipe pattern , moving the cursor for setting the chroma key and correcting the Colour A-bus / B-bus.

■ SOURCE SELECT Section



(17) A-bus Selection Buttons (A)

SOURCE 1: Used to select Source 1 Audio/Video Signals (35)(36)(37) supplied to the rear panel.

SOURCE 2: Used to select Source 2 Audio/Video Signals (38)(39)(40) supplied to the rear panel.

SOURCE 3: Used to select Source 3 Audio/Video Signals (41)(42)(43) supplied to the rear panel.

SOURCE 4: Used to select Source 4 Audio/Video Signals (44)(45)(46) supplied to the rear panel.

BACK COL: Used to select the Back Colour.

(18) B-bus Selection Buttons

Same selection can be available as mentioned in the Abus Selection buttons (17).

(19) Effect Out Buttons (EFFECT)

Used to supply the effect signal to the preview and Rec Out connectors.

(20) Still Out Buttons (STILL)

An instant still or frozen image can be obtained by pressing this button.

(21) Mix/Wipe Control (MIX WIPE EFFECT)

Mix and wipe can be performed by operating this control.

(22) Time Control (TIME)

For adjusting the transition time of Auto Fade Function and Auto Take Function.

(23) Auto Fade Button (AUTO FADE)

Automatic fade can be executed according to the time set by TIME Control.

(24) Auto Take Button (AUTO TAKE)

Automatic wipe or mix can be executed according to the time set by TIME Control (22).

■ MODE SETTING Section

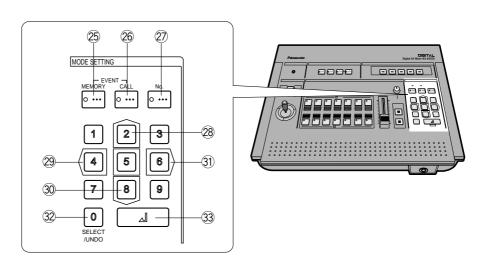
(25) Event Memory Button (EVENT MEMORY)

Used to memorize the present status.

(26) Call Button (CALL)

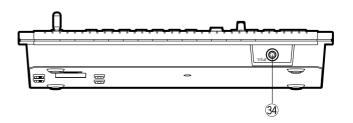
Used to recall the memorized status.

- (27) Number Button (No.)
- (28) Up Button
- (29) Left Button
- (30) Down Button
- (31) Right Button
- (32) SELECT/UNDO Button
- (33) Enter Button (🕹)

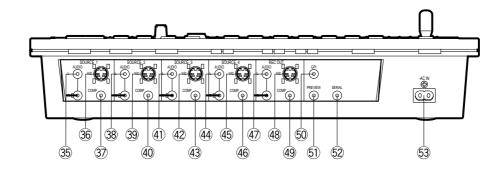


■ Front Panel -

(34) Titler Connector (TITLE)



■ Rear Panel



- (35) Source 1 Audio Input Jack (SOURCE 1 AUDIO)
- (36) Source 1 S-video Input Connector (Y/C)
- (37) Source 1 Composite Video Signal Input Jack
- (38) Source 2 Audio Input Jack (SOURCE 2 AUDIO)
- (39) Source 2 S-video Input Connector (Y/C)
- (40) Source 2 Composite Video Signal Input Jack
- (41) Source 3 Audio Input Jack (SOURCE 3 AUDIO)
- (42) Source 3 S-video Input Connector (Y/C)
- (43) Source 3 Composite Video Signal Input Jack
- (44) Source 4 Audio Input Jack (SOURCE 4 AUDIO)
- (45) Source 4 S-video Input Connector (Y/C)

- (46) Source 4 Composite Video Signal Input Jack
- (47) Recording Out Audio Output Jack (REC OUT AUDIO)
- (48) Recording Out S-video Output Connector (REC OUT Y/C)
- (49) Recording Out Composite Video Signal Output Jack
- (50) GPI Connector (GPI)

Refer to the qualified service personnel or system Installers for this connection.

(51) Preview Output Connector

Connect to video input connector of the preview monitor

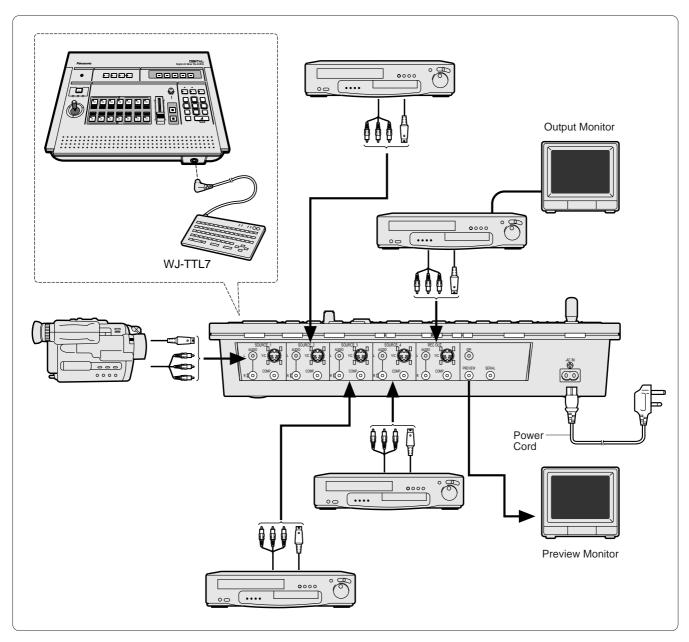
(52) Serial Connector (SERIAL)

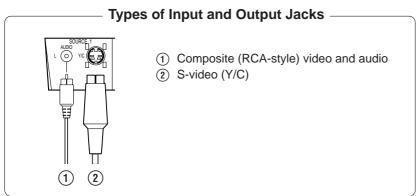
Refer to the qualified service personnel or system Installers for this connection.

(53) Power Socket (AC IN)

Connect the Power Cord (provided) to this socket.

SYSTEM CONNECTION





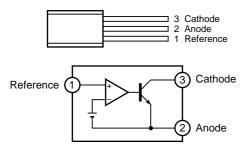
CIRCUIT DESCRIPTION

IC Description

1. Power Board

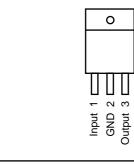
1.1. IC2 on the Power Board is using the Variable Shunt Regulator IC YWTA76431S.

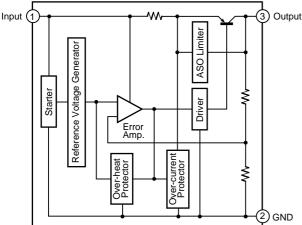
Description of this IC is as follows:



1.2. IC1 on the Power Board is using the-3-terminal Voltage Regulator IC YWUPC24M12HF.

Description of this IC is as follows:

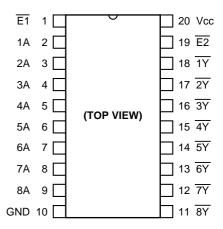




2. Main Board

2.1. IC1 on the Main Board is using the Octal 3-State Bus Buffers IC MC74HC541AF.

Description of this IC is as follows:



Truth Table

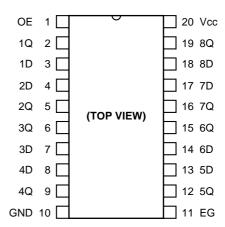
INPL	JTS	OUTPUT
l ₁	E2	Y
L	L	A
Ι	*	7
*	Н	

* : Don't care.

Z: High Impedance

2.2. IC6 and IC7 on the Main Board are using the Octal 3-State D-FFs IC MC74HC374AF.

Description of this IC is as follows:

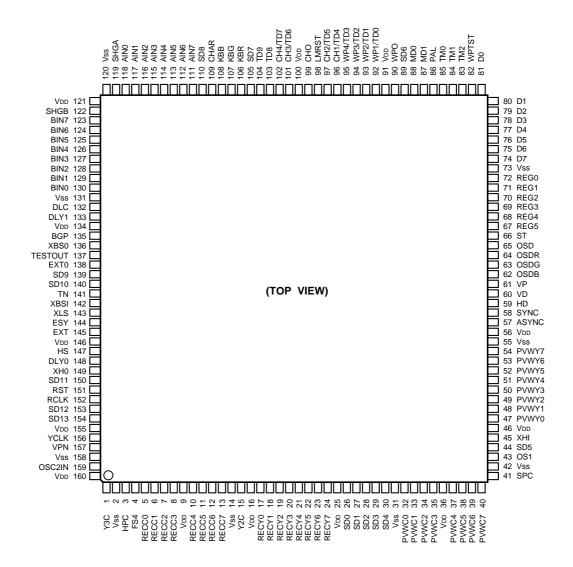


Truth Table

INP	JTS	FUNCTION
OE	EG	FUNCTION
*	L	Latch
*	Н	Q = D
Н	*	Z

* : Don't care. Z : High Impedance

2.3. IC62 on the Main Board is using the 2-D Low Pass Filter HCMOS Gate Array Logic IC YWAJ0016. Description of this IC is as follows:



Pin	Name	I/O	Description
1	Y3C	0	Y3C signal output terminal.
2	Vss	-	Ground terminal.
3	HPC	0	HPC signal output terminal.
4	FS4	0	FS4 signal output terminal.
5	RECC0	0	
6	RECC1	0	REC(C) signal output terminals.
7	RECC2	0	TCEO(O) Signal output terminals.
8	RECC3	0	
9	VDD	_	Power supply terminal.
10	RECC4	0	
11	RECC5	0	DEC(C) signal cutaut terminals
12	RECC6	0	REC(C) signal output terminals.
13	RECC7	0	
14	Vss	_	Ground terminal.
15	Y2C	0	Y2C signal output terminal.

Pin	Name	I/O	Description
16	VDD	_	Power supply terminal.
17	RECY0	0	
18	RECY1	0	
19	RECY2	0	
20	RECY3	0	REC(Y) signal output terminals.
21	RECY4	0	NEO(1) signal output terminals.
22	RECY5	0	
23	RECY6	0	
24	RECY7	0	
25	VDD	-	Power supply terminal.
26	SD0	Ι	
27	SD1	Π	
28	SD2	Ι	SD signal input terminals.
29	SD3	Ī	
30	SD4	Ī	
31	Vss	_	Ground terminal.

Pin	Name	I/O	Description	
32	PVWC0	0	·	
33	PVWC1	0	Draviauv(C) aigraal autout tamainala	
34	PVWC2	0	Preview(C) signal output terminals.	
35	PVWC3	0		
36	Vss	_	Ground terminal.	
37	PVWC4	0		
38	PVWC5	0		
39	PVWC6	0	Preview(C) signal output terminals.	
40	PVWC7	0		
41	SPC	0	SPC signal output terminal.	
42	Vdd	_	Power supply terminal.	
43	OS1I	Т	OS signal input terminal	
44	SD5	Τ	SD signal input terminal.	
45	XHI	Τ	XH signal input terminal.	
46	Vdd	_	Power supply terminal.	
47	PVWY0	0		
48	PVWY1	0		
49	PVWY2	0		
50	PVWY3	0		
51	PVWY4	0	Preview(Y) signal output terminals.	
52	PVWY5	0		
53	PVWY6	0		
54	PVWY7	0		
55	Vss	_	Ground terminal.	
56	Vdd	1	Power supply terminal.	
57	ASY	0	ASY signal output minals	
58	SYC	0	SYC signal output terminas.	
	HD	0	HD signal output terminal.	
60	VD	0	VD signal output terminal.	
61	VP	0	VP signal output terminals.	
62		ı	OSDB signal input terminal.	
	OSDG	1	OSDG signal input terminal.	
	OSDR	1	OSDR signal input terminal	
	OSD	Ш	OSD signal input terminal.	
66			Strobe signal input terminal.	
67				
	REG4			
	REG3	1	Register signal input terminals.	
	REG2	1		
	REG1			
72				
73			Ground terminal.	
	DATA7	<u> </u>		
	DATA6			
	DATA5	<u> </u>	.	
	DATA4	<u> </u>	DATA signal input terminals.	
	DATA3	<u> </u>		
	DATA2	<u> </u>		
80		<u> </u>		
81	DATA0			

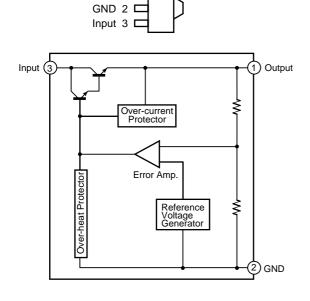
Pin	Name	I/O	Description	
	WPTST	ı, O	WPTST signal input terminal.	
-	TM2	Ė	vvi 101 digital impat terrimia.	
	TM1	Ť	TM signal input terminals.	
	TMO	Ė	· · · · o.g. · a. · · · · p a. · · o · · · · · · · a. · ·	
—	PAL	İ	PAL signal input terminal.	
-	MD1	Ī		
88	MD0	ı	MD signal input terminals.	
89	SD6	Ι	SD signal input terminal.	
90	СНОВ	0	CHOB signal output terminal.	
91	VDD	_	Power supply terminal.	
92	WP1/TD0	Ι		
93	WP2/TD1	I		
94	WP3/TD2	Ι		
95	WP4/TD3	I	TD signal input terminals.	
96	CH1/TD4	I		
97	CH2/TD5	I		
98	LMRST	0	LMRST signal output terminal.	
99	CHOA	0	CHOA signal output terminal.	
100	VDD	-	Ground terminal.	
101	CH3/TD6	I		
102	CH4/TD7	I	TD signal input terminals.	
103	TD8	Ι	10 signal input terminals.	
104	TD9	ı		
105	SD7	I	SD signal input treminal.	
106	KBR	Ι	Red signal input terminal.	
107	KBG	Ι	Green signal input terminal.	
108	KBB	ı	Blue signal input terminal.	
109	CHAR	ı	Character signal input terminal.	
110	SD8	I	SD signal input terminal.	
111	AIN7	Ι		
-	AIN6	Ι		
	AIN5	ı		
-	AIN4	Ι		
_	AIN3	ı	A signal input terminals.	
	AIN2	I		
_	AIN1	I		
	AIN0	Ι		
-	SHGA	ı	SHGA signal input treminal.	
	Vss	_	Ground terminal.	
	VDD	I	Power supply terminal.	
	SHGB	<u> </u>	SHGB signal input terminal.	
	BIN7	ı		
	BIN6	I		
	BIN5	I		
	BIN4	1	B signal input terminals.	
-	BIN5	I	_ 5.3 par to	
	BIN2	I	_	
	BIN1	ı		
_	BIN0	I		
131	Vss	_	Ground terminal.	

Pin	Name	I/O	Description
132	DLC	0	DLC signal output terminal.
133	DLY1	0	DLY1 signal output terminal.
134	VDD	1	Power supply terminal.
135	BGP	0	Burst Gate Pulse output terminal.
136	XBSO	0	XBSO signal output terminal.
137	TESTOUT	0	TEST signal output terminal.
138	EXT0	0	External signal output terminal.
139	SD9	ı	SD Data input terminals
140	SD10		SD Data input terminals.
141	TN	Ι	TN signal input terminal.
142	XBSI	Π	XBSI signal input terminal.
143	XLS	Ι	XLS signal input terminal.
144	XSY	Ι	XSY signal input terminal.
145	EXT	Ι	External signal input terminal.
146	VDD	_	Power supply terminal.
147	HS	0	HS signal output terminal.
148	DLY0	ı	DLY0 signal input terminal.
149	XH0	0	XH signal output terminal.
150	SD11	Ι	SD signal input terminals.
151	RST	Ι	RST signal input terminal.
152	RCLK	Ι	Clock pulse input terminal.
153	SD12	I	CD Data input to main als
154	SD13	_	SD Data input terminals.
155	VDD	_	Power supply terminal.
156	YCLK	0	Clock pulse output terminal.
157	VPN	0	VPN signal output terminal.
158	Vss	_	Ground terminal.
159	OS2I	I	Oscillation signal input terminal.
160	VDD	_	Power supply terminal.

2.4. IC64 on the Main Board is using the 3-Terminal Voltage Regulator IC YW78L09UATE2.

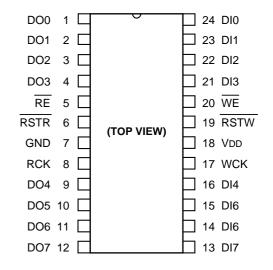
Description of these IC is as follows:

Output 1 □



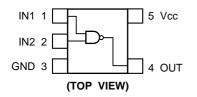
2.5. IC28, IC42 and IC59 on the Main Board are using the PAL 1,135-word x 8-Bit FIFO High Speed Line Buffers IC YWUPD42102G3.

Description of this IC is as follows:



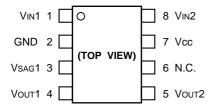
Pin	Name	I/O	Description		
1	DO0	0			
2	DO1	0	Data author tarminala (9 Bit)		
3	DO2	0	Data output terminals. (8-Bit)		
4	DO3	0			
5	RE	I	Read Enable signal input terminal.		
6	RSTR	Ι	Reset Read pulse input terminal.		
7	GND	_	Ground terminal.		
8	RCK	I	Read Clock pulse input terminal.		
9	DO4	0			
10	DO5	0	Data output terminals (9 Bit)		
11	DO6	0	Data output terminals. (8-Bit)		
12	DO7	0			
13	DI7	Ι			
14	DI6	I	Data input terminals. (8-Bit)		
15	DI5	Ι	Data input terminais. (6-bit)		
16	DI4	I			
17	WCK	Ι	Write Clock pulse input terminal.		
18	Vdd	_	Power supply terminal.		
19	RSTW	I	Reset Write Pulse input terminal.		
20	WE	Ι	Write Enable signal input terminal.		
21	DI3	Ι			
22	DI2	I	Data input terminals (9 Pit)		
23	DI1	I	Data input terminals. (8-Bit)		
24	DI0	I			

2.6. IC12, IC47, IC49, and IC50 on the Main Board are using the Single 2-Input AND Gate IC YWSC7S08F. Description of this IC is as follows:

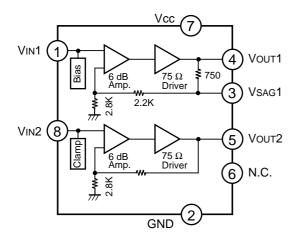


Tru	Truth Table				
Inp	uts	Output			
IN1	IN2	Output			
L	ш	Ι			
Н	ш	Η			
L	I	I			
Н	Η	L			

2.7. IC14 on the Main Board is using the Dual 6dB Video Amplifier IC with 75Ω Driver YWNJM2268V. Description of this IC is as follows:

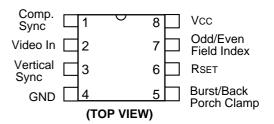


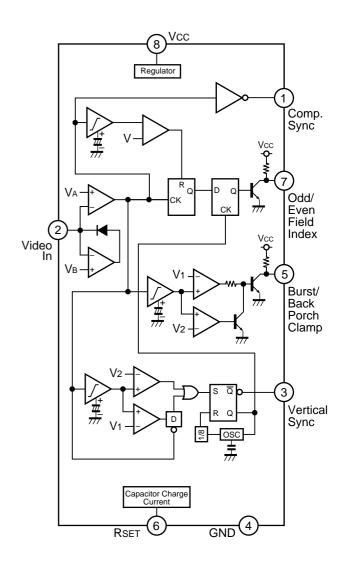
Pin	Name	I/O	Description	
1	Vin1	Ι	Input terminal for Amplifier 1.	
2	GND	_	Ground terminal.	
3	Vsag1	_	Sag compensation terminal for Amplifier 1.	
4	Vour1	0	Output terminal for Amplifier 1.	
5	Vout2	0	Output terminal for Amplifier 2.	
6	N.C.	_	Non connection.	
7	Vcc	_	Power supply terminal.	
8	VIN2	Ι	Input terminal for Amplifier 2.	



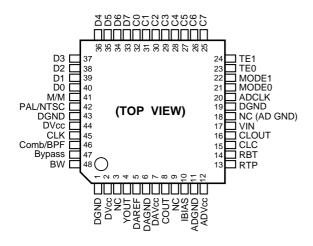
2.8. IC511 and IC512 on the Main Board are using the Video Sync. Separator IC YWLM1881M.

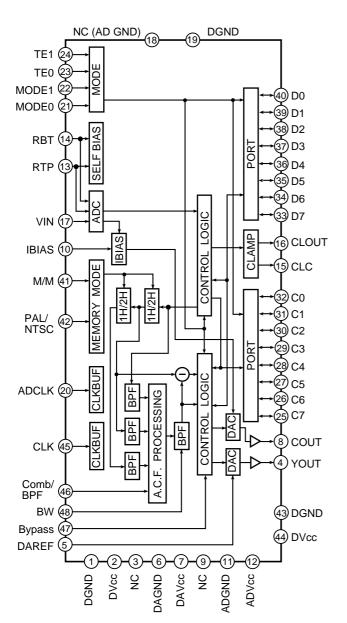
Description of this IC is as follows:





2.9. IC26 and IC40 on the Main Board are using the Comb/BPF Filter IC YWMC141625BFU. Description of this IC is as follows:



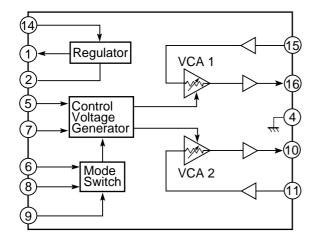


Pin	Name	I/O	Description	
1	DGND	_	Ground terminal for Digital Circuit.	
2	DVCC	_	+5V supply terminal for Digital Circuit.	
3	N.C.	_	Non Connection.	
4	YOUT	0	Luminance signal output terminal.	
5	DAREF	I	Reference Voltage input terminal for D/A Converter circuit.	
6	DAGND	_	Ground terminal for D/A Converter Circuit.	
7	DAVCC	-	+5V supply terminal for D/A Converter Circuit.	
8	COUT	0	Chroma signal output terminal.	
9	N.C.	_	Non Connection.	
10	IBIAS	I	Current Control terminal for A/D and D/A Coverter Circuits.	
11	ADGND	-	Ground terminal for A/D Converter Circuit.	
12	ADVCC	-	+5V supply terminal for A/D Converter Circuit.	
13	RTP	I	Top Reference Voltage input terminal for A/D Converter Circuit.	
14	RBT	I	Bottom Reference Voltage input terminal for A/D Converter Circuit.	
15	CLC	I	Clamp Time Constant setting terminal.	
16	CLOUT	0	Clamp Voltage output terminal.	
17	VIN	I	Voltage input terminal for A/D Converter Circuit; 3.3Vp-p max.	
18	N.C.	_	Non Connection.	
19	DGND	-	Ground terminal for Digital Circuit.	
20	ADCLK	I	Clock pulse input terminal for A/D Converter Circuit.	
21	MODE0	I		
22	MODE1	I	Mode set signal input terminals.	
23	TE0	I	Test Mode set signal input	
24	TE1	I	terminals.	
25	C7	I/O	Data(Y) input/output terminals.	
26	C6	I/O		

Pin	Name	I/O	Description			
33	D7	I/O				
34	D6	I/O	Chrominance Data input/output			
35	D5	I/O				
36	D4	I/O				
37	D3	I/O	terminals.			
38	D2	I/O				
39	D1	I/O				
40	D0	I/O				
41	N/M	I	Colour TV Sytem Select signal input terminals.			
42	PAL/NTSC	ı	N/M PAL/NTSC SYSTEM			
			L L PALB, G, H, I			
			L L NTSC			
			H H PALN			
			H H PALM			
43	DGND	_	Ground terminal for Digital Circuit.			
44	DVcc	-	+5V supply terminal for Digital Circuit.			
45	CLK	I	Clock Pulse input terminal.			
46	COMB/BPF	I	Filter Select signal input terminal. L: Comb Filter; H: Band Pass Filter			
47	BYPASS	I	Bypass signal input terminal.			
48	BW	I	Band switching signal input terminal for Chrominance signal. L: Narrow Band; H: Wide Band			

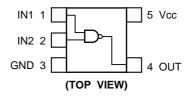
2.10. IC500-503 on the Main Board are using the 2-Channel Electronic Volume/Balance IC YWM51132 FP.

Description of this IC is as follows:



2.11. IC48 on the Main Board is using the Single 2-Input NAND Gate IC YWSC7S00F.

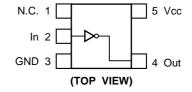
Description of this IC is as follows:



Truth Table						
Inp	uts	Output				
IN1	IN2	Output				
L	ш	Н				
Н	ш	Н				
L	Ι	Н				
Н	Η	L				

2.12. IC18, IC19, IC33, IC44, IC53, IC56, IC100 and IC101 on the Main Board are using the Single Inverter IC YWSC7SU04F.

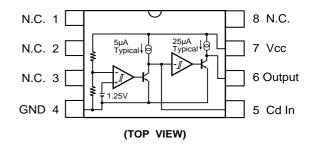
Description of this IC is as follows:

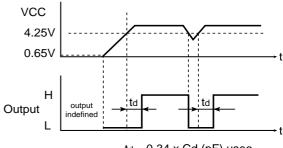


Truth Table						
Input	Output					
L	Н					
Н	L					

2.13. IC3 on the Main Board is using the Voltage Detector IC YWM51953AFP.

Description of this IC is as follows:





 $td \approx 0.34 \text{ x Cd (pF) } \mu \text{sec.}$

2.14. IC30 and IC46 on the Main Board are using the 4-MB Cache DRAM IC YWM5M4V416TP. Description of this IC is as follows:

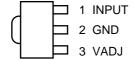
CC1# 4	Vcc DQCI DQCU	1			69	Vss AD9 AD8
WE# 6	CC1#	4 🗆		Ь	67	AD7
CS# 7	CC0#	5 🗆		Ь	66	N.C.
CMD# 8	WE#	6 □		þ	35	N.C.
CMS# 9	CS#	7 🗆		Þ	64	AS9
K 10	CMD#	8 🗆		Þ	3	AS8
DQ0 11	CMS#	9 🗆		Þ	62	AS7
Vss 12	K	10 🗆		Þ	61	AS6
DQ1 13	DQ0	11 🗆		Þ	0	DQ15
DQ2 14	Vss	12 🗆		□ 5	59	Vss
VccQ 15 56 VccQ DQ3 16 55 DQ12 Vss 17 54 Vcc DQ4 19 52 DQ11 VccQ 20 51 VccQ DQ5 21 50 DQ10 DQ6 22 49 DQ9 Vss 23 48 Vss DQ7 24 47 DQ8 N.C. 25 46 N.C. AS0 26 44 AS5 AS1 27 44 AS5 AS2 28 43 AS4 RAS# 29 41 AD6 DTD# 31 40 AD5 AD0 32 39 AD4 AD1 33 37 N.C.	DQ1	13 🗆		卢 5	58	
DQ3 16				_		
Vss 17				P	6	
DQ4 19			(TOP VIEW)			
VccQ 20	Vss	17 🗆	` ,	P	54	Vcc
VccQ 20	DO4	19 🗖		Ļ,	52	DO11
DQ5 21						
DQ6 22				_ `		
Vss 23						
N.C. 25						Vss
ASO 26	DQ7	24		Б	17	DQ8
AS1 27	N.C.	25		F	16	N.C.
AS2 28	AS0	26		Б	15	G#
RAS# 29	AS1	27 🗆		Б	14	AS5
CAS# 30	AS2	28 🗆		Б	13	AS4
DTD# 31	RAS#	29 🗆		⊿ٰ	12	AS3
AD0 32	CAS#	30 □		₽⁴	11	AD6
AD1 33	DTD#	31 🗖				
AD2 34 37 N.C.						
				Ľ	-	
				⊢`	••	

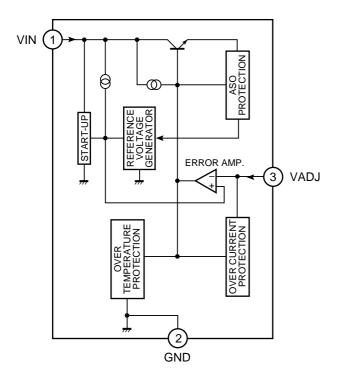
Pin	Name	I/O	Description
1	Vcc	_	Power supply.
2	DQCI	ı	DOO: 1: 1/ : 1
3	DQCU	Ι	DQC signal input terminals.
4	CC1#	Ι	Control clock pulse input
5	CC0#	Ι	terminals.
6	WE#	_	Write Enable signal input terminal.
7	CS#	_	Chip Select signal input terminal.
8	CMD#	I	DRAM clock mask signal input terminal.
9	CMS#	I	SRAM clock mask signal input terminal.
10	K	_	K signal input terminal.
11	DQ0	I/O	DQ signal input/output terminal.
12	Vss	-	Ground terminal.
13	DQ1	I/O	DO sissa di sanda da da da sania da
14	DQ2	I/O	DQ signal input/output terminals.

Dire	None	1/0	Description
Pin 15	Name VccQ	I/O	Description Power supply.
	DQ3	- /O	DQ signal input/output terminal.
_	Vss	_	Ground terminal.
	DQ4	I/O	DQ signal input/output terminal.
20	VccQ	_	Power supply terminal.
21	DQ5	I/O	
	DQ6	I/O	DQ signal input/output terminals.
23	P52/A10	I/O	P52/A10 signal input/output terminal.
24	Vss	_	Ground terminal.
25	N.C.	-	No connection.
26	AS0	I	
27	AS1	I	AS signal input terminals.
28	AS2	I	
29	RAS#	Ι	RAS signal input terminal.
30	CAS#	I	CAS signal input terminal.
31	DTD#	Ι	DTD signal input terminal.
32	Ad0	I	
33	Ad1	Ι	Address signal input terminals.
34	Ad2	Ι	
35	Vcc	_	Power supply terminal.
36	Vss	_	Ground terminal.
37	N.C.	-	No connection.
38	AD3	Ι	
39	AD4	I	
40	AD5	I	Address signal input terminals.
41	AD6	Ι	
42	AS3	I	
43	AS4	I	AS signal input terminals.
44	AS5	I	
45	G#	I	G signal input terminal.
46	N.C.	Ι	No connection.
47	DQ8	I/O	DQ signal input/output terminal.
48	Vss	_	Ground terminal.
49	DQ9	1/0	DQ signal input/output terminals.
50 51	DQ10 VccQ	I/O I	Power supply terminal.
—			
52 54	DQ11 Vcc	I/O	DQ signal input/output terminal.
54 55	DQ12	- /O	Power supply terminal. DQ signal input/output terminal.
55 56		I/O	Power supply terminal.
56	VccQ		r ower suppry terminal.

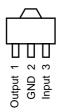
Pin	Name	I/O	Description
57	DQ13	I/O	
58	DQ14	I/O	DQ signal input/output terminals.
59	Vss	_	Ground terminal.
60	DQ15	I/O	DQ signal input/output terminal.
61	AS6	Ι	
62	AS7	1	AS signal input terminals.
63	AS8	1	
64	AS9	_	
65	N.C.	-	No connection.
66	N.C.	_	No connection.
67	AD7	ı	
68	AD8	I	Address signal input terminals.
69	AD8	I	
70	Vss	_	Ground terminal.

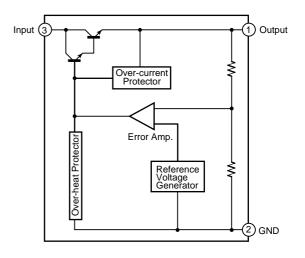
2.15. IC31 and IC51 on the Main Board are using the Voltage Regulator Driver IC YWM5237ML. Description of this IC is as follows:





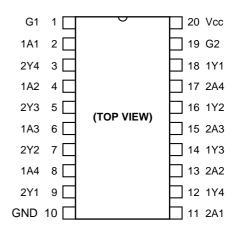
2.16. IC11 on the Main Board is using the 3-Terminal Voltage Regulator IC YW78L05UATE2. Description of this IC is as follows:





2.17. IC513 on the Main Board are using the Quad 3-State Bus Transceivers IC YW74ABT244DB.

Description of this IC is as follows:



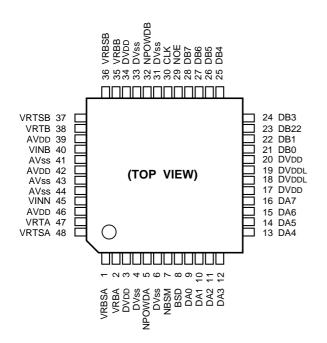
Truth Table

INP	UTS	OUTPUT					
G	Α	Υ					
Н	*	Z					
L	L	L					
L	Н	Н					

* : Don't care.

Z: High Impedance

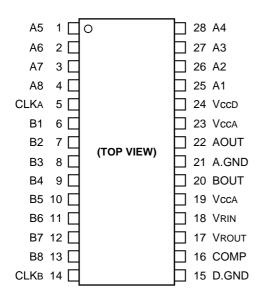
2.18. IC25 and IC39 on the Main Board are using the C-MOS 8-Bit 2-Channel High Speed A/D Converter IC MN65752H. Description of this IC is as follows:



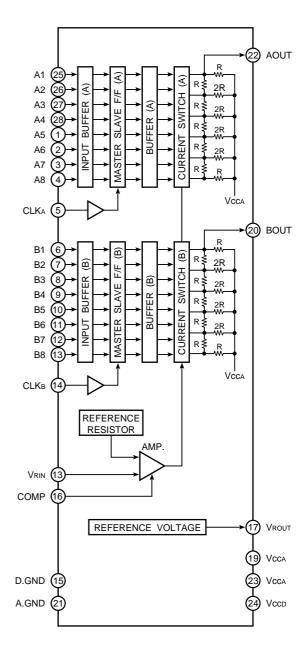
Pin	Name	I/O	Description
1	VRBSA	0	VRBSA signal output terminal.
2	VRBA	ı	VRBA signal inut terminal.
3	DVdd	_	Digital power supply terminal.
4	DVss	_	Digital ground terminal.
5	NPOWDA	I	Power down mode signalinput terminal.
6	DVss	_	Digital ground terminal.
7	NBSM	I	TEOT sinus discount to make als
8	BSD	I	TEST signal input terminals.
9	DA0	0	
10	DA1	0	
11	DA2	0	
12	DA3	0	Digital and autout tarminals
13	DA4	0	Digital code output terminals.
14	DA5	0	
15	DA6	0	
16	DA7	0	
17	DVDD	_	Digital power supply terminal.
18	DVddl	-	Low Voltage Digital power supply
19	DVddl	ı	terminals.
20	DVDD	_	Digital power supply terminal.
21	DB0	0	Digital code output terminals.
22	DB1	0	Digital code output terminals.

<u>Б:</u>	NI	1/0	Description
Pin	Name	I/O	Description
23	DB2	0	
24	DB3	0	
25	DB4	0	Digital code output terminals.
26	DB5	0	- 19.10.1 - 2 - 2 - 2 - 2 - 2 - 2 - 2 - 2 - 2 -
27	DB6	0	
28	DB7	0	
29	NOE	ı	Digital output enable signal input terminal.
30	CLK	I	Clock pulse input terminal.
31	DVss	_	Digital ground terminal.
32	NPOWDB	I	Power down mode signal input terminal.
33	DVss	ı	Digital ground terminal.
34	DVdd	-	Digital power supply terminal.
35	VRBB	I	Bottom side reference voltage input terminal.
36	VRBSB	0	Bottom side reference voltage output terminal.
37	VRTSB	0	Top side reference voltage output terminal.
38	VRTB	I	Top side reference voltage input terminal.
39	AVDD	-	Analog Power supply terminal.
40	VINB	Ι	Analog signal input terminal.
41	AVss	-	Analog ground terminal.
42	AVDD	1	Analog Power supply terminal.
43	AVss	_	Analog ground terminals.
44	AVss	-	Analog ground terminals.
45	VINA	ı	Analog signal input terminal.
46	AVDD	_	Analog Power supply terminal.
47	VRTA	-	Top side reference voltage input terminal.
48	VRTSA	0	Top side reference voltage output terminal.

2.19. IC52 and IC55 on the Main Board are using the 8-Bit 2-Channel D/A Converter IC YWMB40968PF. Description of this IC is as follows:

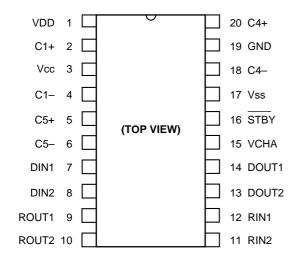


Pin	Name	I/O	Description	
1	A5	Ι		
2	A6	ı	Ach Digital Data input terminals. (8-Bit)	
3	A7	_	Acti Digital Data Input terminals. (o-bit)	
4	A8	_	(LSB)	
5	CLKA	-	Ach Clock pulse input terminal.	
6	B1	-	(MSB)	
7	B2	I		
8	В3	ı		
9	B4	ı	Pob Digital Data input terminals (9 Bit)	
10	B5	Ι	Bch Digital Data input terminals. (8-Bit)	
11	B6	Ι		
12	В7	_		
13	B8	ı	(LSB)	
14	CLKB	_	Bch Clock pulse input terminal.	
15	D.GND	1	Ground terminal for Digital circuit.	
16	COMP	ı	Phase Compensation terminal.	
17	VROUT	0	Reference Voltage output terminal.	
18	VRIN	-	Reference Voltage input terminal.	
19	Vcca	1	Power supply terminal for Analog circuit.	
20	BOUT	0	Bch Analog signal output terminal.	
21	A.GND	1	Ground terminal for Analog circuit.	
22	AOUT	0	Ach Analog signal output terminal.	
23	Vcca	ı	Power supply terminal for Analog circuit.	
24	Vccd	ı	Power supply terminal for Digital circuit.	
25	A1	ı	(MSB)	
26	A2	I	Ash Digital Data input terminals (9 Bit)	
27	А3	I	Ach Digital Data input terminals. (8-Bit)	
28	A4	Ι]	



2.20. IC16 on the Main Board is using the RS-232C Driver IC YWUPD4721GS.

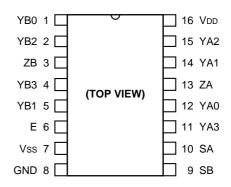
Description of this IC is as follows:



Pin	Name	I/O	Description
1	VDD	-	Power supply terminal.
2	C1+	_	Positive side of capacitor 1 connecting terminal.
3	Vcc		Power supply terminal.
4	C1–	_	Negative side of capacitor 1 connecting terminal.
5	C5+	_	Positive side of capacitor 5 connecting terminal.
6	C5-	1	Negative side of capacitor 5 connecting terminal.
7	DIN1	_	Driver eigned input terminals
8	DIN2	Ι	Driver signal input terminals.
9	ROUT1	0	Descriver signal output terminals
10	ROUT2	0	Receiver signal output terminals.
11	RIN2	Ι	Descrives signal inner towaringle
12	RIN1	-	Receiver signal input terminals.
13	DOUT2	0	Driver simple output to residue
14	DOUT1	0	Driver signal output terminals.
15	VCHA	_	Charge voltage supply terminal.
16	STBY	I	Standby signal input terminal.
17	Vss	_	Ground terminal.
18	C4-	_	Negative side of capacitor 4 connecting terminal.
19	GND	_	Ground terminal.
20	C4+	_	Positive side of capacitor 4 connecting terminal.

2.21. IC20, IC21, IC34, and IC35 on the Main Board are using the Analog Multiplexer/Demultiplexer IC MC74HC4052F.

Description of this IC is as follows:



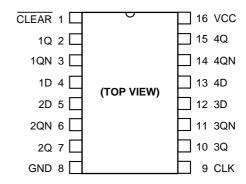
Truth Table

Е	В	Α	X COMMON	Y COMMON
L	L	L	0X	0Y
L	L	Н	1X	1Y
L	Η	L	2X	2Y
L	Н	Н	3X	3Y
Н	*	*	NONE	NONE

* : Don't care.

2.22. IC5 on the Main Board is using the Hex D-FFs IC YWMC74HC175F.

Description of this IC is as follows:

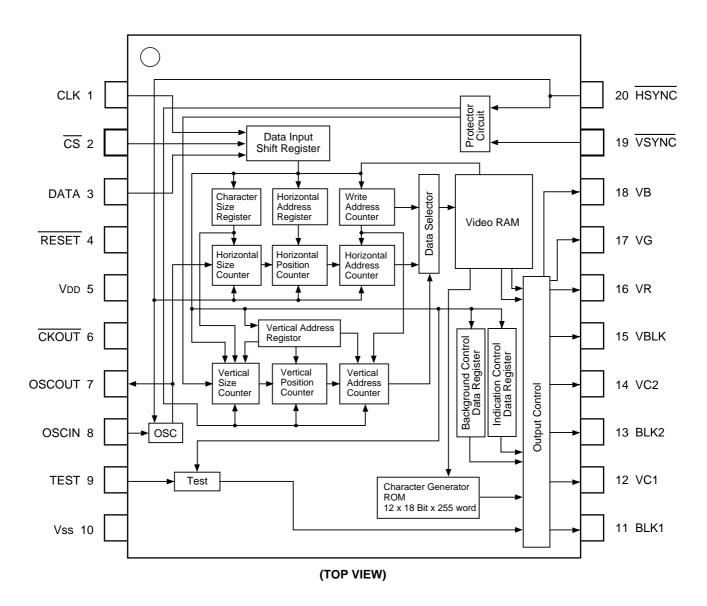


Truth Table

	INPUT	S	OUTPUTS		Function
CLR	D	CLK	Q	lα	Function
L	*	*	L	Н	Clear
Н	L	<u></u>	L	Н	·——
Н	Н	<u></u>	Н	L	
Н	*	1_	Qn	Qn	No Change

*: Don't care.

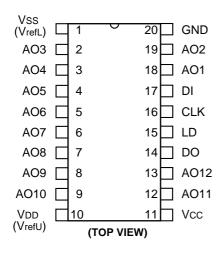
2.23. IC58 on the Main Board is using the Character Generator IC YWBU2874FV. Description of this IC is as follows:

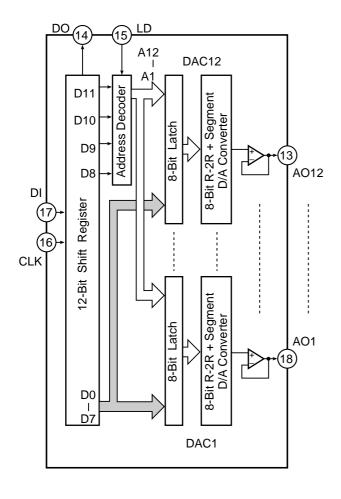


Pin	Name	I/O	Description
1	CLK	ı	Clock Pulse input terminal.
2	S C	ı	Chip Select signal input terminal.
3	DATA	_	Serial Data input terminal.
4	RESET	ı	Reset pulse input terminal.
5	Vdd	_	Power supply terminal.
6	CKOUT	0	Clock pulse output terminal.
7	OSCOUT	0	Oscillator output terminal.
8	OSCIN	Ι	Oscillator input terminal.
9	TEST	ı	Test terminal.
10	Vss	_	Ground terminal.

Pin	Name	I/O	Description	
11	BLK1	0	Blanking Pulse-1 output terminal.	
12	VC1	0	Character singal-1 output terminal.	
13	BLK2	0	Blanking Pulse-2 output terminal.	
14	VC2	0	Character signal-2 output terminal.	
15	VBLK	0	V. Blanking pulse output terminal.	
16	VR	0		
17	VG	0	Character Data output terminals.	
18	VB	0		
19	VSYNC	I	Vertical Sync signal input termnal.	
20	HSYNC	Ī	Horizontal Sync singal input terminal.	

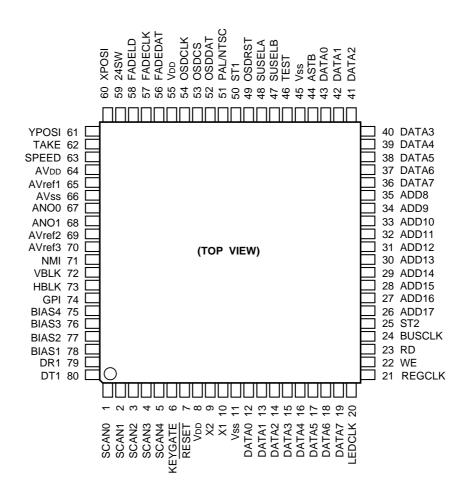
2.24. IC15 on the Main Board is using the 8-Bit 12-Channel D/A Converter YWM62352GP. Description of this IC is as follows:





Pin	Name	I/O	Description
1	VSS (VrefL)	-	Lower reference voltage supply terminal for D/A Converter circuit.
2	AO3	0	
3	AO4	0	
4	AO5	0	
5	AO6	0	Analog Data output terminals.
6	AO7	0	
7	AO8	0	
8	AO9	0	
9	AO10	0	
10	VDD (VrefU)	-	Upper reference voltage supply terminal for D/A Converter circuit.
11	Vcc	_	Power supply terminal terminal.
12	AO11	0	Analog Data output terminals.
13	AO12	0	Analog Data output terminals.
14	DO	0	MSB Data output terminal from 12- Bit Shift Register.
15	LD	I	Load signal input terminal. Data of 12-Bit Shift Register should be loaded to Decoder and D/A Output Registers when LD = H.
16	CLK	I	Shift Clock pulse input terminal. Serial Data from DI terminal should be input to Decoder and 12-Bit Shift Register at raising edge of this signal.
17	DI	-	12-Bit Serial Data input terminal.
18	AO1	0	Analog Data output terminals.
19	AO2	0	7 maiog Data output terminais.
20	GND	_	Ground terminal.

2.25. IC4 on the Main Board is using the 16-Bit Microprocessor IC YW78P4026GCA. Description of this IC is as follows:



Pin	Name	1/0	Description
1	SCAN0	0	
2	SCAN1	0	
3	SCAN2	0	Key Scan signal output terminals.
4	SCAN3	0	
5	SCAN4	0	
6	KEYGATE	0	Key Gate signal output terminal.
7	RESET	Ι	Reset pulse input terminal.
8	VDD	-	Power supply terminal.
9	X2	1	Crystal Oscillator connecting
10	X1	_	terminals.
11	Vss	_	Ground terminal.
12	DATA0	I/O	
13	DATA1	I/O	Data input/output terminals. (8-Bit)
14	DATA2	I/O	(3 2)

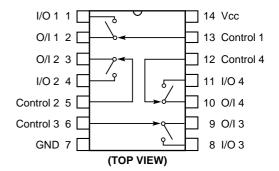
Pin	Name	1/0	Description
15	DATA3	I/O	
16	DATA4	I/O	Data input/output terminals.
17	DATA5	I/O	(8-Bit)
18	DATA6	I/O	
19	DATA7	I/O	
20	LEDCLK	0	LED Clock pulse output terminal.
21	REGCLK	0	Register Clock pulse output terminal.
22	WE	0	Write Enable signal output terminal.
23	RD	0	Read Strobe pulse output terminal.
24	BUSCLK	0	Bus Clock pulse output terminal.
25	ST2	0	ST signal output terminal.

Pin	Name	I/O	Description	
26	ADD17	0		
_	ADD16	0		
28	ADD15	0		
29	ADD14	o	Address signal output terminals	
30	ADD13	0	Address signal output terminals. (12-Bit)	
	ADD12	0		
32	ADD11	o		
_	ADD10	0		
	ADD9	0		
<u> </u>	ADD8	0		
_	DATA7	1/0		
37		1/0		
_	DATA5	1/0		
	DATA4	1/0	Data input/output terminals.	
_	DATA3	1/0	(8-Bit)	
<u> </u>	DATA3	1/0		
	DATA2 DATA1	1/0		
<u> </u>	DATA1	1/0		
F	ASTB	0	Address Strobe signal output	
44			terminal.	
45	Vss	_	Ground terminal.	
46	TEST	ı	TEST signal input terminal.	
47	SVSELB	0	SVSELB signal output terminal.	
48	SVSELA	0	SVSELA signal output terminal.	
49	OSDRST	0	OSDRST signal output terminal.	
50	ST1	0	ST1 signal output terminal.	
51		ı	PAL/NTSC signal input terminal.	
	OSDDAT	0	Port signal input/output terminals.	
	OSDCS	0	(8-Bit)	
54		0		
55		_	Power supply terminal.	
56		0	FADEDAT signal output terminal.	
57	FADECLK	0	FADECLK signal output terminal.	
58		0	FADELD signal output terminal.	
59	24SW	ı	24SW input terminal.	
60	XPOSI	ı	XPOSI signal input terminal.	
61	YPOSI	I	YPOSI signal input terminal.	
62	TAKE	I	TAKE signal inout terminal.	
63	SPEED	I	SPEED signal inout terminal.	
64		-	Analog Power supply terminal.	
65	AVref1	\perp	Reference voltage terminal 1.	
66	AVss	\perp	Analog Ground terminal.	
67	ANO0	0	Analog 0 signal output terminal.	
68	ANO1	0	Analog 1 signal output terminal.	
69	AVref2	_	Reference voltage terminal 2.	

Pin	Name	I/O	Description
70	AVref3	_	Reference voltage terminal 3.
71	NMI	Ι	Non Maskable Interrupt signal input terminal.
72	VBLK	Ι	V.Blanking signal input terminal.
73	HBLK	ı	H.Blanking signal input terminal.
74	GPI	Ι	GPI signal input terminal.
75	BIAS4	Ι	
76	BIAS3	ı	BIAS signal input terminals.
77	BIAS2	Ι	Dir to signal impat terminais.
78	BIAS1	Ι	
79	DR1	Ι	DR signal input terminal.
80	DT1	0	DT signal output terminal.

2.26. IC23 and IC37 on the Main Board are using Quad Analog Switches/Multiplexers/Demultiplexers IC YWMC74HC4066F.

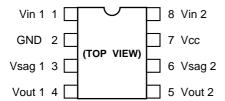
Description of this IC is as follows:



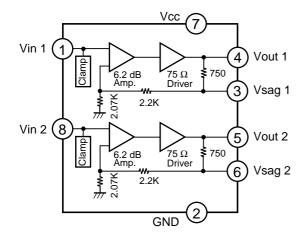
Truth Table

Input	Switch
Control	I/O - O/I
L	OFF
Н	ON

2.27. IC13 on the Main Board is using the 6 dB Video Amplifier with 75Ω Driver IC YWNJM2267M. Description of these IC is as follows:

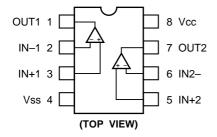


Pin	Name	I/O	Description
1	Vin 1	Ι	Input terminal for Amplifier 1.
2	GND	_	Ground terminal.
3	Vsag 1	_	Sag compensation terminal for Amplifier 1.
4	Vout 1	0	Output terminal for Amplifier 1.
5	Vout 2	0	Output terminal for Amplifier 2.
6	Vsag 2	1	Sag compensation terminal for Amplifier 2.
7	Vcc	_	Power supply terminal.
8	Vin 2	_	Input terminal for Amplifier 2.



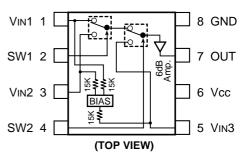
2.28. IC504 and IC505 on the Main Board are using the Dual Operational Amplifier IC NJM3404AM.

Description of these IC is as follows:



2.29. IC900 and IC901 on the Main Board are using the 3-Input Video Switch IC YWNJM2245M.

Description of this IC is as follows:



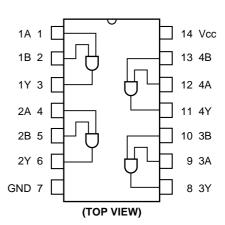
Truth Table

SW1	SW2	OUT
L	L	Vin1
Н	L	Vin2
	Н	Vin3

: Don't care.

2.30. IC801 and IC804 on the Main Board are using the Quad 2-Input AND Gate IC YWMC74F08M.

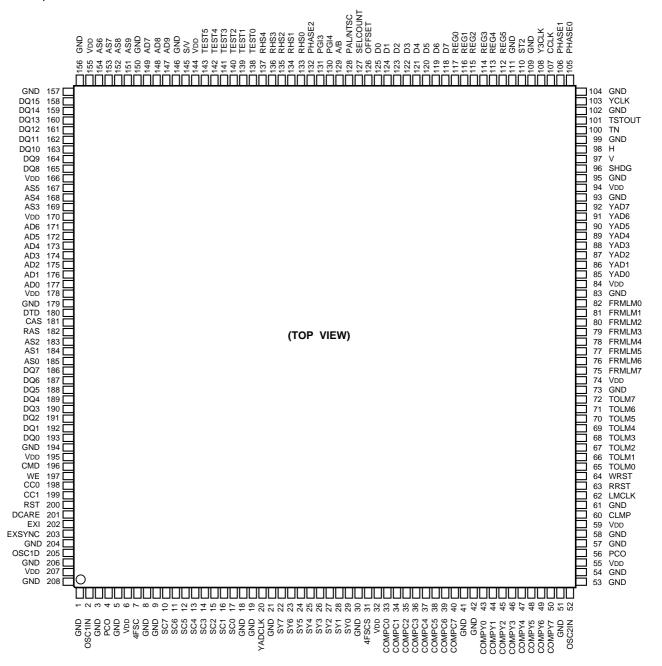
Description of these IC is as follows:



Truth Table

INP	UTS	OUTPUT	
Α	В	Υ	
L	L	L	
L	Н	L	
Ι	_	┙	
11	11	П	

2.31. IC29 and IC43 on the Main Board are using Write Control Gate Array Logic IC YWAJ0014. Description of this IC is as follows:



Pin	Name	I/O	Description	
1	GND	-	Ground terminal.	
2	OSC1IN	Ι	Oscillator input terminal.	
3	GND	_	Ground terminal.	
4	PCO	0	PCO signal output terminal.	
5	GND	١	Ground terminal.	
6	VDD	١	Power supply terminal.	
7	4FSC	0	4FSC signal output terminal.	
8	GND	-	Ground terminal.	
9	GND	_	Ground terminal.	
10	SC7	_	Serial clock pulse input terminal.	

Pin	Name	I/O	Description	
11	SC6	Ī		
12	SC5	I		
13	SC4	ı		
14	SC3	_	Serial clock pulse input terminals.	
15	SC2	_		
16	SC1	-		
17	SC0	_		
18	GND	-	0	
19	GND	_	Ground terminal.	
20	YADCLK	_	Not used.	

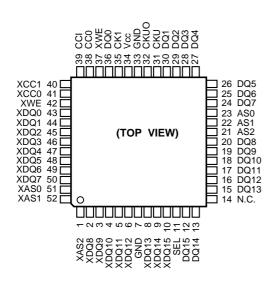
Pin	Name	I/O	Description	
21	GND	_	Ground terminal.	
22	SY7	ı		
23	SY6	ı		
24	SY5	ı		
25	SY4	ı	SY signal input terminals.	
26	SY3	ı	Ŭ I	
27	SY2	ı		
28	SY1	ı		
29		ī		
30		_	Ground terminal.	
31	4FSCS	0	4FSCS signal output terminal.	
32	VDD	_	Power Supply termianl.	
33	COMPC0	ı		
34	COMPC1	ī		
35	COMPC2	i		
36	COMPC3	i	COMPC signal input terminals.	
37	COMPC4	i	c s.gapat torrinido.	
38	COMPC5	i		
39	COMPC6	i		
40		Ť		
41	GND	<u> </u>	Ground terminal.	
42	GND	_	Ground terminal.	
43	COMPY0	ī	Croana terrimiai.	
44	COMPY1	i		
45	COMPY2	÷		
46	COMPY3	i	COMPY signal input terminals.	
47	COMPY4	÷	Com i signal input terminais.	
48	COMPY5	÷		
49	COMPY6	÷		
50	COMPY7	÷		
51	GND	Ť	Ground terminal.	
52	OSC2IN	÷	Oscillator input terminal.	
53	GND	÷	Ground terminal.	
54	GND		Ground terminal.	
55	VDD	_	Power supply terminal.	
56	PCO	0	PCO signal output terminal.	
57	GND	_	Ground terminal.	
58	GND	_	Ground terminal.	
59		_	Power supply terminal.	
60	CLMP	0	CLMP signal output terminal.	
61	GND	_	Ground terminal.	
62	LMCLK	0	LMCLK signal output terminal.	
63	RRST	0	R Reset signal output terminal.	
64	WRST	0	W Reset signal output terminal.	
65	TOLM0	0	<u> </u>	
66	TOLM1	0		
67	TOLM2	0		
68	TOLM3	0	TOLM signal output terminals.	
69	TOLM4	0	3	
70	TOLM5	0		
71	TOLM6	0		
نب		_	_	

Pin	Name	I/O	Description	
72	TOLM7	0	TOLM signal output terminal.	
73	GND		Ground terminal.	
74	Vdd	_	Power supply terminal.	
75	FRMLM7	ı		
76	FRMLM6	ı		
77	FRMLM5	ı		
78	FRMLM4	Ι	FRMLM signal input terminals.	
79	FRMLM3	ı		
80	FRMLM2	ı		
81	FRMLM1	ı		
82	FRMLM0	I		
83	GND	_	Ground terminal.	
84	Vdd	_	Power supply terminal.	
85	YAD0	0		
86	YAD1	0		
87	YAD2	0		
88	YAD3	0		
89	YAD4	0	YAD signal output terminals.	
90	YAD5	0		
91	YAD6	0		
92	YAD7	0		
93	GND	_	Ground terminal.	
94	Vdd	_	Power supply terminal.	
95	GND	_	Ground terminal.	
96	SHDG	ı	SHDG signal input terminal.	
97	V	ı	V signal input terminal.	
98	Н	ı	H signal input terminal.	
99	GND	_	Ground terminal.	
100	TN	ı	TN signal input terminal.	
101	TSTOUT	0	Test signal output terminal.	
102	GND	_	Ground terminal.	
103	YCLK	ı	Y Clock pulse input terminal.	
104	GND	_	Ground terminal.	
105	PHASE0	ı	PHASE signal input terminal.	
106	PHASE1	ı	PHASE signal input terminal.	
107	CCLK	ı	C Clock pulse terminal.	
108	Y3CLK		Y3 Clock pulse terminal.	
109	GND		Ground terminal.	
110	ST2	ı	ST signal input terminal.	
111	GND	I	Ground terminal.	
112	REG5	I		
113	REG4	1		
114	REG3		Register signal input terminals.	
115	REG2	1	Trogistor digital impat terminals.	
116	REG1	ı		
117	REG0	ı		
118	D7	1		
119	D6	1	Data input terminals.	
120	D5	1	4	
121	D4	ı		

Pin	Name	I/O	Description	
122		ı		
123		ī	Data input terminals.	
124		Ť		
125		Ť		
	OFF SET	Ť	OFF SET signal input terminal.	
	SEL COUNT	Ť	SEL COUNT signal input terminal.	
	PAL/NTSC	ī	PAL/NTSC signal input terminal.	
129		Т	A/B signal input terminal.	
	PGI4	Ť	PGI signal input terminal.	
-	PGI3	Т	PGI signal input terminal.	
132	PHASE2	_	PHASE signal input terminal.	
_	RHS0	ı	3 1	
-	RHS1	Т		
_	RHS2	ı	RHS signal input terminal.	
	RHS3	Т	1 1 3 1 1 1 1 1 1	
	RHS4	Т		
I	TEST0	Т		
	TEST1	Т		
	TEST2	T		
_	TEST3	Ť	TEST signal input terminal.	
\vdash	TEST4	Ť	1201 olgilar ilipat tollillilari	
	TEST5	Ť		
	VDD	_	Power supply terminal.	
145		ī	S/V signal input terminal.	
	GND	Ė	Ground terminal.	
	AD9	0	Ground terminal.	
1	AD8	0	Address signal output terminal.	
	AD7	0	Address signal output terrillial.	
	GND		Ground terminal.	
	AS9	0	Ground terminal.	
	AS8	0		
	AS7	0	AS signal output terminals.	
	AS6	0		
	VDD		Dower augusty terminal	
	GND	_	Power supply terminal. Ground terminal.	
		_	Ground terminal.	
	GND DO15	-	Ground terminal.	
-	DQ15	1/0		
	DQ14	1/0		
-	DQ13	1/0		
	DQ12	1/0	DQ signal input/output terminal.	
	DQ11	1/0		
-	DQ10	1/0		
-	DQ9	1/0		
	DQ8	I/O	Davis and the state of the stat	
	VDD	_	Power supply terminal.	
	AS5	0	AC gignel output to main al-	
	AS4	0	AS signal output terminals.	
	AS3	0		
	VDD	_	Power supply terminal.	
1	AD6	0	AD signal output terminals.	
172	AD5	0	5 ,	

Pin	Name	I/O	Description
173	ADR 4	0	•
-	ADR 3	0	
175	ADR 2	0	ADR signal output terminal.
	ADR 1	0	3
-	ADR 0	0	
178	VDD	_	Power Supply terminal.
-	GND	_	Ground terminal.
180	DTD	0	DTD signal output terminal.
181	CAS	0	Column Address Strobe signal output terminal.
182	RAS	0	Row Address Strobe signal output terminal.
183	AS2	0	
184	AS1	0	AS signal output terminals.
185	AS0	0	
186	DQ7	I/O	
187	DQ6	I/O	
	DQ5	I/O	
	DQ4	I/O	DO -ili
	DQ3	I/O	DQ signal input/output terminals.
	DQ2	I/O	
	DQ1	I/O	
	DQ0	I/O	
	GND	-	Ground terminal.
	VDD	_	Power Supply terminal.
	CMD	0	CMD signal output terminal.
	WE	0	Write enable signal output terminal.
	CC0	0	CC signal output terminals.
	CC1	0	oo signal output terrilinais.
	RST	ı	Reset signal input terminal.
	DC ARE	_	DC ARE signal input terminal.
	EXI	_	External signal input terminal.
	EXSYNC	Ι	External sync signal input terminal
	GND	_	Ground terminal.
I I	OSC1D	_	Not used.
	GND	_	Ground terminal.
	VDD	_	Power Supply terminal.
208	GND	_	Ground terminal.

2.32. IC800 on the Main Board are using Gate Array Logic IC YWUPD6511GC. Description of this IC is as follows:



Pin	Name	I/O	Description	
1	XAS2	0	XAS signal output terminal.	
2	XDQ8	0		
3	XDQ9	0		
4	XDQ10	0	XDQ signal output terminals.	
5	XDQ11	0		
6	XDQ12	0		
7	GND	ı	Ground termial.	
8	XDQ13	0		
9	XDQ14	0	XDQ signal output terminals.	
10	XDQ15	0		
11	SEL	Ι	SEL signal input terminal.	
12	DQ15	Ι	DQ signal output terminals.	
13	DQ14	I	DQ signal output terminals.	
14	N.C.	ı	No connection.	
15	DQ13	_		
16	DQ12	Ι		
17	DQ11	-	DQ signal input terminals.	
18	DQ10	I	DQ signal input terminals.	
19	DQ9	-		
20	DQ8	Ι		
21	AS2	Ι		
22	AS1	I	AS signal input terminal.	
23	AS0	Ι	Ao signal input terminal.	
24	DQ7	Ι		
25	DQ6	I	DQ signal output terminals.	
26	DQ5	I	שע signal output terminals.	
27	DQ4	_		

Pin	Name	I/O	Description	
28	DQ3	ı		
29	DQ2	ı	DQ signal input terminals.	
30	DQ1	ı		
31	CKU	ı	CKU signal input terminal.	
32	CKUO	Ι	CKUO signal input terminal.	
33	GND	ı	Ground terminal.	
34	Vcc	I	Power supply terminal.	
35	CKI	ı	CKI signal input terminal.	
36	DQ0	ı	DQ signal input terminal.	
37	XWE	I	Write enable input terminal.	
38	CC0	I	00 - i l i t t i l -	
39	CC1	ı	CC signal input terminals.	
40	XCC1	0	VCC signal output terminals	
41	XCC0	0	XCC signal output terminals.	
42	XWB	0	XWB signal output terminal.	
43	XDQ0	0		
44	XDQ1	0		
45	XDQ2	0		
46	XDQ3	0	VDO signal autout tarminala	
47	XDQ4	0	XDQ signal output terminals.	
48	XDQ5	0		
49	XDQ6	0		
50	XDQ7	0		
51	XAS0	0	VAC along all accepts the margin all-	
52	XAS1	0	XAS signal output terminals.	

ADJUSTMENT PROCEDURE

1. Test Equipment Required

- The following Test Equipments are required for adjustment of the Digital AV Mixer WJ-AVE55.
- Oscilloscope
- Frequency Counter
- Digital Voltmeter
- Vectorscope
- Waveform Monitor
- Underscanned Colour Video Monitor
- Video Signal Generator
- Audio Generator
- Extension Board (Part Number: YWV01034AN) for Power Board and Main Board as shown Fig. 1-1.



Fig. 1-1

2. Disassembling Procedure for Adjustment

 Referring to Fig. 2-1, remove nine screws that secure the Upper Cover and remove the Upper Cover.

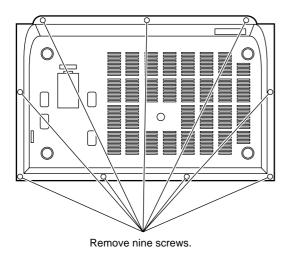


Fig. 2-1

 Referring to Fig. 2-2, remove five screws that secure the Shield Cover and remove the Shield Cover.

Disconnect the Flat Cable from CN3 on the Power Board and CN3 on the Main Board.

Remove five screws that secure the Main Board and remove the Main Board.

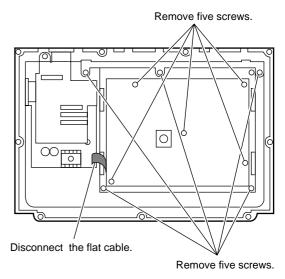


Fig. 2-2

 Referring to Fig. 2-3, connect the Extension Board between CN3 on the Power Board and CN3 on the Main Board.

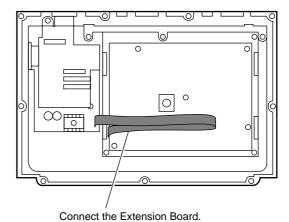


Fig. 2-3

3. Connection and Setting Up for Adjustment

 The Fig. 3-1 shows the connection diagram for the adjustment procedure.

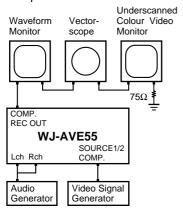


Fig. 3-1

- Connect the Underscanned Colour Video Monitor through Waveform Monitor to the COMP OUT Connector on the REC OUT Section of the Rear Panel.
- Terminate the input terminal of the Underscanned Colour Video Monitor with 75 Ω.
- Connect the probe of the Digital Voltmeter, Oscilloscope or Frequency Counter at the desired Test Point in each adjustment step.
- The adjustments should be done after 10-minute warm up.

4. Adjustment Procedure

 Refer to the Location of the Test Points and Adjusting Controls on page 30.

1. Subcarrier Frequency Adjustment

Test Point: TP21 (FSC) Main Board Adjust: VR3 (FSC) Main Board

- Disconnect all signals from the Input terminals of the WJ-AVE55.
- Connect the Frequency Counter to TP21.
- Adjust VR3 to obtain 17.732676 MHz ± 5 Hz.

2. Read VCO Adjustment

Test Point: TP6 (READ VCO) Main Board Adjust: L929 (READ VCO) Main Board

- Disconnect all signals from the Source Input Connectors of the WJ-AVE55.
- Connect the Digital Voltmeter to TP6.
- Adjust L929 to obtain 2.8 ± 0.1V.

3. Write A VCO Adjustment

Test Point: TP2 (WRITE A VCO) Main Board Adjust: L72 (WRITE A VCO) Main Board

- Supply the Composite Video signal to the COMP Connector of the SOURCE1 section.
- Press the SOURCE1 Button of the A-Bus.
- Connect the Digital Voltmeter to TP2.
- Adjust L72 to obtain 1.8 ± 0.1V.

4. Write B VCO Adjustment

Test Point: TP4 (WRITE B VCO) Main Board
Adjust: L71 (WRITE B VCO) Main Board

- Supply the Composite Video signal to the COMP Connector of the SOURCE1 section.
- Press the SOURCE1 Button of the B-Bus.
- Connect the Digital Voltmeter to TP4.
- Adjust L71 to obtain 1.8 ± 0.1V.

5. A-Bus Y Gain Adjustment

Test Point: COMP Connector of REC OUT Rear Panel Adjust: VR2 (Y GAIN) Main Board

- Supply the Composite Video signal to the COMP Connectors of the SOURCE1 and SOURCE2 sections.
- Press the SOURCE1 Button of the A-Bus and SOURCE2 Button of the B-Bus.
- Connect the Colour Video Monitor to the Preview Output Connector on the Rear Panel.
- Press the Wipe Button, the Wipe Menu should be displayed on the Colour Video Monitor.
- Select by using the Up/Down/Left/Right Buttons.
- Select by using the SELECT/UNDO Button.
- Connect the terminated Oscilloscope with 75 Ω to the COMP Connector of the REC OUT section.
- Set the Mix/Wipe Control to the B-Bus side (down side).
- Confirm the Luminance signal level of the B-bus.
- Set the Mix/Wipe Control to the A-Bus side (upper side).
- Adjust VR2 so that the Luminance signal level becomes same level ± 21 mV as B-Bus Luminance signal level as shown in Fig. 4-1.

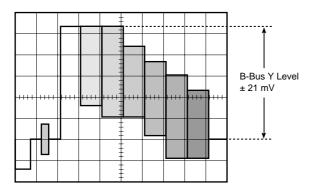


Fig. 4-1

6. A-B H Phase Adjustment

Test Point: TP10 (A SYNC) Main Board
TP11 (B SYNC) Main Board
Adjust: VR5 (H PHASE) Main Board

- Supply the Composite Cross-hatch Pattern signal to the COMP Connectors of the SOURCE1.
- Press the Mix/Wipe Button.
- Press the SOURCE1 Button of the A-Bus and B-Bus.
- Connect the Video Monitor to the Preview Output Connector on the Rear panel.
- Set the WIPE/MIX Control to the Center position.
- Adjust VR5 so that the Cross-hatch Pattern signal of A-Bus and B-Bus becomes coincides on the Video Monitor as shown in Fig. 4-2.

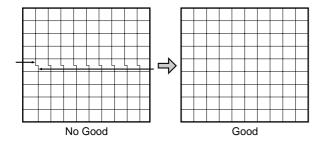
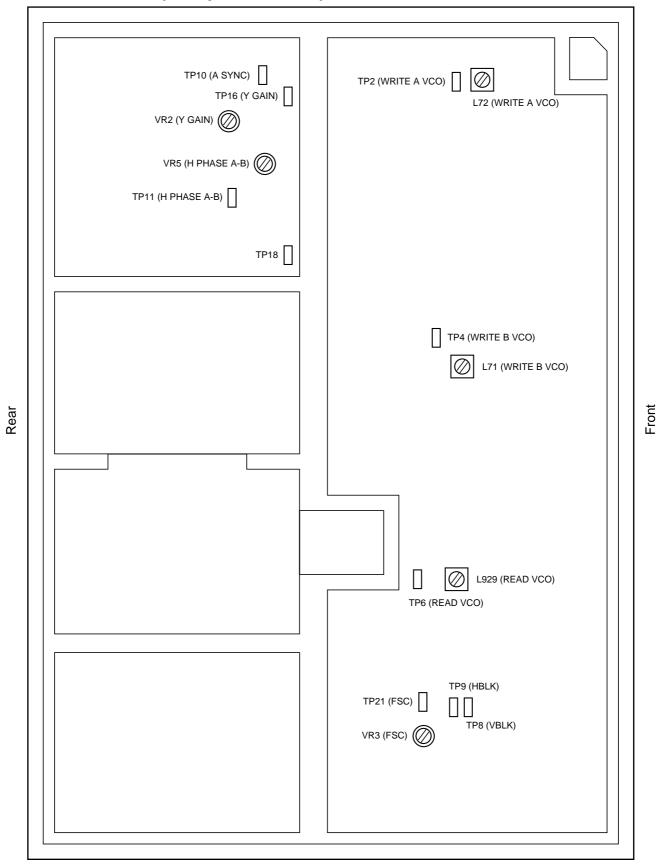


Fig. 4-2

LOCATION OF TEST POINTS AND ADJUSTING CONTROLS

MAIN BOARD (Component Side)



APPEARANCE OF IC, TRANSISTOR AND DIODE

YWAJ0014 YWAJ0016 YW78P4026GCA YWM5M4V416 YWUPD6511GC YWM141625BFU YWMB40968PF YWUPD42102G3 MN65752H MC74HC374AF YWM51132FP MC74HC4066F YWNJM2267M YWSC7SU04F YWM5237ML YW78L05UATE1 YWTA76431S YWUPC24M12HF MC74HC4052F YWSC7S00F YWUPD4721GS YWMC74HC08F YWLM1881M YW78L05UATE2 YWMC74HC175F YWSC7S08F YWM62352GP YWNJM2268V MC74HC541F NJM3404AM YWM51953AFP YW74ABT244DB 1SV153 YWERA1502 YWKV1471 YWRB421D YWRD18JT1B2 S1WBA60 2SA1576 2SC3377 2SC2866 2SK662-PQR YWERA84009 MA141KTX 2SC4081 2SD1979 YWERA34-10 MA741TX 2SB1219QRST YWERA9102 2SC4713K 2SD601-QR K **—)** A К 🗐 🗀 А

CHIP COMPONENTS

1. Chip Transistor

The transistor number is indicated on the top surface of the chip transistor using two alphabet letters or one numerical number and two alphabet letters.



Transistor Number

(Chip Transistor)

Letter	Transistor No.	Letter	Transistor No.
A	2SB709	X	2SD602A
В	2SB709A	Y	2SD601
c	2SB710	z	2SD601A
D	2SB710A	1A	2SB799
E	2SA1022	1B	2SB814
F	2SA1034	1C	2SB902
Н	2SA1035	1F	2SK321
ı	2SB792	1K	2SK316
К	2SC2778	1L	2SK247
Р	2SD814	1M	2SJ84
Q	2SD813	1N	2SK199
R	2SC2480	10	2SK198
S	2SC2405	1T	2SC3077
Т	2SC2406	1X	2SC2845
U	2SC2404	1Z	2SD1030
V	2SC2295	2B	2SK374
W	2SD602	2C	2SK116
BQ	2SB766A	UMT	2SC4081

(Small Chip Transistor) (Pair Transistor)

Letter	Transistor No.
Α	2SB1218
В	2SB1218A
D	2SB1219A
J	2SC3931
W	2SD1820
Х	2SD1820A
Υ	2SD1819
E3	2SA1226
os	2SB1219
UC	2SA1532
YU	2SC3938

Letter	Transistor No.	Letter	Transistor No.
5R	XN1501	5H	XP4501
7S	XN1601	5C	XP4601
5H	XN4501	5H	XP4501
5C	XN4601	5L	XP5501
5L	XN5501	4N	XP5601
4N	XN5601	7S	XP6501
5N	XN6501	7W	XP6435
7W	XN6435	7F	XP6534
7F	XN6534	X1	UMX1
5R	XP1501	Z1	UMZ1
7S	XP1601		

Example: WQ -

WQ → 2SD602-Q

YQ → 2SD601-Q

1BS → 2SB814-S

Appearance and Symbols

Transistor



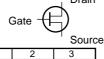
C: Collector

B: Base

E: Emitter

FE





	1	2	3
Eacept 2SK199	Drain	Source	Gate
2SK199	Gate	Drain	Source

2. Chip Diode

The diode number is indicated on the top surface of the chip diode using two alphabet letters.



Diode Number

Letter	Diode No.	Letter	Diode No.
MA	MA151A	MI	MA152K
MB	MA152A	MK	MA28W-B
MC	MA153	ML	MA28T-A
MD	MA28-A	MN	MA151WA
ME	MA28-B	MO	MA152WA
MF	MA28W-A	MT	MA151WK
MH	MA151K	MU	MA152WK
MH	MA141K	6.2	MA3062
MC	MA143	SMD	RD421D

Appearance and Symbols

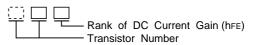




	1	2	3
MA28/MA28W/MA28T	_	Anode	Cathode
MA151K/MA152K	_	Anode	Cathode
MA151A/MA152A	-	Cathode	Anode
MA151WK/MA152WK	Anode	Anode	Cathode
MA151WA/MA152WA	Cathode	Cathode	Anode
MA153	Cathode	Anode	Common
MA141K	-	Anode	Cathode
MA143	Anode	Cathode	Common
MA3062	Anode	-	Cathode
RD421D	Anode	_	Cathode

3. Chip Resistor

The resistor value is indicated on the bottom surface of the chip resistor using three digit numbers.



Example:

330 \longrightarrow 33 x 10⁰ = 33 Ω 561 \longrightarrow 56 x 10¹ = 560 Ω 123 \longrightarrow 12 x 10³ = 12 kΩ

Note: Zero ohm resistor (jumper chip) is colored red or green.

4. Chip Capacitor

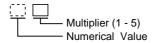
The capacitive value of replacement chip capacitors is indicated on the bottom surface. Original parts have no value indication.

If the capacitive value is less than 100 pF, the value will be indicated by one or two digit number expressing the capacity directly in pF.

Example:

$$0.5 \longrightarrow 0.5 \text{ pF}$$
 $2.5 \longrightarrow 2.5 \text{ pF}$
 $.75 \longrightarrow 0.75 \text{ pF}$ $33 \longrightarrow 33 \text{ pF}$
 $1 \longrightarrow 1 \text{ pF}$ $82 \longrightarrow 82 \text{ pF}$

If the capacitive value is 100 pF or greater, the value will be indicated by an alpha-numeric code. The letter precedes the number and expresses a numerical value to be multiplied by the number which follows.



Numerical Value

Letter	Value	Letter	Value
Α	10	N	33
В	11	Р	36
С	12	Q	39
D	13	R	43
Е	15	S	47
F	16	Т	51
G	18	U	56
Н	20	V	62
J	22	W	68
K	24	X	75
L	27	Υ	82
М	30	Z	91

* Letters I and O are not used.

Example: A1
$$\longrightarrow$$
 10 x 10¹ = 100 pF
N2 \longrightarrow 33 x 10² = 3300 pF
S3 \longrightarrow 47 x 10³ = 47000 pF

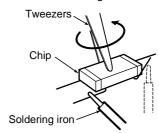
5. Precautions in replacing the chip component

- 1. Make sure that the unit is turned OFF when replacing the chip.
- 2. Use tweezers to prevent any damage to the chip surface.
- 3. Do not re-use the chips after removal.
- 4. Do not rub the electrode of chips.
- 5. Do not subject the chips to excessive stress.
- 6. It is recommended that a pencil-type soldering iron to be used.
- 7. The solder whose diameter is less than 0.5 mm is recommended.
- 8. Do not heat the chip more than 3 seconds.
- 9. Maintain temperature control under 260°C (500°F) when soldering.

5-1. Removal (Transistor, Diode, Resistor and Capacitor)

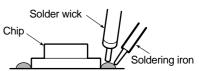
- 1. Add the solder to both ends of the chip (three leads for chip transistor).
- 2. While attaching the soldering iron to both ends of the chip (three leads for chip transistor) as shown below, remove the chip by turning with tweezers.

Note: Be careful not to damage other chips.

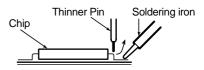


5-2. Removal (IC)

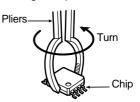
1. Add the solder wick and soldering iron to each lead of the IC and remove solder.



2. Add the soldering iron to each lead of the IC and left each lead of the IC using thinner pin.

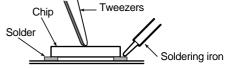


3. Remove the IC turning with pliers.

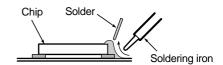


5-3. Mounting

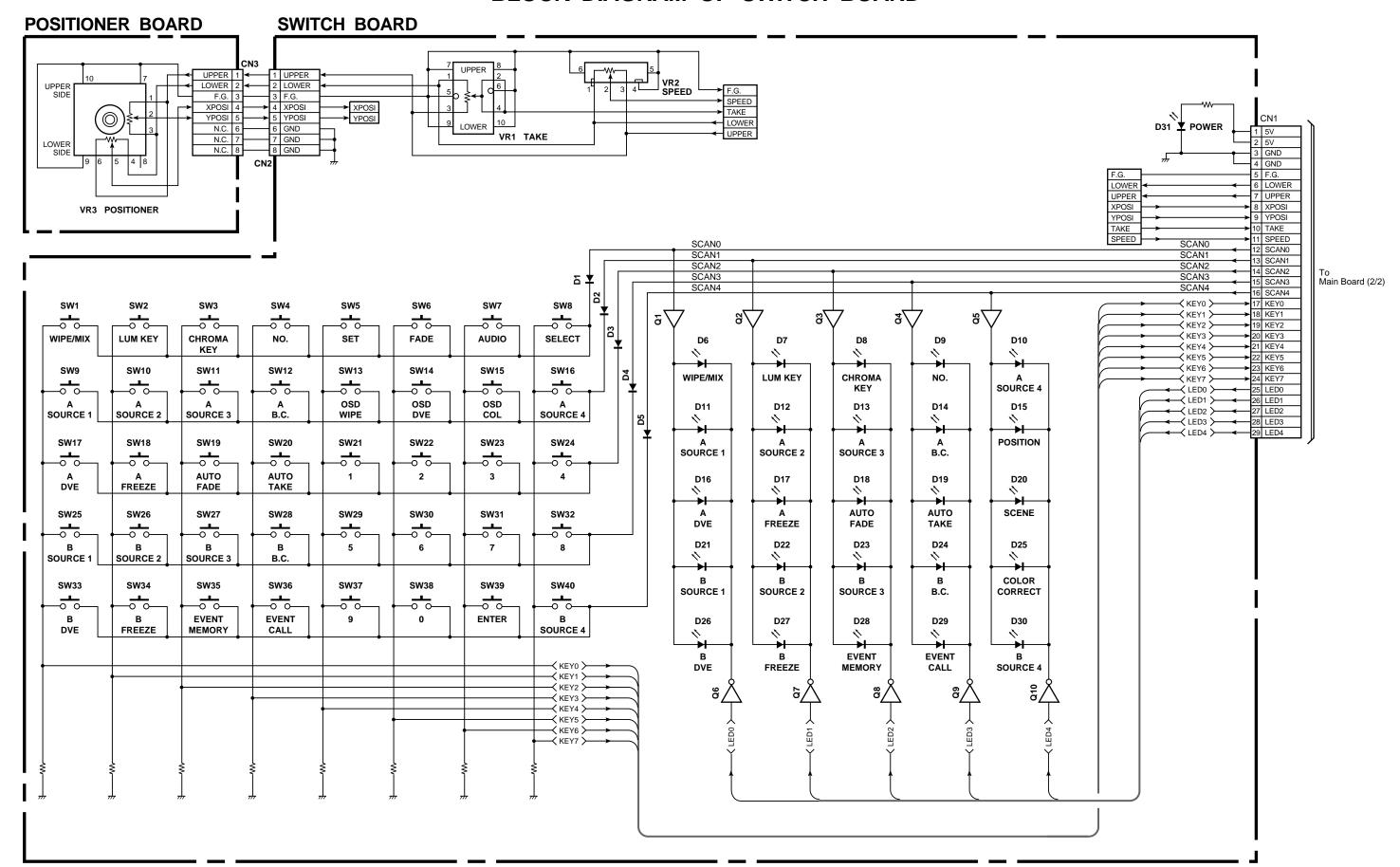
- 1. Place the solder thinly on the chip mounting foil.
- 2. Solder the chip temporarily while holding the chip with the tweezers.



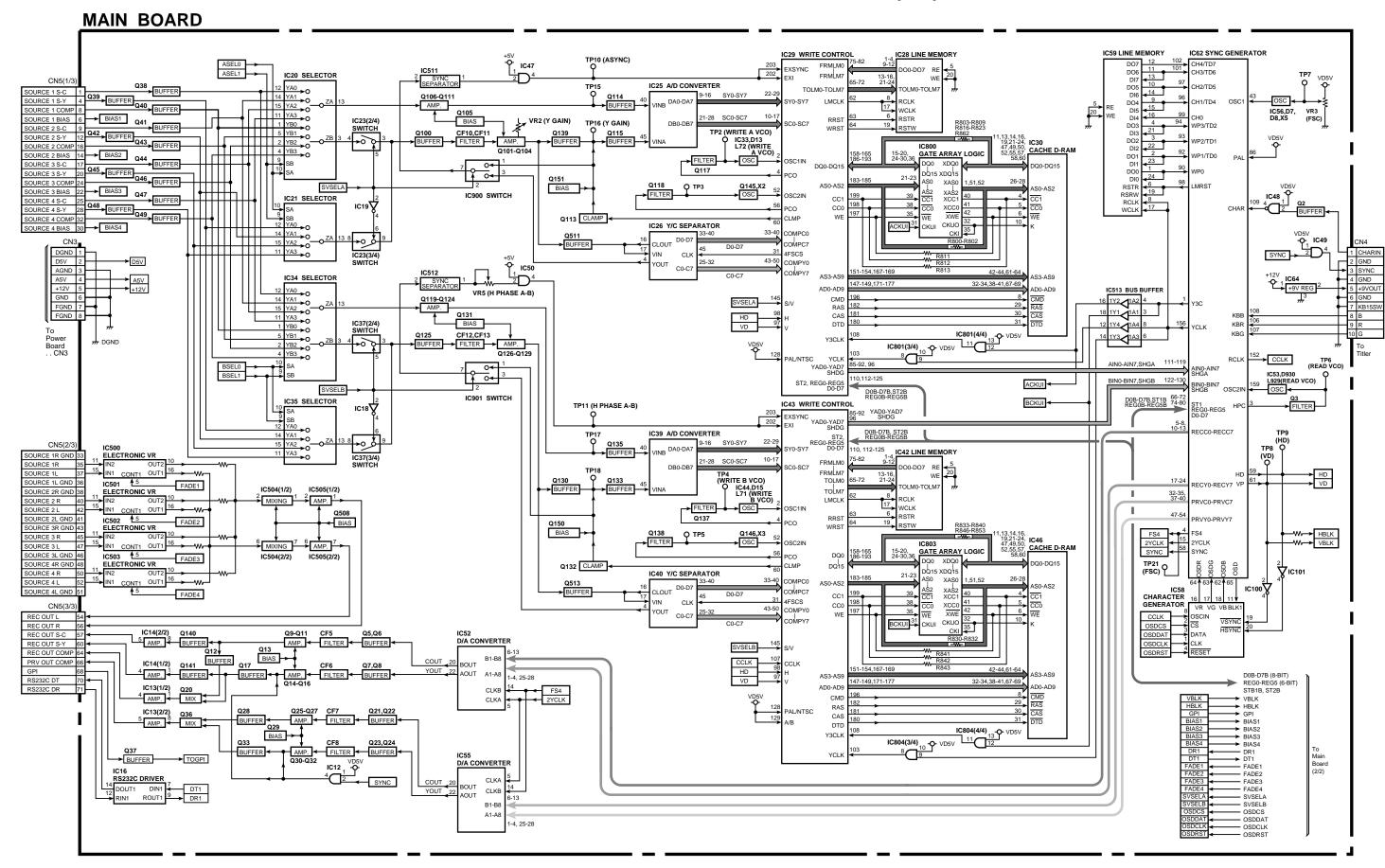
3. Solder both ends of the chip (three leads for chip transistor).



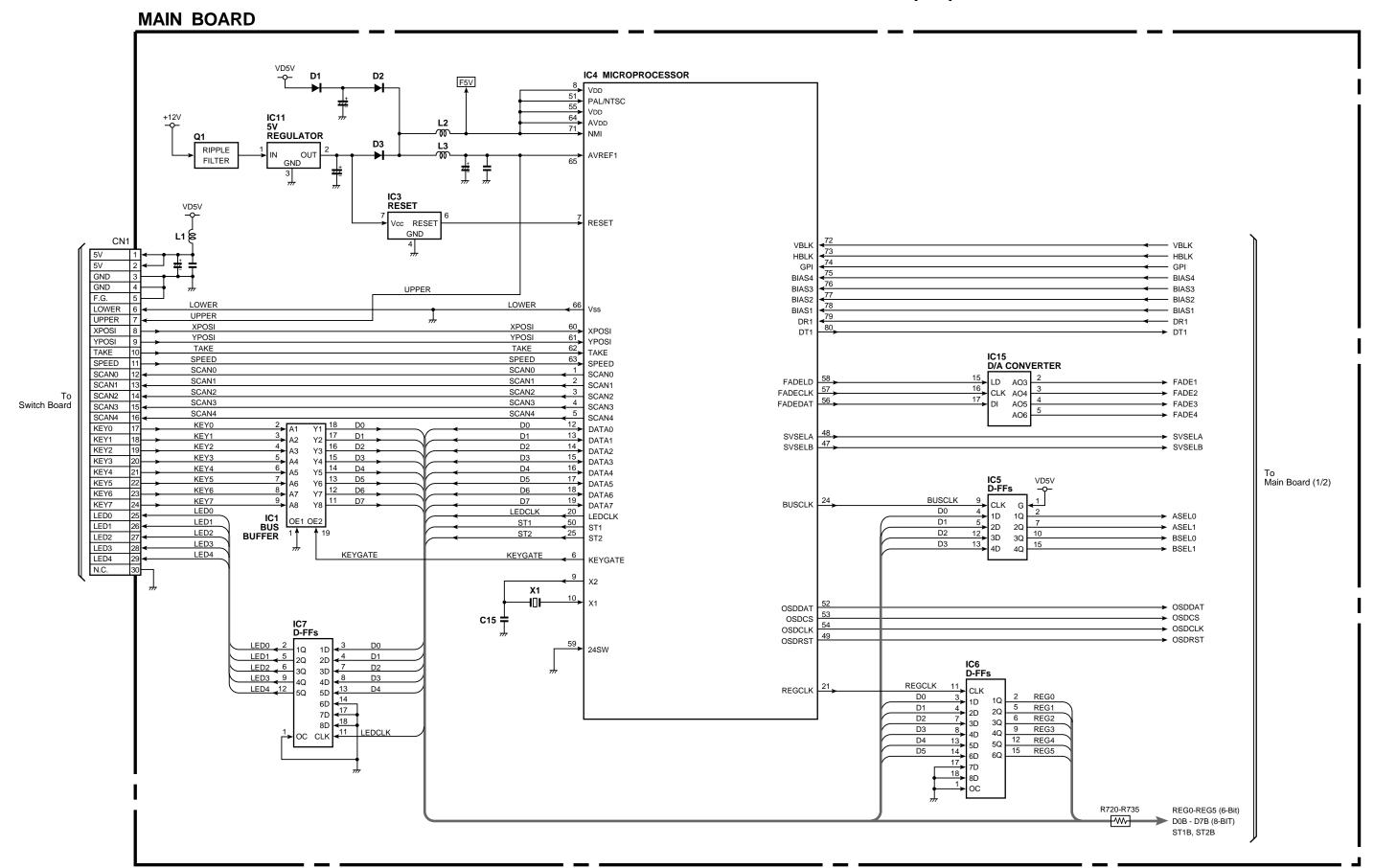
BLOCK DIAGRAM OF SWITCH BOARD



BLOCK DIAGRAM OF MAIN BOARD (1/2)



BLOCK DIAGRAM OF MAIN BOARD (2/2)



EXPLODED VIEW

