

MN74HC00/MN74HC00S

Quad 2-Input NAND Gates

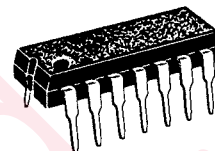
■ Outline

The MN74HC00/MN74HC00S is a 2-input positive logic NAND gate having four built-in circuits in one chip. Owing to the silicon gate CMOS process, this NAND gate has realized low power consumption and high noise immunity equivalent to those of a standard CMOS and the operation speed as high as of an LS TTL. The buffer added to the gate output improves the input/ output transfer characteristic and minimizes the propagation delay time fluctuation caused by the load capacity increase. The MN74HC00/MN74HC00S can directly drive ten LS TTL inputs. To protect the input and output against electrostatic breakdown, a resistor and a diode are used for the V_{CC} and the GND. The pin configuration and the function are the same as those of the standard 54LS/74LS logic family.

■ Logic Diagram (1 Gate)

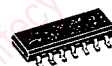


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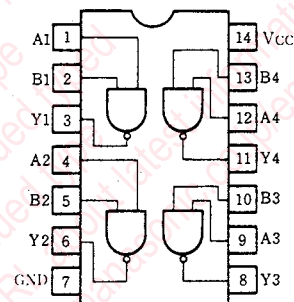
14-pin plastic DIL package

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14-pin PANAFLAT package (SO-14D)

Pin Configuration



■ Absolute Maximum Ratings

Item			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input output voltage			V_I, V_O	$-0.5 \sim V_{CC} + 0.5$	V
Input protective diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 25	mA
Supply current			I_{CC}, I_{GND}	± 50	mA
Storage temperature			T_{stg}	$-65 \sim +150$	$^{\circ}\text{C}$
Power dissipation	MN74HC00	$T_a = -40 \sim +60^{\circ}\text{C}$	P_D	400	mW
		$T_a = +60 \sim +85^{\circ}\text{C}$		Decrease to 200mW at the rate of $8\text{mW}/^{\circ}\text{C}$	
	MN74HC00S	$T_a = -40 \sim +60^{\circ}\text{C}$	P_D	275	mW
		$T_a = +60 \sim +85^{\circ}\text{C}$		Decrease to 200mW at the rate of $3.8\text{mW}/^{\circ}\text{C}$	

■ Recommended Operating Conditions

Item	Symbol	V _{CC} (V)	Rating	Unit
Operating power supply voltage	V _{CC}		1.4~6.0	V
Input output voltage	V _I , V _O		0~V _{CC}	V
Operating temperature	T _A		-40~+85	°C
Input rise, fall time	t _r , t _f	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

■ DC Characteristics (GND=0V)

Item	Symbol	V _{CC} (V)	Test Condition			Temperature					Unit
			V _I	I _O	Unit	Ta=25°C			Ta=-40~+85°C		
						min.	typ.	max.	min.	max.	
Input voltage high level	V _{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input voltage low level	V _{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output voltage high level	V _{OH}	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V _{IH}	-20.0	μA	4.4	4.5		4.4		
		6.0	or	-20.0	μA	5.9	6.0		5.9		
		4.5	V _{IL}	-4.0	mA	3.92			3.84		
		6.0		-5.2	mA	5.48			5.34		
Output voltage low level	V _{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0	V _{IH}	20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.26		0.33	
		6.0		5.2	mA			0.26		0.33	
Input leakage current	I _I	6.0	V _I =V _{CC} or GND					±0.1		±1.0	μA
Static supply current	I _{CC}	6.0	V _I =V _{CC} or GND, I _O =0					2.0		20.0	μA

■ AC Characteristics (GND=0V, Input transition time ≤ 6ns, C_L=50pF)

Item	Symbol	V _{CC} (V)	Test Condition	Temperature					Unit
				Ta=25°C			Ta=-40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t _{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t _{THL}	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t _{PLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t _{PHL}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

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