IEEE/ACM MLCAD 2023
FPGA MACRO-PLACEMENT CONTEST
CALL FOR PARTICIPATION

Macro placement plays an integral role in routability and timing closure in both the ASIC and FPGA physical design flows. In particular, the discrete and columnated nature of the FPGA device layout presents unique placement constraints on placeable macros (e.g., BRAM's, DSP's, URAM's, cascaded shapes, etc.). These constraints are challenging for classical optimization and combinatorial approaches, and often the generated floorplans result in netlist design placements with routing and timing closure issues. Inspired by recent deep reinforcement learning (RL) approaches (e.g. https://arxiv.org/abs/2004.10746), the goal of the competition is to spur academic research for developing ML or deep RL approaches to improve upon the current state-of-the-art macro placement tools.

BENCHMARK SUITE DATASET:

The organizers will provide a public benchmark suite dataset (180 designs) using enhanced bookshelf format. There will also be an unpublished blind benchmark suite dataset totally 60 designs. Please refer to https://github.com/TILOS-AI-Institute/MLCAD23-FPGA-Macro-Placement-Contest/blob/main/Documentation/BenchmarkFileFormat.md for a full description of the file format. Each design in the benchmark suite contains the following files:

1. design.nodes: Specifies placeable instances in the netlist (in Bookshelf format).
2. design.nets: Specifies the set of nets in the netlist (in Bookshelf format).
3. design.lib: Specifies the cell library for placeable objects.
4. design.pl: Specifies the site locations of the macros including cascaded macro shape instances, I/O, and fixed objects. This supplied file only contains locations of fixed instances (IBUF/OBUF/BUFGCE etc.). Your task is to supply the locations of the placeable macro instances. Valid locations for macro (and cascaded shape) instances are prescribed in the design.scl file.
5. sample.pl: Specifies a macro placement sample reference solution.
6. design.scl: Extended from the original bookshelf format to represent xcvu3p device layout and permissible site locations for all placeable object types (please refer to Figure 1).
7. design.cascade_shape: Specifies the types of placeable cascaded macro shapes.
8. design.cascade_shape_instances: Specifies the netlist instances of cascaded macro shapes.
9. design.regions: Specifies the box region constraints imposed on placeable objects
10. design.dcp: This file contains the synthesized netlist checkpoint that is required as an input by the Vivado© executable.
11. place_route.tcl: A TCL script to place and route a netlist using the Vivado© flow leveraging the input macro placement solution.

PUBLIC BENCHMARK DATASET LOCATION:

You can download the public benchmark dataset from Kaggle:

https://www.kaggle.com/datasets/ismailbustany/mlcad-2023-fpga-macro-placement-contest-dataset

FPGA DEVICE DESCRIPTION:

The FPGA architecture used in the contest will be based on an UltraScale+© xcvu3p monolithic device (please refer to the UltraScale Architecture and Product Data Sheet: Overview (DS890) (xilinx.com) documentation for more details). The organizers reserve the right to modify the contents of the benchmark designs and format.

EVALUATION METRICS:

The macro placement solution produced by participating placers will be evaluated using the Vivado© physical design compiler. Contestant teams will be provided with a Vivado© license and a place-and-route flow that reads an input macro placement in the extended bookshelf format, check macro placement legality, and perform standard cell placement and routing. The place-and-route flow will be non-timing driven for this contest. The macro placement solution will be evaluated based on the following criteria:

1. Legality of the macro placement
2. Total routed wirelength and routing congestion metrics (within a time-out limit of 6 hours)
3. Macro placement runtime
4. Total placement and routing runtime of the Vivado© place and route flow

The scores will be tallied based on performance on both the publicly released benchmark dataset (180 designs) and an unpublished blind benchmark dataset (60 designs). Further details will be provided on the contest's website: https://github.com/TILOS-AI-Institute/MLCAD23-FPGA-Macro-Placement-Contest.

MACRO-PLACEMENT SOLUTION GUIDELINES:

We encourage teams to develop a ML-based approach, but teams are free to use any approach (e.g., classical optimization, combinatorial, ML, RL, etc.) for their macro-placement solution.

RELEVANT CONTEST DATES:

Please make note of the following dates:

- **04/15/2023**: The Benchmark suite dataset will be provided.
- **05/15/2023**: Registration deadline
- **07/15/2023**: Each team must submit an alpha binary submission for test purposes, otherwise will be disqualified from the contest.
- **08/15/2023**: Teams must submit their final executable binaries by 11:59pm (pacific time).
- The contest results will be announced during the 2023 MLCAD Workshop on 09/13/2023.

CONTEST REGISTRATION:

To register your team, please provide the following information:

1. Please add "MLCAD2023" to the subject of any email
2. Affiliation of the team/contestant(s)
3. Names of team members and advising professor
4. One correspondence e-mail address for the team
5. Name of the macro placer
6. To participate in the contest and obtain a 1-year Vivado© license, the teams' advising professors must register their team through the export compliant Xilinx University Program, https://www.xilinx.com/support/university/donation-program.html.

PRIZES:

Prizes will be awarded to the top three teams. More details on this will be announced on the web site. Prizes will be awarded to the top 5 teams at the 2023 MLCAD Workshop.

Final Prizes

1st Place:	$2,500
2nd Place:	$1,500
3rd Place:	$1,000
4th/5th Places:	$500

Important note on prizes:

1. 40% of each Final Prize is awarded for performance in the contest according to the defined evaluation metric. The remaining 60% is awarded if the team publishes their winning software as open source under a permissive open-source license (BSD, MIT, Apache), within 30 days of being announced as a winner.

2. Applicable taxes may be assessed on and deducted from award payments, subject to U.S. government policies

CONTEST WEBSITE:

https://github.com/TILOS-AI-Institute/MLCAD23-FPGA-Macro-Placement-Contest

E-MAIL CONTACT:

For registration and contest related inquiries, please email: mlcad2023contest@gmail.com

CONTEST COMMITTEE:

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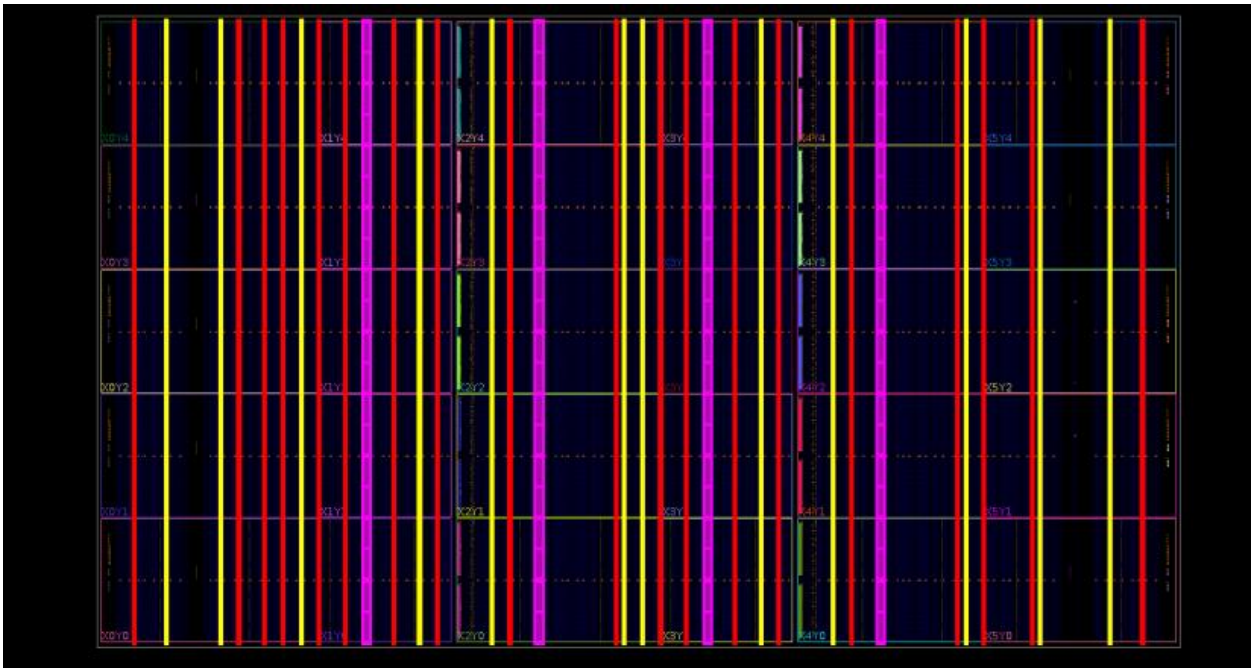

Figure 1: This figure depicts the xcvu3p color-coded macro columnar placement sites for URAM's (magenta), BRAM's (yellow) and DSP's (red).