IEEE/ACM MLCAD 2023
MACROPLACEMENT STUDENT CONTEST

CALL FOR PARTICIPATION

Registration start date: TBD

Registration deadline: TBD

Github site: TBA

E-mail: TBD

Macro placement plays a key role in routability and timing closure for both the ASIC and FPGA the physical design flows. In particular, the discrete and columnated nature of the FPGA device layout presents unique placement constraints on placeable macros (e.g. BRAM's, DSP's, URAM's, cascaded shapes, etc.). These constraints are challenging for classical optimization and combinatorial approaches, and often the floorplans result in designs with routing and timing closure issues. Inspired by recent deep reinforcement learning (RL) approaches (e.g. https://arxiv.org/abs/2004.10746), the goal of the competition is to spur academic research for developing ML or deep RL approaches to improve upon the current state of the arts.

BENCHMARK DESCRIPTION:

The organizers will provide a benchmark suite using enhanced bookshelf format. Each design in the benchmark suite contains the following files:

1) design.nodes: Specifies placeable instances in the design (in Bookshelf format)
2) design.nets: Specifies the set of nets in the design (in Bookshelf format)
3) design.lib: Specifies the cell library for placeable objects
4) design.pl: Specifies the site locations of the macro and cascaded macro shape instances including I/O and fixed objects (please refer to Figure 1).
5) sample.pl: Specifies a sample reference macro placement
6) design.scl: Extended from the original bookshelf format to represent FPGA placeable area and architecture specific placement information
7) design.cascade_shape: Specifies the types of cascaded macro shapes that must be placed together
8) design.cascade_shape_instances: Specifies cascaded macro shape instances.
9) design.regions: Specifies box region constraints imposed on placeable objects
10) design.dcp: Vivado-specific input binary file for the synthesized netlist
11) place_route.tcl: A TCL script to place and route designs in the Vivado flow using the input macro placement

The FPGA architecture used in the contest will be based on an UltrascalePlus xcvu3p monolithic device. The organizers reserve the right to modify the contents of the benchmark designs and format.

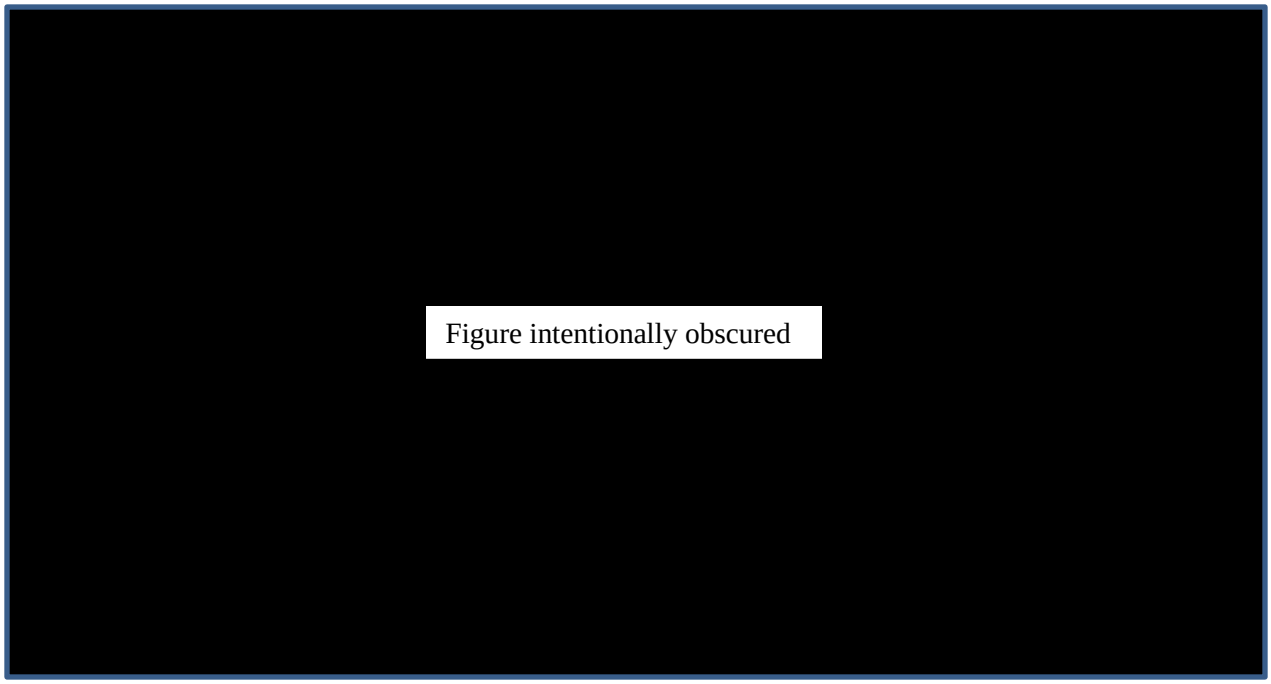

Figure 1: This figure depicts the layout for the xcvu3p and a color-coded macro columnar placement site map for URAM's (magenta), BRAM's (yellow) and DSP's (red).

Note: Teams are encouraged to develop a deep RL-based approach, but are free to use any approach (e.g. classical optimization, combinatorial, ML, RL, etc.) for their macro placement solution.

RELEVANT CONTEST DATES:

Please make note of the following dates:

- To test your tools, a sample benchmark will be provided by ~~February 1st, 2023.~~
- More testing benchmarks will be released by ~~February 15th, 2023~~
- To officially participate, contestants must register by ~~March 1st, 2023~~
- Each team must submit an alpha binary submission by ~~June 1st, 2023~~ for testing purposes, else will be disqualified from the contest.
- Teams are required to submit their final executable binaries by midnight ~~September 15th, 2023~~.
- The contest results will be announced during MLCAD 2023.

CONTEST REGISTRATION:

- For registration and contest related inquiries, please email: TBD.
- Please add "MLCAD2023" to the subject line of any email.
- To register your team, please provide the following information:

1. Affiliation of the team/contestant(s)
2. Names of team members and advising professor

3. One correspondence e-mail address for the team
4. Name of the macro placer
5. To participate in the contes and obtain a 1-year Vivado license, advising professors must register their team through the export compliant university program https://www.xilinx.com/support/university/donation-program.html).

PRIZES:

Monetary prizes will be awarded to the top three teams. More details on this will be announced on the web site.

CONTEST COMMITTEE:

Ismail Bustany (Chair)

Meghraj Kalase
Wuxi Li
Grigor Gasparyan
Amit Gupta

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