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IEEE/ACM MLCAD 2023
FPGA MACROPLACEMENT CONTEST
CALL FOR PARTICIPATION

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Registration start date: 03/15/2023

Registration deadline: 04/15/2023

GitHub site: https://github.com/TILOS-AI-Institute/MLCAD23-FPGA-Macro-Placement-Contest

E-mail: mlcad2023contest@gmail.com

Benchmark Suite Dataset: https://www.kaggle.com/datasets/ismailbustany/mlcad2023-fpga-macroplacement-contest/settings?resource=download

Macro placement plays an integral role in routability and timing closure for both the ASIC and FPGA physical design flows. In particular, the discrete and columnated nature of the FPGA device layout presents unique placement constraints on placeable macros (e.g. BRAM's, DSP's, URAM's, cascaded shapes, etc.). These constraints are challenging for classical optimization and combinatorial approaches, and often the floorplans result in designs with routing and timing closure issues. Inspired by recent deep reinforcement learning (RL) approaches (e.g. https://arxiv.org/abs/2004.10746), the goal of the competition is to spur academic research for developing ML or deep RL approaches to improve upon the current state-of-the-art macro placement tools.

BENCHMARK DESCRIPTION:

The organizers will provide a benchmark suite using enhanced bookshelf format. Please refer to https://github.com/TILOS-AI-Institute/MLCAD23-FPGA-Macro-Placement-Contest/blob/main/Documentation/BenchmarkFileFormat.md for a full description of the file format. Each design in the benchmark suite contains the following files:

1) design.nodes: Specifies placeable instances in the netlist (in Bookshelf format)
2) design.nets: Specifies the set of nets in the netlist (in Bookshelf format)
3) design.lib: Specifies the cell library for placeable objects
4) design.pl: Specifies the site locations of the macros including cascaded macro shape instances, I/O, and fixed objects. This supplied file only contains locations of fixed instances (IBUF/OBUF/BUFGCE etc). Your task is to supply the locations of the placeable macro instances. Valid locations for macro (and cascaded shape) instances are prescribed in the design.scl file.
5) sample.pl: Specifies a macro placement sample reference solution.
6) design.scl: Extended from the original bookshelf format to represent xcvu3p device layout and permissible site locations for all placeable object types (please refer to Figure 1).
7) design.cascade_shape: Specifies the types of placeable cascaded macro shapes.
8) design.cascade_shape_instances: Specifies the netlist instances of cascaded macro shapes.

9) design.regions: Specifies the box region constraints imposed on placeable objects
10) design.dcp: This file contains the synthesized netlist checkpoint that is required as an input by the Vivado© executable.
11) place_route.tcl: A TCL script to place and route a netlist using the Vivado© flow leveraging the input macro placement solution.

FPGA Device: The FPGA architecture used in the contest will be based on an UltrascalePlus xcvu3p monolithic device (please refer to UltraScale Architecture and Product Data Sheet: Overview (DS890) (xilinx.com))The organizers reserve the right to modify the contents of the benchmark designs and format.

MACRO PLACEMENT EVALUTION:

The macro placement solution produced by participating placers will be evaluated using the Vivado© physical design compiler. Contestant teams will be provided with a Vivado© license and a place-and-route flow that reads an input macro placement in the extended bookshelf format, check macro placement legality, and perform standard cell placement and routing. The place-and-route flow will be non-timing driven for this contest. The macro placement solution will be evaluated based on the following criteria:

1) Legality of the macro placement
2) Global and detail routing metrics (within a time-out limit of 6 hours)
3) Total routed wirelength, routing congestion
4) Macro placement runtime
5) Total placement and routing runtime of Vivado© place and route phases.

Further details are provided on https://github.com/TILOS-AI-Institute/MLCAD23-FPGA-Macro-Placement-Contest.

Note: Teams are encouraged to develop a deep RL-based approach, but are free to use any approach (e.g. classical optimization, combinatorial, ML, RL, etc.) for their macro placement solution.

RELEVANT CONTEST DATES:

Please make note of the following dates:

- 03/15/2023: The Benchmark suite dataset will be provided
- 04/15/2023: Registration deadline
- 07/15/2023: Each team must submit an alpha binary submission for test purposes, else will be disqualified from the contest.
- 08/15/2023: Teams are required to submit their final executable binaries by 11:59pm (pacific time).
- The contest results will be announced during MLCAD 2023 on 09/13/2023

CONTEST REGISTRATION:

- For registration and contest related inquiries, please email: mlcad2023contest@gmail.com
- Please add "MLCAD2023" to the subject line of any email.
- To register your team, please provide the following information:

1. Affiliation of the team/contestant(s)
2. Names of team members and advising professor
3. One correspondence e-mail address for the team
4. Name of the macro placer
5. To participate in the contest and obtain a 1-year Vivado license, advising professors must register their team through the export compliant university program: https://www.xilinx.com/support/university/donation-program.html).

PRIZES:

Monetary prizes will be awarded to the top three teams. More details on this will be announced on the web site.

CONTEST COMMITTEE:

Ismail Bustany (Chair)

Meghraj Kalase
Wuxi Li
Grigor Gasparyan
Amit Gupta
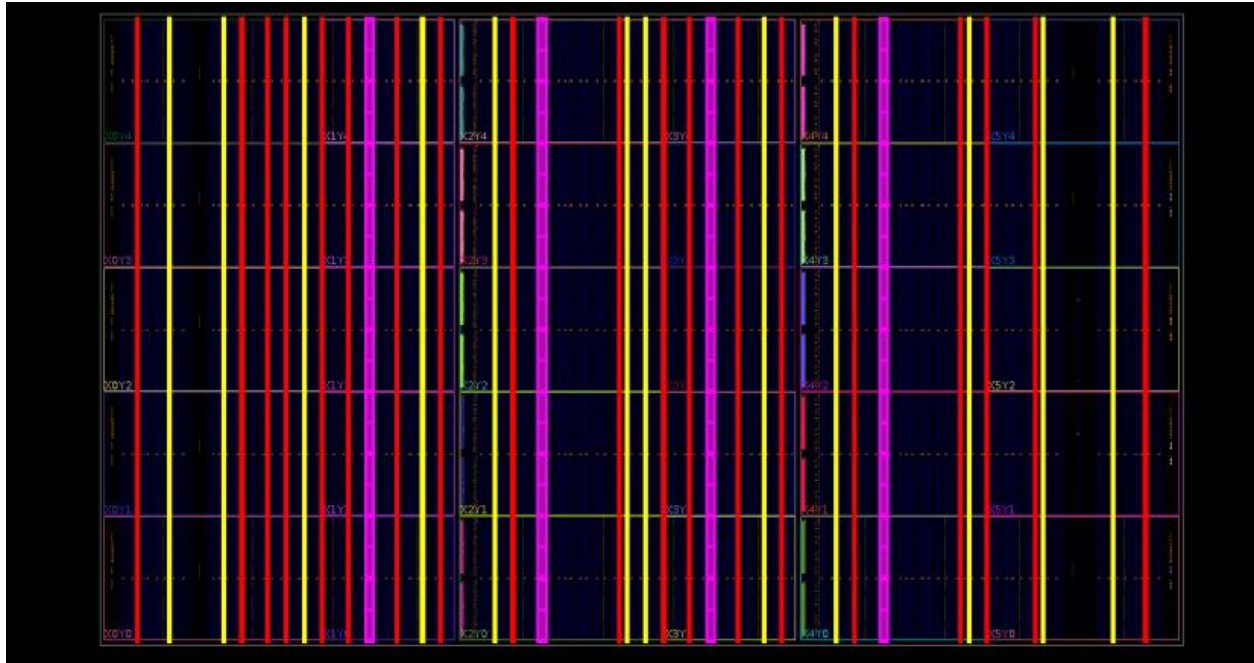Andrew Kahng

ACKNOWLEDGEMENTS:

Figure 1: This figure depicts the xcvu3p color-coded macro columnar placement sites for URAM's (magenta), BRAM's (yellow) and DSP's (red).