



**In Collaboration with UCSD  
(The OpenROAD Project & TILOS AI Institute)**

# **2023 MLCAD FPGA Macro Placement Contest**

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Salt Lake City, Utah

*09/13/2023*

*\*Updated and shared on 10/06/2023*

# Agenda

1. Overview
2. Benchmark Suite
  - Design Specifications
  - Extended Bookshelf Format
3. Evaluation Metrics
4. Participating Teams
  - 1.5 min video presentations
5. Updated Results
  - Public Benchmark Team Scores
  - Hidden Benchmark Team Scores
  - Final Team Rankings
6. Learnings
7. Awards Ceremony!

# Contest Organizing Team

- Ismail Bustany\*
- Meghraj Kalase\*
- Wuxi Li\*
- Grigor Gasparyan \*
- Bodhisatta Pramanik<sup>+</sup>
- Andrew Kahng<sup>+,<sup>τ</sup></sup>
- Amit Gupta\*

## Acknowledgments

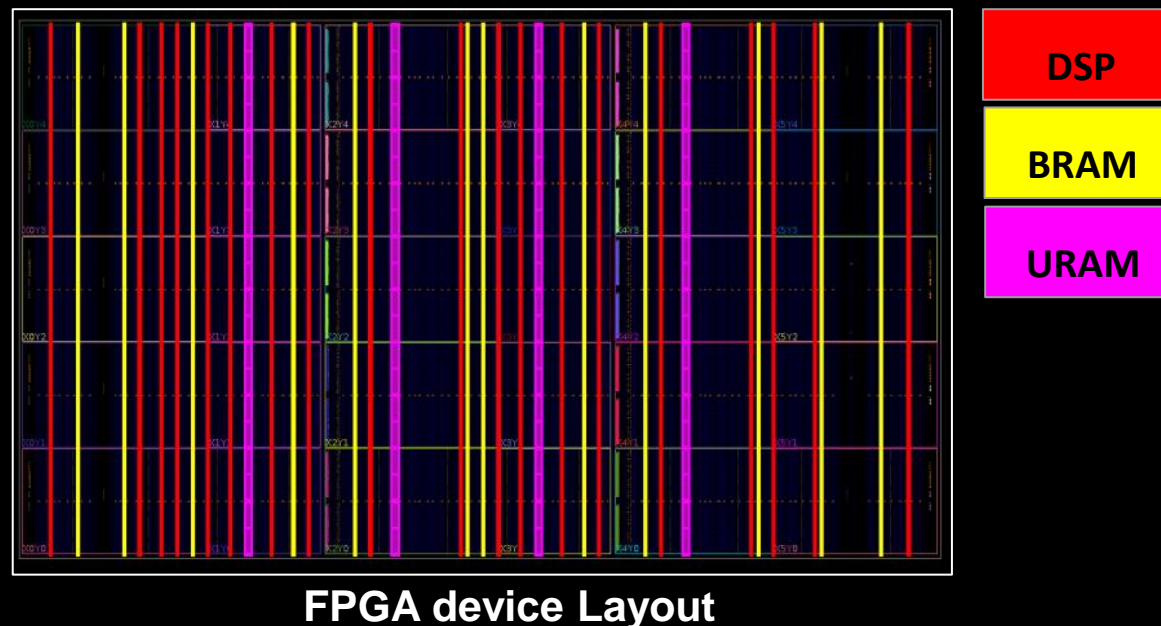
The TILOS AI Institute, Zhiang Wang, Yuji Kukimoto, Sreevidya Maguluri, Ravishankar Menon, Nima Karimpour-Darav, Mehrdad Eslami, Chaithanya Dudha, Lin Chai, Kai Zhu, Kristin Perry, Cathal McCabe, Mark O Brian, and Vishal Suthar for their helpful remarks, advice, and assistance.

## Contest Website

<https://github.com/TILOS-AI-Institute/MLCAD-2023-FPGA-Macro-Placement-Contest>



# Overview



- **Background:** Macro placement is **NP-hard**
  - For FPGA's, there are additional challenges:
    - **Discrete** and site type **columnated** nature of the FPGA device layout
    - **Multiple** clock domains (typically 1 – 100)
    - **1000's** of macros
    - **Multiple** dies
- **Problem:** SOTA algorithms often result in floorplans with **routing and timing closure issues**
- **Goal:** Spur research for developing **ML approaches** that supplant the SOTA

# Overview

- **FPGA Device:** 16nm single-die UltraScale<sup>+</sup> xcvu3p
- **Benchmark suite:** 338 synthetically generated designs
- **Evaluation Metrics:** Macro placement runtime, place-and-route flow runtime, and routability
- **Contest Website:** <https://github.com/TILOS-AI-Institute/MLCAD-2023-FPGA-Macro-Placement-Contest>

## 2. Benchmark Suite

# Benchmark Suite

- Netlists generated synthetically
- Varying levels of difficulty
  - Rent's exponent (0.65, 0.67, 0.7, 0.72)
  - #clocks (1, 16, 24, 30, 34, 38)
  - %utilization
  - LUTs (70, 73, 76, 79, 82, 84)
  - FFs (38, 40, 42, 43, 45, 47)
  - DSP, BRAM (80, 82, 84, 86, 88, 90)
  - URAM's (65, 67, 70, 72)
  - cascaded macro shapes (5, 30, and 60 tall)
- Non-timing-driven
- 140 Publicly released designs (1, 24, 30, and 38 clocks),
  - Download from [https://github.com/TILOS-AI-Institute/MLCAD-2023-FPGA-Macro-Placement-Contest/blob/main/Benchmark\\_Suite/Download\\_Benchmark\\_Suite.md](https://github.com/TILOS-AI-Institute/MLCAD-2023-FPGA-Macro-Placement-Contest/blob/main/Benchmark_Suite/Download_Benchmark_Suite.md)
  - Various bug fixes published on <https://github.com/TILOS-AI-Institute/MLCAD-2023-FPGA-Macro-Placement-Contest/blob/main/Documentation/FAQ.md>
- 198 hidden designs (1, 16, 24, 30, 34, and 38 clocks)
  - To be released after this Workshop



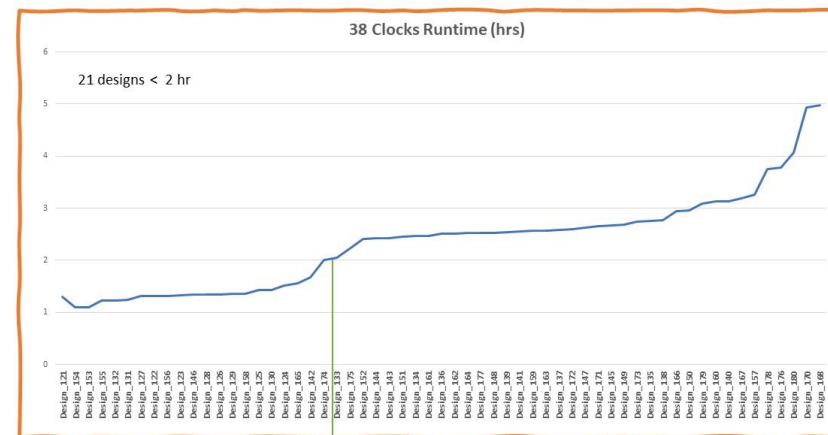
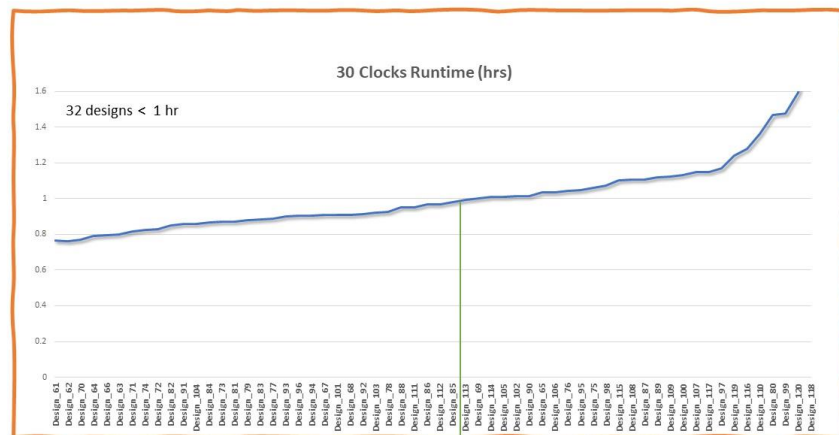
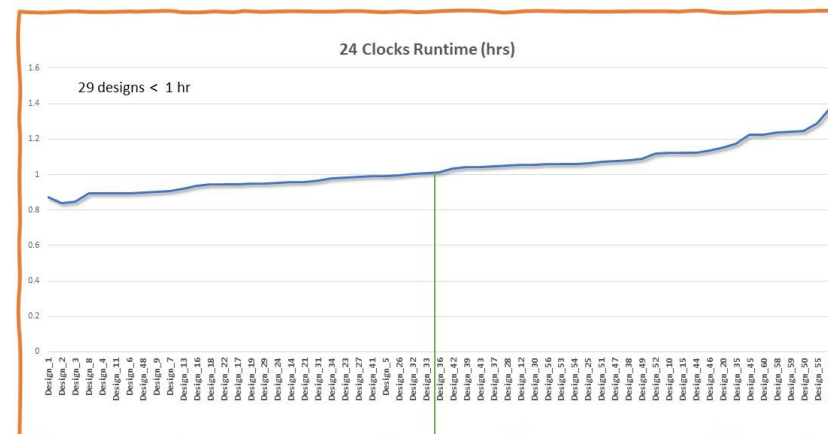
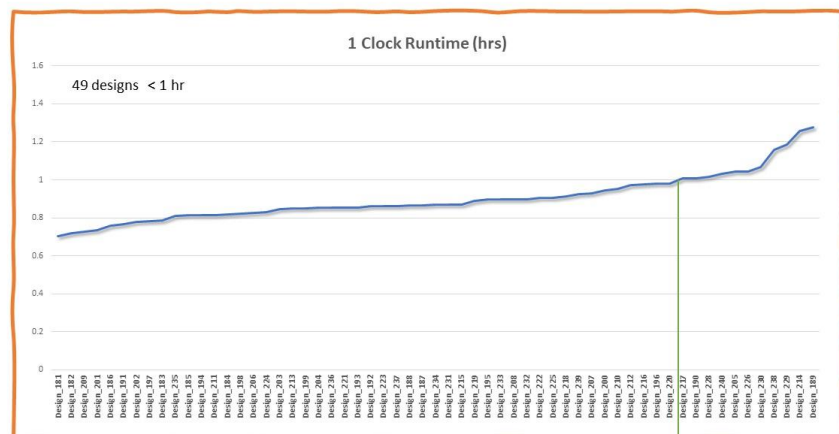
# Sample Netlist Specifications – 1 Clock

| Design     | LUT% | FF% | RAMB% | DSP% | Rept | # Clocks | Runtime (s) | Notes   |
|------------|------|-----|-------|------|------|----------|-------------|---|
| Design_409 | 70   | 38  | 80    | 80   | 0.67 | 1        | 2035        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_410 | 70   | 38  | 80    | 80   | 0.67 | 1        | 2170        | With 2 instances each of semi tall DSP and BRAM |
| Design_411 | 70   | 38  | 80    | 80   | 0.67 | 1        | 2783        | With 4 instances each of tall DSP and BRAM      |
| Design_412 | 70   | 38  | 80    | 80   | 0.72 | 1        | 3269        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_413 | 70   | 38  | 80    | 80   | 0.72 | 1        | 2715        | With 2 instances each of semi tall DSP and BRAM |
| Design_414 | 70   | 38  | 80    | 80   | 0.72 | 1        | 3846        | With 4 instances each of tall DSP and BRAM      |
| Design_415 | 73   | 40  | 82    | 82   | 0.67 | 1        | 3516        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_416 | 73   | 40  | 82    | 82   | 0.67 | 1        | 3067        | With 2 instances each of semi tall DSP and BRAM |
| Design_417 | 73   | 40  | 82    | 82   | 0.67 | 1        | 3621        | With 4 instances each of tall DSP and BRAM      |
| Design_418 | 73   | 40  | 82    | 82   | 0.72 | 1        | 3353        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_419 | 73   | 40  | 82    | 82   | 0.72 | 1        | 3312        | With 2 instances each of semi tall DSP and BRAM |
| Design_420 | 73   | 40  | 82    | 82   | 0.72 | 1        | 4310        | With 4 instances each of tall DSP and BRAM      |
| Design_421 | 76   | 42  | 84    | 84   | 0.67 | 1        | 3028        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_422 | 76   | 42  | 84    | 84   | 0.67 | 1        | 3021        | With 2 instances each of semi tall DSP and BRAM |
| Design_423 | 76   | 42  | 84    | 84   | 0.67 | 1        | 3850        | With 4 instances each of tall DSP and BRAM      |
| Design_424 | 76   | 42  | 84    | 84   | 0.72 | 1        | 3398        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_425 | 76   | 42  | 84    | 84   | 0.72 | 1        | 4972        | With 2 instances each of semi tall DSP and BRAM |
| Design_426 | 76   | 42  | 84    | 84   | 0.72 | 1        | 4564        | With 4 instances each of tall DSP and BRAM      |
| Design_427 | 79   | 43  | 86    | 86   | 0.67 | 1        | 3144        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_428 | 79   | 43  | 86    | 86   | 0.67 | 1        | 3469        | With 2 instances each of semi tall DSP and BRAM |
| Design_429 | 79   | 43  | 86    | 86   | 0.67 | 1        | 2573        | With 4 instances each of tall DSP and BRAM      |
| Design_430 | 79   | 43  | 86    | 86   | 0.72 | 1        | 13027       | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_431 | 79   | 43  | 86    | 86   | 0.72 | 1        | 4624        | With 2 instances each of semi tall DSP and BRAM |
| Design_432 | 79   | 43  | 86    | 86   | 0.72 | 1        | 2937        | With 4 instances each of tall DSP and BRAM      |
| Design_433 | 82   | 45  | 88    | 88   | 0.67 | 1        | 3541        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_434 | 82   | 45  | 88    | 88   | 0.67 | 1        | 3316        | With 2 instances each of semi tall DSP and BRAM |
| Design_435 | 82   | 45  | 88    | 88   | 0.67 | 1        | 4095        | With 4 instances each of tall DSP and BRAM      |
| Design_436 | 82   | 45  | 88    | 88   | 0.72 | 1        | 4342        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_437 | 82   | 45  | 88    | 88   | 0.72 | 1        | 4573        | With 2 instances each of semi tall DSP and BRAM |
| Design_438 | 82   | 45  | 88    | 88   | 0.72 | 1        | 6323        | With 4 instances each of tall DSP and BRAM      |
| Design_439 | 84   | 47  | 90    | 90   | 0.67 | 1        | 3327        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_440 | 84   | 47  | 90    | 90   | 0.67 | 1        | 3376        | With 2 instances each of semi tall DSP and BRAM |
| Design_441 | 84   | 47  | 90    | 90   | 0.67 | 1        | 3728        | With 4 instances each of tall DSP and BRAM      |
| Design_442 | 84   | 47  | 90    | 90   | 0.72 | 1        | 2105        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_443 | 84   | 47  | 90    | 90   | 0.72 | 1        | 3604        | With 2 instances each of semi tall DSP and BRAM |
| Design_444 | 84   | 47  | 90    | 90   | 0.72 | 1        | 3504        | With 4 instances each of tall DSP and BRAM      |
| Design_445 | 84   | 47  | 90    | 90   | 0.72 | 1        | 6626        | With 4 instances each of tall DSP and BRAM      |

# Sample Netlist Specifications – 38 Clocks

| Design     | LUT% | FF% | RAMB% | DSP% | Rent | # Clocks | Runtime (s) | Notes   |
|------------|------|-----|-------|------|------|----------|-------------|---|
| Design_373 | 70   | 38  | 80    | 80   | 0.67 | 38       | 4681        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_374 | 70   | 38  | 80    | 80   | 0.67 | 38       | 4580        | With 2 instances each of semi tall DSP and BRAM |
| Design_375 | 70   | 38  | 80    | 80   | 0.67 | 38       | 5082        | With 4 instances each of tall DSP and BRAM      |
| Design_376 | 70   | 38  | 80    | 80   | 0.72 | 38       | 7635        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_377 | 70   | 38  | 80    | 80   | 0.72 | 38       | 4393        | With 2 instances each of semi tall DSP and BRAM |
| Design_378 | 70   | 38  | 80    | 80   | 0.72 | 38       | 9484        | With 4 instances each of tall DSP and BRAM      |
| Design_379 | 73   | 40  | 82    | 82   | 0.67 | 38       | 3619        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_380 | 73   | 40  | 82    | 82   | 0.67 | 38       | 3123        | With 2 instances each of semi tall DSP and BRAM |
| Design_381 | 73   | 40  | 82    | 82   | 0.67 | 38       | 4886        | With 4 instances each of tall DSP and BRAM      |
| Design_382 | 73   | 40  | 82    | 82   | 0.72 | 38       | 6874        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_383 | 73   | 40  | 82    | 82   | 0.72 | 38       | 4502        | With 2 instances each of semi tall DSP and BRAM |
| Design_384 | 73   | 40  | 82    | 82   | 0.72 | 38       | 6578        | With 4 instances each of tall DSP and BRAM      |
| Design_385 | 76   | 42  | 84    | 84   | 0.67 | 38       | 5126        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_386 | 76   | 42  | 84    | 84   | 0.67 | 38       | 4474        | With 2 instances each of semi tall DSP and BRAM |
| Design_387 | 76   | 42  | 84    | 84   | 0.67 | 38       | 5464        | With 4 instances each of tall DSP and BRAM      |
| Design_388 | 76   | 42  | 84    | 84   | 0.72 | 38       | 5591        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_389 | 76   | 42  | 84    | 84   | 0.72 | 38       | 16205       | With 2 instances each of semi tall DSP and BRAM |
| Design_390 | 76   | 42  | 84    | 84   | 0.72 | 38       | 6680        | With 4 instances each of tall DSP and BRAM      |
| Design_391 | 79   | 43  | 86    | 86   | 0.67 | 38       | 4833        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_392 | 79   | 43  | 86    | 86   | 0.67 | 38       | 5460        | With 2 instances each of semi tall DSP and BRAM |
| Design_393 | 79   | 43  | 86    | 86   | 0.67 | 38       | 5089        | With 4 instances each of tall DSP and BRAM      |
| Design_394 | 79   | 43  | 86    | 86   | 0.72 | 38       | 7501        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_395 | 79   | 43  | 86    | 86   | 0.72 | 38       | 7339        | With 2 instances each of semi tall DSP and BRAM |
| Design_396 | 79   | 43  | 86    | 86   | 0.72 | 38       | 6416        | With 4 instances each of tall DSP and BRAM      |
| Design_397 | 82   | 45  | 88    | 88   | 0.67 | 38       | 3496        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_398 | 82   | 45  | 88    | 88   | 0.67 | 38       | 4707        | With 2 instances each of semi tall DSP and BRAM |
| Design_399 | 82   | 45  | 88    | 88   | 0.67 | 38       | 4710        | With 4 instances each of tall DSP and BRAM      |
| Design_400 | 82   | 45  | 88    | 88   | 0.72 | 38       | 5705        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_401 | 82   | 45  | 88    | 88   | 0.72 | 38       | 6729        | With 2 instances each of semi tall DSP and BRAM |
| Design_402 | 82   | 45  | 88    | 88   | 0.72 | 38       | 5856        | With 4 instances each of tall DSP and BRAM      |
| Design_403 | 84   | 47  | 90    | 90   | 0.67 | 38       | 5910        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_404 | 84   | 47  | 90    | 90   | 0.67 | 38       | 5397        | With 2 instances each of semi tall DSP and BRAM |
| Design_405 | 84   | 47  | 90    | 90   | 0.67 | 38       | 4051        | With 4 instances each of tall DSP and BRAM      |
| Design_406 | 84   | 47  | 90    | 90   | 0.72 | 38       | 4941        | No tall BRM/ DSP/ URAM/ Carries                 |
| Design_407 | 84   | 47  | 90    | 90   | 0.72 | 38       | 6277        | With 2 instances each of semi tall DSP and BRAM |
| Design_408 | 84   | 47  | 90    | 90   | 0.72 | 38       | 6020        | With 4 instances each of tall DSP and BRAM      |

# Sample Baseline Place-and-Route Flow Runtimes



# Benchmark Suite Extended Bookshelf Format

|     | File name                             | Description   |
|-----|---------------------------------------|---|
| 1.  | <b>design.nodes</b>                   | Specifies placeable instances in the netlist (in Bookshelf format)  |
| 2.  | <b>design.nets</b>                    | Specifies the set of nets in the netlist (in Bookshelf format)  |
| 3.  | <b>design.lib</b>                     | Specifies the cell library for placeable objects  |
| 4.  | <b>design.pl</b>                      | Specifies the site locations of the macros including cascade macro shape instances, I/O, and fixed objects. This file only contains locations of fixed instances (IBUF/OBUF/BUFGCE etc.). Your task is to supply the locations of the placeable macro instances. Valid locations for macro (and cascade shape) instances are prescribed in the design.scl file. |
| 5.  | <b>sample.pl</b>                      | Specifies a macro placement sample reference solution.  |
| 6.  | <b>design.scl</b>                     | Extended from the original Bookshelf format to represent xcvu3p device layout and permissible site locations for all placeable object types (please refer to Figure 1).   |
| 7.  | <b>design.cascade_shape</b>           | Specifies the types of placeable cascade macro shapes.  |
| 8.  | <b>design.cascade_shape_instances</b> | Specifies the netlist instances of cascade macro shapes (not provided if no cascade shapes are present in the netlist).   |
| 9.  | <b>design.regions</b>                 | Specifies the box region constraints imposed on placeable objects.  |
| 10. | <b>design.dcp</b>                     | This file contains the synthesized netlist checkpoint that is required as an input by the Vivado© executable.   |
| 11. | <b>vivado_pnr.tcl</b>                 | A TCL script to place and route a netlist using the Vivado© flow leveraging the input macro placement solution.   |
| 12. | <b>design.macros</b>                  | The names of placeable macro blocks in this design.   |

For details please visit: <https://github.com/TILOS-AI-Institute/MLCAD-2023-FPGA-Macro-Placement-Contest>

### **3. Evaluation Metrics**

# Evaluation Metrics

## ➤ Per Design:

- **Score** = runtime(macro placement) x runtime(place-and-route flow) x routability
- $\text{runtime}(\text{macro placement}) = 1 + \max(0, \text{macroplacement}_{\text{runtime}_i} - 10)$  (in mins)
  - Penalty only incurred if macro placement runtime > 10 mins
- runtime (place-and-route flow) = runtime of place-and-route flow in hours

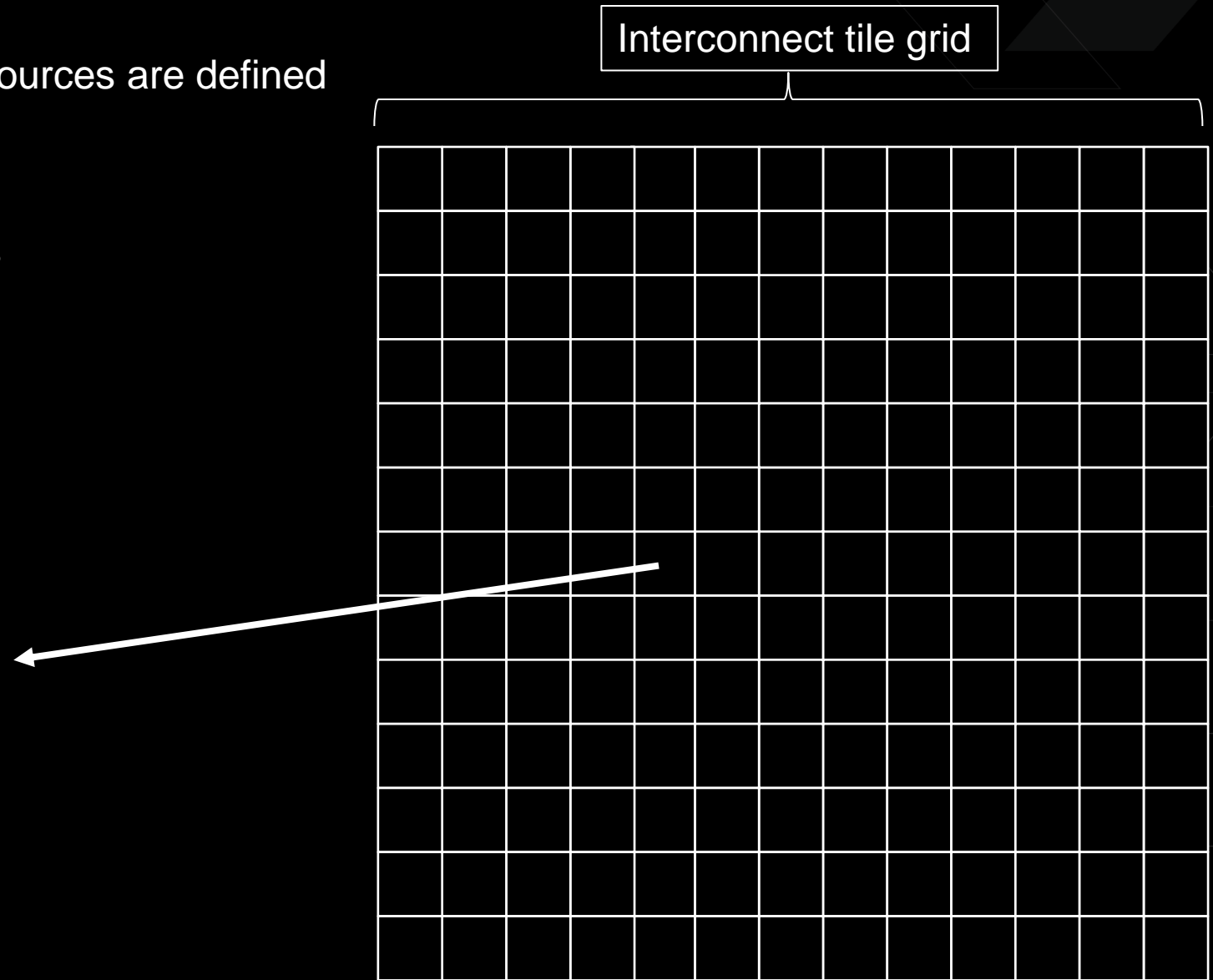
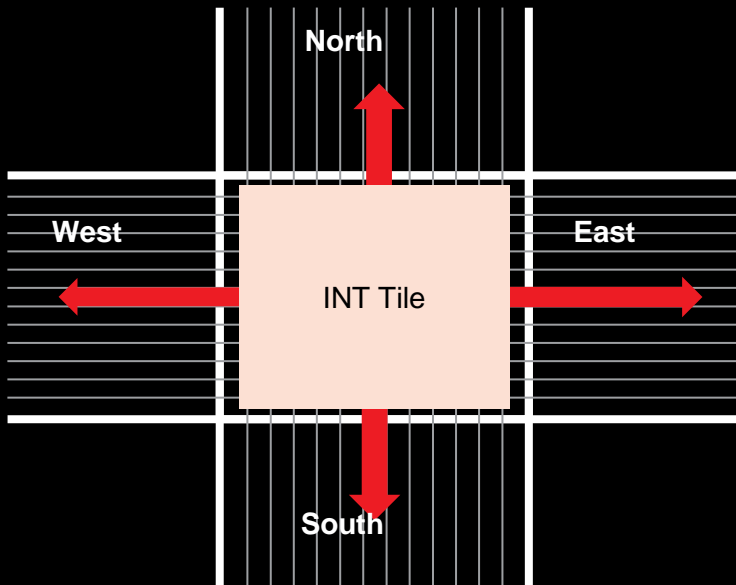
## ➤ Per Team:

- Final Team Score = Weighted geometric mean of all design scores

## ➤ *Lower is better*

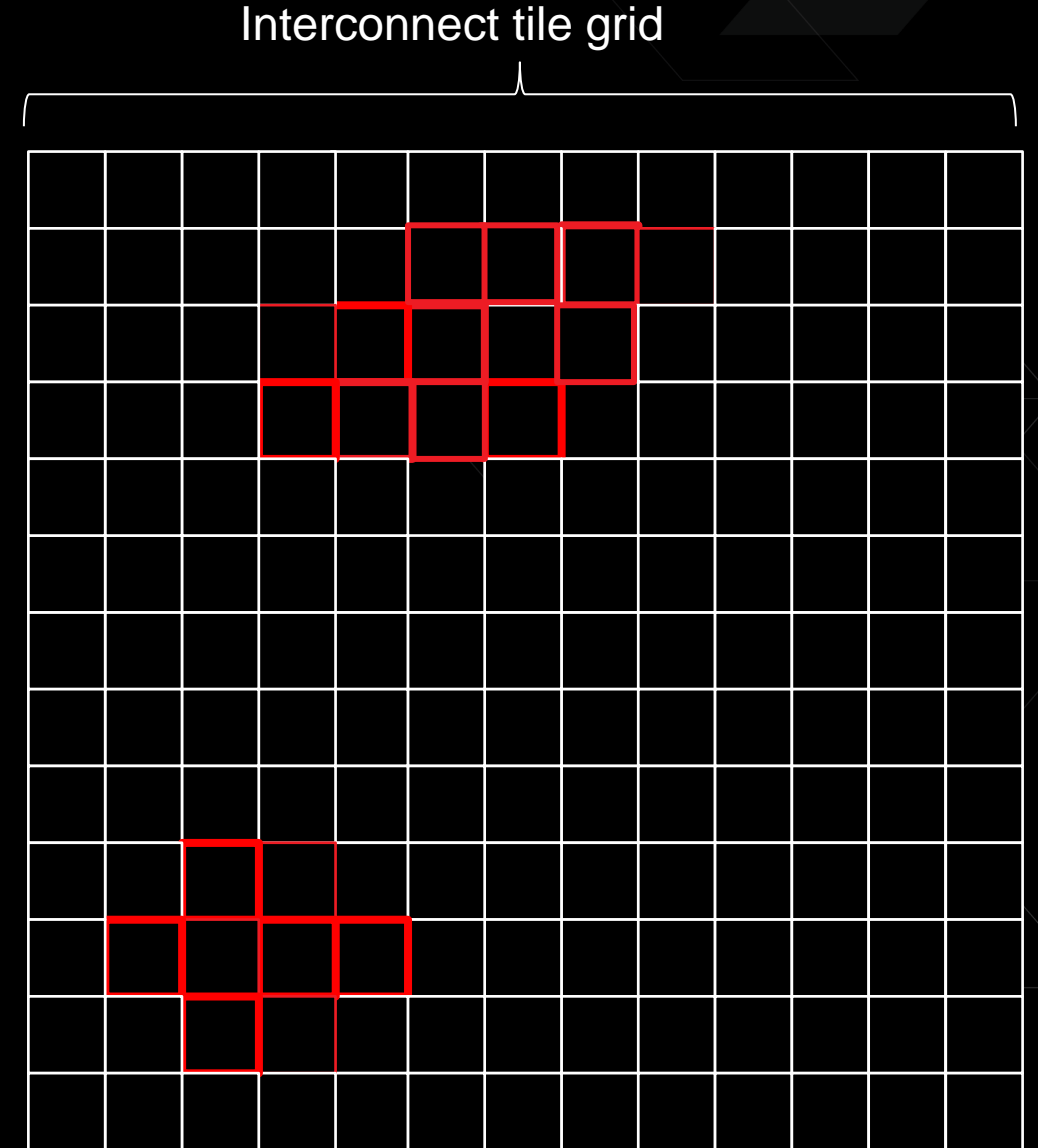
# Evaluation Metrics - Interconnect Tile Grid

- Tile grid where device interconnect resources are defined
- Interconnect tile grid routing resources:
  - **Short:** wires spanning 1-4 tiles
  - **Long:** wires spanning 8 or more tiles



# Evaluation Metrics - What is routing congestion?

- Congestion = Oversubscription of interconnect routing resources
- As the demand region grows, the router struggles to find a feasible solution

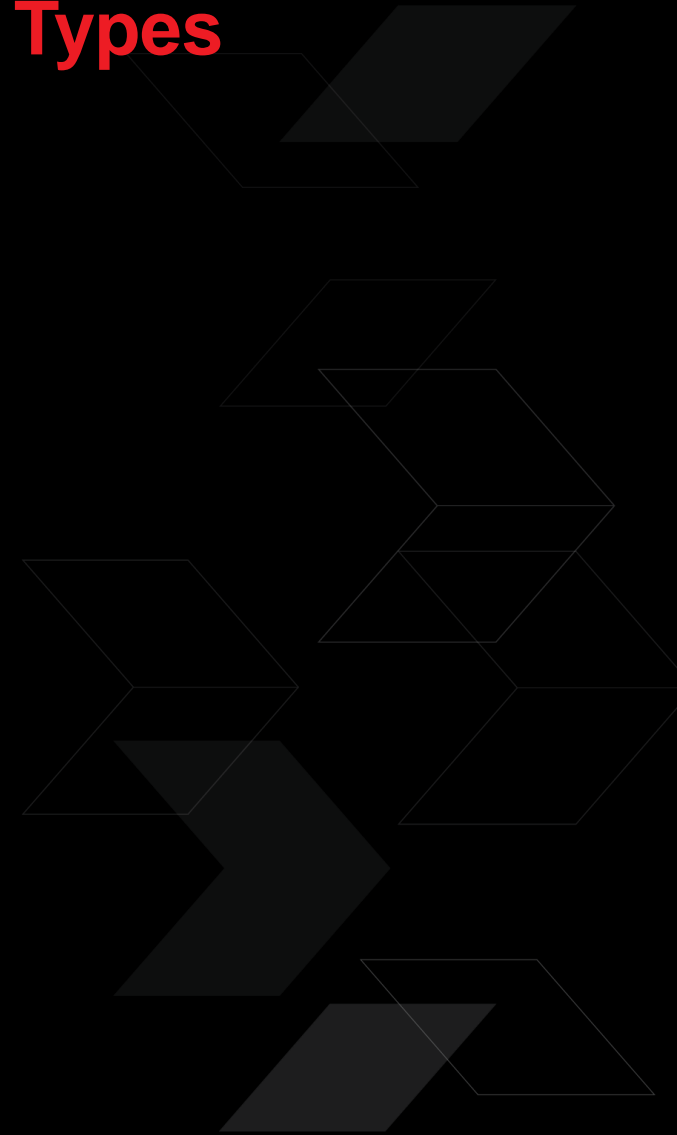




# Evaluation Metrics - Interconnect Tile Congestion Types

Congestion is typed by interconnect length and wire direction (N, S, E, W)

- **Short** congestion
  - Typically caused by “closely clustered cell placements”
  - Potentially leads to routability issues
- **Long** congestion
  - Typically caused by “long spread-out cell placements”
  - Potentially leads to timing and routability issues
- **Global** congestion
  - Aggregation of short and long congestion



# Evaluation Metrics – Routability Score Per Design

- **Routability** = initial\_routing\_score x final\_routing\_score
- **initial\_routing\_score:**

| Wire Direction | Global Congestion |         | Long Congestion |         | Short Congestion |         |
|----------------|-------------------|---------|-----------------|---------|------------------|---------|
|                | Size              | % Tiles | Size            | % Tiles | Size             | % Tiles |
| <b>NORTH</b>   | 32x32             | 4.79    | 128x128         | 20.18   | 4x4              | 1.33    |
| <b>SOUTH</b>   | <b>16x16</b>      | 3.87    | 128x128         | 20.03   | 4x4              | 0.96    |
| <b>EAST</b>    | 32x32             | 5.22    | 64x64           | 18.83   | 8x8              | 3.28    |
| <b>WEST</b>    | 32x32             | 8.29    | 128x128         | 23.46   | 4x4              | 4.50    |

- **Congestion level 4** means there is **16 x16** interconnect tile grid that is congested
- **We only penalize congestion levels > 3**

$$\text{initial routing score} = 1 + \sum_{i=1}^4 [\max(0, \text{short level}_i - 3)^2 + \max(0, \text{global level}_i - 3)^2]$$

- **final\_routing\_score** = No. final router outer iterations
- Unplaceable and unroutable designs are penalized with a score of 500

## 4. Participating Teams

# Participating Teams

- 19 participants – 3@Canada, 6@China, 2@Hong Kong, 1@India, 1@Korea, 1@Taiwan, and 5@USA
- 8 finalists (6 of which are competitive)

| Team   | University   | Professor                        | Members   |
|--------|--|----------------------------------|---|
| TAMU   | Texas A & M  | Jiang Hu                         | Hailiang Hu, Donghao Fang, Yishuang Lin   |
| MPKU   | Peking University                                  | Yibo Lin                         | Jing Mai, Jiarui Wang, Xun Jiang, Zizheng Guo, Yifan Chen                       |
| CUMPLE | CUHK   | Evangeline F.Y. Young            | Qin Luo, Xinshi Zang, Qijing Wang, Fangzhou Wang                                |
| Pomelo | Nanjing University of Posts and Telecommunications | Jieming Yin                      | Hao Wu, Linhua Tao  |
| DAG-MP | Shanghai Jiao Tong University                      | Xinfei Guo                       | Xiaotian Zhao, Tianju Wang, Yuia Sun, Xinfei Guo                                |
| MacroM | Nirma University                                   | Manish I. Patel                  | Jaydeep Solanki, Jugal Gandhi, Pranav Kotadia, Riththika Sukanandan             |
| MacroD | Pohang University                                  | Seokhyeong Kang                  | Junseok Hur, Seongbin Kwon, Jaeseung Lee, JoonSeok Kim, Kyumin cho              |
| IMR    | Not provided                                       | Liang Yi                         | Fu Mingjian, Ma Jimiao  |
| SEU    | Southeast University                               | Ziran Zhu, Jun Yang, Jianli Chen | Hao Gu, Jian Gu, Yuxian Yue   |
| GoFish | Georgia Tech                                       | Callie Hao                       | Stefan Abi-Karam  |
| EFM    | University of Calgary                              | Laleh Behjat                     | Erfan Aghaeekiasaraee   |
| BO     | University of Illinois-Urbana Champaign            | Elyse Rosenbaum                  | Michael Molter  |
| Duke   | Duke University                                    | Yiran Chen                       | Guangle i Zhou, Jingyu Pan, Chen-Chia Chang, Yiran Chen                         |
| UBCP   | UBC  | Steven Wilton                    | Andrew Gunter, Martin Chua, Nikhil Ghanathe, Elmira Nezamfar, Roozmehr Jalilian |
| GD     | Dalian University of Technology                    | Yan Xing, Weijun Li              | Yihao Huang, Juming Xian, Zhihao Chen, Wenhao Liu, Zhongnuo Wang                |
| MacroW | Simon Fraser University                            | Behnam Ghavami and Lesley Shanon | Mani Sadati, Mohammad Sahidzade, and Saba Jahan-Tighi.                          |
| CUMP   | CUHK   | Bei Yu, Tinghuan Chen            | Yuan Pu, Hongduo Liu, Mingjun Li, Lanchen Zou                                   |
| UTDA   | UT Austin  | David Pan                        | Zhili Xiong, Rachel S. Rajarathnam, Zhixing Jiang, Hanqing Zhu                  |
| NTHU   | National Tsing Hua University                      | Ting-Chi Wang,                   | Woei-Haur Hong, Hsu Chi, Tung-Yeh Wu, Yung-Hsuan Fu, Chia-en Lu, Hao-Wei Chen   |

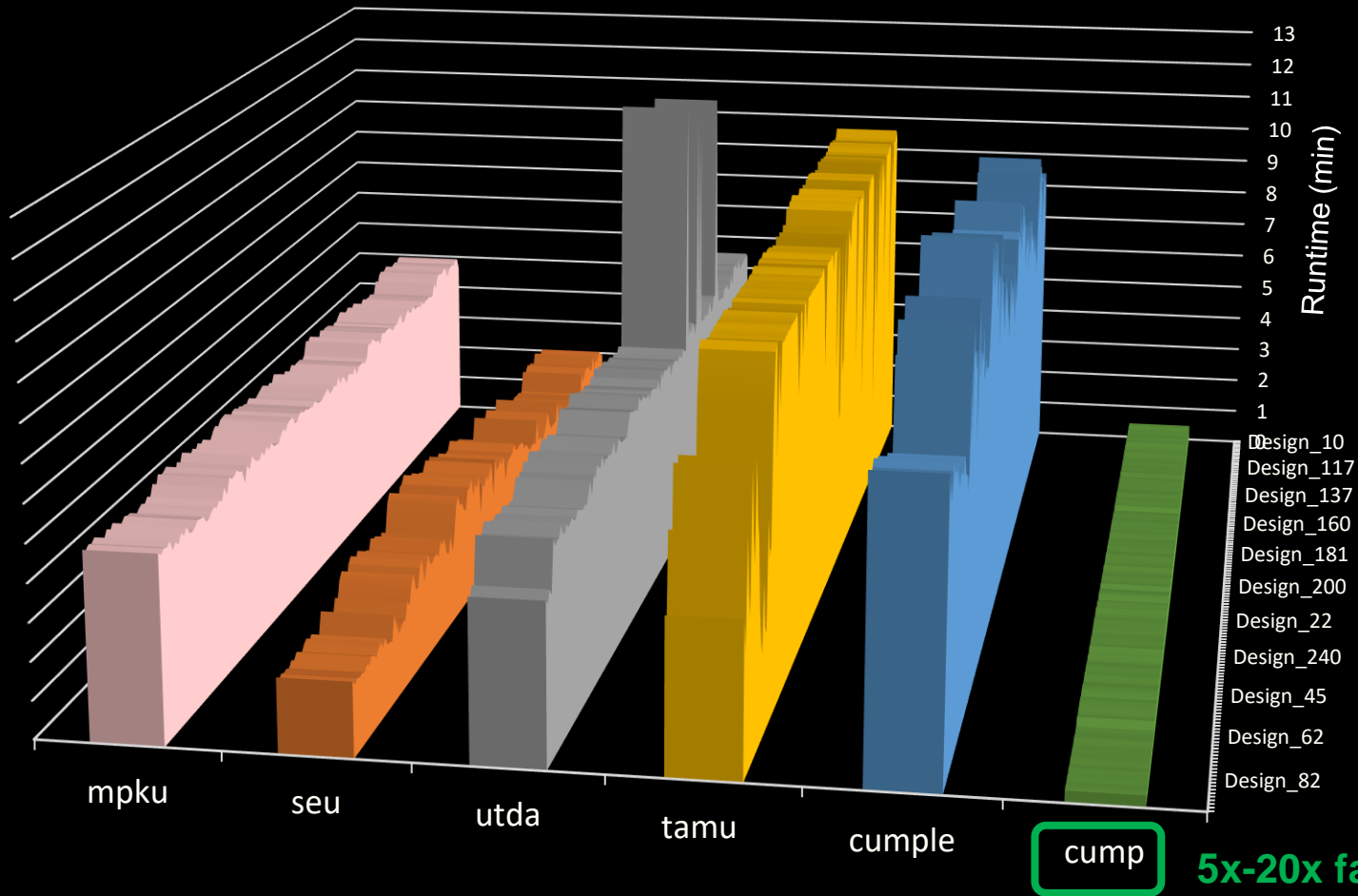
# 8 Finalists

| Team   | University                    | Professor                        | Members   |
|--------|-------------------------------|----------------------------------|---|
| TAMU   | Texas A & M                   | Jiang Hu                         | Hailiang Hu, Donghao Fang, Yishuang Lin   |
| MPKU   | Peking University             | Yibo Lin                         | Jing Mai, Jiarui Wang, Xun Jiang, Zizheng Guo, Yifan Chen                       |
| CUMPLE | CUHK                          | Evangeline F.Y. Young            | Qin Luo, Xinshi Zang, Qijing Wang, Fangzhou Wang                                |
| SEU    | Southeast University          | Ziran Zhu, Jun Yang, Jianli Chen | Hao Gu, Jian Gu, Yuxian Yue   |
| UBCP   | UBC                           | Steven Wilton                    | Andrew Gunter, Martin Chua, Nikhil Ghanathe, Elmira Nezamfar, Roozmehr Jalilian |
| UTDA   | UT Austin                     | David Pan                        | Zhili Xiong, Rachel S. Rajarathnam, Zhixing Jiang, Hanqing Zhu                  |
| NTHU   | National Tsing Hua University | Ting-Chi Wang,                   | Woei-Haur Hong, Hsu Chi, Tung-Yeh Wu, Yung-Hsuan Fu, Chia-en Lu, Hao-Wei Chen   |
| CUMP   | CUHK                          | Bei Yu, Tinghuan Chen            | Yuan Pu, Hongduo Liu, Mingjun Li, Lanchen Zou                                   |

**1.5 min Team Video Presentations**

## 5. Updated Results

# Results – Public Benchmark Macro Placement Runtimes



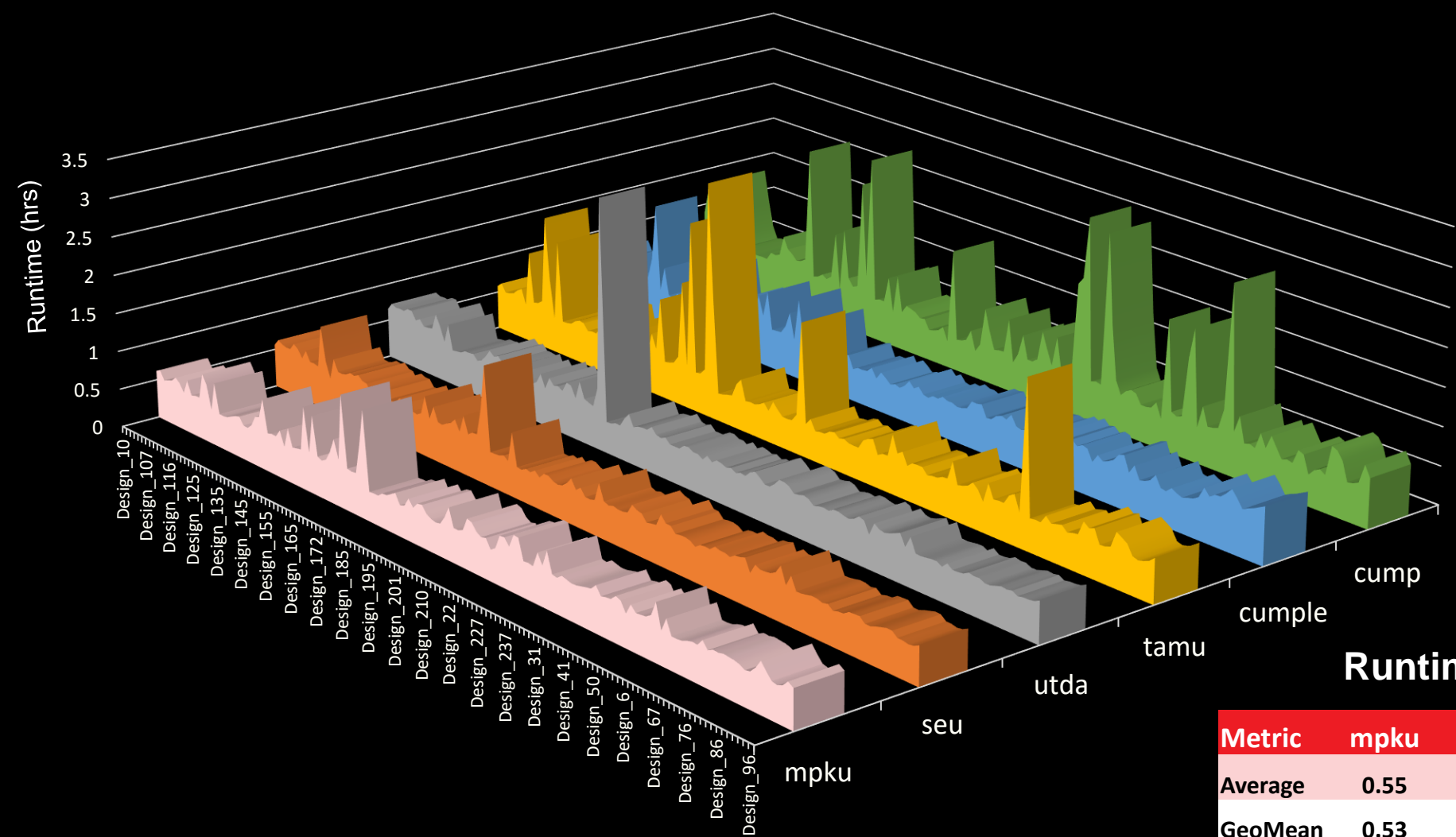
Runtime Summary (min)

| Metric  | mpku | seu  | utda  | tamu | cumple | cump |
|---------|------|------|-------|------|--------|------|
| Average | 4.80 | 2.20 | 5.62  | 7.92 | 8.02   | 0.44 |
| GeoMean | 4.80 | 2.16 | 5.55  | 7.54 | 7.96   | 0.43 |
| Stddev  | 0.15 | 0.43 | 1.07  | 2.09 | 1.02   | 0.06 |
| Max     | 5.08 | 3.30 | 12.29 | 9.66 | 10.87  | 0.58 |

➔ Except for 4 runs, all macro placers ran under 10-min threshold, triggering no runtime penalty



# Results – Public Benchmark Place-and-Route Runtimes

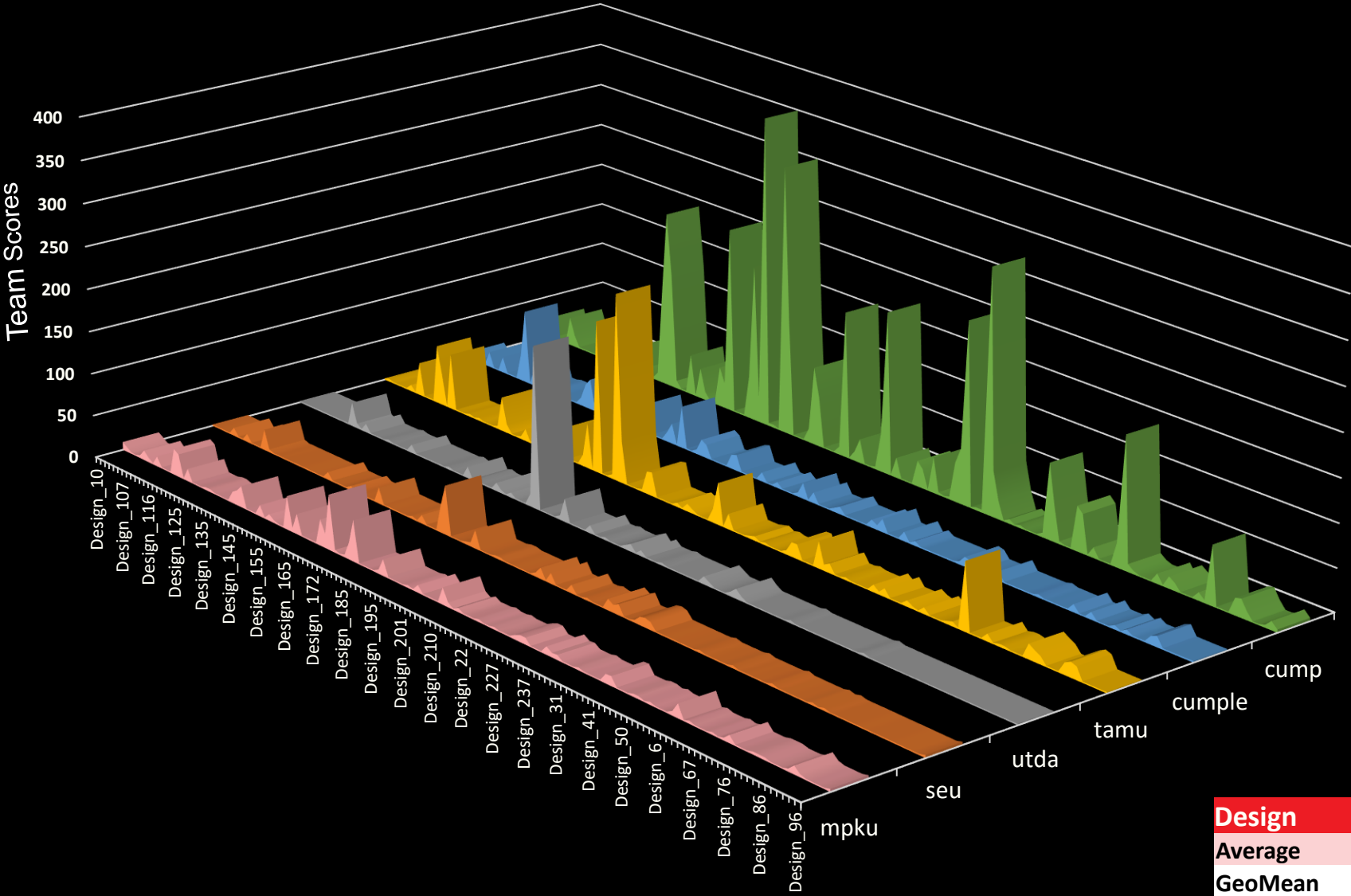


Runtime Summary (hr)

| Metric  | mpku | seu  | utda | tamu | cuple | cump |
|---------|------|------|------|------|-------|------|
| Average | 0.55 | 0.55 | 0.58 | 0.62 | 0.59  | 0.76 |
| GeoMean | 0.53 | 0.54 | 0.56 | 0.56 | 0.58  | 0.68 |
| Stddev  | 0.16 | 0.13 | 0.25 | 0.39 | 0.16  | 0.46 |

➡ mpku and seu had the slowest runtimes overall

# Results - Public Benchmark Team Scores



Score Summary

| Design  | mpku  | seu   | utda   | tamu   | cumple | cump   |
|---------|-------|-------|--------|--------|--------|--------|
| Average | 5.716 | 3.675 | 4.204  | 10.775 | 6.188  | 30.603 |
| GeoMean | 3.023 | 2.233 | 2.120  | 3.593  | 3.029  | 6.650  |
| Stddev  | 9.181 | 6.495 | 16.236 | 26.859 | 10.648 | 63.609 |

# Results - Public Benchmark Team Scores

| Design     | mpku   | seu    | utda    | tamu    | cumple | cump    |
|------------|--------|--------|---------|---------|--------|---------|
| Design_10  | 9.394  | 1.564  | 1.658   | 1.585   | 1.604  | 17.689  |
| Design_100 | 5.608  | 1.650  | 1.749   | 3.617   | 10.007 | 26.253  |
| Design_101 | 1.539  | 1.615  | 1.722   | 1.541   | 1.593  | 3.930   |
| Design_102 | 1.566  | 1.598  | 1.728   | 1.553   | 1.600  | 1.768   |
| Design_105 | 3.495  | 1.602  | 1.723   | 1.578   | 1.620  | 1.821   |
| Design_106 | 11.570 | 9.825  | 1.769   | 1.640   | 18.128 | 34.839  |
| Design_107 | 5.446  | 1.648  | 1.770   | 7.734   | 1.738  | 14.284  |
| Design_11  | 1.501  | 1.550  | 1.663   | 1.487   | 1.528  | 1.696   |
| Design_110 | 11.795 | 9.706  | 1.704   | 39.550  | 18.957 | 1.538   |
| Design_111 | 1.515  | 1.551  | 1.627   | 1.564   | 1.556  | 1.558   |
| Design_112 | 1.534  | 1.553  | 1.633   | 1.580   | 1.601  | 1.548   |
| Design_115 | 1.538  | 1.538  | 1.648   | 1.629   | 1.580  | 1.553   |
| Design_116 | 31.048 | 24.725 | 28.692  | 69.927  | 30.847 | 1.548   |
| Design_117 | 27.036 | 3.640  | 5.877   | 37.491  | 87.442 | 1.548   |
| Design_12  | 1.453  | 1.451  | 1.541   | 1.467   | 1.475  | 1.553   |
| Design_120 | 14.949 | 1.732  | 10.389  | 66.195  | 23.392 | 1.548   |
| Design_121 | 1.447  | 1.590  | 1.469   | 1.465   | 1.439  | 1.658   |
| Design_122 | 1.443  | 1.583  | 1.481   | 1.469   | 1.424  | 1.649   |
| Design_125 | 1.456  | 1.604  | 1.490   | 1.486   | 3.314  | 1.678   |
| Design_126 | 3.280  | 1.646  | 1.532   | 3.390   | 3.258  | 30.048  |
| Design_127 | 3.347  | 1.635  | 3.370   | 1.573   | 1.493  | 3.960   |
| Design_130 | 1.540  | 1.669  | 1.542   | 3.436   | 1.489  | 1.751   |
| Design_131 | 1.451  | 1.615  | 1.475   | 1.478   | 1.438  | 1.682   |
| Design_132 | 1.443  | 1.606  | 1.508   | 1.497   | 1.458  | 1.700   |
| Design_135 | 1.503  | 1.508  | 1.585   | 1.490   | 1.579  | 10.121  |
| Design_136 | 13.441 | 1.623  | 9.773   | 3.517   | 9.629  | 113.445 |
| Design_137 | 17.637 | 9.268  | 1.629   | 40.590  | 28.005 | 209.770 |
| Design_140 | 24.945 | 1.601  | 1.662   | 10.467  | 36.532 | 137.447 |
| Design_141 | 1.500  | 1.516  | 1.598   | 1.499   | 1.556  | 9.415   |
| Design_142 | 1.520  | 1.524  | 1.596   | 1.464   | 1.545  | 1.583   |
| Design_145 | 1.515  | 1.545  | 1.584   | 3.345   | 1.578  | 1.639   |
| Design_147 | 13.240 | 5.487  | 1.623   | 14.402  | 5.543  | 48.356  |
| Design_15  | 1.431  | 1.487  | 1.475   | 1.438   | 1.595  | 1.522   |
| Design_150 | 7.796  | 1.607  | 3.516   | 10.111  | 18.998 | 36.329  |
| Design_151 | 3.241  | 1.516  | 1.506   | 1.467   | 1.637  | 9.914   |
| Design_152 | 1.488  | 1.501  | 1.486   | 1.491   | 1.643  | 1.614   |
| Design_155 | 1.500  | 1.542  | 1.538   | 1.514   | 1.669  | 3.630   |
| Design_156 | 39.373 | 18.954 | 13.666  | 6.133   | 20.357 | 47.375  |
| Design_16  | 5.151  | 1.526  | 1.502   | 21.065  | 3.685  | 30.389  |
| Design_160 | 23.751 | 1.702  | 3.658   | 35.544  | 35.890 | 218.866 |
| Design_161 | 1.513  | 1.526  | 1.588   | 1.494   | 1.528  | 1.549   |
| Design_162 | 1.487  | 1.518  | 1.605   | 1.508   | 1.536  | 1.575   |
| Design_165 | 1.528  | 1.561  | 1.568   | 1.535   | 1.540  | 1.572   |
| Design_166 | 1.653  | 1.597  | 9.866   | 13.407  | 11.496 | 50.339  |
| Design_167 | 30.550 | 3.662  | 3.711   | 53.425  | 24.083 | 186.057 |
| Design_17  | 17.038 | 1.532  | 1.550   | 1.566   | 1.514  | 30.589  |
| Design_170 | 64.344 | 10.218 | 6.082   | 178.838 | 49.504 | 365.959 |
| Design_171 | 3.397  | 1.551  | 1.589   | 1.522   | 1.571  | 3.581   |
| Design_172 | 1.532  | 1.597  | 1.563   | 1.534   | 1.574  | 3.539   |
| Design_175 | 3.393  | 1.601  | 1.544   | 5.484   | 5.485  | 1.583   |
| Design_176 | 20.363 | 32.281 | 14.753  | 219.919 | 19.620 | 316.935 |
| Design_180 | 48.282 | 57.293 | 189.305 | 48.936  | 15.721 | 134.550 |
| Design_181 | 1.382  | 1.450  | 1.409   | 1.365   | 1.408  | 1.413   |
| Design_182 | 1.389  | 1.452  | 1.416   | 1.377   | 1.437  | 1.431   |

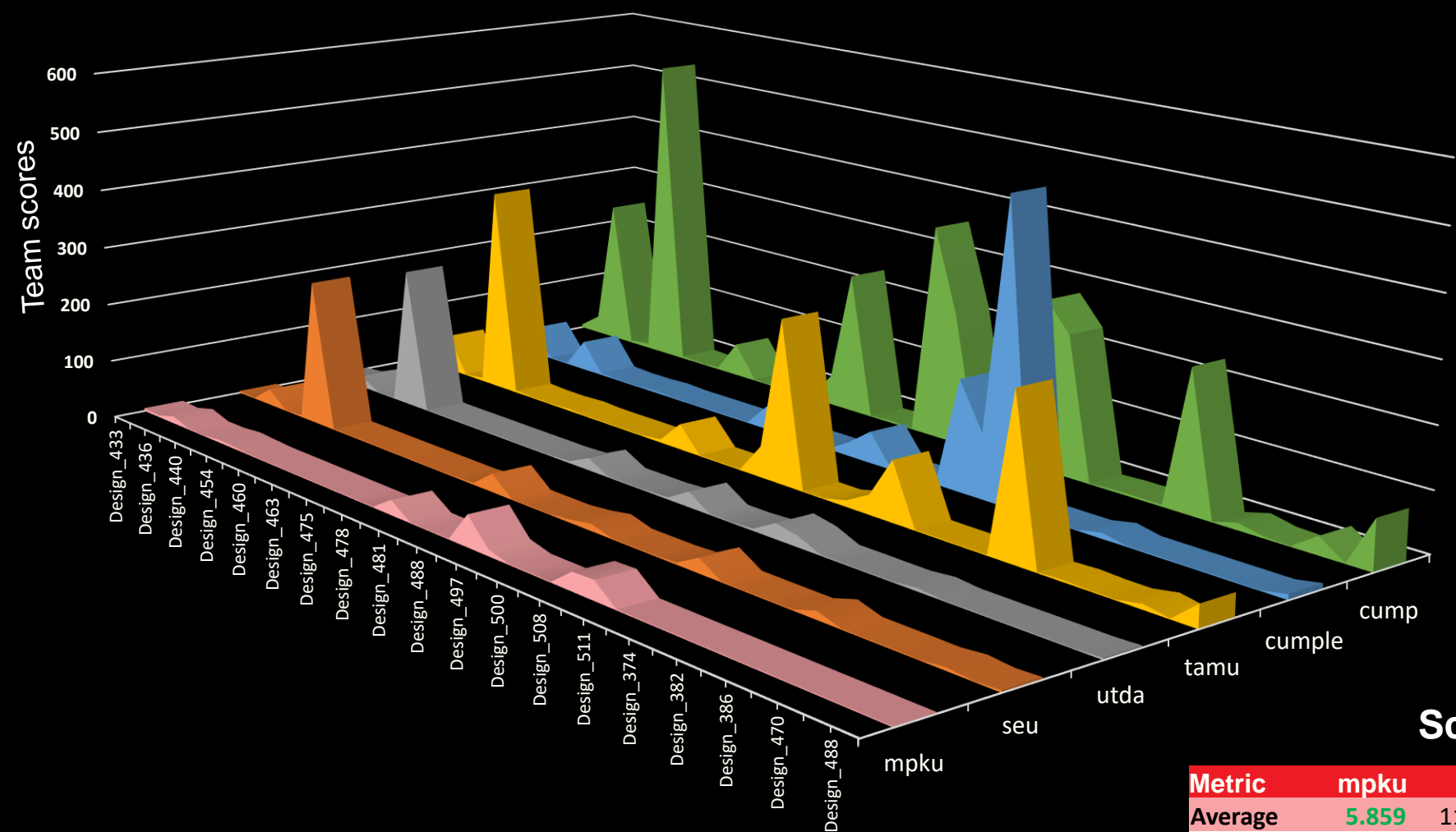
| Design     | mpku   | seu    | utda   | tamu   | cumple | cump    |
|------------|--------|--------|--------|--------|--------|---------|
| Design_185 | 1.389  | 1.460  | 1.445  | 1.399  | 1.424  | 1.459   |
| Design_186 | 1.442  | 3.268  | 1.440  | 3.113  | 1.462  | 16.139  |
| Design_187 | 4.919  | 4.901  | 5.296  | 26.379 | 16.640 | 92.307  |
| Design_190 | 19.346 | 21.649 | 27.245 | 27.807 | 18.785 | 58.871  |
| Design_191 | 1.531  | 1.414  | 1.496  | 1.415  | 1.429  | 1.423   |
| Design_192 | 1.401  | 1.407  | 1.529  | 1.427  | 1.469  | 1.438   |
| Design_195 | 1.424  | 1.445  | 1.539  | 1.423  | 1.467  | 1.469   |
| Design_196 | 1.540  | 3.142  | 1.540  | 1.450  | 1.479  | 9.382   |
| Design_197 | 3.195  | 3.246  | 9.290  | 5.086  | 10.811 | 171.911 |
| Design_2   | 1.531  | 1.414  | 1.526  | 1.414  | 1.427  | 1.478   |
| Design_20  | 8.942  | 1.486  | 1.511  | 9.026  | 1.531  | 11.499  |
| Design_200 | 1.455  | 1.488  | 3.392  | 5.021  | 6.816  | 28.298  |
| Design_201 | 1.419  | 1.446  | 1.478  | 1.412  | 1.419  | 1.479   |
| Design_202 | 1.404  | 1.428  | 1.478  | 1.409  | 1.449  | 1.496   |
| Design_205 | 1.418  | 1.447  | 1.478  | 1.418  | 1.425  | 3.301   |
| Design_206 | 19.798 | 5.108  | 5.235  | 16.034 | 5.024  | 44.299  |
| Design_207 | 5.687  | 13.018 | 8.971  | 48.760 | 18.461 | 190.535 |
| Design_21  | 1.444  | 1.470  | 1.511  | 1.445  | 1.493  | 1.542   |
| Design_210 | 4.911  | 12.485 | 6.948  | 18.082 | 12.619 | 23.673  |
| Design_211 | 1.475  | 1.433  | 1.469  | 1.402  | 1.458  | 1.517   |
| Design_212 | 1.644  | 1.430  | 1.542  | 1.416  | 1.441  | 1.516   |
| Design_215 | 1.623  | 1.451  | 1.485  | 1.421  | 1.491  | 1.569   |
| Design_216 | 3.378  | 9.815  | 3.375  | 3.242  | 5.041  | 30.289  |
| Design_217 | 1.496  | 1.487  | 1.523  | 5.066  | 8.875  | 22.787  |
| Design_22  | 1.515  | 1.462  | 1.496  | 1.436  | 1.501  | 1.560   |
| Design_220 | 3.078  | 3.263  | 1.518  | 3.205  | 1.502  | 41.852  |
| Design_221 | 1.445  | 1.466  | 1.480  | 1.425  | 1.473  | 3.352   |
| Design_222 | 1.624  | 1.466  | 1.509  | 1.420  | 1.483  | 1.535   |
| Design_225 | 1.634  | 1.485  | 1.495  | 1.420  | 1.507  | 3.396   |
| Design_226 | 5.264  | 13.174 | 1.566  | 5.234  | 9.404  | 45.940  |
| Design_227 | 7.903  | 9.088  | 9.298  | 16.802 | 5.495  | 64.747  |
| Design_230 | 7.877  | 12.727 | 5.290  | 17.079 | 15.354 | 215.774 |
| Design_231 | 1.453  | 1.467  | 1.496  | 1.431  | 1.482  | 1.546   |
| Design_232 | 1.460  | 1.482  | 1.494  | 1.472  | 1.492  | 3.449   |
| Design_235 | 1.448  | 3.286  | 1.550  | 1.472  | 1.557  | 3.409   |
| Design_236 | 9.536  | 9.574  | 5.551  | 31.543 | 11.099 | 286.189 |
| Design_237 | 5.146  | 10.966 | 11.415 | 7.151  | 1.564  | 54.023  |
| Design_240 | 5.856  | 9.061  | 5.458  | 11.210 | 5.610  | 21.923  |
| Design_25  | 1.463  | 1.491  | 1.540  | 1.448  | 1.526  | 1.513   |
| Design_26  | 1.448  | 1.503  | 1.550  | 1.505  | 1.504  | 5.403   |
| Design_27  | 1.502  | 1.505  | 1.571  | 3.326  | 1.532  | 1.631   |
| Design_30  | 3.265  | 1.489  | 1.550  | 1.511  | 1.589  | 3.540   |
| Design_31  | 1.467  | 1.444  | 1.493  | 1.433  | 1.602  | 1.486   |
| Design_32  | 1.471  | 1.493  | 1.515  | 1.451  | 1.586  | 1.483   |
| Design_35  | 1.488  | 1.502  | 1.527  | 1.456  | 1.610  | 1.500   |
| Design_36  | 1.506  | 1.498  | 1.513  | 8.649  | 3.656  | 5.410   |
| Design_37  | 10.629 | 3.424  | 3.421  | 3.298  | 11.368 | 88.915  |
| Design_40  | 11.124 | 1.537  | 1.554  | 10.097 | 9.778  | 42.005  |
| Design_41  | 1.484  | 1.538  | 1.534  | 1.469  | 1.618  | 3.397   |
| Design_42  | 1.502  | 1.514  | 1.522  | 1.486  | 1.638  | 1.510   |
| Design_45  | 1.510  | 1.561  | 1.551  | 1.516  | 1.577  | 1.537   |
| Design_46  | 3.463  | 1.568  | 1.608  | 7.269  | 3.561  | 52.329  |
| Design_47  | 3.402  | 3.502  | 1.584  | 3.336  | 11.190 | 45.233  |
| Design_5   | 1.421  | 1.433  | 1.438  | 1.393  | 1.454  | 1.475   |

| Design    | mpku   | seu   | utda  | tamu   | cumple | cump    |
|-----------|--------|-------|-------|--------|--------|---------|
| Design_50 | 3.431  | 1.560 | 1.604 | 7.603  | 1.568  | 12.371  |
| Design_51 | 1.487  | 1.528 | 1.553 | 1.476  | 1.514  | 1.528   |
| Design_52 | 1.493  | 1.533 | 1.542 | 1.486  | 1.542  | 1.539   |
| Design_55 | 1.505  | 1.544 | 1.563 | 1.485  | 1.586  | 1.563   |
| Design_56 | 5.269  | 1.585 | 1.593 | 3.535  | 1.678  | 28.156  |
| Design_57 | 16.295 | 3.722 | 3.573 | 5.615  | 3.742  | 153.625 |
| Design_6  | 1.426  | 1.484 | 1.479 | 1.453  | 1.504  | 9.260   |
| Design_60 | 3.511  | 1.627 | 1.629 | 78.819 | 1.621  | 4.000   |
| Design_61 | 1.414  | 1.465 | 1.454 | 1.428  | 1.458  | 1.491   |
| Design_62 | 1.413  | 1.469 | 1.449 | 1.439  | 1.475  | 1.513   |
| Design_65 | 1.422  | 1.482 | 1.459 | 1.433  | 1.512  | 1.486   |
| Design_66 | 3.195  | 1.498 | 1.470 | 8.946  | 9.309  | 11.919  |
| Design_67 | 1.470  | 3.284 | 1.472 | 1.472  | 1.468  | 1.537   |
| Design_7  | 3.221  | 1.472 | 1.434 | 3.286  | 1.454  | 14.108  |
| Design_70 | 8.981  | 3.276 | 1.501 | 3.324  | 8.808  | 9.246   |
| Design_71 | 1.459  | 1.436 | 1.450 | 1.445  | 1.481  | 1.471   |
| Design_72 | 1.496  | 1.456 | 1.452 | 1.466  | 1.453  | 1.495   |
| Design_75 | 1.490  | 1.461 | 1.464 | 1.479  | 1.477  | 1.476   |
| Design_76 | 3.316  | 1.509 | 1.504 | 17.641 | 5.082  | 9.674   |
| Design_77 | 3.297  | 1.514 | 1.488 | 13.185 | 1.539  | 3.598   |
| Design_80 | 3.283  | 1.518 | 1.492 | 9.492  | 5.731  | 68.922  |
| Design_81 | 1.474  | 1.456 | 1.459 | 1.460  | 1.601  | 1.490   |
| Design_82 | 1.437  | 1.455 | 1.461 | 1.467  | 1.650  | 1.528   |
| Design_85 | 1.452  | 1.483 | 1.486 | 1.493  | 1.655  | 1.483   |
| Design_86 | 3.355  | 1.503 | 1.508 | 13.942 | 9.981  | 19.908  |
| Design_87 | 9.489  | 1.524 | 1.499 | 17.587 | 12.621 | 21.771  |
| Design_90 | 3.395  | 1.522 | 1.514 | 15.148 | 1.714  | 10.100  |
| Design_91 | 1.461  | 1.466 | 1.476 | 1.486  | 1.605  | 1.495   |
| Design_92 | 1.445  | 1.465 | 1.490 | 1.464  | 1.644  | 1.509   |
| Design_95 | 1.473  | 1.449 | 1.492 | 1.483  | 1.673  | 3.400   |
| Design_96 | 1.548  | 1.461 | 1.504 | 1.515  | 1.712  | 10.426  |
| Design_97 | 3.305  | 3.295 | 1.539 | 1.578  | 1.751  | 3.638   |

## Score Summary

| Metric  | mpku  | seu   | utda   | tamu   | cumple | cump   |
|---------|-------|-------|--------|--------|--------|--------|
| Average | 5.716 | 3.675 | 4.204  | 10.775 | 6.188  | 30.603 |
| GeoMean | 3.023 | 2.233 | 2.120  | 3.593  | 3.029  | 6.650  |
| Stddev  | 9.181 | 6.495 | 16.236 | 26.859 | 10.648 | c      |

# Results – Hidden\* Benchmark Team Scores



Score Summary

| Metric  | mpku   | seu    | utda   | tamu   | cumple | cump    |
|---------|--------|--------|--------|--------|--------|---------|
| Average | 5.859  | 11.100 | 10.933 | 34.448 | 15.380 | 71.529  |
| GeoMean | 2.566  | 2.846  | 2.933  | 5.373  | 3.585  | 10.633  |
| Stddev  | 11.028 | 40.166 | 38.691 | 82.058 | 35.956 | 128.078 |

\* Ran on a representative set of 38 designs from the 198 hidden benchmark suite because of runtime constraints

# Results – Hidden\* Benchmark Team Scores

| Design     | mpku   | seu     | utda    | tamu    | cumple  | cump    |
|------------|--------|---------|---------|---------|---------|---------|
| Design_433 | 5.085  | 3.361   | 1.542   | 5.345   | 1.615   | 5.567   |
| Design_434 | 3.301  | 1.529   | 5.294   | 3.403   | 3.500   | 30.824  |
| Design_436 | 12.209 | 27.974  | 19.707  | 63.946  | 48.640  | 253.753 |
| Design_439 | 1.502  | 1.538   | 1.557   | 1.541   | 1.594   | 3.518   |
| Design_440 | 1.516  | 3.389   | 1.564   | 5.291   | 1.638   | 7.479   |
| Design_443 | 5.085  | 248.059 | 239.319 | 353.023 | 51.947  | 538.871 |
| Design_454 | 3.176  | 1.453   | 1.475   | 3.366   | 3.304   | 3.733   |
| Design_457 | 1.435  | 1.453   | 1.452   | 1.478   | 1.468   | 1.672   |
| Design_460 | 1.485  | 1.510   | 1.468   | 1.531   | 1.514   | 3.735   |
| Design_461 | 1.467  | 1.480   | 1.472   | 3.456   | 3.406   | 57.339  |
| Design_463 | 1.426  | 1.464   | 1.446   | 1.500   | 1.491   | 1.652   |
| Design_464 | 1.448  | 1.478   | 1.562   | 1.627   | 1.522   | 1.625   |
| Design_475 | 1.435  | 1.499   | 1.613   | 1.686   | 1.627   | 1.653   |
| Design_476 | 1.461  | 1.491   | 1.623   | 1.643   | 1.581   | 3.670   |
| Design_478 | 1.534  | 3.476   | 3.678   | 5.857   | 1.635   | 51.462  |
| Design_479 | 25.288 | 30.976  | 20.894  | 43.490  | 41.510  | 240.531 |
| Design_481 | 1.447  | 1.406   | 1.638   | 1.565   | 1.464   | 1.472   |
| Design_487 | 1.449  | 1.461   | 1.675   | 1.558   | 1.451   | 3.270   |
| Design_488 | 1.453  | 1.473   | 1.682   | 1.588   | 1.495   | 1.502   |
| Design_496 | 52.887 | 5.387   | 3.895   | 51.999  | 23.693  | 361.085 |
| Design_497 | 11.271 | 11.983  | 25.720  | 273.807 | 53.318  | 221.208 |
| Design_499 | 1.534  | 1.518   | 1.720   | 1.600   | 1.510   | 1.511   |
| Design_500 | 1.500  | 1.492   | 1.652   | 1.523   | 1.570   | 1.550   |
| Design_502 | 1.605  | 1.567   | 3.771   | 11.316  | 3.480   | 12.852  |
| Design_508 | 30.575 | 3.651   | 25.726  | 33.004  | 185.635 | 285.071 |
| Design_509 | 31.965 | 24.487  | 18.266  | 101.007 | 109.031 | 237.315 |
| Design_511 | 1.558  | 1.546   | 1.740   | 1.559   | 1.47    | 1.603   |
| Design_512 | 1.528  | 1.501   | 1.759   | 1.546   | 1.703   | 3.461   |
| Design_374 | 1.472  | 1.453   | 1.469   | 1.485   | 1.452   | 3.495   |
| Design_380 | 1.452  | 1.480   | 1.484   | 1.472   | 1.473   | 3.347   |
| Design_382 | 1.605  | 13.585  | 5.425   | 269.895 | 9.737   | 237.461 |
| Design_385 | 1.508  | 1.525   | 1.501   | 1.528   | 1.493   | 1.567   |
| Design_386 | 1.512  | 1.528   | 1.517   | 3.348   | 1.496   | 12.305  |
| Design_458 | 1.435  | 1.434   | 1.429   | 1.424   | 1.433   | 3.252   |
| Design_470 | 1.470  | 1.108   | 1.469   | 1.467   | 1.445   | 1.474   |
| Design_473 | 1.532  | 5.207   | 1.528   | 9.002   | 1.509   | 30.603  |
| Design_488 | 1.481  | 1.448   | 1.445   | 1.411   | 1.412   | 1.434   |
| Design_491 | 1.537  | 3.424   | 3.257   | 37.727  | 9.193   | 84.162  |

## Score Summary

| Metric  | mpku   | seu    | utda   | tamu   | cumple | cump    |
|---------|--------|--------|--------|--------|--------|---------|
| Average | 5.859  | 11.100 | 10.933 | 34.448 | 15.380 | 71.529  |
| GeoMean | 2.566  | 2.846  | 2.933  | 5.373  | 3.585  | 10.633  |
| Stddev  | 11.028 | 40.166 | 38.691 | 82.058 | 35.956 | 128.078 |

# Final Rankings

- For each team,
  - Combined 140 public + 38 hidden scores to have equal contributions to final score
    - $w_{\text{public}} = 1$
    - $w_{\text{hidden}} = 140/38$
  - **Final Score** = weighted geometric mean ( $w_{\text{public}}, w_{\text{hidden}}$ )

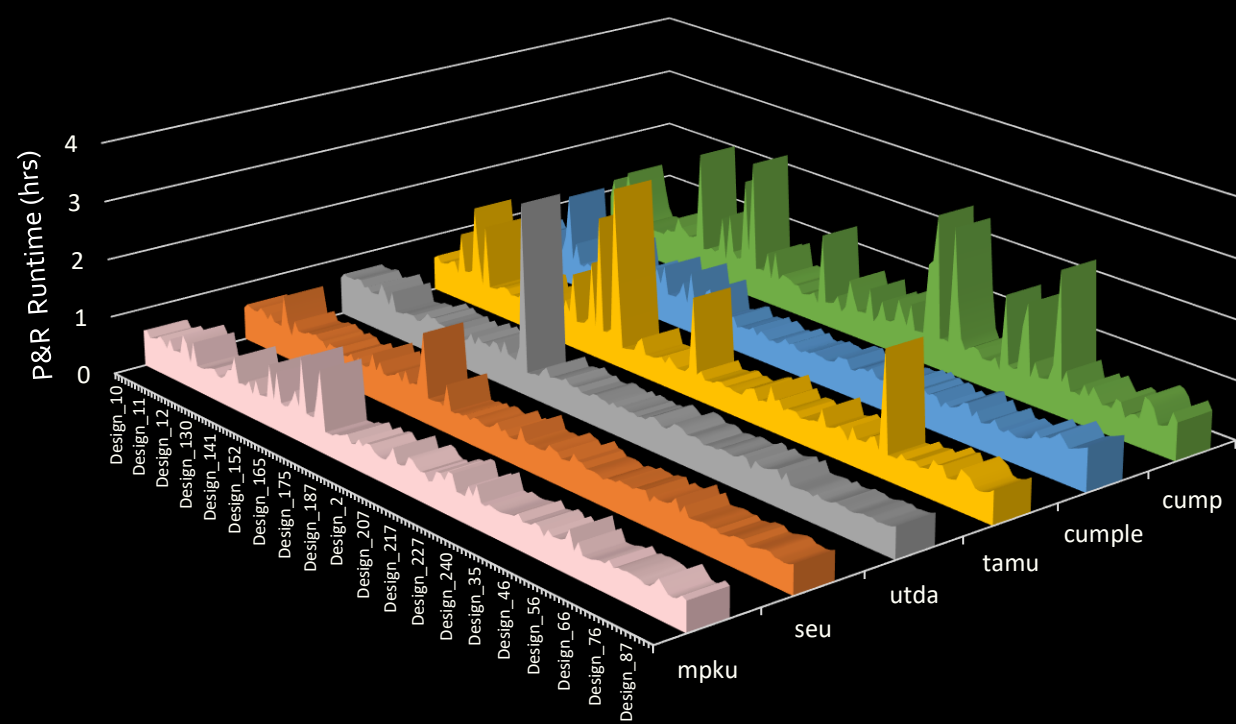
$$\bar{x} = \left( \prod_{i=1}^n x_i^{w_i} \right)^{1/\sum_{i=1}^n w_i} = \exp\left( \frac{\sum_{i=1}^n w_i \ln x_i}{\sum_{i=1}^n w_i} \right)$$

## ➤ Final Team Scores:

| Team   | Weighted GeoMean | Rank |
|--------|------------------|------|
| utda   | 2.513            | 1*   |
| seu    | 2.516            | 1*   |
| mpku   | 2.751            | 2    |
| cumple | 3.605            | 3    |
| Tamu   | 4.399            | 4    |
| cump   | 8.433            | 5    |

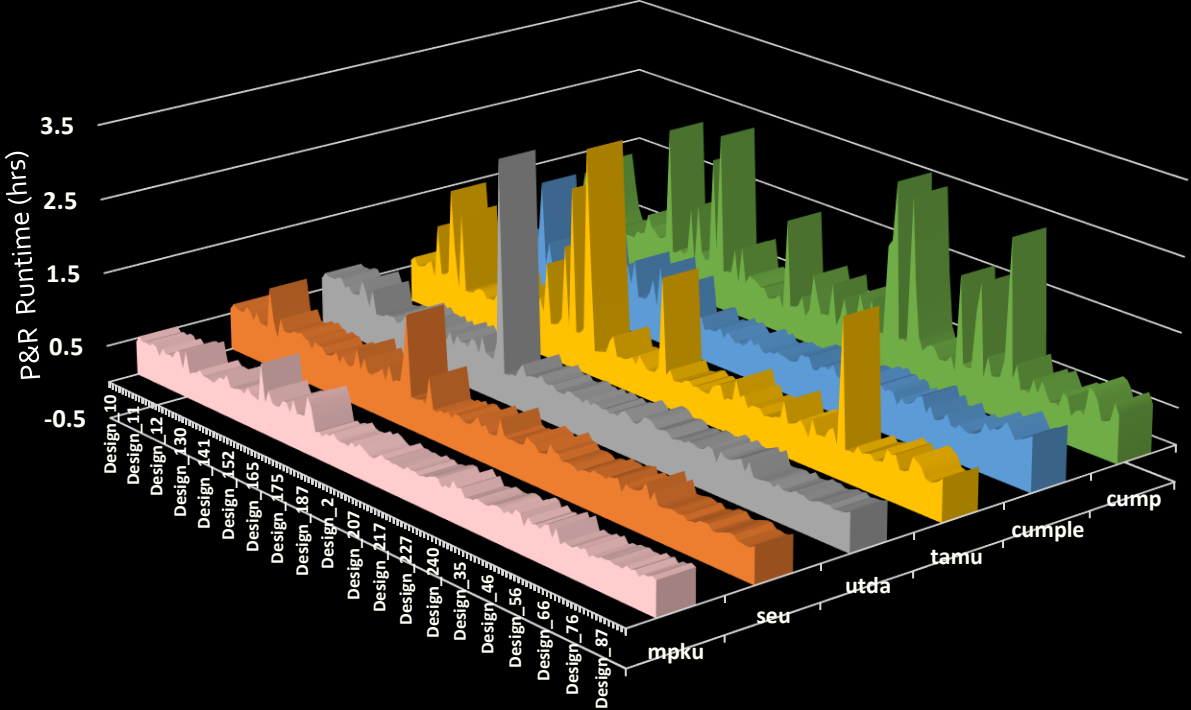
## **5. Results with Updated Team MPKU Exec**

# Results\* - Public Benchmark Place-and-Route Runtimes with Updated MPKU exec



Runtime Summary

| Metric  | mpku | seu  | utda | tamu | cumple | cump |
|---------|------|------|------|------|--------|------|
| Average | 0.55 | 0.55 | 0.58 | 0.62 | 0.59   | 0.76 |
| GeoMean | 0.53 | 0.54 | 0.56 | 0.56 | 0.58   | 0.68 |
| Stddev  | 0.16 | 0.13 | 0.25 | 0.39 | 0.16   | 0.46 |



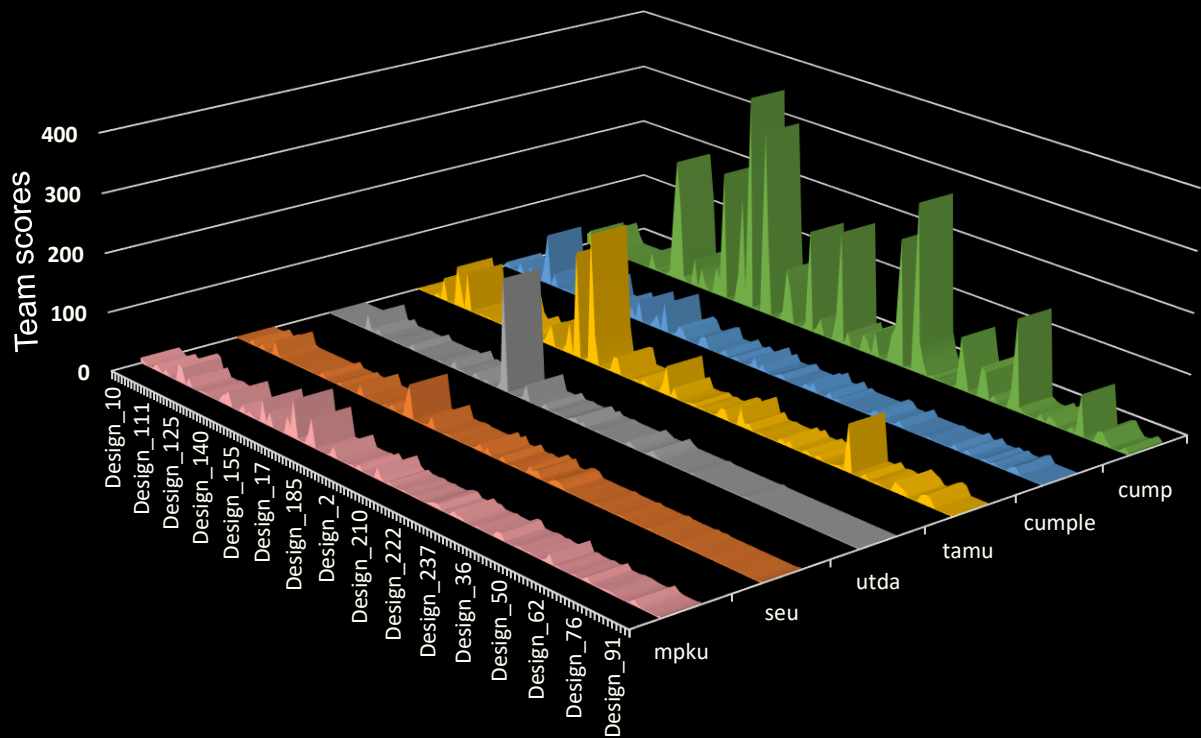
Runtime Summary

| Metric  | mpku | seu  | utda | tamu | cumple | cump |
|---------|------|------|------|------|--------|------|
| Average | 0.46 | 0.55 | 0.58 | 0.62 | 0.59   | 0.76 |
| GeoMean | 0.45 | 0.54 | 0.56 | 0.56 | 0.58   | 0.68 |
| Stddev  | 0.08 | 0.13 | 0.25 | 0.39 | 0.16   | 0.46 |
| Max     | 0.94 | 1.54 | 3.28 | 3.09 | 1.62   | 2.68 |

\*Contest organizers requested Team MPKU to submit an executable post the contest deadline related to fixing some errors observed in a subset of hidden benchmark designs during the evaluation process.

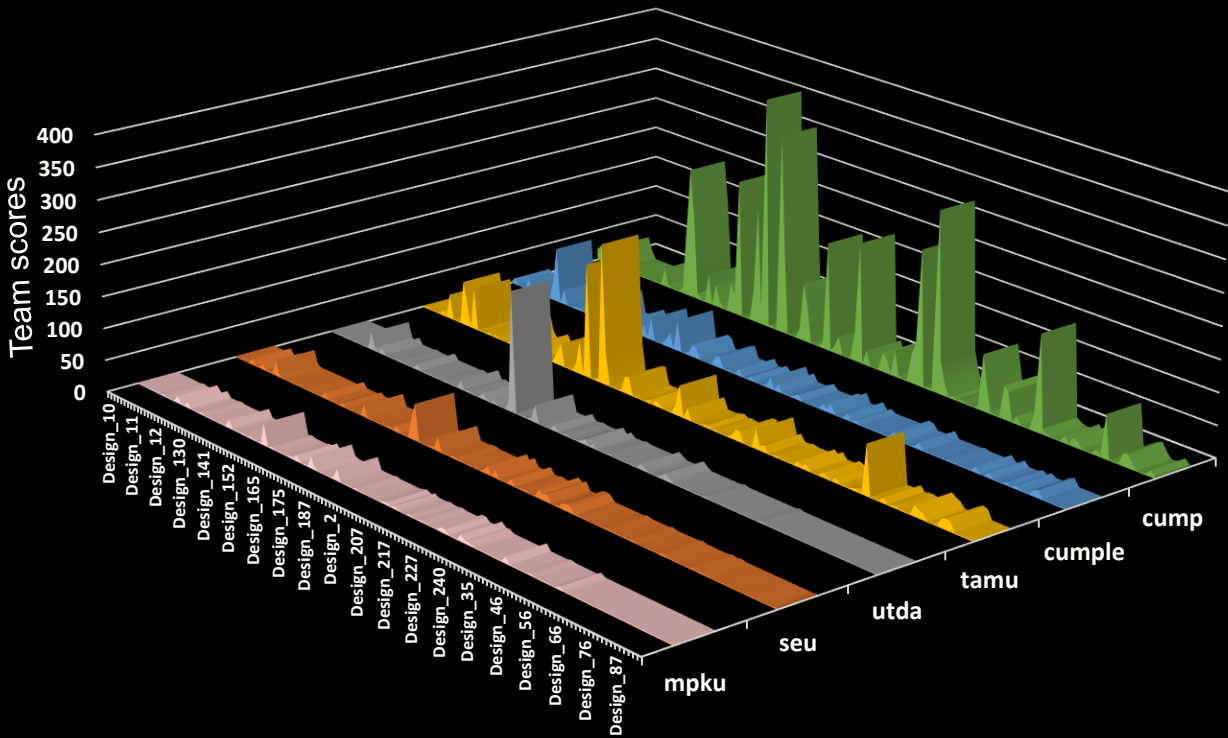


# Results\* - Public Benchmark Team Scores with Updated MPKU exec



Score Summary

| Design  | mpku  | seu   | utda   | tamu   | cumple | cump   |
|---------|-------|-------|--------|--------|--------|--------|
| Average | 5.716 | 3.675 | 4.204  | 10.775 | 6.188  | 30.603 |
| GeoMean | 3.023 | 2.233 | 2.120  | 3.593  | 3.029  | 6.650  |
| Stddev  | 9.181 | 6.495 | 16.236 | 26.859 | 10.648 | 63.609 |

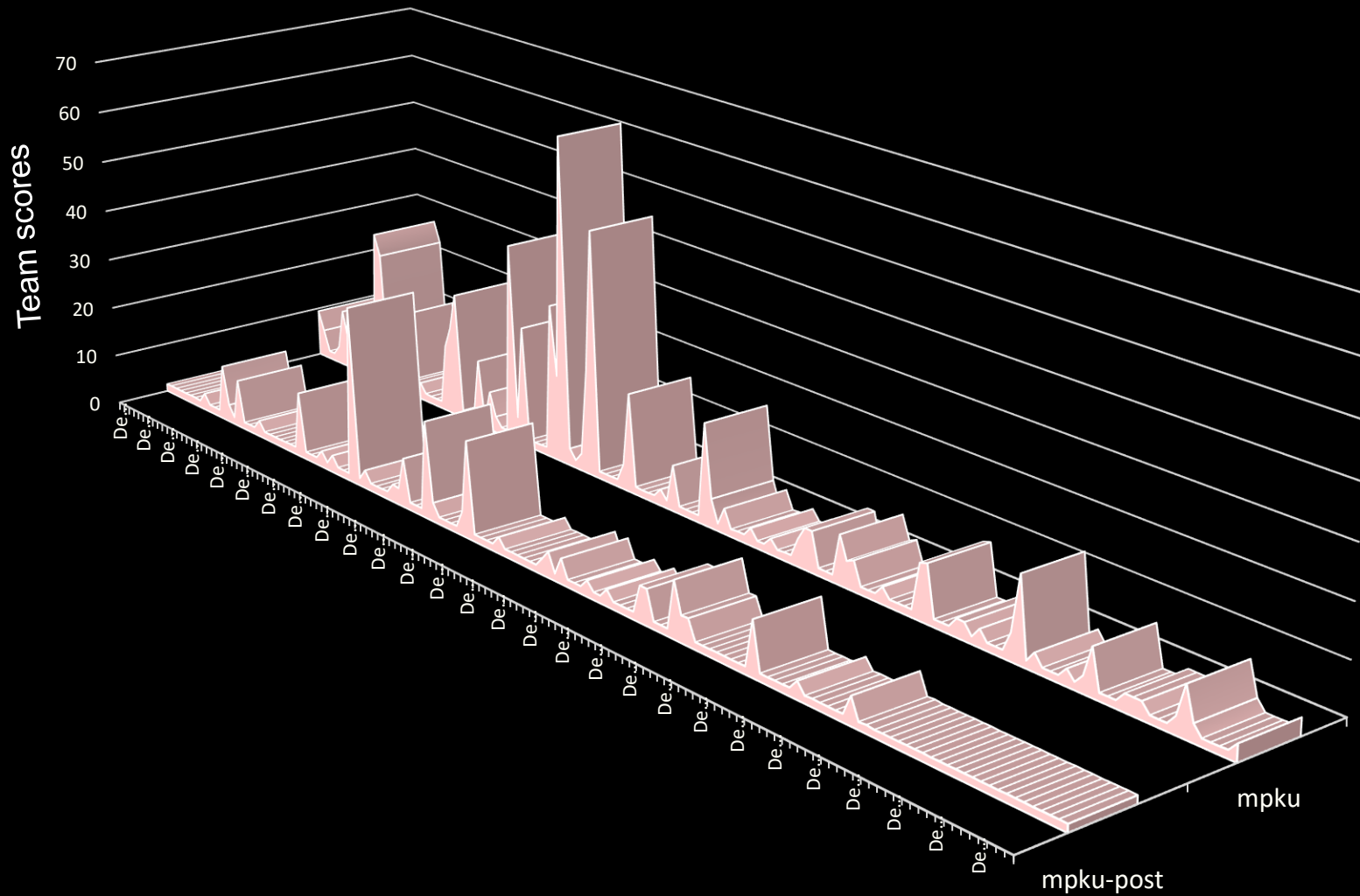


Score Summary

| Metric  | mpku  | seu   | utda   | tamu   | cumple | cump   |
|---------|-------|-------|--------|--------|--------|--------|
| Average | 2.738 | 3.675 | 4.204  | 10.775 | 6.188  | 30.603 |
| GeoMean | 1.950 | 2.233 | 2.120  | 3.593  | 3.029  | 6.650  |
| Stddev  | 3.952 | 6.495 | 16.236 | 26.859 | 10.648 | 63.609 |

\*Contest organizers requested Team MPKU to submit an executable post the contest deadline related to fixing some errors observed in a subset of hidden benchmark designs during the evaluation process.

# Public Benchmark – Team MPKU Original vs. Updated Scores



| Metric  | mpku-post-deadline | mpku  |
|---------|--------------------|-------|
| Average | 2.738              | 5.716 |
| GeoMean | 1.950              | 3.023 |
| Stddev  | 3.952              | 9.181 |

# Final Rankings with Updated MPKU exec

- For each team,
  - Combined 140 public + 38 hidden scores to have equal contributions to final score
    - $w_{\text{public}} = 1$
    - $w_{\text{hidden}} = 140/38$
  - **Final Score** = weighted geometric mean ( $w_{\text{public}}, w_{\text{hidden}}$ )

$$\bar{x} = \left( \prod_{i=1}^n x_i^{w_i} \right)^{1/\sum_{i=1}^n w_i} = \exp\left( \frac{\sum_{i=1}^n w_i \ln x_i}{\sum_{i=1}^n w_i} \right)$$

## ➤ Final Team Scores:

| Team   | Weighted GeoMean | Rank |
|--------|------------------|------|
| utda   | 2.513            | 1*   |
| seu    | 2.516            | 1*   |
| mpku   | 2.751            | 2    |
| cumple | 3.605            | 3    |
| Tamu   | 4.399            | 4    |
| cump   | 8.433            | 5    |



Updated Exec Score

2.216



# Contest Lowlights

1. Various bugs in the benchmark suite
2. A bug in the provided place-and-route flow script
3. Place-and-route tool Licensing enablement was not efficient

} → *Flying while building the plane!*

# Contest Highlights

1. 7 team finalists despite all obstacles!
2. 5 submitted competitive solutions!
3. Many contestants gained practical experience in packaging their SW solutions with containers
4. Engaging, excellent feedback and bug reporting from contestants
  - A special ***thank you shout-out*** to teams MPKU, CUMPLE, and CUMP for identifying various bugs and providing candidate solutions.
5. A battle-vetted public benchmark suite with 338 FPGA designs

# Parting Thoughts

- We wish to thank all contestants for their active participation, patience, and diligence.
- No team has fully deployed ML-based methods, with **new classical optimization** still showing promising results
- Hoping to see progress in scalable ML methods in future solutions (MLCAD 2024?)
- Refine and iterate over your solutions till the next contest opportunity!

## **7. Awards Ceremony!**





# 2023 ACM/IEEE Workshop on Machine Learning for CAD

## FPGA Macro Placement Contest

# Fifth Place

## Chinese University of Hong Kong

### CUMP-Placer

**Yuan Pu, Lancheng Zhou, Mingjun Li, Yuhao Ji, Tinghuan Chen, & Bei Yu**

**Andrew Kahng & Husam Amrouch**  
General Chairs

**Jiang Hu**  
Program Chair

**Ismail Bustany**  
Contest Chair



# 2023 ACM/IEEE Workshop on Machine Learning for CAD

## FPGA Macro Placement Contest

**Fourth Place**

**Texas A&M University**

**TAMU-Placer**

**Hailiang Hu, Donghao Fang, Yishuang Lin, Jianfeng Song, & Jiang Hu**

A handwritten signature in black ink, appearing to read 'Andrew Kahng'.

**Andrew Kahng & Husam Amrouch**  
General Chairs

A handwritten signature in black ink, appearing to read 'Husam Amrouch'.

A handwritten signature in blue ink, appearing to read 'Jiang Hu'.

**Jiang Hu**  
Program Chair

A handwritten signature in blue ink, appearing to read 'Ismail Bustany'.

**Ismail Bustany**  
Contest Chair



# 2023 ACM/IEEE Workshop on Machine Learning for CAD

## FPGA Macro Placement Contest

# Third Place

## Chinese University of Hong Kong

### CUMPLE-Placer

**Qin Luo, Xinshi Zang, Qijing Wang, Fangzhou Wang, & Evangeline Young**

**Andrew Kahng & Husam Amrouch**  
General Chairs

**Jiang Hu**  
Program Chair

**Ismail Bustany**  
Contest Chair



# 2023 ACM/IEEE Workshop on Machine Learning for CAD

## FPGA Macro Placement Contest

**Second\* Place**

**Peking University**

**MPKU-Placer**

**Jing Mai, Jiarui Wang, Xun Jiang, Yifan Chen, Zizheng Guo, & Yibo Lin**

A handwritten signature in black ink, likely belonging to Andrew Kahng.

**Andrew Kahng & Husam Amrouch**  
General Chairs

A handwritten signature in black ink, likely belonging to Husam Amrouch.

A handwritten signature in blue ink, likely belonging to Jiang Hu.

**Jiang Hu**  
Program Chair

A handwritten signature in blue ink, likely belonging to Ismail Bustany.

**Ismail Bustany**  
Contest Chair



# 2023 ACM/IEEE Workshop on Machine Learning for CAD

## FPGA Macro Placement Contest

**First\* Place**

**University of Texas at Austin**

**UTDA-Placer**

**Zhili Xiong, Rachel S. Rajarathnam, Zhixing Jiang, Hanqing Zhu, & David Pan**

A stylized signature in black ink, likely belonging to Andrew Kahng or Husam Amrouch.

**Andrew Kahng & Husam Amrouch**  
General Chairs

A stylized signature in blue ink, likely belonging to Jiang Hu.

**Jiang Hu**  
Program Chair

A stylized signature in blue ink, likely belonging to Ismail Bustany.

**Ismail Bustany**  
Contest Chair



**2023 ACM/IEEE Workshop on Machine Learning for CAD**



**FPGA Macro Placement Contest**

**First\* Place**

**Southeast University**

**SEU-Placer**

**Hao Gu, Jian Gu, Yuxian Yue, Ziran Zhu, Jun Yang, & Jianli Chen**

A handwritten signature in black ink, appearing to read 'Andrew Kahng'.

**Andrew Kahng & Husam Amrouch**  
General Chairs

A handwritten signature in black ink, appearing to read 'Husam Amrouch'.

A handwritten signature in blue ink, appearing to read 'Jiang Hu'.

**Jiang Hu**  
Program Chair

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**Ismail Bustany**  
Contest Chair

