RTL8305SC vs. RTL8305SB-VD

RTL8305SC & RTL8305SB-VD COMPARISON GUIDE

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USING THIS DOCUMENT

This document is intended for use in RTL8305SC and RTL8305SB-VD product comparison.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2005/07/20	First release.

Comparison Table

Feature	RTL8305SC	RTL8305SB-VD
VCC	3.3V and 1.8V	3.3V and 2.5V
Number of PHY	5	5
Number of MAC	5	5
Process	0.18um	0.25um
Package	128 PQFP	128 PQFP
MAC address table	1K-entry	1K-entry
CAM	16-entry	16-entry
MDC/MDIO IF for configuration	√	√
Dual MII interface	√	√
MAC mode MII interface at Port4 MAC circuit	√	√
PHY mode MII interface at Port4 MAC circuit	√	√
PHY mode SNI interface at Port4 MAC circuit	√	√
MAC lookup table is accessible	√	X
TX Priority Queues	2	2
Port-based VLAN	√	√
IEEE 802.1Q Tag-based VLAN	√	√
VLAN entries	16	5
Port-based Priority	Per-port enable/disable	Global function
IEEE 802.1P Priority	Per-port enable/disable	Global function
IEEE 802.1P High/Low priority distinction Reg.(3bit)	>=: High priority <: Low priority	>=4 : High priority <4 : Low priority
IPv4 DiffServ Priority	Per-port enable/disable	Global function
Forced Mode flow control - MII & 10/100 PHY	√	√
Broadcast Storm Protection - global	√	√
Crossover detection & auto correction	√	√
10/100 Copper (10BT, 100BTx) - all ports	√	√
100BaseFX Fiber - all ports	√	√
Auto Negotiation	√	√
Flow control IEEE 802.3x	√	√
EEPROM I/F	√	√
LED Mode	4 modes strapped from pins, or globally configured from EEPROM, or internal register	4 modes strapped from pins only
Maximum Frame Size	1536/1552	1536/1552
VLAN enable	√	√
Ingress VLAN member set filtering	√	√
Only admit VLAN tagged frames	√	√

Feature	RTL8305SC	RTL8305SB-VD
Supports Leaky VLAN	√	√
Supports ARP VLAN bypass	√	√
Loop detection enable	√	√
ISP MAC address translation	√	√
Local loop-back	√	X
Pass through DID=01-80-c2-00-00-02	√	X
Supports PVID for each port	√	X
VID of Tagged packet does not match PVID filtering	√	X
Insert tag (PVID) to untagged frame	√	X
Replace tagged frame to PVID	√	X
Supports PHY register for Port4 MII interface	√	√
Supports MII Register 2 and 3	√	X

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