RTL8305SB

SINGLE CHIP 5-PORT 10/100MBPS SWITCH CONTROLLER

LAYOUT GUIDE

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference on the Realtek RTL8305SB controller chips. See the Application Notes for detailed development information.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2002/11/12	First release.
1.1	2003/01/06	Added Differential Signal Layout, page 1.
		Changed the resister of the IBREF to 1.96K ohm.

Table of Contents

List of Tables

List of Figures

1. Introduction

This document provides detailed design and layout guidelines to achieve the best performance when implementing a 2-layer board design with the RTL8305SB 5-port 10/100Mbps single chip switch controller.

The RTL8305SB is a Fast Ethernet switch that integrates memory, five MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip. To benefit BOM costs, one external PNP transistor is used to generate a 2.5V power source. Care needs to be taken, however, to prevent signals from cross-talk and interference due to the small package, and most importantly, to support a stable 2.5V power plane, which determines the performance of data recovery and transmit jitter. The fifth port (port 4) supports an external MAC interface, which can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with a routing engine, HomePNA, or VDSL transceiver. The MII interface layout also plays an important part in the system PCB design.

2. Design and Layout Guide

In order to achieve maximum performance using the RTL8305SB, good design practices are required throughout the process. The following are some recommendations for implementing a high performance system.

2.1. General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<100mV).
- Verify that critical components such as the clock source and transformer meet application requirements.
- Keep power and ground noise levels below 100mV.
- Use bulk capacitors (4.7µF-10µF) between the power and ground planes.
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8305SB chip.

2.2. Differential Signal Layout

- Keep differential pairs as close as possible and route both traces as identically as possible.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other. Run orthogonally or separate by a ground plane.
- 50-ohm impedance match resisters and 0.1uF common mode noise filter capacitors should be placed near the RTL8305SB chip.

2.3. Clock Circuit

- If possible, surround the clock by ground trace to minimize high-frequency emissions.
- Place the crystal or oscillator as close to the RTL8305SB as possible.

2.4. 2.5V Power

- Do not connect a bead directly between the collector of the PNP transistor and VDDAL. This will significantly affect the stability of the 2.5V power.
- Use a bulk capacitor (4.7µF-10µF) between the collector of the PNP transistor and the ground plane.
- Do not use one PNP transistor for more than one RTL8305SB chip, even if the rating is enough. Use one transistor for each RTL8305SB chip.

2.5. Power Planes

- Divide the power plane into 2.5V digital, 2.5V analog, and 3.3V analog.
- Use 0.1μF decoupling capacitors and bulk capacitors between each power plane and the ground plane.
- Power line connects from source to the RTL8305SB pin should at least 10 mil width.

2.6. Ground Planes

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.
- Ensure the chassis ground area is voided at some point such that no ground loop exists on the chassis ground area.

3. Transformer Application Circuit

A transformer supporting Autoxover with a 1:1 turn ratio on both transmit and receive paths should be used with the RTL8305SB. There are many venders improving their transformer design to meet this requirement, and several are listed below.

Table 1. Transformer Vendors

Vendor	Quad	Single
Pulse	H1164	H1102
Magnetic 1	ML164	ML102
BothHand	40ST1041AX	TS6121C
Lankom	SQ-H48W	LF-H41S
GTS	FC-578S	FC618SM

A 10/100Base-T UTP application circuit with transformer is shown on the following two figures. The first is a circuit with Quad transformer and the second is with a single transformer.

- Because of the RTL8305SB's special design, the center-tap of the primary side of the transformer ***should not*** be connected to ground with capacitors.
- The center-tap of the secondary side of the transformer ***should*** be connected to chassis ground via a 50-pF capacitor.
- The center-tap of the 50Ω termination-resister ***should*** be connected to ground with a 0.1uF capacitor.
- The IBREF pin ***should*** connect to ground via a 1.96K Ω, 1% resister to bias the differential output voltage.

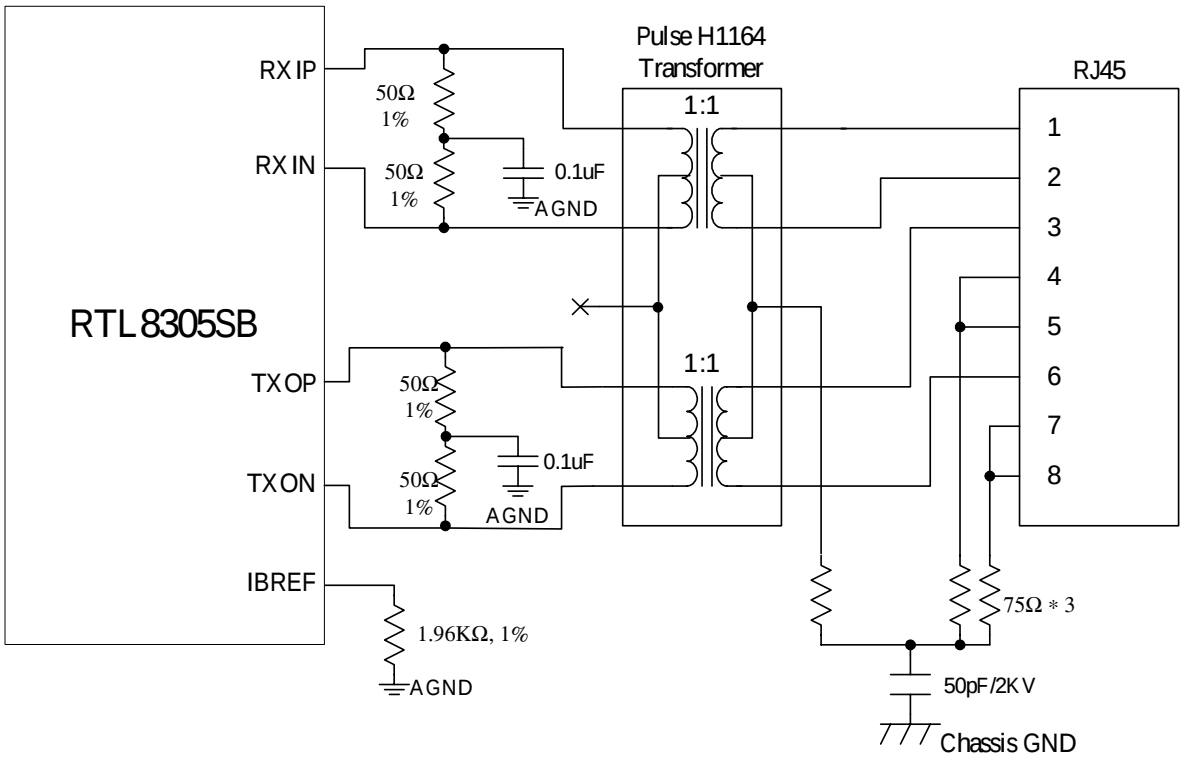


Figure 1. UTP Application for Transformer with Connected Central Tap

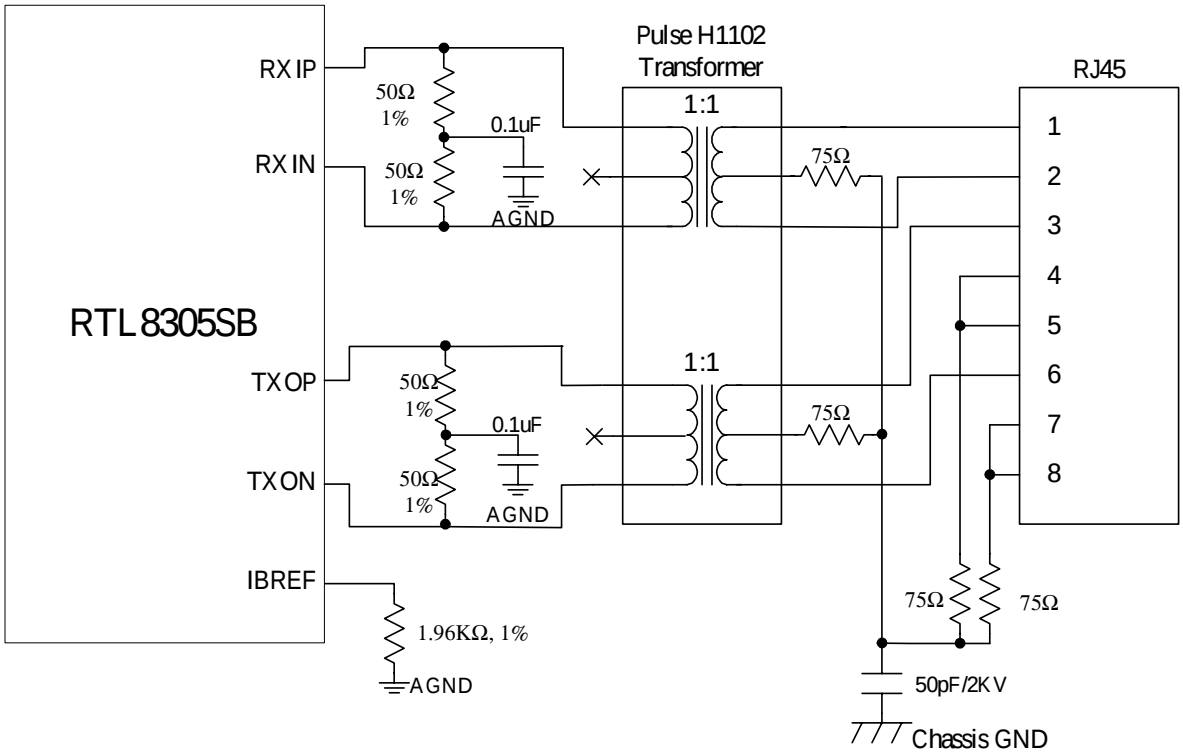


Figure 2. UTP Application for Transformer with Separate Central Tap

4. 100Base-FX Application Circuit

All ports support 100Base-FX, which shares pins with UTP (TX+-/RX+-) and needs no SD+- pins (Realtek patent). 100Base-FX can be forced into half or full duplex mode with optional flow control. In order to operate correctly, both sides of the connection should be set to the same duplex and flow control settings.

Note that 100Base-FX does not support Auto-Negotiation according to IEEE 802.3u. In 100Base-FX mode, a scrambler is not needed and Pins GxANeg/GyANeg/P4Aneg, as well as GxSpd100/GySpd100/P4Spd100, are not used and may be left floating. Compared to common 100Base-FX applications, the RTL8305SB removes a pair of differential SD (Signal Detect) signals that provide a link monitoring function, which reduces the pin count (Realtek patent).

The following is an example of an RTL8305SB connecting to a 3.3V fiber transceiver application circuit with a SIEMENS V23809-C8-C10 (3.3V~5V fiber transceiver, 1*9 SC Duplex Multimode 1300 nm LED Fast Ethernet/FDDI/ATM Optical Transceiver Module). See the following page for a 5V fiber transceiver application circuit example.

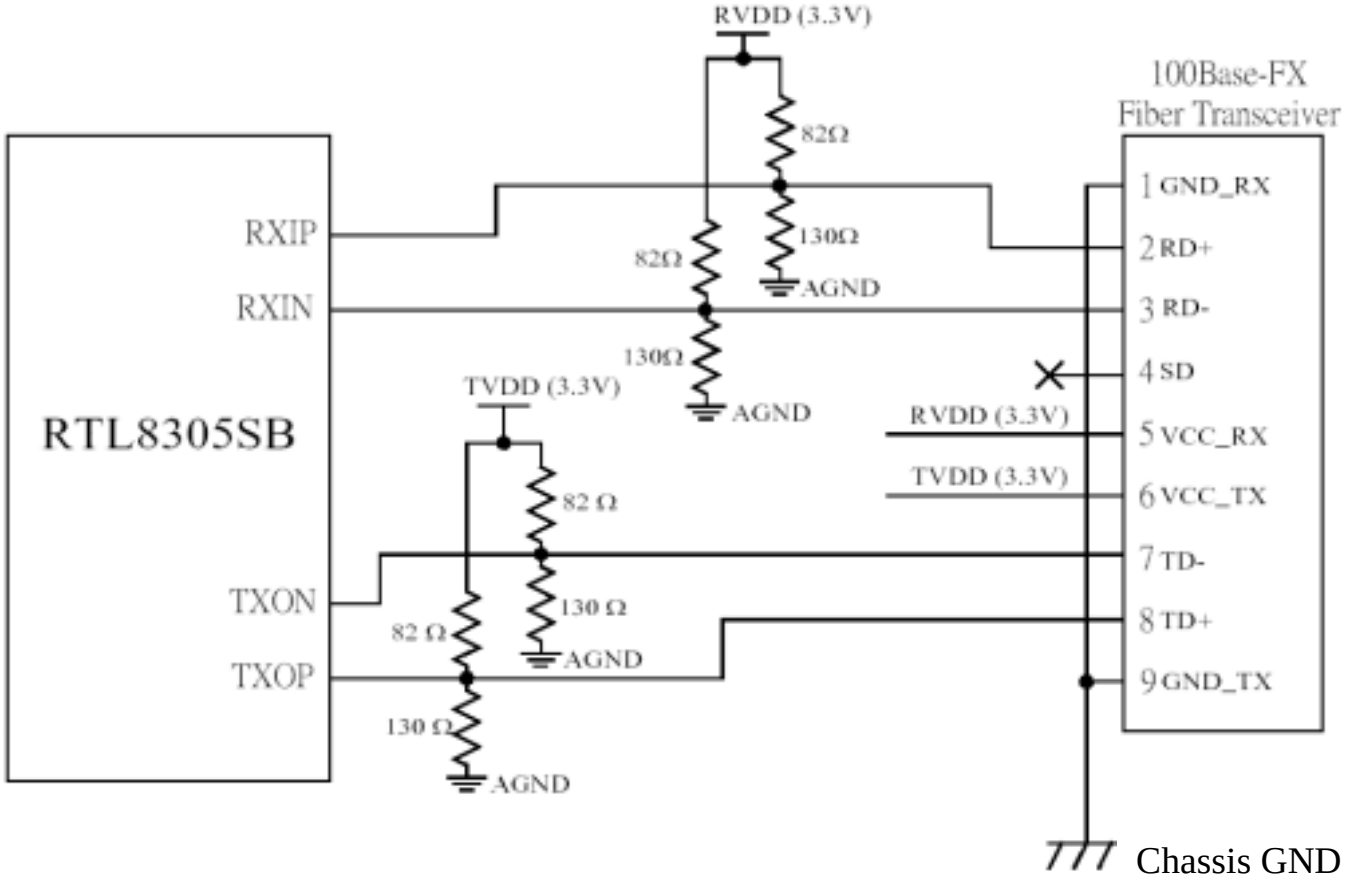


Figure 3. 100Base-FX with 3.3V Fiber Transceiver Application

The following is an example of an RTL8305SB connected to a 5V fiber transceiver application circuit with a SIEMENS V23809-C8-C10 (3.3V~5V fiber transceiver, 1*9 SC Duplex Multimode 1300 nm LED Fast Ethernet/FDDI/ATM Optical Transceiver Module).

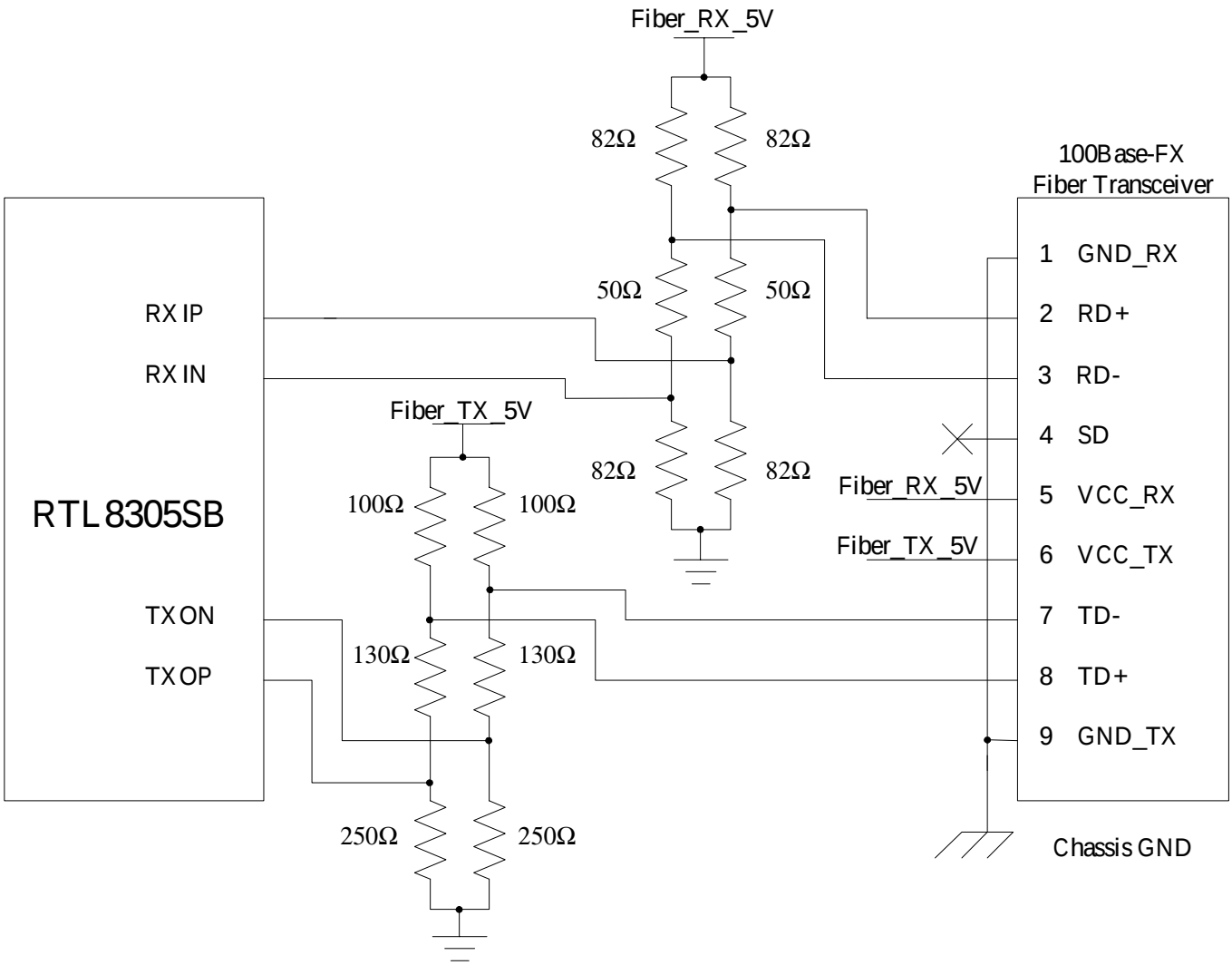


Figure 4. 100Base-FX with 5V Fiber Transceiver Application

5. MII Interface Application Circuit

5.1. Port4 Operating Mode

The fifth port (port 4) supports an external MAC interface which can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to operate with the external MAC of a routing engine, PHY of a HomePNA, or other physical layer transceiver.

If the MAC part of Port4 connects with an external MAC, e.g. the processor of a router application, it will act as a PHY. This is PHY mode MII, or PHY mode SNI. In PHY mode MII or PHY mode SNI, Port4 uses the MAC part only, and provides an external MAC interface to connect to the MAC of an external device. In order to connect both MACs, the MII of the switch MAC should be reversed into PHY mode.

If the MAC part of Port4 connects with an external PHY, such as a PHY for a HomePNA application, Port4 will act as a MAC. This is MAC mode MII. In MAC mode MII, Port4 uses its MAC to connect to the external PHY and ignores the internal PHY.

5.2. Port4 Status Pins

When P4MODE[1:0]=11, Port4 can be either UTP or MAC mode MII. Port4 will automatically detect the link status of UTP from internal PHY, and link status MAC mode MII from both TXC of external PHY and P4LNKSTA#. If both the UTP and MII ports are linked OK, UTP gets higher priority and the RTL8305SB will ignore MII port signals.

In UTP and FX mode, the internal PHY provides the port status (Link/Speed/Duplex/Full Flow Control ability) in real time. In order to provide the initial configuration of Port4's PHY (UTP or FX mode), four pins (P4ANEG, P4Full, P4Spd100, P4EnFC) are used to strap upon reset.

Note: These 4 pins are changed to high active in order to provide a dual function. For example: RTL8305SB=P4SpdSta/P4Spd100, RTL8305SB=P4SpdSta#.

In the other three modes, four pins (P4LNKSTA#, P4SpdSta, P4DupSta, P4FLCTRL) are necessary in order to provide the port status to Port4's MAC in real time. That means that the external MAC or PHY should be forced to the same port status as Port4's MAC.

5.3. Related Pins

Pin **SEL_MIIMAC#** can be used to indicate MII MAC port active after reset for the purpose of UTP/MII auto-detection. One 25MHz clock output (pin CK25MOUT) can be used as a clock source of the underlying HomePNA/other PHY physical device.

Note: The RTL8305SB output voltage is 2.5V. For the RTL8305S it is 3.3V.

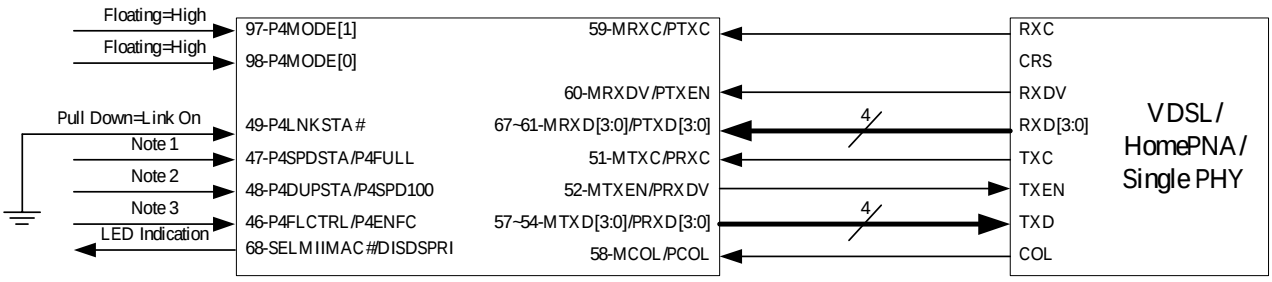
5.4. PHY Mode MII/PHY Mode SNI

In routing applications, the RTL8305SB cooperates with a routing engine to communicate with the WAN (Wide Area Network) through MII/SNI. In such applications, P4LNKSTA# =0 and P4MODE[1] are pulled low upon reset. P4MODE[0] determines whether MII or SNI mode is selected.

In MII (nibble) mode (P4MODE[0]=1):

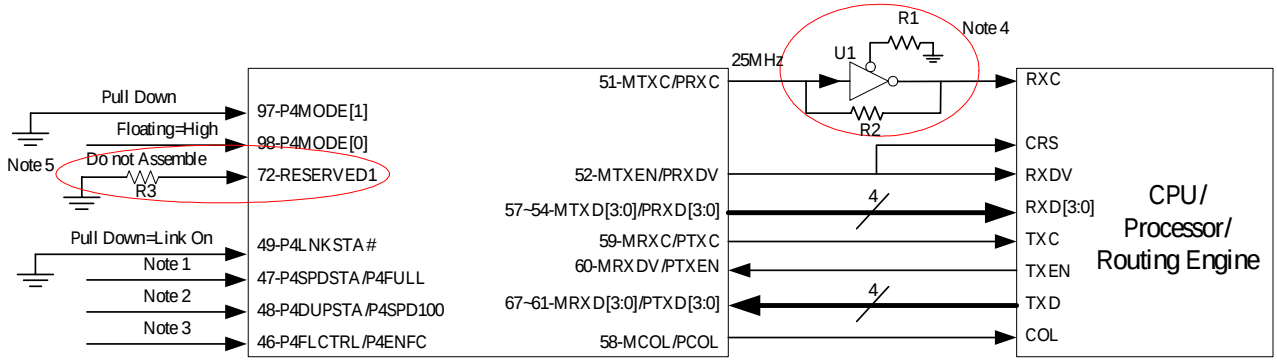
- P4SPDSTA=1: The MII operates at 100Mbps with MTXC and MRXC running at 25MHz.
- P4SPDSTA=0: The MII operates at 10Mbps with MTXC and MRXC running at 2.5MHz.

In SNI (serial) mode (P4MODE[0]=0), P4SPDSTA has no effect and should be pulled-down. SNI mode operates at 10Mbps only, with MTXC and MRXC running at 10MHz. The RTL8305SB does not loopback the RXDV signal as a response to TXEN, and does not support the heart-beat function (asserting COL signal for each completed TXEN signal).



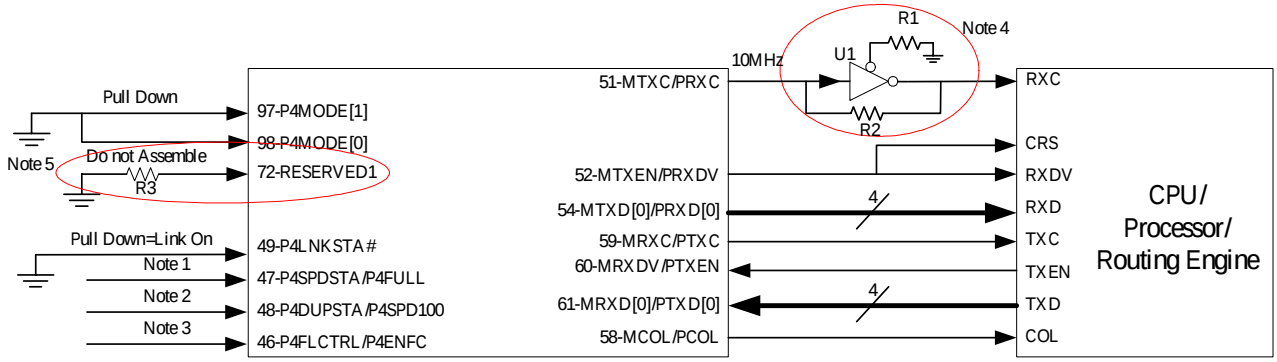
MAC mode MII

Figure 5. MAC Mode MII Interface Application Circuit



PHY mode MII

Figure 6. PHY Mode MII Interface Application Circuit



PHY mode SNI

Figure 7. PHY Mode SNI Interface Application Circuit

Note 1: Pulled high or floating sets the speed to 100Mbps. Pulled down sets the speed to 10Mbps.
Note 2: Pulled high or floating enables full duplex. Pulled down sets half duplex.
Note 3: Pulled high or floating enables flow control or backpressure. Pulled down disables flow control or backpressure.
Note 4: R1 is used to enable/disable the single logic gate. R2 is used to bypass the single logic gate. U1 may be optionally selected as 74LVC1G04 or 74LVC1G125 (gate delay within 5 ns) to fine tune the timing of the MII interface trace.
Note 5: R3 is reserved for future use and should not be assembled.

6. LED Application Circuit

The RTL8305SB supports four parallel LEDs for each port, and two special LEDs (SELMIIMAC# and LOOPLED#). Each port has four LED indicator pins. Each pin may have different indicator meanings (LEDMode[1:0]; refer to the pin descriptions for details).

Upon reset, the RTL8305SB supports chip diagnostics and LED functions by blinking all LEDs once for 320ms. This function can be disabled by asserting EN_RST_LINK to 0. LED_BLINK_TIME determines LED blinking period for activity and collision (1 = 43ms and 0 = 120ms). The parallel LEDs corresponding to port 4 can be three-stated (LED functions disabled) for MII port applications by setting ENP4LED in EEPROM to 0. In UTP applications, this bit should be set to 1 to drive the port 4 LEDs.

All LED pins are dual function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is floating upon reset, the pin output is active low after reset. If the pin input is pulled down upon reset, the pin output is active high after reset. Exception: Bi-color Link/Act mode of pin LED_ADD[4:0] when LEDMode[1:0]=10.

Below is an example LED circuit. The typical value for pull-down resistors is 10K Ω.

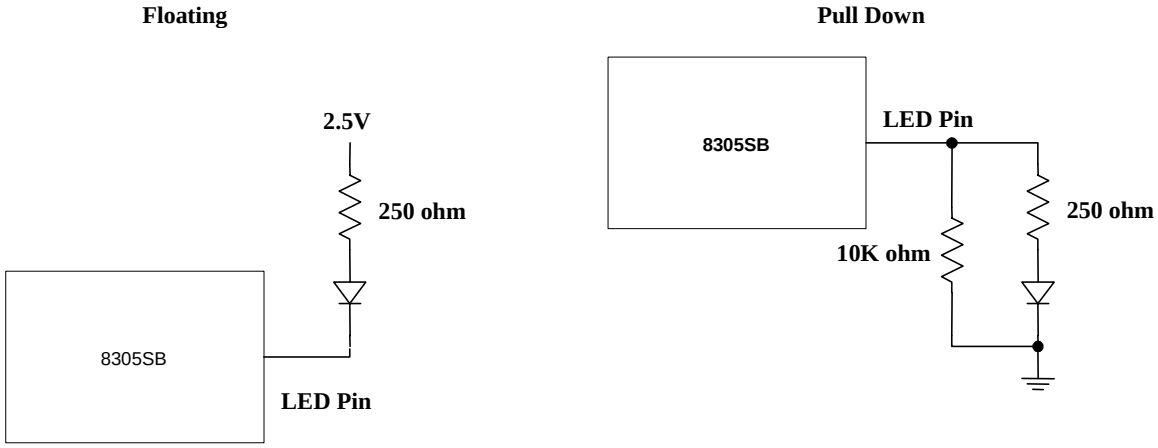


Figure 8. Floating and Pull-Down of LED Pins

For two pin Bi-color LED mode (LEDMode[1:0]=10) Bi-color Link/Act (pin LED_ADD) and Spd (pin LED_SPD) can be used for one Bi-color LED package. This is a single LED package with two LEDs connected in parallel with opposite polarity. When LEDMode[1:0]=10, the active status of LED_ADD is the opposite of LED_SPD and does not affect input upon reset.

Table 2. Truth Table of Spd and Bi-color Link/Act

Indication	**Bi-Color state**	**Spd:Input=Floating, Active Low.** **Bi-color Link/Act:** the active status of LED_ADD is opposite that of LED_SPD and does nothing with input upon reset.		**Spd:Input=Pull-down, Active High.** **Bi-color Link/Act:** the active status of LED_ADD is opposite that of LED_SPD and does nothing with input upon reset.	
		Spd	**Link/Act**	**Spd**	**Link/Act**
No Link	Both Off	1	1	0	0
100M Link	Green On	0	1	1	0
10M Link	Yellow On	1	0	0	1
100M Act	Green Flash	0	Flashing	1	Flashing
10M Act	Yellow Flash	1	Flashing	0	Flashing

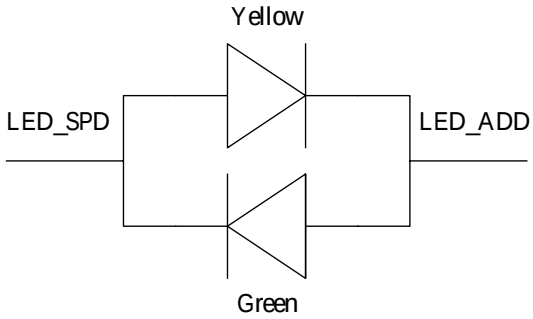


Figure 9. Two Pin Bi-color LED for SPD Floating or Pulled-high

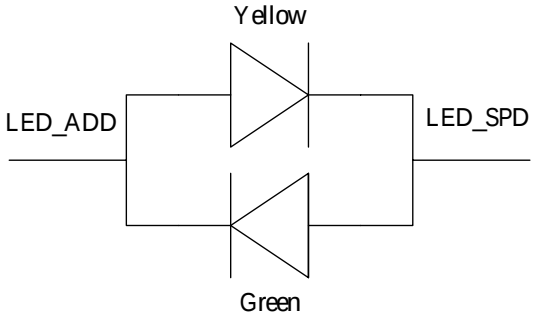


Figure 10. Two Pin Bi-color LED for SPD Pulled-down

7. 2.5V Power Generation

The RTL8305SB uses a PNP transistor to generate 2.5V from the 3.3V power supply. This 2.5V provides for digital core and analog receive circuits. When designs require more than one RTL8305SB chip (a system greater than 8 ports), do not use a single PNP transistor for all of the RTL8305SB chips (even if the rating is sufficient). Use one PNP transistor for each RTL8305SB chip.

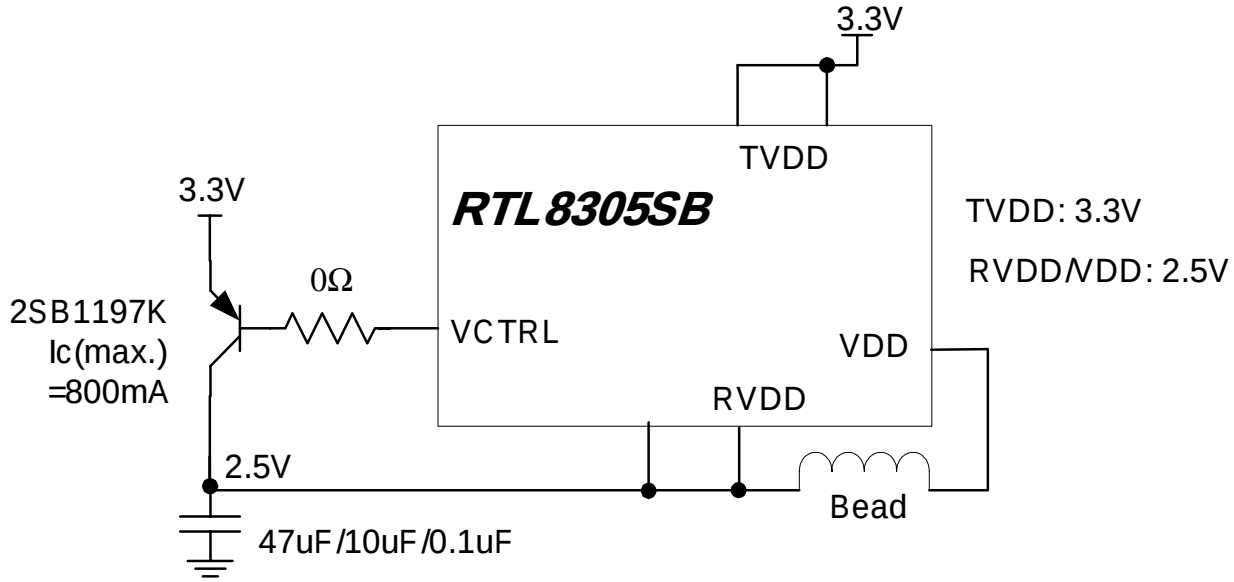


Figure 11. Using a PNP Transistor to Produce 2.5V

Note: Do not connect any beads directly between the collector of the PNP transistor and RVDD. This will affect the stability of the 2.5V power significantly.

The power transistor is a 2SB1197K. Specifications are shown in the following table.

Absolute maximum ratings (Ta=25°C)

Table 3. 2SB1197K PNP Power Transistor Specification

Parameter	Symbol	Limits	Unit
Collector-base voltage	VCBO	-40	V
Collector-emitter voltage	VCEO	-32	V
Emitter-base voltage	VEBO	-5	V
Collector current	IC	-0.8	A (DC)
Collector power dissipation	PC	0.2	W
Junction temperature	Tj	150	°C
Storage temperature	Tstg	-55~+150	°C

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