RTL8186/RTL8186P

WIRELESS LAN ACCESS POINT/ GATEWAY CONTROLLER

Preliminary DATASHEET

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

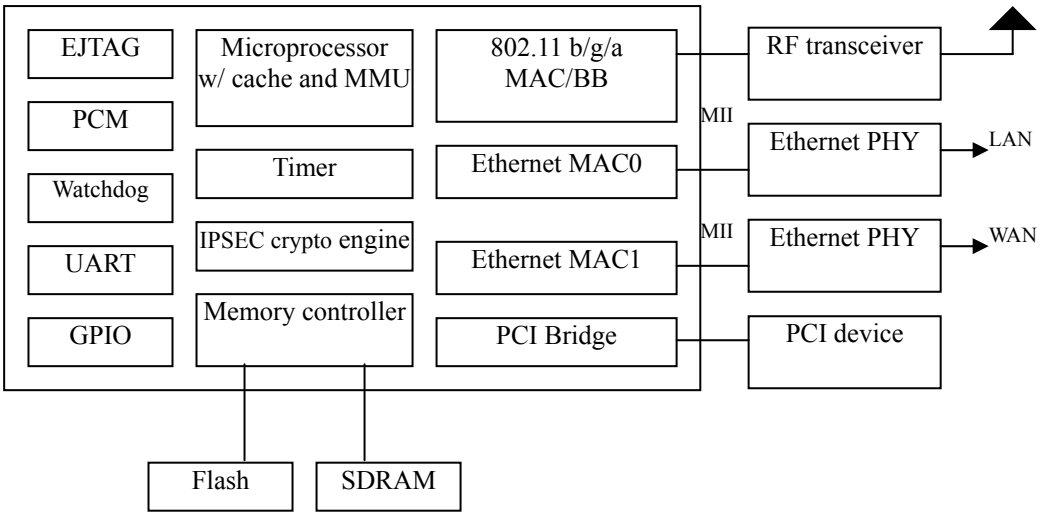
Revision	Release Date	Summary
0.97	2005/8/11	1. Add lead-free, green package ordering information 2. Add thermal characteristics 3. Add DC and AC characteristics 4. Add base clock configuration definition of TCCNR 5. Modify definition on GPIO Port E/F Direction Register
0.96	2005/7/4	Modify DPLL table, PCMISR, GPEPIN and some definitions on memory controller setting.
0.95	2005/4/8	Fix NOR flash and SDRAM chip select pin definition
0.94	2005/3/30	Revise GPIO (A/B/C/D/E/F) pins read/write definition Revise PCI memory space mapping Revise bridge definition
0.93	2005/2/24	Revise C19, C20 pin definition
0.92	2005/1/7	Fix PCI memory space mapping
0.91	2004/12/16	Fix GPIO configuration
0.9	2004/8/4	First preliminary release.

Table of Contents

1. Overview

The RTL8186 is a highly integrated system-on-a-chip (SoC), embedded with a high-performance 32-bit RISC processor, Ethernet, and WLAN controller. It is a cost-effective and high-performance solution for wireless LAN Access Point, wireless SOHO router, wireless Internet gateway systems, etc.

System block diagram:



The embedded processor is a Lexra LX5280 32-bit RISC CPU, with separate 8K instruction and 8K data caches. A Memory Management Unit (MMU) allows the memory to be segmented and protected. Such protection is a requirement of modern operating systems (e.g., Windows NT, 2000, XP, Linux).

The processor pipeline is a dual-issue 6-stage architecture. The dual-issue CPU fetches two instructions per cycle, allowing two instructions to be executed concurrently in two pipes for an up to 30% improvement over uni-scalar architecture.

It includes two Fast Ethernet MACs, one possibly used for the LAN interface and the other connected to a WAN port. An IEEE 802.11a/b/g WLAN MAC+Baseband processor is embedded. By interfacing with an external Realtek RF module, it could provide the total solution for 2.4GHz or 5G.Hz WLAN system.

To support the emergence of VPN applications and the latest test criteria of ICSA, RTL8186 incorporates a full function SH1/MD5/DES/3DES/AES-128 crypto engine. The crypto engine offloads the packet authentication/encryption/decryption job with just a single pass of DMA, and thus it could achieve high performance when IPSEC is deployed in system.

RTL8186 provides a glueless interface for external SDRAM and flash memory devices. It allows customers to use from 1M to 64M bytes SDRAM/flash memory with 16-bit or 32-bit variable length in great flexibility. RTL8186 can also support NOR and NAND type flash, and booting from NAND type flash could be fulfilled without extra cost.

Additionally, RTL8186 provides UART, PCI and PCM interfaces as well as more than 60 GPIO (Programmable I/O) pins. With the PCM interface, the wireless VoIP applications are made possible.

Realtek will provide turn-key solution in both hardware and software. Beside the evaluation board, we will provide hardware reference design kit, and software development kit for customization and adding new features.

Features

Core Processor

- LX5280 32-bit RISC architecture compatible to MIPS R3000 ISA-1
- Superscalar architecture, containing 2 execution pipelines with better performance
- Embedded with 8K I-Cache, 8K D-Cache, 4K I-RAM and 4K D-RAM

- 16-entry MMU supported
- Up to 180MHZ operating frequency

WLAN Controller

- Integrated IEEE 802.11a/b/g complied MAC and DSSS Baseband processor
- Data rate of 54M, 48M, 36M, 24M, 18M, 12M, 9M, 6M, 11M, 5.5M, 2M and 1M
- Support antenna diversity and AGC
- Support 802.11h DFS and TPC
- Embedded with encryption/decryption engine for 64 bits/128 bits WEP, TKIP/MIC and AES
- RF interface to Realtek 2.4G and 5G RF module

Fast Ethernet Controller

- Fully compliant with IEEE 802.3/802.3u
- Supports MII interface with full and half duplex capability
- Supports descriptor-based buffer management with scatter-gather capability
- Supports IP, TCP, and UDP checksum offload
- Supports IEEE 802.1Q VLAN tagging and 802.1P priority queue
- Supports full duplex flow control (IEEE 802.3X)

UART

- 2 UART interfaces
- 16550 compatible
- 16 bytes FIFO size
- Auto CTS/RTS flow control

Memory Controller

- Supports external 16/32-bit SDRAM with 2 banks access, up to 32M bytes for each bank
- Supports two external 16-bit NOR-type Flash memory, up to 8M bytes for each bank
- Supports two external 8-bit NAND-type Flash memory, up to 32M bytes for each bank
- Support boot from NAND type to reduce total bone cost

IPSEC Crypto Engine

- Supports DES, 3DES and AES-128 encryption/decryption algorithm for ESP encryption with throughput up to 120Mbps
- Supports HMAC-MD5 and HMAC-SHA-1 authentication algorithms
- Supports CBC or EBC mode with DES/3DES/AES algorithm
- A 32-bit PRNG (pseudo random number generator)
- Single pass for both authentication and encryption/decryption

PCI Bridge

- Complies with PCI 2.2.
- Supports four external PCI devices.
- Supports PCI master/slave mode with shared IRQ
- 3.3 and 5V I/O tolerance
- One of the PCI device supports memory mapping space up to 16M bytes, others up 512K bytes

GPIO

- 11 dedicate programmable I/O ports and 58 shared GPIO ports
- Individually configurable to input, output and edge transition

Watchdog/Timer/Counter

- Hardware watchdog timer, used to reset the processor if the system hangs.
- 4 sets of general timers/counter

EJTAG

- Use standard IEEE 1149.1 JTAG interface for software debugging

PCM

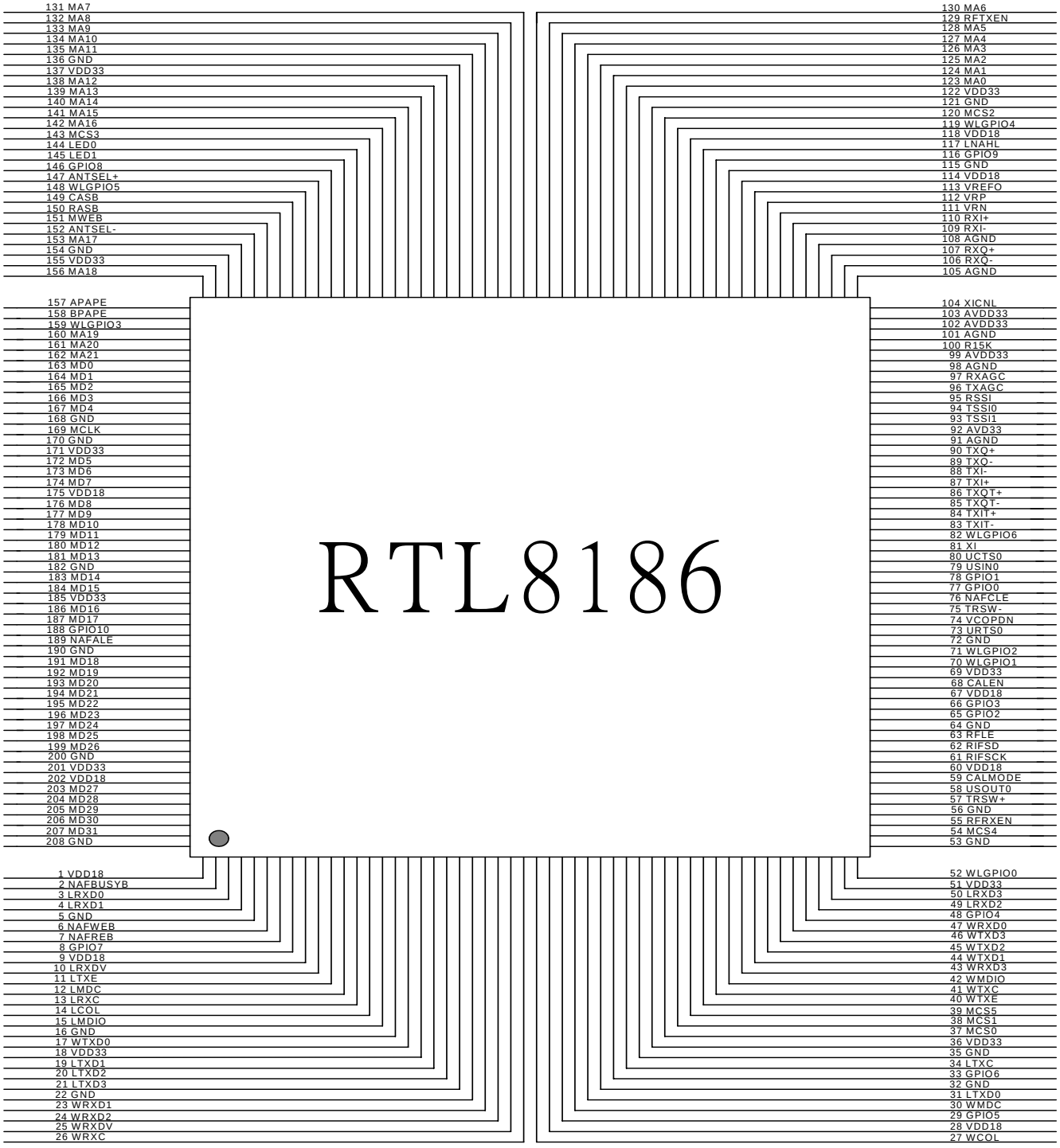
- Supports 4 audio channels
- Supports bus master mode
- Supports G..711 u-law and a-law

Package

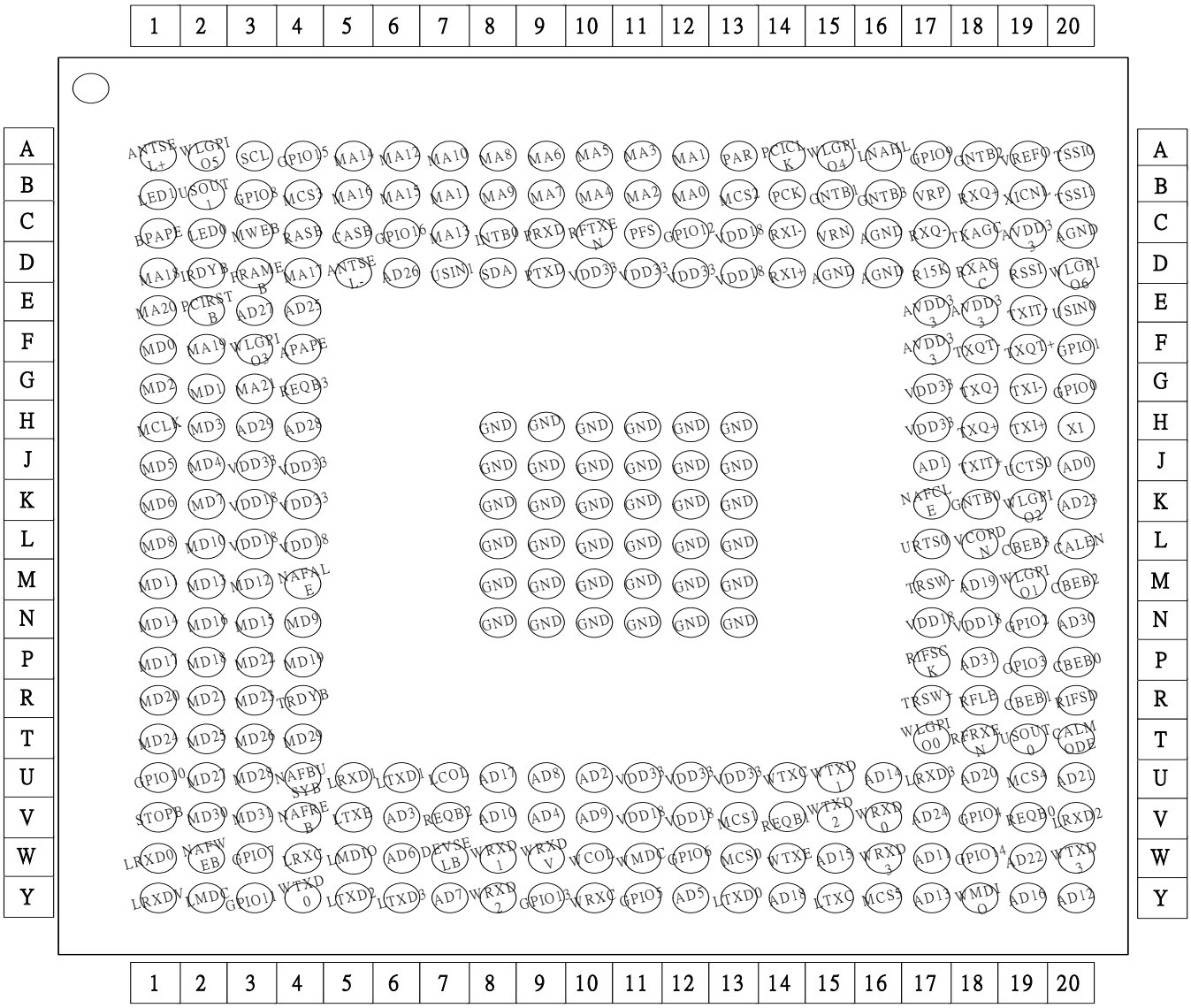
- RTL8186 208-Pin QFP (Without PCI Interface).
- RTL8186P 292-Pin TFBGA (With PCI Interface).

2. Pin Assignments

RTL8186 208-Pin QFP Pin Assignments:


RTL8186
1 VDD18
2 NAFBUSYB
3 LRXD0
4 LRXD1
5 GND
6 NAFWEB
7 NAFREB
8 GPIO7
9 VDD18
10 LRXDV
11 LTXE
12 LMDC
13 LRXC
14 LCOL
15 LMDIO
16 GND
17 WTXD0
18 VDD33
19 LTXD1
20 LTXD2
21 LTXD3
22 GND
23 WRXD1
24 WRXD2
25 WRXDV
26 WRXC
27 WCOL
28 VDD18
29 GPIO5
30 WMDC
31 LTXD0
32 GND
33 GPIO6
34 LTXC
35 GND
36 VDD33
37 MCS0
38 MCS1
39 MCS5
40 WTXE
41 WTXC
42 WMDIO
43 WRXD3
44 WTXD1
45 WTXD2
46 WTXD3
47 WRXD0
48 GPIO4
49 LRXD2
50 LRXD3
51 VDD33
52 WLGPIO0
53 GND
54 MCS4
55 RFRXEN
56 GND
57 TRSW+
58 USOUT0
59 CALMODE
60 VDD18
61 RIFSCK
62 RIFSD
63 RFLE
64 GND
65 GPIO2
66 GPIO3
67 VDD18
68 CALEN
69 VDD33
70 WLGPIO1
71 WLGPIO2
72 GND
73 URTS0
74 VCOPDN
75 TRSW-
76 NAFCLE
77 GPIO0
78 GPIO1
79 USIN0
80 UCTS0
81 XI
82 WLGPIO6
83 TXIT-
84 TXIT+
85 TXQT-
86 TXQT+
87 TXI+
88 TXI-
89 TXQ-
90 TXQ+
91 AGND
92 AVD33
93 TSSI1
94 TSSI0
95 RSSI
96 TXAGC
97 RXAGC
98 AGND
99 AVDD33
100 R15K
101 AGND
102 AVDD33
103 AVDD33
104 XICNL
105 AGND
106 RXQ-
107 RXQ+
108 AGND
109 RXI-
110 RXI+
111 VRN
112 VRP
113 VREFO
114 VDD18
115 GND
116 GPIO9
117 LNAHL
118 VDD18
119 WLGPIO4
120 MCS2
121 GND
122 VDD33
123 MA0
124 MA1
125 MA2
126 MA3
127 MA4
128 MA5
129 RFTXEN
130 MA6
131 MA7
132 MA8
133 MA9
134 MA10
135 MA11
136 GND
137 VDD33
138 MA12
139 MA13
140 MA14
141 MA15
142 MA16
143 MCS3
144 LED0
145 LED1
146 GPIO8
147 ANTSEL+
148 WLGPIO5
149 CASB
150 RASB
151 MWEB
152 ANTSEL-
153 MA17
154 GND
155 VDD33
156 MA18
157 APAPE
158 BPAPE
159 WLGPIO3
160 MA19
161 MA20
162 MA21
163 MD0
164 MD1
165 MD2
166 MD3
167 MD4
168 GND
169 MCLK
170 GND
171 VDD33
172 MD5
173 MD6
174 MD7
175 VDD18
176 MD8
177 MD9
178 MD10
179 MD11
180 MD12
181 MD13
182 GND
183 MD14
184 MD15
185 VDD33
186 MD16
187 MD17
188 GPIO10
189 NAFALE
190 GND
191 MD18
192 MD19
193 MD20
194 MD21
195 MD22
196 MD23
197 MD24
198 MD25
199 MD26
200 GND
201 VDD33
202 VDD18
203 MD27
204 MD28
205 MD29
206 MD30
207 MD31
208 GND

RTL8186P 292-Pin TFBGA Pin Assignments:



3. Pin Description

Memory Interface

Symbol	Type	208 QFP Pin No	256 BGA Pin No	Description
Memory Interface				
MDPIN[0] MDPIN[1] MDPIN[2] MDPIN[3]	I/O	163 164 165 166	F1 G2 G1 H2	Data for SDRAM, Nor-type and NAND-type Flash.

MDPIN[4]		167	J2	
MDPIN[5]		172	J1	
MDPIN[6]		173	K1	
MDPIN[7]		174	K2	
MDPIN[8]		176	L1	
MDPIN[9]		177	N4	
MDPIN[10]		178	L2	
MDPIN[11]		179	M1	
MDPIN[12]		180	M3	
MDPIN[13]		181	M2	
MDPIN[14]		183	N1	
MDPIN[15]		184	N3	
MDPIN[16]		186	N2	
MDPIN[17]		187	P1	
MDPIN[18]		191	P2	
MDPIN[19]		192	P4	
MDPIN[20]		193	R1	
MDPIN[21]		194	R2	
MDPIN[22]		195	P3	
MDPIN[23]		196	R3	
MDPIN[24]		197	T1	
MDPIN[25]		198	T2	
MDPIN[26]		199	T3	
MDPIN[27]		203	U2	
MDPIN[28]		204	U3	
MDPIN[29]		205	T4	
MDPIN[30]		206	V2	
MDPIN[31]		207	V3	
MAPIN[0]	O	123	B12	Address for SDRAM, Nor-type and NAND-type Flash.
MAPIN[1]		124	A12	MAPIN[18-15] mapping to DQM[3-0] for SDRAM
MAPIN[2]		125	B11	
MAPIN[3]		126	A11	
MAPIN[4]		127	B10	
MAPIN[5]		128	A10	
MAPIN[6]		130	A9	
MAPIN[7]		131	B9	
MAPIN[8]		132	A8	
MAPIN[9]		133	B8	
MAPIN[10]		134	A7	
MAPIN[11]		135	B7	
MAPIN[12]		138	A6	
MAPIN[13]		139	C7	
MAPIN[14]		140	A5	
MAPIN[15]		141	B6	
MAPIN[16]		142	B5	
MAPIN[17]		153	D4	
MAPIN[18]		156	D1	
MAPIN[19]		160	F2	
MAPIN[20]		161	E1	
MAPIN[21]		162	G3	
SDCLKPIN	O	169	H1	SDRAM clock
MCSPIN[0]	O	37	W13	Nor-type Flash chip select
MCSPIN[1]		38	V13	
MCSPIN[2]	O	120	B13	SDRAM chip select
MCSPIN[3]		143	B4	
MCSPIN[4]	O	54	U19	NAND-type Flash chip select
MCSPIN[5]		39	Y16	
RASBPIN	O	150	C4	Raw address strobe for SDRAM, this pin is also the output enable pin for Nor-type Flash

CASBPIN	O	149	C5	SDRAM column address strobe
MWEBPIN	O	151	C3	Write enable for SDRAM and Flash
NAFBUSYBPIN	I	2	U4	NAND-type flash ready/busy status indication.
NAFWEBPIN	O	6	W2	NAND-type flash Write Enable.
NAFREBPIN	O	7	V4	NAND-type flash Read Enable.
NAFCLEPIN	O	76	K17	NAND-type flash Command Latch Enable.
NAFALEPIN	O	189	M4	NAND-type flash Address Latch Enable.
UART0 Interface				
UCTS0PIN	I	80	J19	Uart0 Clear-to-Send signal. This pin mux-ed function with I2C SDAPIN at 208 QFP package.
URTS0PIN	O	73	L17	Uart0 Request-to-Send signal. This pin mux-ed function with I2C SCLPIN at 208 QFP package.
USIN0PIN	I	79	E20	Uart0 In data signal.
USOUT0PIN	O	58	T19	Uart0 Out data signal.
UART1 Interface				
USIN1PIN	I	NA	D7	Uart1 In data signal.
USOUT1PIN	O	NA	B2	Uart1 Out data signal.
I2C Interface				
SDAPIN	I/O	NA	D8	I2C data signal.
SCLPIN	O	NA	A3	I2C clock signal.
PCM Interface				
PCKPIN	I/O	NA	B14	PCM clock signal.
PFSPIN	O	NA	C11	PCM FS signal.
PTXDPIN	O	NA	D9	PCM TX data signal.
PRXDPIN	O	NA	C9	PCM RX data signal.
WLAN Traffic LED Control				
WLLED0PIN[0]	O	144	C2	WLAN Tx/Rx traffic indicator.
WLLED0PIN[1]	O	145	B1	WLAN Tx/Rx traffic indicator.
RF Interface for Realtek 8225 [802.11 b/g RF]				
VREFO	X	113	A19	Not used in 8225 RF chipset.
VRP	X	112	B17	Not used in 8225 RF chipset.
VRN	X	111	C15	Not used in 8225 RF chipset.
RXIP RXIN	I I	110 109	D14 C14	Receive (Rx) In-phase Analog Data.
RXQP RXQN	I	107 106	B18 C17	Receive (Rx) Quadrature-phase Analog Data.
R15K	I/O	100	D17	This pin must be pulled low by a 15K Ω resistor.
RXAGC	O	97	D18	Not used in 8225 RF chipset.
TXAGC	O	96	C18	Not used in 8225 RF chipset.
RSSI	I	95	D19	Analog Input to the Receive Power A/D Converter for Receive AGC Control.
TSSI0	I	94	A20	Input to the Transmit Power A/D Converter for 2.4GHz Transmit AGC Control.
TSSI1	I	93	B20	Not used in 8225 RF chipset.
TXQP TXQN	O O	90 89	H18 G18	Not used in 8225 RF chipset.
TXIN TXIP	O O	88 87	G19 H19	Not used in 8225 RF chipset.
XI	I	81	H20	40 MHz OSC Input.
XIPWRSEL	I	104	B19	Operating frequency voltage selection between 3.3v and 1.8v.
TXQTP TXQTN	O O	86 85	F19 F18	Transmit (TX) Quadrature-phase Analog Data.
TXITP TXITN	O O	84 83	J18 E19	Transmit (TX) In-phase Analog Data.
RIFSCKPIN	O	61	P17	Serial Clock Output. All operation mode switching and register setting is done by 4-wire serial interface.

RIFSDPIN	I/O	62	R20	Serial Data Input/Output.
RFLEPIN	O	63	R18	Serial Enable control.
CALENPIN	O	68	L20	Serial Read/Write control.
CALMODEPIN	I/O	59	T20	Not used in 8225 RF chipset.
VCOPDNPIN	O	74	L18	This pin is used to turn on/off RF transceiver.
hTRSWPIN TRSWBPIN	O O	57 75	R17 M17	Transmit/Receive path select. The TRSW select signal controls the direction of the Transmit/Receive switch.
RFTXENPIN	O	129	C10	Not used in 8225 RF chipset.
RFRXENPIN	O	55	T18	Not used in 8225 RF chipset.
LNAHLPIN	O	117	A16	Not used in 8225 RF chipset.
ANTSELPIN ANTSELBPIN	O O	147 152	A1 D5	Antenna Select. The antenna detects signal change states as the receiver switches from antenna to antenna during the acquisition process in antenna diversity mode.
A_PAPEPIN	O	157	F4	2.4GHz Transmit Power Amplifier Power Enable.
B_PAPEPIN	O	158	C1	Not used in 8225 RF chipset.
WLGPIOPIN[0]	I/O	52	T17	General purpose input/output pin.
WLGPIOPIN[1]	I/O	70	M19	General purpose input/output pin.
WLGPIOPIN[2]	I/O	71	K19	General purpose input/output pin.
WLGPIOPIN[3]	I/O	159	F3	General purpose input/output pin.
WLGPIOPIN[4]	I/O	119	A15	General purpose input/output pin.
WLGPIOPIN[5]	I/O	148	A2	General purpose input/output pin.
WLGPIOPIN[6]	I/O	82	D20	General purpose input/output pin.
RF Interface for Realtek 8255 [802.11 a/b/g RF]				
VREFO	X	113	A19	Not used in 8255 RF chipset.
VRP	X	112	B17	Not used in 8255 RF chipset.
VRN	X	111	C15	Not used in 8255 RF chipset.
RXIP RXIN	I I	110 109	D14 C14	Receive (Rx) In-phase Analog Data.
RXQP RXQN	I	107 106	B18 C17	Receive (Rx) Quadrature-phase Analog Data.
R15K	I/O	100	D17	This pin must be pulled low by a 15K Ω resistor.
RXAGC	O	97	D18	Not used in 8255 RF chipset.
TXAGC	O	96	C18	Not used in 8255 RF chipset.
RSSI	I	95	D19	Analog Input to the Receive Power A/D Converter for Receive AGC Control.
TSSI0	I	94	A20	Input to the Transmit Power A/D Converter for 2.4GHz Transmit AGC Control.
TSSI1	I	93	B20	Input to the Transmit Power A/D Converter for 5GHz Transmit AGC Control.
TXQP TXQN	O O	90 89	H18 G18	Transmit (TX) Quadrature-phase Analog Data.
TXIN TXIP	O O	88 87	G19 H19	Transmit (TX) In-phase Analog Data.
XI	I	81	H20	40 MHz OSC Input.
XIPWRSEL	I	104	B19	Operating frequency voltage selection between 3.3v and 1.8v.
TXQTP TXQTN	O O	86 85	F19 F18	Not used in 8255 RF chipset.
TXITP TXITN	O O	84 83	J18 E19	Not used in 8255 RF chipset.
RIFSCKPIN	O	61	P17	Serial Clock Output. All operation mode switching and register setting is done by 3-wire serial interface.
RIFSDPIN	I/O	62	R20	Serial Data Input/Output.
RFLEPIN	O	63	R18	Serial Enable control.
CALENPIN	O	68	L20	Not used in 8255 RF chipset.

CALMODEPIN	I/O	59	T20	Not used in 8255 RF chipset.
VCOPDNPIN	O	74	L18	This pin is used to turn on/off RF transceiver.
TRSWPIN TRSWBPIN	O O	57 75	R17 M17	Transmit/Receive path select. The TRSW select signal controls the direction of the Transmit/Receive switch.
RFTXENPIN	O	129	C10	Not used in 8255 RF chipset.
RFRXENPIN	O	55	T18	Not used in 8255 RF chipset.
LNAHLPIN	O	117	A16	Not used in 8255 RF chipset.
ANTSELPIN ANTSELBPIN	O O	147 152	A1 D5	Antenna Select. The antenna detects signal change states as the receiver switches from antenna to antenna during the acquisition process in antenna diversity mode.
A_PAPEPIN	O	157	F4	2.4GHz Transmit Power Amplifier Power Enable.
B_PAPEPIN	O	158	C1	5GHz Transmit Power Amplifier Power Enable.
WLGPIOPIN[0]	I/O	52	T17	General purpose input/output pin.
WLGPIOPIN[1]	I/O	70	M19	General purpose input/output pin.
WLGPIOPIN[2]	I/O	71	K19	General purpose input/output pin.
WLGPIOPIN[3]	I/O	159	F3	General purpose input/output pin.
WLGPIOPIN[4]	I/O	119	A15	General purpose input/output pin.
WLGPIOPIN[5]	I/O	148	A2	General purpose input/output pin.
WLGPIOPIN[6]	I/O	82	D20	General purpose input/output pin.
LAN Interface				
LRXCPIN	I	13	W4	This is a continuous clock that is recovered from the incoming data. The RX clock is 25MHz in 100Mbps and 2.5Mhz in 10Mbs.
LRXDPIN[0] LRXDPIN[1] LRXDPIN[2] LRXDPIN[3]	I	3 4 49 50	W1 U5 V20 U17	This is a group of 4 data signals aligned on nibble boundaries which are driven synchronous to the RX clock by the external physical unit
LRXDVPIN	I	10	Y1	Data valid is asserted by an external PHY when receive data is present on the RXD[3:0] lines, and it is deasserted at the end of the packet. This signal is valid on the rising of the RXC.
LTXCPIN	I	34	Y15	TXC is a continuous clock that provides a timing reference for the transfer of TXD[3:0], TXE. In MII mode, it uses the 25 MHz or 2.5 MHz supplied by the external PMD device.
LTXEPIN	O	11	V5	Indicates the presence of valid nibble data on TXD[3:0].
LTXDPIN[0] LTXDPIN[1] LTXDPIN[2] LTXDPIN[3]	O	31 19 20 21	Y13 U6 Y5 Y6	Four parallel transmit data lines which are driven synchronous to the TXC for transmission by the external physical layer chip.
LCOLPIN	I	14	U7	This signal is asserted high synchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
LMDIOPIN	I/O	15	W5	Management Data Input/Output: This pin provides the bi-directional signal used to transfer management information.
LMDCPIN	O	12	Y2	Management Data Clock: This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks.
WAN Interface				
WRXCPIN	I	26	Y10	This is a continuous clock that is recovered from the incoming data. The RX clock is 25MHz in 100Mbps and 2.5Mhz in 10Mbs.
WRXDPIN[0] WRXDPIN[1] WRXDPIN[2] WRXDPIN[3]	I	47 23 24 43	V16 W8 Y8 W16	This is a group of 4 data signals aligned on nibble boundaries which are driven synchronous to the RX clock by the external physical unit
WRXDVPIN	I	25	W9	Data valid is asserted by an external PHY when receive data is present on the RXD[3:0] lines, and it is deasserted at the end of the packet. This signal is valid on the rising of the RXC.
WTXCPIN	I	41	U14	TXC is a continuous clock that provides a timing reference for the transfer of TXD[3:0], TXE. In MII mode, it uses the 25 MHz or 2.5 MHz supplied

				by the external PMD device.
WTXEPIN	O	40	W14	Indicates the presence of valid nibble data on TXD[3:0].
WTXDPIN[0] WTXDPIN[1] WTXDPIN[2] WTXDPIN[3]	O	17 44 45 46	Y4 U15 V15 W20	Four parallel transmit data lines which are driven synchronous to the TXC for transmission by the external physical layer chip.
WCOLPIN	I	27	W10	This signal is asserted high synchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
WMDIOPIN	I/O	42	Y18	Management Data Input/Output: This pin provides the bi-directional signal used to transfer management information.
WMDCPIN	O	30	W11	Management Data Clock: This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks.
GPIO Group A				
GPAPIN[0]	I/O	77	G20	
GPAPIN[1]	I/O	78	F20	
GPAPIN[2]	I/O	65	N19	
GPAPIN[3]	I/O	66	P19	
GPAPIN[4]	I/O	48	V18	
GPAPIN[5]	I/O	29	Y11	
GPAPIN[6]	I/O	33	W12	This pin also be JTAG_TDI when JTAG function is enabled.
GPAPIN[7]	I/O	8	W3	This pin also be JTAG_TMS when JTAG function is enabled.
GPAPIN[8]	I/O	146	B3	This pin also be JTAG_TRSTN when JTAG function is enabled.
GPAPIN[9]	I/O	116	A17	This pin also be JTAG_TDO when JTAG function is enabled.
GPAPIN[10]	I	188	U1	EXTERNAL RESET_
GPIO Group F				
GPFPIN[0]	I/O	NA	Y3	Reserved
GPFPIN[1]	I/O	NA	C12	
GPFPIN[2]	I/O	NA	Y9	
GPFPIN[3]	I/O	NA	W18	
GPFPIN[4]	I/O	NA	A4	
GPFPIN[5]	I/O	NA	C6	
PCI Interface				
PCIADPIN[0] PCIADPIN[1] PCIADPIN[2] PCIADPIN[3] PCIADPIN[4] PCIADPIN[5] PCIADPIN[6] PCIADPIN[7] PCIADPIN[8] PCIADPIN[9] PCIADPIN[10] PCIADPIN[11] PCIADPIN[12] PCIADPIN[13] PCIADPIN[14] PCIADPIN[15] PCIADPIN[16] PCIADPIN[17] PCIADPIN[18] PCIADPIN[19] PCIADPIN[20] PCIADPIN[21] PCIADPIN[22] PCIADPIN[23] PCIADPIN[24]	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA NA	J20 J17 U10 V6 V9 Y12 W6 Y7 U9 V10 V8 W17 Y20 Y17 U16 W15 Y19 U8 Y14 M18 U18 U20 W19 K20 V17	PCI address and data multiplexed pins. The address phase is the first clock cycle in which FRAMEB is asserted. During the address phase, AD31-0 contains a physical address (32 bits). For I/O, this is a byte address, and for configuration and memory, it is a double-word address. Write data is stable and valid when IRDYB is asserted. Read data is stable and valid when TRDYB is asserted. Data I is transferred during those clocks where both IRDYB and TRDYB are asserted.

PCIADPIN[25] PCIADPIN[26] PCIADPIN[27] PCIADPIN[28] PCIADPIN[29] PCIADPIN[30] PCIADPIN[31]	I/O I/O I/O I/O I/O I/O I/O	NA NA NA NA NA NA NA	E4 D6 E3 H4 H3 N20 P18	
CBEBPIN[0] CBEBPIN[1] CBEBPIN[2] CBEBPIN[3]	I/O I/O I/O I/O	NA NA NA NA	P20 R19 M20 L19	PCI bus command and byte enables multiplexed pins. During the address phase of a transaction, C/BE3-0 define the bus command. During the data phase, C/BE3-0 are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0 applies to byte 0, and C/BE3 applies to byte 3.
PCICLKPIN	O	NA	A14	PCI clock: This clock input provides timing for all PCI transactions and is input to the PCI device.
PCIRTSBPIN	O	NA	E2	Reset: Active low signal to reset the PCI device.
FRAMEBPIN	I/O	NA	D3	Cycle Frame: As a bus master, this pin indicates the beginning and duration of an access. FRAMEB is asserted low to indicate the start of a bus transaction. While FRAMEB is asserted, data transfer continues. When FRAMEB is deasserted, the transaction is in the final data phase. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
IRDYBPIN	I/O	NA	D2	Initiator Ready: This indicates the initiating agent's ability to complete the current data phase of the transaction. As a bus master, this signal will be asserted low when the RTL8186 is ready to complete the current data phase transaction. This signal is used in conjunction with the TRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low. As a target, this signal indicates that the master has put data on the bus.
TRDYBPIN	I/O	NA	R4	Target Ready: This indicates the target agent's ability to complete the current phase of the transaction. As a bus master, this signal indicates that the target is ready for the data during write operations and with the data during read operations. As a target, this signal will be asserted low when the (slave) device is ready to complete the current data phase transaction. This signal is used in conjunction with the IRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low.
STOPBPIN	I/O	NA	V1	Stop: Indicates that the current target is requesting the master to stop the current transaction.
DEVSELBPIN	I/O	NA	W7	Device Select: As a bus master, the RTL8186 samples this signal to insure that a PCI target recognizes the destination address for the data transfer.
PARPIN	I/O	NA	A13	Parity: This signal indicates even parity across AD31-0 and C/BE3-0 including the PAR pin. PAR is stable and valid one clock after each address phase. For data phase, PAR is stable and valid one clock after either IRDYB is asserted on a write transaction or TRDYB is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. As a bus master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.
REQB0PIN	I	NA	V19	Request: Request indicates to the arbiter that this agent desires use of the bus.
GNTB0PIN	O	NA	K18	Grant: Grant indicate to the agent that access to the bus has been granted.
REQB1PIN	I	NA	V14	Request: Request indicates to the arbiter that this agent desires use of the bus.
GNTB1PIN	O	NA	B15	Grant: Grant indicate to the agent that access to the bus has been granted.
REQB2PIN	I	NA	V7	Request: Request indicates to the arbiter that this agent desires use of the bus.
GNTB2PIN	O	NA	A18	Grant: Grant indicate to the agent that access to the bus has been granted.
REQB3PIN	I	NA	G4	Request: Request indicates to the arbiter that this agent desires use of the

				bus.
GNTB3PIN	O	NA	B16	Grant: Grant indicate to the agent that access to the bus has been granted.
INTB0PIN	I	NA	C8	Interrupt A: Used to request an interrupt. It is asserted low when an interrupt condition occurs, as defined by the Interrupt Status, Interrupt Mask.
Power & GND				
DVDD33	-	18 36 51 69 122 137 155 171 185 201	D10 D11 D12 G17 H17 J3 J4 K4 U11 U12 U13	CPU power +3.3V (Digital),
DGND33	-	16 35 53 72 121 136 154 168 182 200	H10 H11 H12 H13 H8 H9 J10 J11 J12 J13	CPU 3.3 GND (Digital)
DVDD18	-	1 9 28 60 67 114 118 175 202	C13 D13 K3 L3 L4 N17 N18 V11 V12	CPU +1.8V (Digital)
DGND18	-	5 22 32 56 64 115 170 190 208	J8 J9 K10 K11 K12 K13 K8 K9 L10 L11 L12 L13 L8 L9 M10 M11 M12 N10 N11 N12 N13 N8 N9	CPU 1.8Ground (Digital)

			M13 M8 M9	
VDDA	-	102 103	E17 E18 F17	Wireless LAN power 3.3V(Analog)
GNDA	-	101 105	C16 D15 D16	Wireless LAN Ground (Analog)
GNDSUB	-	108	-	Wireless LAN Ground (Analog), GA7 VSUB
VDDBG	-	99	-	Analog VDD for WLAN Baseband.
GNDBG	-	98	-	Analog GND for WLAN Baseband.
VDDPLL	-	92	C19	PLL power(Analog)
GNDPLL	-	91	C20	PLL Ground(Analog)

4. Address Mapping

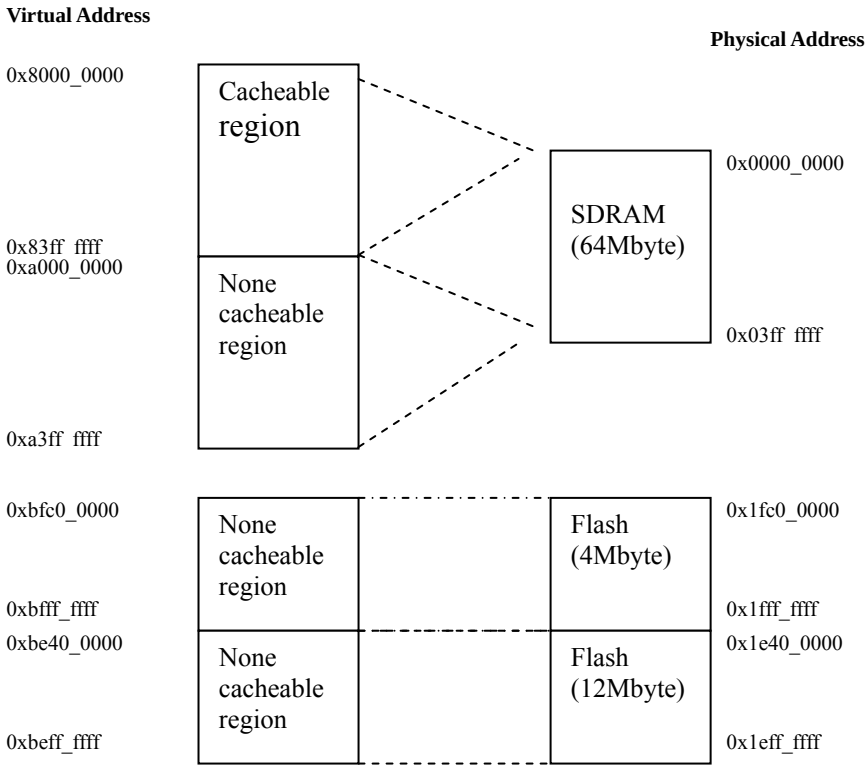
The RTL8186 supports up to 4 gigabytes of logical address space, mapped to two kinds of memory device (SDRAM and ROM/FLASH). The memory address mapping is managed by MMU, which translates the virtual address to physical address. The memory is segmented into four regions by its access mode and caching capability as shown in following table.

Segment	Size	Caching	Virtual address range	Physical address range	Mode
KUSEG	2048M	cacheable	0x0000_0000-0x7fff_ffff	set in TLB	user/kernel
KSEG0	512M	cacheable	0x8000_0000-0x9fff_ffff	0x0000_0000-0x1fff_ffff	kernel
KSEG1	512M	uncachable	0xa000_0000-0xbfff_ffff	0x0000_0000-0x1fff_ffff	kernel
KSEG2	512M	cacheable	0xc000_0000-0xfeff_ffff	set in TLB	kernel
KSEG2	512M	cacheable	0xff00_0000-0xffff_ffff	0xff00_0000-0xffff_ffff	kernel

The RTL8186 has two memory mapping modes: direct memory mapping and TLB (Translation Look-aside Buffer) address mapping. When virtual address is located in the regions KSEG0, KSEG1 or higher half of KSEG2 segments, it physical address will be mapped directly from virtual address with an offset. If a virtual address is used in the region of KUSEG or lower half of KSEG2 segment, its physical address will be referred from TLB entry. RTL8186 contains 16 TLB entries, each of which maps to a page, with read/write access, cache-ability and process id.

In RTL8186, SDRAM is mapped from physical address 0x0000_0000 to maximum 0x03ff_ffff (64M bytes). After reset, RTL8186 will start to fetch instructions from logical address 0xbfc0_0000, the starting address of first flash memory. The flash memory is mapped from physical address 0x1fc0_0000 to maximum 0x1fff_ffff (4M bytes). If flash size is greater than 4M, the physical address of flash memory more than 4M, will map from 0x1e40_0000 to 0x1eff_ffff.

Memory Map (without TLB):



The memory map of RTL8186 I/O devices and registers are located in KSEG1 segment (uncacheable region). The following table illustrates the address map:

Virtual address range	Size (bytes)	Mapped device
0xBD01_0000 – 0xBD01_0FFF	4K	Special function registers (note)
0xBD01_1000 – 0xBD01_1FFF	4K	Memory controller registers
0xBD10_0000 – 0xBD17_FFFF	512K	IPSec Crypto Engine registers
0xBD18_0000 – 0xBD1F_FFFF	512K	TKIP MIC calculator registers
0xBD20_0000 – 0xBD27_FFFF	512K	Ethernet0
0xBD28_0000 – 0xBD2F_FFFF	512K	PCM
0xBD30_0000 – 0xBD3F_FFFF	1M	Ethernet1
0xBD40_0000 – 0xBD4F_FFFF	1M	WLAN controller
0xBD50_0000 – 0xBD5F_FFFF	1M	IO map address of PCI device
0xBD60_0000 – 0xBD67_FFFF	512K	Memory map address of PCI device 0, 1
0xBD68_0000 – 0xBD6F_FFFF	512K	Memory map address of PCI device 2
0xBB00_0000 – 0xBB07_FFFF	512K	Memory map address of PCI device 3
0xBD71_0000 – 0xBD71_FFFF	64K	Configuration space of PCI device0
0xBD72_0000 – 0xBD72_FFFF	64K	Configuration space of PCI device1
0xBD74_0000 – 0xBD74_FFFF	64K	Configuration space of PCI device2
0xBD78_0000 – 0xBD78_FFFF	64K	Configuration space of PCI device3

NOTE: The special function includes interrupt control, timer, watchdog, UART, and GPIO.

5. Register Mapping

The following table displays the address mapping of the all registers:

Virtual Address	Register Symbol	Register Name
Interrupt Controller		
0xBD01_0000	GIMR	Global mask register
0xBD01_0004	GISR	Global interrupt status register
Scratch Registers		
0xBD01_0040	SR0	Scratch register 0
0xBD01_0044	SR1	Scratch register 1
0xBD01_0048	SR2	Scratch register 2
0xBD01_004C	SR3	Scratch register 3
Timer		
0xBD01_0050	TCCNT	Timer/Counter control register
0xBD01_0054	TCIR	Timer/Counter interrupt register
0xBD01_0058	CBDR	Clock division base register
0xBD01_005C	WDTCNR	Watchdog timer control register
0xBD01_0060	TC0DATA	Timer/Counter 0 data register
0xBD01_0064	TC1DATA	Timer/Counter 1 data register
0xBD01_0068	TC2DATA	Timer/Counter 2 data register
0xBD01_006C	TC3DATA	Timer/Counter 3 data register
0xBD01_0070	TC0CNT	Timer/Counter 0 count register
0xBD01_0074	TC1CNT	Timer/Counter 1 count register
0xBD01_0078	TC2CNT	Timer/Counter 2 count register
0xBD01_007C	TC3CNT	Timer/Counter 3 count register
UART0		
0xBD01_00C3	UART0_RBR	UART0 receiver buffer register
0xBD01_00C3	UART0_THR	UART0 transmitter holding register
0xBD01_00C3	UART0_DLL	UART0 divisor latch LSB
0xBD01_00C7	UART0_DLM	UART0 divisor latch MSB
0xBD01_00C7	UART0_IER	UART0 interrupt enable register
0xBD01_00CB	UART0_IIR	UART0 interrupt identification register
0xBD01_00CB	UART0_FCR	UART0 FIFO control register
0xBD01_00CF	UART0_LCR	UART0 line control register
0xBD01_00D3	UART0_MCR	UART0 modem control register
0xBD01_00D7	UART0_LSR	UART0 line status register
0xBD01_00DB	UART0_MSR	UART0 modem status register
0xBD01_00DF	UART0_SCR	UART0 scratch register
UART1		
0xBD01_00E3	UART1_RBR	UART1 receiver buffer register
0xBD01_00E3	UART1_THR	UART1 transmitter holding register
0xBD01_00E3	UART1_DLL	UART1 divisor latch LSB
0xBD01_00E7	UART1_DLM	UART1 divisor latch MSB
0xBD01_00E7	UART1_IER	UART1 interrupt enable register
0xBD01_00EB	UART1_IIR	UART1 interrupt identification register
0xBD01_00EB	UART1_FCR	UART1 FIFO control register
0xBD01_00EF	UART1_LCR	UART1 line control register
0xBD01_00F3	UART1_MCR	UART1 modem control register
0xBD01_00F7	UART1_LSR	UART1 line status register
0xBD01_00FB	UART1_MSR	UART1 modem status register
0xBD01_00FF	UART1_SCR	UART1 scratch register
System Configuration register		
0xBD01_0100	BDGCR	BDG0, BDG1 and PCI bridge configuration register
0xBD01_0104	PLLMNR	DLL M ,N parameter register
0xBD01_0108	SYSCLKR	System clock setting register

0xBD01_0110	TKNR	Master token setting register
0xBD01_0114	BDGWTR	Bridge master weight setting register
0xBD01_0118	PCIWTR	PCI master weight setting register
GPIO A/B		
0xBD01_0120	GPABDATA	Port A/B data register
0xBD01_0124	GPABDIR	Port A/B direction register
0xBD01_0128	GPABIMR	Port A/B interrupt mask register
0xBD01_012C	GPABISR	Port A/B interrupt register
GPIO C/D		
0xBD01_0130	GPCDDATA	Port C/D data register
0xBD01_0134	GPCDDIR	Port C/D direction register
0xBD01_0138	GPCDIMR	Port C/D interrupt mask register
0xBD01_013C	GPCDISR	Port C/D interrupt register
GPIO E/F		
0xBD01_0140	GPEFDATA	Port E/F data register
0xBD01_0144	GPEFDIR	Port E/F direction register
0xBD01_0148	GPEFIMR	Port E/F interrupt mask register
0xBD01_014C	GPEFISR	Port E/F interrupt register
GPIO G		
0xBD01_0150	GPGDATA	Port G data register
0xBD01_0154	GPGDIR	Port G direction register
0xBD01_0158	GPGIMR	Port G interrupt mask register
0xBD01_015C	GPGISR	Port G interrupt register
Memory controller		
0xBD01_1000	MCR	Memory configuration register
0xBD01_1004	MTCR0	Memory timing configuration register 0
0xBD01_1008	MTCR1	Memory timing configuration register 1
0xBD01_100C	NCR	NAND flash Control Register
0xBD01_1010	NCAR	NAND flash Command Register
0xBD01_1014	NADDR	NAND flash Address Register
0xBD01_1018	NDR	NAND flash Data Register
IPSec Crypto Engine		
0xBD10_0000	IPSSDAR	IPSec Source Descriptor Starting Address Register
0xBD10_0004	IPSDDAR	IPSec Destination Descriptor Starting Address Register
0xBD10_0008	IPSCFR	IPSec Configuration Register
0xBD10_0009	IPSCR	IPSec Command Register
0xBD10_000A	IPSIMR	IPSec Interrupt Mast Register
0xBD10_000B	IPSISR	IPSec Interrupt Status Register
0xBD10_000C	IPSCTR	IPSec Control Register
TKIP MIC Calculator		
0xBD18_0000	MICLVAL	MIC L value Register
0xBD18_0004	MICRVAL	MIC R value Register
0xBD18_0008	MICSAR	MIC Start Address Register
0xBD18_000C	MICLENR	MIC Length Register
0xBD18_0010	MICDMAR	MIC DMA Length Register
0xBD18_0014	MICCR	MIC Control Register
0xBD18_0018	MICPSNR	MIC Pseudo Random Number Register
Ethernet0		
0xBD20_0000	ETH0_IDR	Ethernet0 ID register
0xBD20_0008	ETH0_MAR	Ethernet0 Multicast Register
0xBD20_0010	ETH0_TXOKCNT	Ethernet0 Transmit OK Counter Register
0xBD20_0012	ETH0_RXOKCNT	Ethernet0 Receive OK Counter Register
0xBD20_0014	ETH0_TXERR	Ethernet0 Transmit Error Counter Register
0xBD20_0016	ETH0_RXERR	Ethernet0 Receive Error Counter Register
0xBD20_0018	ETH0_MISSPKT	Ethernet0 Missed Packet Counter Register
0xBD20_001A	ETH0_FAE	Ethernet0 Frame Alignment Error Counter Register
0xBD20_001C	ETH0_TX1COL	Ethernet0 Transmit 1st Collision Counter Register

0xBD20_001E	ETH0_TXMCOL	Ethernet0 Transmit Multi-Collision Counter Register
0xBD20_0020	ETH0_RXOKPHY	Ethernet0 RX Physical Address Matched Register
0xBD20_0022	ETH0_RXOKBRD	Ethernet0 RX OK of Broadcast Matched Register
0xBD20_0024	ETH0_RXOKMUL	Ethernet0 RX OK of Multicast Matched Register
0xBD20_0026	ETH0_TXABT	Ethernet0 TX Abort Counter Register
0xBD20_0028	ETH0_TXUNDRN	Ethernet0 TX under-run Counter Register
0xBD20_0034	ETH0_TRSR	Ethernet0 Transmit/Receive Status Register
0xBD20_003B	ETH0_CR	Ethernet0 Command Register
0xBD20_003C	ETH0_IMR	Ethernet0 Interrupt Mask Register
0xBD20_003E	ETH0_ISR	Ethernet0 Interrupt Status Register
0xBD20_0040	ETH0_TCR	Ethernet0 Transmit Configuration Register
0xBD20_0044	ETH0_RCR	Ethernet0 Receive Configuration Register
0xBD20_0058	ETH0_MSR	Ethernet0 Media Status Register
0xBD20_005C	ETH0_MIIAR	Ethernet0 MII Access Register
0xBD20_1300	ETH0_TXFDP1	Ethernet0 TX First Descriptor 1 Register
0xBD20_1304	ETH0_TXCDO1	Ethernet0 TX Current Descriptor Offset 1 Register
0xBD20_1380	ETH0_TXFDP2	Ethernet0 TX First Descriptor 2 Register
0xBD20_1384	ETH0_TXCDO2	Ethernet0 TX Current Descriptor Offset 2 Register
0xBD20_13F0	ETH0_RXFDP	Ethernet0 RX First Descriptor Register
0xBD20_13F4	ETH0_RXCDO	Ethernet0 RX Current Descriptor Offset Register
0xBD20_13F6	ETH0_RXRINGSIZE	Ethernet0 RX Descriptor Ring Size Register
0xBD20_1430	ETH0_RXCPUDESC	Ethernet0 RX CPU's Descriptor Number Register
0xBD20_1432	ETH0_RXPSEDESC	Ethernet0 RX Descriptor Number difference Register
0xBD20_1434	ETH0_IOCMD	Ethernet0 I/O Command Register
PCM Controller		
0xBD28_0000	PCMCR	PCM interface Control Register
0xBD28_0004	PCMCHCNR	PCM Channel specific Control Register
0xBD28_0008	PCMTSR	PCM Time Slot Assignment Register
0xBD28_000C	PCMBSIZE	PCM Channels Buffer Size register
0xBD28_0010	CH0TXBSA	PCM Channel 0 TX buffer starting address pointer
0xBD28_0014	CH1TXBSA	PCM Channel 1 TX buffer starting address pointer
0xBD28_0018	CH2TXBSA	PCM Channel 2 TX buffer starting address pointer
0xBD28_001C	CH3TXBSA	PCM Channel 3 TX buffer starting address pointer
0xBD28_0020	CH0RXBSA	PCM Channel 0 RX buffer starting address pointer
0xBD28_0024	CH1RXBSA	PCM Channel 1 RX buffer starting address pointer
0xBD28_0028	CH2RXBSA	PCM Channel 2 RX buffer starting address pointer
0xBD28_002C	CH3RXBSA	PCM Channel 3 RX buffer starting address pointer
0xBD28_0030	PCMIMR	PCM channels Interrupt Mask Register
0xBD28_0034	PCMISR	PCM channels Interrupt Status Register
Ethernet1		
0xBD30_0000	ETH1_IDR	Ethernet1 ID register
0xBD30_0008	ETH1_MAR	Ethernet1 Multicast Register
0xBD30_0010	ETH1_TXOKCNT	Ethernet1 Transmit OK Counter Register
0xBD30_0012	ETH1_RXOKCNT	Ethernet1 Receive OK Counter Register
0xBD30_0014	ETH1_TXERR	Ethernet1 Transmit Error Counter Register
0xBD30_0016	ETH1_RXERR	Ethernet1 Receive Error Counter Register
0xBD30_0018	ETH1_MISSPKT	Ethernet1 Missed Packet Counter Register
0xBD30_001A	ETH1_FAE	Ethernet1 Frame Alignment Error Counter Register
0xBD30_001C	ETH1_TX1COL	Ethernet1 Transmit 1st Collision Counter Register
0xBD30_001E	ETH1_TXMCOL	Ethernet1 Transmit Multi-Collision Counter Register
0xBD30_0020	ETH1_RXOKPHY	Ethernet1 RX Physical Address Matched Register
0xBD30_0022	ETH1_RXOKBRD	Ethernet1 RX OK of Broadcast Matched Register
0xBD30_0024	ETH1_RXOKMUL	Ethernet1 RX OK of Multicast Matched Register
0xBD30_0026	ETH1_TXABT	Ethernet1 TX Abort Counter Register
0xBD30_0028	ETH1_TXUNDRN	Ethernet1 TX Underrun Counter Register
0xBD30_0034	ETH1_TRSR	Ethernet1 Transmit/Receive Status Register
0xBD30_003B	ETH1_CR	Ethernet1 Command Register

0xBD30_003C	ETH1_IMR	Ethernet1 Interrupt Mask Register
0xBD30_003E	ETH1_ISR	Ethernet1 Interrupt Status Register
0xBD30_0040	ETH1_TCR	Ethernet1 Transmit Configuration Register
0xBD30_0044	ETH1_RCR	Ethernet1 Receive Configuration Register
0xBD30_0058	ETH1_MSR	Ethernet1 Media Status Register
0xBD30_005C	ETH1_MIIAR	Ethernet1 MII Access Register
0xBD30_1300	ETH1_TXFDP1	Ethernet1 TX First Descriptor 1 Register
0xBD30_1304	ETH1_TXCDO1	Ethernet1 TX Current Descriptor Offset 1 Register
0xBD30_1380	ETH1_TXFDP2	Ethernet1 TX First Descriptor 2 Register
0xBD30_1384	ETH1_TXCDO2	Ethernet1 TX Current Descriptor Offset 2 Register
0xBD30_13F0	ETH1_RXFDP	Ethernet1 RX First Descriptor Register
0xBD30_13F4	ETH1_RXCDO	Ethernet1 RX Current Descriptor Offset Register
0xBD30_13F6	ETH1_RXRINGSIZE	Ethernet1 RX Descriptor Ring Size Register
0xBD30_1430	ETH1_RXCPUDESC	Ethernet1 RX CPU's Descriptor Number Register
0xBD30_1432	ETH1_RXPSEDESC	Ethernet1 RX Descriptor Number difference Register
0xBD30_1434	ETH1_IOCMD	Ethernet1 I/O Command Register
WLAN controller		
0xBD40_0000	WLAN_ID	WLAN ID
0xBD40_0008	WLAN_MAR	WLAN multicast register
0xBD40_0018	WLAN_TSFTR	WLAN timing synchronization function timer register
0xBD40_0020	WLAN_TLPDA	WLAN transmit low priority descriptors start address
0xBD40_0024	WLAN_TNPDA	WLAN transmit normal priority descriptors start address
0xBD40_0028	WLAN_THPDA	WLAN transmit high priority descriptors start address
0xBD40_002C	WLAN_BRSR	WLAN basic rate set register
0xBD40_002E	WLAN_BSSID	WLAN basic service set ID
0xBD40_0034	WLAN_RR	WLAN response rate
0xBD40_0035	WLAN_EIFS	WLAN EIFS register
0xBD40_0037	WLAN_CR	WLAN command register
0xBD40_003C	WLAN_IMR	WLAN interrupt mask register
0xBD40_003E	WLAN_ISR	WLAN interrupt status register
0xBD40_0040	WLAN_TCR	WLAN transmit configuration register
0xBD40_0044	WLAN_RCR	WLAN receive configuration register
0xBD40_0048	WLAN_TINT	WLAN timer interrupt register
0xBD40_004C	WLAN_TBDA	WLAN transmit beacon descriptor start address
0xBD40_0050	WLAN_CR	WLAN command register
0xBD40_0051	WLAN_CONFIG0	WLAN configuration register 0
0xBD40_0052	WLAN_CONFIG1	WLAN configuration register 1
0xBD40_0053	WLAN_CONFIG2	WLAN configuration register 2
0xBD40_0054	WLAN_ANAPARM	WLAN analog parameter
0xBD40_0058	WLAN_MSR	WLAN media status register
0xBD40_0059	WLAN_CONFIG3	WLAN configuration register 3
0xBD40_005A	WLAN_CONFIG4	WLAN configuration register 4
0xBD40_005B	WLAN_TESTR	WLAN test mode register
0xBD40_0070	WLAN_BCNITV	WLAN beacon interval register
0xBD40_0072	WLAN_ATIMWND	WLAN ATIM window register
0xBD40_0074	WLAN_BINTRITV	WLAN beacon interrupt interval register
0xBD40_0076	WLAN_ATIMTRITV	WLAN ATIM interrupt interval register
0xBD40_007C	WLAN_PHYADDR	WLAN PHY address register
0xBD40_007D	WLAN_PHYDATAW	WLAN write data to PHY
0xBD40_007E	WLAN_PHYDATAR	WLAN read data from PHY
0xBD40_0080	WLAN_RFPINOUT	WLAN RF Pins output register
0xBD40_0082	WLAN_RFPINEN	WLAN RF Pins enable register
0xBD40_0084	WLAN_RFPINSEL	WLAN RF Pins select register
0xBD40_0086	WLAN_RFPININPUT	WLAN RF Pins input register
0xBD40_0088	WLAN_RFPARA	WLAN RF parameter register
0xBD40_008C	WLAN_RFTIMING	WLAN RF timing register

0xBD40_009C	WLAN_TXAGC	WLAN auto TX AGC control
0xBD40_009D	WLAN_CCKTXAGC	WLAN auto TX AGC control for CCK
0xBD40_009E	WLAN_OFDMTXAGC	WLAN auto TX AGC control for OFDM
0xBD40_009F	WLAN_ANTSEL	WLAN TX Antenna select
0xBD40_00A0	WLAN_CAMRW	WLAN CAM (Content Access Memory) read/write register
0xBD40_00A4	WLAN_CAMOUTPUT	WLAN data written to CAM
0xBD40_00A8	WLAN_CAMINPUT	WLAN data read from DMA
0xBD40_00AC	WLAN_CAMDEBUG	WLAN CAM debug interface
0xBD40_00B0	WLAN_WPACONFIG	WLAN WPA (WiFi Protected Access) configuration register
0xBD40_00B2	WLAN_AESMASK	WLAN AES (Advanced Encryption Standard) mask register
0xBD40_00B4	WLAN_SIFS	WLAN SIFS setting register
0xBD40_00B5	WLAN_DIFS	WLAN DIFS setting register
0xBD40_00B6	WLAN_SLOTTIME	WLAN slot setting register
0xBD40_00B7	WLAN_USTUNE	WLAN micro-second fine tune register
0xBD40_00BC	WLAN_CWCONFIG	WLAN contention window config register
0xBD40_00BD	WLAN_CWVALUE	WLAN contention window value register
0xBD40_00BE	WLAN_RATECTRL	WLAN auto rate fallback control register
0xBD40_00D8	WLAN_CONFIG5	WLAN configuration register 5
0xBD40_00D9	WLAN_TPPOLL	WLAN transmit priority polling register
0xBD40_00DC	WLAN_CWR	WLAN contention window register
0xBD40_00DE	WLAN_RETRYCTR	WLAN retry count register
0xBD40_00E4	WLAN_RDSAR	WLAN receive descriptor start address register
0xBD40_0100	WLAN_DFSCR	WLAN DFS control register
0xBD40_0104	WLAN_ DFSSLR	WLAN DFS Schmitt trigger low-threshold setting register
0xBD40_0100	WLAN_DFSCR	WLAN DFS control register
0xBD40_0104	WLAN_DFSCR	WLAN DFS control register
0xBD40_0108	WLAN_DFSSHR	WLAN DFS Schmitt trigger high-threshold setting register
0xBD40_010C	WLAN_DFSDLR	WLAN DFS Pulse-duration low-threshold setting register
0xBD40_0110	WLAN_ DFSDHR	DFS Pulse-duration high-threshold setting register
0xBD40_0114	WLAN_ DFSPCR	WLAN DFS valid pulse count register
0xBD40_0118	WLAN_ DFSTS0R	WLAN DFS Time Stamp 0 register
0xBD40_011C	WLAN_ DFSTS1R	WLAN DFS Time Stamp 1 register
0xBD40_0120	WLAN_ DFSTS2R	WLAN DFS Time Stamp 2 register
0xBD40_0124	WLAN_ DFSTS3R	WLAN DFS Time Stamp 3 register
0xBD40_0128	WLAN_ DFSTS4R	WLAN DFS Time Stamp 4 register
0xBD40_012C	WLAN_ DFSTS5R	WLAN DFS Time Stamp 5 register
0xBD40_0130	WLAN_ DFSTS6R	WLAN DFS Time Stamp 6 register
0xBD40_0134	WLAN_ DFSTS7R	WLAN DFS Time Stamp 7 register
0xBD40_0138	WLAN_ DFSTS8R	WLAN DFS Time Stamp 8 register
0xBD40_013C	WLAN_ DFSTS9R	WLAN DFS Time Stamp 9 register
0xBD40_0140	WLAN_ DFSTSAR	WLAN DFS Time Stamp A register
0xBD40_0144	WLAN_ DFSTSBR	WLAN DFS Time Stamp B register
0xBD40_0148	WLAN_ DFSTSCR	WLAN DFS Time Stamp C register
0xBD40_014C	WLAN_ DFSTSDR	WLAN DFS Time Stamp D register
0xBD40_0150	WLAN_ DFSTSER	WLAN DFS Time Stamp E register
0xBD40_0154	WLAN_ DFSTSFR	WLAN DFS Time Stamp F register
0xBD40_0158	WLAN_ DFSTSGR	WLAN DFS Time Stamp G register
0xBD40_015C	WLAN_ DFSTSHR	WLAN DFS Time Stamp H register

0xBD40_0160	WLAN_DFSTSIR	WLAN DFS Time Stamp I register
0xBD40_0164	WLAN_DFSTSJR	WLAN DFS Time Stamp J register
0xBD40_0168	WLAN_DFSCTSR	WLAN DFS Current Time Stamp register

6. System Configuration

In RTL8186, several system parameters are loaded from hardware settings rather than software configuration. The signal group ICFG controls the default setting for memory width and system clock. The values of ICFG signals are strapped from GPIO pins. The mapping relationship is illustrated as following table:

ICFG Bit field	Strapping Pin Name	Default State	Function Description
0	RFLEPIN	N/A	CPU clock rate select. ICFG[3:0]. See the table below for detailed CPU and SDRAM clock setting combination.
1	CALENPIN	N/A	
2	CALMODEPIN	N/A	
3	VCOPDNPIN	N/A	
4	GPAPIN[4]	N/A	SDRAM clock synchronous/asynchronous select. 1: Synchronous (identical to system bus clock) 0: Asynchronous
5	GPAPIN[5]	1	NOR-type flash data bus width select ICFG[6:5] = 00: 8-bit data bus 01: 16-bit data bus 10: 32-bit data bus 11: Reserved
6	GPAPIN[9]	0	
7	WTXDPIN[0]	0	SDRAM clock delay parameter ICFG[8:7] = 00: No delay 01: Delay 1 unit 10: Delay 2 units 11: Delay 3 units
8	WTXDPIN[1]	0	
9	WTXDPIN[2]	0	Boot device select ICFG[9] = 0: Boot from NOR-type flash 1: Boot from NAND-type flash
10	WTXDPIN[3]	0	Function switch of PCM and WAN in 208 QFP package ICFG[10] = 0: Select WAN function at WAN pin-out in 208 QFP package 1: Select PCM function at WAN pin-out in 208 QFP package
11	SOUT0PIN	0	Function switch of I2C and UART0 in 208 QFP package ICFG[11] = 0: Select UART0 function at UART0 pin-out in 208 QFP package 1: Select I2C function at UART0 pin-out in 208 QFP package
12	MAPIN[19]	N/A	Function switch of GPIOB and UART0 ICFG[12] = 0: Select UART0 function at UART0 pin-out 1: Select GPIO B function at UART0 pin-out
13	MAPIN[20]	N/A	Function switch of GPIO C and Memory data upper 16 pins ICFG[13] = 0: Select Memory Data function at memory data pin-out 1: Select GPIO C function at memory data pin-out
14	MAPIN[21]	N/A	Function switch of GPIO D and WAN function at WAN pin-out. Notice that the WAN also has function switch with PCM, the GPIO D function is selected at WAN pin-out only when PCM function is not selected. ICFG[14] = 0: Select WAN function or PCM function at WAN pin-out 1: Select GPIO D function at WAN pin-out
15	TRSWPIN	0	Function switch of GPIO E and NAND flash control pin-out ICFG[15] = 0: Select NAND flash control function at NAND flash pin-out 1: Select GPIO E function at NAND flash pin-out
16	TRSWBPIN	1	Function switch of GPIO G and PCI AD bus pin-out ICFG[16] = 0: Select GPIO G function at PCI AD bus pin-out 1: Select PCI AD function at PCI AD bus pin-out
17	ANTSELPIN	0	JTAG function enable ICFG[17] = 0: JTAG function disabled

			1: JTAG function enabled
18	ANTSELBPIN	1	System bus grant control by external pin ICFG[18] = 0: Enable external control of system bus grant 1: Disable external control system bus grant
19	LTXDPIN[0]	N/A	External clock enable. Notice than this bit is effective only when ICFG[3:0] = 0001. ICFG[19] = 0: System clock comes from internal PLL 1: System clock comes from external pin input.
20	LTXDPIN[1]	N/A	CPU Scan test enable ICFG[20] = 0: Disable Scan test of CPU 1: Enable Scan test of CPU
21	LTXDPIN[2]	N/A	CP test enable ICFG[21] = 0: Disable CP test 1: Enable CP test
22	LTXDPIN[3]	N/A	Lexra mode CP test enable ICFG[22] = 0: Disable Lexra mode CP test 1: Enable Lexra mode CP test

The operation rate of CPU/System Bus and SDRAM is determined by the signal **ICFG[3-0]** as follows.

ICFG[3-0]	CPU/System Bus clock rate (unit: MHz)	SDRAM clock rate (unit: MHz)
0000	180	120.0
0001	195.0	130.0
0010	192.0	128.0
0011	190.0	126.7
0100	188.0	125.3
0101	186.7	124.4
0110	185.0	123.3
0111	200.0	133.3
1000	160.0	133.3
1001	152.0	126.7
1010	148.0	123.3
1011	190.0	95.0
1100	180.0	90.0
1101	123.3	123.3
1110	100.0	100.0
1111	66.7	50.0

Please note, the CPU clock will be synchronous to system bus clock.

Besides the signal group, there is a set of registers provided for software to control the internal bridge or clock module. Also there is another set of registers to control the Lexra bus arbitration.

The RTL8186 has three bridges attached to system bus, thus it will have four master devices including CPU, and which needs an arbiter for bus access arbitration. The system arbiter provides a dynamic adjustable priority. Through setting of ARB_PRIREG register, the weight of bus master device can be changed in software according to the need of different applications. The three bridges contains 9 bus masters devices, each of them are:

Bridge name	Attached Bus Master Devices
BDG0	Ethernet1, WLAN controller, PCM
BDG1	IPSec engine, TKIP-MIC engine, Ethernet0
PCI Bridge	PCI device 0,1,2,3

The bus clocks under each bridge also can be configurable through register BDGCR. Note that the clock divider at BDGCR cannot be odd number or zero.

Arbitration of each bus masters under certain bridge can be configured through corresponding bridge priority setting register. For example, setting BDG0_PRIREG can prioritize the three bus masters of bridge0. Please note, the priority weight of any

bus master cannot be zero; otherwise the master will never gain the bus grant.

These system-configuration related registers are defined as follow:

Register Summary

Virtual address	Size (byte)	Name	Description
0xBD01_0100	4	BDGCR	BDG0, BDG1 and PCI bridge configuration register
0xBD01_0104	4	PLLMNR	RTL8186 DPLL M, N parameter register
0xBD01_0108	4	SYSCLKR	RTL8186 System clock setting register
0xBD01_0110	4	TKNR	RTL8186 master token setting register
0xBD01_0114	4	BDGWTR	RTL8186 bridge weight setting register
0xBD01_0118	4	PCIWTR	RTL8186 PCI bridge weight setting register

0xBD01_0100 **Bridge Configuration Register (BDGCR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																				PDIV				B1DIV				B0DIV			

Reset: 0x0000_0511

Bit	Bit Name	Description	R/W	InitVal
11-8	PDIV	Bus clock to PCI Bridge clock ratio. 0001= 2:1, 0011= 4:1, 0101= 6:1, 0111= 8:1, Other values are reserved.	R/W	0101
7-4	B1DIV	Bus clock to Bridge1 clock ratio. 0001= 2:1, 0011= 4:1, 0101= 6:1, 0111= 8:1, Other values are reserved.	R/W	0001
3-0	B0DIV	Bus clock to Bridge0 clock ratio. 0001= 2:1, 0011= 4:1, 0101= 6:1, 0111= 8:1, Other values are reserved.	R/W	0001

0xBD01_0104 **DPLL M,N parameter Register (PLLMNR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)														ARBWS		RSVD	MNEN	MDIV						RSVD				NDIV			

Reset: 0x0003_1703

Bit	Bit Name	Description	R/W	InitVal
17-16	ARBWS	Arbiter Wait Parameter Setting.	R/W	11
14	MNEN	MDIV and NDIV write enable, 0: disable, 1: enable.	R/W	0
13-8	MDIV	DPLL M parameter	R/W	010111
4-0	NDIV	DPLL N parameter	R/W	00011

Note: The equation of DPLL clock rate is: 40MHz*(M+1)/(N+1)

0xBD01_0108 **System Clock Setting Register (SYSCLKR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								PCIIOS								CPUEN		RSVD		CPUS				MEMEN		RSVD			MEMS		

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
23-22	PCIIOS	PCI IO map control register. 00 – use PCI IO map for 16 bits 11 – use PCI IO map for 32 bits	R/W	00
15	CPUEN	Write enable control for CPU setting register.	R/W	0
11-8	CPUS	CPU setting register	R/W	0000
7	MEMEN	Write enable control for memory setting register	R/W	0
3-0	MEMS	Memory setting register	R/W	0000

The relation among CPUS/MEMS value, CPU/System-bus clock, SDRAM timing and signal **ICFG[3-0]** are defined as follows.

ICFG[3-0]	CPUS	MEMS	CPU/System Bus clock rate (unit: MHz)	SDRAM clock rate (unit: MHz)
0000	2	4	200.0	133.3
0001	2	4	200.0	133.3
0010	2	5	200.0	100.0
0011	2	5	200.0	160.0
0100	3	5	200.0	125.0
0101	2	4	220.0	146.7
0110	2	4	213.3	142.2
0111	2	5	213.3	106.7
1000	2	4	192.0	128.0
1001	1	3	192.0	115.2
1010	2	5	190.0	95.0
1011	2	4	180.0	120.0
1100	1	4	180.0	90.0
1101	5	5	100.0	100.0
1110	4	6	100.0	50.0
1111	4	6	66.7	33.3

0xBD01_0110 **Master Token Register (TKNR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPUTKN								BDG0TKN								BDG1TKN								PCIBTKN							

Reset: 0x0F01_0101

Bit	Bit Name	Description	R/W	InitVal
31-24	CPUTKN	CPU Token setting	R/W	00001111
23-16	BDG0TKN	BDG0 Token setting	R/W	00000001
15-8	BDG1TKN	BDG1 Token setting	R/W	00000001
7-0	PCIBTKN	PCI Bridge Token setting	R/W	00000001

0xBD01_0114 **Bridge Weight Setting Register (BDGWTR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

B1R3	B1R2	B1R1	B1R0	B0R3	B0R2	B0R1	B0R0

Reset: 0x1111_1111

Bit	Bit Name	Description	R/W	InitVal
31-28	B1R3	BDG1 Master 3 request weight setting	R/W	0001
27-24	B1R2	BDG1 Master 2 request weight setting	R/W	0001
23-20	B1R1	BDG1 Master 1 request weight setting	R/W	0001
19-16	B1R0	BDG1 Master 0 request weight setting	R/W	0001
15-12	B0R3	BDG0 Master 3 request weight setting	R/W	0001
11-8	B0R2	BDG0 Master 2 request weight setting	R/W	0001
7-4	B0R1	BDG0 Master 1 request weight setting	R/W	0001
3-0	B0R0	BDG0 Master 0 request weight setting	R/W	0001

0xBD01_0118 **PCI Master Weight Setting Register (PCIWTR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																PBR3				PBR2				PBR1				PBR0			

Reset: 0x0000_2222

Bit	Bit Name	Description	R/W	InitVal
15-12	PBR3	PCI Bridge Master 3 request weight setting	R/W	0001
11-8	PBR2	PCI Bridge Master 2 request weight setting	R/W	0001
7-4	PBR1	PCI Bridge Master 1 request weight setting	R/W	0001
3-0	PBR0	PCI Bridge Master 0 request weight setting	R/W	0001

7. Interrupt Controller

The RTL8186 provides six internal hardware-interrupt inputs (IRQ0-IRQ5). Some devices share the same IRQ signal. The following table displays the IRQ map used by devices.

IRQ Number	Interrupt Source
0	Timer/Counter interrupt.
1	GPIO/LBC interrupt.
2	WLAN interrupt.
3	UART/PCI interrupt.
4	Ethernet0 interrupt.
5	Ethernet1/MIC/IPSEC interrupt.

When any one of above IRQ is happened, RTL8186 will assert the corresponding bit in CPU coprocessor cause and status register. Besides, it has two additional registers for the interrupt control. The **GIMR** register can enable/disable the peripheral interrupt source. The **GISR** shows the pending peripheral interrupt status.

Register Summary

Virtual address	Size (byte)	Name	Description
0xBD01_0000	2	GIMR	Global interrupt mask register
0xBD01_0004	2	GISR	Global interrupt status register

0xBD01_0000 **Global Interrupt Mask Register (GIMR)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)							MICIE	IPSIE	LBCIE	PCMIE	PCIIE	ETH1IE	ETH0IE	UARTIE	WLANIE	GPIOIE	TCIE

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
10	MICIE	MIC calculator interrupt enable. 0: Disable, 1: Enable	R/W	0
9	IPSIE	IPSec engine interrupt enable. 0: Disable, 1: Enable	R/W	0
8	LBC1E	LBC time-out interrupt enable. 0: Disable, 1: Enable	R/W	0
7	PCMIE	PCM interrupt enable. 0: Disable, 1: Enable	R/W	0
6	PCIIE	PCI interrupt enable. 0: Disable, 1: Enable	R/W	0
5	ETH1IE	Ethernet1 interrupt enable. 0: Disable, 1: Enable	R/W	0
4	ETH0IE	Ethernet0 interrupt enable. 0: Disable, 1: Enable	R/W	0
3	UARTIE	UART interrupt enable. 0: Disable 1: Enable	R/W	0
2	WLANIE	WLAN controller interrupt enable. 0: Disable, 1: Enable	R/W	0
1	GPIOIE	GPIO interrupt enable. 0: Disable, 1: Enable	R/W	0
0	TCIE	Timers/Counters interrupt enable. 0: Disable, 1: Enable	R/W	0

0xBD01_0004 **Global Interrupt Status Register (GISR)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)							MICIP	IPSIP	LBCIP	PCMIP	PCIIP	ETH1IP	ETH0IP	UARTIP	WLANIP	GPIOIP	TCIP

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
10	MICIP	MIC calculator interrupt pending flag. 0: no pending, 1: pending	R	0
9	IPSIP	IPSec engine interrupt pending flag. 0: no pending, 1: pending	R	0
8	LBCIP	LBC time-out interrupt pending flag. 0: no pending, 1: pending	R	0
7	PCMIP	PCM interrupt pending flag. 0: no pending, 1: pending	R	0
6	PCIIP	PCI interrupt pending flag. 0: no pending, 1: pending	R	0
5	ETH1IP	Ethernet1 interrupt pending flag. 0: no pending, 1: pending	R	0
4	ETH0IP	Ethernet0 interrupt pending flag.	R	0

		0: no pending, 1: pending		
3	UARTIP	UARTI interrupt pending flag. 0: no pending, 1: pending	R	0
2	WLANIP	WLAN controller interrupt pending flag. 0: no pending, 1: pending	R	0
1	GPIOIP	GPIO interrupt pending flag. 0: no pending, 1: pending	R	0
0	TCIP	Timers/Counters interrupt pending flag. 0: no pending, 1: pending	R	0

8. Memory Controller

RTL8186 integrates a memory control module to access external SDRAM and flash memory.

The interface is designed to PC100 or PC133-compliant SDRAM, supports auto-refresh mode, which requires 4096 refresh cycle within 64 ms. The SDRAM interface supports two chips (CS0#, and CS1#), and the SDRAM size and timing is configurable in registers. The data width of SDRAM could be chosen as 16-bit or 32-bit in register as well. If 32-bit is configured, 2 16-bit SDRAM chips may be used to expand the data bus width to 32 bits or use one 32-bit SDRAM chip is allowable.

Besides, RTL8186 could also supports two flash memory chips (F_CS0# and F_CS1#). The interface could support only 16-bit NOR-type flash memory. Another flash memory type, NAND flash, is also support by this interface. The system can be configured to boot from NOR type flash or NAND. When NOR type is used, the system will boot from KSEG1 at virtual address 0xBFC0_0000 (physical address: 0x1FC0_0000). Chip1 flash memory will be mapped to the address "0x1FC0_000 + flash size". The flash size is configurable from 1M to 8M bytes for each chip. If flash size set to 4M or 8M the 0xBFC0_0000 still map the first 4M bytes of flash. There will have a new memory mapping from 0xBE00_0000. The 0xBE00_0000 mapped to the chip0 byte 0.

If NAND type flash is selected in signal group ICFG[9], the memory controller will move first block of NAND flash (16K byte long) to SDRAM at virtual address 0x8000_00000, and then it will run the system software from there. The first 3rd and 4th bytes of the image will be referred for SDRAM configuration setting, please refer the paragraph 'NAND flash layout' below for detail.

Register Summary

Virtual address	Size (byte)	Name	Description
0xBD01_1000	4	MCR	Memory Configuration Register
0xBD01_1004	4	MTCR0	Memory Timing Configuration Register 0
0xBD01_1008	4	MTCR1	Memory Timing Configuration Register 1
0xBD01_100C	4	NCR	NAND Flash Control Register
0xBD01_1010	4	NCAR	NAND Flash Command Register
0xBD01_1014	4	NADDR	NAND Flash Address Register
0xBD01_1018	4	NDR	NAND Flash Data Register

Note: These registers should be accessed in double word.

0xBD01_1000 **Memory Configuration Register (MCR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSIZE		SDRSIZE		CASL	RSVD						SDBUSWID	MCK2LCK	BUSCLK			(Reserved)															

Reset: 0xB290_0000

Bit	Bit Name	Description	R/W	InitVal
31-30	FLSIZE	Flash size respective to one bank (byte). 00: 1M 01: 2M 10: 4M 11: 8M	R/W	11
29-28	SDRSIZE	SDRAM size respective to one bank (bit). 00: 512Kx16x2 01: 1Mx16x4 10: 2Mx16x4 11: 4Mx16x4	R/W	01
27	CASL	CAS Latency 0: Latency=2 1: Latency=3	R/W	0
26-25	NORFLASH_0	Bus width of NOR flash 0. 00: 8 bit 01: 16 bit 10: 32 bit 11: N/A	R	
24-23	NORFLASH_1	Bus width of NOR flash 1. 00: 8 bit 01: 16 bit 10: 32 bit 11: N/A	R/W	
22-21	RSVD	Reserved	R	0
20	SDBUSWID	SDRAM bus width 0: 16 bit 1: 32 bit	R/W	1
19	MCK2LCK	SDRAM clock synchronous/asynchronous select. 1: Synchronous (identical to system bus clock) 0: Asynchronous	R	
18-16	BUSCLK	Bus Clock to control auto-refresh timing 000: 200 MHz 001: 100 MHz 010: 50 MHz 011: 25 MHz 100: 12.5 MHz 101: 6.25 MHz 110: 3.125 MHz 111: 1.5625 MHz	R/W	000
15-0	Reserved	Must be set to bit value 00.	R/W	00

0xBD01_1004 **Memory Timing Configuration Register 0 (MTCR0)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CE0T_CS				CE0T_WP				CE1T_CS				CE1T_WP				EXCS0T_CS				EXCS0T_WP				(Reserved)							

Reset: 0xFFFF_FF00

Bit	Bit Name	Description	R/W	InitVal
31-28	CE0T_CS	The timing interval between F_CE0# to WR# Basic unit, 2*clock cycle	R/W	1111

		"0000" means 1 unit (2 clock cycles)		
27-24	CE0T_WP	The timing interval for WR# to be pulled-low Basic unit, 2*clock cycle "0000" means 1 unit (2 clock cycles)	R/W	1111
23-20	CE1T_CS	The timing interval between F_CE1# to WR# Basic unit, 2*clock cycle "0000" means 1 unit (2 clock cycles)	R/W	1111
19-16	CE1T_WP	The timing interval for WR# to be pulled-low Basic unit, 2*clock cycle "0000" means 1 unit (2 clock cycles)	R/W	1111
15-12	EXCS0T_CS	The timing interval between EXT_CE0# to WR# Basic unit, 2*clock cycle "0000" means 1 unit (2 clock cycles)	R/W	1111
11-8	EXCS0T_WP	The timing interval for WR# to be pulled-low Basic unit, 2*clock cycle "0000" means 1 unit (2 clock cycles)	R/W	1111

Note: The clock cycle is based on memory clock.

0xBD01_1008 **Memory Timing Configuration Register 1 (MTCR1)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																			CE23T_RP (T_RCD)			CE23T_RAS					CE23T_RFC			

Reset: 0x0000_1FFF

Bit	Bit Name	Description	R/W	InitVal
12-10	CE23T_RP (T_RCD)	T_RP and T_RCD timing parameter Basic unit, 1*clock cycle "000" means 1 unit (1 clock cycle) Only "001" and "010" are valid for correct operation.	R/W	111
9-5	CE23T_RAS	T_RAS timing parameter Basic unit, 1*clock cycle "0000" means 1 unit (1 clock cycle)	R/W	11111
4-0	CE23T_RFC	T_RFC timing parameter for refresh interval Basic unit, 1*clock cycle "0000" means 1 unit (1 clock cycle)	R/W	11111

Note: The clock cycle is based on memory clock.

0xBD01_100C **NAND Flash Control Register (NCR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NFRB	RSVD	RBS	WBS	(Reserved)				CE_TWP				CE_TWB				CE_TRR				CE_TREA				CE_TH				CE_TS			

Reset: 0xB0FF_FFFF

Bit	Bit Name	Description	R/W	InitVal
31	NFRB	Nand flash Ready/Busy status indication bit 0: Busy 1: Ready	R	1
30	RSVD	Reserved	R	0
29	RBS	Read Byte Swapping. 0: The byte order of NDR register read is {0, 1, 2, 3} 1: The byte order of NDR register read is {3, 2, 1, 0}	R/W	1
28	WBS	Write Byte Swapping.	R/W	1

		0: The byte order of NDR register write is {0, 1, 2, 3} 1: The byte order of NDR register write is {3, 2, 1, 0}		
23-20	CE_TWP	Write pulse width. Base unit: 1 * clock cycle	R/W	1111
19-16	CE_TWB	WE high to busy. Base unit: 1 * clock cycle	R/W	1111
15-12	CE_TRR	Ready to RE falling edge. Base unit: 1 * clock cycle	R/W	1111
11-8	CE_TREA	RE access time. Base unit: 1 * clock cycle	R/W	1111
7-4	CE_TH	CLE, CE, ALE, DATA and WE hold time. Base unit: 1* clock cycle	R/W	1111
3-0	CE_TS	CLE, CE, ALE and DATA setup time. Base unit: 1 * clock cycle	R/W	1111

0xBD01_1010 **NAND Flash Command Register (NCAR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CECS4	CECS5	(Reserved)																						CE_CMD							

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31	CECS4	Command enable to CS4 connected NAND flash ‘1’: Command Enable ‘0’: No command enabled	W	1
30	CECS5	Command enable to CS5 connected NAND flash ‘1’: Command Enable ‘0’: No command enabled	W	0
7-0	CE_CMD	Command port to NAND flash memory	W	0

0xBD01_1014 **NAND Flash Address Register (NADDR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)					AD2EN	AD1EN	AD0EN	CE_ADD2								CE_ADD1								CE_ADDR0							

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
26	AD2EN	Address port 2 enable ‘1’: Address port 2 is valid to output to NAND flash ‘0’: Address port 2 is not output to NAND flash	W	0
25	AD1EN	Address port 1 enable ‘1’: Address port 1 is valid to output to NAND flash ‘0’: Address port 1 is not output to NAND flash	W	0
24	AD0EN	Address port 0 enable ‘1’: Address port 0 is valid to output to NAND flash ‘0’: Address port 0 is not output to NAND flash	W	0
23-16	CE_ADDR2	Address2 port to NAND flash memory.	W	0
15-8	CE_ADDR1	Address1 port to NAND flash memory.	W	0
7-0	CE_ADDR0	Address0 port to NAND flash memory.	W	0

0xBD01_1018 **NAND Flash Data Register (NDR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

DATA3	DATA2	DATA1	DATA0

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-24	DATA3	NAND flash DATA0 port. Read/Write this field during data phase will reflects to external NAND flash I/O ports. When bit RBS or bit WBS in NCR register is '1', this data byte is the highest address of the register word. Else this byte is the lowest address byte of the register word.	R/W	0
23-16	DATA2	NAND flash DATA1 port. Read/Write this field during data phase will reflects to external NAND flash I/O ports. When bit RBS or bit WBS in NCR register is '1', this data byte is the 3rd address of the register word. Else this byte is the 2nd address byte of the register word.	R/W	0
15-8	DATA1	NAND flash DATA1 port. Read/Write this field during data phase will reflects to external NAND flash I/O ports. When bit RBS or bit WBS in NCR register is '1', this data byte is the 2nd address of the register word. Else this byte is the 3rd address byte of the register word.	R/W	0
7-0	DATA0	NAND flash DATA0 port. Read/Write this field during data phase will reflects to external NAND flash I/O ports. When bit RBS or bit WBS in NCR register is '1', this data byte is the lowest address of the register word. Else this byte is the highest address byte of the register word.	R/W	0

NAND flash layout

Address 0x0 – 0x1	**Address 0x2 – 0x3**	**Address 0x4 - …**	**…**	**Address 0x4000**	**Address 0x4001**		**Address End**
NAND flash Header					**Data**		
NAND flash boot image							

NAND flash header format

Byte Address 3								Byte Address 2								Byte Address 1								Byte Address 0							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
SDRSZ		CASL	SDBUSWID					T_RCD				T_RAS				T_RFC								OPCODE							

Byte Address 3

Bit	Bit Name	Description	R/W	InitVal
7-6	SDRSZ	SDRAM size respective to one bank (bit). 00: 512Kx16x2 01: 1Mx16x4 10: 2Mx16x4 11: Reserved	R/W	10
5	CASL	CAS Latency	R/W	0

		0: Latency=2 1: Latency=3		
4	SDBUSWID	SDRAM bus width 0: 16 bit 1: 32 bit	R/W	0
3-1	BUSCLK	Bus Clock to control auto-refresh timing 000: 200 MHz 001: 100 MHz 010: 50 MHz 011: 25 MHz 100: 12.5 MHz 101: 6.25 MHz 110: 3.125 MHz 111: 1.5625 MHz	R/W	000
0	T_RCD	Combined with 1st field of next table.		

Byte Address 2

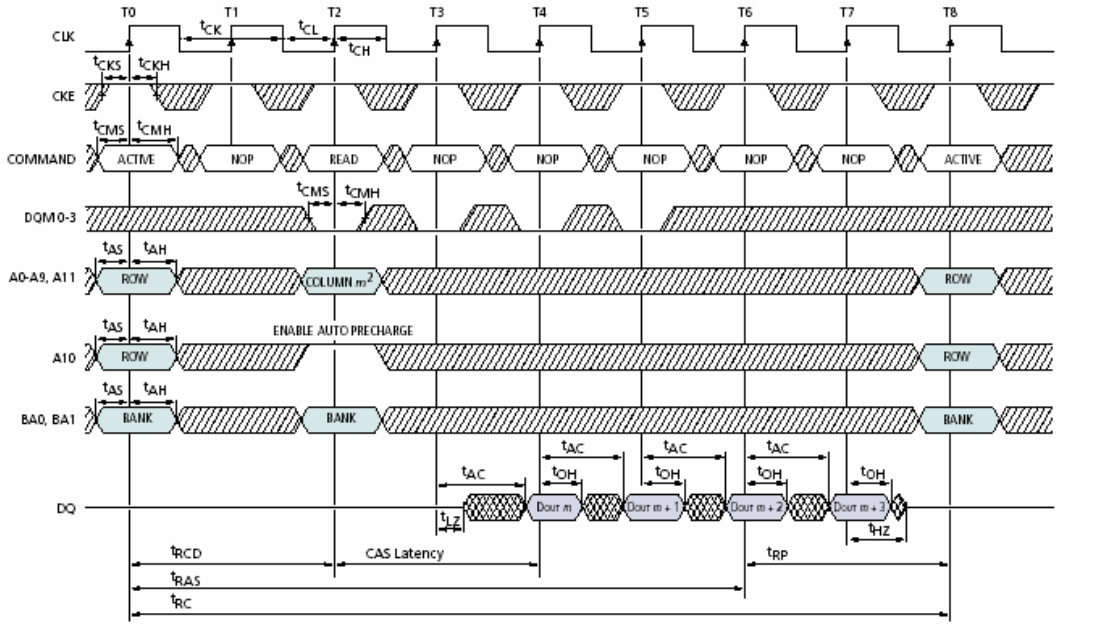
Bit	Bit Name	Description	R/W	InitVal
0-7-6	T_RCD	T_RP and T_RCD timing parameter Basic unit, 4*clock cycle "000" means 1 unit (4 clock cycle)	R/W	111
5-3	T_RAS	T_RAS timing parameter Basic unit, 4*clock cycle "000" means 1 unit (4 clock cycle)	R/W	111
2-0	T_RFC	T_RFC timing parameter for refresh interval Basic unit, 4*clock cycle "000" means 1 unit (4 clock cycle)	R/W	111

Byte Address 1-0

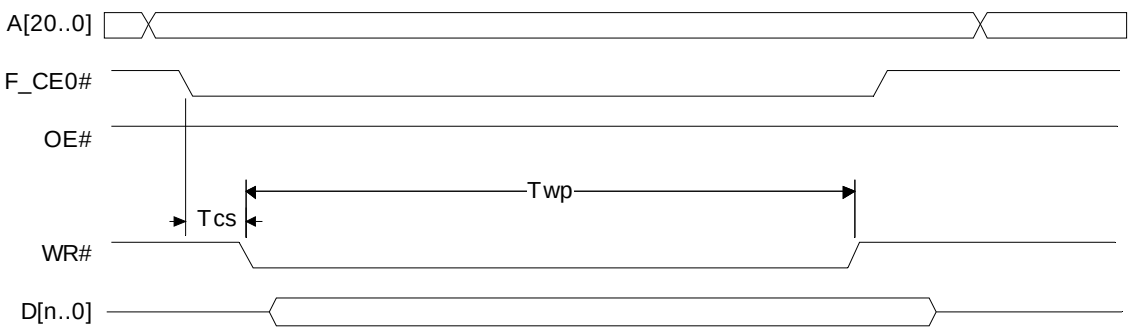
Bit	Bit Name	Description	R/W	InitVal
7-0	OPCODE	The OPCODE of first instruction in big endian format.	R/W	x

Timing Diagram

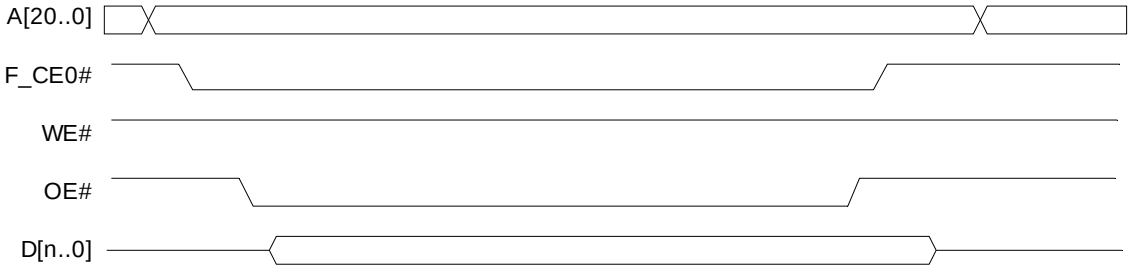
The SDRAM timing:



The write access timing of flash memory:



The read access timing of flash memory:



9. Ethernet Network Interface Controller

There are two 10/100M Ethernet NIC modules embedded in RTL8186. The Ethernet device has bus master capability and moves packets between SDRAM and the Ethernet controller through a DMA mechanism, lessening the CPU loading and giving better performance. Both the Ethernet controller support the following feature:

- Supports 10/100 Full/Half (collision) Flow control (control frame transmission).
- Supports IEEE802.1P/Q VLAN handling.
- TCP, UDP, IP receiving checksum offload
- Hardware Priority queue with one receive descriptor ring and two transmit descriptor rings.
- Unicast Address Recognition.

The Ethernet controller supports up to 64 consecutive descriptors for transmit and receive separately. Besides, it includes 3 descriptor rings, one high priority transmit ring, one normal priority transmit ring and the other is for receive descriptor ring. Each descriptor ring may consist of up to 64 consecutive descriptors, and each descriptor is consisted of 4 consecutive words. The starting address of each descriptor group should be 256-byte alignment. Software must pre-allocate enough buffers and configures all descriptor rings before transmitting and/or receiving packets. Descriptors can be chained for both transmitting and receiving packet. Any transmit buffer pointed by one of transmit descriptor should be at least 4 bytes. And for transmit packet padding; the Ethernet controller will automatically pad any packet less than 64 bytes (including 4 bytes CRC) to 64-byte long (including 4-byte CRC) before transmitting that packet into network medium.

Also the Ethernet controller offloads the calculation of IP/TCP/UDP checksum at the receiving path FIFO. The packet parser insides the controller can identify:

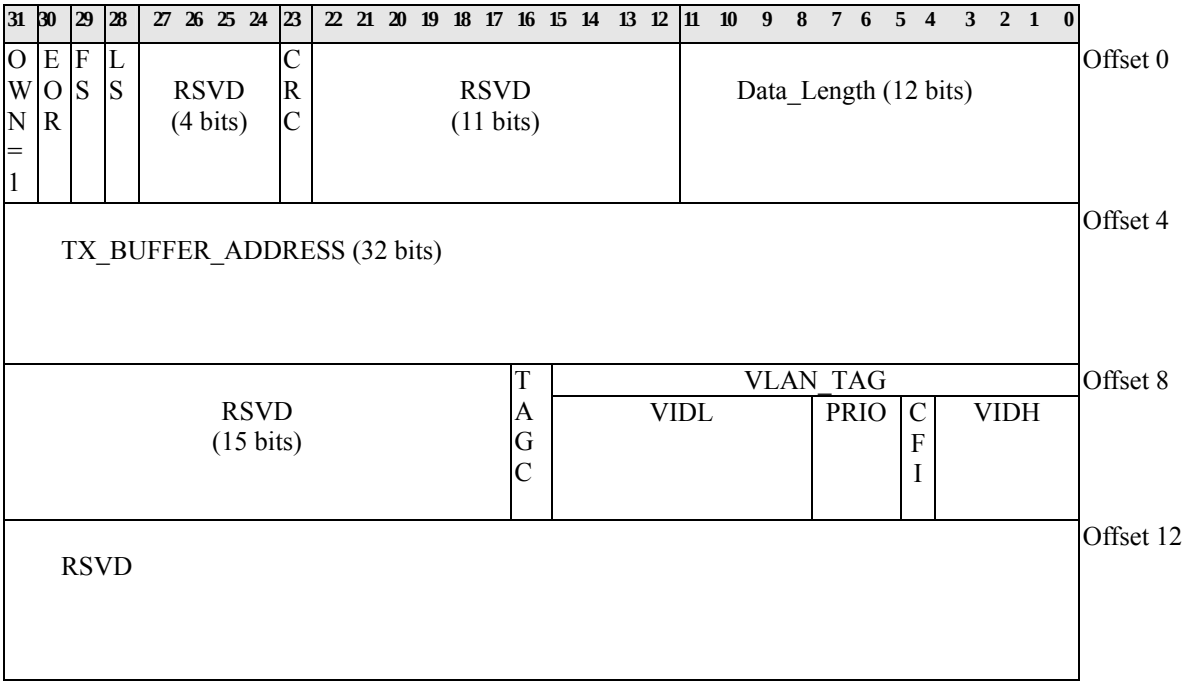
- 802.3 Ethernet packets
- RFC894 Ethernet II packets
- PPPOE packets
- VLAN packets

Inside the IP payload, the packet parser determines whether the packet is TCP/UDP or neither of the two. For TCP/UDP checksum, the IP pseudo header must be included in the checksum one's complement summation. The Ethernet NIC also identifies fragmented packets and handles TCP/UDP checksum by performing one's complement summation per IP packet, recording the sum/packet in the last descriptor and reporting fragmentation on status descriptor. For non-fragmented packets, Ethernet NIC module checks the calculated TCP/UDP checksum and reports the status in the descriptor.

Descriptor Data Structure

The descriptors in the queuing rings serve to exchange messages between CPU and the Ethernet Controller. A transmit descriptor changes form before and after transmit. Also the receive descriptor changes form before and after receive. The descriptor data structures are illustrated as follow:

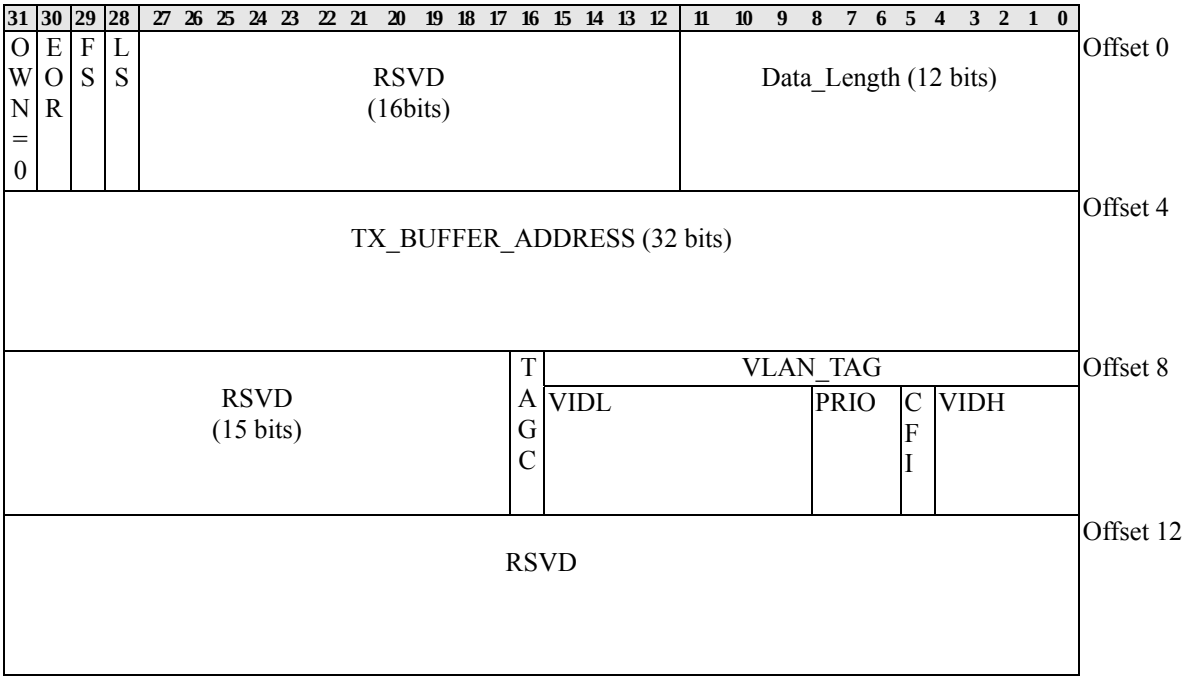
■ Normal Tx Descriptor Format (before transmitting, OWN=1, Tx command mode 1)



Offset#	Bit#	Symbol	Description
0	31	OWN	When set, indicates that the descriptor is owned by NIC, and the data relative to this descriptor is ready to be transmitted. When cleared, indicates that the descriptor is owned by host system. NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1. **Value** / **Meaning** 0 / Descriptor own by host system 1 / Descriptor own by NIC
0	30	EOR	End of descriptor Ring. When set, indicates that this is the last descriptor in descriptor ring. When NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data associates with this descriptor.
0	29	FS	First segment descriptor. When set, indicates that this is the first descriptor of a segmented Tx packet, and this descriptor is pointing to the first segment of the packet.
0	28	LS	Last segment descriptor. When set, indicates that this is the last descriptor of a segmented Tx packet, and this descriptor is pointing to the last segment of the packet.
0	27-24	RSVD	Reserved bits.

0	23	CRC	If this bit is set then append CRC at the end of Ethernet frame. **Value** / **Meaning** 0 – No CRC appended 1 – CRC appended
0	22-12	RSVD	Reserved bits.
0	11-0	Frame_Length	Transmit frame length. This field indicates the length in TX buffer page, in byte, to be transmitted
4	31-0	TxBuff	Physical 32-bit address of transmit buffer.
8	31-17	RSVD	Reserved bits.
8	16	TAGC	VLAN tag control bit. 1: Enable. 0: Disable. **Value** / **Meaning** 0 – Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as upper layer passed it down. 1 – Insert TAG 0x8100 (Ethernet encoded tag protocol ID) after source address, indicating that this is a IEEE 802.1Q VLAN packet. And 2 bytes are inserted after the TAG that copied from VLAN_TAG field in Tx descriptor.
8	15-0	VLAN_TAG	The 2-byte VLAN_TAG contains information, from upper layer, of user priority, canoethernetal format indicator, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canoethernetal Format Indicator.
12	31-0	RSVD	Reserved

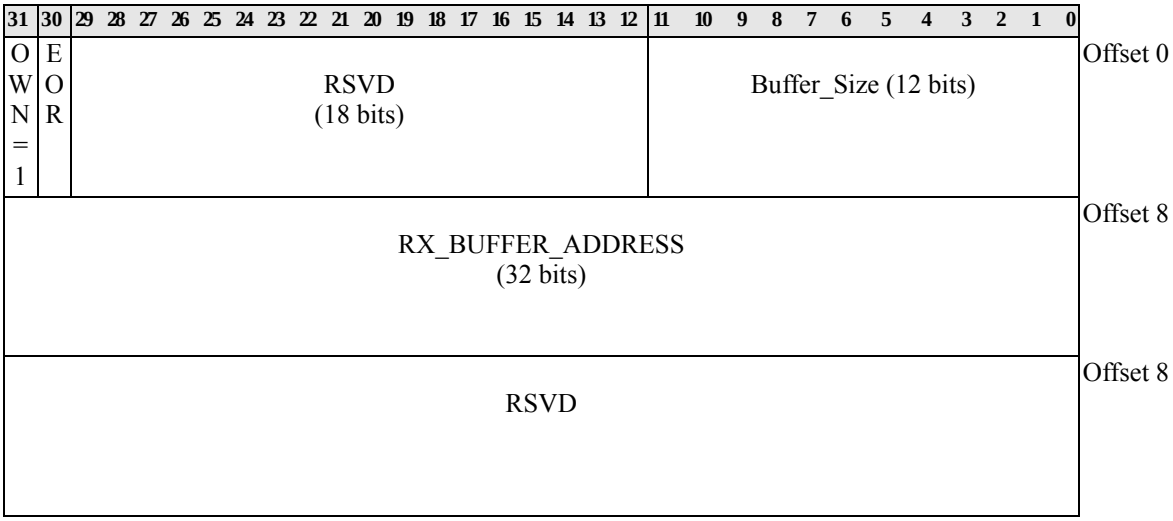
■ Tx Status Descriptor (after transmitting, OWN=0, Tx status mode)



Offset#	Bit#	Symbol	Description
0	31	OWN	When set, indicates that the descriptor is owned by NIC. When clear

			indicates that the descriptor is owned by host system. NIC clears this bit when the relative buffer data is already transmitted. In this case, OWN=0. **Value** / **Meaning** 0 / Descriptor own by host system 1 / Descriptor own by NIC
0	30	EOR	End of descriptor Ring. When set, indicates that this is the last descriptor in descriptor ring. When NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data associates with this descriptor.
0	29	FS	First segment descriptor. When set, indicates that this is the first descriptor of a segmented Tx packet, and this descriptor is pointing to the first segment of the packet.
0	28	LS	Last segment descriptor. When set, indicates that this is the last descriptor of a segmented Tx packet, and this descriptor is pointing to the last segment of the packet.
0	27-12	RSVD	Reserved.
0	11-0	Data_Length	Transmit data length. This field indicates the length in TX buffer page, in byte, transmitted
4	31-0	TxBuff	The physical 32-bit address of transmit buffer.
8	31-17	RSVD	Reserved bits.
8	16	TAGC	Record of previous VLAN information: VLAN tag control bit. 1: Tag was inserted. 0: Tag was not inserted
8	15-0	VLAN_TAG	Record of previous VLAN information: The 2-byte VLAN_TAG contains information, from upper layer, of user priority, canoethernetal format indicator, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canoethernetal Format Indicator.
12	31-0	RSVD	Reserved

■ Rx Command Descriptor (OWN=1)



RSVD	Offset 12

Offset#	Bit#	Symbol	Description
0	31	OWN	When set, indicates that the descriptor is owned by NIC, and is ready to receive packet. The OWN bit is set by driver after having pre-allocated buffer at initialization, or the host has released the buffer to driver. In this case, OWN=1. **Value** / **Meaning** 0 – Descriptor own by host system 1 – Descriptor own by NIC
0	30	EOR	End of Rx descriptor Ring. Set to 1 indicates that this descriptor is the last descriptor of Rx descriptor ring. Once NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of Rx descriptor ring after this descriptor is used by packet reception.
0	29-12	RSVD	Reserved bits.
0	11-0	Buffer_Size	This field indicate the receive buffer size in bytes. The NIC purges all data after 4K bytes if the packet is larger than 4K-byte long.
4	31-0	Rx_Buff_addr	The 32-bit physical address of receive buffer.
8	31-0	RSVD	Reserved bits.
12	31-0	RSVD	Reserved bits.

■ Rx Status Descriptor (OWN=0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10 9 8 7 6 5 4 3 2 1 0	
OWN=0	EOR	FS	LS	FAE	MAR	PAM	BAR	PPPOE	E802.3	LPKT	RES	RUNT	CRC	PID1	PID0	IPF	UDPF	TCPF	IPSEG	RSVD	Data_Length (11 bits)	Offset 0
RX_BUFFER_ADDRESS (32 bits)																						Offset 8
OFFST	FRAG	RSVD (13 bits)											TAVA	VLAN_TAG								Offset 8
														VIDL (8 bits)				PRIO (3 bits)	CFI	VIDH (4 bits)		
RSVD (16 bits)														PARTIAL_CHECKSUM (16 bits)								Offset 12

Offset#	Bit#	Symbol	Description
0	31	OWN	When set, indicates that the descriptor is owned by NIC. When cleared, indicates that the descriptor is owned by host system. NIC clears this bit when NIC has filled up this Rx buffer with a packet or part of a packet. In

<table>
<tr><td></td><td></td><td></td><td>this case, OWN=0.
<table><tr><th>Value</th><th>Meaning</th></tr><tr><td>0</td><td>Descriptor own by host system</td></tr><tr><td>1</td><td>Descriptor own by NIC</td></tr></table></td></tr>
<tr><td>0</td><td>30</td><td>EOR</td><td>End of Rx descriptor Ring. Set to 1 indicates that this descriptor is the last descriptor of Rx descriptor ring. Once NIC’s internal receive descriptor pointer reaches here, it will return to the first descriptor of Rx descriptor ring after this descriptor is used by packet reception.</td></tr>
<tr><td>0</td><td>29</td><td>FS</td><td>First segment descriptor. When set, indicates that this is the first descriptor of a received packet, and this descriptor is pointing to the first segment of the packet.</td></tr>
<tr><td>0</td><td>28</td><td>LS</td><td>Last segment descriptor. When set, indicates that this is the last descriptor of a received packet, and this descriptor is pointing to the last segment of the packet.</td></tr>
<tr><td>0</td><td>27</td><td>FAE</td><td>Frame Alignment Error. When set, indicates a frame alignment error has occurred on the received packet. The FAE packet can be received only when AER bit at RCR register is set.</td></tr>
<tr><td>0</td><td>26</td><td>MAR</td><td>Multicast Address packet Received. When set, indicates that a multicast packet is received</td></tr>
<tr><td>0</td><td>25</td><td>PAM</td><td>Physical Address Matched. When set, indicates that the destination address of this Rx packet matches to the value in Ethernet’s ID registers. Use to address packets to gateway.</td></tr>
<tr><td>0</td><td>24</td><td>BAR</td><td>Broadcast Address Received. When set, indicates that a broadcast packet is received. BAR and MAR will not be set simultaneously.</td></tr>
<tr><td>0</td><td>23</td><td>PPPOE</td><td>Identifies if current packet is PPPOE packet</td></tr>
<tr><td>0</td><td>22</td><td>E802.3</td><td>Identifies if current packet is of Ethernet 802.3 format</td></tr>
<tr><td>0</td><td>21</td><td>RWT</td><td>Receive Watchdog Timer expired. When set, indicates that the received packet length exceeds 4096 bytes, the receive watchdog timer will expire and stop receive engine.</td></tr>
<tr><td>0</td><td>20</td><td>RES</td><td>Receive Error Summary. When set, indicates at least one of the following errors occurred: CRC, RUNT, RWT, FAE. This bit is valid only when LS (Last segment bit) is set</td></tr>
<tr><td>0</td><td>19</td><td>RUNT</td><td>Runt packet. When set, indicates that the received packet length is smaller than 64 bytes. RUNT packet can be received only when AR bit at RCR register is set.</td></tr>
<tr><td>0</td><td>18</td><td>CRC</td><td>CRC error. When set, indicates that a CRC error has occurred on the received packet. A CRC packet can be received only when AER bit at RCR register is set.</td></tr>
<tr><td>0</td><td>17, 16</td><td>PID1, PID0</td><td>Protocol ID1, Protocol ID0: These 2 bits indicate the protocol type of the packet received.
<table><tr><td></td><td>PID1</td><td>PID0</td></tr><tr><td>Non-IP</td><td>0</td><td>0</td></tr><tr><td>TCP/IP</td><td>0</td><td>1</td></tr><tr><td>UDP/IP</td><td>1</td><td>0</td></tr><tr><td>IP</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>0</td><td>15</td><td>IPF</td><td>When set, indicates IP checksum failure.</td></tr>
<tr><td>0</td><td>14</td><td>UDPF</td><td>When set, indicates UDP checksum failure.</td></tr>
<tr><td>0</td><td>13</td><td>TCPF</td><td>When set, indicates TCP checksum failure.</td></tr>
<tr><td>0</td><td>12</td><td>RSVD</td><td>Reserved</td></tr>
<tr><td>0</td><td>11-0</td><td>Data_Length</td><td>This indicates the number of bytes of data on the page pointed by the descriptor. The content of the page should start with no reserve at the start of the page (unless offset bit is set)</td></tr>
<tr><td>4</td><td>31-0</td><td>RxBuff</td><td>The 32-bit physical address of receive buffer.</td></tr>
</table>

8	31	OFFST	Defines if a 2-byte offset exists on this page before valid data.
8	30	FRAG	Indicates the fragmentation flag is set
8	29-17	RSVD	Reserved bits.
8	16	TAVA	Tag Available. When set, the received packet is an IEEE802.1Q VLAN TAG (0x8100) available packet.
8	15-0	VLAN_TAG	If the packet 's TAG (EtherType field) is 0x8100, The NIC extracts four bytes from after source ID, sets TAVA bit to1, and moves the TAG value to this field in Rx descriptor. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canoethernetal Format Indicator.
12	31-0	RSVD	Reserved bits.
12	15-0	PARTIAL_CHECKSUM	In the case of IP packet with no fragmentation: This field is the non-inverted accumulate sum for this IP PDU including Pseudo Header. Result should be 0xFFFF if there are no errors. In the case of IP fragmentation: This field is the non-inverted accumulate sum for this IP PDU excluding Pseudo Header. Summing all partial sums of packets crossing multiple IP PDU's and performing One's complement' inversion is done by software). If the TCP/UDP packet is fragment and carried over 2 more IP packets, only the accumulate sum and not the pseudo header is included in the summation. This value is valid in descriptor with LS=1.

Register Summary

Virtual Address	Size (byte)	Name	Description	Access
0xBD20_0000	6	ETH0_IDR	ID Register. The ID register is only permitted to write by 4-byte access. Read access can be byte, word, or double word access. The initial value is autoloaded from Flash.	R/W
0xBD20_0008	8	ETH0_MAR	Multicast Register. The MAR register is only permitted to write by 4-byte access. Read access can be byte, word, or double word access. Driver is responsible for initializing these registers. The MAR defines 64 bits that is a bit wise index of the multicast function of multicast addresses. The hash function of multicast address is the upper 6 MSB's of the CRC32 of the address (destination). The index then is the numerical representation of those 6 bits in hex format.	R/W
0xBD20_0010	2	ETH0_TXOKCNT	16-bit counter of Tx DMA Ok packets.	R/W
0xBD20_0012	2	ETH0_RXOKCNT	16-bit counter of Rx Ok packets.	R/W
0xBD20_0014	2	ETH0_TXERR	16-bit packet counter of Tx errors including Tx abort, carrier lost, Tx underrun (should be happened only on jumbo frames), and out of window collision.	R/W
0xBD20_0016	2	ETH0_RXERR	16-bit packet counter of Rx errors including CRC error packets (should be larger than 8 bytes) and missed packets.	R/W
0xBD20_0018	2	ETH0_MISSPKT	16-bit counter of missed packets resulting from Rx FIFO full.	R/W

0xBD20_001A	2	ETH0_FAE	16-bit counter of Frame Alignment Error packets.	R/W
0xBD20_001C	2	ETH0_TX1COL	16-bit counter of those Tx Ok packets with only 1 collision happened before Tx Ok.	R/W
0xBD20_001E	2	ETH0_TXMCOL	16-bit counter of those Tx Ok packets with more than 1, and less than 16 collisions happened before Tx Ok.	R/W
0xBD20_0020	2	ETH0_RXOKPHY	16-bit counter of all Rx Ok packets with physical address matched destination ID.	R/W
0xBD20_0022	2	ETH0_RXOKBRD	16-bit counter of all Rx Ok packets with broadcast destination ID.	R/W
0xBD20_0024	2	ETH0_RXOKMUL	16-bit counter of all Rx Ok packets with multicast destination ID.	R/W
0xBD20_0026	2	ETH0_TXABT	16-bit counter of Tx abort packets.	R/W
0xBD20_0028	2	ETH0_TXUNDRN	16-bit counter of Tx underrun and discarded packets.	R/W
0xBD20_0034	4	ETH0_TRSR	Tx/Rx Status Register.	R
0xBD20_003B	1	ETH0_CR	Command Register.	R/W
0xBD20_003C	2	ETH0_IMR	Interrupt Mask Register.	R/W
0xBD20_003E	2	ETH0_ISR	Interrupt Status Register.	R/W
0xBD20_0040	4	ETH0_TCR	Transmit (Tx) Configuration Register.	R/W
0xBD20_0044	4	ETH0_RCR	Receive (Rx) Configuration Register.	R/W
0xBD20_0058	4	ETH0_MSR	Media Status Register.	R/W
0xBD20_005C	4	ETH0_MIIAR	MII Access Register.	R/W
0xBD20_1300	4	ETH0_ TXFDP1	Tx First Descriptor Pointer (FDP) for high priority queue.	R/W
0xBD20_1304	2	ETH0_ TXCDO1	Tx Current Descriptor Offset (CDO) for high priority queue.	R/W
0xBD20_1380	4	ETH0_ TXFDP2	Tx First Descriptor Pointer (FDP) for low priority queue.	R/W
0xBD20_1384	2	ETH0_ TXCDO2	Tx Current Descriptor Offset (CDO) for low priority queue.	R/W
0xBD20_13F0	4	ETH0_ RXFDP	Rx First Descriptor Pointer (FDP).	R/W
0xBD20_13F4	2	ETH0_ CDO	Rx Current Descriptor Offset (CDO).	R/W
0xBD20_13F6	1	ETH0_ RXRINGSIZE	Rx Ring Size (in number of Descriptors).	R/W
0xBD20_1430	2	ETH0_ RXCPUDESC	This is the descriptor number which the CPU has finished processing and returned to IO. CPU needs to update this.	R/W
0xBD20_1432	2	ETH0_ RXPSEDESC	Specifies the difference between ETH0_ RXCPUDESC and the descriptor number currently in use by NIC in which flow control will be assert.	R/W
0xBD20_1434	4	ETH0_ IOCMD	ETHER_IO_CMD.	R/W

Virtual Address	Size (byte)	Name	Description	Access
0xBD30_0000	6	ETH1_IDR	ID Register. The ID register is only permitted to write by 4-byte access. Read access can be byte, word, or double word access. The initial value is autoloaded from Flash.	R/W

0xBD30_0008	8	ETH1_MAR	Multicast Register. The MAR register is only permitted to write by 4-byte access. Read access can be byte, word, or double word access. Driver is responsible for initializing these registers. The MAR defines 64 bits that is a bit wise index of the multicast function of multicast addresses. The hash function of multicast address is the upper 6 MSB's of the CRC32 of the address (destination). The index then is the numerical representation of those 6 bits in hex format.	R/W
0xBD30_0010	2	ETH1_TXOKCNT	16-bit counter of Tx DMA Ok packets.	R/W
0xBD30_0012	2	ETH1_RXOKCNT	16-bit counter of Rx Ok packets.	R/W
0xBD30_0014	2	ETH1_TXERR	16-bit packet counter of Tx errors including Tx abort, carrier lost, Tx underrun (should be happened only on jumbo frames), and out of window collision.	R/W
0xBD30_0016	2	ETH1_RXERR	16-bit packet counter of Rx errors including CRC error packets (should be larger than 8 bytes) and missed packets.	R/W
0xBD30_0018	2	ETH1_MISSPKT	16-bit counter of missed packets resulting from Rx FIFO full.	R/W
0xBD30_001A	2	ETH1_FAE	16-bit counter of Frame Alignment Error packets.	R/W
0xBD30_001C	2	ETH1_TX1COL	16-bit counter of those Tx Ok packets with only 1 collision happened before Tx Ok.	R/W
0xBD30_001E	2	ETH1_TXMCOL	16-bit counter of those Tx Ok packets with more than 1, and less than 16 collisions happened before Tx Ok.	R/W
0xBD30_0020	2	ETH1_RXOKPHY	16-bit counter of all Rx Ok packets with physical address matched destination ID.	R/W
0xBD30_0022	2	ETH1_RXOKBRD	16-bit counter of all Rx Ok packets with broadcast destination ID.	R/W
0xBD30_0024	2	ETH1_RXOKMUL	16-bit counter of all Rx Ok packets with multicast destination ID.	R/W
0xBD30_0026	2	ETH1_TXABT	16-bit counter of Tx abort packets.	R/W
0xBD30_0028	2	ETH1_TXUNDRN	16-bit counter of Tx underrun and discarded packets.	R/W
0xBD30_0034	4	ETH1_TRSR	Tx/Rx Status Register.	R
0xBD30_003B	1	ETH1_CR	Command Register.	R/W
0xBD30_003C	2	ETH1_IMR	Interrupt Mask Register.	R/W
0xBD30_003E	2	ETH1_ISR	Interrupt Status Register.	R/W
0xBD30_0040	4	ETH1_TCR	Transmit (Tx) Configuration Register.	R/W
0xBD30_0044	4	ETH1_RCR	Receive (Rx) Configuration Register.	R/W
0xBD30_0058	4	ETH1_MSR	Media Status Register.	R/W
0xBD30_005C	4	ETH1_MIIAR	MII Access Register.	R/W
0xBD30_1300	4	ETH1_ TXFDP1	Tx First Descriptor Pointer (FDP) for high priority queue.	R/W
0xBD30_1304	2	ETH1_ TXCDO1	Tx Current Descriptor Offset (CDO) for high priority queue.	R/W
0xBD30_1380	4	ETH1_ TXFDP2	Tx First Descriptor Pointer (FDP) for low priority queue.	R/W
0xBD30_1384	2	ETH1_ TXCDO2	Tx Current Descriptor Offset (CDO) for low priority queue.	R/W
0xBD30_13F0	4	ETH1_ RXFDP	Rx First Descriptor Pointer (FDP).	R/W
0xBD30_13F4	2	ETH1_ CDO	Rx Current Descriptor Offset (CDO).	R/W
0xBD30_13F6	1	ETH1_ RXRINGSIZE	Rx Ring Size (in number of Descriptors).	R/W

0xBD30_1430	2	ETH1_ RXCPUDESC	This is the descriptor number which the CPU has finished processing and returned to IO. CPU needs to update this.	R/W
0xBD30_1432	2	ETH1_ RXPSEDESC	Specifies the difference between ETH1_ RXCPUDESC and the descriptor number currently in use by NIC in which flow control will be assert.	R/W
0xBD30_1434	4	ETH1_ IOCMD	ETHER_IO_CMD.	R/W

0xBD20_0000 **Ethernet0 ID Register (ETH0_IDR)**
0xBD30_0000 **Ethernet1 ID Register (ETH1_IDR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID3								ID2								ID1								ID0							

0xBD20_0004 **cont. of Ethernet0 ID Register (ETH0_IDR)**
0xBD30_0004 **cont. of Ethernet1 ID Register (ETH1_IDR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																ID5								ID4							

Reset: 0x0

Bit	Bit Name	Description	R/W	InitVal
7-0	ID0	ID Register. The ID register0-5 are only permitted to write by 4-byte access. Read access can be byte, word, or double word access. The initial value is autoloaded from Flash.	R/W	?
15-8	ID1			
23-16	ID2			
31-0	ID3			
7-0	ID4			
15-8	ID5			

0xBD20_0008 **Ethernet0 Multicast Register (ETH0_MAR)**
0xBD30_0008 **Ethernet1 Multicast Register (ETH1_MAR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR3								MAR2								MAR1								MAR0							

0xBD20_000C **cont. of Ethernet0 Multicast Register (ETH0_MAR)**
0xBD30_000C **cont. of Ethernet1 Multicast Register (ETH1_MAR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAR7								MAR6								MAR5								MAR4							

Reset: 0x?

Bit	Bit Name	Description	R/W	InitVal
7-0	MAR0	Multicast Register. The MAR register0-7 is only permitted to write by 4-byte access. Read access can be byte, word, or double word access. Driver is responsible for initializing these registers. The MAR7-0 defined a 64-bits, which is a bit wise index of the multicast function of multicast addresses. The hash function of multicast address is the upper 6 MSB's of the CRC32 of the address (destination). The index then is the numerical representation of those 6 bits in hex format.	R/W	?
15-8	MAR1			
23-16	MAR2			
31-0	MAR3			
7-0	MAR4			
15-8	MAR5			
23-16	MAR6			
31-24	MAR7			

0xBD20_0010 **Ethernet0 TX DMA OK Counter Register (ETH0_TXOKCNT)**
0xBD30_0010 **Ethernet1 TX DMA OK Counter Register (ETH1_TXOKCNT)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		TxOkCnt															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	TxOkCnt	16-bit counter of Tx DMA Ok packets. Rolls over automatically. Write to clear.	R/W	0

0xBD20_0012 **Ethernet0 RX DMA OK Counter Register (ETH0_RXOKCNT)**
0xBD30_0012 **Ethernet1 RX DMA OK Counter Register (ETH1_RXOKCNT)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		RxOkCnt															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	RxOkCnt	16-bit counter of Rx DMA Ok packets. Rolls over automatically. Write to clear.	R/W	0

0xBD20_0014 **Ethernet0 TX Error Counter Register (ETH0_TXERR)**
0xBD30_0014 **Ethernet1 TX Error Counter Register (ETH1_TXERR)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		TxErrCnt															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	TxErrCnt	16-bit counter of Tx error packets. Rolls over automatically. Write to clear.	R/W	0

0xBD20_0016 **Ethernet0 RX Error Counter Register (ETH0_RXERR)**
0xBD30_0016 **Ethernet1 RX Error Counter Register (ETH1_RXERR)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		RxErrCnt															

Reset: 0x01

Bit	Bit Name	Description	R/W	InitVal
15-0	RxErrCnt	16-bit counter of Rx error packets. Rolls over automatically. Write to clear.	R/W	1

0xBD20_0018 **Ethernet0 Miss Packet Counter Register (ETH0_MISSPKT)**
0xBD30_0018 **Ethernet1 Miss Packet Counter Register (ETH1_MISSPKT)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		MissPkt															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	MissPkt	16-bit counter missed packets. Rolls over automatically. Write to clear.	R/W	0

0xBD20_001A **Ethernet0 FAE Counter Register (ETH0_FAE)**
0xBD30_001A **Ethernet1 FAE Counter Register (ETH1_FAE)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		FAECnt															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	FAECnt	16-bit counter of Fragment Alignment Error packets. Rolls over automatically. Write to clear.	R/W	0

0xBD20_001C **Ethernet0 Tx 1st Collision Counter Register (ETH0_TX1COL)**
0xBD30_001C **Ethernet1 Tx 1st Collision Counter Register (ETH1_TX1COL)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Tx1Col															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	Tx1Col	16-bit counter of TxCol packets. Rolls over automatically. Write to clear. This only records which have entered just one collision before Tx OK.	R/W	0

0xBD20_001E **Ethernet0 Tx Multi Collision Counter Register (ETH0_TXMCOL)**
0xBD30_001E **Ethernet1 Tx Multi Collision Counter Register (ETH1_TXMCOL)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		TxMCol															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	TxMCol	16-bit counter of Tx Multi Collision packets. Rolls over automatically. Write to clear. This keeps track of those packets with less than 16 collisions (or the configured retry count) before Tx Ok.	R/W	0

0xBD20_0020 **Ethernet0 Rx Ok Physical addr matched Counter Register (ETH0_RXPHY)**
0xBD30_0020 **Ethernet1 Rx Ok Physical addr matched Counter Register (ETH1_RXPHY)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		RxPhyAddM															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	RxPhyAddM	16-bit counter of Rx Ok packets with physical address matching destination address. Rolls over automatically. Write to clear.	R/W	0

0xBD20_0022 **Ethernet0 Rx Ok Broadcast addr matched Counter Register (ETH0_RXBRD)**
0xBD30_0022 **Ethernet1 Rx Ok Broadcast addr matched Counter Register (ETH1_RXBRD)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

	RxBrdAddM

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	RxBrdAddM	16-bit counter of Rx Ok packets with broadcast destination address. Rolls over automatically. Write to clear.	R/W	0

0xBD20_0024 **Ethernet0 Rx Ok Multicast addr matched Counter Register (ETH0_RXMUL)**
0xBD30_0024 **Ethernet1 Rx Ok Multicast addr matched Counter Register (ETH1_RXMUL)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		RxMulAddM															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	RxMulAddM	16-bit counter of Rx Ok packets with multicast destination address. Rolls over automatically. Write to clear.	R/W	0

0xBD20_0026 **Ethernet0 Tx Abort Counter Register (ETH0_TXABT)**
0xBD30_0026 **Ethernet1 Tx Abort Counter Register (ETH1_TXABT)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		TxAbt															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	TxAbt	16-bit counter of Tx aborted packets. Rolls over automatically. Write to clear. This accounts for over collision, underrun, LNK failure conditions.	R/W	0

0xBD20_0028 **Ethernet0 Tx Underrun Counter Register (ETH0_TXUNDRN)**
0xBD30_0028 **Ethernet1 Tx Underrun Counter Register (ETH1_TXUNDRN)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		TxUndrn															

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
15-0	TxUndrn	16-bit counter of Tx Underrun packets. Rolls over automatically. Write to clear. (Only possible for jumbo frame which may not be allowed in RTL8186)	R/W	0

0xBD20_0034 **Ethernet0 Tx/Rx Status Register (ETH0_TRSR)**
0xBD30_0034 **Ethernet1 Tx/Rx Status Register (ETH1_TRSR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																												TOK	TUN	RXFE	RSVD

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
3	TOK	Transmit OK: Set to 1 indicates that the transmission of a packet was completed successfully and no transmit underrun occurs.	R	0
2	TUN	Transmit FIFO Underrun: Set to 1 if the Tx FIFO was exhausted during the transmission of a packet. The NIC can re-transfer data if the Tx FIFO underruns and can also transmit the packet to the wire successfully even though the Tx FIFO underruns. That is, when TSD<TUN>=1, TSD<TOK>=0 and ISR<TOK>=1 (or ISR<TER>=1). Handle underrun transmit with care.	R	0
1	RXFE	Rx FIFO is Empty.	R	0
0	RSVD	Reserved.	-	-

0xBD20_003B **Ethernet0 Command Register (ETH0_CR)**
0xBD30_003B **Ethernet1 Command Register (ETH1_CR)**

31	8	7	6	5	4	3	2	1	0
		(Reserved)					RXVLAN	RXCSE	RST

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
2	RXVLAN	Receive VLAN de-tagging enable. 1: Enable. 0: Disable.	R/W	0
1	RXCSE	Receive checksum offload enable. 1: Enable. 0: Disable.	R/W	0
0	RST	Reset: Setting to 1 to force the NIC enters a software reset state which disables the transmitter and receiver, reinitializes the FIFOs, triggers interrupt Swint for RISC to reset the system buffer pointer to the initial value Tx/Rx FDP. The values of IDR0-5 and MAR0-7 will have no changes. This bit is 1 during the reset operation, and is cleared to 0 by the NIC when the reset operation is complete.	R/W	0

0xBD20_003C **Ethernet0 Interrupt Mask Register (ETH0_IMR)**
0xBD30_003C **Ethernet1 Interrupt Mask Register (ETH1_IMR)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		(Reserved)					SWInt	TDU	LNKCHG	TER	TOK	RDU	RXFULL	RSVD	RXRUNT	RSVD	ROK

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
10	SWInt	1: enable interrupt 0: disable interrupt	R/W	0
9	TDU	1: enable interrupt	R/W	0

		0: disable interrupt		
8	LNKCHG	1: enable interrupt 0: disable interrupt	R/W	0
7	TER	1: enable interrupt 0: disable interrupt	R/W	0
6	TOK	1: enable interrupt 0: disable interrupt	R/W	0
5	RDU	1: enable interrupt 0: disable interrupt	R/W	0
4	RXFULL	1: enable interrupt 0: disable interrupt	R/W	0
3, 1	RSVD	Reserved.	-	-
2	RXRUNT	1: enable interrupt 0: disable interrupt	R/W	0
0	ROK	1: enable interrupt 0: disable interrupt	R/W	0

0xBD20_003E **Ethernet0 Interrupt Status Register (ETH0_ISR)**
0xBD30_003E **Ethernet1 Interrupt Status Register (ETH1_ISR)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		(Reserved)					SWInt	TDU	LNKCHG	TER	TOK	RDU	RXFULL	RSVD	RXRUNT	RSVD	ROK

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
10	SWInt	Software Interrupt pending: When set to 1 indicates a software interrupt was forced. Write 1 to clear.	R/W	0
9	TDU	Tx Descriptor Unavailable: When set, indicates Tx descriptor is unavailable.	R/W	0
8	LNKCHG	Link Change: Set to 1 when link status is changed. Write 1 to clear.	R/W	0
7	TER	Transmit (Tx) Error: Indicates that a packet transmission was aborted, due to excessive collisions, according to the TXRR's setting. Write 1 to clear.	R/W	0
6	TOK	Transmit Interrupt: Indicates that the DMA of the last descriptor of RxIntMitigation number of Tx packet has completed and the last descriptor has been closed. Write 1 to clear.	R/W	0
5	RDU	Rx Descriptor Unavailable: When set, indicates Rx descriptor is unavailable or Rx_Pse_Des_Thres was broken.	R/W	0
4	RXFULL	Rx FIFO Overflow, caused by RBO/RDU, poor system bus (Lexra bus) performance, or overloaded Lexra bus traffic.	R/W	0
3, 1	RSVD	Reserved.	-	-
2	RXRUNT	Rx error caused by runt error characterized by the frame length in bytes being less than 64 bytes. Write 1 to clear.	R/W	0
0	RXOK	Receive (Rx) OK: This interrupt is set either when RxIntMitigation	R/W	0

		packet is met or RxPktTimer expires. Write 1 to clear.		

0xBD20_0040 **Ethernet0 Transmit Configuration Register (ETH0_TCR)**
0xBD30_0040 **Ethernet1 Transmit Configuration Register (ETH1_TCR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																			IFG			LBK		(Reserved)							

Reset: 0x0000_0C00

Bit	Bit Name	Description	R/W	InitVal
12-10	IFG	InterFrameGap Time: This field allows the user to adjust the interframe gap time longer than the standard: 9.6 us for 10Mbps, 960 ns for 100Mbps. The time can be programmed from 9.6 us to 14.4 us (10Mbps) and 960ns to 1440ns (100Mbps). The formula for the inter frame gap is: IFG: IFG@100MHz (nS) / IFG@10MHz (uS) 0 1 1: 960 / 9.6 1 0 0: 960 + 8 * 10 / 9.6 +8 * 0.1 1 0 1: 960 + 16 * 10 / 9.6 +16 * 0.1 1 1 0: 960 + 24 * 10 / 9.6 +24 * 0.1 1 1 1: 960 + 32 * 10 / 9.6 +32 * 0.1 0 0 0: 960 + 40 * 10 / 9.6 +40 * 0.1 0 0 1: 960 + 48 * 10 / 9.6 +48 * 0.1 0 1 0: 960 + 96 * 10 / 9.6 +96 * 0.1	R/W	3
9-8	LBK	Loopback test. There will be no packet on the TX+/- lines under the Loopback test condition. The loopback function must be independent of the link state. 00 : normal operation 01 : Reserved 10 : Reserved 11 : Loopback mode	R/W	0

0xBD20_0044 **Ethernet0 Receive Configuration Register (ETH0_RCR)**
0xBD30_0044 **Ethernet1 Receive Configuration Register (ETH1_RCR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																									AFLOW	AER	AR	AB	AM	APM	AAP

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
6	AFLOW	Set 1 to accept flow control packets	R/W	0
5	AER	Accept Error Packet: When set to 1, all packets with CRC error, alignment error, and/or collided fragments will be accepted. When set to 0, all packets with CRC error, alignment error, and/or collided fragments will be rejected.	R/W	0
4	AR	Accept Runt: This bit allows the receiver to accept	R/W	0

		packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt. Set to 1 to accept runt packets.		
3	AB	Set to 1 to accept broadcast packets, 0 to reject.	R/W	0
2	AM	Set to 1 to accept multicast packets, 0 to reject.	R/W	0
1	APM	Set to 1 to accept physical match packets, 0 to reject.	R/W	0
0	AAP	Set to 1 to accept all packets with physical destination address, 0 to reject.	R/W	0

0xBD20_0058 **Ethernet0 Media Status Register (ETH0_MSR)**
0xBD30_0058 **Ethernet1 Media Status Register (ETH1_MSR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																								FTXFC	RXFCE	TXFCE	RSVD	SPEED	LINKB	TXPF	RXPF

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
7	FTXFC	Force Tx Flow Control: 1 = enabled Flow control in the absence of NWAY. 0 = disables Flow control in the absence of NWAY.	R/W	0
6	RXFCE	RX Flow control Enable: The flow control is enabled in full-duplex mode only. Packets are dropped if buffer is exhausted. Default is 0. 1 = Rx Flow Control Enabled. 0 = Rx Flow Control Disabled.	R/W	0
5	TXFCE	Tx Flow Control Enable: 1 = enable flow control ACCEPT ERRORS MUST NOT BE ENABLED	R/W	0
4	RSVD	Reserved.	R/W	0
3	SPEED	Media Mode: 1 = 10 Mbps. 0 = 100Mbps.	R/W	0
2	LINKB	Inverse of Link status. 0 = Link OK. 1 = Link Fail.	R/W	0
1	TXPF	Tx Pause frame: 1: Ethernet NIC has sent a pause packet. 0: Ethernet NIC has sent a timer done packet.	R/W	0
0	RXPF	Pause Flag: 1 = Ethernet NIC is in backoff state because a pause packet received. 0: pause state is clear.	R/W	0

0xBD20_005C **Ethernet0 MII Access Register (ETH0_MIIAR)**
0xBD30_005C **Ethernet1 MII Access Register (ETH1_MIIAR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLAG	PHYADDR					(Reserved)					REGADDR					DATA																

Reset: 0x0400_0000

Bit	Bit Name	Description	R/W	InitVal
31	FLAG	Flag bit, used to identify access to MII register: 1: Write data to MII register. Turns to 0	R/W	0

		automatically upon completion of MAC writing to the specified MII register. 0: Read data from MII register. Turns to 1 automatically upon completion of MAC reading the specified MII register. Read write turn around time I s about 64 us.		
30-26	PHYADDR	Defines the Phy address for the MII.	R/W	0x1
20-16	REGADDR	5-bit MII register address.	R/W	0
15-0	DATA	16 bit MII resgister data.	R/W	0

0xBD20_1300 **Ethernet0 TX First Descriptor Pointer 1 Register (ETH0_TXFDP1)**
0xBD30_1300 **Ethernet1 TX First Descriptor Pointer 1 Register (ETH1_TXFDP1)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxFDP1																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	TxFDP1	High priority Tx First Descriptor Pointer to the Tx Ring.	R/W	0

0xBD20_1304 **Ethernet0 TX Current Descriptor Offset 1 Register (ETH0_TXCDO1)**
0xBD30_1304 **Ethernet1 TX Current Descriptor Offset 1 Register (ETH1_TXCDO1)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																(Reserved)										TxCDO1					

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
5-0	TxCDO1	High priority Tx Current Descriptor Offset: FDP+CDO = current descriptor pointer. CDO increments by 16 bytes each time.	R/W	0

0xBD20_1380 **Ethernet0 TX First Descriptor Pointer 2 Register (ETH0_TXFDP2)**
0xBD30_1380 **Ethernet1 TX First Descriptor Pointer 2 Register (ETH1_TXFDP2)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxFDP2																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	TxFDP2	Tx First Descriptor Pointer to the low priority Tx Ring.	R/W	0

0xBD20_1384 **Ethernet0 TX Current Descriptor Offset 2 Register (ETH0_TXCDO2)**
0xBD30_1384 **Ethernet1 TX Current Descriptor Offset 2 Register (ETH1_TXCDO2)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																(Reserved)										TxCDO2					

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
5-0	TxCDO2	Low priority Tx Current Descriptor Offset: FDP+CDO = current descriptor pointer. CDO	R/W	0

		increments by 16 bytes each time.		

0xBD20_13F0 **Ethernet0 RX First Descriptor Pointer Register (ETH0_RXFDP)**
0xBD30_13F0 **Ethernet1 RX First Descriptor Pointer Register (ETH1_RXFDP)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxFDP																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	RxFDP	Rx First Descriptor Pointer to the Rx Descriptor Ring.	R/W	0

0xBD20_13F4 **Ethernet0 RX Current Descriptor Offset Register (ETH0_RXCDO)**
0xBD30_13F4 **Ethernet1 RX Current Descriptor Offset Register (ETH1_RXCDO)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)										RxCDO							

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
5-0	RxCDO	Rx Current Descriptor Offset: RxFDP+RxCDO = current descriptor pointer. CDO increments by 16 each time (each increment is one byte).	R/W	0

0xBD20_13F6 **Ethernet0 RX Descriptor Ring Size Register (ETH0_RXRINGSIZE)**
0xBD30_13F6 **Ethernet1 RX Descriptor Ring Size Register (ETH1_RXRINGSIZE)**

31	8	7	6	5	4	3	2	1	0
(Reserved)								SIZE	

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
1-0	SIZE	This is the total number of descriptors in the Rx descriptor ring. 00: 16 descriptors 01: 32 descriptors 10: 64 descriptors	R/W	0

0xBD20_1430 **Ethernet0 RX CPU Descriptor Number Register (ETH0_RXCPUDESC)**
0xBD30_1430 **Ethernet1 RX CPU Descriptor Number Register (ETH1_RXCPUDESC)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)									WRAP	RSVD		Rx_CPU_Des_Num					

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
8	WRAP	This indicates to Ethernet NIC that Ethernet driver has allocated free RX CMD descriptors past End Of Ring. Ethernet NIC module will clear this bit when it wraps around the RX CMD descriptor ring.	R/W	0
5-0	Rx_CPU_Des_N	This is the descriptor # which the CPU has	R/W	0

	um	finished processing and returned to IO. CPU needs to update this. When Ethernet descriptor processing reaches End Of Ring, Ethernet driver must set "WRAP" (1431h) bit to high. This will indicate to Ethernet NIC module that descriptors have been allocated past end of ring descriptor.		

0xBD20_1432 **Ethernet0 RX PSE Descriptor Threshold Register (ETH0_RXPSEDESC)**
0xBD30_1432 **Ethernet1 RX PSE Descriptor Threshold Register (ETH1_RXPSEDESC)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)												Rx_PSE_Des_Num					

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
5-0	Rx_PSE_Des_Num	Tx Threshold: Specifies the threshold level in the Tx FIFO to begin the transmission. When the byte count of the data in the Tx FIFO reaches this level, (or the FIFO contains at least one complete packet or the end of a packet) the Ethernet NIC module will transmit this packet.	R/W	0

0xBD20_1434 **Ethernet0 I/O Command Register (ETH0_IOCMD)**
0xBD30_1434 **Ethernet1 I/O Command Register (ETH1_IOCMD)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)											TXTH		TxInt Mitigation			RXPkt Timer			RXFTH		RxInt Mitigation			(Reserved)				RE	TE	TXFNL	TXFNH

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
20-19	TXTH	Tx Threshold: Specifies the threshold level in the Tx FIFO to begin the transmission. When the byte count of the data in the Tx FIFO reaches this level, (or the FIFO contains at least one complete packet or the end of a packet) the NIC will transmit this packet. 00: 64 bytes 01: 128 bytes 10: 256 bytes 11: Reserved	R/W	0
18-16	TxIntMitigation	This sets the number of packets received before TxOK interrupt is triggered. 000- 1 pkt / 001- 2 pkts 010- 3 pkt / 011- 4 pkts 100- 5 pkt / 101- 6 pkts 110- 7 pkt / 111- 8 pkts	R/W	0
15-13	RXPktTimer	Timer to trigger RxOK interrupt after receipt of RxIntMitigation pkts. 000 – no timer set 001 ~ 111 : the timer interval defining a multiple	R/W	0

		of 82us ex: 011 = timer interval set to 3 x 82us or 246us This only applies to packets of size larger than 128 bytes. Once RxOK is asserted the timer mechanism is reinitialized.		
12-11	RXFTH	Rx FIFO Threshold: Specifies Rx FIFO Threshold level. When the number of the received data bytes from a packet, which is being received into the Rx FIFO, has reached to this level (or the FIFO has contained a complete packet), the Lexra bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following table: 00 = no rx threshold. The NIC begins the transfer of data after having received a whole packet in the FIFO. 01 = 32 bytes 10 = 64 bytes 11 = 128 bytes	R/W	0
10-8	RxIntMitigation	This sets the number of packets received before RxOK interrupt is triggered. This only applies to packets of size larger than 128 bytes. Once RxOK is asserted the mitigation mechanism is reinitialized. 000- 1 pkt / 001- 2 pkts 010- 3 pkts / 011- 4 pkts 100- 5 pkts / 101- 6 pkts 110- 7 pkts / 111- 8 pkts	R/W	0
3	RE	MII Rx Enable	R/W	0
2	TE	MII Tx Enable	R/W	0
1	TXFNL	Low Priority DMA-Ethernet Transmit enable. 1: Enable. 0: Disable.	R/W	0
0	TXFNH	High Priority DMA-Ethernet Transmit enable. 1: Enable. 0: Disable.	R/W	0

10. UART Controller

RTL8186 features two 16C550 compatible UART, containing a 16-bytes FIFO on each. In addition, auto flow control is provided, in which, auto-CTS mode (CTS controls transmitter) and auto-RTS mode (Receiver FIFO contents and threshold control RTS) are both supported. The baud rate is programmable and allows division of any input reference clock by 1 to (2^16-1) and generates an internal 16x clock. RTL8186 provides fully programmable serial interface, which can be configured to support 7,8 bit characters, even, odd, no parity generation and detection, and 1 or 2 stop bit generation. Also, fully prioritized interrupt control and loopback functionality for diagnostic capability are provided.

Register Summary

Virtual address	Size (byte)	Name	Description	Access
0xBD01_00C3	1	UART0_RBR	Receiver buffer register. (DLAB=0)	R
0xBD01_00C3	1	UART0_THR	Transmitter holding register. (DLAB=0)	W
0xBD01_00C3	1	UART0_DLL	Divisor latch LSB. (DLAB=1)	R/W

0xBD01_00C7	1	UART0_IER	Interrupt enable register. (DLAB=0)	R/W
0xBD01_00C7	1	UART0_DLM	Divisor latch MSB. (DLAB=1)	R/W
0xBD01_00CB	1	UART0_IIR	Interrupt identification register.	R
0xBD01_00CB	1	UART0_FCR	FIFO control register	W
0xBD01_00CF	1	UART0_LCR	Line control register	R/W
0xBD01_00D3	1	UART0_MCR	Modem control register	R/W
0xBD01_00D7	1	UART0_LSR	Line status register	R/W
0xBD01_00DB	1	UART0_MSR	Modem status register	R/W
0xBD01_00DF	1	UART0_SCR	Scratch register	R/W
0xBD01_00E3	1	UART1_RBR	Receiver buffer register. (DLAB=0)	R
0xBD01_00E3	1	UART1_THR	Transmitter holding register. (DLAB=0)	W
0xBD01_00E3	1	UART1_DLL	Divisor latch LSB. (DLAB=1)	R/W
0xBD01_00E7	1	UART1_IER	Interrupt enable register. (DLAB=0)	R/W
0xBD01_00E7	1	UART1_DLM	Divisor latch MSB. (DLAB=1)	R/W
0xBD01_00EB	1	UART1_IIR	Interrupt identification register.	R
0xBD01_00EB	1	UART1_FCR	FIFO control register	W
0xBD01_00EF	1	UART1_LCR	Line control register	R/W
0xBD01_00F3	1	UART1_MCR	Modem control register	R/W
0xBD01_00F7	1	UART1_LSR	Line status register	R/W
0xBD01_00FB	1	UART1_MSR	Modem status register	R/W
0xBD01_00FF	1	UART1_SCR	Scratch register	R/W

0xBD01_00C3 (DLAB = 0, Read_Mode) **UART0 Receive Buffer Register (UART0_RBR)**
0xBD01_00E3 (DLAB = 0, Read_Mode) **UART1 Receive Buffer Register (UART1_RBR)**

31	8	7	6	5	4	3	2	1	0
		RDATA							

Reset: 0x00

0xBD01_00C3 (DLAB = 0, Write_Mode) **UART0 Transmitter Holding Register (UART0_THR)**
0xBD01_00E3 (DLAB = 0, Write_Mode) **UART1 Transmitter Holding Register (UART1_THR)**

31	8	7	6	5	4	3	2	1	0
		WDATA							

Reset: 0x00

0xBD01_00C3 (DLAB = 1) **UART0 Divisor Latch LSB Register (UART0_DLL)**
0xBD01_00E3 (DLAB = 1) **UART1 Divisor Latch LSB Register (UART1_DLL)**

31	8	7	6	5	4	3	2	1	0
		DLLB							

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
7-0	RDATA	Receive Data	R	0
Bit	**Bit Name**	**Description**	**R/W**	**InitVal**
7-0	WDATA	Write Transmit Holding Data	W	0
Bit	**Bit Name**	**Description**	**R/W**	**InitVal**
7-0	DLLB	Divisor Latch LSB	R/W	0

0xBD01_00C7 (DLAB = 0) **UART0 Interrupt Enable Register (UART0_IER)**
0xBD01_00E7 (DLAB = 0) **UART1 Interrupt Enable Register (UART1_IER)**

31	8	7	6	5	4	3	2	1	0

RSVD	ELP	ESLP	EDSSI	ELSI	ETBEI	ERBI	

Reset: 0x00

0xBD01_00C7 (DLAB = 1) **UART0 Divisor Latch MSB Register (UART0_DLM)**
0xBD01_00E7 (DLAB = 1) **UART1 Divisor Latch MSB Register (UART1_DLM)**

31	8	7	6	5	4	3	2	1	0
		DLMB							

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
7-6	RSVD	Reserved		
5	ELP	Low power mode enable	R/W	0
4	ESLP	Sleep mode enable	R/W	0
3	EDSSI	Enable modem status register interrupt	R/W	0
2	ELSI	Enable receiver line status interrupt	R/W	0
1	ETBEI	Enable transmitter holding register empty interrupt	R/W	0
0	ERBI	Enable received data available interrupt	R/W	0
Bit	**Bit Name**	**Description**	**R/W**	**InitVal**
7-0	DLMB	Divisor Latch MSB	R/W	0

0xBD01_00CB **UART0 Interrupt Identification Register (UART0_IIR)**
0xBD01_00EB **UART1 Interrupt Identification Register (UART1_IIR)**

31	8	7	6	5	4	3	2	1	0
		FIFO64			RSVD	IID			IPND

Reset: 0xC0

Bit	Bit Name	Description	R/W	InitVal
7-5	FIFO64	000 = no FIFO 110 = 16-byte FIFO	R	110
4	RSVD	Reserved	R	0
3-1	IID	Interrupt ID. IID[1:0] indicates the interrupt priority. Illustrated at following table:	R	000
0	IPND	Interrupt pending 0 = interrupt pending	R	0

Interrupt Priority

Interrupt Identification Register				Priority level	Interrupt type	Interrupt source	Interrupt reset method
Bit3	Bit2	Bit1	Bit0				
0	0	0	1	None	None	None	None
0	1	1	0	1	Receiver line status	Overrun, parity, framing errors or break	Read LSR
0	1	0	0	2	Received data available	DR bit is set.	Read RBR.
1	1	0	0	2	Character time-out indication	No characters have been removed from or input to FIFO during the last character times and at 1 character in it.	Read RBR

0	0	1	0	3	Transmitter holding register empty	THRE bit set.	Reading IIR or write THR
0	0	0	0	4	Modem status	CTS#,DSR#,RI#,DCD#	Reading MSR

0xBD01_00CB **UART0 FIFO Control Register (UART0_FCR)**
0xBD01_00EB **UART1 FIFO Control Register (UART1_FCR)**

31	8	7	6	5	4	3	2	1	0
		RTRG		RSVD			TFRST	RFRST	EFIFO

Reset: 0xC0

Bit	Bit Name	Description	R/W	InitVal
7-6	RTRG	Receiver trigger level Trigger level: 16-byte 00 = 01 01 = 04 10 = 08 11 = 14	W	11
3-5	RSVD	Reserved		
2	TFRST	Transmitter FIFO reset. Writes 1 to clear the transmitter FIFO.	W	0
1	RFRST	Receiver FIFO reset. Writes 1 to clear the receiver FIFO.	W	0
0	EFIFO	Enable FIFO. When this bit is set, enable the transmitter and receiver FIFO. Changing this bit clears the FIFO.	W	0

0xBD01_00CF **UART0 Line Control Register (UART0_LCR)**
0xBD01_00EF **UART1 Line Control Register (UART1_LCR)**

31	8	7	6	5	4	3	2	1	0
		DLAB	BRK	EPS		PEN	STB	WLS	

Reset: 0x03

Bit	Bit Name	Description	R/W	InitVal
7	DLAB	Divisor latch access bit.	R/W	0
6	BRK	Break control. Set this bit force TXD to the spacing (low) state.(break) Clear this bit to disable break condition.	R/W	0
5-4	EPS[1:0]	Even parity select 00 = odd parity 01 = even parity 10 = mark parity 11 = space parity	R/W	0
3	PEN	Parity enable	R/W	0
2	STB	Number of stop bits 0 = 1 bit 1 = 2 bits	R/W	0
1-0	WLS[1:0]	Word length select 10 = 7 bits	R/W	11

		11 = 8 bits		

0xBD01_00D3 **UART0 Modem Control Register (UART0_MCR)**
0xBD01_00F3 **UART1 Modem Control Register (UART1_MCR)**

31	8	7	6	5	4	3	2	1	0
		RSVD		AFE	LOOP	RSVD		RTS	RSVD

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
7-6	RSVD	Reserved		
5	AFE	Auto flow control enable	R/W	0
4	LOOP	Loopback	R/W	0
2-3	RSVD	Reserved		
1	RTS	Request to send 0 = Set RTS# high 1 = Set RTS# low	R/W	0
0	RSVD	Reserved		

0xBD01_00D7 **UART0 Line Status Register (UART0_LSR)**
0xBD01_00F7 **UART1 Line Status Register (UART1_LSR)**

31	8	7	6	5	4	3	2	1	0
		RFE	TEMT	THRE	BI	FE	PE	OE	DR

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
7	RFE	Errors in receiver FIFO. At least one parity, framing and break error in the FIFO.	R	0
6	TEMT	Transmitter empty Character mode: both THR and TSR are empty. FIFO mode: both transmitter FIFO and TSR are empty	R	0
5	THRE	Transmitter holding register empty. Character mode: THR is empty. FIFO mode: transmitter FIFO is empty	R	0
4	BI	Break interrupt indicator	R	0
3	FE	Framing error	R	0
2	PE	Parity error	R	0
1	OE	Overrun error. An overrun occurs when the receiver FIFO is full and the next character is completely received in the receiver shift register. An OE is indicated. The character in the shift register will be overwritten.	R	0
0	DR	Data ready. Character mode: data ready in RBR FIFO mode: receiver FIFO is not empty.	R	0

0xBD01_00DB **UART0 Modem Status Register (UART0_MSR)**
0xBD01_00FB **UART1 Modem Status Register (UART1_MSR)**

31	8	7	6	5	4	3	2	1	0

DCD	RI	DSR	CTS	RSVD	ΔCTS

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
7	DCD	In loopback mode, returns the bit 2 of MCR. In normal mode, returns 1.	R	1
6	RI	In loopback mode, returns the bit 3 of MCR. In normal mode, returns 0.	R	0
5	DSR	In loopback mode, returns the bit 0 of MCR In normal mode, returns 1.	R	1
4	CTS	Clear to send. 0 = CTS# detected high 1 = CTS# detected low	R	0
3-1	RSVD	Reserved		
0	ΔCTS	Delta clear to send. CTS# signal transits.	R	0

11. Timer & Watchdog

There are four sets of hardware timers and one watchdog timer. Each timer can be configured as timer mode or counter mode. In both counter and timer mode, the time value is counted down from the initial value to zero (the value is reduced one for every timer clock). When the value reaches zero, the timer stops and an interrupt is issued. When an interrupt is issued in timer mode, the time value will be reset to its initial value and the count down will restart. An interrupt will be issued whenever the count down value reaches zero.

The source clock of timer could be configured to use base clock directly, or based on the base clock divided by a configurable register value – CDBR.

When watchdog timer is enabled, it will cause a system reset when a time-out occurs. The time-out interval may be set in the registers. The time unit value is based on the base clock divided by the base value, which is the same used by all timer.

Register Summary

Virtual address	Size (byte)	Name	Description	Access
0xBD01_0050	2	TCCNR	Timer/Counter control register	R/W
0xBD01_0054	1	TCIR	Timer/Counter interrupt register	R/W
0xBD01_0058	2	CDBR	Clock division base register	R/W
0xBD01_005C	2	WDTCNR	Watchdog timer control register	R/W
0xBD01_0060	3	TC0DATA	Timer/Counter 0 data register. It specifies the time-out duration.	R/W
0xBD01_0064	3	TC1DATA	Timer/Counter 1 data register. It specifies the time-out duration.	R/W
0xBD01_0068	4	TC2DATA	Timer/Counter 2 data register. It specifies the time-out duration.	R/W
0xBD01_006C	4	TC3DATA	Timer/Counter 3 data register. It specifies the time-out duration.	R/W
0xBD01_0070	3	TC0CNT	Timer/Counter 0 count register	R
0xBD01_0074	3	TC1CNT	Timer/Counter 1 count register	R
0xBD01_0078	4	TC2CNT	Timer/Counter 2 count register	R
0xBD01_007C	4	TC3CNT	Timer/Counter 3 count register	R

0xBD01_0050 **Timer/Counter Control register (TCCNR)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		RSVD		TCXCK	RSVD	TC3SRC	TC2SRC	TC1SRC	TC0SRC	TC3MODE	TC3EN	TC2MODE	TC2EN	TC1MODE	TC1EN	TC0MODE	TC0EN

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
13	TCXCK	timer/iic reference to xck 0 : xck = 22MHz 1 : xck = 20MHz	R/W	0
11	TC3SRC	Timer/Counter 3 clock source 0=Base clock 1=Basic timer	R/W	0
10	TC2SRC	Timer/Counter 2 clock source 0=Base clock 1=Basic timer	R/W	0
9	TC1SRC	Timer/Counter 1 clock source 0=Base clock 1=Basic timer	R/W	0
8	TC0SRC	Timer/Counter 0 clock source 0=Base clock 1=Basic timer	R/W	0
7	TC3MODE	Timer/Counter 3 mode 0=counter mode 1=timer mode	R/W	0
6	TC3EN	Timer/Counter 3 enable	R/W	0
5	TC2MODE	Timer/Counter 2 mode 0=counter mode 1=timer mode	R/W	0
4	TC2EN	Timer/Counter 2 enable	R/W	0
3	TC1MODE	Timer/Counter 1 mode 0=counter mode 1=timer mode	R/W	0
2	TC1EN	Timer/Counter 1 enable	R/W	0
1	TC0MODE	Timer/Counter 0 mode 0=counter mode 1=timer mode	R/W	0
0	TC0EN	Timer/Counter 0 enable	R/W	0

0xBD01_0054 **Timer/Counter Interrupt Register (TCIR)**

31	8	7	6	5	4	3	2	1	0
		TC3IP	TC2IP	TC1IP	TC0IP	TC3IE	TC2IE	TC1IE	TC0IE

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
7	TC3IP	Timer/Counter 3 interrupt pending. Write “1” to clear the interrupt.	R/W	0
6	TC2IP	Timer/Counter 2 interrupt pending. Write “1” to clear the interrupt.	R/W	0
5	TC1IP	Timer/Counter 1 interrupt pending. Write “1” to	R/W	0

		clear the interrupt.		
4	TC0IP	Timer/Counter 0 interrupt pending. Write “1” to clear the interrupt.	R/W	0
3	TC3IE	Timer/Counter 3 interrupt enable	R/W	0
2	TC2IE	Timer/Counter 2 interrupt enable	R/W	0
1	TC1IE	Timer/Counter 1 interrupt enable	R/W	0
0	TC0IE	Timer/Counter 0 interrupt enable	R/W	0

0xBD01_0058 **Clock Division Base Register (CDBR)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		DivFactor															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
15-0	DivFactor	The divide factor of clock source. If the DivFactor is N, the watchdog timer is divided by N+1. This value cannot be 0 in timer or watchdog mode. The clock source is 22MHz.	R/W	0

0xBD01_005C **Watchdog Control Register (WDTCNR)**

31	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		(Reserved)					OVSEL		WDTCLR	WDTE							

Reset: 0x00A5

Bit	Bit Name	Description	R/W	InitVal
10-9	OVSEL	Overflow select. These bits specify the overflow condition when the watchdog timer counts to the value. 00 = 2^{13} 01 = 2^{14} 10 = 2^{15} 11 = 2^{16}	R/W	00
8	WDTCLR	Watchdog clear. Write a 1 to clear the watchdog counter. It is auto cleared after the write.	W	0
7-0	WDTE	Watchdog enable. When these bits are set to 0xA5, the watchdog timer stops. Other value can enable the watchdog timer and cause a system reset when an overflow signal occurs.	W	0xA5

0xBD01_0060 **Timer/Counter 0 Data register (TC0DATA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)								TC0Data																							

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
23-0	TC0Data	Timer/Counter 0 data register. It specifies the time-out duration.	R/W	0

0xBD01_0064 **Timer/Counter 1 Data register (TC1DATA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)								TC1Data																							

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
23-0	TC1Data	Timer/Counter 1 data register. It specifies the time-out duration.	R/W	0

0xBD01_0068 **Timer/Counter 2 Data register (TC2DATA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC2Data																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	TC2Data	Timer/Counter 2 data register. It specifies the time-out duration.	R/W	0

0xBD01_006C **Timer/Counter 3 Data register (TC3DATA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC3Data																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	TC3Data	Timer/Counter 3 data register. It specifies the time-out duration.	R/W	0

0xBD01_0070 **Timer/Counter 0 Counter register (TC0CNT)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)								TC0Value																							

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
23-0	TC0Value	The timer or counter initial value	R/W	0

0xBD01_0074 **Timer/Counter 1 Counter register (TC1CNT)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)								TC1Value																							

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
23-0	TC1Value	The timer or counter initial value	R/W	0

0xBD01_0078 **Timer/Counter 2 Counter register (TC2CNT)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC2Value																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	TC2Value	The timer or counter initial value	R/W	0

0xBD01_007C **Timer/Counter 3 Counter register (TC3CNT)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC3Value																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	TC3Value	The timer or counter initial value	R/W	0

12. GPIO Control

RTL8186 provides seven sets of GPIO pins – PortA , PortB, PortC, PortD, PortE, PortF, and PortG. Every GPIO pin can be configured as input or output pins via register **PxDIR.** Register **PxDATA** could be used to control the signals (high or low) of GPIO pins. Only the GPIO PortA and PortF have dedicated pins, the others are shared pins with other functions. Following table illustrates the GPIO PortX pin-out and their mux-ed function pins.

GPIO Group Pins	Shared Function Pins	Available Package	Control Mechanism
GPBPIN[0] GPBPIN[1]	CTS0PIN RTS0PIN	Both	In 208 QFP package: ICFG[12] = 1 and ICFG[11] = 0 to enable the GPIOB function, else disable GPIOB. In 256 BGA package: ICFG[12] = 1 to enable the GPIOB function, else disable GPIOB.
GPBPIN[2] GPBPIN[3]	SIN0PIN SOUT0PIN	Both	In both package, ICFG[12] = 1 to enable the GPIOB function, else disable GPIOB.
GPCPIN[0] GPCPIN[1] GPCPIN[2] GPCPIN[3] GPCPIN[4] GPCPIN[5] GPCPIN[6] GPCPIN[7] GPCPIN[8] GPCPIN[9] GPCPIN[10] GPCPIN[11] GPCPIN[12] GPCPIN[13] GPCPIN[14] GPCPIN[15]	MDPIN[16] MDPIN[17] MDPIN[18] MDPIN[19] MDPIN[20] MDPIN[21] MDPIN[22] MDPIN[23] MDPIN[24] MDPIN[25] MDPIN[26] MDPIN[27] MDPIN[28] MDPIN[29] MDPIN[30] MDPIN[31]	Both	In both package, ICFG[13] = 1 to enable the GPIOC function, else disable GPIOC.
GPDPIN[0]	WRXCPIN	Both	In both package, SYSCFG[14] = 1 to enable GPIOD function, else disable GPIOD
GPDPIN[1] GPDPIN[2] GPDPIN[3] GPDPIN[4]	WRXDPIN[0] WRXDPIN[1] WRXDPIN[2] WRXDPIN[3]	Both	In 208 QFP package: SYSCFG[14] = 1 and SYSCFG[10] = 0 to enable GPIOD function, else disable GPIOD. In 256 BGA package: SYSCFG[14] = 1 to enable GPIOD function, else disable GPIOD.
GPDPIN[5] GPDPIN[6] GPDPIN[7]	WRXDVPIN WTXCPIN WTXEPIN	Both	In both package, SYSCFG[14] = 1 to enable GPIOD function, else disable GPIOD

GPDPIN[8] GPDPIN[9] GPDPIN[10] GPDPIN[11] GPDPIN[12] GPDPIN[13] GPDPIN[14]	WTXDPIN[0] WTXDPIN[1] WTXDPIN[2] WTXDPIN[3] WCOLPIN WMDIOPIN WMDCPIN		
GPEPIN[0] GPEPIN[1] GPEPIN[2] GPEPIN[3] GPEPIN[4] GPEPIN[5] GPEPIN[6]	MCSPIN[4] MCSPIN[5] NAFCLEPIN NAFALEPIN NAFWEBPIN NAFREBPIN NAFBUSYBPIN	Both	In both package, SYSCFG[15] = 1 to enable GPIOE function, else disable GPIOE
GPGPIN[0] GPGPIN[1] GPGPIN[2] GPGPIN[3] GPGPIN[4] GPGPIN[5] GPGPIN[6] GPGPIN[7] GPGPIN[8] GPGPIN[9] GPGPIN[10] GPGPIN[11] GPGPIN[12] GPGPIN[13] GPGPIN[14] GPGPIN[15] GPGPIN[16] GPGPIN[17] GPGPIN[18] GPGPIN[19] GPGPIN[20] GPGPIN[21] GPGPIN[22] GPGPIN[23] GPGPIN[24] GPGPIN[25] GPGPIN[26] GPGPIN[27] GPGPIN[28] GPGPIN[29] GPGPIN[30] GPGPIN[31]	PCIADPIN[0] PCIADPIN[1] PCIADPIN[2] PCIADPIN[3] PCIADPIN[4] PCIADPIN[5] PCIADPIN[6] PCIADPIN[7] PCIADPIN[8] PCIADPIN[9] PCIADPIN[10] PCIADPIN[11] PCIADPIN[12] PCIADPIN[13] PCIADPIN[14] PCIADPIN[15] PCIADPIN[16] PCIADPIN[17] PCIADPIN[18] PCIADPIN[19] PCIADPIN[20] PCIADPIN[21] PCIADPIN[22] PCIADPIN[23] PCIADPIN[24] PCIADPIN[25] PCIADPIN[26] PCIADPIN[27] PCIADPIN[28] PCIADPIN[29] PCIADPIN[30] PCIADPIN[31]	256 BGA	In 256 BGA package, SYSCFG[16] = 1 to enable GPIOG, else disable GPIOG.

Register Summary

Virtual address	Size (byte)	Name	Description	Access
0xBD01_0120	4	GPABDATA	Port A/B data register	R/W
0xBD01_0124	4	GPABDIR	Port A/B direction register	R/W
0xBD01_0128	4	GPABIMR	Port A/B interrupt mask register	R/W
0xBD01_012C	4	GPABISR	Port A/B interrupt status register	R/W
0xBD01_0130	4	GPCDDATA	Port C/D data register	R/W
0xBD01_0134	4	GPCDDIR	Port C/D direction register	R/W
0xBD01_0138	4	GPCDIMR	Port C/D interrupt mask register	R/W

0xBD01_013C	4	GPCDISR	Port C/D interrupt status register	R/W
0xBD01_0140	4	GPEFDATA	Port E/F data register	R/W
0xBD01_0144	4	GPEFDIR	Port E/F direction register	R/W
0xBD01_0148	4	GPEFIMR	Port E/F interrupt mask register	R/W
0xBD01_014C	4	GPEFISR	Port E/F interrupt status register	R/W
0xBD01_0150	4	GPGDATA	Port G data register	R/W
0xBD01_0154	4	GPGDIR	Port G direction register	R/W
0xBD01_0158	4	GPGIMR	Port G interrupt mask register	R/W
0xBD01_015C	4	GPGISR	Port G interrupt status register	R/W

0xBD01_0120 **GPIO Port A/B DATA Register (GPABDATA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)												DATAB(R)				(Reserved)					DATAA(R)										
(Reserved)																					DATAA(W)							DATAA/B(W)		

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
19-16	DATAB	Pin data of Port B	R	00
10-0	DATAA	Pin data of Port A	R	00
10-0	DATAA	Pin data of Port A	W	
3-0	DATAB	Pin data of Port B	W	

Please note, the read/write address of GPIO port A/B is different, and set GPIO port A[3:0] and GPIO port B[3:0] as output pin in the same time is inhibited.

0xBD01_0124 **GPIO Port A/B Direction Register (GPABDIR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)												DRCB(R)				(Reserved)					DRCA(R)										
(Reserved)																					DRCA(W)							DRCA/B(W)		

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
19-16	DRCB	Pin direction configuration of Port B 0 = configured as input pin 1 = configured as output pin	R	00
10-0	DRCA	Pin direction configuration of Port A 0 = configured as input pin 1 = configured as output pin	R	00
10-0	DRCA	Pin direction configuration of Port A 0 = configured as input pin 1 = configured as output pin	W	
3-0	DRCB	Pin direction configuration of Port B 0 = configured as input pin 1 = configured as output pin	W	

0xBD01_0128 **GPIO Port A/B Interrupt Mask Register (GPABIMR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)												BIMR(R)				(Reserved)					AIMR(R)										
(Reserved)																					AIMR(W)							A/BIMR(W)		

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal

19-16	BIMR	PortB interrupt enable 0 = disable interrupt 1 = enable interrupt	R	00
10-0	AIMR	PortA interrupt enable 0 = disable interrupt 1 = enable interrupt	R	00
10-0	AIMR	PortA interrupt enable 0 = disable interrupt 1 = enable interrupt	W	
3-0	BIMR	PortB interrupt enable 0 = disable interrupt 1 = enable interrupt	W	

0xBD01_012C **GPIO Port A/B Interrupt Status Register (GPABISR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)												BISR(R)				(Reserved)					AISR(R)										
(Reserved)																					AISR(W)							A/BISR(W)		

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
19-16	BISR	GPIO B interrupt pending status.	R	0
15-0	AISR	GPIO A interrupt pending status.	R	0
15-0	AISR	GPIO A interrupt pending status. Write ‘1’ to clear interrupt pending status.	W	
3-0	BISR	GPIO B interrupt pending status. Write ‘1’ to clear interrupt pending status.	W	

0xBD01_0130 **GPIO Port C/D DATA Register (GPCDDATA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	DATAD(R)															DATAC(R)															
RSVD	Reserved															DATAC/D(W)															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
30-16	DATAD	Pin data of Port D	R	00
15-0	DATAC	Pin data of Port C	R	00
15-0	DATAC/D	Pin data of Port C/D	W	

Please note, the read/write address of GPIO port C/D is different, and set GPIO port C[15:0] and GPIO port D[15:0] as output pin in the same time is inhibited.

0xBD01_0134 **GPIO Port C/D Direction Register (GPCDDIR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	DRCD(R)															DRCC(R)															

RSVD	Reserved	DRCC/D(W)

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
30-16	DRCD	Pin direction configuration of Port D 0 = configured as input pin 1 = configured as output pin	R	00
15-0	DRCC	Pin direction configuration of Port C 0 = configured as input pin 1 = configured as output pin	R	00
15-0	DRCC/D	Pin direction configuration of Port C/D 0 = configured as input pin 1 = configured as output pin	W	

0xBD01_0138 **GPIO Port C/D Interrupt Mask Register (GPCDIMR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	DIMR(R)															CIMR(R)															
RSVD	Reserved															C/DIMR(W)															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
30-16	DIMR	PortD interrupt enable 0 = disable interrupt 1 = enable interrupt	R	0
15-0	CIMR	PortC interrupt enable 0 = disable interrupt 1 = enable interrupt	R	0
15-0	C/DIMR	PortC/D interrupt enable 0 = disable interrupt 1 = enable interrupt	W	

0xBD01_013C **GPIO Port C/D Interrupt Status Register (GPCDISR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DISR(R)															CISR(R)															
	Reserved															C/DISR(W)															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
30-16	DISR	GPIO D interrupt pending status.	R	0
15-0	CISR	GPIO C interrupt pending status.	R	0
15-0	C/DISR	GPIO C/D interrupt pending status. Write '1' to clear interrupt pending status.	W	

0xBD01_0140 **GPIO Port E/F DATA Register (GPEFDATA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

(Reserved)	DATAF(R)	(Reserved)	DATAE(R)
(Reserved)			DATAE/F(W)

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
21-16	DATAF	Pin data of Port F	R	00
6-0	DATAE	Pin data of Port E	R	00
6-0	DATAE/F	Pin data of Port E/F	W	

Please note, the read/write address of GPIO port E/F is different, and set GPIO port E[6:0] and GPIO port F[6:0] as output pin in the same time is inhibited.

0xBD01_0144 **GPIO Port E/F Direction Register (GPEFDIR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																										DRCF(R/W)					
																									DRCE(R/W)					

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
5-0	DRCF	Pin direction configuration of Port F 0 = configured as input pin 1 = configured as output pin	R/W	00
6-0	DRCE	Pin direction configuration of Port E 0 = configured as input pin 1 = configured as output pin	R/W	00

0xBD01_0148 **GPIO Port E/F Interrupt Mask Register (GPEFIMR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)										FIMR(R)						(Reserved)									EIMR(R)						
(Reserved)																									E/FIMR(W)						

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
21-16	FIMR	PortF interrupt enable 0 = disable interrupt 1 = enable interrupt	R	00
6-0	EIMR	PortE interrupt enable 0 = disable interrupt 1 = enable interrupt	R	00
6-0	E/FIMR	PortE interrupt enable 0 = disable interrupt 1 = enable interrupt	W	

0xBD01_014C **GPIO Port E/F Interrupt Status Register (GPEFISR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)										FISR(R)						(Reserved)									EISR(R)						
(Reserved)																									E/FISR(W)						

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal

21-16	FISR	GPIO F interrupt pending status.	R	0
6-0	EISR	GPIO E interrupt pending status.	R	0
6-0	E/EISR	GPIO F/E interrupt pending status. Write '1' to clear interrupt pending status.	W	0

0xBD01_0150 **GPIO Port G DATA Register (GPGDATA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATAG																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	DATAG	Pin data of Port G	R/W	00

0xBD01_0154 **GPIO Port G Direction Register (GPGDIR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRCG																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	DRCG	Pin direction configuration of Port G 0 = configured as input pin 1 = configured as output pin	R/W	0

0xBD01_0158 **GPIO Port G Interrupt Mask Register (GPGIMR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GIMR																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	GIMR	PortG interrupt enable 0 = disable interrupt 1 = enable interrupt	R/W	00

0xBD01_015C **GPIO Port G Interrupt Status Register (GPGISR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GISR																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	GISR	GPIO G interrupt pending status. Write '1' to clear interrupt pending status.	R/W	0

13. IPSec Crypto Engine

The RTL8186 implements an AES/DES/3DES/HMAC-SHA-1/HMAC-MD5 crypto engine to accelerate the packet processing speed when IPSec is enabled within communication protocol. These crypto algorithms can be applied to AH or ESP protocol according to the requirement of security policy. The security engine uses descriptor based access mechanism to service software request. Two descriptor rings are implemented, one called as Source Crypto Descriptors, specifying the source data for encryption/ decryption, and the other one is Destination Crypto Descriptor, defining the output data of

encryption/decryption.

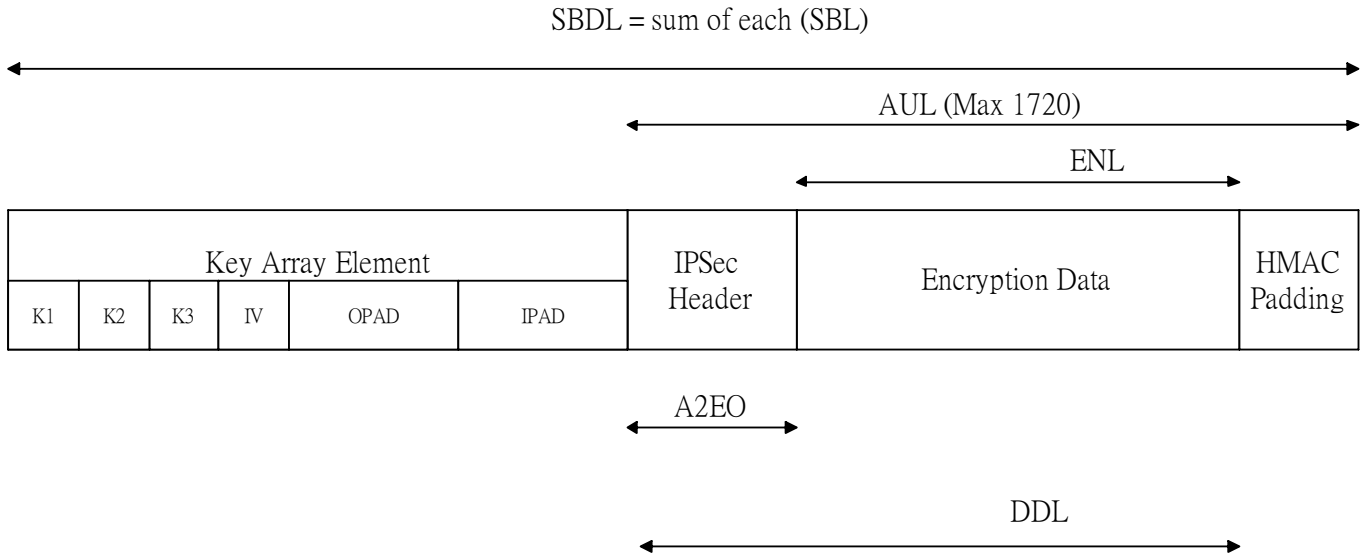
The Crypto Engine supports AES/DES/3DES algorithm to operate in both of the two modes: Electronic Code Block (ECB) and Cipher Block Chaining (CBC). The mode applied to the algorithm was specified at descriptor field.

The Crypto Engine supports IV and Key management in descriptor-based manner, these IV and keys are well-organized data structure named Key Array Element. The Crypto Engine loads the keys and IV from the first descriptor of the packet, which the FS field is '1'. The key array resided at system memory and has no alignment limitation.

To accommodate the fragmentation in IP standard, the Destination Crypto Descriptor supports fragment gathering DMA behavior. The cipher text can overwrite plaintext by setting DDBP field in Destination Crypto Descriptor identical to the SDBP in Source Crypto Descriptor. Number of the Destination Crypto Descriptors is limited to 64, but it is unlimited in the descriptor number of Source Crypto Descriptor.

Descriptor Data Structures used in Crypto Engine

■ Payload format diagram



■ Source Crypto Descriptor

31	30	29	28	27	26 25 24 23 22 21 20 19 18 17 16	15 14	13	12	11	10 9 8 7 6 5 4 3 2 1 0	
OWN	RSVD	FS	LS	RSVD	Authentication Length, AUL (11 bits)	MS (2 bit)	MD5	3DES	AES	Destination DMA Length, DDL (11 bits)	Offset 0
Destination Descriptor Index, DDI (8 bits)					Authentication to Encryption Offset, A2EO (8 bits)	KAM (3 bits)		CBC	RSVD	Encryption Length, ENL (11 bits)	Offset 4
Source Data Buffer Pointer, SDBP											Offset 8

RSVD (5 bits)	Source Buffer DMA Length, SBDL (11 bits)	RSVD (5 bits)	Source Buffer Length, SBL (11 bits)	Offset 12
Next Descriptor Address Pointer, NDAP				Offset 16

Offset#	Bit#	Symbol	Description
0	31	OWN	When set, indicates that the Source Crypto Descriptor is owned by IPSec Crypto Engine. When cleared, indicates that the Source Crypto Descriptor is owned by host system. IPSec Crypto Engine clears this bit when the relative buffer data is already encrypted or decrypted. **Value** / **Meaning** 0 – Descriptor own by host system 1 – Descriptor own by IPSec
0	30	RSVD	Reserved.
0	29	FS	First Segment. **Value** / **Meaning** 1 – This is the first Source Crypto Descriptor of an IP packet; the SDBP pointes to the physical address of Key Array Element of this packet. 0 – This is NOT the first Source Crypto Descriptor of an IP Packet.
0	28	LS	Last Segments. **Value** / **Meaning** 1 – This is the last Source Crypto Descriptor of the packet. 0 – This is NOT the last Source Crypto Descriptor of the packet.
0	26-16	AUL	Authentication Length. If authentication algorithm such as SHA-1/MD5 is applied, this is the byte length that the authentication algorithm should process.
0	15-14	MS	Mode Select. **Value** / **Meaning** 00 – Use DES or 3DES ESP algorithm. 01 – Use SHA-1 or MD5 AH algorithm. 10 – SHA-1/MD5 then DES/3DES 11 – DES/3DES then SHA-1/MD5
0	13	MD5	MD5 algorithm selected. ‘1’: Use MD5 in AH algorithm. ‘0’: Use SHA-1 in AH algorithm.
0	12	3DES	3DES algorithm selected. Effective only when AES bit is ‘0’. ‘1’: Use 3DES in ESP algorithm. ‘0’: Use DES in ESP algorithm.
0	11	AES	AES algorithm selected. Apply Encrypt/Decrypt (depends on AESAG) algorithm to do ESP.

			‘1’: Use AES in ESP algorithm. ‘0’: Use DES or 3DES (depends on 3DES filed) in ESP algorithm.
0	10-0	DDL	Destination Data Length. This value is the length of the write-back packet that processed by the crypto engine.
4	31-24	DDI	Destination Descriptor Index. This is an index value used to identify the relationship of Source Crypto Descriptor and Destination Crypto Descriptor. When the crypto engine processed the Source Crypto Descriptor, it would write this index value back to the current Destination Crypto Descriptor that crypto engine consumed.
4	23-16	A2EO	Authentication to Encryption Offset. This is the byte-offset value between the data applied to authentication and encryption. This value must be 4-byte aligned.
4	15-13	KAM	Key Applied Mechanism. This field specified the mechanism used when 3DES encryption is selected. **Value** / **Meaning** 000 – Decrypt with K1, K2, K3 010 – Decrypt with K1, encrypt with K2, decrypt with K3 101 – Encrypt with K1, decrypt with K2, encrypt with K3 111 – Encrypt with K1, K2, K3 K1, K2, and K3 are Key1, Key2, Key3 used in 3DES algorithm.
2	12	CBC	CBC mode in 3DES algorithm selected. ‘1’: Use CBC mode in 3DES ESP algorithm. ‘0’: Use EBC in 3DES ESP algorithm.
2	11	RSVD	Reserved..
4	10-0	ENL	Encryption data Length. This is the length of encryption data in byte.
8	31-0	SDBP	Source Data Buffer Pointer. This pointer points to the physical address of source data buffer. If FS = ‘1’, this pointer points to the Key Array Element of the packet.
12	26-16	SBDL	Source Buffer DMA Length. This field takes effect only when FS field is set to ‘1’. SBDL is the DMA byte count of a packet, which may comprise from several descriptors.
12	10-0	SBL	Source Buffer Length. This is the length of source data buffer in byte in each descriptor.
16	31-0	NXTDA	Next Descriptor Address. This is the physical address pointer to next descriptor. If This field contains all zero, then this is the end of the descriptor list.

■ Destination Crypto Descriptor (OWN = 1)

31	30	29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0	
OWN = 1	EOR	Reserved (19 bits)	Destination Buffer Length, DBL (11 bits)	Offset 0
Reserved				Offset 4

Destination Data Buffer Pointer, DDBP	Offset 8
Reserved	Offset 12
Reserved	Offset 16
Reserved	Offset 20
Reserved	Offset 24
Reserved	Offset 28

Offset#	Bit#	Symbol	Description
0	31	OWN	When set, indicates that the Destination Crypto Descriptor is owned by IPSec Crypto Engine. When cleared, indicates that the Destination Crypto Descriptor is owned by host system. IPSec Crypto Engine clears this bit when the destination buffer is filled with encrypted or decrypted data.
0	30	EOR	End Of Ring. When set, indicates this descriptor is at the end of the descriptor ring.
0	10-0	DBL	Destination Buffer Length. This is the available length of destination buffer in this descriptor.
8	31-0	DDBP	Destination Data Buffer Pointer. This is the destination data buffer physical starting address.

■ Destination Crypto Descriptor (OWN = 0)

31	30	29	28	27	26 25 24 23 22 21 20 19 18 17 16	15 14	13	12	11	10 9 8 7 6 5 4 3 2 1 0	
OWN	EOR	FS	LS	RSVD	Authentication Length, AUL (11 bits)	MS (2 bit)	MD5	3DES	RSVD	Destination DMA Length, DDL (11 bits)	Offset 0
Destination Descriptor Index, DDI (8 bits)					Authentication to Encryption Offset, A2EO (8 bits)	KAM (3 bits)		CBC	RSVD	Encryption Length, ENL (11 bits)	Offset 4
Destination Data Buffer Pointer, DDBP											Offset 8
ICV (for SHA-1, ICV = 160 bits; for MD5, ICV = 128 bits)											Offset 12 Offset 16 Offset 20

Offset 24 Offset 28

Offset#	Bit#	Symbol	Description
0	31	OWN	When set, indicates that the Destination Crypto Descriptor is owned by IPSec Crypto Engine. When cleared, indicates that the Destination Crypto Descriptor is owned by host system. IPSec Crypto Engine clears this bit when the relative buffer data is already encrypted or decrypted. **Value** / **Meaning** 0 – Descriptor own by host system 1 – Descriptor own by IPSec
0	30	EOR	End of descriptor Ring. When set, this is the last descriptor of the ring.
0	29	FS	First Segment. **Value** / **Meaning** 1 – This is the first Destination Crypto Descriptor of an IP packet. 0 – This is NOT the first Destination Crypto Descriptor of an IP Packet.
0	28	LS	Last Segments. **Value** / **Meaning** 1 – This is the last Destination Crypto Descriptor of the packet. 0 – This is NOT the last Destination Crypto Descriptor of the packet.
0	26-16	AUL	Authentication Length. If authentication algorithm such as SHA-1/MD5 is applied, this is the byte length that the authentication algorithm had processed.
0	15-14	MS	Mode Select. **Value** / **Meaning** 00 – Use DES or 3DES ESP algorithm. 01 – Use SHA-1 or MD5 AH algorithm. 10 – SHA-1/MD5 then DES/3DES 11 – DES/3DES then SHA-1/MD5
0	13	MD5	MD5 algorithm selected. ‘1’: Use MD5 in AH algorithm. ‘0’: Use SHA-1 in AH algorithm.
0	12	3DES	3DES algorithm selected. ‘1’: Use 3DES in ESP algorithm. ‘0’: Use DES in ESP algorithm.
0	10-0	DDL	Destination Data Length. This value is the length of the write-back packet that processed by the crypto engine.
4	31-24	DDI	Destination Descriptor Index. This value is copied from Source Crypto Descriptor that output to this destination descriptor.
4	23-16	A2EO	Authentication to Encryption Offset. This is the byte-offset value between the data applied to authentication and encryption. This value must be 4-byte aligned.
4	15-13	KAM	Key Applied Mechanism. This field specified the mechanism used when

			3DES encryption is selected. **Value** / **Meaning** 000 – Decrypt with K1, K2, K3 010 – Decrypt with K1, encrypt with K2, decrypt with K3 101 – Encrypt with K1, decrypt with K2, encrypt with K3 111 – Encrypt with K1, K2, K3 K1, K2, and K3 are Key1, Key2, Key3 used in 3DES algorithm.
4	12	CBC	CBC mode in 3DES algorithm selected. '1': Use CBC mode in 3DES ESP algorithm. '0': Use EBC in 3DES ESP algorithm.
4	10-0	ENL	Encryption data Length. This is the length of encrypted data in byte.
8	31-0	DDBP	Destination Data Buffer Pointer. This pointer points to the physical address of destination data buffer.
12-31	31-0	ICV	Integrity Check Value. This is the result of HMAC-SHA-1 or HMAC-MD5. If SHA-1 is used, the length of ICV is 160 bits. If MD5 is used, the length of ICV is 128 bits.

■ Key Array Element

K1L, Key 1 Left Part	Offset 0
K1R, Key 1 Right Part	Offset 4
K2L, Key 2 Left Part	Offset 8
K2R, Key 2 Right Part	Offset 12
K3L, Key 3 Left Part	Offset 16
K3R, Key 3 Right Part	Offset 20
IVL, IV Left Part	Offset 24
IVR, IV Right Part	Offset 28
OPAD	Offset 32-95
IPAD	Offset 96-159

Offset#	Bit#	Symbol	Description
0	31-0	K1L	3DES/DES: Key 1 Left Part. AES: First four bytes of the key Note: For AES decryption, the key is the decryption round 1 key.
4	31-0	K1R	3DES/DES: Key 1 Right Part. AES: Second four bytes of the key. Note: For AES decryption, the key is the decryption round 1 key.
8	31-0	K2L	3DES: Key 2 Left Part. AES: Third four bytes of the key.

			Note: For AES decryption, the key is the decryption round 1 key.
12	31-0	K2R	3DES: Key 2 Right Part. AES: Fourth four bytes of the key. Note: For AES decryption, the key is the decryption round 1 key.
16	31-0	K3L	3DES: Key 3 Left Part. AES: First four bytes of the IV.
20	31-0	K3R	3DES: Key 3 Right Part. AES: Second four bytes of the IV.
24	31-0	IVL	3DES/DES: IV Left Part. AES: Third four bytes of the IV.
28	31-0	IVR	3DES/DES: IV Right Part. AES: Fourth four bytes of the IV.
32-95	31-0	OPAD	In SHA-1/MD5, these 64 bytes are output padding XOR-ed with key.
96-159	31-0	IPAD	In SHA-1/MD5, these 64 bytes are input padding XOR-ed with key.

Register Summary

Virtual address	Size (byte)	Name	Description	Access
0xBD10_0000	4	IPSSDAR	IPSec Source Descriptor Starting Address Register	R/W
0xBD10_0004	4	IPSDDAR	IPSec Destination Descriptor Starting Address Register	R/W
0xBD10_0008	1	IPSCFR	IPSec Configuration Register	R/W
0xBD10_0009	1	IPSCR	IPSec Command Register	R/W
0xBD10_000A	1	IPSIMR	IPSec Interrupt Mast Register	R/W
0xBD10_000B	1	IPSISR	IPSec Interrupt Status Register	R/W
0xBD10_000C	4	IPSCTR	IPSec Control Register	R/W

0xBD10_0000 **IPSec Source Descriptor Starting Address Register (IPSSDAR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDSA																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	SDSA	Source Descriptor Starting Address. This is the physical address of first available Source Crypto Descriptor. The address should be 256 byte aligned.	R/W	0

0xBD10_0004 **IPSec Destination Descriptor Starting Address Register (IPSDDAR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDSA																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	DDSA	Destination Descriptor Starting Address. This is the physical address of first available Destination Crypto Descriptor.	R/W	0

0xBD10_0008 **IPSec Configuration Register (IPSCFR)**

31	8	7	6	5	4	3	2	1	0

RSVD		CFE	LBKM	CKE	CEE

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
3	CFE	Configuration Register Enable. Set '1' to enable the configuration to IPSCTR register.	R/W	0
2	LBKM	Loopback mode enable. Set '1' to enable loop mode of the crypto engine. This will override the command setting in the descriptor.	R/W	0
1	CKE	Clock Enable. Set '1' to enable the crypto engine clock.	R/W	0
0	CEE	Crypto Engine Enable. Set '1' to enable the crypto engine.	R/W	0

0xBD10_0009 **IPSec Command Register (IPSCR)**

31 ... 8	7	6	5	4	3	2	1	0
Reserved								POLL

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
0	POLL	Descriptor Polling. Set this bit to '1' will kick the crypto engine to fetch the first Source Descriptor pointed by IPSSDAR register.	R/W	0

0xBD10_000A **IPSec Interrupt Mask Register (IPSIMR)**

31 ... 8	7	6	5	4	3	2	1	0
						SBFE	DDUE	DDOK

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
2	SBFE	Source Buffer Full Error Interrupt Mask. 1: Enable 0: Disable	R/W	0
1	DDUE	Destination Descriptor Unavailable Error Interrupt Mask. 1: Enable 0: Disable	R/W	0
0	DDOK	Destination Descriptor OK Interrupt Mask. 1: Enable 0: Disable	R/W	0

0xBD10_000B **IPSec Interrupt Status Register (IPSISR)**

31 ... 8	7	6	5	4	3	2	1	0
						SBFE	DDUE	DDOK

Reset: 0x00

Bit	Bit Name	Description	R/W	InitVal
2	SBFE	Source Buffer Full Error Interrupt. Write '1' to clear.	R/W	0
1	DDUE	Destination Descriptor Unavailable Error Interrupt. Write '1' to clear.	R/W	0
0	DDOK	Destination Descriptor OK Interrupt. Write '1' to clear.	R/W	0

0xBD10_000C **IPSec Control Register (IPSCTR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CKS		Reserved						BR	BIST	RSVD	DETS			RSVD	DMBS			Reserved					SMBS		

Reset: 0x0300_0000

Bit	Bit Name	Description	R/W	InitVal
25-24	CKS	Crypto engine Clock Source Select. 00: 80 MHz crypto clock 01: 100 MHz crypto clock 10: 120 MHz crypto clock 11: Bus clock crypto clock	R/W	11
17	BR	BIST Result. '1': BIST success. '0': BIST fail.	R/W	0
16	BIST	Crypto engine internal RAM BIST enable. Set '1' to enable BIST, when BIST complete, this bit will cleared to '0' and the BR bit indicates the result.	R/W	0
14-12	DETS	Destination Early DMA Threshold Size.	R/W	111
10-8	DMBS	Destination DMA Maximum Burst Size. 000: 16 Byte 001: 32 Byte 010: 64 Byte 011: 128 Byte 1XX: Reserved.	R/W	010
2-0	SMBS	Source DMA Maximum Burst Size. 000: 16 Byte 001: 32 Byte 010: 64 Byte 011: 128 Byte 1XX: Reserved.	R/W	010

14. MIC Calculator

To offload the computation task of CPU, RTL8186 integrates a TKIP-Michael hardware calculator. Register MICLVAL and MICRVAL are used to set the key of TKIP-Michael. After calculated, these two registers will store the output MIC value.

Beside the MIC engine, the calculator also embedded with a PRNG (Pseudo Random Number Generator) to provide uniform distributed random number. To use the PRNG, you may write an initial number into MICPRNR register as a seed number, and then read back the MICPRNR value as the output random number.

Register Summary

Virtual address	Size (byte)	Name	Description	Access
0xBD18_0000	4	MICLVAL	MIC L value register	R/W
0xBD18_0004	4	MICRVAL	MIC R value register	R/W
0xBD18_0008	4	MICSAR	MIC calculation starting address register	R/W
0xBD18_000C	4	MICLENR	MIC calculation length register	R/W

0xBD18_0010	4	MICDMAR	MIC calculation DMA length register	R/W
0xBD18_0014	4	MICCR	MIC control register	R/W
0xBD18_0018	4	MICPRNR	MIC Pseudo Random Number Generator register	R/W

0xBD18_0000 **MIC L Value Register (MICLVAL)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LVal																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	LVal	MIC L value register. The initial L value is written to this register; when calculation done, read this register for new L value.	R/W	0

0xBD18_0004 **MIC R Value Register (MICRVAL)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RVal																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	RVal	MIC R value register. The initial R value is written to this register; when calculation done, read this register for new R value.	R/W	0

0xBD18_0008 **MIC Starting Address Register (MICSAR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SADDR																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	SADDR	The physical address of the data that MIC calculator is going to do calculation. The address has no alignment restriction.	R/W	0

0xBD18_000C **MIC Calculation Length Register (MICLENR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TLEN																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	TLEN	The data length that MIC calculator is going to do calculation.	R/W	0

0xBD18_0010 **MIC Calculation DMA Length Register (MICDMAR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLEN																															

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-0	DLEN	The DMA length that MIC calculator is going to	R/W	0

		do calculation. The relation between data length (LEN) and DMA length (DLEN) is: DLEN = (TLEN/4 + 2)*4		

0xBD18_0014 **MIC Control Register (MICCR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																							IS	(Reserved)						IEN	RUN

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
8	IS	Interrupt Status. When MIC calculation is done, this bit is set to ‘1’. Write ‘1’ to clear the status.	R/W	0
1	IEN	Interrupt Enable. When MIC calculation is done and this bit is set to ‘1’, the MIC calculator will assert interrupt to CPU. If this bit is not set, only the IS bit is set while calculation done.	R/W	0
0	RUN	MIC Calculator run. Write this bit ‘1’ will trigger the hardware start calculation. When calculation done, this bit auto reset to ‘0’.	R/W	0

0xBD18_0018 **MIC PRNG Register (MICPRNR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRNG																															

Reset: 0x5412_3333

Bit	Bit Name	Description	R/W	InitVal
31-0	PRNG	The Pseudo Random Number Generator. Notice that if write 0 to this register, the PRNG will fail to generate random number.	R/W	0x54123333

15. PCM Controller

The RTL8186 integrates a PCM controller, which supports four channels of voice application and both A-law and u-low compression.

Register Summary

Virtual address	Size (byte)	Name	Description	Access
0xBD28_0000	4	PCMCR	PCM interface Control Register	R/W
0xBD28_0004	4	PCMCHCNR	PCM Channel specific Control Register	R/W
0xBD28_0008	4	PCMTSR	PCM Time Slot Assignment Register	R/W
0xBD28_000C	4	PCMBSIZE	PCM Channels Buffer Size register	R/W
0xBD28_0010	4	CH0TXBSA	PCM Channel 0 TX buffer starting address pointer	R/W
0xBD28_0014	4	CH1TXBSA	PCM Channel 1 TX buffer starting address pointer	R/W
0xBD28_0018	4	CH2TXBSA	PCM Channel 2 TX buffer starting address pointer	R/W
0xBD28_001C	4	CH3TXBSA	PCM Channel 3 TX buffer starting address pointer	R/W
0xBD28_0020	4	CH0RXBSA	PCM Channel 0 RX buffer starting address pointer	R/W
0xBD28_0024	4	CH1RXBSA	PCM Channel 1 RX buffer starting address pointer	R/W
0xBD28_0028	4	CH2RXBSA	PCM Channel 2 RX buffer starting address pointer	R/W
0xBD28_002C	4	CH3RXBSA	PCM Channel 3 RX buffer starting address pointer	R/W
0xBD28_0030	4	PCMIMR	PCM channels Interrupt Mask Register	R/W

0xBD28_0034	4	PCMISR	PCM channels Interrupt Status Register	R/W

0xBD28_0000 **PCM interface Control Register (PCMCR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																			PCME	CKDIR	PXDSE	FSINV	(Reserved)					ICC			

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
12	PCME	PCM interface Enable. While PCM interface is disabled, all logic and registers will reset to initial state. 0: Disable 1: Enable	R/W	0
11	CKDIR	CLK and FS signal source select of PCM interface. 0: External source from Codec 1: From internal PLL (output to Codec)	R/W	0
10	PXDSE	PCM interface extra data strobe enable. 0: Disable extra data strobe 1: Enable extra data strobe	R/W	0
9	FSINV	PCM interface frame synchronization polarity invert. 0: PCMFS set to high active 1: PCMFS set to low active	R/W	0
3-0	ICC	PCM interface channels inter change control. When two channels was set as interchange mode, the channel data received from one channel will auto transfer to another for output, without pass through the internal FIFO. 0001: Channel 0, 1 talk 0010: Channel 0, 2 talk 0011: Channel 0, 3 talk 0100: Channel 1, 2 talk 0101: Channel 1, 3 talk 0110: Channel 2, 3 talk 1001: Channel 0, 1 talk and channel 2, 3 talk 1010: Channel 0, 2 talk and channel 1, 3 talk 1011: Channel 0, 3 talk and channel 1, 2 talk others: No interchange talk function enabled.	R/W	0

0xBD28_0004 **PCM Channel Control Register (PCMCHCNR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			C0ILBE	C0CMPE	CH0UA	CH0TE	CH0RE	RSVD				C1CMPE	CH1UA	CH1TE	CH1RE	RSVD				C2CMPE	CH2UA	CH2TE	CH2RE	RSVD				C3CMPE	CH3UA	CH3TE	CH3RE

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
28	C0ILBE	Channel 0 Internal Loop-back Enable. When loop-back function enabled, the data in TX FIFO transmits to TXD and also the RX FIFO.	R/W	0

		0: Disable loop-back 1: Enable loop-back		
27	C0CMPE	Channel 0 Compander Enable. When channel compander enabled, the 8-bit data from RXD expands to 16 bits and sent to RX FIFO. In the other direction, the compander suppresses 16 bit data from TX FIFO to 8 bits and sent to TXD. 0: Disable 1: Enable	R/W	0
26	CH0UA	Channel 0 u-law/A-law select. 0: u-law 1: A-law	R/W	0
25	CH0TE	Channel 0 Transmitter Enable. 0: Disable 1: Enable	R/W	0
24	CH0RE	Channel 0 Receiver Enable. 0: Disable 1: Enable	R/W	0
19	C1CMPE	Channel 1 Compander Enable. When channel compander enabled, the 8-bit data from RXD expands to 16 bits and sent to RX FIFO. In the other direction, the compander suppresses 16 bit data from TX FIFO to 8 bits and sent to TXD. 0: Disable 1: Enable	R/W	0
18	CH1UA	Channel 1 u-law/A-law select. 0: u-law 1: A-law	R/W	0
17	CH1TE	Channel 1 Transmitter Enable. 0: Disable 1: Enable	R/W	0
16	CH1RE	Channel 1 Receiver Enable. 0: Disable 1: Enable	R/W	0
11	C1CMPE	Channel 1 Compander Enable. When channel compander enabled, the 8-bit data from RXD expands to 16 bits and sent to RX FIFO. In the other direction, the compander suppresses 16 bit data from TX FIFO to 8 bits and sent to TXD. 0: Disable 1: Enable	R/W	0
10	CH2UA	Channel 2 u-law/A-law select. 0: u-law 1: A-law	R/W	0
9	CH2TE	Channel 2 Transmitter Enable. 0: Disable 1: Enable	R/W	0
8	CH2RE	Channel 2 Receiver Enable. 0: Disable 1: Enable	R/W	0
3	C3CMPE	Channel 3 Compander Enable. When channel compander enabled, the 8-bit data from RXD expands to 16 bits and sent to RX FIFO. In the other direction, the compander suppresses 16 bit data from TX FIFO to 8 bits and sent to TXD. 0: Disable 1: Enable	R/W	0
2	CH3UA	Channel 3 u-law/A-law select.	R/W	0

		0: u-law 1: A-law		
1	CH3TE	Channel 3 Transmitter Enable. 0: Disable 1: Enable	R/W	0
0	CH3RE	Channel 3 Receiver Enable. 0: Disable 1: Enable	R/W	0

0xBD28_0008 **PCM Time Slot Assignment Register (PCMTSR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				CH0TSA				RSVD			CH1TSA					RSVD			CH2TSA					RSVD			CH3TSA				

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
28-24	CH0TSA	Channel 0 Time Slot Assignment. CH0TSA[4:0] mapping to Slot 0 .. Slot 31.	R/W	0
20-16	CH1TSA	Channel 1 Time Slot Assignment. CH1TSA[4:0] mapping to Slot 0 .. Slot 31.	R/W	0
12-8	CH2TSA	Channel 2 Time Slot Assignment. CH2TSA[4:0] mapping to Slot 0 .. Slot 31.	R/W	0
4-0	CH3TSA	Channel 3 Time Slot Assignment. CH3TSA[4:0] mapping to Slot 0 .. Slot 31.	R/W	0

0xBD28_000C **PCM Buffer Size Register (PCMBSIZE)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH0BSIZE								CH1BSIZE								CH2BSIZE								CH3BSIZE							

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-24	CH0BSIZE	Channel 0 buffer size in unit of 4(n+1) bytes.	R/W	0x0
23-16	CH1BSIZE	Channel 1 buffer size in unit of 4(n+1) bytes.	R/W	0x0
15-8	CH2BSIZE	Channel 2 buffer size in unit of 4(n+1) bytes.	R/W	0x0
7-0	CH3BSIZE	Channel 3 buffer size in unit of 4(n+1) bytes.	R/W	0x0

0xBD28_0010 **PCM Channel 0 TX Base Address Register (CH0TXBSA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXBUFPR																														P1OWN	P0OWN

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-2	TXBUFPR	TX Buffer Pointer. This is a physical address with word-align limitation.	R/W	0x0
1	P1OWN	Page 1 Own bit 0: Page 1 owned by CPU 1: Page 1 owned by PCM controller	R/W	0x0
0	P0OWN	Page 0 Own bit 0: Page 0 owned by CPU	R/W	0x0

		1: Page 0 owned by PCM controller		

0xBD28_0014 **PCM Channel 1 TX Base Address Register (CH1TXBSA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXBUFPR																														P1OWN	P0OWN

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-2	TXBUFPR	TX Buffer Pointer. This is a physical address with word-align limitation.	R/W	0x0
1	P1OWN	Page 1 Own bit 0: Page 1 owned by CPU 1: Page 1 owned by PCM controller	R/W	0x0
0	P0OWN	Page 0 Own bit 0: Page 0 owned by CPU 1: Page 0 owned by PCM controller	R/W	0x0

0xBD28_0018 **PCM Channel 2 TX Base Address Register (CH2TXBSA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXBUFPR																														P1OWN	P0OWN

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-2	TXBUFPR	TX Buffer Pointer. This is a physical address with word-align limitation.	R/W	0x0
1	P1OWN	Page 1 Own bit 0: Page 1 owned by CPU 1: Page 1 owned by PCM controller	R/W	0x0
0	P0OWN	Page 0 Own bit 0: Page 0 owned by CPU 1: Page 0 owned by PCM controller	R/W	0x0

0xBD28_001C **PCM Channel 3 TX Base Address Register (CH3TXBSA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXBUFPR																														P1OWN	P0OWN

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-2	TXBUFPR	TX Buffer Pointer. This is a physical address with word-align limitation.	R/W	0x0
1	P1OWN	Page 1 Own bit 0: Page 1 owned by CPU 1: Page 1 owned by PCM controller	R/W	0x0
0	P0OWN	Page 0 Own bit 0: Page 0 owned by CPU	R/W	0x0

		1: Page 0 owned by PCM controller		

0xBD28_0020 **PCM Channel 0 RX Base Address Register (CH0RXBSA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXBUFPR																														P1OWN	P0OWN

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-2	RXBUFPR	RX Buffer Pointer. This is a physical address with word-align limitation.	R/W	0x0
1	P1OWN	Page 1 Own bit 0: Page 1 owned by CPU 1: Page 1 owned by PCM controller	R/W	0x0
0	P0OWN	Page 0 Own bit 0: Page 0 owned by CPU 1: Page 0 owned by PCM controller	R/W	0x0

0xBD28_0024 **PCM Channel 1 RX Base Address Register (CH1RXBSA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXBUFPR																														P1OWN	P0OWN

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-2	RXBUFPR	RX Buffer Pointer. This is a physical address with word-align limitation.	R/W	0x0
1	P1OWN	Page 1 Own bit 0: Page 1 owned by CPU 1: Page 1 owned by PCM controller	R/W	0x0
0	P0OWN	Page 0 Own bit 0: Page 0 owned by CPU 1: Page 0 owned by PCM controller	R/W	0x0

0xBD28_0028 **PCM Channel 2 RX Base Address Register (CH2RXBSA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXBUFPR																														P1OWN	P0OWN

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-2	RXBUFPR	RX Buffer Pointer. This is a physical address with word-align limitation.	R/W	0x0
1	P1OWN	Page 1 Own bit 0: Page 1 owned by CPU 1: Page 1 owned by PCM controller	R/W	0x0
0	P0OWN	Page 0 Own bit 0: Page 0 owned by CPU	R/W	0x0

		1: Page 0 owned by PCM controller		

0xBD28_002C **PCM Channel 3 RX Base Address Register (CH3RXBSA)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXBUFPR																														P1OWN	P0OWN

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31-2	RXBUFPR	RX Buffer Pointer. This is a physical address with word-align limitation.	R/W	0x0
1	P1OWN	Page 1 Own bit 0: Page 1 owned by CPU 1: Page 1 owned by PCM controller	R/W	0x0
0	P0OWN	Page 0 Own bit 0: Page 0 owned by CPU 1: Page 0 owned by PCM controller	R/W	0x0

0xBD28_0030 **PCM Interrupt Mask Register (PCMIMR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Reserved)																CH0P0OKIE	CH0P1OKIE	CH0TBUAIE	CH0RBUAIE	CH1P0OKIE	CH1P1OKIE	CH1TBUAIE	CH1RBUAIE	CH2P0OKIE	CH2P1OKIE	CH2TBUAIE	CH2RBUAIE	CH3P0OKIE	CH3P1OKIE	CH3TBUAIE	CH3RBUAIE

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
15	CH0P0OKIE	Channel 0 Page 0 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
14	CH0P1OKIE	Channel 0 Page 1 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
13	CH0TBUAIE	Channel 0 Transmit Buffer Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
12	CH0RBUAIE	Channel 0 Receive Buffer Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
11	CH1P0OKIE	Channel 1 Page 0 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
10	CH1P1OKIE	Channel 1 Page 1 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
9	CH1TBUAIE	Channel 1 Transmit Buffer Unavailable Interrupt Enable. 0: Disable interrupt	R/W	0

		1: Enable interrupt		
8	CH1RBUAIE	Channel 1 Receive Buffer Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
7	CH2P0OKIE	Channel 2 Page 0 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
6	CH2P1OKIE	Channel 2 Page 1 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
5	CH2TBUAIE	Channel 2 Transmit Buffer Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
4	CH2RBUAIE	Channel 2 Receive Buffer Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
3	CH3P0OKIE	Channel 3 Page 0 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
2	CH3P1OKIE	Channel 3 Page 1 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
1	CH3TBUAIE	Channel 3 Transmit Buffer Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0
0	CH3RBUAIE	Channel 3 Receive Buffer Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	R/W	0

0xBD28_0034 **PCM Interrupt Status Register (PCMISR)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH0P0TOK	CH0P1TOK	CH0P0ROK	CH0P1ROK	CH0P0TBU	CH0P1TBU	CH0P0RBU	CH0P1RBU	CH1P0TOK	CH1P1TOK	CH1P0ROK	CH1P1ROK	CH1P0TBU	CH1P1TBU	CH1P0RBU	CH1P1RBU	CH2P0TOK	CH2P1TOK	CH2P0ROK	CH2P1ROK	CH2P0TBU	CH2P1TBU	CH2P0RBU	CH2P1RBU	CH3P0TOK	CH3P1TOK	CH3P0ROK	CH3P1ROK	CH3P0TBU	CH3P1TBU	CH3P0RBU	CH3P1RBU

Reset: 0x0000_0000

Bit	Bit Name	Description	R/W	InitVal
31	CH0P0TOK	Channel 0 Page 0 Transmit OK. 0: Transmit Not OK 1: Transmit OK, write ‘1’ to clear.	R/W	0
30	CH0P1TOK	Channel 0 Page 1 Transmit OK. 0: Transmit Not OK 1: Transmit OK, write ‘1’ to clear.	R/W	0
29	CH0P0ROK	Channel 0 Page 0 Receive OK. 0: Receive Not OK 1: Receive OK, write ‘1’ to clear.	R/W	0
28	CH0P1ROK	Channel 0 Page 1 Receive OK. 0: Receive Not OK 1: Receive OK, write ‘1’ to clear.	R/W	0

27	CH0P0TBU	Channel 0 Page 0 Transmit Buffer Unavailable. 0: Transmit buffer Not unavailable 1: Transmit buffer unavailable, write ‘1’ to clear.	R/W	0
26	CH0P1TBU	Channel 0 Page 1 Transmit Buffer Unavailable. 0: Transmit buffer Not unavailable 1: Transmit buffer unavailable, write ‘1’ to clear.	R/W	0
25	CH0P0RBU	Channel 0 Page 0 Receive Buffer Unavailable. 0: Receive buffer Not unavailable 1: Receive buffer unavailable, write ‘1’ to clear.	R/W	0
24	CH0P1RBU	Channel 0 Page 1 Receive Buffer Unavailable. 0: Receive buffer Not unavailable 1: Receive buffer unavailable, write ‘1’ to clear.	R/W	0
23	CH1P0TOK	Channel 1 Page 0 Transmit OK. 0: Transmit Not OK 1: Transmit OK, write ‘1’ to clear.	R/W	0
22	CH1P1TOK	Channel 1 Page 1 Transmit OK. 0: Transmit Not OK 1: Transmit OK, write ‘1’ to clear.	R/W	0
21	CH1P0ROK	Channel 1 Page 0 Receive OK. 0: Receive Not OK 1: Receive OK, write ‘1’ to clear.	R/W	0
20	CH1P1ROK	Channel 1 Page 1 Receive OK. 0: Receive Not OK 1: Receive OK, write ‘1’ to clear.	R/W	0
19	CH1P0TBU	Channel 1 Page 0 Transmit Buffer Unavailable. 0: Transmit buffer Not unavailable 1: Transmit buffer unavailable, write ‘1’ to clear.	R/W	0
18	CH1P1TBU	Channel 1 Page 1 Transmit Buffer Unavailable. 0: Transmit buffer Not unavailable 1: Transmit buffer unavailable, write ‘1’ to clear.	R/W	0
17	CH1P0RBU	Channel 1 Page 0 Receive Buffer Unavailable. 0: Receive buffer Not unavailable 1: Receive buffer unavailable, write ‘1’ to clear.	R/W	0
16	CH1P1RBU	Channel 1 Page 1 Receive Buffer Unavailable. 0: Receive buffer Not unavailable 1: Receive buffer unavailable, write ‘1’ to clear.	R/W	0
15	CH2P0TOK	Channel 2 Page 0 Transmit OK. 0: Transmit Not OK 1: Transmit OK, write ‘1’ to clear.	R/W	0
14	CH2P1TOK	Channel 2 Page 1 Transmit OK. 0: Transmit Not OK 1: Transmit OK, write ‘1’ to clear.	R/W	0
13	CH2P0ROK	Channel 2 Page 0 Receive OK. 0: Receive Not OK 1: Receive OK, write ‘1’ to clear.	R/W	0
12	CH2P1ROK	Channel 2 Page 1 Receive OK. 0: Receive Not OK 1: Receive OK, write ‘1’ to clear.	R/W	0
11	CH2P0TBU	Channel 2 Page 0 Transmit Buffer Unavailable. 0: Transmit buffer Not unavailable 1: Transmit buffer unavailable, write ‘1’ to clear.	R/W	0
10	CH2P1TBU	Channel 2 Page 1 Transmit Buffer Unavailable. 0: Transmit buffer Not unavailable 1: Transmit buffer unavailable, write ‘1’ to clear.	R/W	0
9	CH2P0RBU	Channel 2 Page 0 Receive Buffer Unavailable. 0: Receive buffer Not unavailable 1: Receive buffer unavailable, write ‘1’ to clear.	R/W	0
8	CH2P1RBU	Channel 2 Page 1 Receive Buffer Unavailable.	R/W	0

		0: Receive buffer Not unavailable 1: Receive buffer unavailable, write ‘1’ to clear.		
7	CH3P0TOK	Channel 3 Page 0 Transmit OK. 0: Transmit Not OK 1: Transmit OK, write ‘1’ to clear.	R/W	0
6	CH3P1TOK	Channel 3 Page 1 Transmit OK. 0: Transmit Not OK 1: Transmit OK, write ‘1’ to clear.	R/W	0
5	CH3P0ROK	Channel 3 Page 0 Receive OK. 0: Receive Not OK 1: Receive OK, write ‘1’ to clear.	R/W	0
4	CH3P1ROK	Channel 3 Page 1 Receive OK. 0: Receive Not OK 1: Receive OK, write ‘1’ to clear.	R/W	0
3	CH3P0TBU	Channel 3 Page 0 Transmit Buffer Unavailable. 0: Transmit buffer Not unavailable 1: Transmit buffer unavailable, write ‘1’ to clear.	R/W	0
2	CH3P1TBU	Channel 3 Page 1 Transmit Buffer Unavailable. 0: Transmit buffer Not unavailable 1: Transmit buffer unavailable, write ‘1’ to clear.	R/W	0
1	CH3P0RBU	Channel 3 Page 0 Receive Buffer Unavailable. 0: Receive buffer Not unavailable 1: Receive buffer unavailable, write ‘1’ to clear.	R/W	0
0	CH3P1RBU	Channel 3 Page 1 Receive Buffer Unavailable. 0: Receive buffer Not unavailable 1: Receive buffer unavailable, write ‘1’ to clear.	R/W	0

16. 802.11a/b/g WLAN Controller

RTL8186 integrates with a wireless LAN MAC and a direct sequence spread spectrum baseband processor. The WLAN controller implements Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and Orthogonal Frequency Division Multiplexing (OFDM) baseband processing to support all IEEE 802.11a, 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available along with complementary code keying to provide data rates of 1, 2, 5.5 and 11Mbps, with long or short preamble. A high speed Fast Fourier Transform (FFT)/Inverse Fast Fourier Transform (IFFT), combined with BPSK, QPSK, 16QAM and 64QAM modulation of the individual subcarriers, provides data rates of 6, 9, 12, 18, 24, 36, 48 and 54Mbps, with rate compatible punctured convolutional coding with a coding rate of 1/2, 2/3 and 3/4.

The WLAN controller also builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate the severe multipath effects. Efficient IQ-imbalance calibration, DC offset, phase noise, frequency offset and timing offset compensation are provided for the radio frequency front-end impairments. Selectable digital transmit and receiver FIR filters are provided to meet the requirement of transmit spectrum mask and to reject the adjacent channel interference, respectively. Both in the transmitter and receiver, programmable scaling in digital domain trades the quantization noise against the increasing probability of clipping. Furthermore, robust signal detection, symbol boundary detection and channel estimation are performed well at the minimum sensitivity.

Besides, it supports fast receiver Automatic Gain Control (AGC) and antenna diversity functions, and adaptive transmit power control function to obtain better performance in the analog portions of the transceiver. It also has on-chip digital-to-analog converters and analog-to-digital converters for analog I and Q inputs and outputs, transmit TSSI and receiver RSSI input, and transmit and receiver AGC outputs.

To support 802.11h, RTL8186 implements a dynamic frequency selection (DFS) and transmit power control (TPC) that could be used to satisfy regulator requirements for operation in the 5GHz band in Europe.

For security issues, RTL8186 has implemented a high performance security engine to support WEP, TKIP and AES encryption/decryption for transmitting and receiving packet.

The WLAN controller is a DMA bus-master device, and uses descriptor-based buffer structure for packet transmission and reception. These features will definitely offload much CPU loading.

RTL8186 provides interfaces for external RF module. Now Realtek RTL8225 (802.11 b/g) and RFL8255 (802.11 a/b/g) RF chipset are supported.

Register Summary

Virtual Address	Size (byte)	Name	Description	RW
0xBD40_0000	8	WLAN_ID	ID Register. The ID register is only permitted to write via 4-byte access. Read access can be byte, word, or double word access.	RW
0xBD40_0008	8	WLAN_MAR	Multicast Register. The MAR register is only permitted to write via 4-byte access. Read access can be byte, word, or double word access.	RW
0xBD40_0018	8	WLAN_TSFTR	Timing Synchronization Function Timer Register.	R
0xBD40_0020	4	WLAN_TLPDA	Transmit Low Priority Descriptors Start Address (32-bit) (256-byte alignment).	RW
0xBD40_0024	4	WLAN_TNPDA	Transmit Normal Priority Descriptors Start Address (32-bit). (256-byte alignment).	RW
0xBD40_0028	4	WLAN_THPDA	Transmit High Priority Descriptors Start Address (32-bit). (256-byte alignment).	RW
0xBD40_002C	4	WLAN_BRSR	Basic Rate Set Register.	RW
0xBD40_002E	6	WLAN_BSSID	Basic Service Set ID.	RW
0xBD40_0034	1	WLAN_RR	Response Rate.	RW
0xBD40_0035	1	WLAN_EIFS	Extended InterFrame Space Time. The value is in units of 4µs.	RW
0xBD40_0037	1	WLAN_CR	Command Register.	RW
0xBD40_003C	2	WLAN_IMR	Interrupt Mask Register.	RW
0xBD40_003E	2	WLAN_ISR	Interrupt Status Register.	RW
0xBD40_0040	4	WLAN_TCR	Transmit (Tx) Configuration Register.	RW
0xBD40_0044	4	WLAN_RCR	Receive (Rx) Configuration Register.	RW
0xBD40_0048	4	WLAN_TINT	Timer Interrupt Register. Once having written a non-zero value to this register, the Timeout bit of the WLAN_ISR register will be set whenever the least 32 bits of the WLAN_TSFTR reaches this value. The Timeout bit will not be set as long as the WLAN_TINT register is zero.	RW
0xBD40_004C	4	WLAN_TBDA	Transmit Beacon Descriptor start Address (32-bit) (256-byte alignment).	RW
0xBD40_0050	1	WLAN_CR	Command Register.	RW
0xBD40_0051	1	WLAN_CONFIG0	Configuration Register 0.	R
0xBD40_0052	1	WLAN_CONFIG1	Configuration Register 1.	RW
0xBD40_0053	1	WLAN_CONFIG2	Configuration Register 2.	RW
0xBD40_0054	4	WLAN_ANAPARM	Analog Parameter.	RW
0xBD40_0058	1	WLAN_MSR	Media Status Register.	RW
0xBD40_0059	1	WLAN_CONFIG3	Configuration Register 3.	RW
0xBD40_005A	1	WLAN_CONFIG4	Configuration Register 4.	RW
0xBD40_005B	1	WLAN_TESTR	Test mode Register.	RW
0xBD40_0070	2	WLAN_BCNITV	Beacon Interval Register.	RW
0xBD40_0072	2	WLAN_ATIMWND	Atim Window Register.	RW
0xBD40_0074	2	WLAN_BINTRITV	Beacon interrupt Interval Register.	RW
0xBD40_0076	2	WLAN_ATIMTRITV	Atim Interrupt Interval Register.	RW
0xBD40_007C	1	WLAN_PHYADDR	PHY interface Address Register.	RW

Virtual Address	Size (byte)	Name	Description	RW
0xBD40_007D	1	WLAN_PHYDATAW	Write Data to PHY.	W
0xBD40_007E	1	WLAN_PHYDATAR	Read Data from PHY.	R
0xBD40_0080	2	WLAN_RFPINOUT	RF Pins Output	RW
0xBD40_0082	2	WLAN_RFPINEN	RF Pins Enable	RW
0xBD40_0084	2	WLAN_RFPINSEL	RF Pins Select	RW
0xBD40_0086	2	WLAN_RFPININPUT	RF Pins Input	RW
0xBD40_0088	4	WLAN_RFPARA	RF Parameter	RW
0xBD40_008C	4	WLAN_RFTIMING	RF Timing	RW
0xBD40_009C	1	WLAN_TXAGC	Auto TXAGC Control.	RW
0xBD40_009D	1	WLAN_CCKTXAGC	Complementary Code Keying TX Automatic Gain Control.	RW
0xBD40_009E	1	WLAN_OFDMTXAGC	Orthogonal Frequency Division Multiplexing TX Automatic Gain Control.	RW
0xBD40_009F	1	WLAN_ANTSEL	TX Antenna Select.	RW
0xBD40_00A0	4	WLAN_CAMRW	Content Access Memory Read/Write.	RW
0xBD40_00A4	4	WLAN_CAMOUTPUT	Date written to Content Access Memory.	RW
0xBD40_00A8	4	WLAN_CAMINPUT	Date read from Content Access Memory.	RW
0xBD40_00AC	4	WLAN_CAMDEBUG	Content Access Memory Debug Interface.	RW
0xBD40_00B0	2	WLAN_WPACONFIG	Wi-Fi Protected Access Config.	RW
0xBD40_00B2	2	WLAN_AESMASK	Advanced Encryption Standard Mask.	RW
0xBD40_00B4	1	WLAN_SIFS	Short InterFrame Spacing Timer Setting.	RW
0xBD40_00B5	1	WLAN_DIFS	Distributed InterFrame Spacing Timer Setting.	RW
0xBD40_00B6	1	WLAN_SLOTTIME	Slot Time Setting.	RW
0xBD40_00B7	1	WLAN_USTUNE	Micro-second Fine Tune Config.	RW
0xBD40_00BC	1	WLAN_CWCONFIG	Contention Window Config.	RW
0xBD40_00BD	1	WLAN_CWVALUE	Contention Window Value.	RW
0xBD40_00BE	1	WLAN_RATECTRL	Auto Rate Fallback Control.	RW
0xBD40_00D8	1	WLAN_CONFIG5	Configuration Register 5.	RW
0xBD40_00D9	1	WLAN_TPPOLL	Transmit Priority Polling register.	W
0xBD40_00DC	2	WLAN_CWR	Contention Window Register.	R
0xBD40_00DE	1	WLAN_RETRYCTR	Retry Count Register.	R
0xBD40_00E4	4	WLAN_RDSAR	Receive Descriptor Start Address Register (32-bit). (256-byte alignment).	RW
0xBD40_0100	4	WLAN_DFSCR	DFS control register	RW
0xBD40_0104	4	WLAN_DFSSLR	DFS Schmitt trigger low-threshold setting register	RW
0xBD40_0108	4	WLAN_DFSSHR	DFS Schmitt trigger high-threshold setting register	RW
0xBD40_010C	4	WLAN_DFSDLR	DFS Pulse-duration low-threshold setting register	RW
0xBD40_0110	4	WLAN_DFSDHR	DFS Pulse-duration high-threshold setting register	RW
0xBD40_0114	4	WLAN_DFSPCR	DFS valid pulse count register	R
0xBD40_0118	4	WLAN_DFSTS0R	DFS Time Stamp 0 register	RW
0xBD40_011C	4	WLAN_DFSTS1R	DFS Time Stamp 1 register	RW
0xBD40_0120	4	WLAN_DFSTS2R	DFS Time Stamp 2 register	RW
0xBD40_0124	4	WLAN_DFSTS3R	DFS Time Stamp 3 register	RW
0xBD40_0128	4	WLAN_DFSTS4R	DFS Time Stamp 4 register	RW
0xBD40_012C	4	WLAN_DFSTS5R	DFS Time Stamp 5 register	RW
0xBD40_0130	4	WLAN_DFSTS6R	DFS Time Stamp 6 register	RW
0xBD40_0134	4	WLAN_DFSTS7R	DFS Time Stamp 7 register	RW
0xBD40_0138	4	WLAN_DFSTS8R	DFS Time Stamp 8 register	RW
0xBD40_013C	4	WLAN_DFSTS9R	DFS Time Stamp 9 register	RW
0xBD40_0140	4	WLAN_DFSTSAR	DFS Time Stamp A register	RW
0xBD40_0144	4	WLAN_DFSTSBR	DFS Time Stamp B register	RW
0xBD40_0148	4	WLAN_DFSTSCR	DFS Time Stamp C register	RW
0xBD40_014C	4	WLAN_DFSTSDR	DFS Time Stamp D register	RW

Virtual Address	Size (byte)	Name	Description	RW
0xBD40_0150	4	WLAN_DFSTSER	DFS Time Stamp E register	RW
0xBD40_0154	4	WLAN_DFSTSFR	DFS Time Stamp F register	RW
0xBD40_0158	4	WLAN_DFSTSGR	DFS Time Stamp G register	RW
0xBD40_015C	4	WLAN_DFSTSHR	DFS Time Stamp H register	RW
0xBD40_0160	4	WLAN_DFSTSIR	DFS Time Stamp I register	RW
0xBD40_0164	4	WLAN_DFSTSJR	DFS Time Stamp J register	RW
0xBD40_0168	4	WLAN_DFSCTSR	DFS Current Time Stamp register	R

0xBD40_0018 **TSF Timer Register (WLAN_TSFTR)**

Bit	Bit Name	Description	RW
63-0	TSFT	Timing Synchronization Function Timer. The RTL8186/RTL8186P maintains a TSF timer with modules 2^64 counting in increments of microseconds. The 8 octets are the timestamp field of beacon and probe response frames.	R

0xBD40_002C **Basic Rate Set Register (WLAN_BRSR)**

Bit	Bit Name	Description			R/W
15-12	-	Reserved.			
11-0	BRSR	Basic Rate Set Register.			R/W
			1Mbps	Bit 0	
			2Mbps	Bit 1	
			5.5Mbps	Bit 2	
			11Mbps	Bit 3	
			6Mbps	Bit 4	
			9Mbps	Bit 5	
			12Mbps	Bit 6	
			18Mbps	Bit 7	
			24Mbps	Bit 8	
			36Mbps	Bit 9	
			48Mbps	Bit 10	
			54Mbps	Bit 11	

0xBD40_002E **Basic Service Set ID Register (WLAN_BSSID)**

Bit	Bit Name	Description	RW
47-0	BSSID	Basic Service Set Identification. The driver writes to this register to set BSSID after a NIC joins a network or creates a BSS/IBSS network.	RW

0xBD40_0034 **Response Rate (WLAN_RR)**

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th><th>RW</th></tr>
<tr><td>7-4</td><td>MAX_RESPONSE_RATE</td><td>Maximum Response Rate.
If the rate of the received unicast packet/RTS is larger than the Maximum Response Rate, the hardware uses the Maximum Response Rate to respond to the received packet.</td><td>RW</td></tr>
<tr><td>3-0</td><td>MIN_RESPONSE_RATE</td><td>Minimum Response Rate.
If the rate of the received unicast packet/RTS is not larger than the Maximum Response Rate and is not one of the basic rates shown below, the hardware uses the Minimum Response Rate to respond to the received packet.
<table>
<tr><th></th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>1Mbps</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2Mbps</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>5.5Mbps</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>11Mbps</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>6Mbps</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>9Mbps</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>12Mbps</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>18Mbps</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>24Mbps</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>36Mbps</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>48Mbps</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>54Mbps</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
</table></td><td>RW</td></tr>
</table>

0xBD40_0037 **Command Register (WLAN_CR)**

Bit	Bit Name	Description	RW
7-5		Reserved.	
4	RST	Reset. Setting this bit to 1 forces the RTL8186/RTL8186P perform a WLAN MAC reset. During the reset state, it disables the transmitter and receiver and reinitializes the FIFOs. The values of WLAN_IDR and WLAN_MAR are not changed. This bit is 1 during the reset operation, and is cleared to 0 when the reset operation is complete.	RW
3	RE	Receiver Enable. When set to 1 whilst the receive state machine is idle, the receive machine becomes active. This bit will read back as 1 whenever the receive state machine is active. After initial power-up, software must insure that the receiver has completely reset before setting this bit. 1: Enable 0: Disable	RW
2	TE	Transmitter Enable. When set to 1 whilst the transmit state machine is idle, the transmit state machine becomes active. This bit will read back as 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit. 1: Enable 0: Disable	RW
1		Reserved.	
0	MULRW	Multiple Bus Read/Write Enable. 1: Enable 0: Disable	RW

0xBD40_003C **Interrupt Mask Register (WLAN_IMR)**

Bit	Bit Name	Description	RW
15	TXFOVW	Tx FIFO Overflow Interrupt. 1: Enable 0: Disable	RW

Bit	Bit Name	Description	RW
14	TimeOut	Time Out interrupt. 1: Enable 0: Disable	RW
13	BcnInt	Beacon Time out Interrupt. 1: Enable 0: Disable	RW
12	ATIMInt	ATIM Time Out Interrupt. 1: Enable 0: Disable	RW
11	TBDER	Tx Beacon Descriptor Error interrupt. 1: Enable 0: Disable	RW
10	TBDOK	Tx Beacon Descriptor OK interrupt. 1: Enable 0: Disable	RW
9	THPDER	Tx High Priority Descriptor Error interrupt. 1: Enable 0: Disable	RW
8	THPDOK	Tx High Priority Descriptor OK interrupt. 1: Enable 0: Disable	RW
7	TNPDER	Tx Normal Priority Descriptor Error interrupt. 1: Enable 0: Disable	RW
6	TNPDOK	Tx Normal Priority Descriptor OK interrupt. 1: Enable 0: Disable	RW
5	RXFOVW	Rx FIFO Overflow interrupt. 1: Enable 0: Disable	RW
4	RDU	Rx Descriptor Unavailable interrupt. 1: Enable 0: Disable	RW
3	TLPDER	Tx Low Priority Descriptor Error interrupt. 1: Enable 0: Disable	RW
2	TLPDOK	Tx Low Priority Descriptor OK interrupt. 1: Enable 0: Disable	RW
1	RER	Rx Error interrupt. 1: Enable 0: Disable	RW
0	ROK	Rx OK interrupt. 1: Enable 0: Disable	RW

0xBD40_003E **Interrupt Status Register (WLAN_ISR)**

Bit	Bit Name	Description	RW
15	TXFOVW	Tx FIFO Overflow.	RW
14	TimeOut	Time Out. This bit is set to 1 when the least 32 bits of the TSFTR register reaches the value of the TimerInt register.	RW
13	BcnInt	Beacon time out Interrupt. When set, this bit indicates that the TBTT (Target Beacon Transmission Time) has reached the value set in the Beacon Interrupt Interval Register.	RW

Bit	Bit Name	Description	RW
12	ATIMInt	ATIM Time Out Interrupt. When set, this bit indicates that the ATIM window has reached the value set in the Atim Interrupt Interval Register.	RW
11	TBDER	Transmit Beacon priority Descriptor Error. Indicates that a beacon priority descriptor transmission was aborted due to reception of a beacon frame.	RW
10	TBDOK	Transmit Beacon priority Descriptor OK. Indicates that a beacon priority descriptor exchange sequence has been successfully completed.	RW
9	THPDER	Transmit High Priority Descriptor Error. Indicates that a high priority descriptor transmission was aborted due to an SSRC (Station Short Retry Count) having reached SRL (Short Retry Limit), or an SLRC (Station Long Retry Count) having reached LRL (Long Retry Limit).	RW
8	THPDOK	Transmit High Priority Descriptor OK. Indicates that a high priority descriptor exchange sequence has been successfully completed.	RW
7	TNPDER	Transmit Normal Priority Descriptor Error. Indicates that a normal priority descriptor transmission was aborted due to an SSRC (Station Short Retry Count) having reached SRL (Short Retry Limit), or an SLRC (Station Long Retry Count) having reached LRL (Long Retry Limit).	RW
6	TNPDOK	Transmit Normal Priority Descriptor OK. Indicates that a normal priority descriptor exchange sequence has been successfully completed.	RW
5	FOVW	Rx FIFO Overflow. This bit set to 1 is caused by Receive Descriptor Unavailable (RDU), poor PCI performance, or overloaded PCI traffic.	RW
4	_RDU	Rx Descriptor Unavailable. When set, this bit indicates that the Rx descriptor is currently unavailable.	RW
3	TLPDER	Transmit Low Priority Descriptor Error. Indicates that a low priority descriptor transmission was aborted due to an SSRC (Station Short Retry Count) having reached SRL (Short Retry Limit), or an SLRC (Station Long Retry Count) having reached LRL (Long Retry Limit).	RW
2	TLPDOK	Transmit Low Priority Descriptor OK. Indicates that a low priority descriptor exchange sequence has been successfully completed.	RW
1	RER	Receive Error. Indicates that a packet has a CRC32 or ICV error.	RW
0	ROK	Receive OK. In normal mode, indicates the successful completion of a packet reception.	RW

0xBD40_0040 **Transmit Configuration Register (WLAN_TCR)**

Bit	Bit Name	Description	RW
31-30		Reserved	
29	NO_PROBE_RSP_TIMESTAMP	Disable tagging a timestamp onto probe response frames.	RW
28		Reserved.	
24	PLCP_LENGTH	HW/SW Physical Layer Convergence Procedure Length Mechanism. 1: Software provides the PLCP length and LENGEXT. 0: Hardware provides the PLCP length and LENGEXT.	RW
23-21	MXDMA2, 1, 0	Max DMA burst size per Tx DMA burst. This field sets the maximum size of transmit DMA data bursts according to the following: 000: 16 bytes, 001: 32 bytes, 010: 64 bytes, 011: 128 bytes, 100: 256 bytes, 101: 512 bytes, 110: 1024 bytes, 111: 2048 bytes	RW

Bit	Bit Name	Description	RW
20	DISCW	Disable Contention Window Backoff. This bit indicates the existence of a backoff procedure during packet transmission. 0: Uses IEEE 802.11 random backoff procedure 1: No random backoff procedure	RW
19	ICV	Append ICV (Integrity Check Value). This bit indicates the existence of an ICV appended at the end of an encipherment packet. 0: ICV appended 1: No ICV appended	RW
18-17	LBK1, LBK0	Loopback Test. There are no packets on the TXI+/- and TXQ+/- lines under the Loopback test condition. The loopback function must be independent of the link state. 00: Normal operation, 01: MAC Loopback 10: Baseband Loopback, 11: Continue TX.	RW
16	CRC	Append CRC32. This bit indicates the existence of a CRC32 appended at the end of a packet. 0: A CRC32 is appended 1: No CRC32 appended	RW
15-8	SRL	Short Retry Limit RTS Retry Limit. Indicates the maximum retry time for frames of length less than or equal to the RTSThreshold.	RW
7-0	LRL	Long Retry Limit: Data Packet Retry Limit. Indicates the maximum retransmission times for Data or Management frames of length greater than RTSThreshold.	RW

0xBD40_0044 **Receive Configuration Register (WLAN_RCR)**

Bit	Bit Name	Description	RW
31	ONLYERLPKT	Early Receiving based on Packet Size. Early Receiving is only performed for packets with a size greater than 1536 bytes.	RW
30	ENCS2	Enable Carrier Sense Detection Method 2.	RW
29	ENCS1	Enable Carrier Sense Detection Method 1.	RW
28	ENMARP	Enable MAC Auto-reset PHY.	RW
27-24		Reserved.	
23	CBSSID	Check BSSID ‘To DS’ and ‘From DS’ Match Packet. When set to 1, the RTL8186/RTL8186P will check the Rx data type frame’s BSSID ‘To DS’ and ‘From DS’ fields, according to NETYPE (bits 3:2, MSR), to determine if it is set to Link ok.	RW
22	APWRMGT	Accept Power Management packet. This bit determines whether the RTL8186/RTL8186P will accept or reject packets with the power management bit set. 0: Reject 1: Accept	RW
21	ADD3	Accept Address 3 match packets. Set this bit to 1 to accept broadcast/multicast data type frames that Address 3 match the RTL8186/RTL8186P’s MAC address. This bit is valid only when NETYPE (bits 3:2, MSR) is set to Link ok in an Infrastructure network.	RW
20	AMF	Accept Management Frame. This bit determines whether the RTL8186/RTL8186P will accept or reject a management frame. 0: Reject 1: Accept	RW

Bit	Bit Name	Description	RW
19	ACF	Accept Control Frame. This bit determines whether the RTL8186/RTL8186P will accept or reject a control frame. 0: Reject 1: Accept	RW
18	ADF	Accept Data Frame. This bit determines whether the RTL8186/RTL8186P will accept or reject a data frame. 0: Reject 1: Accept	RW
17-16		Reserved.	
15-13	RXFTH2, 1, 0	Rx FIFO Threshold. This bit specifies the Rx FIFO Threshold level. When the number of the received data bytes from a packet being received into the Rx FIFO of the RTL8186/RTL8186P has reached the set level (or the FIFO contains a complete packet), the receive PCI bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following: 000: Reserved, 001: Reserved, 010: 64 bytes, 011: 128 bytes 100: 256 bytes, 101: 512 bytes, 110: 1024 bytes, 111: No Rx threshold. The RTL8186/RTL8186P begins the transfer of data after receiving a whole packet into the FIFO.	
12	AICV	Accept ICV error packets. This bit determines whether packets with ICV (Integrity Check Value) errors will be accepted or rejected. 1: Accept 0: Reject	
11		Reserved.	
10-8	MXDMA2, 1, 0	Max. DMA burst size per Rx DMA burst. This field sets the maximum size of the receive DMA data bursts according to the following: 000: 16 bytes, 001: 32 bytes, 010: 64 bytes, 011: 128 bytes 100: 256 bytes, 101: 512 bytes, 110: 1024 bytes, 111: Unlimited	
7-6		Reserved.	
5	ACRC32	Accept CRC32 error packets. This bit determines whether packets with CRC32 errors will be accepted or rejected. 0: Reject 1: Accept	
4		Reserved.	
3	AB	Accept Broadcast packets. This bit determines whether broadcast packets will be accepted or rejected. 0: Reject 1: Accept	
2	AM	Accept Multicast packets. This bit determines whether multicast packets will be accepted or rejected. 0: Reject 1: Accept	
1	APM	Accept Physical Match packets. This bit determines whether physical match packets will be accepted or rejected. 0: Reject 1: Accept	
0	AAP	Accept destination Address Packets. This bit determines whether packets with a destination address will be accepted or rejected. 0: Reject 1: Accept	

0xBD40_0050 **Command Register (WLAN_CR)**

Bit	Bit Name	Description	RW
7-6	EEM	These 2 bits select the operating mode. 00: Operating in network/host communication mode. 11: Before writing to the WLAN_CONFIG0, 1, 2, and 3 registers, the RTL8186/RTL8186P must be placed in this mode. This prevents accidental changes to the WLAN controller configurations.	RW
5-0		Reserved.	

0xBD40_0051 **Configuration Register 0 (WLAN_CONFIG0)**

Bit	Bit Name	Description	RW
7-4		Reserved.	
3	Aux_Status	Auxiliary power present Status. This bit indicates the existence of auxiliary power. The value of this bit is fixed after each reset. 1: Auxiliary power is present 0: Auxiliary power is absent	RW
2		Reserved.	
1-0	GL	Geographic Location. These bits indicate the current operational region in which the RTL8186/RTL8186P transmits and receives packets. 11: USA, 10: Europe, 0: Japan	RW

0xBD40_0052 **Configuration Register 1 (WLAN_CONFIG1)**

Bit	Bit Name	Description	RW
7-6	LED	WLAN LED indicator, which bit values are defined as: LED0-1 / 00 / 01 / 10 / 11 LED0 / TX/RX / TX/RX / TX / LINK/ACT LED1 / Infrastructure / LINK / RX / Infrastructure	RW
5-0		Reserved.	

0xBD40_0053 **Configuration Register 2 (WLAN_CONFIG2)**

Bit	Bit Name	Description	RW
7	LCK	Locked Clocks. Set this bit to 1 to lock the transmit frequency and symbol clocks to the same oscillator.	RW
6	ANT	Antenna diversity. 0: Disable 1: Enable	RW
5-4		Reserved.	
3	DPS	Descriptor Polling State. Test mode. 0: Normal working state. This is also the power-on default value 1: Test mode	RW
2	PAPE_sign	Power Amplifier Enable timing. 1: The RTL8186/RTL8186P will advance PAPE_time to enable the PAPE pin when transmitting data 0: The RTL8186/RTL8186P will delay PAPE_time to enable the PAPE pin when transmitting data	RW
1-0	PAPE_time	These two bits indicate that the RTL8186/RTL8186P has enabled the PAPE pin (in µs).	RW

0xBD40_0058 **Media Status Register (WLAN_MSR)**

Bit	Bit Name	Description	RW
7-4		Reserved.	
3-2	NETTYPE	Network Type and Link Status. The values of these bits are written by the driver. 10: Infrastructure client, 01: Ad-hoc, 11: Access Point, 00: No link	RW
1-0		Reserved.	

0xBD40_0059 **Configuration Register 3 (WLAN_CONFIG3)**

Bit	Bit Name	Description	RW
7		Reserved.	
6	PARM_En	Parameter write Enable. Setting this bit to 1 and asserting WLAN_CR register bit EEM1 and EEM0 at the same time will enable the WLAN_ANAPARM register to be written via software.	RW
4-1		Reserved.	
0	FBtBEn	Fast Back to Back Enable. 0: Disable 1: Enable	RW

0xBD40_005A **Configuration Register 4 (WLAN_CONFIG4)**

Bit	Bit Name	Description	RW
7	VCOPDN	VCO Power Down. 0: Normal working state. This is the power-on default value 1: VCO power down mode. Setting this bit enables the VCOPDN pin and turns off the external RF front end power (including VCO) and most of the internal power of the RTL8186/RTL8186P	RW
6	PWROFF	Power Off. 0: Normal working state. This is the power-on default value 1: Power Off mode. Turn off the external RF front end power (excluding VCO) and most of the internal power of the RTL8186/RTL8186P	RW
5	PWRMGT	Power Management. 0: Normal working state. This is the power-on default value 1: Power management mode. Sets a Tx packet's power management bit to 1 to include a control type frame	RW
4-0		Reserved.	

0xBD40_0070 **Beacon Interval Register (WLAN_BCNITV)**

Bit	Bit Name	Description	RW
15-0	BCNITV	Beacon Interval. The Beacon Interval represents the number of time units (1 TU = 1024μs) between target beacon transmissions (TBTTs). This register is written by the driver after starting a BSS/IBSS or joining an IBSS network.	RW

0xBD40_0072 **ATIM Window Register (WLAN_ATIMWND)**

Bit	Bit Name	Description	RW
15-0	ATIMWND	This register indicates the ATIM Window length in Time Units (TU). It is written by the driver after the NIC joins or creates an ad-hoc network.	RW

0xBD40_0074 **Beacon Interrupt Interval Register (WLAN_BINTRITV)**

Bit	Bit Name	Description	RW
15-0	BINTRITV	This timer register generates BcnInt (bit 13, ISR) at a set time interval before TBTT to prompt the host to prepare the beacon. The unit of this register is microseconds. It is written by the driver after the NIC joins a network or creates an ad-hoc network.	RW

0xBD40_0076 **ATIM Interrupt Interval Register (WLAN_ATIMTRITV)**

Bit	Bit Name	Description	RW
15-0	ATIMTRITV	This timer register generates ATIMInt (bit 12, ISR) at a set time interval before the end of the ATIM window in an ad-hoc network. The unit of this register is microseconds. It is written by the driver after the NIC joins a network or creates an ad-hoc network.	RW

0xBD40_0078 **PHY Delay Register (WLAN_PHYDELAY)**

Bit	Bit Name	Description	RW
7-3		Reserved.	
2-0	PHYDELAY	Physical layer Delay. These three bits represent the delay time in μs between the wireless MAC and RF front end when transmitting data.	RW

0xBD40_00A0 **Read/Write CAM (WLAN_CAMRW)**

Bit	Bit Name	Description	RW
31	POLLING	Polling bit	RW
30-17		Reserved	
16	WRITE_ENABLE	Write Enabled	RW
15-7		Reserved	
6-0	CAM_ADDRESS	CAM Address	RW

0xBD40_00AC **CAM Debug Interface (WLAN_CAMDEBUG)**

Bit	Bit Name	Description	RW
31	SEL_TX_CAM_INFO	Select TX/RX CAM Information	RW
30	KEY_FOUND	TX/RX Security Key is Found.	
29-24	WPA_CONFIG	TX/RX WPA Config	RW
23-0	CAM_KEY	CAM Key.	RW

0xBD40_00B0 **WPA Config (WLAN_WPACONFIG)**

Bit	Bit Name	Description	RW
31-9		Reserved.	
8	RX_WPA_DUMMY	Enable RX Dummy Function.	RW
7-4		Reserved.	
3	DISABLE_RX_AES_MIC	Disable RX AES MIC.	RW
2	RX_DECRYPT	Enable RX Decryption.	RW
1	TX_ENCRYPTION	Enable Tx Encryption	RW
0	USING_DEFAULT_KET	Force HW Using Default Key.	RW

0xBD40_00BC **Contention Window Config (WLAN_CWCONFIG)**

Bit	Bit Name	Description	RW
7-2		Reserved.	
1	PER_PACKET_RETRY_LIMIT	Enable Per-packet Retry Limit.	RW

Bit	Bit Name	Description	RW
0	PER_PACKET_CW	Enable Per-Packet Contention Window.	RW

0xBD40_00BD **Contention Window Value (WLAN_CWVALUE)**

Bit	Bit Name	Description	RW
7-4	CWMAX	Maximum Contention Window. CWMax = 2^n-1.	RW
3-0	CWMIN	Minimum Contention Window. CWMin = 2^n-1.	RW

0xBD40_00BE **Auto Rate Fallback Control (WLAN_RATECTRL)**

Bit	Bit Name	Description	RW
7	ENABL_RATE_FALLBACK	Enable Auto Rate Fallback..	RW
6-2		Reserved	
1-0	FALLBACK_STEP	Auto Rate Fallback Step. Auto rate fallback per 2^n retry.	

0xBD40_00D8 **Configuration Register 5 (WLAN_CONFIG5)**

Bit	Bit Name	Description	RW
7	TX_FIFI_OK	Built in Self-Test for TX FIFO. 1: OK 0: Fail	R
6	RX_FIFO_OK	Built in Self-Test for RX FIFO. 1: OK 0: Fail	R
5-0		Reserved.	

0xBD40_00D9 **Transmit Priority Polling Register (WLAN_TPPOLL)**

Bit	Bit Name	Description	RW
7	BQ	Beacon Queue Polling. The RTL8186 will clear this bit automatically after a beacon packet has been transmitted or received. Writing to this bit has no effect	W
6	HPQ	High Priority Queue Polling. Write a 1 to this bit by software to notify the RTL8186 that there is a high priority packet(s) waiting to be transmitted. The RTL8186 will clear this bit automatically after all high priority packets have been transmitted. Writing a 0 to this bit has no effect.	W
5	NPQ	Normal Priority Queue Polling. DPS (bit3, Config 2) set to 0: The RTL8186 will clear this bit automatically after all normal priority packets have been transmitted or received. Writing to this bit has no effect. DPS (bit3, Config 2) set to 1: Write a 1 to this bit via software to notify the RTL8186 that there is a normal priority packet(s) waiting to be transmitted. The RTL8186 will clear this bit automatically after all normal priority packets have been transmitted. Writing a 0 to this bit has no effect.	W

Bit	Bit Name	Description	RW
4	LPQ	Low Priority Queue Polling. Write a 1 to this bit via software to notify the RTL8186 that there is a low priority packet(s) waiting to be transmitted. The RTL8186 will clear this bit automatically after all low priority packets have been transmitted. Writing a 0 to this bit has no effect.	W
3	SBQ	Stop High Priority Queue. Write a 1 to this bit via software to notify the RTL8186 to stop the DMA mechanism of the High Priority Queue.	
2	SHPQ	Stop High Priority Queue. Write a 1 to this bit via software to notify the RTL8186 to stop the DMA mechanism of the High Priority Queue.	
1	SNPQ	Stop Normal Priority Queue. Write a 1 to this bit via software to notify the RTL8186 to stop the DMA mechanism of the Normal Priority Queue. This bit is invalid when DPS (bit3, Config 2) is set to 1.	
0	SLPQ	Stop Low Priority Queue. Write a 1 to this bit via software to notify the RTL8186 to stop the DMA mechanism of the Low Priority Queue.	

0xBD40_00DC **Contention Window Register (WLAN_CWR)**

Bit	Bit Name	Description	RW
15-10		Reserved	
9-0	CW	Contention Window. This register indicates the number of contention windows before transmitting a packet.	R

0xBD40_00DE **Retry Count Register (WLAN_RETRYCTR)**

Bit	Bit Name	Description	RW
7-0	RETRYCT	Retry Count. This register indicates the number of retry counts when a packet transmit is completed.	R

0xBD40_00E4 **Receive Descriptor Start Address Register (WLAN_RDSAR)**

Bit	Bit Name	Description	RW
31-0	RDSA	Receive Descriptor Start Address. This is a 32-bit address.	RW

0xBD40_0100 **DFS Control Register (DFSCR)**

Bit	Bit Name	Description	R/W
7	TSFS	Time Stamp Format select. When this bit is set, the time stamp registers use LSb for recording the CCA status, else the time stamp registers recording the current time while detecting valid pulse. '1': Record CCA status at LSb of time stamp registers '0': Record current time at time stamp registers	R/W
6	CCAEN	CCA filter enable. When this bit is set, the CCA signal will filter the valid pulse during CCA on. '1': Enable CCA filtering '0': Disable CCA filtering	R/W
5	TDS	Time Stamp clock divider select. '1': 5/64 MHz clock selected '0': 5/128 MHz clock selected	R/W

4	TXONE	TX on filter enable. When this bit is set, the DFS detection will stop while TX is on, else disable the TX on filter. '1': Enable TX ON filtering '0': Disable TX ON filtering	R/W
3	IQCKS	I-Q sample clock phase select. When this bit is set, the IQ sample clock use falling edge of the clock, else the IQ sample clock use rising clock edge. '1': falling clock edge '0': rising clock edge	R/W
2	IQEN	I-Q power detection mechanism enable. When this bit set, the DFS module use I-Q power detection mechanism to detect radar pulse, else the DFS module use RSSI threshold mechanism. '1': Enable I-Q power detection. '0': Enable RSSI threshold detection.	R/W
1	DCCAEN	Delay CCA mechanism enable. When this bit is set, the Delay CCA signal will mask the RSSI input. Else the Delay CCA signal has no effect at all. '1': Enable Delay CCA filtering '0': Disable Delay CCA filtering.	R/W
0	DFSEN	DFS module enable. When the DFS module is enabled, the Time Stamp registers are updated when valid pulse is detected. When the DFS module is disabled, the Time Stamp registers are reset to default state. '1': Enable DFS function '0': Disable DFS function	R/W

0xBD40_0104 **DFS Schmitt trigger Low Threshold Register (DFSSLR)**

Bit	Bit Name	Description	R/W
31-7		Reserved	
6-0	LT	Low Threshold value of Schmitt trigger	R/W

0xBD40_0108 **DFS Schmitt trigger High Threshold Register (DFSSHR)**

Bit	Bit Name	Description	R/W
31-7		Reserved	
6-0	HT	High Threshold value of Schmitt trigger	R/W

0xBD40_010C **Pulse Duration Low Threshold Register (DFSDLR)**

Bit	Bit Name	Description	R/W
31-6		Reserved	
5-0	LT	Low Threshold value of Pulse Duration (unit: 0.2 us)	R/W

0xBD40_0110 **Pulse Duration High Threshold Register (DFSDHR)**

Bit	Bit Name	Description	R/W
31-6		Reserved	
5-0	HT	High Threshold value of Pulse Duration (unit: 0.2 us)	R/W

0xBD40_0114 **Pulse Count Register (DFSPCR)**

Bit	Bit Name	Description	R/W
31-5		Reserved	
4-0	PC	Valid Pulse Count. While DFS is enabled, the number of valid pulse detected is show at this register. This value also indicates who many time stamp registers are valid. Disable DFS module will reset this register.	R

0xBD40_0118 **Time Stamp 0 Register (DFSTS0R)**
0xBD40_011C **Time Stamp 1 Register (DFSTS1R)**
0xBD40_0120 **Time Stamp 2 Register (DFSTS2R)**
0xBD40_0124 **Time Stamp 3 Register (DFSTS3R)**
0xBD40_0128 **Time Stamp 4 Register (DFSTS4R)**
0xBD40_012C **Time Stamp 5 Register (DFSTS5R)**
0xBD40_0130 **Time Stamp 6 Register (DFSTS6R)**
0xBD40_0134 **Time Stamp 7 Register (DFSTS7R)**
0xBD40_0138 **Time Stamp 8 Register (DFSTS8R)**
0xBD40_013C **Time Stamp 9 Register (DFSTS9R)**
0xBD40_0140 **Time Stamp A Register (DFSTSAR)**
0xBD40_0144 **Time Stamp B Register (DFSTSBR)**
0xBD40_0148 **Time Stamp C Register (DFSTSCR)**
0xBD40_014C **Time Stamp D Register (DFSTSDR)**
0xBD40_0150 **Time Stamp E Register (DFSTSER)**
0xBD40_0154 **Time Stamp F Register (DFSTSFR)**
0xBD40_0158 **Time Stamp G Register DFSTSGR)**
0xBD40_015C **Time Stamp H Register (DFSTSHR)**
0xBD40_0160 **Time Stamp I Register (DFSTSIR)**
0xBD40_0164 **Time Stamp J Register (DFSTSJR)**

Bit	Bit Name	Description	R/W
31-16		Reserved	
15-1	TS	The time stamp of detected valid pulse. This value will reset while DFS module is disabled.	R
0	CCA	When TSFS of DFSCR register is set, this bit is the CCA signal status of the time that time stamp register is updated. Else this bit indicates the LSb of TS.	R

0xBD40_0168 **Current Time Stamp Register (DFSCTSR)**

Bit	Bit Name	Description	R/W
31-16		Reserved	
15-0	TS	Current real-time stamp. The real-time time stamp will reset to 0 while DFS module is disabled.	R

Packet Buffering
RTL8186 WLAN controller incorporates two independent FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data freeing the host system from the real-time demands of the network.

The way in which the FIFOs are emptied and filled is controlled by the FIFO threshold values in the Receive Configuration registers. These values determine how full or empty the FIFOs must be before the device requests the bus. Once RTL8186 requests the bus, it will attempt to empty or fill the FIFOs as allowed by the respective MXDMA settings in the Transmit Configuration and Receive Configuration registers.

Transmit Buffer Manager
The buffer management scheme used on the WLAN controller allows quick, simple and efficient use of the frame buffer memory. The buffer management scheme uses separate buffers and descriptors for packet information. This allows effective transfers of data to the transmit buffer manager by simply transferring the descriptor information to the transmit queue.
The Tx Buffer Manager DMAs packet data from system memory and places it in the 4KB transmit FIFO, and pulls data from the FIFO to send to the Tx MAC. Multiple packets may be present in the FIFO, allowing packets to be transmitted with short interframe space. Additionally, once RTL8186 requests the bus, it will attempt to fill the FIFO as allowed by the MXDMA setting.

The Tx Buffer Manager process also supports priority queuing of transmit packets. It handles this by drawing from two separate descriptor lists to fill the internal FIFO. If packets are available in the high priority queues, they will be loaded into the FIFO before those of low priority.

Receive Buffer Manager

The Rx Buffer Manager uses the same buffer management scheme as used for transmits. The Rx Buffer Manager retrieves packet data from the Rx MAC and places it in the 2KB receive data FIFO, and pulls data from the FIFO for DMA to system memory. The receive FIFO is controlled by the FIFO threshold value in RXFTH. This value determines the number of long words written into the FIFO from the MAC unit before a DMA request for system memory occurs. Once the RTL8186 gets the bus, it will continue to transfer the long words from the FIFO until the data in the FIFO is less than one long word, or has reached the end of the packet, or the max DMA burst size is reached, as set in MXDMA.

Transmit & Receive Operation

The RTL8186 supports descriptor-based buffer management that will significantly lower host CPU utilization. The RTL8186 supports unlimited consecutive transmit descriptors and up to 64 consecutive descriptors for receive. There are four transmission descriptor rings for beacon, high priority packet, normal priority packet and low priority packet respectively. Besides, it includes another descriptor ring for receiving packet. Each transmit descriptor ring may consist of up to infinite 8-double-word consecutive descriptors and the receive descriptor array may consist of up to 64 4-double-word consecutive descriptors. The start address of each descriptor group should be in 256-byte alignment.

Transmit Descriptor

The following describes what the Tx descriptor may look like, depending on different states in each Tx descriptor.

Tx Descriptor Format (before transmitting, OWN=1, Tx command mode 1)

31	30	29	28	27 26 25 24	23	22 21 20 19	18	17	16	15	14 13 12	11 10 9 8 7 6 5 4 3 2 1 0	
OWN=1	DMAOK	FS	LS	TXRATE (4 bits)	RTSEN	RTSRATE (4 bits)	CTSEN	MOREFRAG	SPLCP	NO_ENCRYPT	RSVD	TPKTSIZE (12 bits)	Offset 0
LENGEXT	Length (15 bits)											RTSDUR (16 bits)	Offset 4
TX_BUFFER_ADDRESS													Offset 8
RSVD												Frame_Length (12 bits)	Offset 12
NEXT_TX_DESCRIPTOR_ADDRESS													Offset 16
RATE_FALL BACK_LIMIT (4 bits)			RSVD (3 bits)	ANTENNA	AGC (8 bits)		RETRY_LIMIT (8 bits)			CWMAX (4 bits)		CWMIN (4 bits)	Offset 20
RSVD													Offset 24
RSVD													Offset 28

Offset#	Bit#	Symbol	Description

<table>
<tr><th>Offset#</th><th>Bit#</th><th>Symbol</th><th>Description</th></tr>
<tr><td>0</td><td>31</td><td>OWN</td><td>Ownership.
When set, this bit indicates that the descriptor is owned by the NIC, and the data relative to this descriptor is ready to be transmitted. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1.</td></tr>
<tr><td>0</td><td>30</td><td>DMA OK</td><td>DMA OK.
Set by the driver, reset by the RTL8186 when TX DMA OK. If IMR's corresponding bit is set and the driver sets this bit, the RTL8186 resets this bit and issues an interrupt right after DMA OK of the last segment (LS). If not, the RTL8186 just resets this bit without asserting an interrupt.</td></tr>
<tr><td>0</td><td>29</td><td>FS</td><td>First Segment Descriptor.
When set, this bit indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.</td></tr>
<tr><td>0</td><td>28</td><td>LS</td><td>Last Segment Descriptor.
When set, indicates that this is the last descriptor of a Tx packet, and this descriptor is pointing to the last segment of the packet.</td></tr>
<tr><td>0</td><td>27:24</td><td>TXRATE</td><td>Tx Rate.
These four bits indicate the current frame's transmission rate.
<table>
<tr><th></th><th></th><th>Bit 27</th><th>Bit 26</th><th>Bit 25</th><th>Bit 24</th><th></th></tr>
<tr><td></td><td>1Mbps</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td></tr>
<tr><td></td><td>2Mbps</td><td>0</td><td>0</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>5.5Mbps</td><td>0</td><td>0</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>11Mbps</td><td>0</td><td>0</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>6Mbps</td><td>0</td><td>1</td><td>0</td><td>0</td><td></td></tr>
<tr><td></td><td>9Mbps</td><td>0</td><td>1</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>12Mbps</td><td>0</td><td>1</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>18Mbps</td><td>0</td><td>1</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>24Mbps</td><td>1</td><td>0</td><td>0</td><td>0</td><td></td></tr>
<tr><td></td><td>36Mbps</td><td>1</td><td>0</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>48Mbps</td><td>1</td><td>0</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>54Mbps</td><td>1</td><td>0</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>Reserved</td><td colspan="4">All other combinations</td><td></td></tr>
</table></td></tr>
<tr><td>0</td><td>23</td><td>RTSEN</td><td>RTS Enable.
Set to 1 indicates that an RTS/CTS handshake shall be performed at the beginning of any frame exchange sequence where the frame is of type Data or Management, the frame has an unicast address in the Address1 field, and the length of the frame is greater than RTSThreshold.</td></tr>
<tr><td>0</td><td>22:19</td><td>RTSRATE</td><td>RTS Rate.
These four bits indicate the RTS frame's transmission rate before transmitting the current frame and will be ignored if the RTSEN bit is set to 0.
<table>
<tr><th></th><th></th><th>Bit 22</th><th>Bit 21</th><th>Bit 20</th><th>Bit 19</th><th></th></tr>
<tr><td></td><td>1Mbps</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td></tr>
<tr><td></td><td>2Mbps</td><td>0</td><td>0</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>5.5Mbps</td><td>0</td><td>0</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>11Mbps</td><td>0</td><td>0</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>6Mbps</td><td>0</td><td>1</td><td>0</td><td>0</td><td></td></tr>
<tr><td></td><td>9Mbps</td><td>0</td><td>1</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>12Mbps</td><td>0</td><td>1</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>18Mbps</td><td>0</td><td>1</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>24Mbps</td><td>1</td><td>0</td><td>0</td><td>0</td><td></td></tr>
<tr><td></td><td>36Mbps</td><td>1</td><td>0</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>48Mbps</td><td>1</td><td>0</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>54Mbps</td><td>1</td><td>0</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>Reserved</td><td colspan="4">All other combinations</td><td></td></tr>
</table></td></tr>
</table>

Offset#	Bit#	Symbol	Description
0	18	CTSEN	CTS Enable. Both RTSEN and CTSEN set to 1 indicates that the CTS-to-self protection mechanism will be used.
0	17	MOREFRAG	More Fragment. This bit is set to 1 in all data type frames that have another fragment of the current packet to follow.
0	16	SPLCP	Short Physical Layer Convergence Protocol format. When set, this bit indicates that a short PLCP preamble will be added to the header before transmitting the frame.
0	15	NO_ENCRYPT	No Encryption. This packet will be sent out without encryption even if Tx encryption is enabled.
0	14:12	RSVD	Reserved.
0	11:0	TPKTSIZE	Transmit Packet Size. This field indicates the number of bytes required to transmit the frame.
4	31	LENGEXT	Length Extension. This bit is used to supplement the Length field (bits 30:16, offset 4). This bit will be ignored if the TXRATE is set to 1Mbps, 2Mbps, or 5.5Mbps.
4	30:16	Length	PLCP Length: The PLCP length field indicates the number of microseconds required to transmit the frame.
4	15:0	RTSDUR	RTS Duration: These bits indicate the RTS frame's duration field before transmitting the current frame and will be ignored if the RTSEN bit is set to 0.
8	31:0	TxBuff	32-bit Transmit Buffer Address.
12	31:28	RSVD	Reserved.
12	15:12	RSVD	Reserved.
12	11:0	Frame_Length	Transmit Frame Length. This field indicates the length in the Tx buffer, in bytes, to be transmitted.
16	31:0	NTDA	32-bit Address of the Next Transmit Descriptor.
20	31:28	RATE_FALLBACK_LIMIT	Data Rate Auto Fallback Limit.
20	27:25	RSVD	Reserved.
20	24	ANTENNA	Tx Antenna.
20	23:16	AGC	Tx AGC.
20	15:8	RETRY_LIMIT	Retry Count Limit.
20	7:4	CWMAX	Maximum Contention Window.
20	3:0	CWMIN	Minimum Contention Window.
24	31:0	RSVD	Reserved.
28	31:0	RSVD	Reserved.

Tx Status Descriptor (after transmitting, OWN=0, Tx status mode)

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27 26 25 24 23 22 21 20 19 18 17</td><td>16</td><td>15</td><td>14 13 12 11 10 9 8</td><td>7 6 5 4 3 2 1 0</td><td></td></tr>
<tr><td>OWN=0</td><td>DMA_OK</td><td>FS</td><td>LS</td><td colspan="2">RSVD (11 bits)</td><td>UDR</td><td>TOK</td><td>RTS RC (7 bits)</td><td>Packet RC (8 bits)</td><td>Offset 0</td></tr>
<tr><td colspan="10">RSVD</td><td>Offset 4</td></tr>
<tr><td colspan="10">TX_BUFFER_ADDRESS</td><td>Offset 8</td></tr>
</table>

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RSVD (20 bits)																				Frame_Length (12 bits)												Offset 12
NEXT_TX_DESCRIPTOR_ADDRESS																																Offset 16
RSVD																																Offset 20
RSVD																																Offset 24
RSVD																																Offset 28

Offset#	Bit#	Symbol	Description
0	31	OWN	Ownership. When set, this bit indicates that the descriptor is owned by the NIC. When clear, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the related buffer data has been transmitted. In this case, OWN=0.
0	30	DMA_OK	DMA Okay.
0	29	FS	First Segment Descriptor. When set, this bit indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	Last Segment Descriptor. When set, this bit indicates that this is the last descriptor of a Tx packet, and that this descriptor is pointing to the last segment of the packet.
0	27:17	RSVD	Reserved.
0	16	UDR	FIFO under run during transmission of this packet.
0	15	TOK	Transmit (Tx) OK. Indicates that a packet exchange sequence has completed successfully.
0	14:8	RTS RC	RTS Retry Count. The RTS RC's initial value is 0. It indicates the number of retries of RTS.
0	7:0	Packet RC	Packet Retry Count. The RC's initial value is 0. It indicates the number of retries before a packet was transmitted properly.
4	31:0	RSVD	Reserved.
8	31:0	TxBuff	32-bit Transmit Buffer Address.
12	31:12	RSVD	Reserved.
12	11:0	Frame_Length	Transmit Frame Length. This field indicates the length in the Tx buffer, in bytes, to be transmitted.
16	31:0	NTDA	32-bit Address of Next Transmit Descriptor.
20	31:0	RSVD	Reserved.
24	31:0	RSVD	Reserved.
28	31:0	RSVD	Reserved.

Receive

This section describes what an Rx descriptor could look like, depending on different states in each Rx descriptor. An Rx buffer pointed to by one of the Rx descriptors should be at least 4 bytes.

Rx Command Descriptor (OWN=1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OWN=1	EOR	RSVD (17 bits)																		Buffer_Size (12 bits)												Offset 0
RSVD (32 bits)																																Offset 4

RX_BUFFER_ADDRESS	Offset 8
RSVD	Offset 12

Offset#	Bit#	Symbol	Description
0	31	OWN	Ownership. When set, this bit indicates that the descriptor is owned by the RTL8186, and is ready to receive a packet. The OWN bit is set by the driver after having pre-allocated a buffer at initialization, or the host has released the buffer to the driver. In this case, OWN=1.
0	30	EOR	End of Rx Descriptor Ring. This bit set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the RTL8186 internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.
0	29:12	RSVD	Reserved.
0	11:0	Buffer_Size	Buffer Size. This field indicates the receive buffer size in bytes.
4	31:0	RSVD	Reserved.
8	31:0	RxBuff	32-bit Receive Buffer Address.
12	31:0	RSVD	Reserved.

Rx Status Descriptor (OWN=0)

31	30	29	28	27	26	25	24	23 22 21 20	19	18	17	16	15	14	13	12	11 10 9 8 7 6 5 4 3 2 1 0	
OWN=0	EOR	FS	LS	DMAF	FOVF	SPLCP	RSVD	RXRATE (4 bits)	RSVD	MAR	PAM	BAR	RES	PWRMGT	CRC32	ICV	Frame_Length (12 bits)	Offset 0
RSVD (6 bits)						WAKEUP	DECRYPTED	AGC (8 bits)					ANTENNA	RSSI (7 bits)			SQ (8 bits)	Offset 4
TSFTL																		Offset 8
TSFTH																		Offset 12

Offset#	Bit#	Symbol	Description
0	31	OWN	Ownership. When set, this bit indicates that the descriptor is owned by the RTL8186. When cleared, it indicates that the descriptor is owned by the host system. The RTL8186 clears this bit when the NIC has filled this Rx buffer with a packet or part of a packet. In this case, OWN=0.
0	30	EOR	End Of Rx Descriptor Ring. This bit set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the RTL8186 internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.
0	29	FS	First Segment Descriptor. When set, this bit indicates that this is the first descriptor of a received packet, and that this descriptor is pointing to the first segment of the packet.

<table>
<tr><th>Offset#</th><th>Bit#</th><th>Symbol</th><th>Description</th></tr>
<tr><td>0</td><td>28</td><td>LS</td><td>Last Segment Descriptor.
When set, this bit indicates that this is the last descriptor of a received packet, and this descriptor is pointing to the last segment of the packet.</td></tr>
<tr><td>0</td><td>27</td><td>DMAF</td><td>RX DMA Fail.
When set, it indicates this packet is wrong in DMA, and it should be discarded by driver.</td></tr>
<tr><td>0</td><td>26</td><td>FOVF</td><td>FIFO Overflow.
When set, this bit indicates that the receive FIFO was exhausted before this packet was fully received.</td></tr>
<tr><td>0</td><td>25</td><td>SPLCP</td><td>Short Physical Layer Convergence Protocol format.
When set, this bit indicates that a short PLCP preamble was added to the current received frame.</td></tr>
<tr><td>0</td><td>24</td><td>RSVD</td><td>Reserved.</td></tr>
<tr><td>0</td><td>23:20</td><td>RXRATE</td><td>Rx Rate.
These four bits indicate the current frame’s receiving rate.
<table>
<tr><th></th><th></th><th>Bit 23</th><th>Bit 22</th><th>Bit 21</th><th>Bit 20</th><th></th></tr>
<tr><td></td><td>1Mbps</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td></tr>
<tr><td></td><td>2Mbps</td><td>0</td><td>0</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>5.5Mbps</td><td>0</td><td>0</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>11Mbps</td><td>0</td><td>0</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>6Mbps</td><td>0</td><td>1</td><td>0</td><td>0</td><td></td></tr>
<tr><td></td><td>9Mbps</td><td>0</td><td>1</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>12Mbps</td><td>0</td><td>1</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>18Mbps</td><td>0</td><td>1</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>24Mbps</td><td>1</td><td>0</td><td>0</td><td>0</td><td></td></tr>
<tr><td></td><td>36Mbps</td><td>1</td><td>0</td><td>0</td><td>1</td><td></td></tr>
<tr><td></td><td>48Mbps</td><td>1</td><td>0</td><td>1</td><td>0</td><td></td></tr>
<tr><td></td><td>54Mbps</td><td>1</td><td>0</td><td>1</td><td>1</td><td></td></tr>
<tr><td></td><td>Reserved</td><td colspan="4">All other combinations</td><td></td></tr>
</table></td></tr>
<tr><td>0</td><td>19</td><td>RSVD</td><td>Reserved.</td></tr>
<tr><td>0</td><td>18</td><td>MAR</td><td>Multicast Address Packet Received.
When set, this bit indicates that a multicast packet was received.</td></tr>
<tr><td>0</td><td>17</td><td>PAM</td><td>Physical Address Matched.
When set, this bit indicates that the destination address of this Rx packet matches the value in the WLAN ID registers.</td></tr>
<tr><td>0</td><td>16</td><td>BAR</td><td>Broadcast Address Received.
When set, this bit indicates that a broadcast packet was received. BAR and MAR will not be set simultaneously.</td></tr>
<tr><td>0</td><td>15</td><td>RES</td><td>Receive Error.
Valid if DMAF=0</td></tr>
<tr><td>0</td><td>14</td><td>PWRMGT</td><td>Receive Power Management Packet.
When set, this bit indicates that the Power Management bit is set on the received packet.</td></tr>
<tr><td>0</td><td>13</td><td>CRC32</td><td>CRC32 Error.
When set, this bit indicates that a CRC32 error has occurred on the received packet. A CRC32 packet can be received only when RCR_ACRC32 is set.</td></tr>
<tr><td>0</td><td>12</td><td>ICV</td><td>Integrity Check Value Error.
When set, this bit indicates that an ICV error has occurred on the received packet. A ICV packet can be received only when RCR_AICV is set.</td></tr>
<tr><td>0</td><td>11:0</td><td>Frame_Length</td><td>When OWN=0 and LS =1, this bit indicates the received packet length including CRC32, in bytes.</td></tr>
<tr><td>4</td><td>31:27</td><td>RSVD</td><td>Reserved.</td></tr>
<tr><td>4</td><td>26</td><td>WAKEUP</td><td>The received packet is a unicast wakeup packet.</td></tr>
<tr><td>4</td><td>25</td><td>DECRYPTED</td><td>The received packet has been decrypted.</td></tr>
<tr><td>4</td><td>24</td><td>ANTENNA</td><td>The received packet is received through this antenna.</td></tr>
<tr><td>4</td><td>23:16</td><td>AGC</td><td>The AGC of the received packet.</td></tr>
</table>

Offset#	Bit#	Symbol	Description
4	15:8	RSSI	Received Signal Strength Indicator. The RSSI is a measure of the RF energy received by the PHY.
4	7:0	SQ	Signal Quality. The SQ is a measure of the quality of BAKER code lock, providing an effective measure during the full reception of a PLCP preamble and header.
8	31:0	TSFTL	A snapshot of the TSFTR's least significant 32 bits. Valid only when LS is set.
12	31:0	TSFTH	A snapshot of the TSFTR's most significant 32 bits. Valid only when LS is set.

17. Thermal Characteristics

■ Storage and Operating Range:

Parameter	Maximum	Minimum	Units
Storage Temperature	-55	+150	˚C
Ambient Operating Temperature	0	+70	˚C

■ Characteristics:

In this section, we present the thermal characteristic for TFBGA & QFP packages mounted on 4 / 6-layer PCB using the Finite Element Modeling (FEM) method. The PCB size is 160x100 / 80x50 mm. The junction-to-ambient thermal resistance is utilized to evaluate thermal performance for this package and then to predict the power dissipation capability by given ambient and maximum junction temperatures.

■ Terminology:

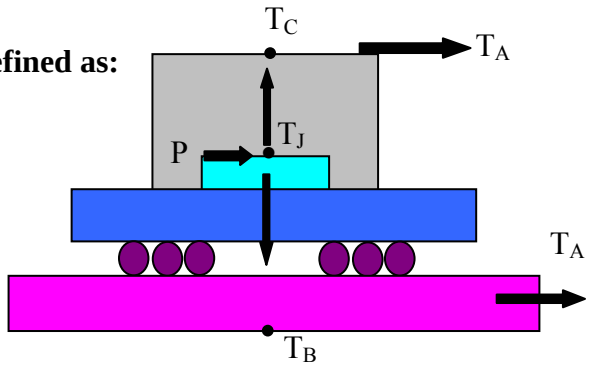
The major thermal dissipation paths can be illustrated as following

***T_J*: the maximum junction temperature;**
***T_A*: the ambient or environment temperature;**
***T_C*: the maximum compound surface temperature;**
***T_B*: the maximum surface temperature of PCB bottom;**
***P*: total input power**

The thermal parameter can be define as following

1. *BGA Junction to ambient thermal resistance, θ_{JA}*, **defined as:**

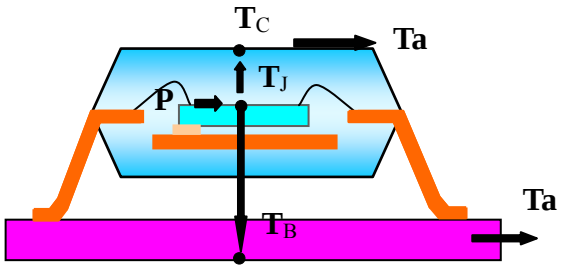
$$\theta_{JA} = \frac{T_J - T_A}{P} \; ; \qquad (1)$$



Thermal Dissipation of BGA package

2. *QFP Junction to ambient thermal resistance,* θ_{JA}**, defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \; ; \qquad (1)$$



Thermal Dissipation of QFP package

■ **Result Summaries:**

	0 m/s	1 m/s	2 m/s	3 m/s
Theta JA, 4L PCB	33	28.6	27.7	27.1
Theta JA, 6L PCB	38.2	29.4	28	27.3
Psi JT, 4L PCB	5	5.9	6.5	6.6
Psi JT, 6L PCB	5.2	6.1	6.7	6.9

Thermal Performance of QFP208 under air flow conditions

PKG type	PCB	Theta JA	Psi JT	Power	Ta	Tj	Tc
QFP208	4L PCB	33	5	1.78	25	83.7	74.84
QFP208	6L PCB	38.2	5.2	1.78	25	93	83.74

	0 m/s	1 m/s	2 m/s	3 m/s
Theta JA, 4L PCB	30.4	27.9	26.7	26
Theta JA, 6L PCB	27.7	24.3	22.7	21.8
Psi JT, 4L PCB	2	2.4	2.6	3
Psi JT, 6L PCB	1.9	2.3	2.4	2.8

Thermal Performance of TFBGA292 under air flow conditions

PKG type	PCB	Theta JA	Psi JT	Power	Ta	Tj	Tc
TFBGA292	4L PCB	30.4	2	1.78	25	79.1	75.55
TFBGA292	6L PCB	27.7	1.9	1.78	25	74.3	70.92

18. DC Characteristics

Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table . Electrical Characteristics/Ratings

Parameter	Min	Max	Units
Vcc Supply Referenced to GND	-0.5	+4.0	V
Digital Input Voltage	-0.5	VDD	V
DC Output Voltage	-0.5	VDD	V

Operating Range

Parameter	Min	Typical	Max	Units
3.3 Vcc Supply Voltage Range	3.15	3.3	3.45	V
1.8 Vcc Supply Voltage Range	1.7	1.8	1.9	V

Power Dissipation

Parameter	SYM	Typical	Units
Power Supply Current for Digital and analog 3.3V	Icc	170	mA
Power Supply Current for Digital 1.8	Icc	380	mA

SDRAM Bus DC Parameters

Table . SDRAM Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage	LVTTL	2.0			V	1
V_{IL}	Input-low voltage	LVTTL			0.8	V	2
V_{OH}	Output-high voltage		2.4			V	3
V_{OL}	Output-low voltage				0.4	V	3
I_{IL}	Input-leakage current	V_{IN}= 3.3V or 0	-10	±1	10	µA	
I_{OZ}	Tri-state Output-leakage current		-10	±1	10	µA	
R_{PU}	Input Pull-up resistance			75		KΩ	4
R_{PD}	Input Pull-down resistance			75		KΩ	4

Note 1: V_{IH} overshot: $V_{IH\,(MAX)}$=V_{DDH} + 2V for a pulse width ≤3ns, and the pulse width cannot be greater than one third of the cycle rate.

Note 2: V_{IL} undershot: $V_{IL\,(MIN)}$=-2V for a pulse width ≤3ns cannot be exceeded.

Note 3: The output current buffer is 16mA for SDRAM clock, address, and data bus.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

Flash Bus DC Parameters

Table . Flash Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage	LVTTL	2.0			V	1
V_{IL}	Input-low voltage	LVTTL			0.8	V	2
V_{OH}	Output-high voltage		2.4			V	3
V_{OL}	Output-low voltage				0.4	V	3
I_{IL}	Input-leakage current	V_{IN}= 3.3V or 0	-10	±1	10	µA	

I_{OZ}	Tri-state Output-leakage current		-10	±1	10	µA	
R_{PU}	Input Pull-up resistance			75		KΩ	4
R_{PD}	Input Pull-down resistance			75		KΩ	4

Note 1: VIH overshot: VIH (MAX)=VDDH + 2V for a pulse width ≤3ns cannot be exceeded.
Note 2: V_{IL} undershot: $V_{IL\ (MIN)=}$-2V for a pulse width ≤3ns cannot be exceeded.
Note 3: The output current buffer is 16 mA for the flash address and data bus; and is 8mA for Flash control signals.
Note 4: These values are typical values checked in the manufacturing process and are not tested.

PCI DC Parameters

Table . PCI DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage	LVTTL	2.0			V	3
V_{IL}	Input-low voltage	LVTTL			0.8	V	3
V_{OH}	Output-high voltage		2.4			V	1, 3
V_{OL}	Output-low voltage				0.4	V	1, 3
I_{IL}	Input-leakage current	V_{IN}= 3.3V or 0	-10	±1	10	µA	2, 3
I_{OZ}	Tri-state Output-leakage current		-10	±1	10	µA	2, 3
R_{PU}	Input Pull-up resistance			75		KΩ	2, 3
R_{PD}	Input Pull-down resistance			75		KΩ	2, 3

Note 1: The output current buffer is: 8mA for the PCI clock, and 4mA for other PCI related signals.
Note 2: These values are typical values checked in the manufacturing process and are not tested.
Note 3: For additional information, see the PCI Local Bus Specification, Revision 2.2.

UART DC Parameters

Table . UART DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage	LVTTL	2.0			V	
V_{IL}	Input-low voltage	LVTTL			0.8	V	
V_{OH}	Output-high voltage		2.4			V	1
V_{OL}	Output-low voltage				0.4	V	1
I_{IL}	Input-leakage current	V_{IN}= 3.3V or 0	-10	±1	10	µA	2
R_{PU}	Input Pull-up resistance			75		KΩ	2
R_{PD}	Input Pull-down resistance			75		KΩ	2

Note 1: The output current buffer is 4mA for UART related signals.
Note 2: These values are typical values checked in the manufacturing process and are not tested.

GPIO DC Parameters

Table . GPIO DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage	LVTTL	2.0			V	
V_{IL}	Input-low voltage	LVTTL			0.8	V	
V_{OH}	Output-high voltage		2.4			V	1
V_{OL}	Output-low voltage				0.4	V	1
I_{IL}	Input-leakage current		-10	±1	10	μA	2
R_{PD}	Input Pull-down resistance			75		KΩ	2

Note 1: The output current buffer is 4mA for GPIO related signals.
Note 2: These values are typical values checked in the manufacturing process and are not tested.

JTAG DC Parameters

Table . JTAG DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage	LVTTL	2.0			V	
V_{IL}	Input-low voltage	LVTTL			0.8	V	
V_{OH}	Output-high voltage	$\lvert I_{OH} \rvert$ =2~16mA	2.4			V	1
V_{OL}	Output-low voltage	$\lvert I_{OL} \rvert$ =2~16mA			0.4	V	1
I_{IL}	Input-leakage current		-10	±1	10	μA	2
R_{PD}	Input Pull-down resistance			75		KΩ	2

Note 1: The output current buffer is 4mA for JTAG related signals.
Note 2: These values are typical values checked in the manufacturing process and are not tested.

MII DC Parameters

Table . MII Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-high voltage	LVTTL	2.0			V	
V_{IL}	Input-low voltage	LVTTL			0.8	V	
V_{OH}	Output-high voltage		2.4			V	1
V_{OL}	Output-low voltage				0.4	V	1
I_{IL}	Input-leakage current	V_{IN}= 3.3V or 0	-10	±1	10	μA	2
I_{OZ}	Tri-state Output-leakage current		-10	±1	10	μA	2
R_{PU}	Input Pull-up resistance			75		KΩ	2
R_{PD}	Input Pull-down resistance			75		KΩ	2

Note 1: The output current buffer is 4mA for MII related signals and 8mA for MDC clock.
Note 2: These values are typical values checked in the manufacturing process and are not tested.

Reset DC Parameters

Table . Reset DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0			V	
V_{IL}	Input-Low Voltage	LVTTL			0.8	V	

LED DC Parameters

Table . LED DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{OHED}	Output-High Voltage		2.4			V	1
V_{OLLED}	Output-Low Voltage				0.4	V	1

Note: The output current buffer for LED signals is 8mA.

19. AC Characteristics

SDRAM Clock Timing

Table . SDRAM Clock Timing

Symbol	Parameter	50~140MHz			Units	Notes
		Min. (140Mhz)	Typ. (130Mhz)	Max. (50Mhz)		
$T_{PERIOD\_SDRAMCLK}$	Clock period for SDRAM clock	7.14	7.7	20	ns	
$T_{CLKHIGH}$	SDRAM clock high time	3.57	3.57`	3.57	ns	
T_{CLKLOW}	SDRAM clock low time	3.57	3.57	3.57	ns	
$T_{RISE/FALL}$	Rising and falling time requirements for SDRAM clock			2	ns	
$T_{RISE/FALL\_OUTPUT}$	Propagation delay for output rising and falling		N.A.		ns	

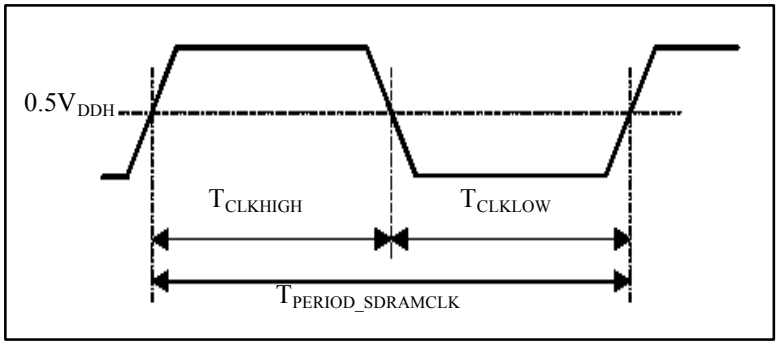


Figure . SDRAM Clock Specifications-1

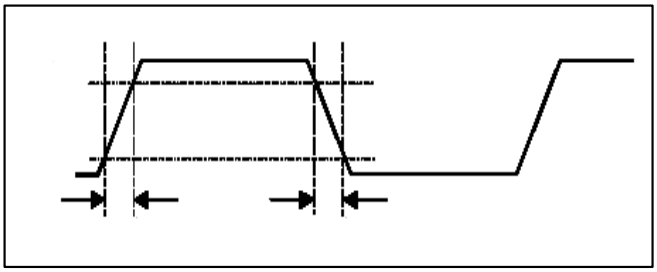


Figure . SDRAM Clock Specifications-2

PCI Clock Timing

Table . PCI Clock Timing

Symbol	Parameter	33MHz			Units	Notes
		Min.	Typ.	Max.		
T_{PERIOD_PCICLK}	Clock period for PCI clock		30		ns	
$T_{CLKHIGH}$	PCI clock high time		15		ns	
T_{CLKLOW}	PCI clock low time		15		ns	
$T_{RISE/FALL}$	Rise and fall time requirements for PCI clock			2	ns	
$T_{RISE/FALL\_OUTPUT}$	Propagation delay for output rising and falling		N.A.		ns	

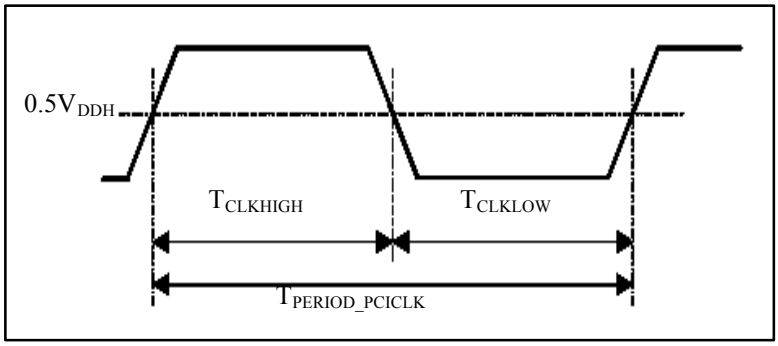


Figure . PCI Clock Specifications-1

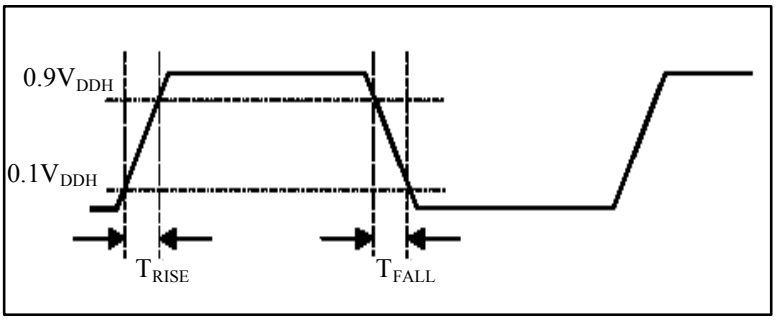


Figure . PCI Clock Specifications-2

MII Clock Timing

Table . MII Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{PERIOD100Mbit}$	Clock period for Tx and Rx Ethernet clocks		25	25		
$T_{PERIOD10Mbit}$	Clock period for Tx and Rx Ethernet clocks		2.5	2.5	MHz	
T_{DUTY}	Duty cycle for Tx and Rx Ethernet clocks	35	50	65	%	
$T_{RISE/FALL}$	Rise and fall time requirement for Tx and Rx Ethernet clocks			2	ns	
$T_{RISE/FALL\_OUTPUT}$	Propagation delay for output rising and falling		N.A.		ns	

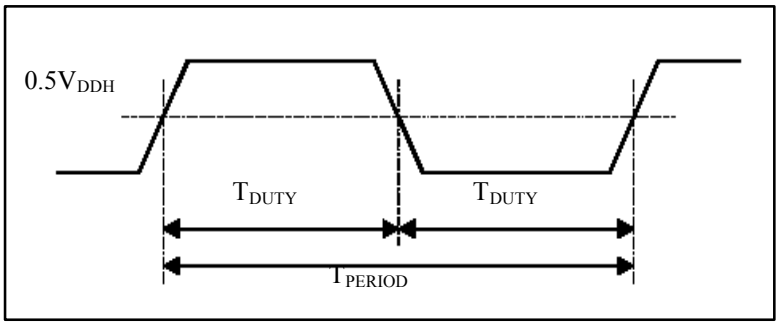


Figure . MII Clock Specifications-1

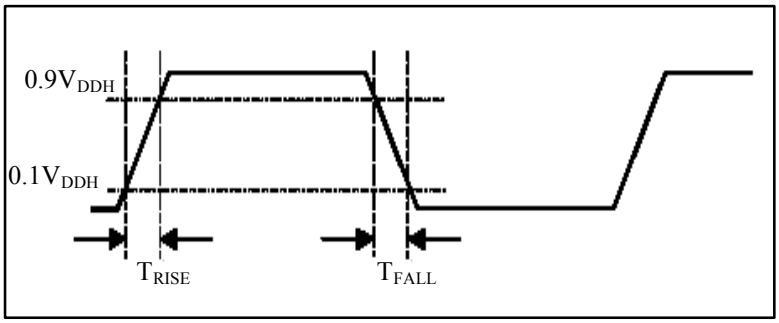


Figure . MII Clock Specifications-2

SDRAM Bus Timing

Table . SDRAM Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{CLK2OUT}$	Rising edge of clock-to-signal output. Outputs include this timing are D[31: 0], CS0#, CS1#,RAS#, CAS#, LDQM, UDQM, WE# (during a write operation).			3	ns	1
$T_{HOLDOUT}$	Signal output hold time after the rising edge of the clock. Outputs included in this timing are D[31: 0] (during a write operation).	1			ns	1

Note 1: Timing was tested with 75-pF capacitor to ground.

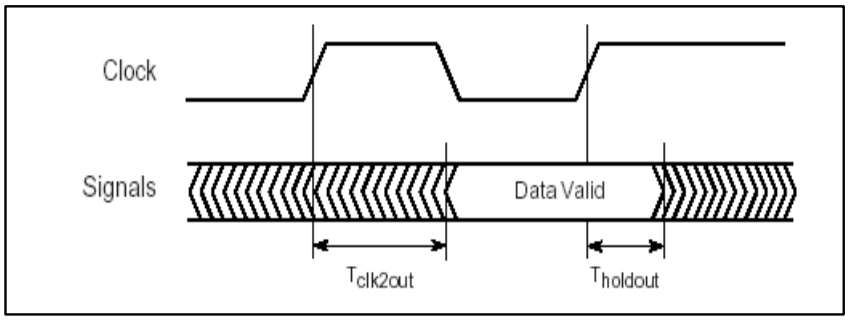


Figure . SDRAM Output Timing

Table . SDRAM Access Control Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{REFRESH}$	Auto-refresh timing.	Controlled by Reg. 0xBD01_1000 (MCR)			µs	
T_{RCD}	The time interval between RAS# active and CAS# active.	Controlled by Reg. 0xBD01_1008 (MTCR1)			ns	
T_{RP}	The time interval between pre-charge and the next active.	Controlled by Reg. 0xBD01_1008 (MTCR1)			ns	
T_{RAS}	The time interval between active and pre-charge.	Controlled by Reg. 0xBD01_1008 (MTCR1)			ns	
T_{RC}	The time interval between active and the next active.	Controlled by Reg. 0xBD01_1008 (MTCR1)			ns	1
T_{RFC}	The time interval between auto-refresh and active.	Controlled by Reg. 0xBD01_1008 (MTCR1)			ns	
$T_{CAS\_LATENCY}$	The data output delay after The CAS# active.	Controlled by Reg. 0xBD01_1000 (MCR)			ns	

Note 1: TRC=TRAS + TRP.

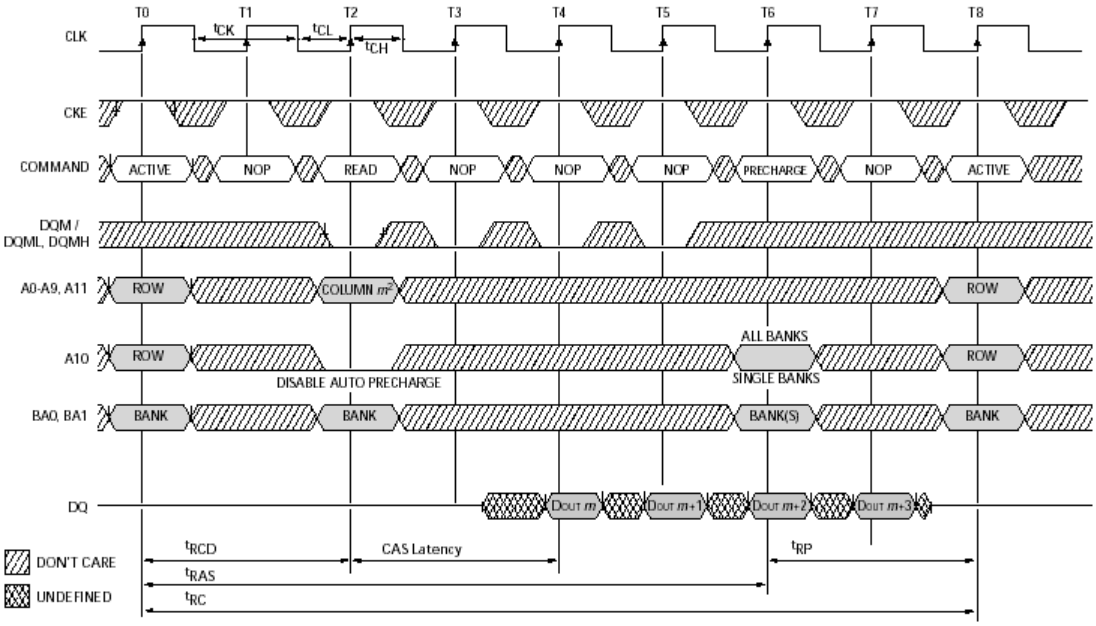


Figure . SDRAM Access Control Timing

Flash Bus Timing

Table . Flash Access Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{CS}	The timing interval between F_CS0#(or F_CS1#) and WE#	Controlled by Reg. 0xBD01_1004 (MTCR0)			ns	
T_{WP}	The timing interval for WE# to pulled low (RAS# for read operation).	Controlled by Reg. 0xBD01_1004 (MTCR0)			ns	

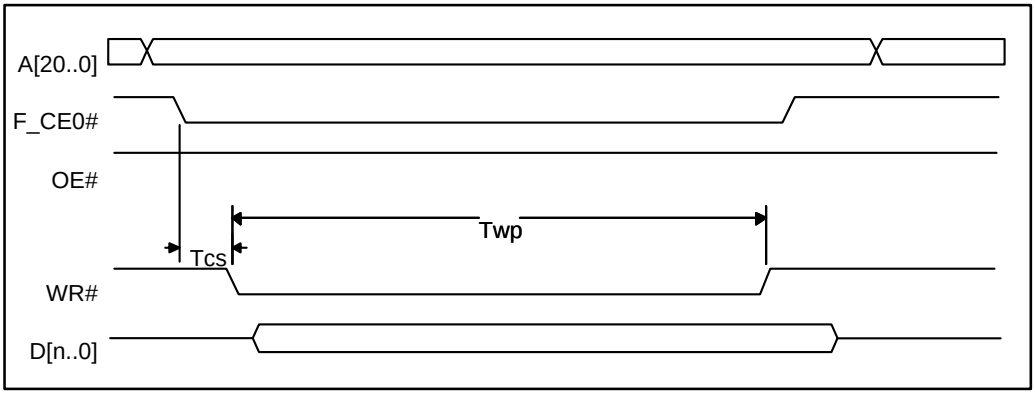


Figure . Flash Access Timing

PCI Bus Timing

Table . PCI Bus Signal Timing

Symbol	Parameter	33MHz			Units	Notes
		Min.	Typ.	Max.		
$T_{CLK2OUTB}$	Clock to output for all bused signals. This is the PAD[0:31], BE[0:3]#, FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, INTA#, PAR	2		7	ns	1, 2, 5, 7, 8
$T_{CLK2OUT}$	Clock to output for all point-to-point signals. This is the GNT[0:1]#, REQ[0:1]# only	2		7	ns	1, 2, 5, 7, 8
T_{SETUPB}	Input setup time for all bused signals. This is the PAD[0:31], BE[0:3]#, FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, INTAB, PAR	6			ns	4, 6, 7, 8
T_{SETUP}	Input setup time for all point-to-point signals. This is the GNT[0:1]#, REQ[0:1]# only	10			ns	4, 7, 8
T_{HOLD}	Input hold time from clock	1			ns	4, 7, 8
$T_{RST-OFF}$	Reset active-to-output float delay			40	ns	5, 6, 7, 8

Note 1: See the timing measurement conditions.
Note 2: Parts compliant to 3.3V signal environment.
Note 3: REQ# and GNT# are point-to-point signal and have different output valid delay and input setup time than do bused signal.
Note 4: RST# is asserted and de-asserted asynchronously with respect to PCICLK.
Note 5: All PCI outputs must be asynchronously driven to a tri-state when RST# is active.
Note 6: Setup time applies only when the device is not driving the pin. The device cannot drive and receive signals at the same time.
Note 7: Timing was tested with a 70-pF capacitor to ground.
Note 8: For additional information, see the PCI LOCAL BUS Specification, Revision 2.2.

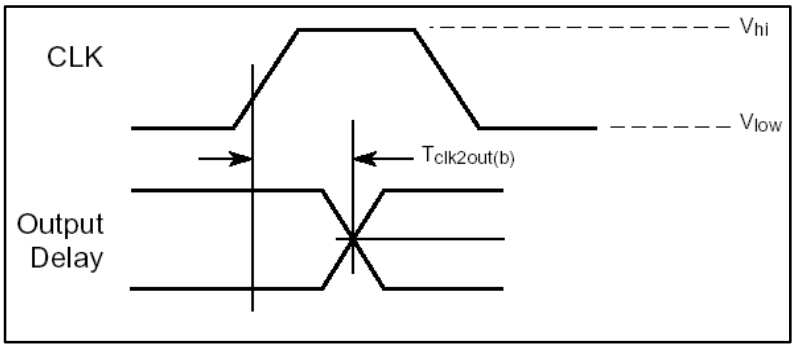


Figure . PCI Output Timing-1

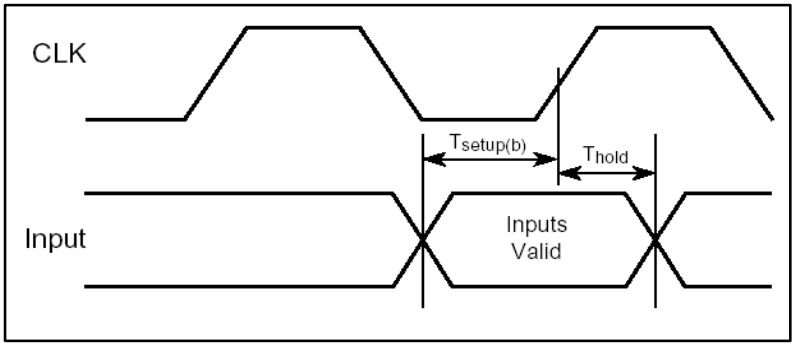


Figure . PCI Input Timing-2

MII Interface Timing

Table. MII Output Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_1	Clock rising edge to output delay for TXD[3:0] and TXEN (for RTL8186 MII MAC mode)			12	ns	
T_1	TXD[3:0] and TXEN setup time prior to rising edge of TXCLK (for RTL8186 MII PHY mode)	17			ns	
T_2	TXD[3:0] and TXEN setup time prior to rising edge of TXCLK (for RTL8186 MII PHY mode)	21			ns	

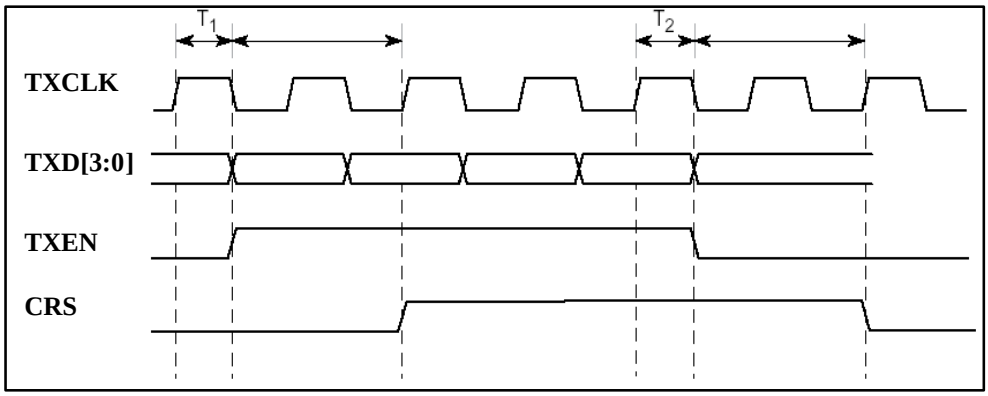


Figure . MII Output Timing

Table . MII Input Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_3	RXD[3:0] and RXDV setup time prior to rising edge of RXCLK	10			ns	
T_4	RXD[3:0] and RXDV hold time after the rising edge of RXCLK	10			ns	

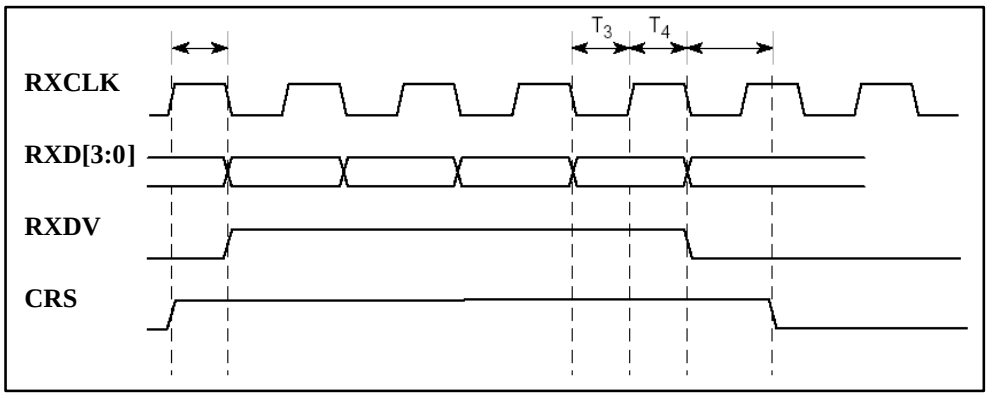


Figure . MII Input Timing

JTAG Interface Timing

Table . Boundary-Scan Interface Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{BSCL}	JTAG clock low time	50			ns	1
T_{BSCH}	JTAG clock high time	50			ns	1
T_{BSIS}	TDI, TMS setup time to rising edge of TCK	10			ns	
T_{BSIH}	TDI, TMS hold time from rising edge of TCK	10			ns	
T_{BSOH}	TDO hold time after falling edge of TCK	1.5			ns	
T_{BSOD}	TDO output from falling edge of TCK			40	ns	
T_{BSR}	JTAG reset period	30			ns	
T_{BSRS}	TMS setup time to rising edge of JTAG reset	10			ns	
T_{BSRH}	TMS hold time from rising edge of JTAG reset	10			ns	

Note: JTAG clock TCK may be stopped indefinitely in either the low or high phase.

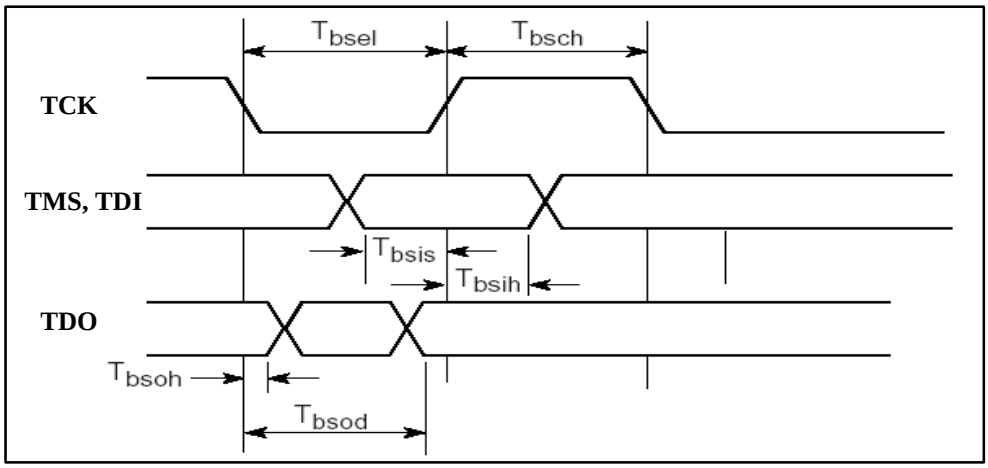


Figure. Boundary-Scan General Timing

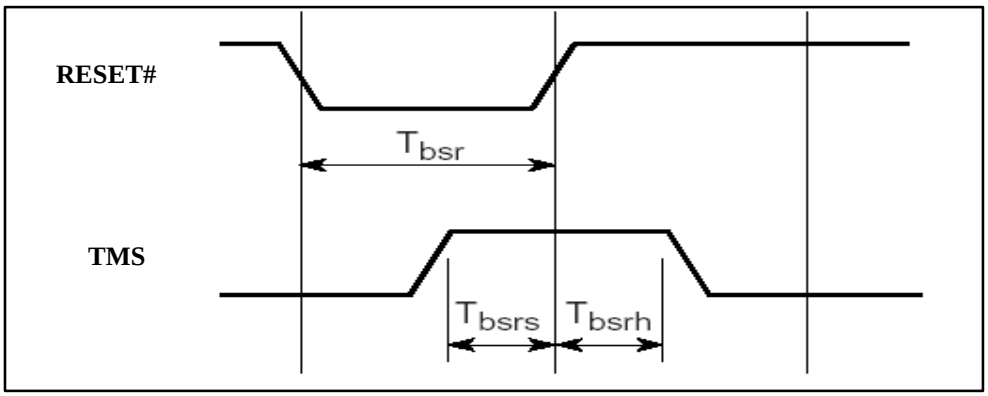


Figure. Boundary-Scan Reset Timing

20. Design and Layout Guide

In order to achieve maximum performance using the RTL8186/RTL8186P, good design attention is required throughout the design and layout process. The following are some recommendations on how to implement a high performance system.

General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<50mV).
- Keep power and ground noise levels below 50mV.
- Use bulk capacitors (4.7µF-10µF) between the power and ground planes.
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8186/RTL8186P chip.

Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other. Run orthogonally or separate by a ground plane.

Clock Circuit

- If possible, surround the clock by ground trace to minimize high-frequency emissions.
- Keep the crystal or oscillator as close to the RTL8186/RTL8186P as possible.

Power Plane

- Divide the power plane into 1.8V digital, 3.3V analog, and 3.3V digital.
- Use 0.1µF decoupling capacitors and bulk capacitors between each power plane and the ground plane.

Ground Plane

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.

RF Interface

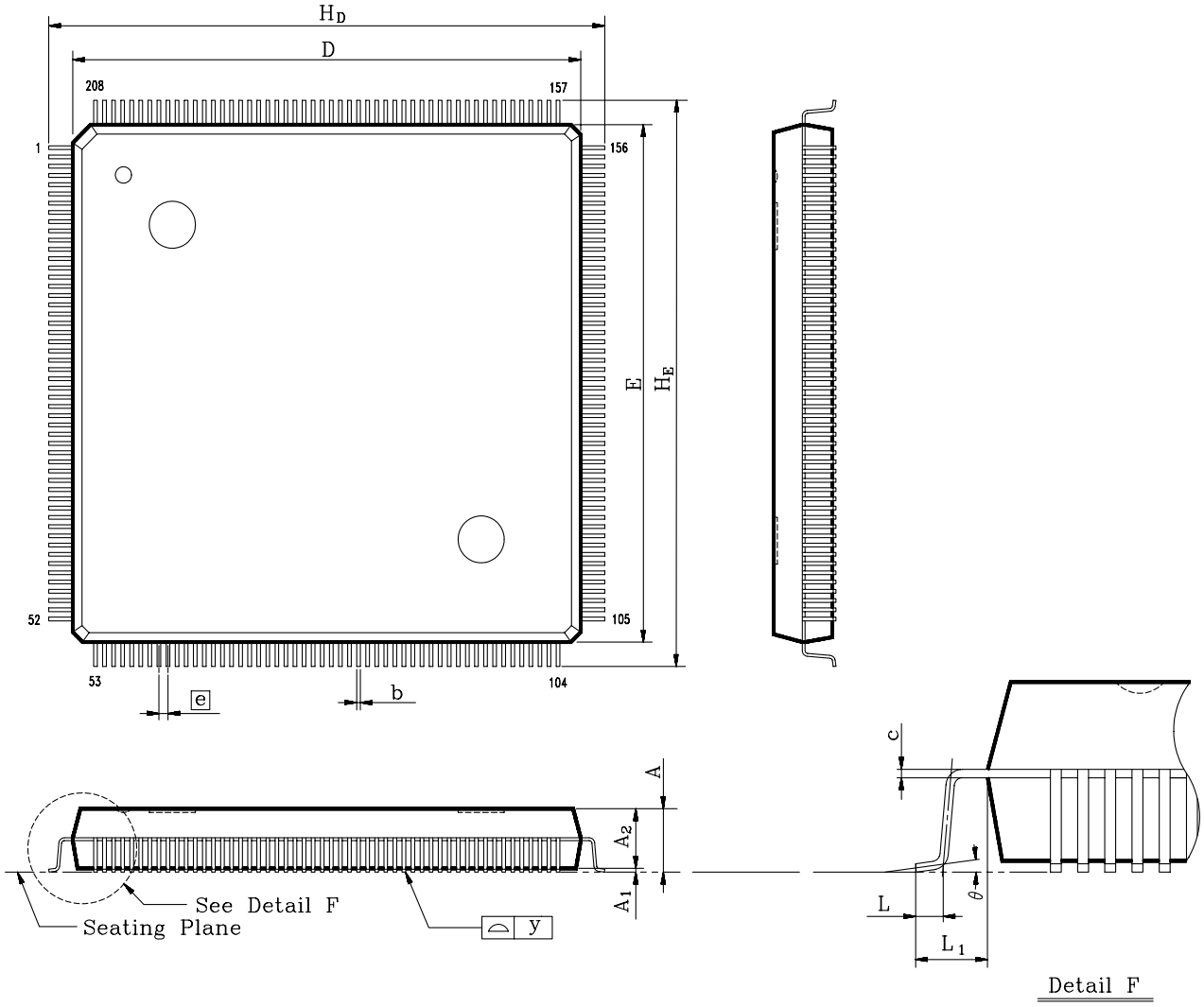
- As the RF interface is complex and power noise sensitive, we strongly recommend customers to hard copy the RF design from Realtek.

Memory Interface

- Keep the SDRAM as close as possible to the RTL8186/RTL8186P. The FLASH timing is slower than SDRAM so place the SDRAM closer than FLASH if space considerations prevent placing both components equally close to the RTL8186/RTL8186P.
- Where two banks of SDRAM are used, the memory clock trace should have the same length.

21. Mechanical Dimensions

Package Outline for 208 LQFP (28*28*1.4mm)



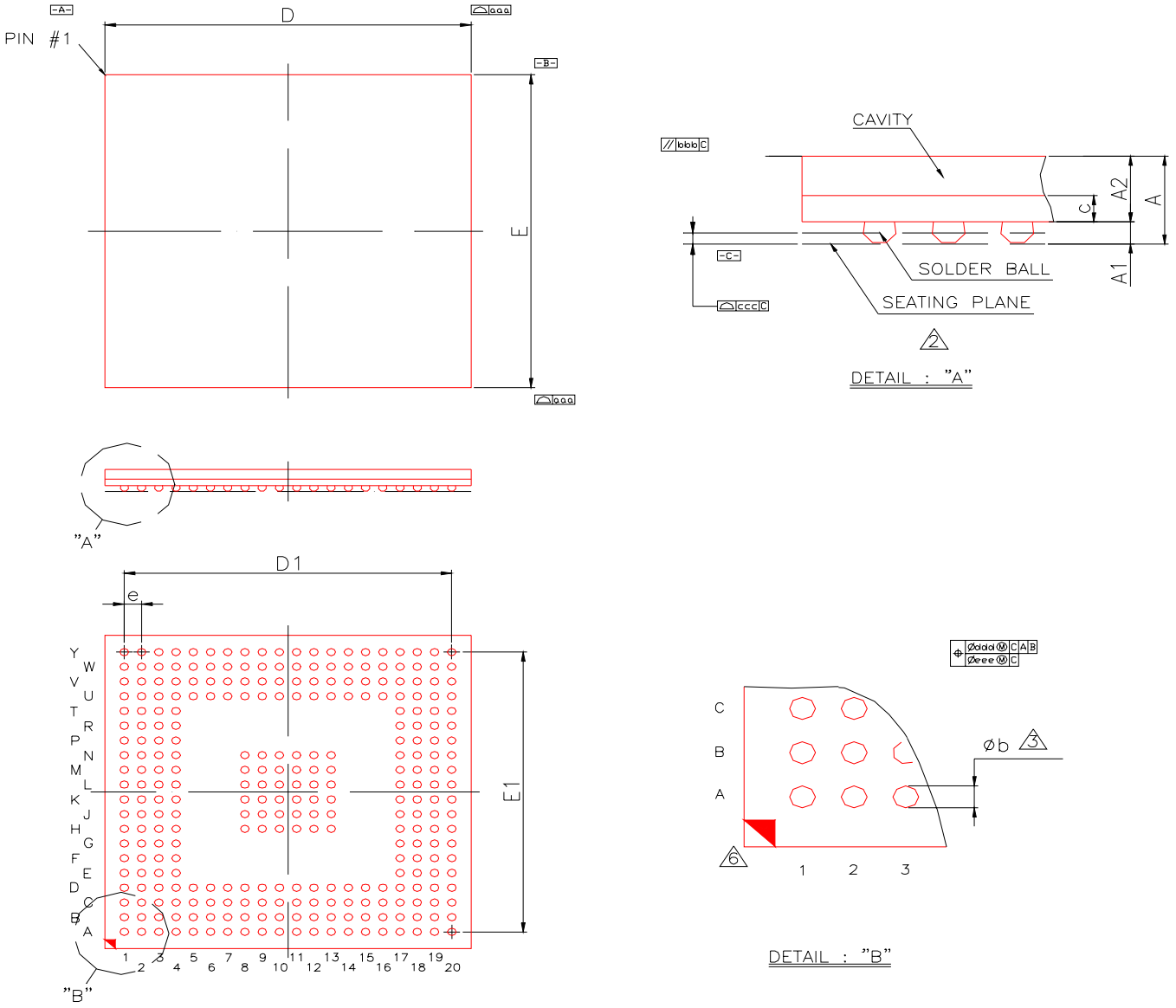
Notes for 208 LQFP

Symbol	Dimension in inch			Dimension in mm		
	Min	Typ	Max	Min	Typ	Max
A	0.136	0.144	0.152	3.45	3.65	3.85
A1	0.004	0.010	0.036	0.10	0.25	0.91
A2	0.119	0.128	0.136	3.02	3.24	3.46
b	0.004	0.008	0.012	0.10	0.20	0.30
c	0.002	0.006	0.010	0.04	0.15	0.26
D	1.093	1.102	1.112	27.75	28.00	28.25
E	1.093	1.102	1.112	27.75	28.00	28.25
e	0.012	0.020	0.031	0.30	0.50	0.80
HD	1.169	1.205	1.240	29.70	30.60	31.50
HE	1.169	1.205	1.240	29.70	30.60	31.50
L	0.010	0.020	0.030	0.25	0.50	0.75
L1	0.041	0.051	0.061	1.05	1.30	1.55
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : 208L QFP (28x28 mm*2) FOOTPRINT 2.6mm			
PACKAGE OUTLINE DRAWING			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	
		PAGE	
CHECK		DWG NO.	
		DATE	
REALTEK SEMICONDUCTOR CORP.			

Package Outline for TFBGA 292 BALL (17*17 mm)



Notes for TFBGA 292 BALL

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.30	---	---	0.051
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	013	0.014	0.016
D	16.90	17.00	17.10	0.665	0.669	0.673
E	16.90	17.00	17.10	0.665	0.669	0.673
D1	---	15.20	---	---	0.598	---
E1	---	15.20	---	---	0.598	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.10			0.004		
bbb	0.10			0.004		

Notes:

1. CONTROLLING DIMENSION: MILLIMETER
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT: JEDEC MO-205.
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

TITLE : 292LD TFBGA (17x17mm) PACKAGE OUTLINE
SUBSTRATE MATERIAL: BT RESIN

ccc	0.12	0.005
ddd	0.15	0.006
eee	0.08	0.003
MD/ME	20/20	20/20

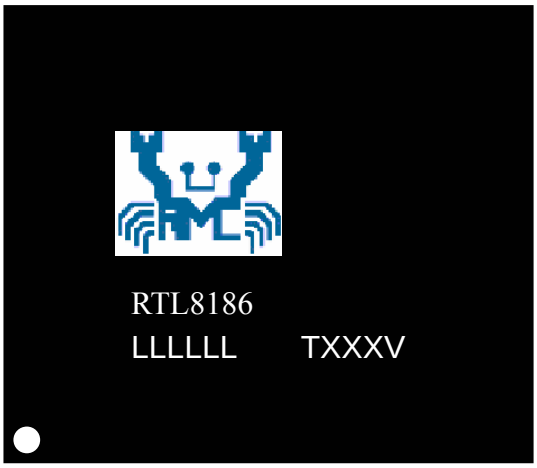
APPR.		DWG NO.	
ENG.		Rev NO	
QM.		PRODUCT CODE	
CHK.		DAT	
DWG.		SHT I	
REALTEK SEMICONDUCTOR CORP.			

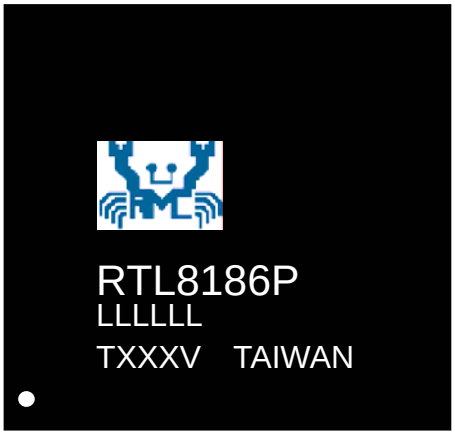
20. Ordering Information

Part Number	Package	Status
RTL8186	208-pin PQFP	MP
RTL8186-LF	208-pin PQFP Lead(Pb)-Free	MP
RTL8186P	292-pin TFBGA	MP
RTL8186P-LF	292-pin TFBGA Lead(Pb)-Free	MP

21. Package Identification

Lead(Pb)-free package is indicated by an “L” in the location marked “T” in the following figures.





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