RTL8305SB-D

SINGLE CHIP 5-PORT 10/100MBPS SWITCH CONTROLLER WITH DUAL MII INTERFACES

DEMO BOARD USER GUIDE

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USING THIS DOCUMENT

This document provides detailed user guidelines to achieve the best performance when implementing a 2-layer board PC design with the RTL8305SB-D 5-port 10/100Mbps single chip switch controller.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2003/03/01	First release.

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1. General Description

The RTL8305SB-D is a Fast Ethernet switch that integrates memory, five MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip. To benefit BOM costs, one external PNP transistor is used to generate a 2.5V power source. The fifth port (port 4) supports an external MAC interface, which can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with a routing engine, HomePNA, or VDSL transceiver. The MII interface layout also plays an important part in the system PCB design.

2. Jumper & Connector Locations

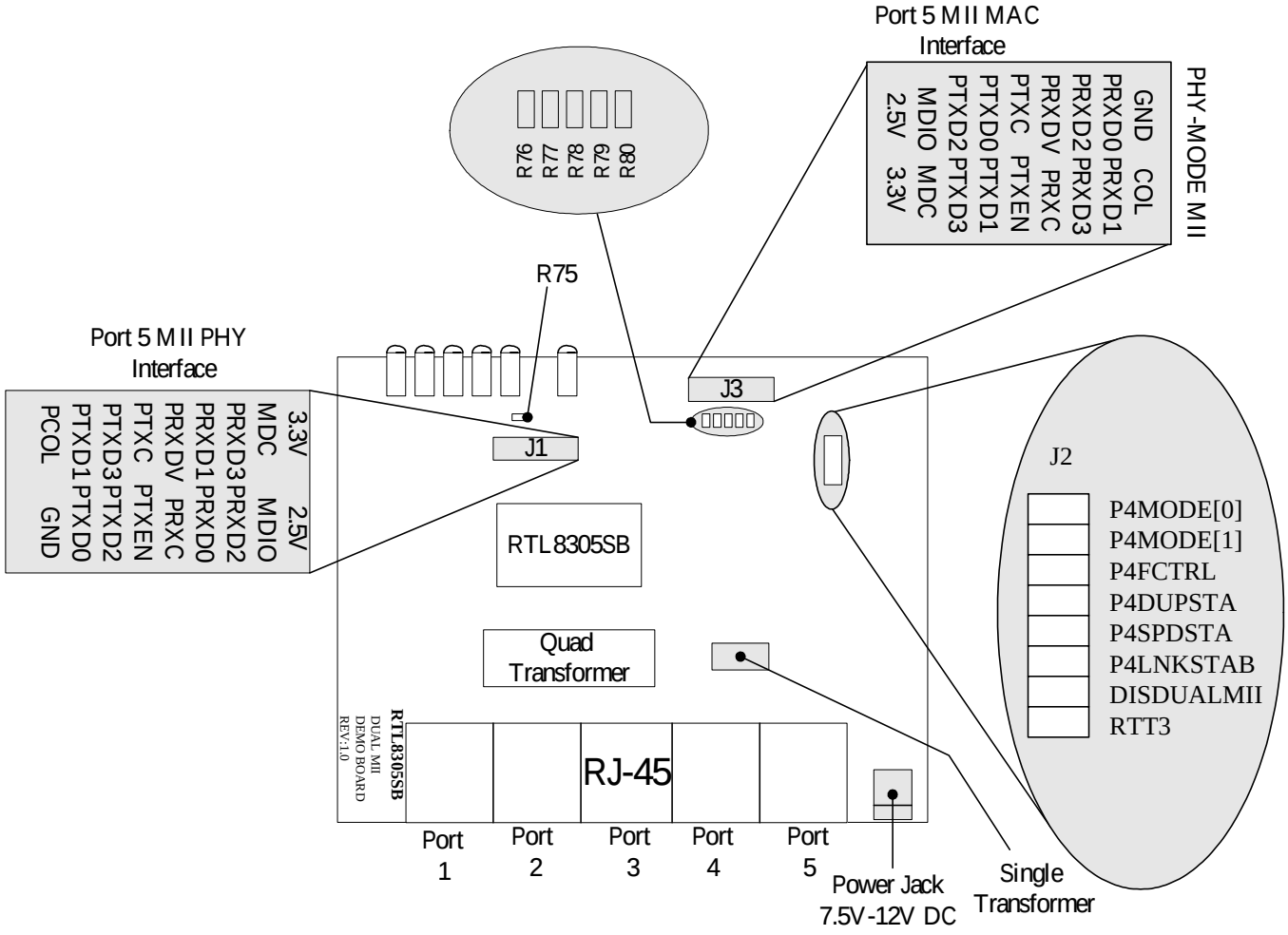
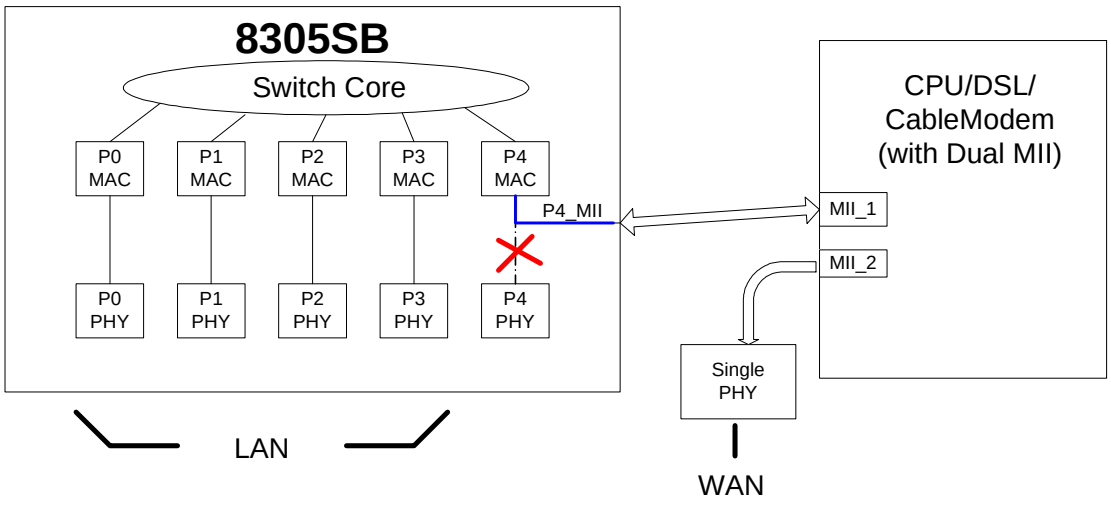


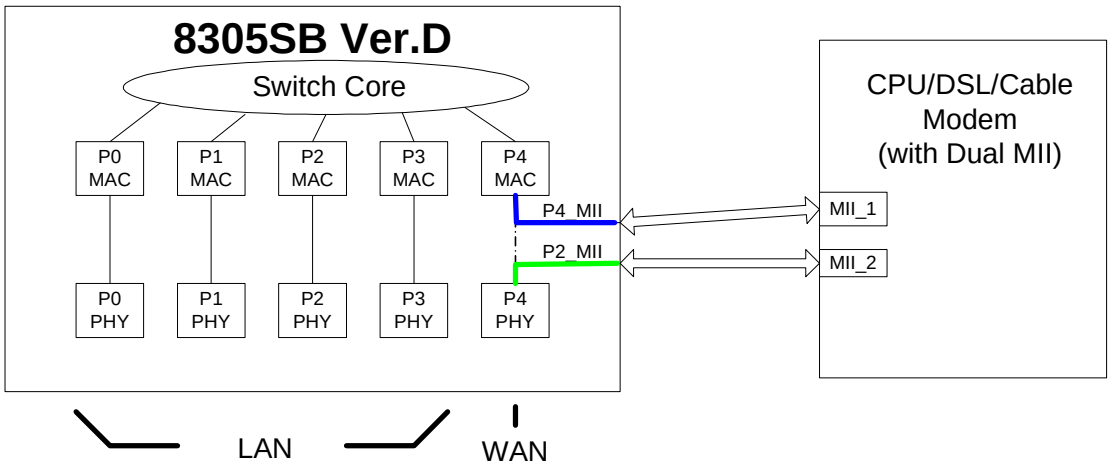
Figure 1. Jumper & Connector Locations/Pin Assignments

3. Mode Settings Overview

- The RTL8305SB-D supports a dual MII interface for Gateway/Router applications as shown in Figure 2, page 3.
- The RTL8305SB-D features 5 MAC and 5 PHY transceivers on a single chip. The fifth MAC supports PHY-Mode MII and SNI interface to connect with a CPU/DSL/Cable Modem chip supporting an Ethernet MII interface. This fifth MAC also supports MAC-Mode MII for connecting to HomePNA PHYceivers or VDSL PHYceivers. This function is the same as that of the RTL8305SB Rev. C.
- If DISDUALMII (Pin42) is tied to VDD (2.5V) and P4 MAC is operated in PHY-Mode MII for single MII operation, the PHY address = 4 when reading P4 MAC MII register 0.8, 0.13, and 1.2 via the SMI interface (MDC/MDIO).
- If DISDUALMII (Pin42) is tied to ground to enable the DUAL MII function, and the P4 MAC is operated in PHY mode MII for MII operation, then the PHY address = 5 when reading P4 MAC MII register 0.8, 0.13, 1.2, Reg.4, and Reg.5 via the SMI interface (MDC/MDIO).
- The operating mode of fifth MAC (P4 MAC) and fifth PHY (P4 PHY) may be set via DISDUALMII, P4MODE [1:0] signals as shown in Table 1, page 4.
- In PHY-Mode MII operation of the P4 MAC, the P4 MAC may be operated in force mode by setting P4LNKSTA# (Pin 49), P4DUPSTA (Pin 48), P4SPDSTA (Pin 47) and P4FLCTRL (Pin 46) as shown in Table 3, page 5.
- In the RTL8305SB-D, the fifth PHY transceiver (P4 PHY) supports a second MII interface (signal name: PHY2Pxxxx) as a standalone Ethernet PHYceiver (same as the RTL8201BL) when DISDUALMII (Pin 42) is tied to Ground.
  The fifth PHY transceiver (P4 PHY) supports auto-negotiation in UTP mode, and the MII Register may be accessed via the SMI interface (MDC/MDIO) when PHY address = 4.
- Don’t assemble R75, R76, R77, R78, R79, and R80 when the P4 MAC MII interface is disabled or in a 5-port dumb switch application. Assemble these resisters when the MII interface is enabled. The resistor’s location is shown in Figure 1, page 1.
- If the RTL8305SB-D is operated as a 5-port dumb Switch, leave Jumper Block 2 jumpers DISDUALMII, P4LNKSTAB, P4SPDSTA, P4DUPSTA, P4FCTRL, P4MODE[1] and P4MODE[0] open.



Single MII Application



Dual MII Application

Figure 2. Single & Dual MII Applications

Table 1. Port 4 Mode Setting Table

Name	DISDUALMII	P4MODE [1]	P4MODE [0]	RESERVED1
Component Location	J2.3, J2.4	J2.13, J2.14	J2.15, J2.16	R1
5-Port Dumb Switch	Open	Open	Open	NC
Enable Dual MII (P4MAC = MAC Mode, P4PHY = UTP Mode)	Short	Open	Open	1K
Enable Dual MII (P4MAC = MAC Mode, P4PHY = 100FX Mode)	Short	Open	Short	1K
Enable Dual MII (P4MAC = PHY Mode, P4PHY = UTP Mode)	Short	Short	Open	1K
Enable Dual MII (P4MAC = SNI Mode, P4PHY = UTP Mode)	Short	Short	Short	1K
Single MII (P4Mac = MAC Mode)	Open	Open	Open	1K
Single MII (P4Mac = 100FX Mode)	Open	Open	Short	1K
Single MII (P4Mac = PHY Mode)	Open	Short	Open	1K
Single MII (P4Mac = SNI Mode)	Open	Short	Short	1K

3.1. P4 MAC in MII Mode (MAC-MODE MII/PHY-MODE MII)

Table 2. P4 MAC in MII Mode (MAC-MODE MII/PHY-MODE MII)

P4MAC=MII	100M-Full	100M-Half	10M-Full	10M-Half
P4LNKSTAB (J2.5, J2.6)	Short	Short	Short	Short
P4DUPSTA (J2.9, J2.10)	Open	Short	Open	Short
P4SPDSTA (J2.7, J2.8)	Open	Open	Short	Short
P4FCTRL (J2.11, J2.12)	Open for Enable Flow Control, Short for disable	Open	Open for Enable Flow Control, Short for disable	Open

3.2. P4 MAC in PHY-MODE SNI Mode

Table 3. P4 MAC in PHY-MODE SNI Mode

P4MAC=SNI	10M-Full	10M-Half
P4LNKSTA# (J2.5, J2.6)	Short	Short
P4DUPSTA (J2.9, J2.10)	Open	Short
P4SPDSTA (J2.7, J2.8)	Short	Short
P4FCTRL (J2.11, J2.12)	Open for Enable Flow Control, Short for Disable	Short

3.3. Example 1

Enable Dual MII function for P4 MAC = PHY-Mode MII and force to 100M-Full, Flow control Enabled, and P4 PHY = PHY MII.

3.3.1. Example 1 Settings (J2 Jumper Block)

Table 4. Example 1 Settings (J2 Jumper Block)

J2 Label Name	Jumper	Function
PTT3	Open	Reserved
DISDUALMII	Short	Enable Dual MII
P4LNKSTAB	Short	Force Link On
P4SPDSTA	Open	Speed = 100M
P4DUPSTA	Open	Duplex = Full duplex
P4FCTRL	Open	Enable Flow Control
P4MODE[1]	Short	PHY-Mode MII
P4MODE[0]	Open	PHY-Mode MII

3.3.2. Example 1 Settings (J3 Connector)

For J3 connector location and pin assignments, see Figure 1, page 1.

Table 5. Example 1 Settings (J3 Connector)

J3 Label Name	PHY-Mode MII	I/O
SCL_MDC	MDC	Input
SCL_MDIO	MDIO	I/O
MRXD[3]	PTXD[3]	Input
MRXD[2]	PTXD[2]	Input
MRXD[1]	PTXD[1]	Input
MRXD[0]	PTXD[0]	Input
MRXDV	PTXEN	Input
MRXC	PTXC	Output
MTXC	PRXC	Output
MTXEN	PRXDV	Output

J3 Label Name	PHY-Mode MII	I/O
MTXD[3]	PRXD[3]	Output
MTXD[2]	PRXD[2]	Output
MTXD[1]	PRXD[1]	Output
MTXD[0]	PRXD[0]	Output
MCOL	PCOL	Output

3.3.3. Example 1 Settings (J1 Connector)

Table 6. Example 1 Settings (J1 Connector)

J1 Label Name	PHY MII	I/O
PHY2PRXD3	PHY2PRXD3	Output
PHY2PRXD2	PHY2PRXD2	Output
PHY2PRXD1	PHY2PRXD1	Output
PHY2PRXD0	PHY2PRXD0	Output
PHY2PRXDV	PHY2PRXDV	Output
PHY2PRXC	PHY2PRXC	Output
PHY2PTXC	PHY2PTXC	Output
PHY2PTXEN	PHY2PTXEN	Input
PHY2PTXD3	PHY2PTXD3	Input
PHY2PTXD2	PHY2PTXD2	Input
PHY2PTXD1	PHY2PTXD1	Input
PHY2PTXD0	PHY2PTXD0	Input
PHY2PCOL	PHY2PCOL	Output

Note 1. To change P4 MAC SPEED, DUPLEX, FLOW_CONTROL, refer to Table 2, page 5 .

Note 2. The CPU may poll the MII registers of P4 MAC by PHY Address = 5 via SMI (MDC/MDIO). The RTL8305SB-D supports MII registers (Reg. 0,1,4 and 5.) of P4 MAC and those registers are read only.

Note 3. The RTL8305SB-D supports MII registers of P4 PHY by PHY Address = 4 via SMI (MDC/MDIO). See the RTL8305SB-D datasheet for details.

3.3.4. Example 1 Optional Settings

For R75, R76, R77, R78, R79, and R80 physical location on the board, see Figure 1, page 1.

Table 7. Example 1 Optional Settings

Location	Value	Comment
R75	10K	Assemble when Dual MII enabled
R76	10K	Assemble when MII enabled
R77	10K.	Assemble when MII enabled
R78	10K.	Assemble when MII enabled
R79	10K.	Assemble when MII enabled
R80	10K.	Assemble when MII enabled
R1	1K	
R2	1K	
R3	N.C.	Enable EEPROM
R4	N.C.	Enable Back-Pressure
R5	N.C.	Enable Group X Flow Control
R6	N.C.	Enable Group Y Flow Control
R8	N.C.	Enable Auto-Crossover
R9	N.C.	Reserved
R11	N.C.	Assembled means priority method is “Always High Priority First”
R13	N.C.	Assemble to set port 3 as high priority port. Removed to disable this feature
R14	N.C.	Disable Priority Tag-based QoS
R15	N.C.	Disable Broadcast Control
R16	N.C.	Disable VLAN
U2	N.C.	Setting by Strapping Pins only

3.4. Example 2

Enable Single MII function for P4 MAC = PHY-Mode MII, force to 100M-Full, Disable Flow control.

3.4.1. Example 2 Settings (J2 Jumper Block)

Table 8. Example 2 Settings (J2 Jumper Block)

J2 Label Name	Jumper	Function
PTT3	Open	Reserved
DISDUALMII	Open	Disable Dual MII
P4LNKSTAB	Short	Force Link On
P4SPDSTA	Open	Speed = 100M
P4DUPSTA	Open	Duplex = Full duplex
P4FCTRL	Short	Disable Flow Control
P4MODE[1]	Short	PHY-Mode MII
P4MODE[0]	Open	PHY-Mode MII

3.4.2. Example 2 Settings (J3 Connector)

For R75, R76, R77, R78, R79, and R80 physical location on the board, see Figure 1, page 1.

Table 9. Example 2 Settings (J3 Connector)

J3 Label Name	PHY-Mode MII	I/O
SCL_MDC	MDC	Input
SCL_MDIO	MDIO	I/O
MRXD[3]	PTXD[3]	Input
MRXD[2]	PTXD[2]	Input
MRXD[1]	PTXD[1]	Input
MRXD[0]	PTXD[0]	Input
MRXDV	PTXEN	Input
MRXC	PTXC	Output
MTXC	PRXC	Output
MTXEN	PRXDV	Output
MTXD[3]	PRXD[3]	Output
MTXD[2]	PRXD[2]	Output
MTXD[1]	PRXD[1]	Output
MTXD[0]	PRXD[0]	Output
MCOL	PCOL	Output

Note 1: To change P4 MAC SPEED, DUPLEX, or FLOW_CONTROL, see Table 3, page 5.

Note 2: The RTL8305SB-D supports MII Registers of P4 MAC by PHY Address = 4 via SMI (MDC/MDIO).

3.4.3. Example 2 Settings (J1 Connector)

The J1 connector should be floating.

3.4.4. Example 2 Optional Settings

For R75, R76, R77, R78, R79, and R80 physical location on the board, see Figure 1, page 1.

Table 10. Example 2 Optional Settings

Location	Value	Note
R75	N.C.	Disable Port 0 priority
R76	10K	Assemble when MII is enabled
R77	10K	Assemble when MII is enabled
R78	10K	Assemble when MII is enabled
R79	10K	Assemble when MII is enabled
R80	10K	Assemble when MII is enabled
R1	1K	RXC tuning
R2	1K	For EMI reduction
R3	N.C.	Enable EEPROM
R4	N.C.	Enable Back-Pressure
R5	N.C.	Enable Group X Flow Control
R6	N.C.	Enable Group Y Flow Control
R8	N.C.	Enable Auto-Crossover
R9	N.C.	Reserved
R11	N.C.	Assembled means priority method is “Always High Priority First”
R13	N.C.	Assembled sets port 3 as high priority port. Removed to disable this feature
R14	N.C.	Disable Priority Tag base QoS
R15	N.C.	Disable Broadcast Control
R16	N.C.	Disable VLAN
U2	N.C.	Setting by Strapping Pins only

3.5. Example 3

Enable Single SNI function for P4 MAC = PHY-Mode SNI and force to 10M-Full, Disable Flow control.

3.5.1. Example 3 Settings (J2 Jumper Block)

Table 11. Example 3 Settings (J2 Jumper Block)

J2 Label Name	Jumper	Function
PTT3	Open	Reserved
DISDUALMII	Open	Disable Dual MII
P4LNKSTAB	Short	Force Link On
P4SPDSTA	Short	Speed = 10M
P4DUPSTA	Open	Duplex = Full duplex
P4FCTRL	Short	Disable Flow Control
P4MODE[1:0]	Short	Value = 00b for PHY-Mode SNI

3.5.2. Example 3 Settings (J3 Connector)

Table 12. Example 3 Settings (J3 Connector)

J3 Label Name	PHY-Mode SNI	I/O
SCL_MDC	MDC	Input
SCL_MDIO	MDIO	I/O
MRXD[3]	N/A	Input
MRXD[2]	N/A	Input
MRXD[1]	N/A	Input
MRXD[0]	PTXD[0]	Input
MRXDV	PTXEN	Input
MRXC	PTXC	Output
MTXC	PRXC	Output
MTXEN	PRXDV	Output
MTXD[3]	N/A	Output
MTXD[2]	N/A	Output

J3 Label Name	PHY-Mode SNI	I/O
MTXD[1]	N/A	Output
MTXD[0]	PRXD[0]	Output
MCOL	PCOL	Output

Note: To change P4 MAC DUPLEX, see Table 3, page 5.

3.5.3. Example 3 Settings (J1 Connector)

The J1 connector should be floating.

3.5.4. Example 3 Optional Settings

For R75, R76, R77, R78, R79, and R80 physical location on the board, see Figure 1, page 1.

Table 13. Example 3 Optional Settings

Location	Value	Note
R75	N.C.	Disable Port 0 priority
R76	10K	
R77	10K	
R78	10K	
R79	10K	
R80	10K	
R1	1K	RXC tuning
R2	1K	
R3	N.C.	Enable EEPROM
R4	N.C.	Enable Back-Pressure
R5	N.C.	Enable Group X Flow Control
R6	N.C.	Enable Group Y Flow Control
R8	N.C.	Enable Auto-Crossover
R9	N.C.	Reserved

Location	Value	Note
R11	N.C.	R11, assembled means priority method is "Always High Priority First"
R13	N.C.	assembled to set port 3 as high priority port and removed to disable this feature
R14	N.C.	Disable Priority Tag base QoS
R15	N.C.	Disable Broadcast Control
R16	N.C.	Disable VLAN
U2	N.C.	Setting by Strapping Pins only

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