NGSPICE Simulation of CMOS Circuits

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SPICE simulation of CMOS Circuits using open-source NGSPICE.

Contents

1. Environments

2. Sources

2.1. FreePDK45

2.2. Inverter

The schematic diagram of the CMOS inverter is shown in Figure 1.

2.3. NAND2

2.4. AND2

A. Links

- GitHub: Teddy-van-Jerry/ngspice-cmos
- Website: spice.tvj.one

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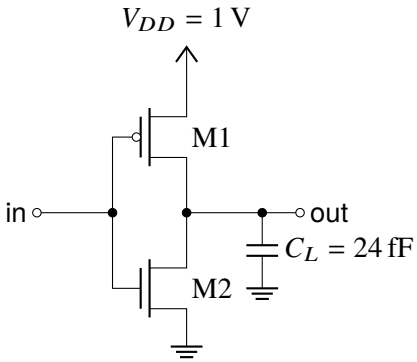

Figure 1: CMOS inverter schematic.

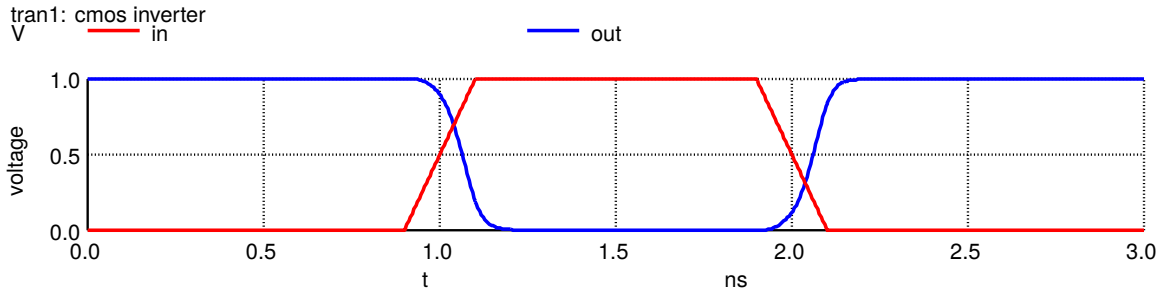

Figure 2: Response of the inverter.

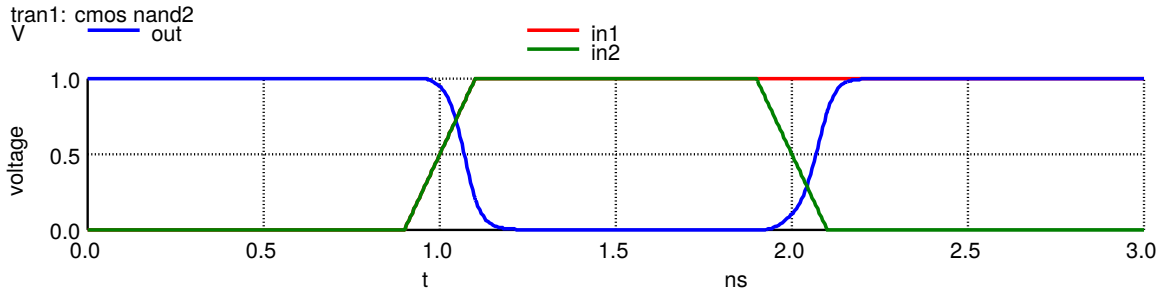

Figure 3: Response of the NAND2 gate.

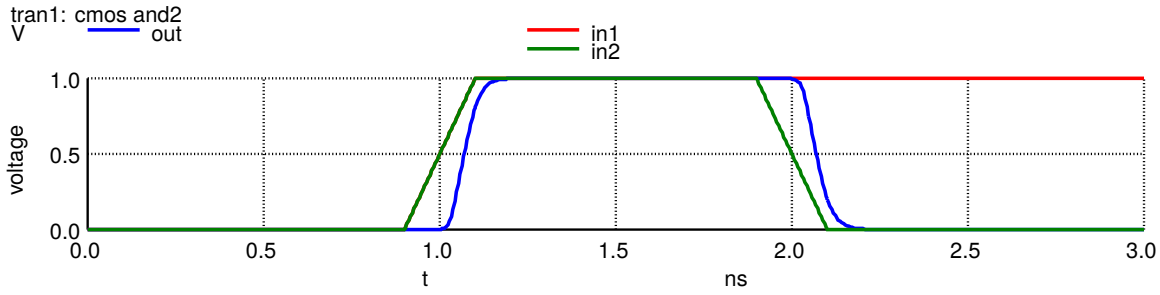

Figure 4: Response of the AND2 gate.

B. Source Code

B.1. Inverter

Listing 1: `inv.inc`

```
* ================================================================================
* Circuit     : CMOS Inverter
* Description: 1 PMOS + 1 NMOS
*
* Author      : Wuqiong Zhao (me@wqzhao.org)
* Date        : 2023-06-02
* License     : MIT
* ================================================================================

.subckt INV gnd i o vdd
  *  src  gate drain body type
  M1 vdd  i    o     vdd  PMOS_VTL W=360nm L=45nm
  M2 gnd  i    o     gnd  NMOS_VTL W=225nm L=45nm
.ends INV

.subckt NOT gnd i o vdd
  *  src  gate drain body type
  M1 vdd  i    o     vdd  PMOS_VTL W=360nm L=45nm
  M2 gnd  i    o     gnd  NMOS_VTL W=225nm L=45nm
.ends NOT
```

Listing 2: `inv.cir`

```
* ================================================================================
* Circuit     : CMOS Inverter with 1 PMOS + 1 NMOS
* Description: tr = tf when C_L = 0.024pF
*
* Author      : Wuqiong Zhao (me@wqzhao.org)
* Date        : 2023-06-01
* License     : MIT
* ================================================================================

* Reference:
* https://github.com/cornell-ece5745/ece5745-tut10-spice/blob/master/sim/inv-sim.sp

.title CMOS Inverter

* Parameters and Model
* --------------------------------------------------------------------------------
.param VDD='1.0V'
.temp  27
.inc ./FreePDK45/ff.inc

* Supply Voltage Source
* --------------------------------------------------------------------------------
Vdd vdd gnd VDD

* Inverter
* --------------------------------------------------------------------------------
.inc ./inv.inc
XInv gnd in out vdd INV

* Load Capacitor
* --------------------------------------------------------------------------------
CL out gnd 24fF

* Input Signals
* --------------------------------------------------------------------------------
Vin in gnd PWL
+ (
+   0.0ns  0V
+   0.9ns  0V
+   1.1ns VDD
+   1.9ns VDD
+   2.1ns  0V
```

```
+   3.0ns  0V
+ )

* Analysis
* --------------------------------------------------------------------------------
.ic    V(out)=VDD
.tran  0.005ns 3ns

.control
  run
  * >>>>> plot >>>>>>
  set xgridwidth  = 2
  set xbrushwidth = 3
  * "svgwidth", "svgheight",  "svgfont-size", "svgfont-width", "svguse-color",
   ↪ "svgstroke-width", "svggrid-width",
  set svg_intopts = ( 1024 256 16 0 1 2 0 )
  * "svgbackground", "svgfont-family", "svgfont"
  setcs svg_stropts = ( white Arial Arial )
  set hcopydevtype = svg
  set color1       = black
  set color2       = blue
  set color3       = red

  hardcopy fig/plot_inv_t.svg
  + out in
  + title 'CMOS Inverter'
  + xlabel 't'
  + ylabel 'Voltage'
  + ylimit 0 1

  * for MS Windows, using Edge
  if $oscompiled = 1 | $oscompiled = 8
    shell Start fig/plot_inv_t.svg
  else
    if $oscompiled = 7
      * macOS (using Safari, no need to install X11)
      shell open -a safari fig/plot_inv_t.svg &
    else
      * for CYGWIN, Linux, using feh and X11
      shell feh --magick-timeout 1 fig/plot_inv_t.svg &
    end
  end
  * <<<<< plot <<<<<
.endc

* Measurement
* --------------------------------------------------------------------------------
.measure tran tr   trig V(out) val='VDD*0.1' rise=1 targ V(out) val='VDD*0.9' rise=1
.measure tran tf   trig V(out) val='VDD*0.9' fall=1 targ V(out) val='VDD*0.1' fall=1
.measure tran tpdr trig V(in)  val='VDD/2'   fall=1 targ V(out) val='VDD/2'   rise=1
.measure tran tpdf trig V(in)  val='VDD/2'   rise=1 targ V(out) val='VDD/2'   fall=1
.measure tran tpd  param='(tpdr+tpdf)/2'

.end
```

B.2. NAND2

Listing 3: nand2.inc

```
* ================================================================================
* Circuit     : CMOS NAND2 Gate
* Description: 2 PMOS + 2 NMOS
*
* Author      : Wuqiong Zhao (me@wqzhao.org)
* Date        : 2023-06-01
* License     : MIT
* ================================================================================

.subckt NAND2 gnd i1 i2 o vdd
  *    src  gate drain body type
```

```
  Mp1 vdd  i1   o     vdd  PMOS_VTL W=360nm L=45nm
  Mp2 vdd  i2   o     vdd  PMOS_VTL W=360nm L=45nm
  Mn1 t1   i1   o     gnd  NMOS_VTL W=450nm L=45nm
  Mn2 gnd  i2   t1    gnd  NMOS_VTL W=450nm L=45nm
.ends NAND2

.subckt NAND gnd i1 i2 o vdd
  *   src  gate drain body type
  Mp1 vdd  i1   o     vdd  PMOS_VTL W=360nm L=45nm
  Mp2 vdd  i2   o     vdd  PMOS_VTL W=360nm L=45nm
  Mn1 t1   i1   o     gnd  NMOS_VTL W=450nm L=45nm
  Mn2 gnd  i2   t1    gnd  NMOS_VTL W=450nm L=45nm
.ends NAND
```

Listing 4: nand2.cir

```
* ================================================================================
* Circuit     : CMOS NAND2 Gate
* Description: 2 PMOS + 2 NMOS
*
* Author      : Wuqiong Zhao (me@wqzhao.org)
* Date        : 2023-06-01
* License     : MIT
* ================================================================================

.title CMOS NAND2

* Parameters and Model
* --------------------------------------------------------------------------------
.param VDD='1.0V'
.temp  27
.inc ./FreePDK45/ff.inc

* Supply Voltage Source
* --------------------------------------------------------------------------------
Vdd vdd gnd VDD

* NAND2
* --------------------------------------------------------------------------------
XNAND2 gnd in1 in2 out vdd NAND2
.inc ./nand2.inc

* Load Capacitor
* --------------------------------------------------------------------------------
CL out gnd 24fF

* Input Signals
* --------------------------------------------------------------------------------
Vin1 in1 gnd PWL
+ (
+   0.0ns  0V
+   0.9ns  0V
+   1.1ns VDD
+   3.0ns VDD
+ )

Vin2 in2 gnd PWL
+ (
+   0.0ns  0V
+   0.9ns  0V
+   1.1ns VDD
+   1.9ns VDD
+   2.1ns  0V
+   3.0ns  0V
+ )

* Analysis
* --------------------------------------------------------------------------------
.ic    V(out)=VDD
.tran  0.005ns 3ns

.control
```

```
  run
  * >>>>> plot >>>>>>
  set xgridwidth  = 2
  set xbrushwidth = 3
  * "svgwidth", "svgheight",  "svgfont-size", "svgfont-width", "svguse-color",
   ↪ "svgstroke-width", "svggrid-width",
  set svg_intopts = ( 1024 256 16 0 1 2 0 )
  * "svgbackground", "svgfont-family", "svgfont"
  setcs svg_stropts = ( white Arial Arial )
  set hcopydevtype = svg
  set color1       = black
  set color2       = red
  set color3       = blue
  set color4       = green

  hardcopy fig/plot_nand2_t.svg
  + in1 out in2
  + title 'CMOS NAND2'
  + xlabel 't'
  + ylabel 'Voltage'
  + ylimit 0 1

  * for MS Windows, using Edge
  if $oscompiled = 1 | $oscompiled = 8
    shell Start fig/plot_nand2_t.svg
  else
    if $oscompiled = 7
      * macOS (using Safari, no need to install X11)
      shell open -a safari fig/plot_nand2_t.svg &
    else
      * for CYGWIN, Linux, using feh and X11
      shell feh --magick-timeout 1 fig/plot_nand2_t.svg &
    end
  end
  * <<<<< plot <<<<<
.endc

* Measurement
* --------------------------------------------------------------------------
.measure tran tr   trig V(out) val='VDD*0.1' rise=1 targ V(out) val='VDD*0.9' rise=1
.measure tran tf   trig V(out) val='VDD*0.9' fall=1 targ V(out) val='VDD*0.1' fall=1
.measure tran tpdr trig V(in2) val='VDD/2'   fall=1 targ V(out) val='VDD/2'   rise=1
.measure tran tpdf trig V(in1) val='VDD/2'   rise=1 targ V(out) val='VDD/2'   fall=1
.measure tran tpd  param='(tpdr+tpdf)/2'

.end
```

B.3. AND2

Listing 5: and2.inc

```
* ============================================================================
* Circuit     : CMOS AND2 Gate
* Description: NMOS2 + Inverter (3 PMOS + 3 NMOS)
*
* Author      : Wuqiong Zhao (me@wqzhao.org)
* Date        : 2023-06-02
* License     : MIT
* ============================================================================

.subckt AND2 gnd i1 i2 o vdd
  XNAND gnd i1 i2 o1 vdd NAND2
  XInv  gnd o1     o vdd INV
.ends AND2

.subckt AND gnd i1 i2 o vdd
  XNAND gnd i1 i2 o1 vdd NAND2
  XInv  gnd o1     o vdd INV
.ends AND

```

```
.inc ./nand2.inc
.inc ./inv.inc
```

Listing 6: and2.cir

```
* ================================================================================
* Circuit     : CMOS AND2 Gate
* Description: NMOS2 + Inverter (3 PMOS + 3 NMOS)
*
* Author      : Wuqiong Zhao (me@wqzhao.org)
* Date        : 2023-06-02
* License     : MIT
* ================================================================================

.title CMOS AND2

* Parameters and Model
* --------------------------------------------------------------------------------
.param VDD='1.0V'
.temp  27
.inc ./FreePDK45/ff.inc

* Supply Voltage Source
* --------------------------------------------------------------------------------
Vdd vdd gnd VDD

* AND2
* --------------------------------------------------------------------------------
XAND2 gnd in1 in2 out vdd AND2
.inc ./and2.inc

* Load Capacitor
* --------------------------------------------------------------------------------
CL out gnd 24fF

* Input Signals
* --------------------------------------------------------------------------------
Vin1 in1 gnd PWL
+ (
+   0.0ns  0V
+   0.9ns  0V
+   1.1ns VDD
+   3.0ns VDD
+ )

Vin2 in2 gnd PWL
+ (
+   0.0ns  0V
+   0.9ns  0V
+   1.1ns VDD
+   1.9ns VDD
+   2.1ns  0V
+   3.0ns  0V
+ )

* Analysis
* --------------------------------------------------------------------------------
.ic    V(out)=0
.tran  0.005ns 3ns

.control
  run
  * >>>>> plot >>>>>>
  set xgridwidth  = 2
  set xbrushwidth = 3
  * "svgwidth", "svgheight",  "svgfont-size", "svgfont-width", "svguse-color",
   ↪ "svgstroke-width", "svggrid-width",
  set svg_intopts = ( 1024 256 16 0 1 2 0 )
  * "svgbackground", "svgfont-family", "svgfont"
  setcs svg_stropts = ( white Arial Arial )
  set hcopydevtype = svg
  set color1       = black
```

```
  set color2       = red
  set color3       = blue
  set color4       = green

  hardcopy fig/plot_and2_t.svg
  + in1 out in2
  + title 'CMOS AND2'
  + xlabel 't'
  + ylabel 'Voltage'
  + ylimit 0 1

  * for MS Windows, using Edge
  if $oscompiled = 1 | $oscompiled = 8
    shell Start fig/plot_and2_t.svg
  else
    if $oscompiled = 7
      * macOS (using Safari, no need to install X11)
      shell open -a safari fig/plot_and2_t.svg &
    else
      * for CYGWIN, Linux, using feh and X11
      shell feh --magick-timeout 1 fig/plot_and2_t.svg &
    end
  end
  * <<<<< plot <<<<<
.endc

* Measurement
* --------------------------------------------------------------------------
.measure tran tr   trig V(out) val='VDD*0.1' rise=1 targ V(out) val='VDD*0.9' rise=1
.measure tran tf   trig V(out) val='VDD*0.9' fall=1 targ V(out) val='VDD*0.1' fall=1
.measure tran tpdr trig V(in1) val='VDD/2'   rise=1 targ V(out) val='VDD/2'   rise=1
.measure tran tpdf trig V(in2) val='VDD/2'   fall=1 targ V(out) val='VDD/2'   fall=1
.measure tran tpd  param='(tpdr+tpdf)/2'

.end
```