

NGSPICE Simulation of CMOS Circuits

Wuqiong Zhao*

June 2, 2023

SPICE simulation of CMOS Circuits using open-source NGSPICE.

Contents

1. Environments	1
2. Sources	1
2.1. FreePDK45	1
2.2. Inverter	1
2.3. NAND2	3
2.4. AND2	3
2.5. AND8	3
2.5.1. Symmetrical Design	3
A. Links	3
B. Source Code	3
B.1. Inverter	3
B.2. NAND2	5
B.3. AND2	7

1. Environments

2. Sources

2.1. FreePDK45

2.2. Inverter

The schematic diagram of the CMOS inverter is shown in [Figure 1](#).

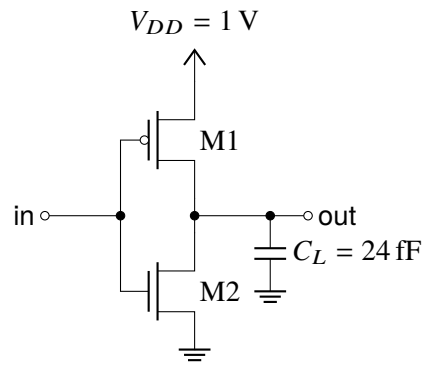


Figure 1: CMOS inverter schematic.

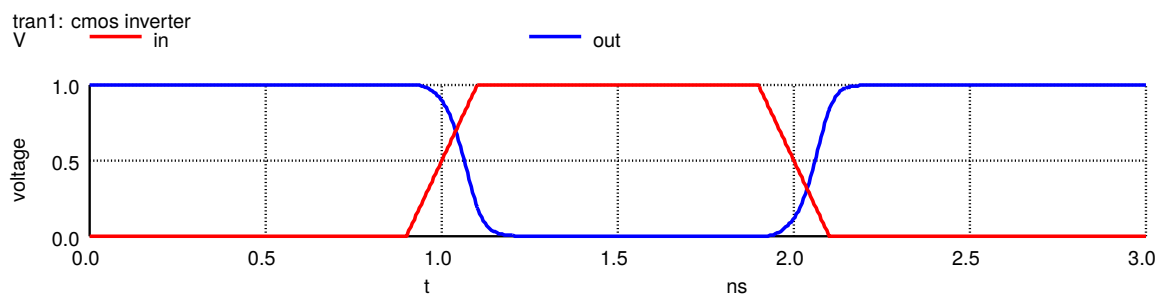


Figure 2: Response of the inverter.

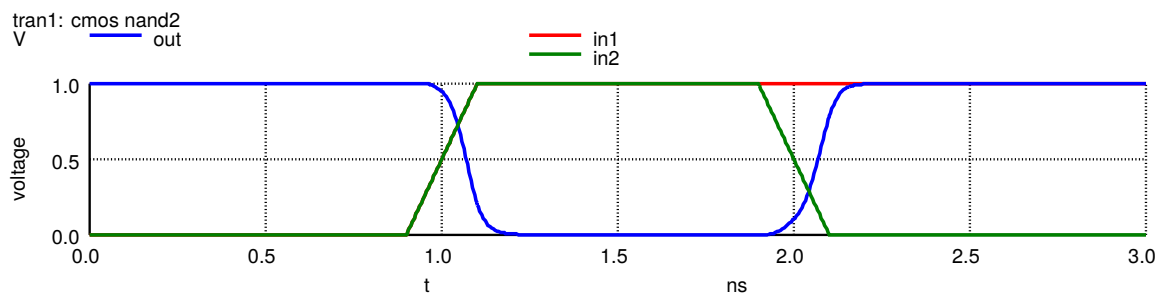


Figure 3: Response of the NAND2 gate.

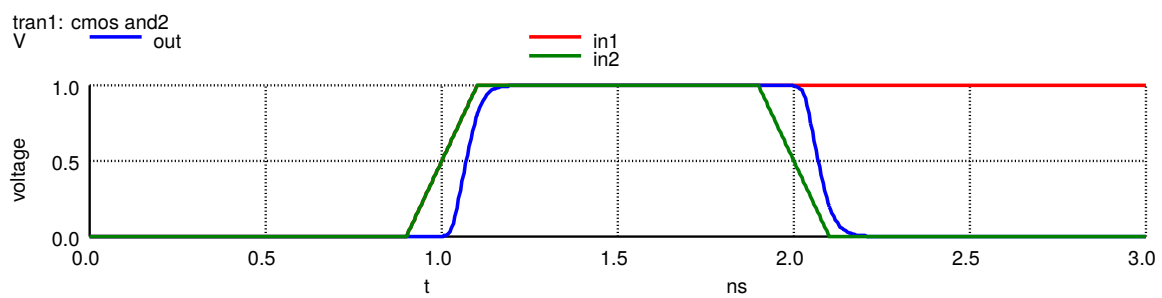


Figure 4: Response of the AND2 gate.

2.3. NAND2

2.4. AND2

2.5. AND8

2.5.1. Symmetrical Design

A. Links

- GitHub: [Teddy-van-Jerry/ngspice-cmos](https://github.com/Teddy-van-Jerry/ngspice-cmos)
- Website: spice.tvj.one

B. Source Code

B.1. Inverter

Listing 1: inv.inc

```

1  * =====
2  * Circuit      : CMOS Inverter
3  * Description: 1 PMOS + 1 NMOS
4  *
5  * Author       : Wuqiong Zhao (me@wqzhao.org)
6  * Date        : 2023-06-02
7  * License      : MIT
8  * =====
9
10 .subckt INV gnd i o vdd
11   * src gate drain body type
12   M1 vdd i o vdd PMOS_VTL W=360nm L=45nm
13   M2 gnd i o gnd NMOS_VTL W=225nm L=45nm
14 .ends INV
15
16 .subckt NOT gnd i o vdd
17   * src gate drain body type
18   M1 vdd i o vdd PMOS_VTL W=360nm L=45nm
19   M2 gnd i o gnd NMOS_VTL W=225nm L=45nm
20 .ends NOT

```

Listing 2: inv.cir

```

1  * =====
2  * Circuit      : CMOS Inverter with 1 PMOS + 1 NMOS
3  * Description: tr = tf when C_L = 0.024pF
4  *
5  * Author       : Wuqiong Zhao (me@wqzhao.org)
6  * Date        : 2023-06-01
7  * License      : MIT
8  * =====
9
10 * Reference:
11 * https://github.com/cornell-ece5745/ece5745-tut10-spice/blob/master/sim/inv-sim.sp
12
13 .title CMOS Inverter
14
15 * Parameters and Model
16 * -----
17 .param VDD='1.0V'
18 .temp 27

```

* This is the course project of FUNDAMENTALS OF VLSI DESIGN, Southeast University, 2023 Spring.
 The author is with the National Mobile Communications Research Laboratory, Southeast University, Nanjing 211189, China.
 (E-Mail: me@wqzhao.org)

```

19 .inc ./FreePDK45/ff.inc
20
21 * Supply Voltage Source
22 * -----
23 Vdd vdd gnd VDD
24
25 * Inverter
26 * -----
27 .inc ./inv.inc
28 XInv gnd in out vdd INV
29
30 * Load Capacitor
31 * -----
32 CL out gnd 24fF
33
34 * Input Signals
35 * -----
36 Vin in gnd PWL
37 + (
38 +   0.0ns 0V
39 +   0.9ns 0V
40 +   1.1ns VDD
41 +   1.9ns VDD
42 +   2.1ns 0V
43 +   3.0ns 0V
44 + )
45
46 * Analysis
47 * -----
48 .ic      V(out)=VDD
49 .tran    0.005ns 3ns
50
51 .control
52   run
53   * >>>> plot >>>>>
54   set xgridwidth = 2
55   set xbrushwidth = 3
56   * "svgwidth", "svgheight", "svgfont-size", "svgfont-width", "svguse-color",
57   ↩ "svgstroke-width", "svggrid-width",
58   set svg_intopts = ( 1024 256 16 0 1 2 0 )
59   * "svgbackground", "svgfont-family", "svgfont"
60   setscs svg_stropts = ( white Arial Arial )
61   set hcopydevtype = svg
62   set color1      = black
63   set color2      = blue
64   set color3      = red
65
66   hardcopy fig/plot_inv_t.svg
67   + out in
68   + title 'CMOS Inverter'
69   + xlabel 't'
70   + ylabel 'Voltage'
71   + ylimit 0 1
72
73   * for MS Windows, using Edge
74   if $oscompiled = 1 | $oscompiled = 8
75     shell Start fig/plot_inv_t.svg
76   else
77     if $oscompiled = 7
78       * macOS (using Safari, no need to install X11)
79       shell open -a safari fig/plot_inv_t.svg &
80     else
81       * for CYGWIN, Linux, using feh and X11
82       shell feh --magick-timeout 1 fig/plot_inv_t.svg &
83     end
84   end
85   * <<<<< plot <<<<<
86 .endc
87
88 * Measurement
89 * -----
90 .measure tran tr   trig V(out) val='VDD*0.1' rise=1 targ V(out) val='VDD*0.9' rise=1
91 .measure tran tf   trig V(out) val='VDD*0.9' fall=1 targ V(out) val='VDD*0.1' fall=1

```

```

91 .measure tran tpdr trig V(in) val='VDD/2' fall=1 targ V(out) val='VDD/2' rise=1
92 .measure tran tpdf trig V(in) val='VDD/2' rise=1 targ V(out) val='VDD/2' fall=1
93 .measure tran tpd param='(tpdr+tpdf)/2'
94
95 .end

```

B.2. NAND2

Listing 3: nand2.inc

```

1  * =====
2  * Circuit      : CMOS NAND2 Gate
3  * Description: 2 PMOS + 2 NMOS
4  *
5  * Author       : Wuqiong Zhao (me@wqzhao.org)
6  * Date        : 2023-06-01
7  * License     : MIT
8  * =====
9
10 .subckt NAND2 gnd i1 i2 o vdd
11   * src gate drain body type
12   Mp1 vdd i1 o vdd PMOS_VTL W=360nm L=45nm
13   Mp2 vdd i2 o vdd PMOS_VTL W=360nm L=45nm
14   Mn1 t1 i1 o gnd NMOS_VTL W=450nm L=45nm
15   Mn2 gnd i2 t1 gnd NMOS_VTL W=450nm L=45nm
16 .ends NAND2
17
18 .subckt NAND gnd i1 i2 o vdd
19   * src gate drain body type
20   Mp1 vdd i1 o vdd PMOS_VTL W=360nm L=45nm
21   Mp2 vdd i2 o vdd PMOS_VTL W=360nm L=45nm
22   Mn1 t1 i1 o gnd NMOS_VTL W=450nm L=45nm
23   Mn2 gnd i2 t1 gnd NMOS_VTL W=450nm L=45nm
24 .ends NAND

```

Listing 4: nand2.cir

```

1  * =====
2  * Circuit      : CMOS NAND2 Gate
3  * Description: 2 PMOS + 2 NMOS
4  *
5  * Author       : Wuqiong Zhao (me@wqzhao.org)
6  * Date        : 2023-06-01
7  * License     : MIT
8  * =====
9
10 .title CMOS NAND2
11
12 * Parameters and Model
13 * -----
14 .param VDD='1.0V'
15 .temp 27
16 .inc ./FreePDK45/ff.inc
17
18 * Supply Voltage Source
19 * -----
20 Vdd vdd gnd VDD
21
22 * NAND2
23 * -----
24 XNAND2 gnd in1 in2 out vdd NAND2
25 .inc ./nand2.inc
26
27 * Load Capacitor
28 * -----
29 CL out gnd 24fF
30
31 * Input Signals
32 * -----

```

```

33 Vin1 in1 gnd PWL
34 + (
35 + 0.0ns 0V
36 + 0.9ns 0V
37 + 1.1ns VDD
38 + 3.0ns VDD
39 + )
40
41 Vin2 in2 gnd PWL
42 + (
43 + 0.0ns 0V
44 + 0.9ns 0V
45 + 1.1ns VDD
46 + 1.9ns VDD
47 + 2.1ns 0V
48 + 3.0ns 0V
49 + )
50
51 * Analysis
52 * -----
53 .ic V(out)=VDD
54 .tran 0.005ns 3ns
55
56 .control
57 run
58 * >>>> plot >>>>>
59 set xgridwidth = 2
60 set xbrushwidth = 3
61 * "svgwidth", "svgheight", "svgfont-size", "svgfont-width", "svguse-color",
62   ↪ "svgstroke-width", "svggrid-width",
63 set svg_intopts = ( 1024 256 16 0 1 2 0 )
64 * "svgbackground", "svgfont-family", "svgfont"
65 setcs svg_stropts = ( white Arial Arial )
66 set hcopydevtype = svg
67 set color1 = black
68 set color2 = red
69 set color3 = blue
70 set color4 = green
71
72 hardcopy fig/plot_nand2_t.svg
73 + in1 out in2
74 + title 'CMOS NAND2'
75 + xlabel 't'
76 + ylabel 'Voltage'
77 + ylimit 0 1
78
79 * for MS Windows, using Edge
80 if $oscompiled = 1 | $oscompiled = 8
81     shell Start fig/plot_nand2_t.svg
82 else
83     if $oscompiled = 7
84         * macOS (using Safari, no need to install X11)
85         shell open -a safari fig/plot_nand2_t.svg &
86     else
87         * for CYGWIN, Linux, using feh and X11
88         shell feh --magick-timeout 1 fig/plot_nand2_t.svg &
89     end
90 end
91 * <<<<< plot <<<<<
92 .endc
93
94 * Measurement
95 * -----
96 .measure tran tr trig V(out) val='VDD*0.1' rise=1 targ V(out) val='VDD*0.9' rise=1
97 .measure tran tf trig V(out) val='VDD*0.9' fall=1 targ V(out) val='VDD*0.1' fall=1
98 .measure tran tpdr trig V(in2) val='VDD/2' fall=1 targ V(out) val='VDD/2' rise=1
99 .measure tran tpdf trig V(in1) val='VDD/2' rise=1 targ V(out) val='VDD/2' fall=1
100 .measure tran tpd param='(tpdr+tpdf)/2'
101
102 .end

```

B.3. AND2

Listing 5: and2.inc

```

1  * =====
2  * Circuit      : CMOS AND2 Gate
3  * Description: NMOS2 + Inverter (3 PMOS + 3 NMOS)
4  *
5  * Author       : Wuqiong Zhao (me@wqzhao.org)
6  * Date        : 2023-06-02
7  * License     : MIT
8  * =====
9
10 .subckt AND2 gnd i1 i2 o vdd
11     XNAND gnd i1 i2 o1 vdd NAND2
12     XInv  gnd o1      o vdd INV
13 .ends AND2
14
15 .subckt AND gnd i1 i2 o vdd
16     XNAND gnd i1 i2 o1 vdd NAND2
17     XInv  gnd o1      o vdd INV
18 .ends AND
19
20 .inc ./nand2.inc
21 .inc ./inv.inc

```

Listing 6: and2.cir

```

1  * =====
2  * Circuit      : CMOS AND2 Gate
3  * Description: NMOS2 + Inverter (3 PMOS + 3 NMOS)
4  *
5  * Author       : Wuqiong Zhao (me@wqzhao.org)
6  * Date        : 2023-06-02
7  * License     : MIT
8  * =====
9
10 .title CMOS AND2
11
12 * Parameters and Model
13 * -----
14 .param VDD='1.0V'
15 .temp 27
16 .inc ./FreePDK45/ff.inc
17
18 * Supply Voltage Source
19 * -----
20 Vdd vdd gnd VDD
21
22 * AND2
23 * -----
24 XAND2 gnd in1 in2 out vdd AND2
25 .inc ./and2.inc
26
27 * Load Capacitor
28 * -----
29 CL out gnd 24fF
30
31 * Input Signals
32 * -----
33 Vin1 in1 gnd PWL
34 + (
35 +   0.0ns 0V
36 +   0.9ns 0V
37 +   1.1ns VDD
38 +   3.0ns VDD
39 + )
40
41 Vin2 in2 gnd PWL
42 + (
43 +   0.0ns 0V

```

```

44 + 0.9ns 0V
45 + 1.1ns VDD
46 + 1.9ns VDD
47 + 2.1ns 0V
48 + 3.0ns 0V
49 + )
50
51 * Analysis
52 * -----
53 .ic V(out)=0
54 .tran 0.005ns 3ns
55
56 .control
57 run
58 * >>>> plot >>>>
59 set xgridwidth = 2
60 set xbrushwidth = 3
61 * "svgwidth", "svgheight", "svgfont-size", "svgfont-width", "svguse-color",
62   ↪ "svgstroke-width", "svggrid-width",
63 set svg_intopts = ( 1024 256 16 0 1 2 0 )
64 * "svgbackground", "svgfont-family", "svgfont"
65 setcs svg_stropts = ( white Arial Arial )
66 set hcopydevtype = svg
67 set color1 = black
68 set color2 = red
69 set color3 = blue
70 set color4 = green
71
72 hardcopy fig/plot_and2_t.svg
73 + in1 out in2
74 + title 'CMOS AND2'
75 + xlabel 't'
76 + ylabel 'Voltage'
77 + ylimit 0 1
78
79 * for MS Windows, using Edge
80 if $oscompiled = 1 | $oscompiled = 8
81     shell Start fig/plot_and2_t.svg
82 else
83     if $oscompiled = 7
84         * macOS (using Safari, no need to install X11)
85         shell open -a safari fig/plot_and2_t.svg &
86     else
87         * for CYGWIN, Linux, using feh and X11
88         shell feh --magick-timeout 1 fig/plot_and2_t.svg &
89     end
90 end
91 * <<<< plot <<<<
92 .endc
93
94 * Measurement
95 * -----
96 .measure tran tr trig V(out) val='VDD*0.1' rise=1 targ V(out) val='VDD*0.9' rise=1
97 .measure tran tf trig V(out) val='VDD*0.9' fall=1 targ V(out) val='VDD*0.1' fall=1
98 .measure tran tpdr trig V(in1) val='VDD/2' rise=1 targ V(out) val='VDD/2' rise=1
99 .measure tran tpdf trig V(in2) val='VDD/2' fall=1 targ V(out) val='VDD/2' fall=1
100 .measure tran tpd param='(tpdr+tpdf)/2'
101 .end

```