POSSESION OF MOBILES IN EXAM IS UFM PRACTICE.

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Jaypee Institute of Information Technology, Noida
T1 Examination, 2022, V Semester

Course Title: Computer Organization Architecture **Maximum Time: 1hr**
Course Code: 15B11CI313 **Maximum Marks: 20**

CO1: Summarize and compare the different computer systems based on RISC and CISC architecture.
CO2: Categorize different types of computers based on instruction set architecture.
CO3: Apply the knowledge of performance metrics to find the performance of systems.
CO4: Design RISC and CISC based computer using hardwired/microprogrammed controllers
CO5: Create and analyse an assembly language program of RISC and CISC based systems.
CO6: Apply the knowledge of pipeline, IO and cache to understand these systems. Further analyse the performance of such systems.

Note: Attempt all the questions

Q1. [CO-1, 2 M] Match the following entries on the left side to correct entry on the right side for the table given below.

1. A sequence of instructions	a. Data path
2. Computer's primitive instructions	b. Micro-program
3. Systematic and organized design of computer systems	c. Gates
4. Micro-architecture level	d. Structured computer organization
5. Problem-oriented language level	e. Program
6. Digital logic level	f. Machine Language
7. Registers are connected to the ALU	g. Compiler
8. Control operation of data path	h. Hardware level

Q2. [CO-3, 3 M] A table is given below showing type of instructions, number of instructions, and CPI for a program having 50 instructions. The average CPI for the program is 2.4. Find the value of X and Y and the percentage of CPU time taken by the instruction C.

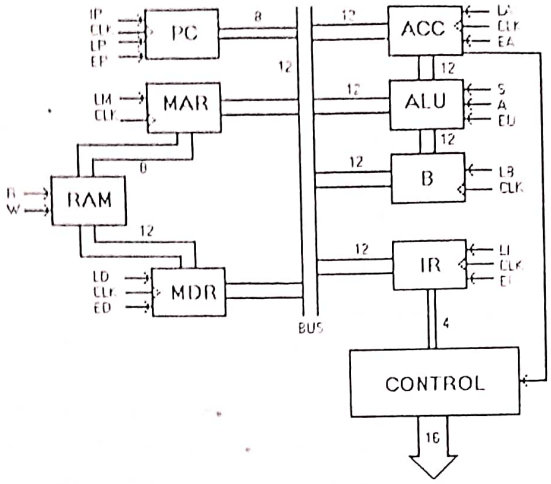
Operation	No. of Instructions	CPI
A	20	1
B	15	4
C	X	Y
D	5	2

Q3. [CO-3, 3 M] Suppose a program contains S portion of code which requires sequential execution and F portion of the code can run in parallel fashion. With a new hardware design, the S portion is speedup by factor N1 and F portion is slow down by N2 factor. Find the overall speedup.

Q4. [CO-2, 3 M] Third generation computers with Byte addressable memory has 32-bit address bus.
a) What is the address space and range of memory address of these computers?
b) What would be the size of program counter (PC) of these computers?
c) If we would like to decrease the address space 4 times, what will be the new address space and size of address bus?
d) What will be the modified PC size?

Q5. [CO-2, 3 M] Consider word addressable processor (word size is 2 byte) with 16 registers and number of instructions are 16 in number. Each instruction has three distinct fields, namely, opcode, one register acting as both source and destination, and 8 bit direct address. The definition of any instruction **ADD R1, [F0]** is **R1 = R1 + Memory [F0]**. Suppose there are 128 such instructions in the program. Calculate how much address space in bytes the program requires. Suppose the program is stored from location 00H. What is the address of last instruction?

Q6. [CO-4, 6 M] For the basic computer shown in figure given below, suppose we add two additional instructions INC and DEC with control signals 'I' and 'D' to ALU with opcode 8 and 9 respectively. Definition of INC is ACC←ACC+1 and for DEC is ACC←ACC-1. Answer the following questions:



a) [1M] Draw the hardwired instruction decoder for INC and DEC instructions.
b) [1M] Write the register transfer/microinstruction and active control signal for INC and DEC instructions.
c) [1M] Draw the hardwired control matrix using Boolean expression for INC and DEC instructions to generate 'I' and 'D' control signal.
d) [3M] Write sequence of micro-instructions stored in micro-routines for Fetch, INC, and DEC instructions (in Hex). INC and DEC are saved in control ROM at location 12H and 14H. The order of control signals in a control word is as follows:

IP, LP, EP, LM, R, W, LD, ED, LI, EI, LA, EA, A, S, EU, LB, I, D

The micro instruction format is as follows:

Control Word (18-bit)	CD (1-bit)	MAP (1-bit)	HLT (1-bit)	CRJA (5-bit)

<-----26 bit----->

1-Bit	1-Bit	1-Bit	5-Bit
CD	MAP	HLT	CRJA