T-1 Examination 2022
COA Solution

Q1. [CO-1, 2 Marks] Match the following table with their correct options.
Answer:0.25 Marks for each correct answer

A sequence of instructions	Program
Computer's primitive instructions	Machine language
Systematic and organized design of computer systems	Structured computer organization
Microarchitecture level	Hardware
Problem-oriented language level	Compiler
Digital logic level	Gates
Registers are connected to the ALU	Data path
Control operation of the data path	Microprogram

Q2.[CO-3, 3M] A table is given below showing, type of instructions, number of instructions, and CPI for a program having 50 instructions. The average CPI for the program is 2.4. Find the value of X and Y and the percentage of CPU time taken by instruction C.

Operation	No. of Instruction	CPI
A	20	1
B	15	4
C	X	Y
D	5	2

Ans 2)
N=50 (total number of Instructions)
CPI=2.4
X=50-20-15-5=10

Operation	NumInst	f=NumInst/N	CPI	f*CPI	f*CPI
A	20	0.4	1	0.4	0.4
B	15	0.3	4	1.2	1.2
C	10	0.2	Y	0.2*Y	0.6
D	5	0.1	2	0.2	0.2

CPI=$\sum$f*CPI = 0.4+1.2+0.2Y+0.2=2.4
Y=3 **[2 Marks]**
% of CPU Time for C instruction = 0.6/2.4*100=25%**[1 Marks]**

Q3. [CO-3, 3M] Suppose a program contains S portion of code which requires sequential execution and F portion of code can run in parallel fashion. With a new hardware design, the S portion is speedup by factor N1 and F portion is slow down by N2 factor. Find overall Speedup?

Ans 3)

Suppose T be the execution time of program without enhancement
So, T1= T(1-F)+ TF **[1 Marks]**
After enhancement,
So, T2= T(1-F)/N1+ TF N2 **[1 Marks]**
Overall Speedup= T1/T2= $1/((1-F)/N1+FN2)$ **[1 Marks]**

Q4 [CO-2,3M] Third generation computers with Byte addressable memory has 32-bit address bus.

a) What is the address space and range of memory address of these computers?
b) What would be the size of program counter (PC) of these computers?
c) If we would like to decrease the address space 4-times, what will be the new address space and size of address bus
d) What will be modified PC size ?

Solution Q4

a) 4GB and address Range [2^{32}-1] **[1 Marks]**
b) PC= 32 bit **[0.5 Marks]**
c) 1GB address space and 30 bits in address bus**[1 Marks]**
d) PC=30 Bits **[0.5 Marks]**

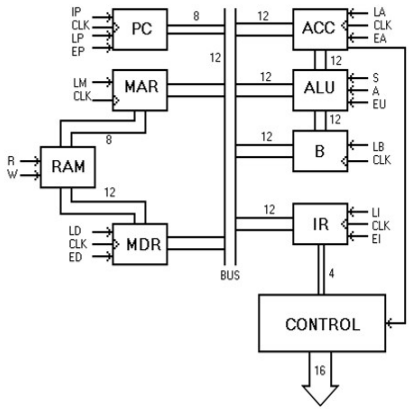
Q5 [CO-2,3M] Consider word addressable processor (Word size is two byte) with 16 registers and number of instructions are 16 in number. Each instruction has three distinct fields, namely, opcode, one register acting as both source and destination and 8 bit direct address. The definition of any instruction ADD R1, [F0] is R1 = R1 + Memory [F0]. Suppose there are 128 such instruction in program. Calculate how much address space in bytes the program requires. Suppose the program is stored from location 00H. What is the address of last instruction?

Solution Q5

Each instruction will require 4 bits for opcode, 4 bits for register and 8 bit for direct address. That means size of each instruction is 16 bit. **[1 Marks]**
Memory require by program is 128 * 2Bytes= 256 Bytes. **[1 Marks]**
Adresss of last instruction is FEH. **[1 Marks]**

Q6[CO-4,6M]

For the given basic computer suppose we add two additional instructions INC and DEC with control signal 'I' and 'D' to ALU with opcode 8 and 9. Definition of INC is ACC←ACC+1 and for DEC is ACC←ACC-1.

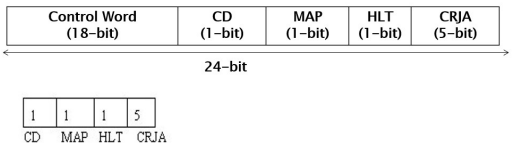


Answer the following questions:

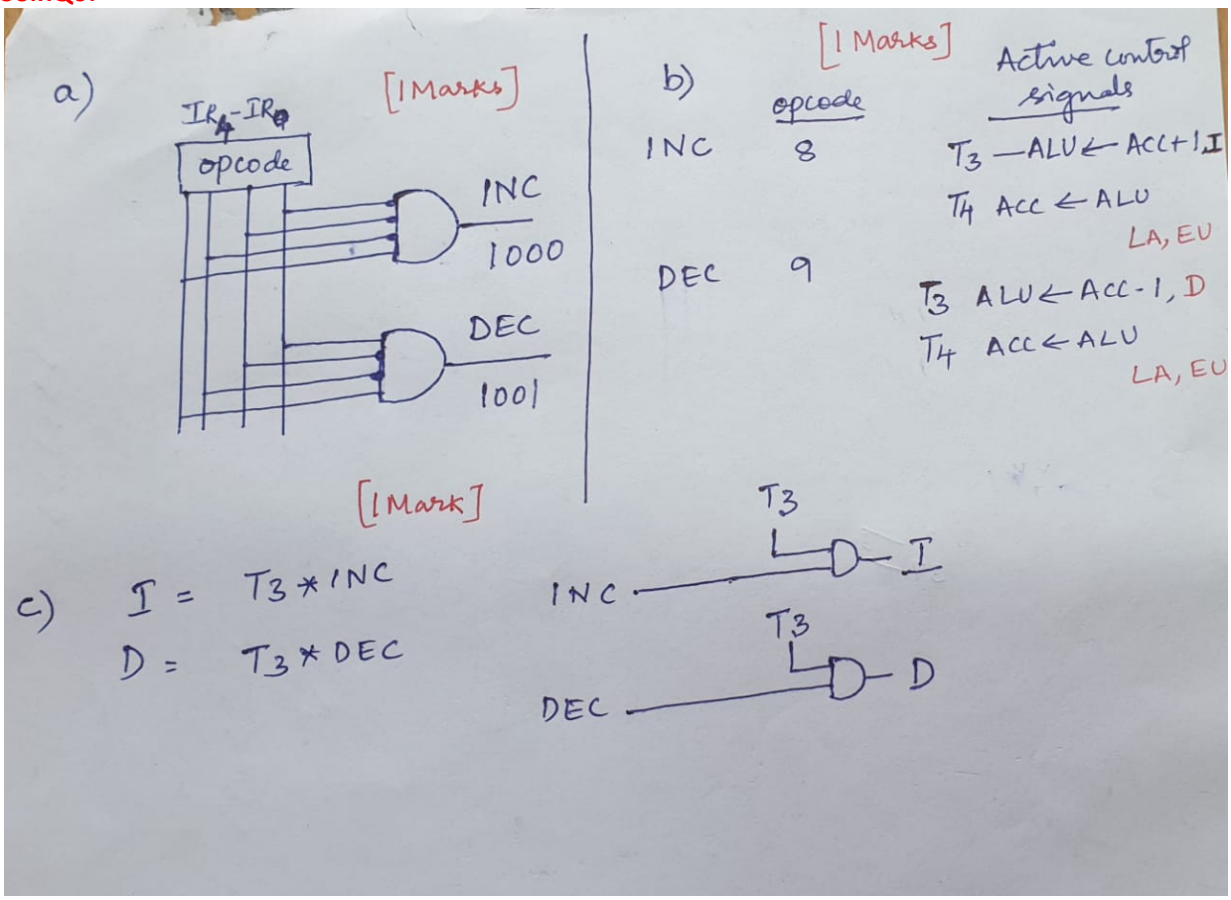
a) Draw the hardwired instruction decoder for these instructions only.
b) Write the register transfer/Microinstruction and active control signal for these instructions only.
c) Draw the hardwired control matrix using Boolean expression of these instructions to generate 'I' and 'D' control signal.
d) Write sequence of micro-instructions stored in micro-routines for fetch, INC and DEC instructions (in Hex). INC and DEC are saved in Control ROM at location 12H and 14H. If order of control signals is as follow in control word.

IP, LP, EP, LM, R, W, LD, ED, LI, EI, LA, EA, A, S, EU, LB, I, D

and the micro instruction format as follows:



SolnQ6:



[3 Marks] one marks each for fetch, INC and DEC

Micro-routine Name	Address-ROM Address (Opcode)	Micro-Instruction Address (5-bits)	Control Signals: IP, LP, EP, LM, R, W, LD, ED, LI, EI, LA, EA, A, S, EU, LB ,I,D	Control Signal In HEX	CD (1-bit)	MAP (1-bit)	HLT (1-bit)	CRJA (5-bit)
"Fetch"	0	00 01 02	00 1100 0000 0000 0000 00 0010 0000 0000 0000 10 0000 0110 0000 0000	0C000 02000 20600	0 0 0	0 0 1	0 0 0	01 02 xx
INC	8	12 13	00 0000 0000 0000 0010 00 0000 0000 1000 1000	00002 00088	0 0	0 0	0 0	13 00
DEC	9	14 15	00 0000 0000 0000 0001 00 0000 0000 1000 1000	00001 00088	0 0	0 0	0 0	15 00
HLT	F	1F		0000	0	0	1	XX