POSSESION OF MOBILES IN EXAM IS UFM PRACTICE.

Name _____ **Enrollment No.**_____

Jaypee Institute of Information Technology, Noida

T-2 Examination, EVEN 2023
B. Tech IV Semester

Course Title: Digital Systems
Course Code: 18B11EC213

Maximum Time: 1 Hr
Maximum Marks: 20

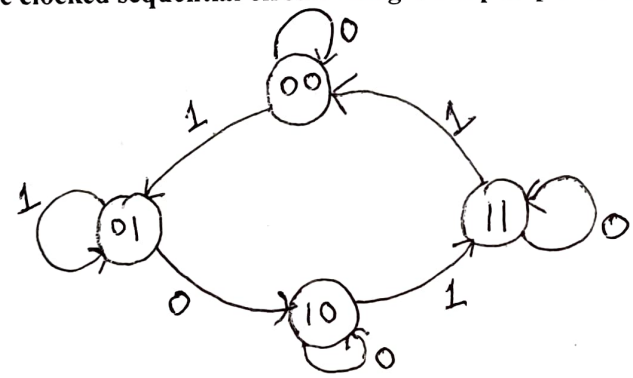
CO1: Familiarize with the fundamentals of number system, Boolean algebra and Boolean function minimization techniques.
CO2: Analyze and design combinational circuit using logic gates.
CO3: Analyze state diagram and design sequential logic circuits using flip flops.
CO4: Understand the classification of signals and systems and learn basic signal operations and Fourier analysis.
CO5: Understand various steps involved in digitization and transmission of signal.

Note: Attempt all questions. All questions are compulsory.

Q. 1 Convert D flip flop in to JK flip flop. [CO3, 4]

Q. 2 Design a 2-bit magnitude comparator using 1-bit magnitude comparator. [CO2, 4]

Q. 3 Design the clocked sequential circuit using JK flip flop whose state diagram is shown below: [CO3, 4]



Q. 4 Design a MOD-5 counter to count the random sequence 0, 1 3, 7, 6. Design should be circulatory to ensure that if we end in any unwanted state, the next clock pulse will reset the counter to zero. Implement the circuit using T-flip flop. [CO3,4]

Q. 5 Design a 4-bit bidirectional shift register with parallel load such that its mode control is as given below. (using 4 x 1 MUX) [CO3, 4]

Mode Control		Register Operation
S1	S0	
0	0	Parallel load
0	1	No change
1	0	Shift right
1	1	Shift left

Solution T2.

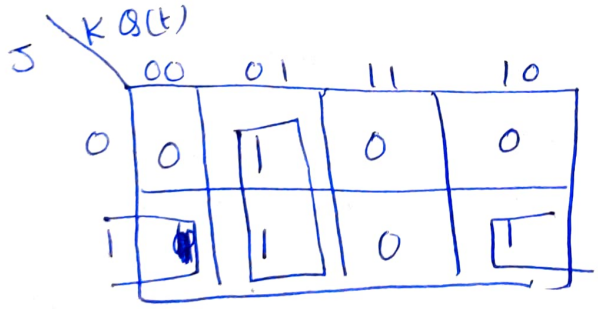
Ques 1 Convert D flip flop into JK Flip Flop.

Soln 1

Desired Flip Flop

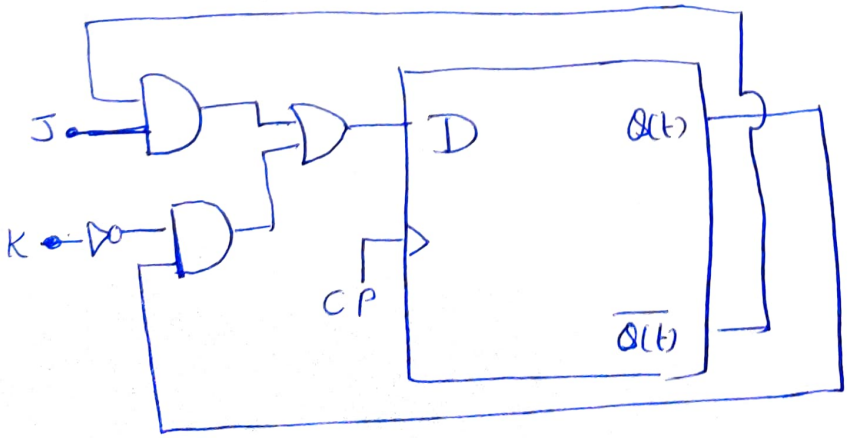
J	K	Q(t)	Q(t+1)	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

—— (1-5) Marks



$D = J\overline{Q(t)} + \overline{K}Q(t)$

1 —— (1-5) Marks



—— (1) Mark

Ques 2 Design a two bit magnitude comparator using 1-bit comparator

Solⁿ 2

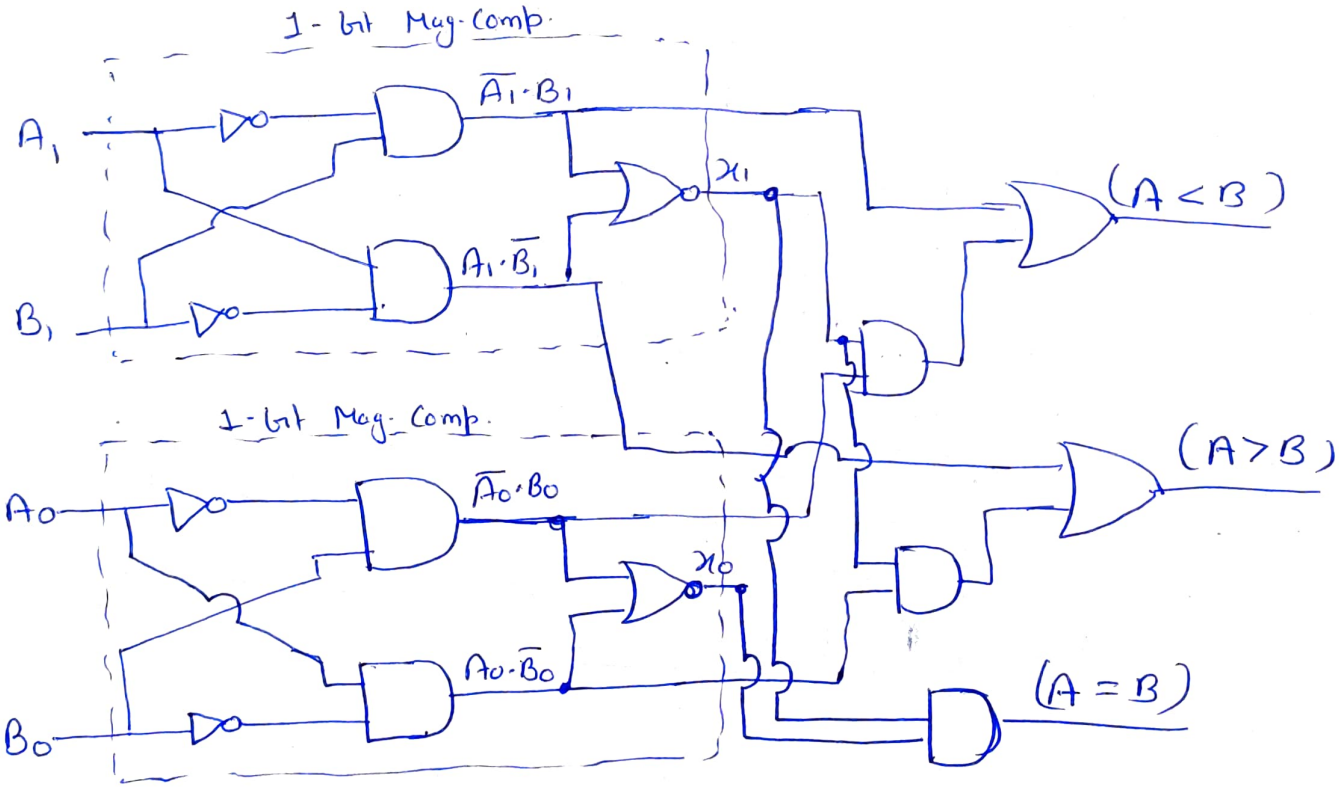
$(A \geq B) = x_1 \cdot A_0 \bar{B_0} + A_1 \bar{B_1}$

$(A < B) = \bar{A_1} \cdot B_1 + x_1 \bar{A_0} B_0$

$(A = B) = x_1 \cdot x_0$ where $x_1 = A_1 B_1 + \bar{A_1} \bar{B_1}$

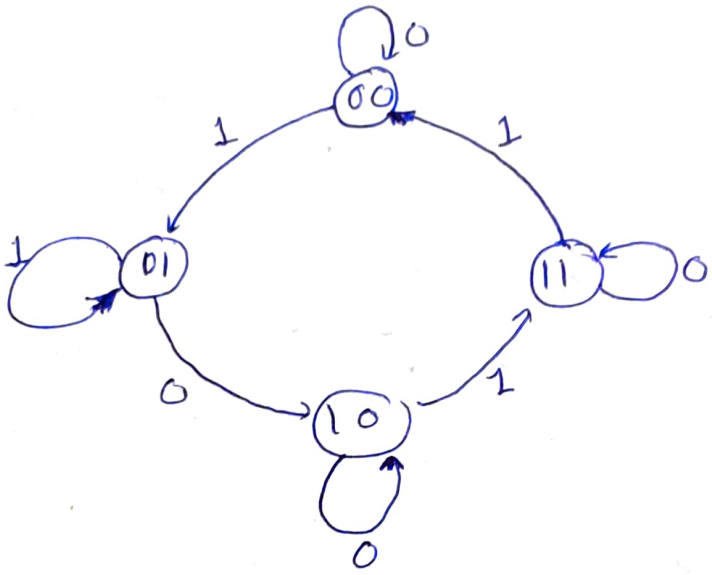
$x_0 = A_0 B_0 + \bar{A_0} \bar{B_0}$

(1·5) Marks



(2·5) Marks

Ques 3 Design the clocked sequential circuit using JK flip flop whose state diagram is shown below



Solution 3

Present State A	Present State B	Input x	Next State A	Next State B	Flip Flop Inputs J_A	K_A	J_B	K_B
0	0	0	0	0	0	x	0	x
0	0	1	0	1	0	x	1	x
0	1	0	1	0	1	x	x	1
0	1	1	0	1	0	x	x	0
1	0	0	1	0	x	0	0	x
1	0	1	1	1	x	0	1	x
1	1	0	1	0	x	0	x	0
1	1	1	0	0	x	1	x	1

(1) Mark

For J_A

A \ Bx	00	01	11	10
0	0	0	0	1
1	x	x	x	x

$\overline{J_A = B\bar{x}}$ -(0.5)

For K_A

A \ Bx	00	01	11	10
0	x	x	x	x
1	0	0	1	0

$K_A = Bx$ (0.5)

For J_B

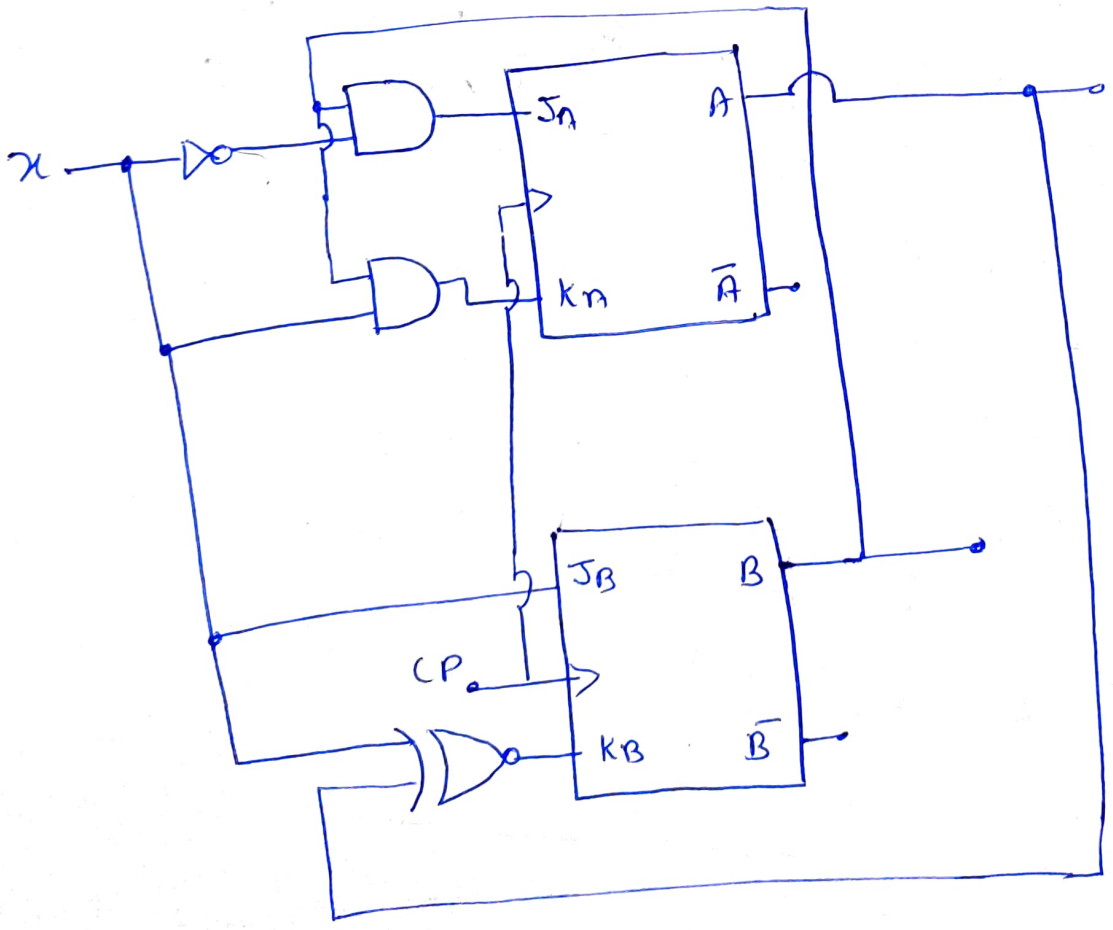
A \ Bx	00	01	11	10
0	0	1	x	0
1	0	1	x	0

$J_B = x$ — (0.5)

For K_B

A \ Bx	00	01	11	10
0	x	x	0	1
1	x	x	1	0

$K_B = A \odot x$ — (0.5)

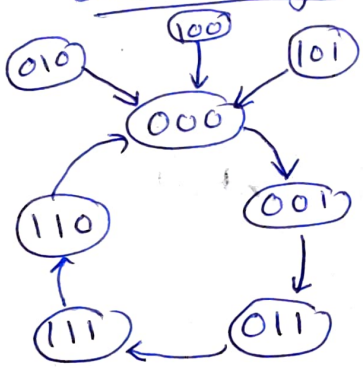


(1) Mark.

Ques 4 Design a module-5 counter to count the random sequence 0, 1, 3, 7, 6. Design should include circulatory to ensure that if we end in any unwanted state. The next clock pulse will reset the counter to zero. Implement the circuit using T-Flip Flop.

Solution

State Diagram



(1.5) Marks

$Q_2 Q_1 Q_0$	$Q_2^+ Q_1^+ Q_0^+$	T_2	T_1	T_0
0 0 0	0 0 1	0	0	1
0 0 1	0 1 1	0	1	0
0 1 0	0 0 0	0	1	0
0 1 1	1 1 1	1	0	0
1 0 0	0 0 0	1	0	0
1 0 1	0 0 0	1	0	1
1 1 0	0 0 0	1	1	0
1 1 1	1 1 0	0	0	1

For T_2

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	1	0
1	1	1	0	1

$$T_2 = Q_2 Q_1 + Q_2 \bar{Q}_0 + \bar{Q}_2 Q_1 Q_0$$ — (0.5)

For T_1

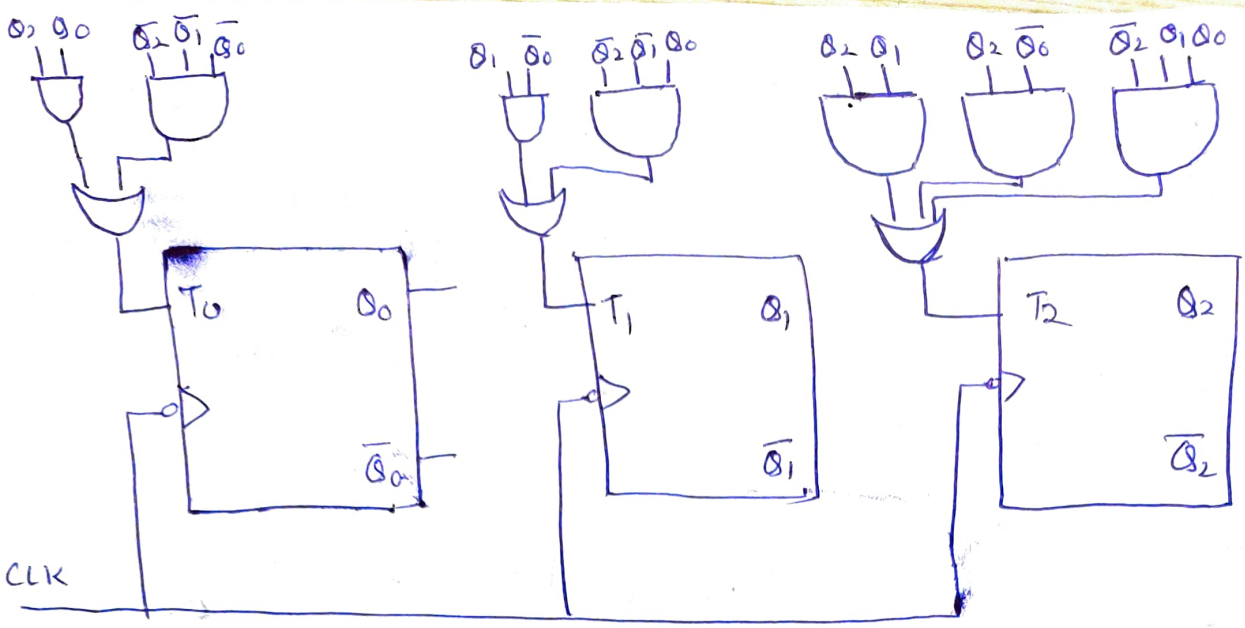
Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	0	1
1	0	0	0	1

$$T_1 = Q_1 \bar{Q}_0 + \bar{Q}_2 \bar{Q}_1 Q_0$$ — (0.5)

For T_0

Q_2 \ Q_1Q_0	00	01	11	10
0	1	0	0	0
1	0	1	1	0

$$T_0 = \bar{Q}_2 \bar{Q}_1 \bar{Q}_0 + Q_2 Q_0$$ — (0.5)



(1) Mark

Ques 5 Design a 4-bit bidirectional shift register with parallel load such that its mode control as given below. (using 4×1 MUX)

Mode control S_1	S_0	Register Operation	Color Line
0	0	Parallel load	→ (1) Mark
0	1	No change	→ (1) Mark
1	0	Shift Right	→ (1) Mark
1	1	Shift left.	→ (1) Mark

Solution