



# TheSyDeKick

System development and verification framework in  
Python

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Authors: TheSyDeKick contributors

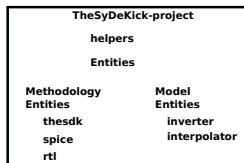
October 24, 2022

# Outline

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- Simulator interfaces
- Analog simulator interface
- Digital simulator interface
- Example 1: Inverter
- Example 2: Inverter chain
- Example 3: ADC model
- Example 4: Multi-user MIMO receiver
- Example 5: Outphasing transmitter
- Example 6: A-Core RISC-V processor chip
- Conclusion and acknowledgements

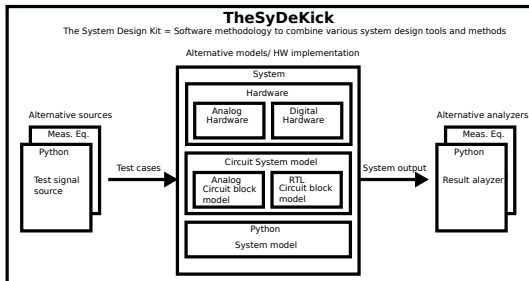
# TheSyDeKick - What it is

# What is it?



- ▶ TheSyDeKick is a well structured container for:
  - ▶ Python packages (Entities), that provide *formalism and methods to run simulations in python, and with external simulators*
  - ▶ Python packages (Entities), that provide formalism to create and use *IO compatible models*
- ▶ TheSyDeKick is a cumulative collection of Python classes and methods that help the designer to carry out the most common tasks encountered in microelectronics design. Most likely the *simulation task you have in mind has some supporting methodology available in TheSyDeKick*
- ▶ TheSyDeKick is *nothing more*

# What is it?



- ▶ TheSyDeKick formalism helps the designed to:
  - ▶ Write and simulate modular, hierarchical, IO compatible hardware models with various levels of abstraction (python, spice/rtl)
  - ▶ Control the abstraction level with one parameter on chosen level of hierarchy.

# What is it?

- ▶ Minimum set of structural constraints,
  - ▶ IO definitions
  - ▶ Blocks described as connected *Entities*.
- ▶ Aims to automation of *repetitive, well structured tasks*
  - ▶ Model and modeling environment structure with init scripts
  - ▶ Running simulations
  - ▶ Defining simulator calls
  - ▶ Documentation of the design with Docstrings
- ▶ Currently supports Python, Verilog, VHDL and three Spice variants.
- ▶ Open source simulators: Icarus for Verilog, NgSpice for analog circuits.
- ▶ Under construction: Measurement equipment.
- ▶ <https://github.com/TheSystemDevelopmentKit>

# TheSyDeKick project file structure

## TheSyDeKick project structure

```
thesydekick_project/  
├── Entities/  
│   ├── thesdk/  
│   ├── rtl/  
│   ├── spice/  
│   └── amplifier/  
│       ├── amplifier/  
│       │   └── __init__.py  
│       ├── spice/  
│       ├── Simulations/  
│       └── doc/
```

# Simulator interfaces



# Analog simulator interface

- ▶ Calling analog simulators is handled through a common interface, the **spice** module
- ▶ Ultimate goal of **spice**: support for most industry standard simulators
  - ▶ General (w.r.t to simulator), reusable simulation testbenches
  - ▶ Centralized post processing based on open source tools and libraries.
- ▶ Save time in re-writing testbenches for different simulations and centralize effort to all-in-one testbench
  - ▶ Currently support for DC, AC, and Transient analysis. Easy to add other analysis types as IO formats are the same.
- ▶ <https://github.com/TheSystemDevelopmentKit/spice>

# Digital simulator interface

- ▶ Calling digital simulators is handled the **rtl** module
  - ▶ Most commonly used simulation testbenches automatically generated for both Verilog and VHDL design under tests.
  - ▶ Automated file IO generation for strings (bit vectors), integers, and complex numbers.
  - ▶ Support for any signal type through customizable format parameter.
- ▶ <https://github.com/TheSystemDevelopmentKit/rtl>

# TheSyDeKick simulation procedure

## 1 Write the testbench

- 1 Specify analysis type, inputs, outputs, supplies etc. based on TB properties
- 2 Configure simulator options, corners, etc. based on testbench properties
- 3 Specify desired outputs, e.g. FFT of waveform, transient waveform
- 4 Specify run cases, e.g. transient analysis for 2 different netlists, etc.

## 2 Run the simulation

## 3 Analyze results

## 4 (Optional) Repeat simulation for different sets of parameters

- Once you have one testbench, reuse for similar applications makes things faster
- Results saved (if user chooses so), no need to repeat lengthy simulations to fix errors in post processing

# Example 1: Inverter

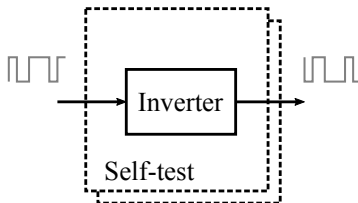
# Example 1: Inverter



- ▶ Functional model: Inverts input signal
- ▶ IOS is a Bundle-type container for storing IO data
- ▶ Can have as many members as needed

# Example 1: Inverter

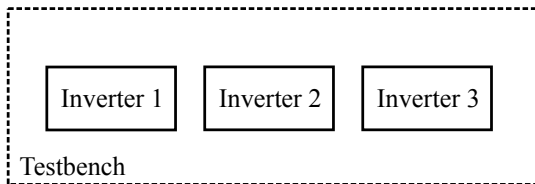
Python / VHDL / SystemVerilog / Eldo



- ▶ Multiple representations of the same entity
- ▶ Self-test is a way to verify the functionality of entity “in vacuum”
- ▶ Self-test generates and feeds the identical input data to all simulators

## Example 2: Inverter chain

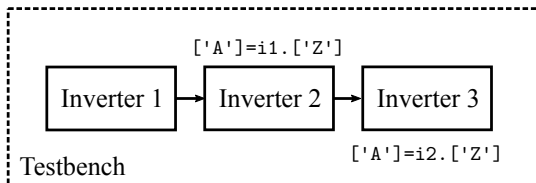
## Example 2: Inverter Chain



- ▶ A separate **Testbench** entity is instantiated
- ▶ Chain of inverter instance is created with a for loop




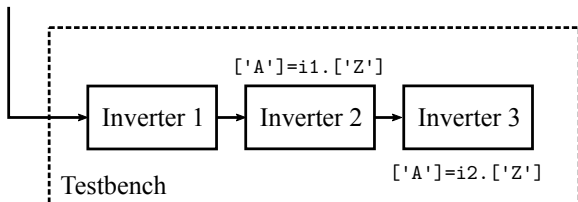
## Example 2: Inverter Chain



- ▶ A separate **Testbench** entity is instantiated
- ▶ Chain of inverter instance is created with a for loop
- ▶ Data flow defined by IOS connections


## Example 2: Inverter Chain

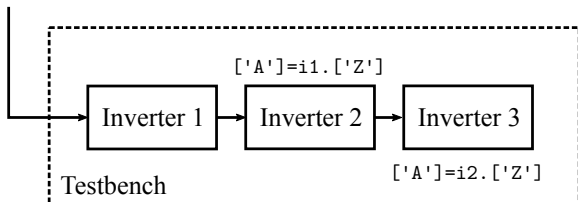
i1.['A'].Data= 



- ▶ A separate **Testbench** entity is instantiated
- ▶ Chain of inverter instance is created with a for loop
- ▶ Data flow defined by IOS connections
- ▶ Testbench input is assigned as input of 1st element

## Example 2: Inverter Chain


i1.['A'].Data= 

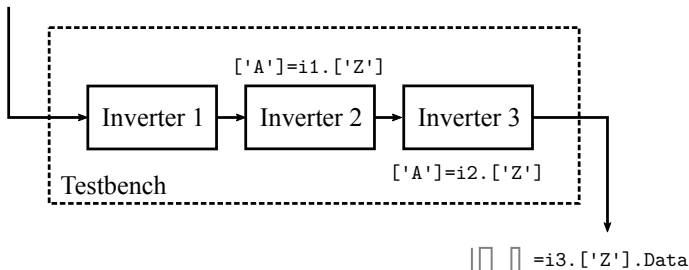


i1.Run() -> i2.Run() -> i3.Run()

- ▶ A separate **Testbench** entity is instantiated
- ▶ Chain of inverter instance is created with a for loop
- ▶ Data flow defined by IOS connections
- ▶ Testbench input is assigned as input of 1st element
- ▶ Signal is propagated through the chain by running the entities in sequence

## Example 2: Inverter Chain

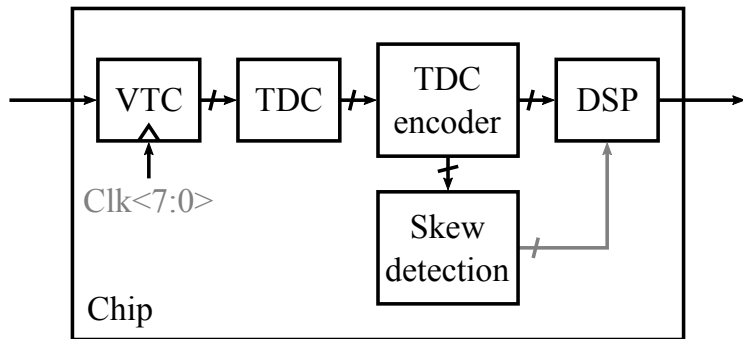
i1.['A'].Data= 



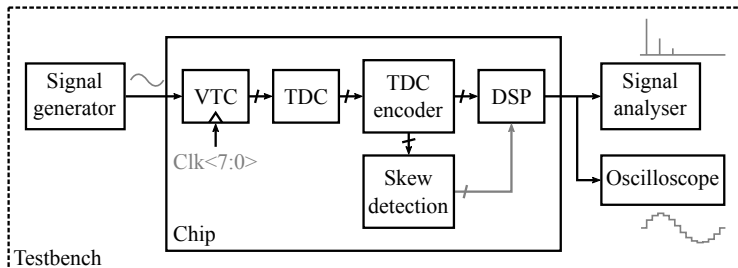
- In the end, the output of the last element contains processed data

## Example 3: ADC model

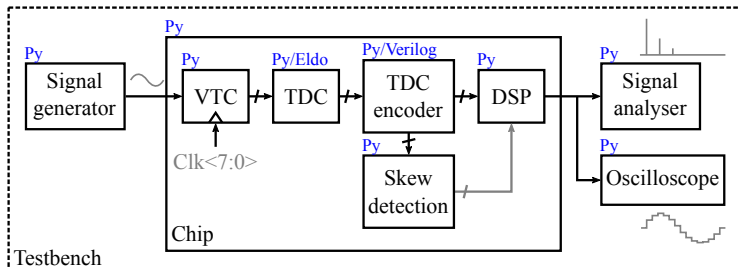
## Example 3: ADC Model



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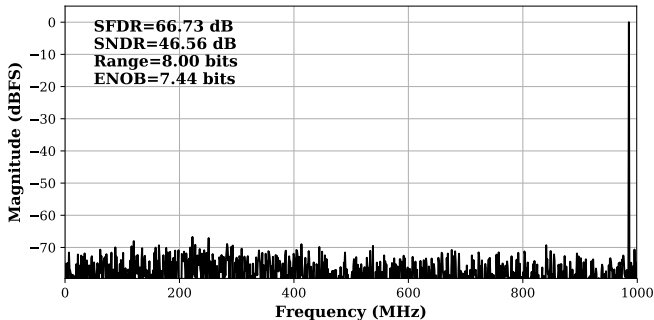
# Example 3: ADC Model





# Example 3: ADC Model

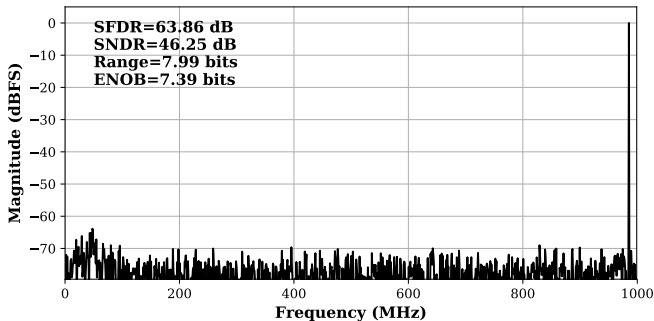
## Full ADC Model in Python



- Spectrum plotted by `signal_analyser` -module, which also calculates SNDR etc.

## Example 3: ADC Model

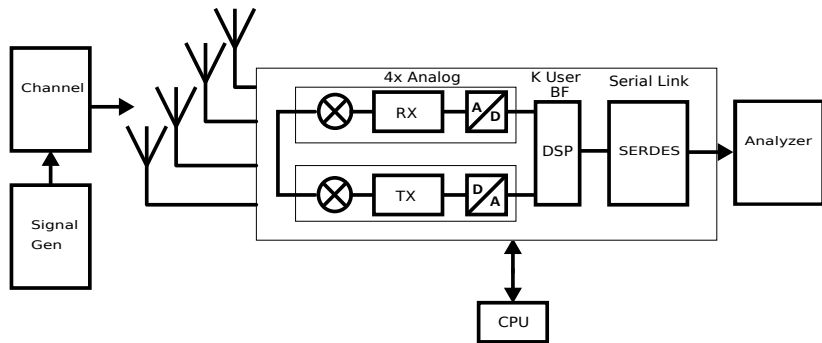
Full ADC Model in Python with Transistor-level TDC Model



- Same exact simulation as before, except the TDC block is simulated as a spice-netlist in Eldo

## Example 4: Multi-user MIMO receiver

## Example 4: Multi-user MIMO receiver



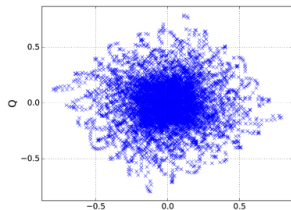
### ► Goals:

- First, model the receiver of a single chip with python
- Python models swappable to RTL and analog models
- Generated sub-blocks verified at the system level
- Control the HW generators of the block (emerging feature)

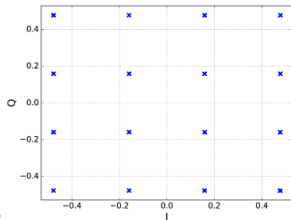
## Channel 802.11n C



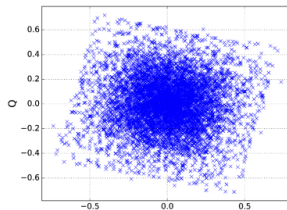
DSP, Ant=0, Usrc=0, py, EVM=0.19 dB, BER= 0.364



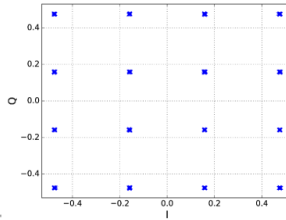
Postproc, Usrc=0, py, EVM=-55.09 dB, BER= 0



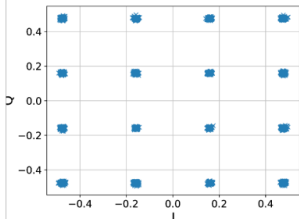
DSP, Ant=0, Usrc=1, py, EVM=2.09 dB, BER= 0.453



Postproc, Usrc=1, py, EVM=-52.50 dB, BER= 0

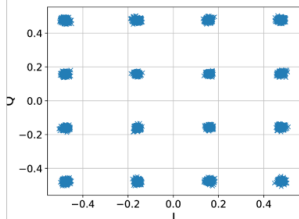


Postproc, U<sub>sr</sub>=0, py, EVM=-40.96 dB, BER= 0



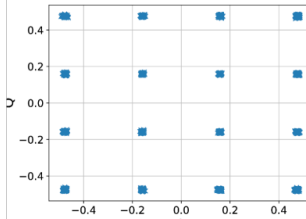
DSP Decimator in python

Postproc, U<sub>sr</sub>=0, py, EVM=-34.47 dB, BER= 0



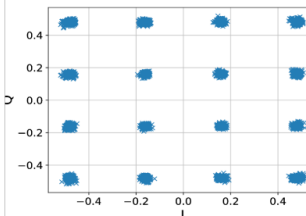
DSP Decimator in verilog

Postproc, U<sub>sr</sub>=1, py, EVM=-41.39 dB, BER= 0



DSP Decimator in python

Postproc, U<sub>sr</sub>=1, py, EVM=-33.41 dB, BER= 0

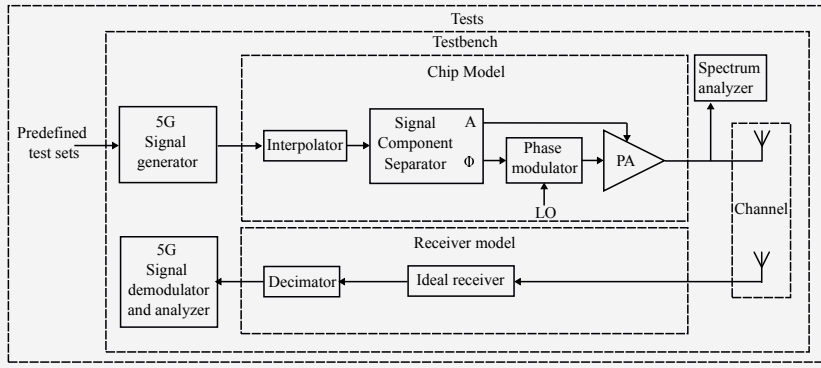


DSP Decimator in verilog

## Example 5: Outphasing transmitter

# Outphasing transmitter system

## Outphasing system simulation

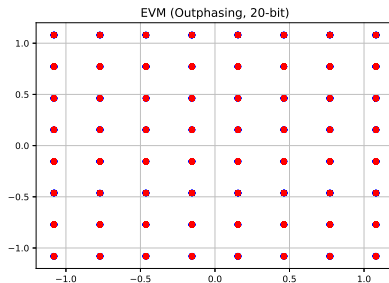
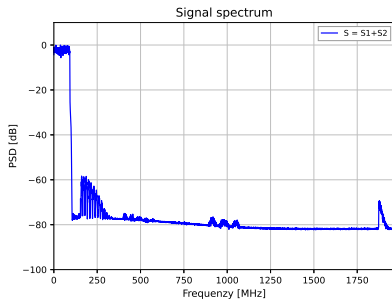


### ► System development

- Model the transmitter chip with python
- Model the ideal receiver in python
- Simulate the functionality



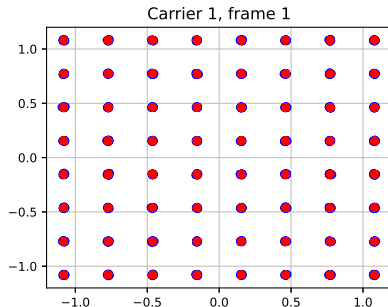
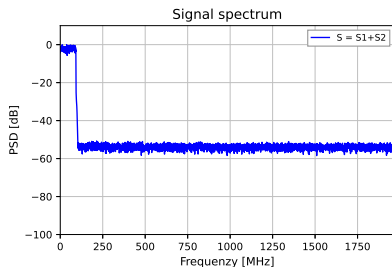
# Outphasing transmitter system



► EVM 0.34

# Outphasing transmitter system

- ▶ System verification
  - ▶ Replace the transmitter DSP with RTL models
  - ▶ Verify functionality

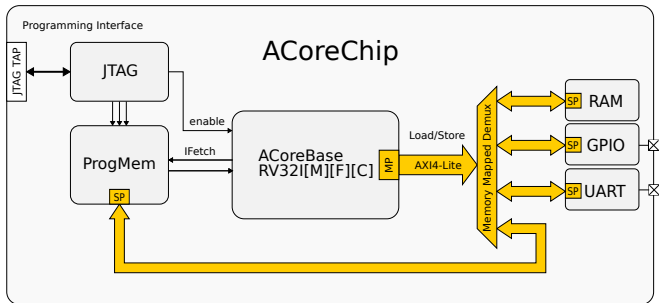


- ▶ EVM=0.60

## Example 6: A-Core RISC-V processor chip

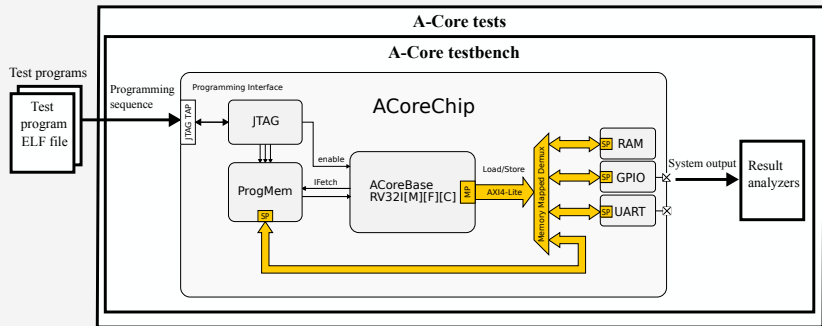
# A-Core RISC-V processor chip

- ▶ SoC built with ACoreBase
- ▶ AXI4-Lite on-chip interconnect
- ▶ Memory mapped peripherals
  - ▶ Random Access Memory (RAM)
  - ▶ Read-only access to instruction memory (ProgMem)
  - ▶ General Purpose Input/Output (GPIO)
  - ▶ Custom accelerator IP



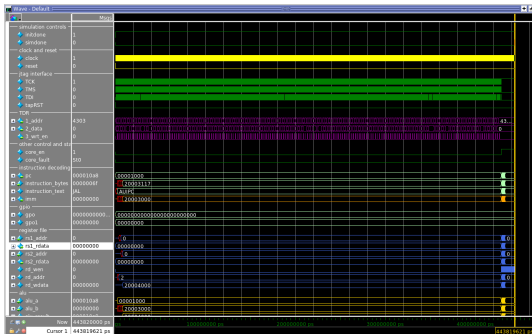
# A-Core chip verification

## A-Core test setup



# TheSyDeKick simulations

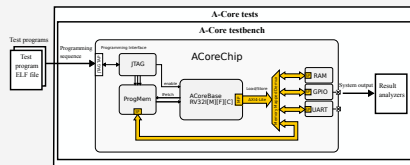
- ▶ For system-level simulations
- ▶ TheSyDeKick automates the following verification tasks
  - ▶ Generate a simulation test vector
    - ▶ JTAG programming waveform from ELF file
    - ▶ Chip control signals (e.g. core enable)
  - ▶ Generate a verilog testbench
  - ▶ Invoke a digital simulator (ModelSim)



# ACoreChip Entity

- ▶ Represents a simulatable model of ACoreChip
- ▶ Submodules
  - ▶ ACoreChip Chisel generator **chisel/**

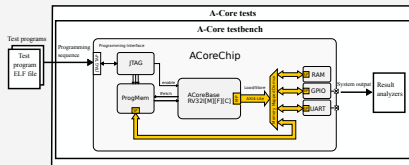
## A-Core test setup



# ACoreTestbenches

- ▶ ACoreTestbenches instance represents a test bench configuration.
- ▶ Testbench configuration is selected with appropriate `define*` method
  - ▶ For example, **`define_acorechip_sim_testbench(**kwargs)`** configures test-bench as a acorechip simulation.
  - ▶ Software, jtag config., etc. are provided as keyword arguments to **`define*`**

## A-Core test setup

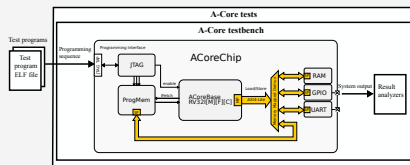




# ACoreTestbenches

- ▶ A testbench configuration is a general combination of entities and related configuration for representing a unique test setup.
- ▶ The simulation testbench has two options: The SyDeKick and cocotb
  - ▶ The SyDeKick uses its own structures to generate the Verilog testbench, IO's and run with modelsim
  - ▶ Cocotb runs a cocotb test - can be used to create interactive debug environments in the future

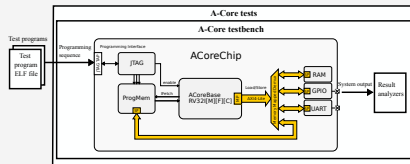
## A-Core test setup



# ACoreTests

- ▶ ACoreTests contains different concrete parameterizations of ACoreTestbenches and their dependencies:
  - ▶ Test software live under **sw/**
  - ▶ Simulation specific do-files live under **interactive\_control\_files/nodelsim**
- ▶ Each test is defined as a method under ACoreTests class.
- ▶ For example, `sim_f_tests` configures a testbench with
  - ▶ F-extension enabled
  - ▶ test program for f-extension

## A-Core test setup



# ACoreTests

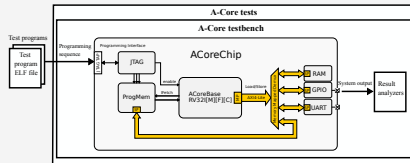
- ▶ The test to be executed is selected with a command line argument. For example,  

```
$ ./configure && make sim test_target=sim_f_tests
```

runs the simulation defined as `sim_f_tests`
- ▶ The simulator option can be selected with `simulator` argument for `make`, for example  

```
$ make sim test_target=sim_f_tests simulator=cocotb
```

## A-Core test setup



# Conlusion and acknowledgements

# Conclusion

- ▶ Modular design environment through well defined IO boundaries and *Entity* definitions.
- ▶ Open Source
- ▶ Automates repetitive verification tasks and provides means for programmatic verification with various simulators
- ▶ Support for measurement equipment under development.
- ▶ *Enables* co-development by multiple designers using various verification tools.
- ▶ *Enabled by* utilization of programming methodology and version control in hardware design context.

# Acknowledgement

- ▶ TheSyDeKick framework has been initiated during 2017-2019 under Marie Skłodowska-Curie project *ADVANTAG5*, in collaboration with Aalto University and University of California, Berkeley. (See licences, <https://github.com/TheSystemDevelopmentKit/thesdk> )
- ▶ Since the end of *ADVANTAG5* 2019, Lot of valuable development work has been carried out by several students of Aalto University, Finland.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement No 704947. Results reflects only the author's view and the European Comissions's Research Executive Agency Agency is not responsible for any use that may be made of the information it contains.