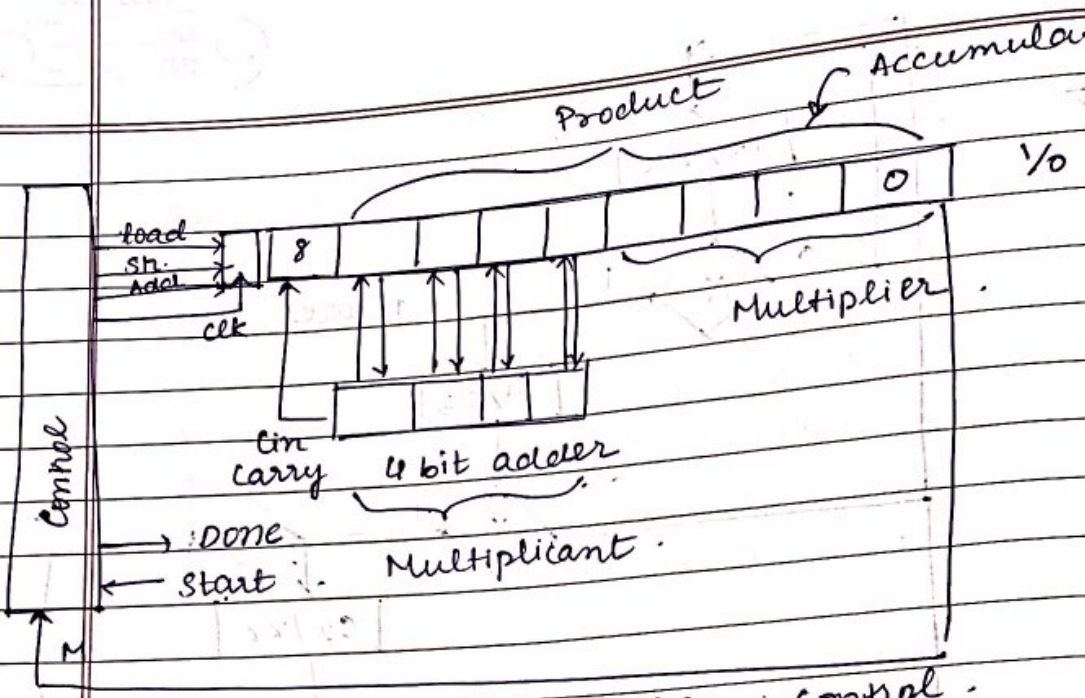


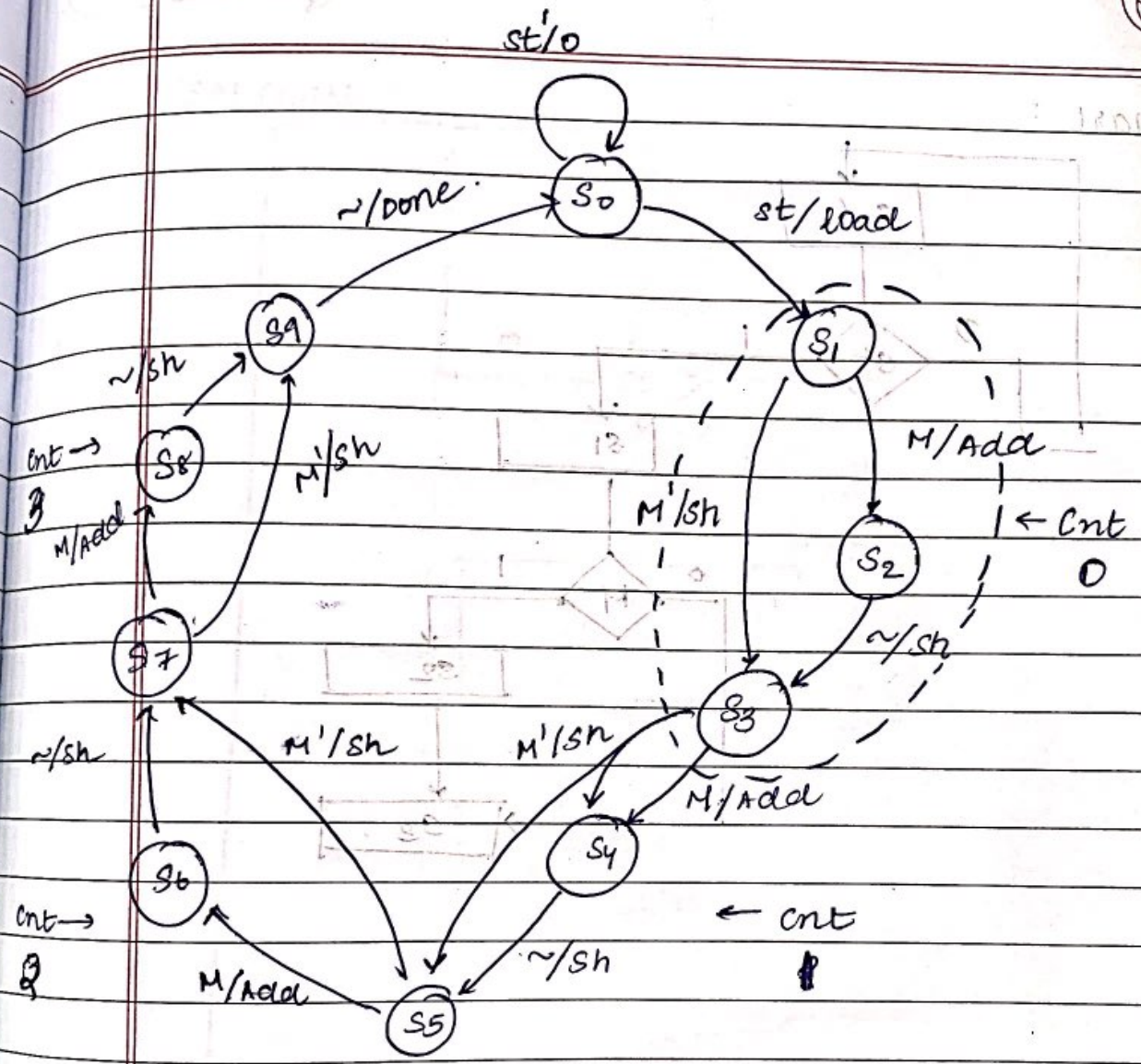
Shift Add Multiplier (control.

- Add - The adder O/P are transfered to the accumulator by the next clock pulse

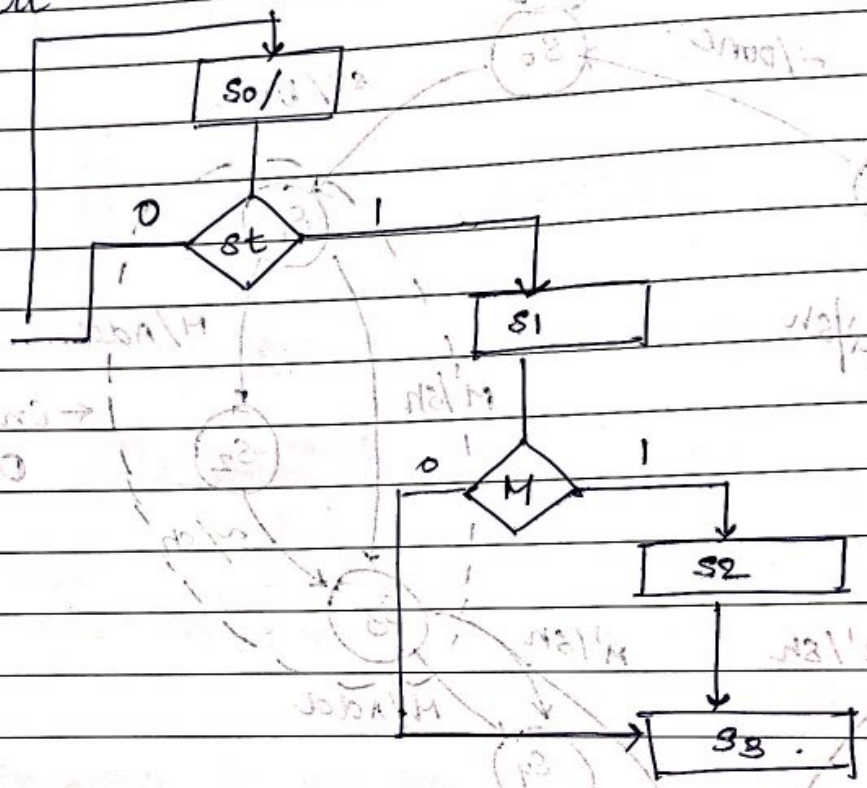
- Sh(Shift) - Shift occurs then all 9 bits of the acc. are shifted right by the →

- st → start (Next state).

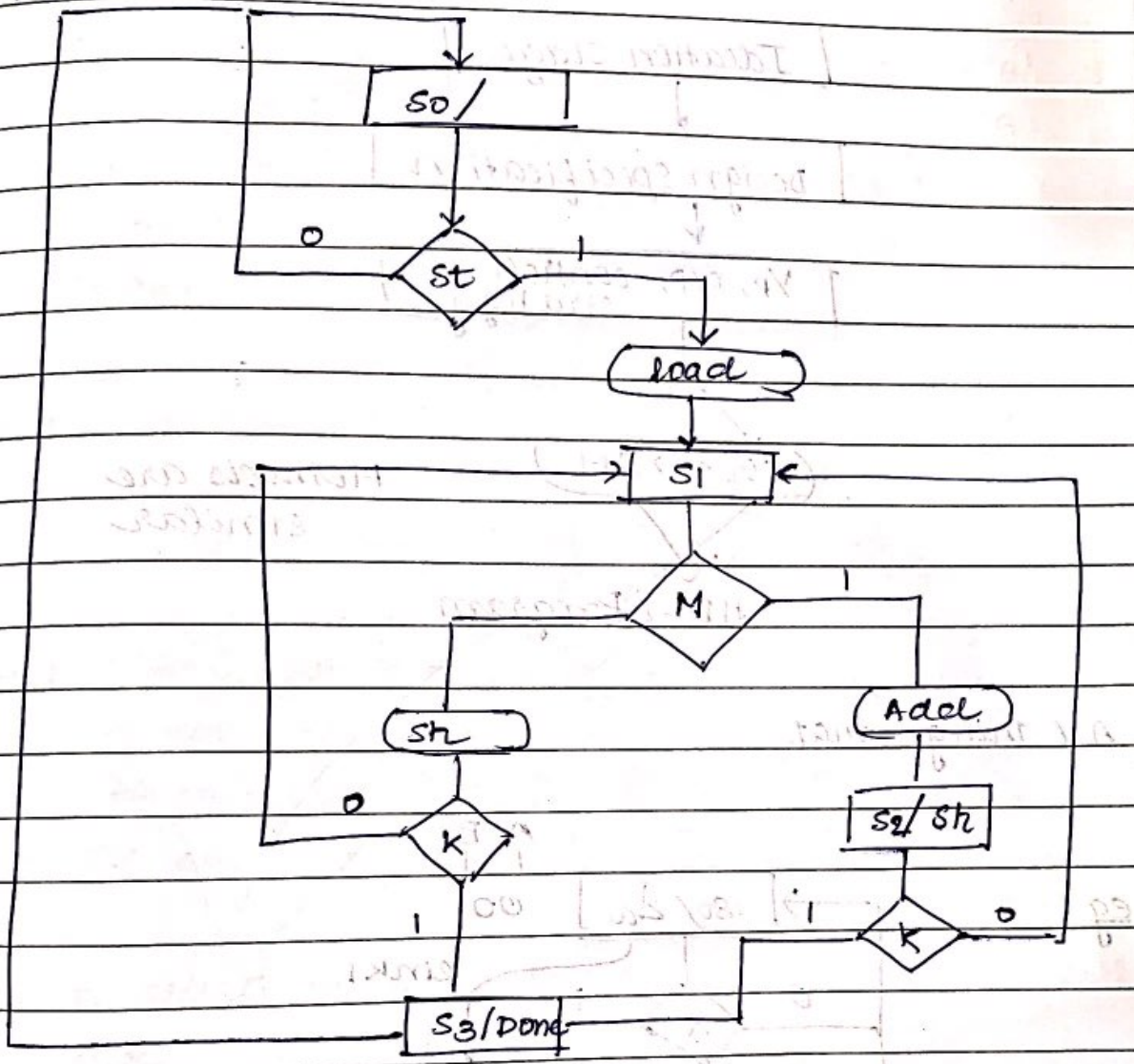
- if M = 1 multiplicant is adder to the acc. followed by a right shift.
  M = 0 followed by a right shift.

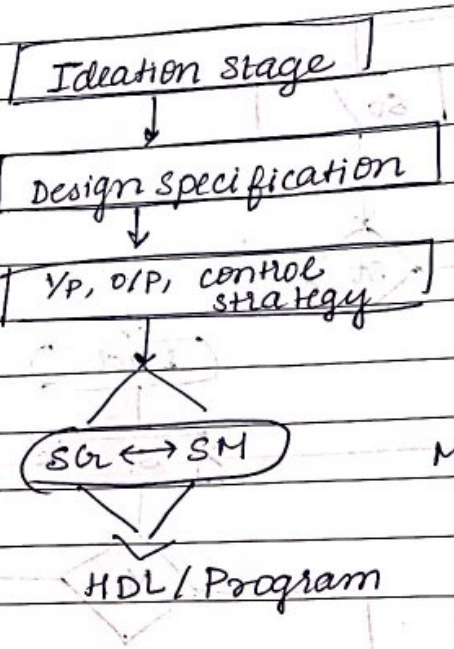


SM chart :



SM chart :

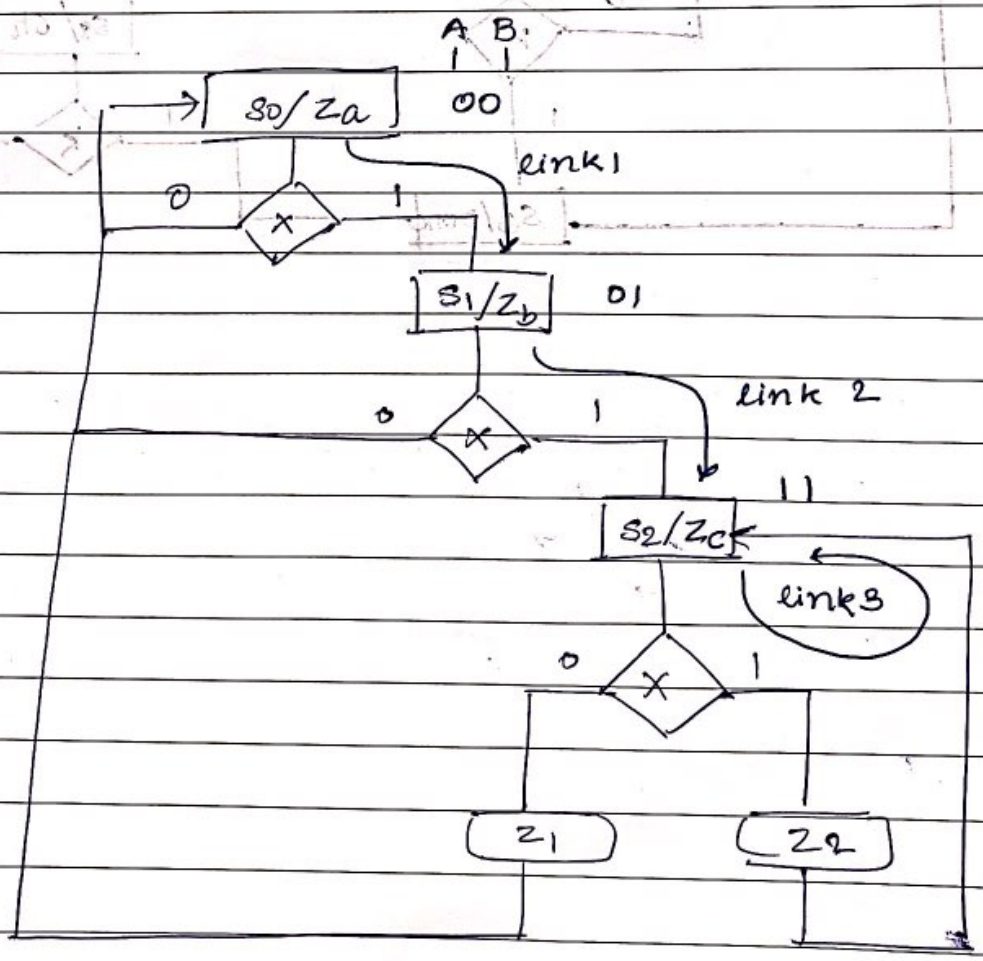




Methods are similar

All things that

eg



Adjacent bits have to be changed by just 1 bit. (00, 01, 11, 10)

$z_a = 1$ only in state 00. $z_a = A'B'$

$z_b = 1$ only in state 01 $z_b = A'B$

$z_c = 1$ only in state 11 $z_c = AB$.

$z_1 = ABx'$

$z_2 = ABx$

Link 1: starts with 00.

takes $x=1$ branch

terminates in $B=1$.

link 1 starts with PS00.

takes $x=1$.

terminates at state which $B=1$.

$\therefore$ NS of B on $B^+ = 1$ when $A'B'x = 1$.

link 2 starts with state 01,

takes $x=1$ branch .....

$B^+ = A'Bx$.

link 3 $B^+ = ABx$

$\therefore$ NS $B^+ = A'Bx + A'B'x + ABx$

$A^+ = A'Bx + ABx$

link 2 link 3.

Procedure for doing SM chart for students :

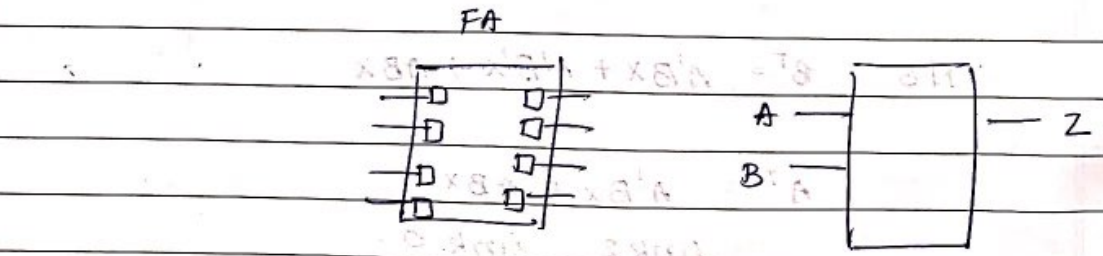
1. Identify all the states in which Q = 1.
2. For each of those states, find all link paths that lead into the state.
3. For each of these link path, find a term that is 1, when the link path is followed.

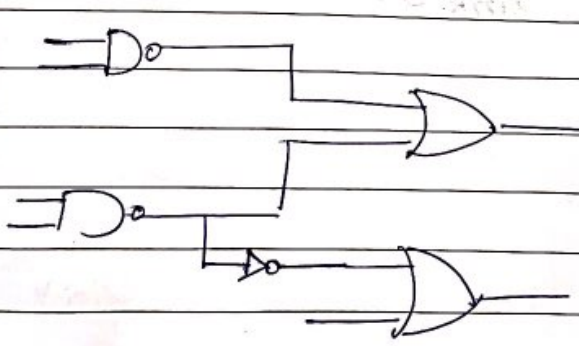
For a link path from S_i to S_j the term will be 1 if the is in state S_i and condition for exiting to S_j satisfies.

4. For expression for Q^+ (NS of Q) is formed by ~~adding~~ ORing together the terms found in stage 3.

Hardware Testing :

Verification	Testing
S/W on HDL	Physical ckts



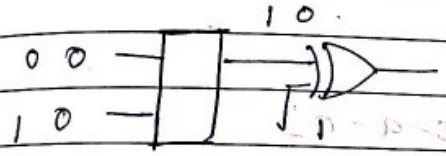


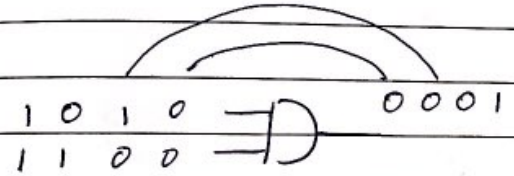
A	0/1	0 0
B	0/1	0 1
		1 0
		1 1

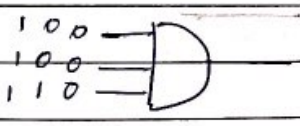
How many test vectors are required?

00	00
01	11
11	10
10	01

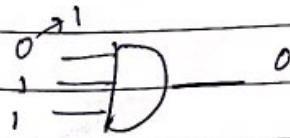
Different

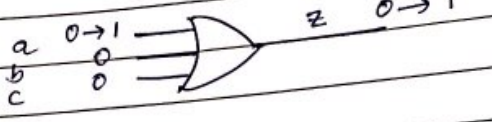




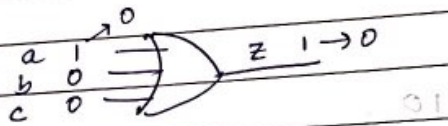


If one of the I/P is stuck as 0 O/P is always 0.

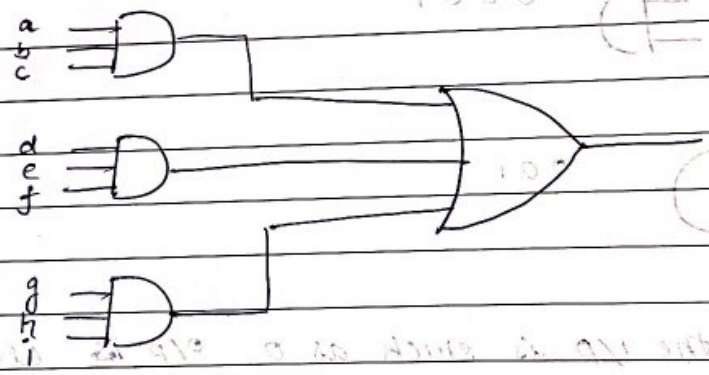




(a1) stuck at 1 (s-a-1)



(a0) stuck at 0 (s-a-0)



(s-a-0 test)

2 level and or

Assume I/p are accesible

bw I/ps to OR is not accesible.

s-a-0 s-a-1 test

in order to change to the OR gate o/p.

Similarly do, eo, fo, go can be tested.

Testing Sequential Logic :

If we can observe all the i/p and o/p sequences and not the states a very large no. of FFs are required

Brute Force Method :

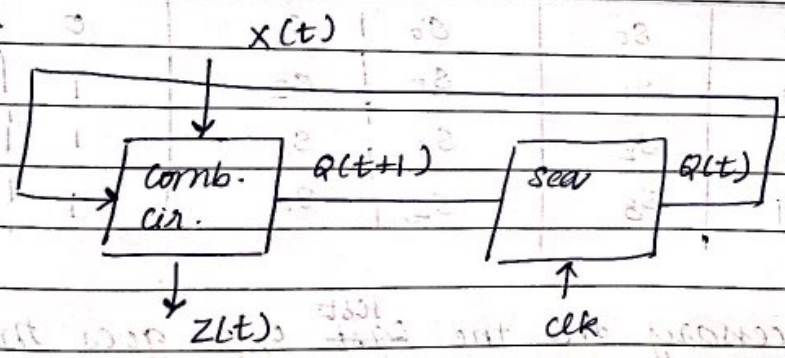
→ Reset → Initial state → Apply a test sequence

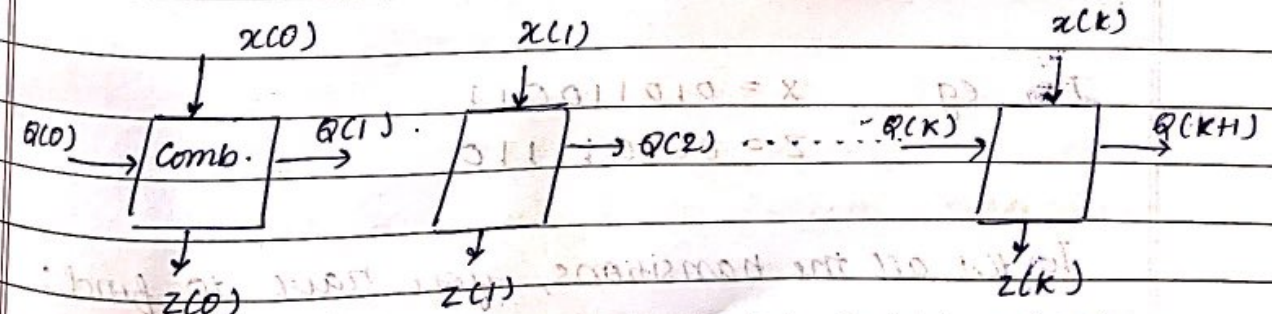
→ observe the output sequence → if correct

→ repeat

Convert in an iterative circuit :

Mealy machine circuit :





K+1 is the logic of

x, z, Q can be shift variable or

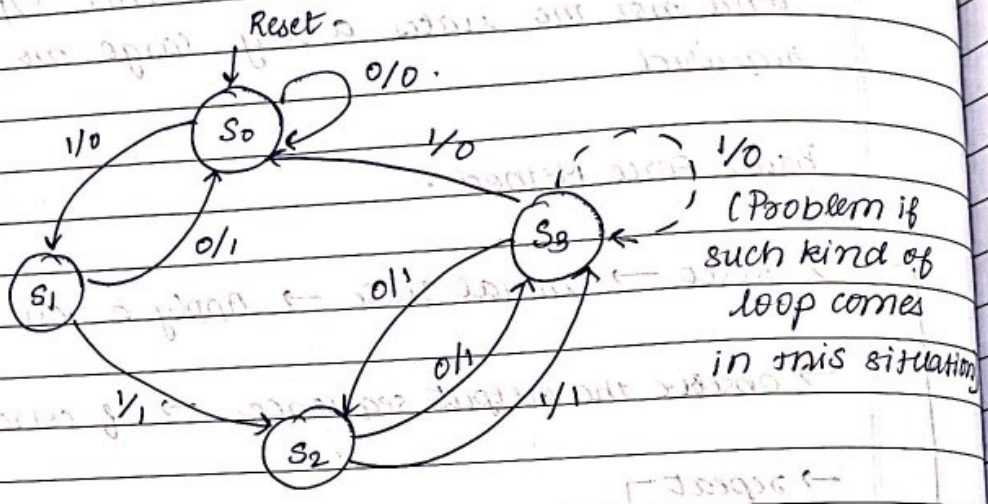


Table:

Q_1	Q_2	State	Next state $x=0$	Next state $x=1$	Output $x=0$	Output $x=1$
0	0	S_0	S_0	S_1	0	1
1	0	S_1	S_0	S_2	1	1
0	1	S_2	S_3	S_3	1	1
1	1	S_3	S_2	S_0	1	0

It is necessary the the ~~last~~ test o/p goes through all the transitions

For eg. x = 0101100111

z = 0010111110

To test all the transitions, you have to find:

Distinguishing sequences:

only 1 finite i/p sequence will cause different o/p sequence

For the above sequence state machine - the distinguishing sequence :

(S_0, S_1, S_2, S_3) groups.

$S_0 . S_3$ $S_1 . S_2$

If i/p = 1 { o/p is 0 for S_0 and S_3
o/p is 1 for S_1 and S_2

1. $S_1 . S_2$ } are distinguished.
S_0 S_3

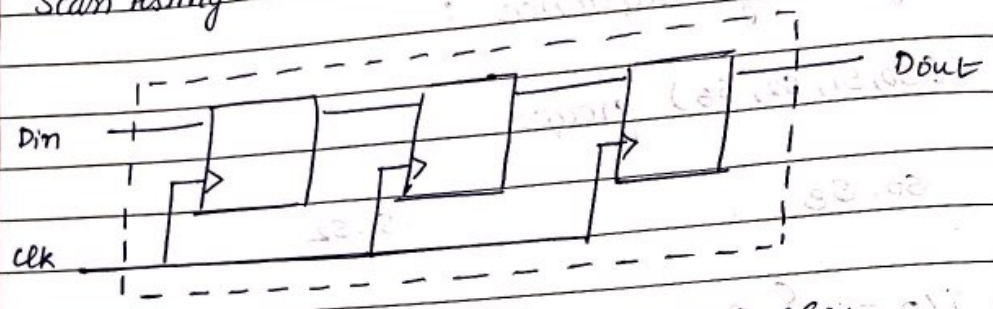
i/p	o/p
Reset 011	001
R 111	010
R 1011	0101
R 1111	0110
R 11011	01100

State graph in which every state can be reached from every other state is called a strongly connected

An input sequence which distinguishes each state from other state is called distinguishing sequence.

The states are distinguishable iff the at least one finite i/p sequence when

Scan testing :

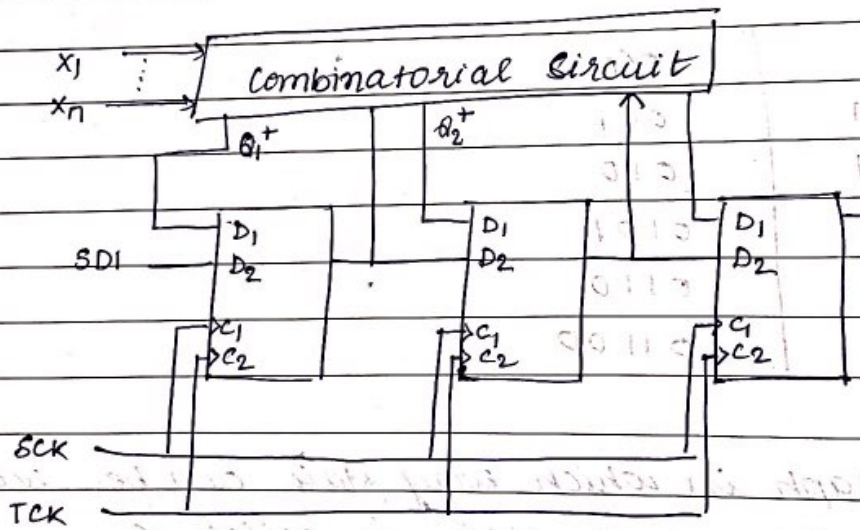


Output must reflect after 3 clock cycles.

Input = 000 Output = 001

01

↳ stuck at 1 in 2nd FF



C1 is pulsed - D1 is

C2 is pulsed - D2 is

NS $Q_1^+, Q_2^+, \ldots$ generated by

when C_1 is pulse $Q_1, Q_2, \ldots$ fed back into the comb. logic

Circuit is not in test

System I/P or O/P { $x_1, x_2, \ldots x_n$ is applied
$z_1, z_2, \ldots z_n$ is generated

Circuit is test

test { SDI.
TCK is applied.

$x_1, x_2, \ldots x_n$ is applied.
$z_1, z_2, \ldots z_n$ is

SCK pulses to the
NS is

Steps to take the scan test:

1. Scan in the test vector q_i values via SDI using TCK (test clk).
2. Apply the test values to x_i inputs.
3. After the combinatorial circuit.
   verify the z_i values (output).
4. Apply on clk