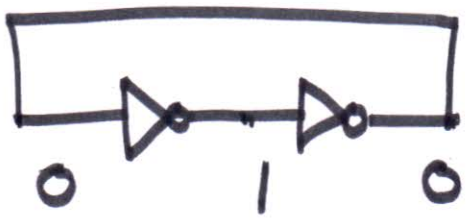
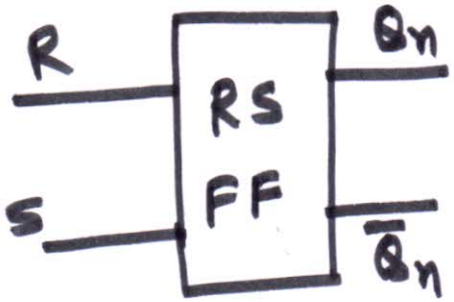
Flip-Flop



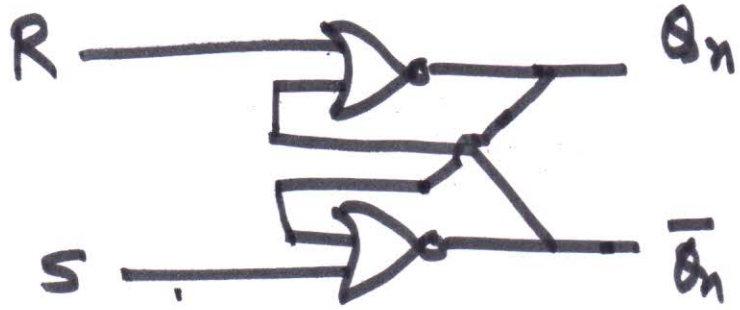
RS Flip-flop

TT

R	S	Q_{n+1}	
0	0	Q_n	(no change)
0	1	1	(set)
1	0	0	(Reset)
1	1	Invalid	



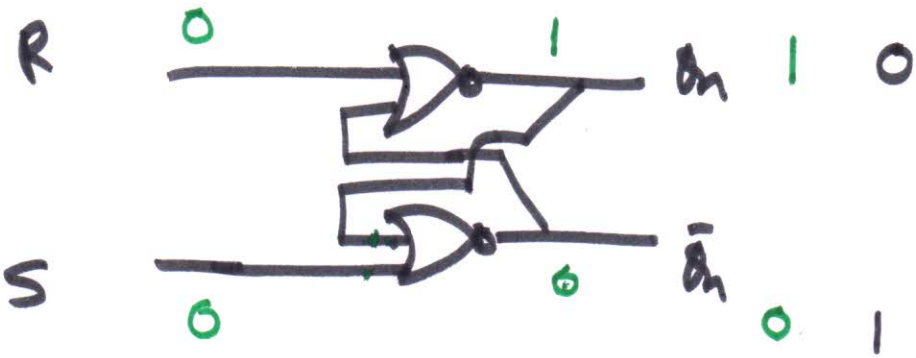
RS Flip Flop using NOR gates



1) $R=0$ & $S=0$

Suppose $Q_n = 1$

So, $\bar{Q}_n = 0$ $\Rightarrow Q_{n+1} = Q_n$



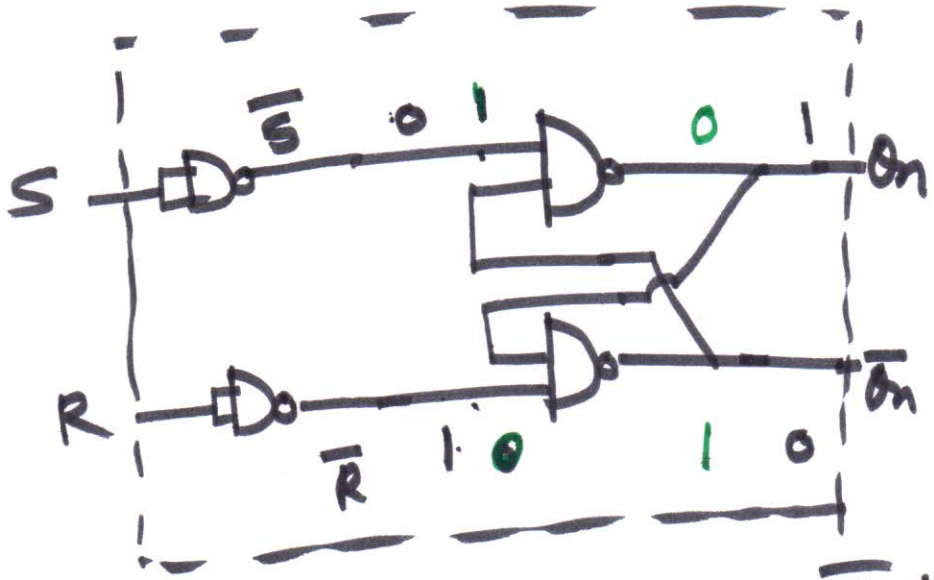
2) $R=0$ & $S=1$

$\Rightarrow Q_{n+1} = 1$

3) $R=1$ & $S=0$

$\Rightarrow Q_{n+1} = 0$

RS Flip-Flop using NAND gates

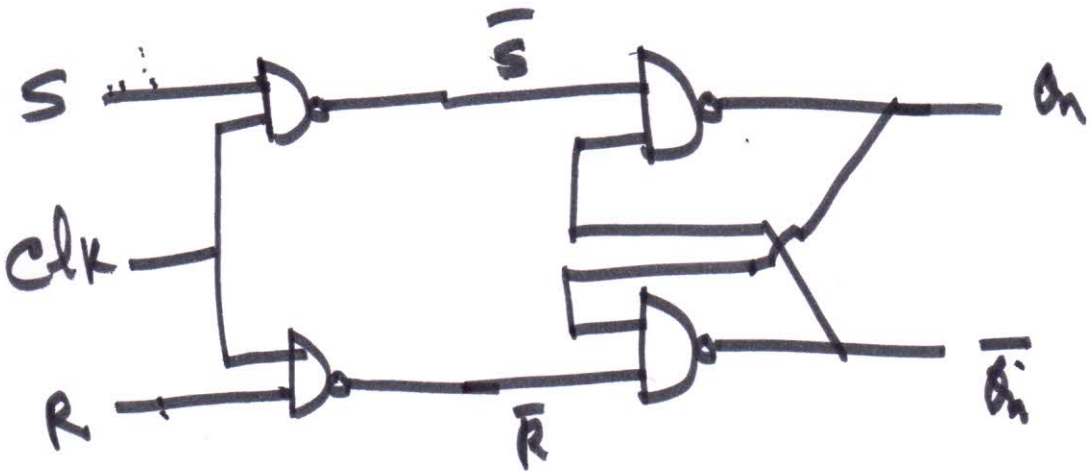


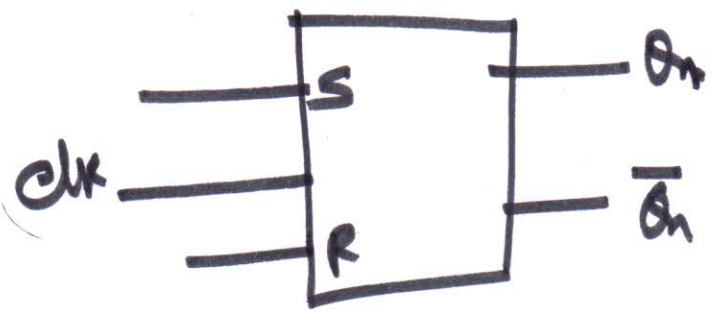
S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Invalid

$\bar{S}$	$\bar{R}$	Q_{n+1}
0	1	1
1	0	0
0	0	Invalid
1	1	Q_n

SR Flip-Flop with clock input

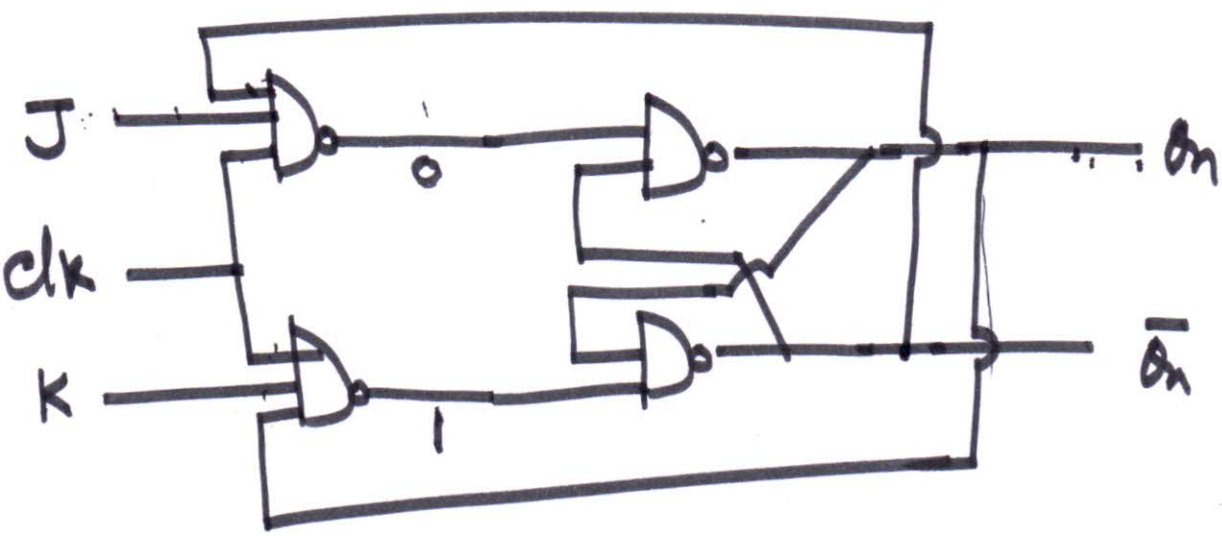
clk	S	R	Q_{n+1}
0	x	x	(x) → Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid





J-K Flip Flop

clk	J	K	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$



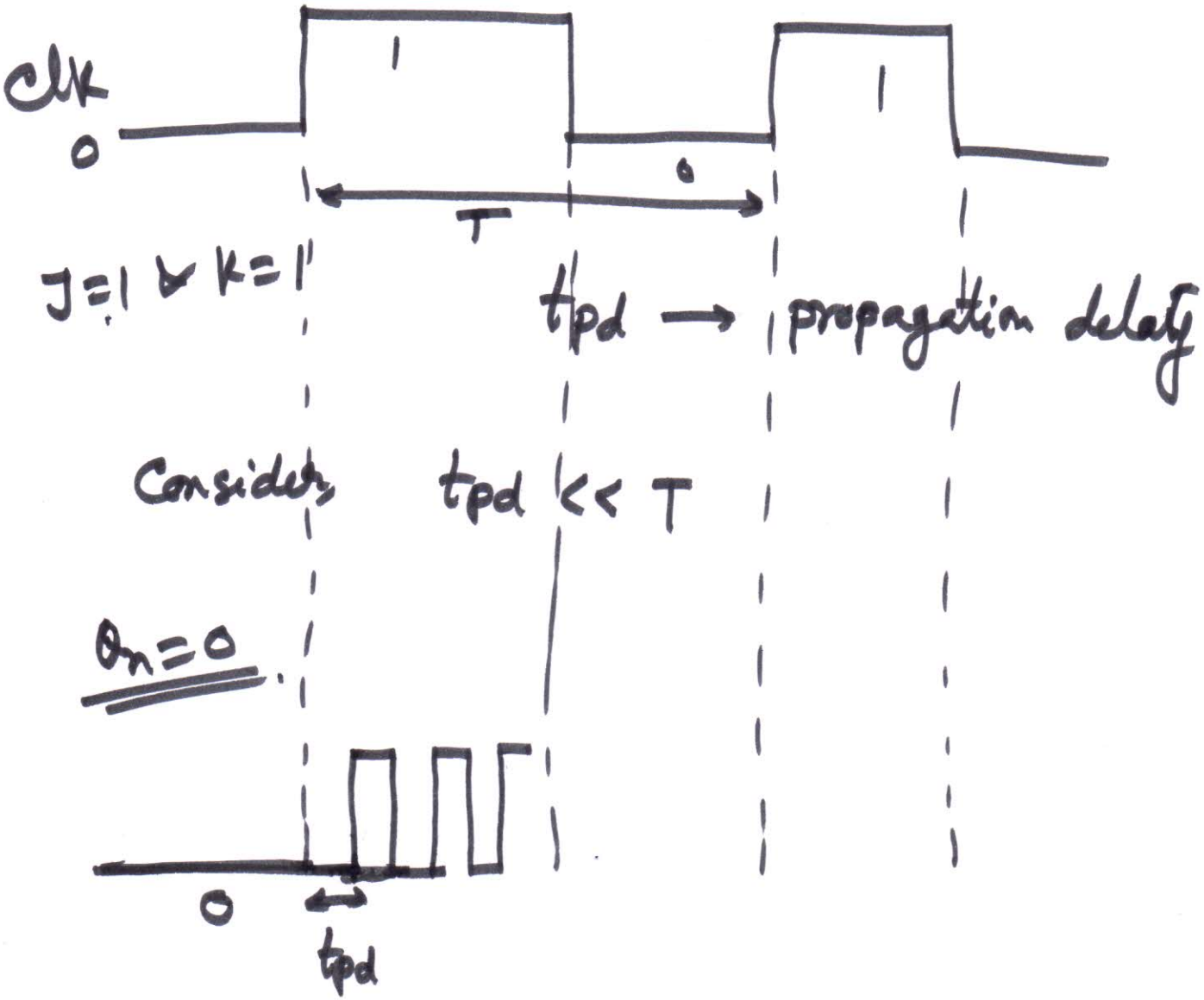
J=1 & K=1 & clk=1

Q_n	Q_{n+1}
0	1
1	0

$\Rightarrow Q_{n+1} = \overline{Q_n}$

(Toggle)

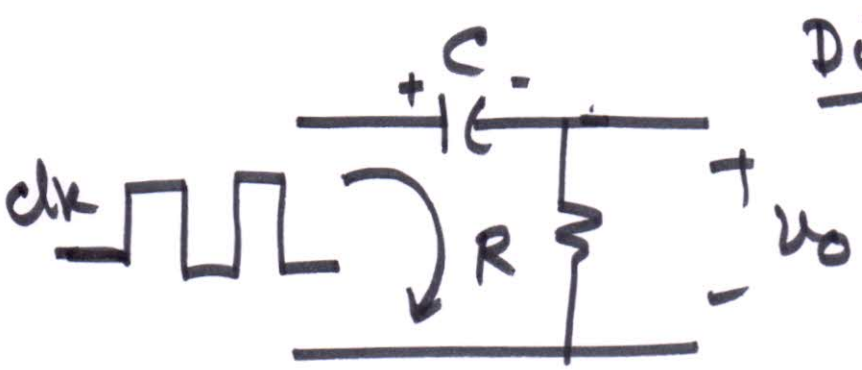
'Race Condition'



(1) Using Edge triggered clock

(2) Master- Slave Flip-Flop

Edge Triggering



Differentiator.

RC → very small