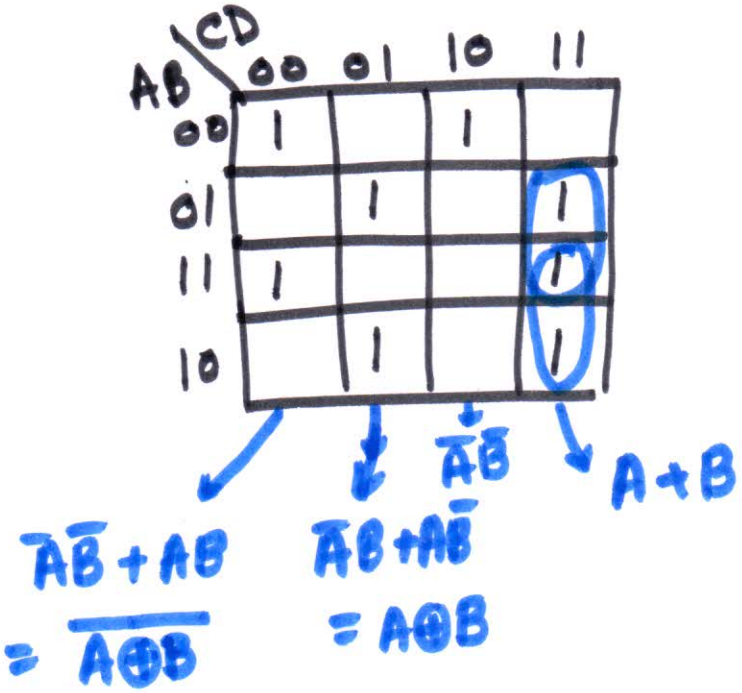
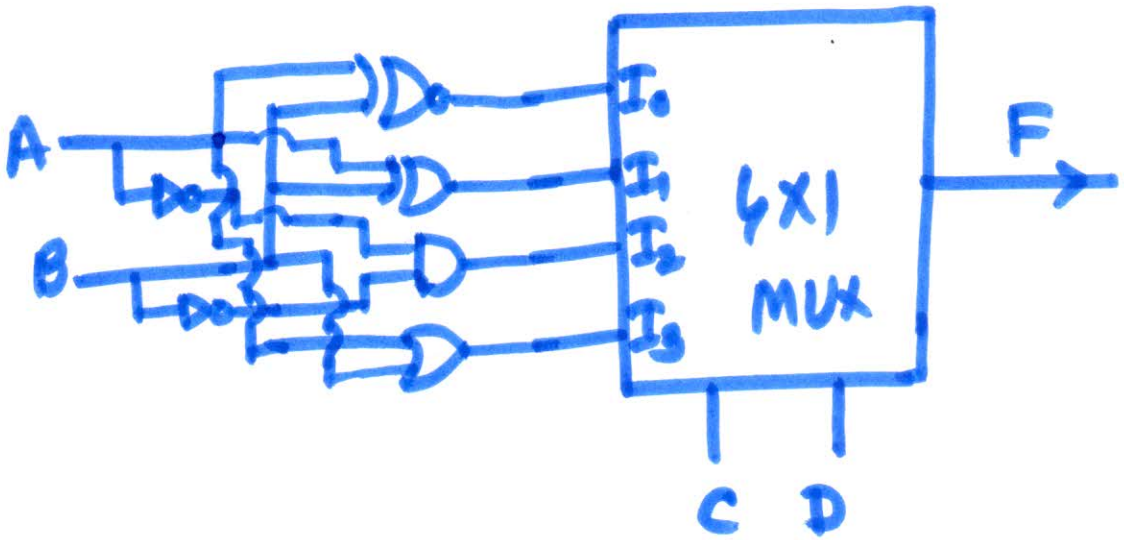
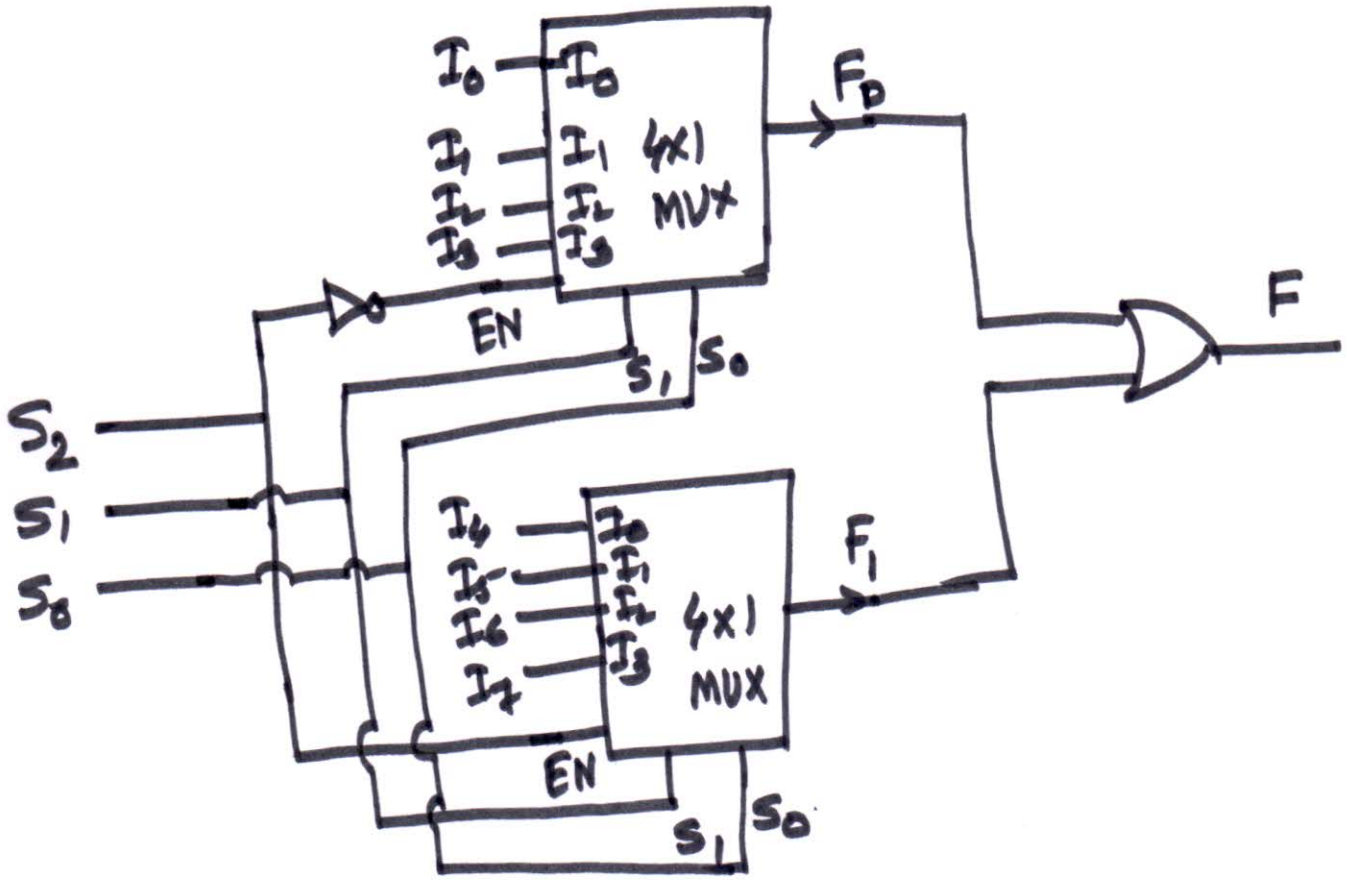
Ex. Implement $F(A, B, C, D) = \sum m(0, 2, 5, 7, 9, 11, 12, 15)$ using 4-to-1 MUX.



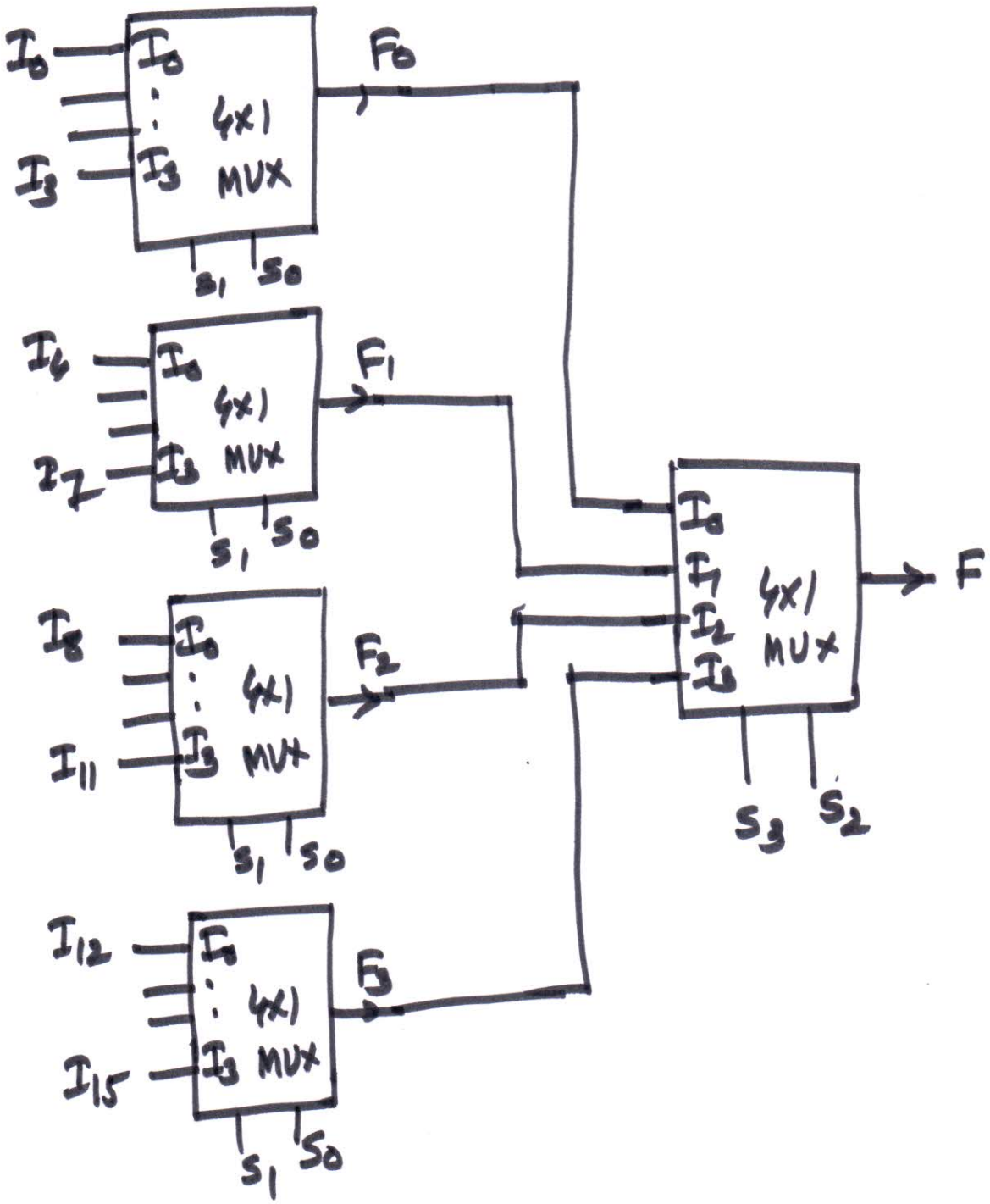


Design a 8-to-1 MUX using two 4-to-1 MUX:



S_2	S_1	S_0	F
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

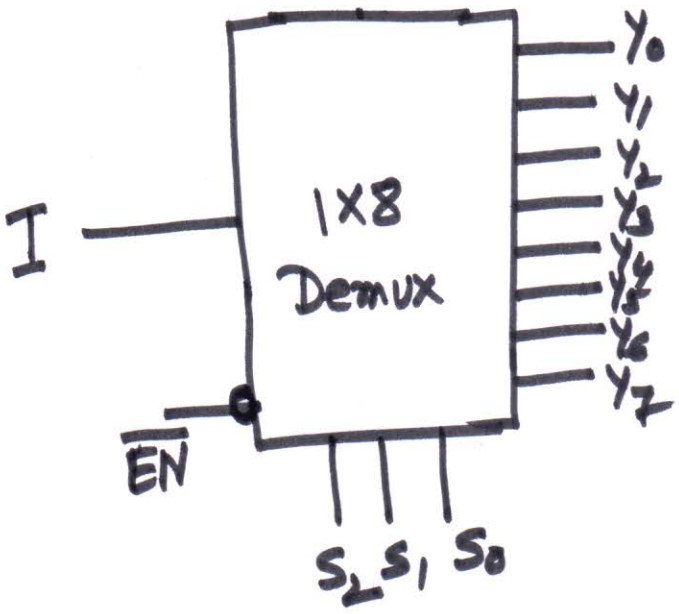
Design a 16-to-1 MUX using five 4-to-1 MUX:



Demultiplexers:

- A demultiplexer or DEMUX is a combinational circuit with one input line, more than one output line and more than one selection line.

1-to-8 Demultiplexer

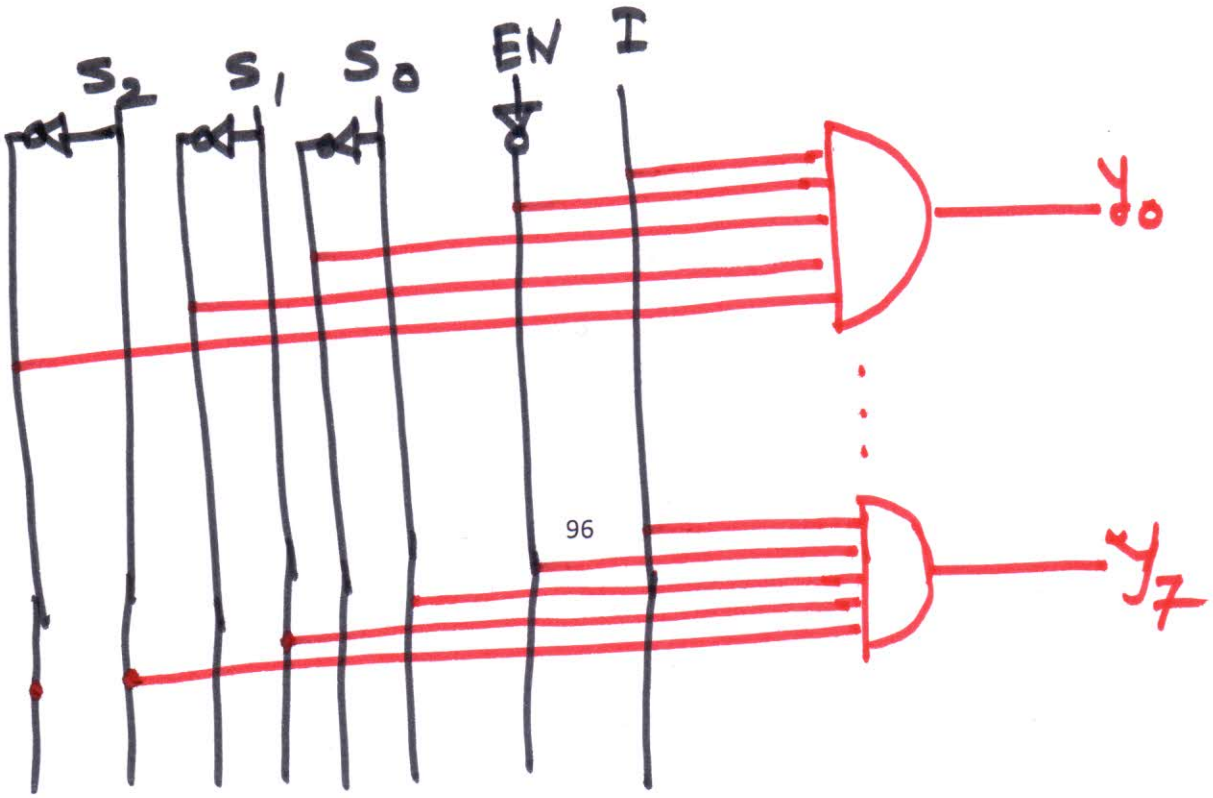


$$Y_0 = \overline{S_2}\,\overline{S_1}\,\overline{S_0}\,.\,\overline{EN}\,.\,I$$

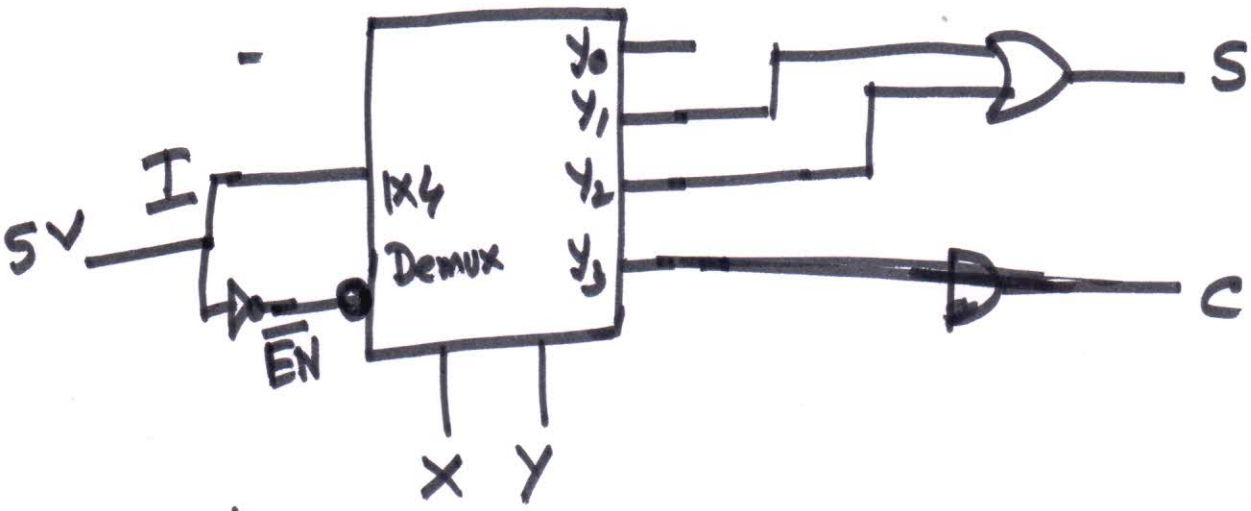
$$Y_1 = \overline{S_2}\,\overline{S_1}\,S_0\,.\,\overline{EN}\,.\,I$$

$$\vdots$$

$$Y_7 = S_2\,.\,S_1\,.\,S_0\,.\,\overline{EN}\,.\,I$$



Design a half-adder using 1-to-4 demultiplexer:



Half Adder

X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Encoder and Decoder