XPS_I2C_SLAVE_v1_10_a

User Manual v1.1

Introduction

XPS_I2C_SLAVE is a communication core to interface Xilinx Microblaze soft processor and a popular USB High Speed microcontroller Cypress CY7C68013A (also known as EzUSB FX2). The XPS_I2C_SLAVE supports Phillips® I2C communication between FPGA and FX2. The I2C serial communication frequency is high speed (400 kHz). The i2c_slave communication core was downloaded from http://www.mikrocontroller.net/attachment/23230/i2c_slave.vhd. Special thanks to the "FPGA-USER" for providing the core to the public.

The XPS_I2C_SLAVE has 6 32-bit registers: 3 for reading and 3 for writing. The transactions are usually 12 bytes long. When an FPGA writes a word to the first register an interrupt is triggered to the FX2. When an interrupt is triggered the FX2 automatically reads the programmed number of bytes (usually 12) from the XPS_I2C_SLAVE registers. When the FX2 writes all 12 bytes to the FPGA registers the microprocessor (Xilinx® Microblaze for example) receives an interrupt to know when the new data was received.

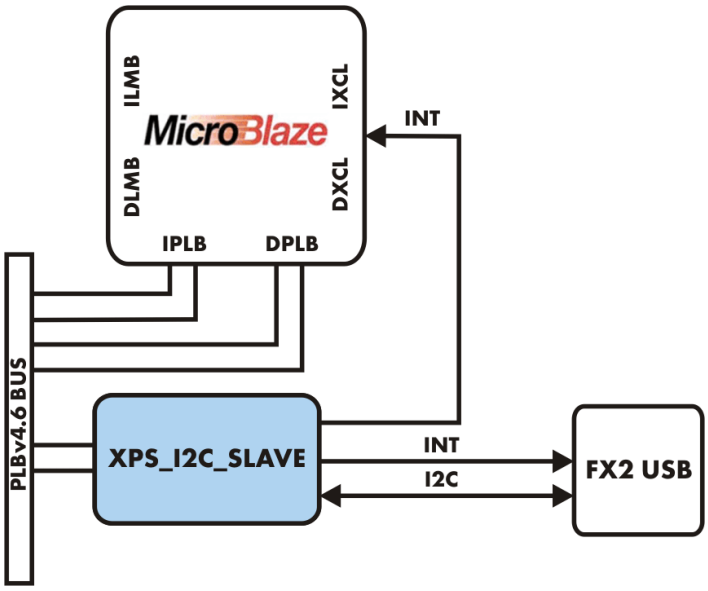


Figure 1: System integration block scheme.

Optomotive, mechatronika d.o.o., V Murglah 229, SI-1000 Ljubljana, Slovenia
+386 1 4292914 | info@optomotive.si | www.optomotive.si

The XPS_I2C_SLAVE has 2 bus interfaces:

- Slave Phillips® I2C bidirectional serial interface.
- Xilinx PLBv4.6 created with IPIF wizard for access to 6 32-bit registers.

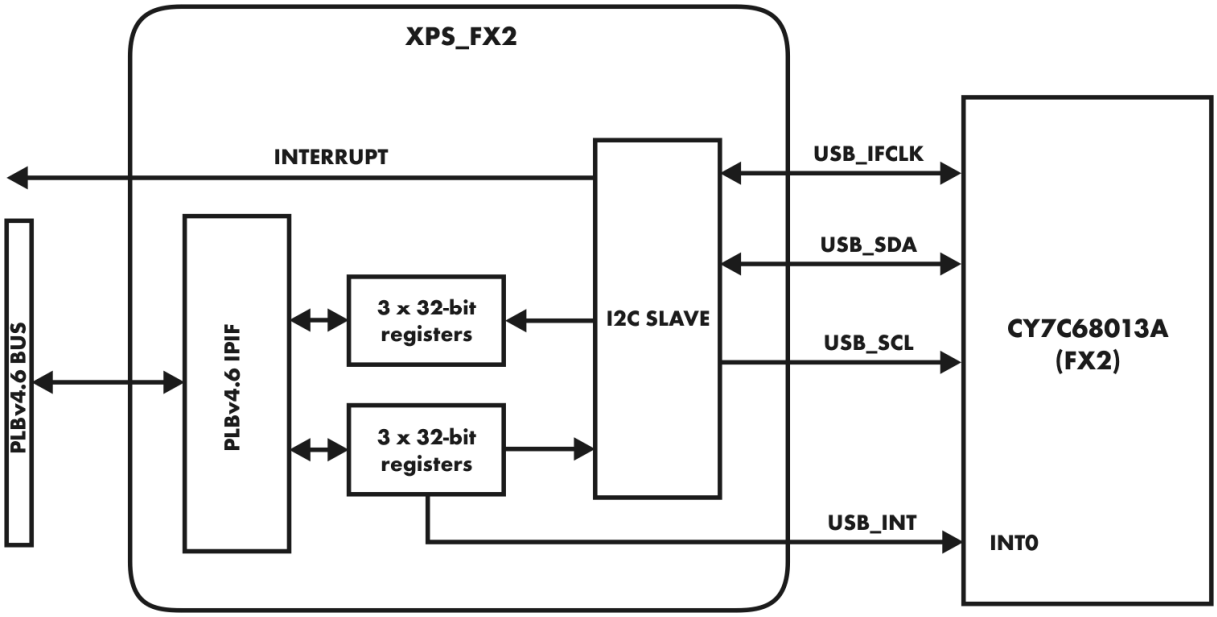


Figure 2: Peripheral internal structure block scheme.

XPS_I2C_SLAVE Core Design Parameters

Table 1: XPS_I2C_SLAVE Core Design Parameters

Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameters				
Target FPGA family	C_FAMILY	spartan3, spartan3e, spartan3a, spartan3adsp, spartan3an, virtex2p, virtex4, qvirtex4, qrvirtex4, virtex5	virtex5	string
PLB Parameters				
PLB base address	C_BASEADDR	Valid Address	None	std_logic_vector
PLB high address	C_HIGHADDR	Valid Address	None	std_logic_vector
PLB least significant address bus width	C_SPLB_AWIDTH	32	32	integer

PLB data width	C_SPLB_DWIDTH	32, 64, 128	32	integer
Shared bus topology	C_SPLB_P2P	0 = Shared bus topology	0	integer
PLB master ID bus Width	C_SPLB_MID_WIDTH	log2(C_SPLB_NUM_MASTERS) with a minimum value of 1	1	integer
Number of PLB masters	C_SPLB_NUM_MASTERS	1 - 16	1	integer
Width of the slave data bus	C_SPLB_NATIVE_DWIDTH	32	32	integer
Burst support	C_SPLB_SUPPORT_BURSTS	0 = No burst support	0	integer
XPS_I2C_SLAVE Parameters				
I2C slave address*	C_I2C_ADDRESS	0-127	63	integer
Number of bytes to trigger IP2INTC_Irpt**	C_MB_INT_BYTES	1-12	12	integer

Notes:

* C_I2C_ADDRESS must be set properly for an I2C_SLAVE to be recognized by FX2. Address 63 is used in all reference designs.

** C_MB_INT_BYTES can be less than 12 to speed up I2C communication by transferring less information. On the other hand since the USB latency is high overall speed would not be increased much.

XPS_I2C_SLAVE Core I/O Signals

Table 2: XPS_I2C_SLAVE I/O Signal Descriptions

Name	Interface	I/O	Initial State	Description
ChipScope[0:31]	-	O	-	Debug port
USB_IFCLK	-	I	-	USB 48MHz clock
USB_INT	-	O	0	USB Interrupt
USB_SCL	-	I	-	USB I2C serial clock
USB_SDA	-	I/O	-	USB I2C serial data
IP2INTC_Irpt	-	O	0	Processor interrupt
OTHERS ARE PLBv4.6 SIGNALS	PLBv4.6			

XPS_I2C_SLAVE Core Registers

XPS_I2C_SLAVE has a full access of a microprocessor to the core functionality through a 6 user 32-bit registers attached to PLBv4.6 bus.

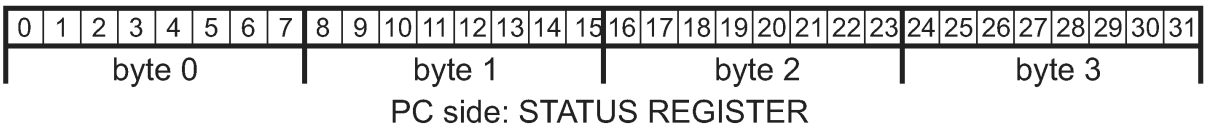
Table 3: XPS_I2C_SLAVE Core Registers

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
XPS FX2 IP Core Grouping				
C_BASEADDR + 00	MB2FX2_REG0	R/W	0x00000000	Microblaze to FX2 register 0
C_BASEADDR + 04	MB2FX2_REG1	R/W	0x00000000	Microblaze to FX2 register 1
C_BASEADDR + 08	MB2FX2_REG2	R/W	0x00000000	Microblaze to FX2 register 2
C_BASEADDR + 0C	FX2MB_REG0	Read	0x00000000	FX2 to Microblaze register 0
C_BASEADDR + 10	FX2MB_REG1	Read	0x00000000	FX2 to Microblaze register 1
C_BASEADDR + 14	FX2MB_REG2	Read	0x00000000	FX2 to Microblaze register 2

Details of XPS_I2C_SLAVE Core Registers

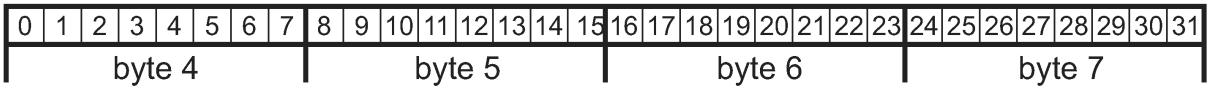
Microblaze to FX2 register 0 (MB2FX2_REG0)

A single beat write to this register triggers interrupt to FX2 (USB_INT).



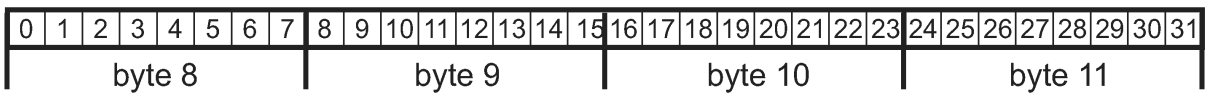
PC side: STATUS REGISTER

Microblaze to FX2 register 1 (MB2FX2_REG1)



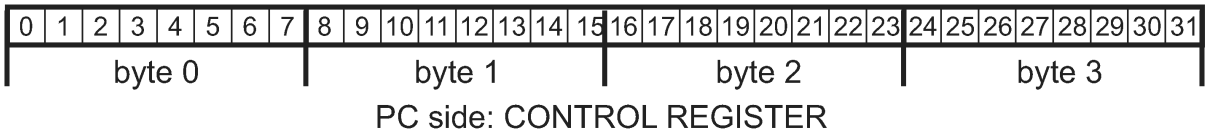
PC side: STATUS COMMAND

Microblaze to FX2 register 2 (MB2FX2_REG2)



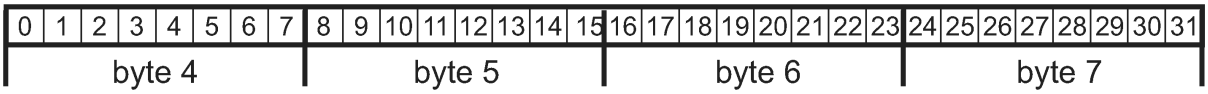
PC side: STATUS DATA

FX2 to Microblaze register 0 (FX2MB_REG0)



PC side: CONTROL REGISTER

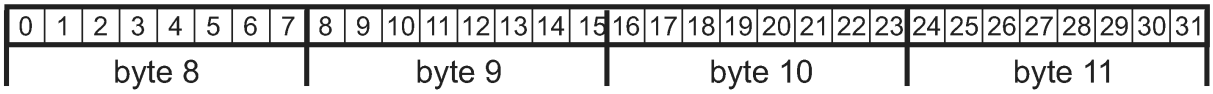
FX2 to Microblaze register 1 (FX2MB_REG1)



PC side: CONTROL COMMAND

FX2 to Microblaze register 2 (FX2MB_REG2)

When FX2 puts a last byte to this register an interrupt is triggered to microprocessor (IP2INTC_Irpt) if C_MB_INT_BYTES is set to 12.



PC side: CONTROL DATA

Programming model

When the microprocessor (Microblaze) receives an interrupt it should read all FX2MB_REGs for new instructions.
When a microprocessor wants to send information to the PC then it should write MB2FX2_REGs. We recommend that the last write is to MB2FX2_REG0 since it triggers USB_INT. When the USB_INT is triggered the FX2 automatically reads all registers (or a programmed number of bytes). The PC polls FX2 for interrupt data and USB_INT status bit. This way a safe bidirectional communication between the FPGA microprocessor and PC is possible.

For using the software header read comments in:
#project#(or IP reposit.)\drivers\XPS_I2C_SLAVE_v1_00_a\src\XPS_I2C_SLAVE.h

Revision history

Rev	Date	Author	Description
1.0	15.8.2009	AG	created
1.1	30.6.2010	AG	Updated to Xilinx tools v11

Optomotive, mechatronika d.o.o., V Murglah 229, SI-1000 Ljubljana, Slovenia
+386 1 4292914 | info@optomotive.si | www.optomotive.si