

Vision Transformer Accelerator ASIC for In-Ear
Sleep Staging

by
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Supervisor: Professor Xilin Liu
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B.A.Sc. Thesis



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Abstract

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Keywords: Sleep staging, ASIC accelerator, vision transformer, computer architecture

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List of Abbreviations

ASIC Application-Specific Integrated Circuit

CMOS Complimentary Metal Oxide Semiconductor

CiM Compute-in-Memory

HDL Hardware Description Language

MAC Multitply-Accumulate

IP Intellectual Property

TSMC Taiwan Semiconductor Manufacturing Company

VCD Value Change Dump

See [1]. I am making an Application-Specific Integrated Circuit (ASIC). It's small, low-power and fast. It's better than Google's.

1 Introduction

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2 Background

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3 How to Design an AI Accelerator

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3.1 Model Prototyping

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3.2 Accelerator Functional Simulation

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3.3 Accelerator Hardware Implementation

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4 Vision Transformer Model Design

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5 ASIC Accelerator Architecture

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5.1 Centralized vs. Distributed Architecture

5.2 Master Architecture

5.3 Data and Control Bus

5.4 Compute-in-Memory: Fixed-Point Accuracy

5.5 Compute-in-Memory: Memory

5.6 Compute-in-Memory: Compute Modules

This section describes the design and performance metrics of the various compute Intellectual Property (IP) modules use by the Compute-in-Memory (CiM) modules. Each is custom-designed for this project. Each module works with signed (2's complement) fixed-point representation. To avoid overflow, the modules use internal temporary variables of fixed-point format Q22.10. Table I shows the performance metrics of the compute modules. The working principles of each modules is described briefly in subsequent sections.

Table I: Performance metrics of the compute modules

Module	Area	Cycle/op	Energy/op	Leakage power	F_{max}
Adder	450.4 μm^2	1	0.99pJ	11.87 μW	6.67GHz
Multiplier	3535.2 μm^2	1	7.05pJ	90.50 μW	1.59GHz
Divider	1719.9 μm^2	35	23.44pJ	34.56 μW	1.11GHz
Exponential	2442.2 μm^2	24	62.73pJ	47.10 μW	7.14GHz
Square Root	1325.2 μm^2	17	18.32pJ	26.30 μW	0.758GHz
MAC ¹	—	386	820.20pJ	—	—
MAC ²	3129.8 μm^2	391	839.32pJ	69.40 μW	2.17GHz
MAC ³	—	456	941.68pJ	—	—
Softmax	2341.1 μm^2	2024	1972.5pJ	51.47 μW	1.20GHz
LayerNorm	3836.89 μm^2	1469+494	1705.7pJ	78.39 μW	0.877GHz
Total	18780.69 μm^2	N/A	N/A	409.59 μW	0.758GHz

¹ No activation function applied

² Linear activation function applied

³ Swish activation function applied

Note that all measurement in Table I are given for standard 65nm Taiwan Semiconductor Manufacturing Company (TSMC) process with a 100MHz clock. To determine these metrics, the following methodology was used with Synopsys Design Compiler 2017.09 running on UofT's EECG cluster:

- Area: Synthesis with the area optimization effort set to `high`, and the area was extracted from the `report_area` command report.

- **Cycle/op:** The latency was observed when running a single operation on a pre-synthesis simulation.
- **Energy/op:** A single-instance testbench running 10000 operations was designed, and a `.saif` file was generated from the Value Change Dump (VCD) dump file of the testbench using Synopsys' `vcd2saif` utility. This provides an average activity factor for each node, yielding an accuracy that is adequate for this discussion. The energy per operation was calculated by multiplying the total dynamic power by the time to complete the 10000 operations, divided by 10000.
- **Leakage current:** Synthesis with the power optimization effort set to `high`, and the leakage power was extracted from the `report_area` command report.
- F_{max} : The `report_timing` command was used to determine the maximum frequency of the design.

It must be noted that the measurements for all composite compute units (i.e. units that make use of shared resources) *exclude* the area/power/etc. of the shared resources. Including them would result in misleadingly high figures, given that they are explicitly designed to share resources. The total area of the CiM provides figures more representative of this integration.

5.6.1 Adder

The adder is a single-cycle, combinational module that adds two fixed-point numbers. It uses a ripple-carry adder architecture. The adder has a latency of 1 cycle, which simplifies the logic that uses it. It also provides an overflow flag. To reduce dynamic power consumption, the adder only updates its output when the `refresh` signal is high.

5.6.2 Multiplier

The multiplier is very similar to the adder. One difference is that it uses Gaussian rounding (also known as banker's rounding). This rounding method rounds 0.5 to the nearest even number. This reduces the bias in the output that is commonly observed with standard rounding methods, which is particularly important in MAC operations where the error can accumulate. The multiplier also has a latency of 1 cycle and provides an overflow flag. Like the adder, the multiplier only updates its output when the `refresh` signal is high.

5.6.3 Divider

The divider is more complicated than the adder and multiplier. It performs bit-wise long-division and has a latency of $N + Q + 3$ cycles, where N is the number of integer bits

and Q is the number of fractional bits. The divider also provides flags for overflow and divide-by-zero and done/busy status signals. The module start division on an active-high pulse of the **start** signal and provides the result when the **done** signal is high. The divider module is mostly used in the MAC module during computation of the Swish activation function.

5.6.4 Exponential

The exponential module computes the exponential e^x of a fixed-point number x . It uses a combination of the identities of exponential and a Taylor series approximation around zero to compute the exponential. Specifically, the module transforms the exponential as such:

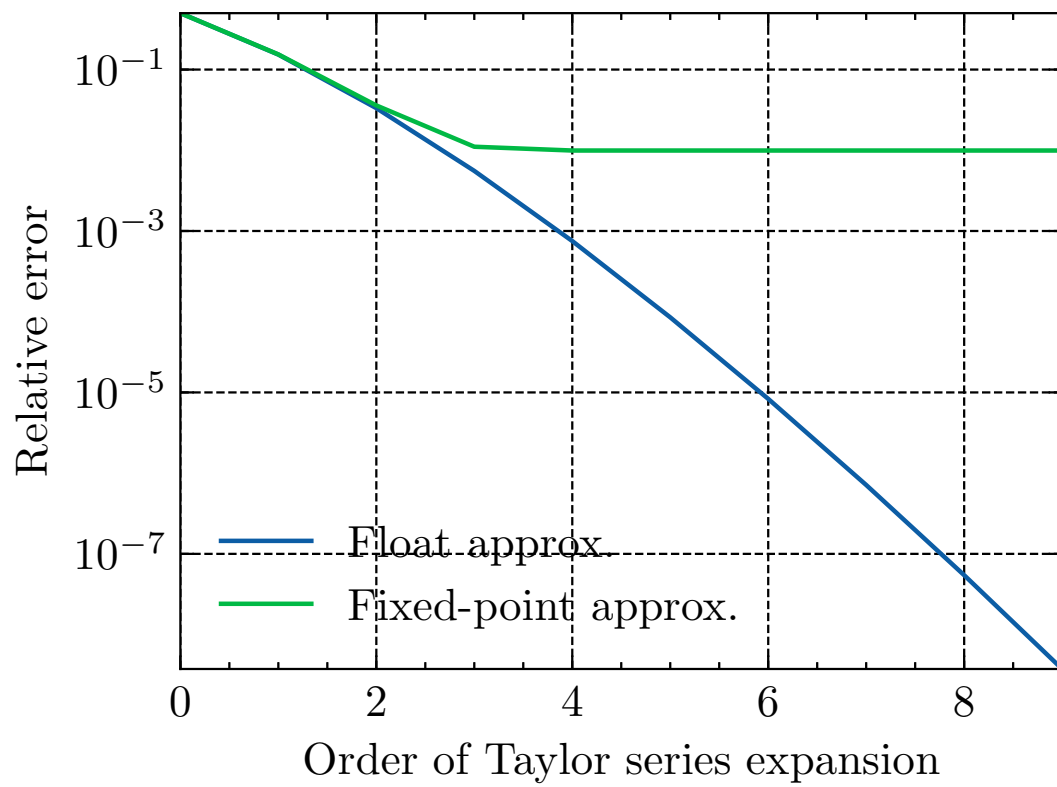
$$e^x = 2^{\frac{x}{\ln(e)}} = 2^z = 2^{\lfloor z \rfloor} 2^{z - \lfloor z \rfloor} \quad (1)$$

The compute can then easily compute $2^{\lfloor z \rfloor}$ as an inexpensive bit-shift operation and $2^{z - \lfloor z \rfloor}$ as a Taylor series approximation. To determine a reasonable number of terms to use for the Taylor series expansion, an accuracy study was ran. Figure 5.6.4 shows the relative error of the exponential module as a function of the order of the Taylor series expansion for both fixed-point (Q22.10) approximation and float (64b) approximation. As can be seen, the error decreases with an increase in the order of the expansion. However, for the fixed-point approximation, it converges to a minimum error of $\tilde{0.992}\%$. This is because the quantization of fixed-point dominates the Taylor series error. Therefore, using a 3rd order Taylor series expansion to approximate the exponential function is a good balance between accuracy and latency/energy. Note that these error was measured over the input range of $[-4, 4]$. According to the functional simulation, this corresponds to roughly ± 3 standard deviations from the mean of inputs to the exponential function. To further speed up the computation, the exponential module uses a lookup table to store the Taylor series coefficients as well as $1/\ln(e)$. To reduce area, the exponential module does not instantiate its own adder and multiplier modules. Rather, it accesses the adder and multiplier modules in the CiM module shared with other compute units. The latency is 24 cycles.

5.6.5 Square Root

The square root module computes the square root of a fixed-point number using an iterative algorithm. It has a latency of $(N+Q)//2+1$ cycles, where $//$ denotes integer division. The module provides flags for overflow and negative radicand and start/busy/done signals. The module starts computation on an active-high pulse of the **start** signal and provides the result when the **done** signal is high.

Figure 1: Error of exponential approximation as a function of Taylor series expansion order



5.6.6 Multiply-Accumulate

The MAC module performs a vector dot-product for a given pair of base addresses for the data and length of the vector and applies a selectable activation function to the result. Similar to the exponential module, it uses shared adder, multiplier, divider and exponential modules in the CiM module. It can implement three activation functions: none, linear and Swish. For a nominal length of 64 (which corresponds to the embedding depth of the model, a very common value for matrix dimensions in the model) and Q22.10 formate, the latencies are 386, 391 and 456, respectively. Note that, although the Swish activation function comprises a divider operation, the MAC compute latency can still be kept fairly short because the divisor is the same for all elements. The module can thus perform the division once and multiply by the inverse, which is a single-cycle operation. Finally, the MAC module can be directed to choose the second vector from weights or intermediate results memory.

5.6.7 Softmax

The softmax module computes the softmax function of a vector of fixed-point numbers. Similarly to the MAC module, it uses shared adder, mulitplier, divider and exponential modules and provides **busy** and **done** signals. For a 64-element Q22.10 vector, the latency is 2024 cycles. This is significantly longer than other vector compute modules such as the MAC because, in the softmax operation, each element is exponantiated individually.

5.6.8 LayerNorm

The final compute module is the LayerNorm module. It computes the Layer Normalization of a vector of fixed-point numbers. As described in section 4, the LayerNorm operation consists of a normalization of the vector on the horizontal dimension followed by scaling and shifting using learnable parameters on the vertical dimension. Because each CiM module stores one vector at a time, the LayerNorm operation must be separated into two stages with a matrix transpose broadcast between the two. The latency for the first half is 1469 cycles and the latency for the second half is 494 cycles. The module provides **busy** and **done** signals and is controlled with a **half-select** and **start** pulse signals. Because the length of the vector is constrained to be a power of two, the module uses bit-shifting instead of division for the normalization operation to decrease latency and energy per operation.

5.7 A Note About Software-Hardware Co-Design

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6 Evaluation of Performance Metrics

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6.1 Vision Transformer

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6.2 Accelerator

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7 Future Work

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8 Conclusion

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References

- [1] Xilin Liu and Andrew G Richardson. “Edge deep learning for neural implants: a case study of seizure detection and prediction”. In: *Journal of Neural Engineering* 18.4 (2021), p. 046034.

A Codebase Statistics

It may be interesting to the reader to appreciate the size of the codebase needed to develop a project of similar scale. The code for this project is available in my GitHub repository. The following table provides a breakdown of the number of lines of code in the project.

Table II: Line and file count per file type in the codebase

File type	File count	Line count	Percent of total
Python	12	3000	33.7%
SystemVerilog	12	2500	30.4%
C++	12	1250	18.9%
TeX	12	670	8.2%
Shell	12	300	4.3%
Other	12	20	4.5%
Total	60	13,000	100%

In addition, there have been 200 commits to the repository.

B Reflection on Learnings and Experience Gained

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