Analog CMOS Integrated Circuit Design Cheat Sheet

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Model of MOS Transistors

Process parameters (n,V_{TH},KP, V_E):

$$t_{OX} = \frac{L_{min}}{50} \tag{1}$$

$$t_{si} = \sqrt{\frac{2\epsilon_{si}(\Phi - V_{BD})}{qN_B}} \tag{2}$$

$$C_{OX} = \frac{\epsilon_{OX}}{t_{OX}} \tag{3}$$

$$C_D = \frac{\epsilon_{si}}{t_{si}} \tag{4}$$

$$KP = \mu C_{OX} \tag{5}$$

$$\beta = KP\frac{W}{L} \tag{6}$$

$$V_{TH} = V_{TH0} + \gamma[\sqrt{|2\Phi_F| + V_{BS}} - \sqrt{||2\Phi_F|}] \tag{7}$$

$$n = \frac{\gamma}{\sqrt{|2\Phi_F| + V_B S}} = 1 + \frac{C_D}{C_{OX}} \tag{8}$$

Channel-Length Modulation:

$$\frac{1}{2}KP\frac{W}{L}(V - V_{TH})^2(1 + \lambda V_{DS}) \tag{9}$$

Value Examples In $0.35\mu m$ Process Nodes

Names	Symbols	Values
dielectric constant of sub-silicon	ϵ_{si}	1 pF/cm
dielectric constant of gate-oxide	ϵ_{OX}	0.34 pF/cm
electron charge	q	1.6×10^{-19} C
minium channel length	L_{min}	$0.35\mu m$
width of gate-oxide capacitor	t_{OX}	0.1μm
width of sub-silicon capacitor	t_{si}	7nm