

Unit 2 BJT

Biasing of Transistor

1) Operating point

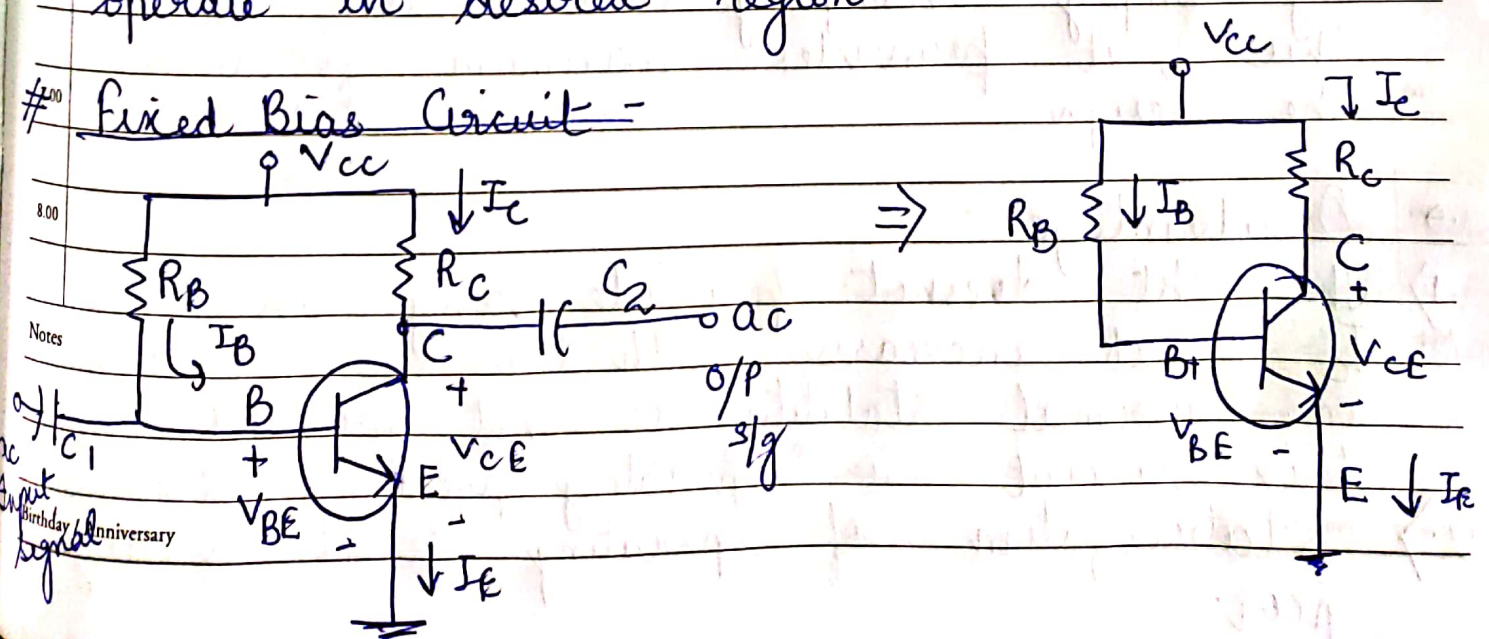
Region of operation.	Emitter base J_{em}^n	Collector base J_{em}^n
Cut off	R B	R B
Active	F B	R B
Saturation	F B	F B

→ When we bias a t/s, we establish a certain current & voltage conditions for the t/s. These conditions are known as d.c. operating point or quiescent point.

2) Need for biasing BJT.

In order to have amplification property, we need proper supply of external d.c. biasing of correct polarity and magnitude of the t/s to operate in desired region.

Fixed Bias Circuit -



13

Analysis -

September 2018

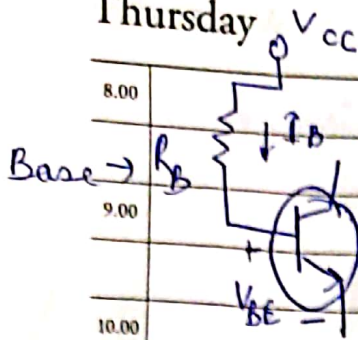
Week 37

Day 256 • 109

Date 13 • 09 • 2018

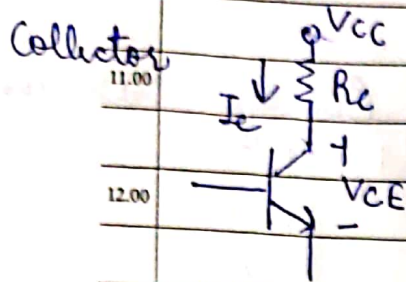
Thursday

SEP'18	M	T	W	T	F	S	S
3	4	5	6	7	8	1	2
10	11	12	13	14	15	8	9
17	18	19	20	21	22	15	16
24	25	26	27	28	29	22	23
						29	30



$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \beta I_B$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

→ Base current is controlled by the value of R_B and I_C is related to I_B by a constant β , the magnitude of I_C is not a function of the resistance R_C .

→ Advantages of a fixed biased Circuits -
1) Simple circuit which uses very few components.

2) The operating point can be fixed anywhere in the active region of the characteristics by simply changing the value of R_B . Thus, it provides maximum flexibility in the design.

Disadvantage -

1) The ckt doesnot provide any check on the I_C which increases with the rise in temperature i.e. thermal stability is not provided by this circuit. So "Operating point is not maintained".
2) Stabilization of operating point is very poor.

	M	T	W	T	F	S	S
OCT '18	1	2	3	4	5	6	7
	8	9	10	11	12	13	14
	15	16	17	18	19	20	21
	22	23	24	25	26	27	28
	29	30	31				

September 2018

Week 37

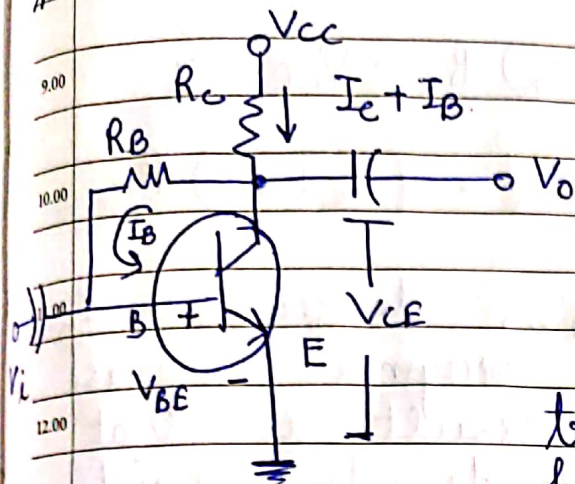
Day 257 • 108

Date 14 • 09 • 2018

14

Friday

Collector to Base bias circuit -



• Voltage feedback as shown in the diagram.

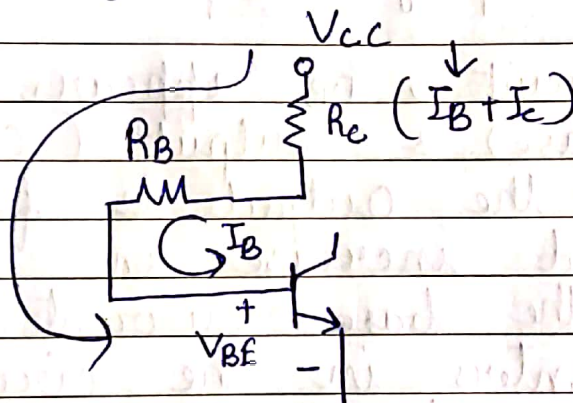
• Improvement over fixed bias circuit.

• Biasing resistor is connected b/w Collector & base of the transistor to provide a feedback path.

Thus I_B flows through R_B & $(I_B + I_C)$ flows through the R_C .

Analysis:

Base Circuit →



$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$

The only difference between the equation for I_B and that obtained for the fixed bias is the term βR_C . Thus, we can say that feedback path results in a reflection of resistance R_C to the input circuit.

15

Saturday

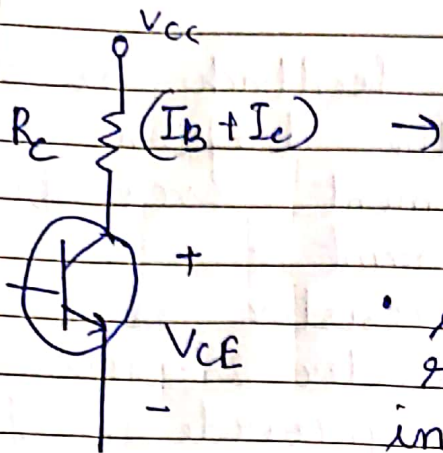
September 2018

Week 37

Day 258 • 107

Date 15 • 09 • 2018

	M	T	W	T	F	S	S
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	10	11	12	13	14	8	9
	17	18	19	20	21	15	16
	24	25	26	27	28	22	23
					29	29	30

Collector Circuit -

$$V_{CC} - (I_E + I_B) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_E + I_B) R_C$$

As $I_C \propto I_B$, decrease in I_B reduces the original increase in I_C . The result is that the circuit tends to maintain a stable value of Collector current keeping Q point fixed.

In this circuit, R_C appears directly across input (base) & output (collector). A part of the output is feedback to the input and increase in collector current decreases the base current. Thus, negative feedback enters in the circuit, so this circuit is also called Voltage feedback bias circuit.

Notes

Birthday / Anniversary

	M	T	W	T	F	S	S
OCT '18	1	2	3	4	5	6	7
	8	9	10	11	12	13	14
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September 2018

Week 37

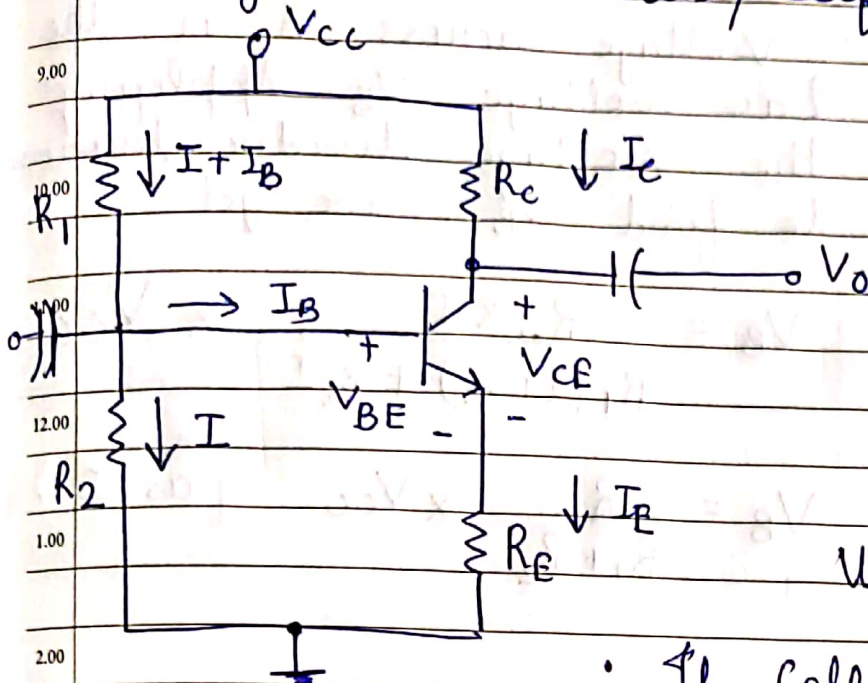
Day 259 • 106

Date 16 • 09 • 2018

16

Sunday

Voltage Divider Bias / Self Bias Circuit -



• Biasing is provided by three resistors R_1 , R_2 and R_E .

• R_1 , R_2 act as a potential divider / Voltage divider giving a fixed voltage to base.

• If Collector current increases due to change in temperature or change in β , the emitter current I_E also increases & voltage drop across R_E rises, reducing the voltage difference between base & emitter (V_{BE}).

• As V_{BE} is reduced, base current I_B & I_E also reduces \rightarrow hence negative feedback exists in the emitter base bias circuit.

Circuit Analysis -

Notes

Birthday / Anniversary

17

Monday

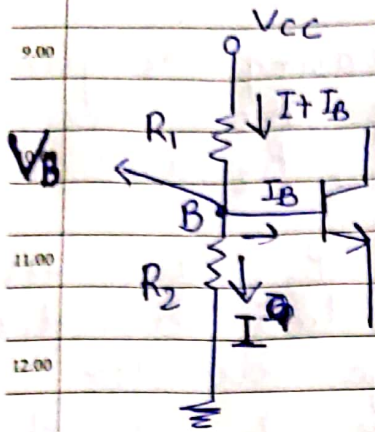
September 2018

Week 38

Day 260 • 105

Date 17 • 09 • 2018

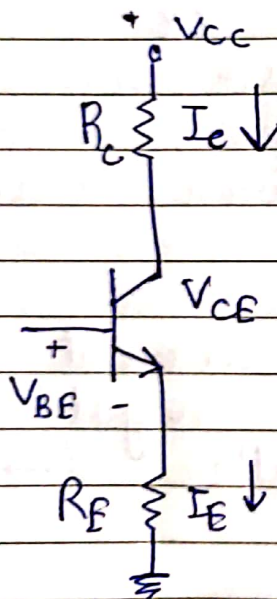
	M	T	W	T	F	S	S
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						29	30

Base Circuit -

Voltage across R_2 is the base voltage V_B . Applying the voltage divider theorem to find V_B , we get

$$V_B = \frac{R_2 \times I}{R_1(I+I_B) + R_2 I} \times V_{CC}$$

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC} \quad (\text{as } I \gg I_B)$$

Collector Circuit

Since, Voltage across R_E (V_E)

$$V_E = I_E R_E = V_B - V_{BE}$$

$$\text{as } (V_{BE} = V_B - V_E)$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

Applying KVL to collector

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Notes Advantage -

- Stability factor S for this bias is less as compared to other biasing circuit.
- More stable & hence commonly used.

Birthday / Anniversary

OCT 18
M T W T F S S
1 2 3 4 5 6 7
8 9 10 11 12 13 14
15 16 17 18 19 20 21
22 23 24 25 26 27 28
29 30 31

September 2018

Week 38

Day 261 • 104

Date 18 • 09 • 2018

18

Tuesday

Comparison of Biasing circuit -

Parameter	Fixed Bias	Collector to Base Bias	Self Bias / Voltage divider
1) Resistors required	1	1	3
2) Stability provided	Poor	Medium	More
3) Simplicity of the circuit	More	More	Less
4) Feedback provided	No	Negative (Voltage Shunt)	Negative (Current Series)

Notes

Birthday / Anniversary