Tutorial - IV

I- Define CPU registers, Main memory, secondary memory, and cache memory ?.

Register - A processor register (CPU register) is one of a small set of data holding places that are part of the computer processor. A register may hold an instruction, a storage address or any kind of data (such as a bit sequence or individual characters). some instruction specify registers as part of the instruction.

Main Memory :- The main memory can not store a vast amount of data. The data stored in main memory is temporary. The data will be lost it they are disconnected from the power supply. Store the input data and immediate calculation result ex- RAM.

Secondary Memory :- secondary memory used to store data permanently for future use. The data is safe even when their power is failure.
Ex- Hard disk.

Cache Memory :- cache memory refers to high speed memory. It is small but faster than RAM (the main memory). The CPU can access the cache comparatively more quickly than its primary memory thus we use it to synchronize with a high-speed CPU and also to improve overall performance.

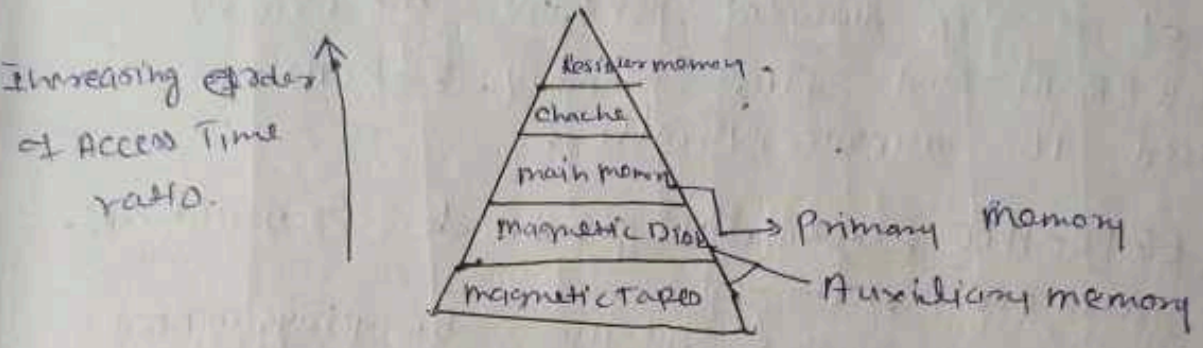
2- Differentiate valatile and non-valatile memory organisation.

Valatile memory	Non-valatile memory
- It is a temporary type of computer memory that stores data and information only until it gets a continous power supply	- It is permanent type of computer memory that stores retains the data even after a user turns the system off.
- The valatile memory stores data of those programs that the CPU is processing in real time. A system stores all the frequently used information and data in the devices valatile memory	- The non-valatile memory stores data from the basic booting process of any computer system BIOS it stores all the type of data and media that need to exist for a longer time or permanently on the computer
- The valatile memory ~~is the~~ does not effect a system performance. A higher amount of storage space for chache RAM and other valatile memory increases the efficiency of a computer system.	- Non-valtile memory also affects system's performance as storage. A higher amount of storage space lets a user save more data permanently thus the system runs comparitively smoother
Ex- chache RAM	ex- ROM, flash memory.

3- what is the necessity of multilevel memory? further explain the memory hierarchy used in computer systems.

A CPU should have rapid, uninterrupted access to its external memories to operate at or near at its maximum speed but memories that operate at speed near to that of CPU are expensive. That's why different level of memories is used in terms of performance and costs.

Memory Hierachy in computer system Design is an enhancement that helps in organising the memory so that it can actualy minimise the access time. The development of the memory Hierarchy accured on a behaviours of program known as locality of refrences. Henry's



(4) Defferentiate between the different types of ROMs. ?

MROM :- (Masked read-only memory) → we Khows that ROM is as old as semiconductor technology MRom was the very first ROM that consist of grid of word lines and bit lines joined together transistor switches. This type of Rom data is physically encoded in the circuit and only be programmed during fabrication of it was not so expensive.

PROM (Programmable read-only memory):.
PROM is a form of digital memory. Each bit is locked by a fuse or anti-fuse. The data stored in it are permanently stored and cannot be changed or erasable. It is used in low-level programs such as firmware or microcode.

3- EPROM (Erasable programmable read only memory): It is a type of PROM but it can be reprogrammed. The data stored in EPROM can be erased and reprogrammed again by Ultraviolet light. Reprogrammed of it is limited. Before the era of EEPROM and flash memory, EPROM was used in microcontrollers.

4- EEPROM (Electrically erasable programmable read only memory)
As its name refers, it can be programmed and erased electrically. The data and program of this ROM can be erased and programmed about ten thousand times. The duration of erasing and programming of the EEPROM is near about 4ms to 10ms. It is used in microcontrollers and remote keyless systems.

5- Explain about ROM and PROM in detail.
ROM stands for Read-only memory. It is non-volatile memory that is used to store important information which is used to operate the system. As its name refers to read only memory we can only read the programs and data stored on it. It is also primary memory unit. It is also known as permanent.

PROM :- The data stored in PROM is permanently, can not be changed and erased.
- A Bipolar transistor is used in PROM
- PROM is more flexible.
- PROM is used in low level programs such as firmware or microcode.

Q-6 Define Random Access Memory and types of RAMs Present

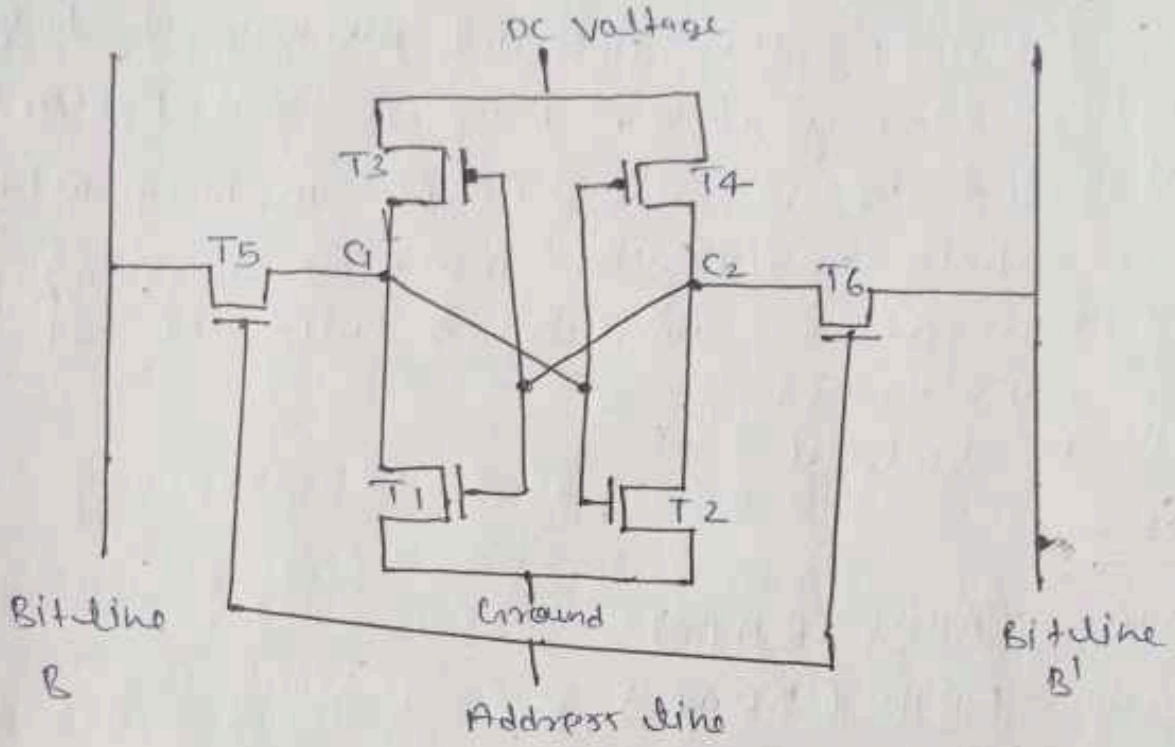
RAM:- RAM is the internal memory of the CPU for storing data, Program and Program result. It is a read / write memory which store data until the machine is working. As soon as the machine is switched off data is erased.
RAM is volatil.

Types:-
Static RAM (SRAM)
Dynamic RAM (DRAM).

Q-7 Differentiate Between SRAM and DRAM.

SRAM	DRAM
- It can store data as long as electricity is available.	- It saves data for as long as the power is on or for a few moments if the power is turned off.
- SRAM has a storage capacity of 1MB to 16MB in most cases	- DRAM which is often found in tablets and smartphones has a capacity of 1GB to 2GB.
- SRAM is more expensive than DRAM	- DRAM is less expensive than SRAM.
- It is comparatively faster	- It is comparatively slower.
- SRAM is used in cache memory	- DRAM is used in main memory.

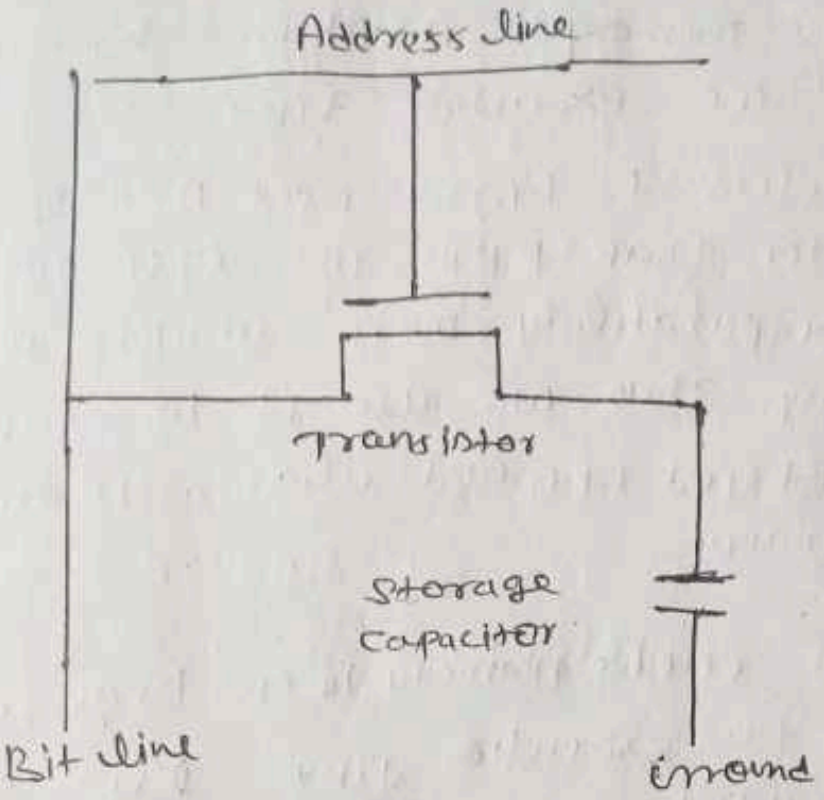
8- Draw and explain the operation of basic SRAM and DRAM cell.:



Static RAM Cell

To generate stable logic state, four transistors T1, T2, T3, T4 are organized in cross-connected way for generating logic state 1; node C1 is high and C2 is low. in this state T1 and T4 are off and T2 and T3 are on for logic state 0 Junction C1 is low and C2 is high in the given state T1 and T4 are on and T2 and T3 are off. Both states are stable until the dc voltage is applied

The SRAM address line is operated for opening and closing the switch and it to control the T5 and T6 transistors, permitted to read and write.



Dynamic RAM cell.

At the time of reading and writing the bit value from the cell the address line is activated. The transistor present in the circuitry behaves as a switch that is closed (allowing current to flow) if a voltage is applied to the address line and open (no current flows) if no voltage is applied to the address line. for the write operation, a voltage signal is employed to bit line where high voltage shows 1 and low voltage indicate 0. A signal is then used to the address line which enables transferring of the charge to the capacitor.

(9) Define Cache memory? Explain how is used to reduce the execution Time.

Cache memory refers to high-speed memory. It is small but faster than RAM. The CPU can access the cache comparatively more quickly than its primary memory. Thus we use it to synchronize with high speed CPU and also to improve its overall performance.

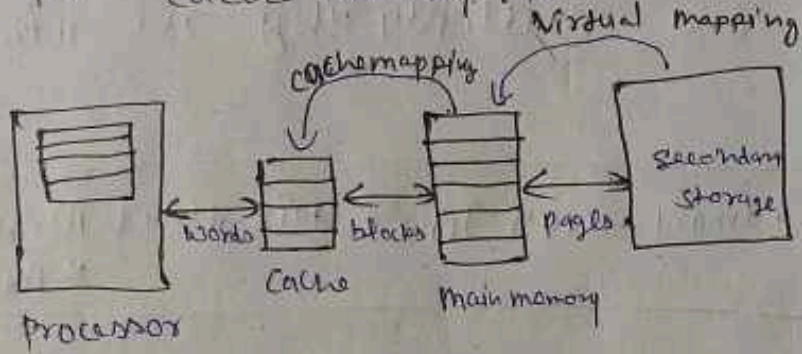
We know that cache memory is a high seed ram it decreases the execution time by storing the most frequent and most probable data and instruction "closer" to the processor. Where the systems CPU can quickly get it.

(10) Differentiate Virtual memory and cache memory

Cache memory	Virtual memory
- cache memory increases CPU access speed	- Virtual memory increase main memory capacity.
- cache memory is a memory unit and is very fast to access	- virtual memory is a technique and involves hard disk and is slower to access.
- cache memory is small in size	- size of virtual memory is much larger than cache memory.
- cache memory keeps recently used data.	- Virtual memory keeps the program which are not getting accomodated in main memory.
- CPU and related hardwares manages Chache memory	- operating system manages virtual memory.

Q-11 - Explain the mapping procedures adopted in the organization of a chache memory?

The process of cache mapping help us define how a certain block that is present in the main memory gets mapped to the memory of a cache in the case any cache miss
In simpler words cache mapping refers to a technique using which we bring the main memory into the cache memory.



- the main memory gets divided into multiple partition of equal size, know as the frame or blocks.
- cache memory actually divided into various partition of the same size as that blocks.
- The main memory block is copied simply to the cache during the process of cache mapping.

Q-12 Define HIT ratio, MISS ratio and Memory Access Time in memory with an example.

HIT Ratio:- A hit ratio is a calculation of chache hits and comparing them with how many total content request were recieved.

$$\text{Hit ratio} = \frac{\#\text{ of chache hits}}{\#\text{ of cache hits} + \#\text{ of chache misses}}$$

$$\text{Hit ratio} = 1 - \text{miss ratio}$$

Miss ratio:- A miss ratio is the flip side of this where the cache misses are calculated and compared with the total no. of content requests that were recieved.

$$\text{Miss ratio} = \frac{\#\text{ of cache miss}}{\#\text{ of content request}}$$

or

$$\text{Miss ratio} = 1 - \text{Hit ratio}$$

Memory access Time:- To calculate memory access time add the hit time and miss ratio and multiply it by the miss penalty.

Average memory access Time = Hit time + Miss ratio × Miss penalty

(13) Consider a 2-level memory hierarchy consisting of a cache memory M1 and M2. Suppose that the cache is 6-times faster than the main memory and the cache can be used 90% of the time How much efficiency and speedup do we gain by using the cache.

Since cache memory is 6x faster than main memory. Let the cache memory access time be $t/6$ units therefore the main memory access time will be t units

Now speedup gain = $\frac{\text{time without use of cache}}{\text{time with use of cache speedup}}$

$$= \frac{t}{\left[0.9 \times \frac{t}{6} + 0.1 \times t\right]}$$

speed up gain = 4

(14) Describe the virtual memory organization and explain in detail?

Virtual memory is a memory management technique where secondary memory can be used as if it were a part of the main memory. Virtual memory uses both hardware and software to enable a computer to compensate for physical memory shortages temporarily transferring data from RAM to disk storage. Mapping chunks of memory to disk files enables a computer to treat secondary memory as though it were main memory.

(15) Explain the following.

(a) Virtual or logical address?

A logical address is generated by CPU while a program is running. Since a logical address does not physically exists it is also known as a virtual address. This address is used as a reference by the CPU to access the actual physical memory location.

(b) Memory management unit (MMU)?

A memory management unit (MMU) is a computer hardware component that handles all memory and caching operations associated with the processor. MMU is responsible for all aspects of memory management. It's usually integrated into the processor although in some systems.

(c) Translation lookaside buffer (TLB) -

A translation lookaside Buffer (TLB) is a memory cache that store the recent translations of virtual memory to physical memory. It is used to reduce the time taken to access a user memory location.