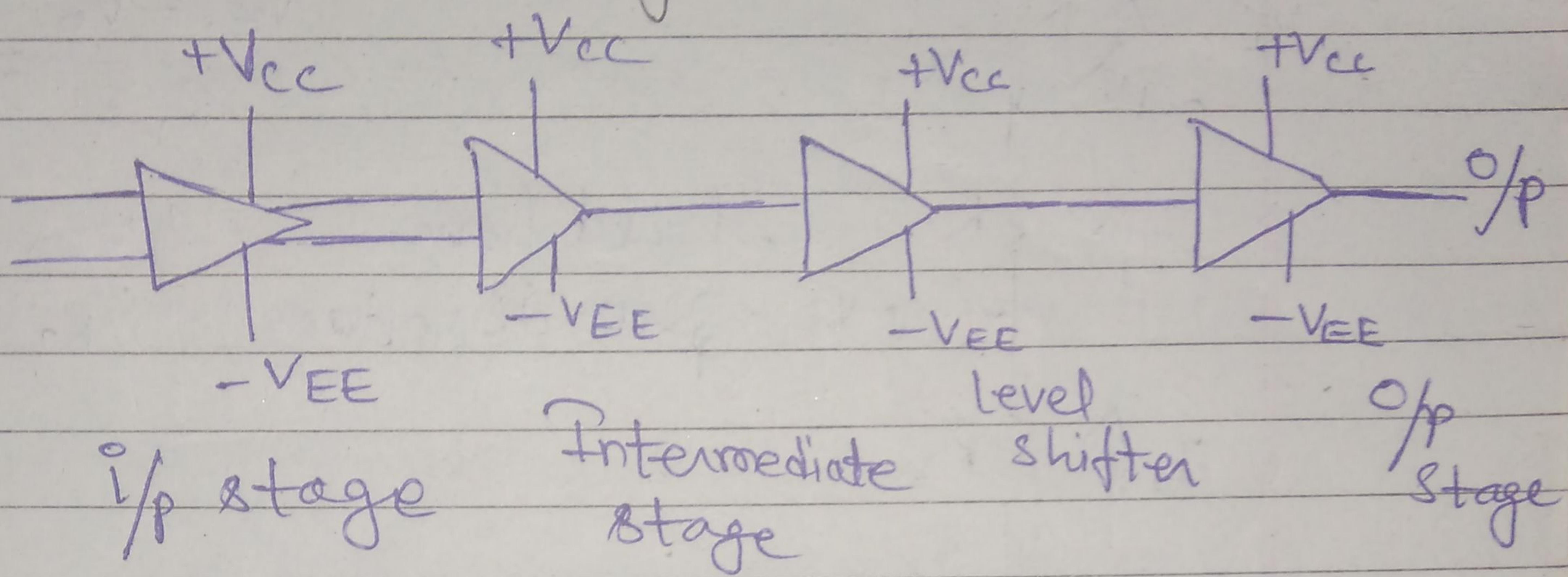


Unit 1-

Functional Diagram of Op-Amp.



Input stage - is dual i/p balanced o/p differential amplifier which provide high i/p resistance and high gain

~~Intermediate~~ Stage - is dual input unbalanced o/p differential amplifier. It increases voltage gain further. Unbalanced o/p contain DC also which will affect the operation of power Amp. and may also distort the final o/p. This DC term is removed by level shifter.

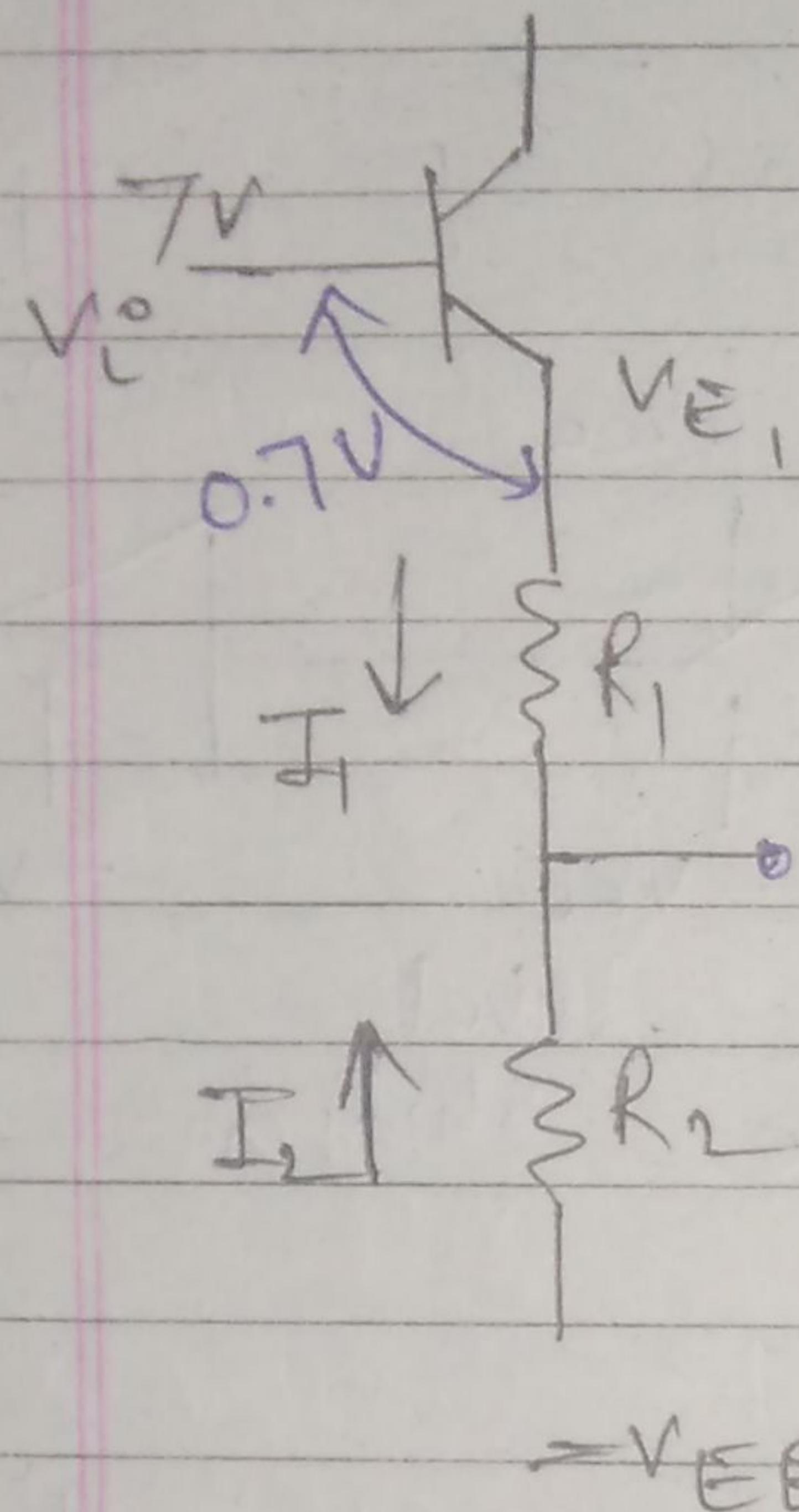
Level Shifter - is common collector or emitter resistance which can eliminate DC present at the o/p of internal stage

Output stage

O/p stage has complementary symmetric

pushpull amplifier

class B fruitful o/p



$$I_1 + I_2 = 0 \Rightarrow I_1 = -I_2$$

$$\frac{V_{E1} - V_o}{R_1} = - \left[\frac{V_{EE} - V_b}{R_2} \right]$$

Should have

$$R_1 = - \frac{V_{E1}}{V_{EE}}$$

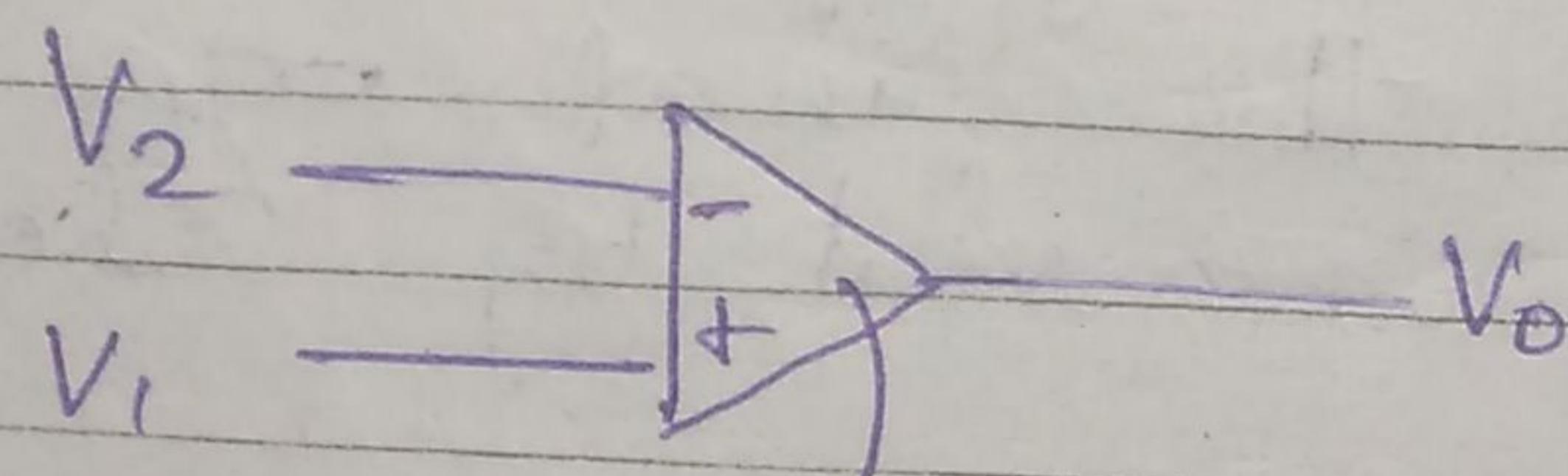
zero dc voltage

$$R_2 = - \frac{V_{E2}}{V_{EE}}$$

It provides power amplification, so that op-amp can drive any type of load. It is also responsible for low o/p resistance of op-amp.

Characteristics of ideal op-amp.

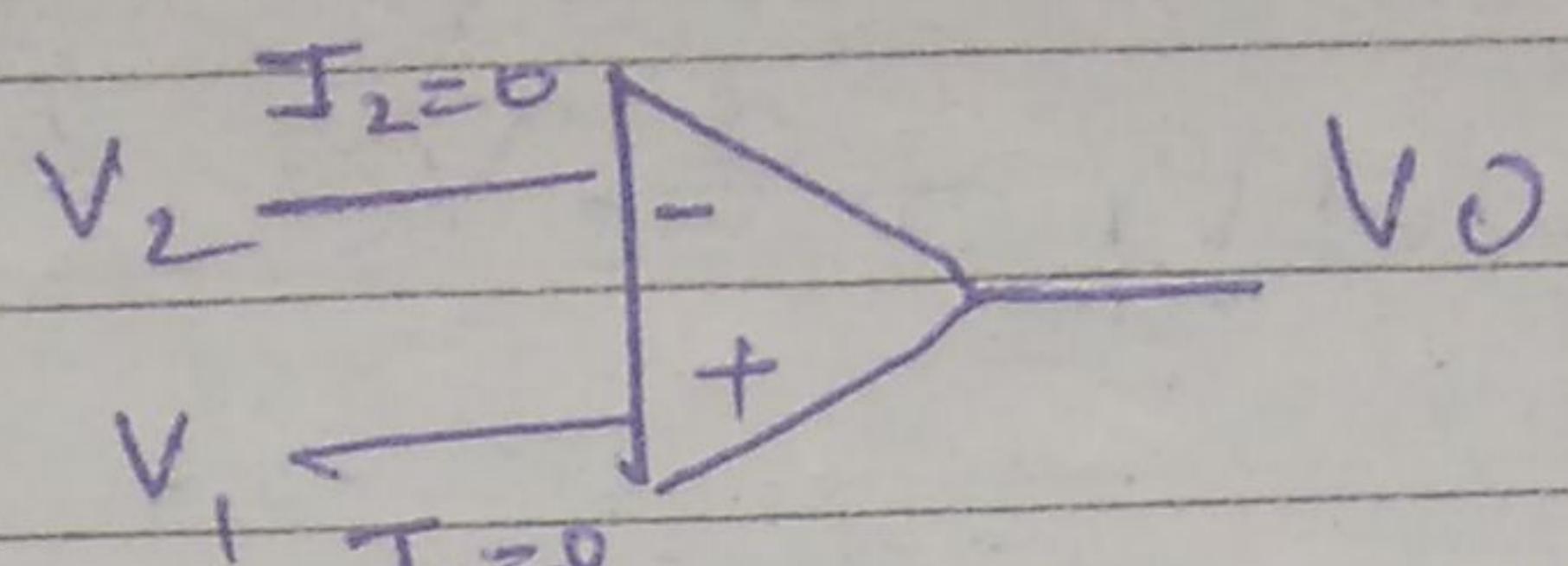
(i) infinite open loop gain, $A_{OL} = \infty$



$$A_{OL} = \frac{V_o}{V_1 - V_2}$$

An op-amp should have infinite gain so that it can amplify even smaller possible voltage difference.

(ii) Infinite input resistance $R_i = \infty$

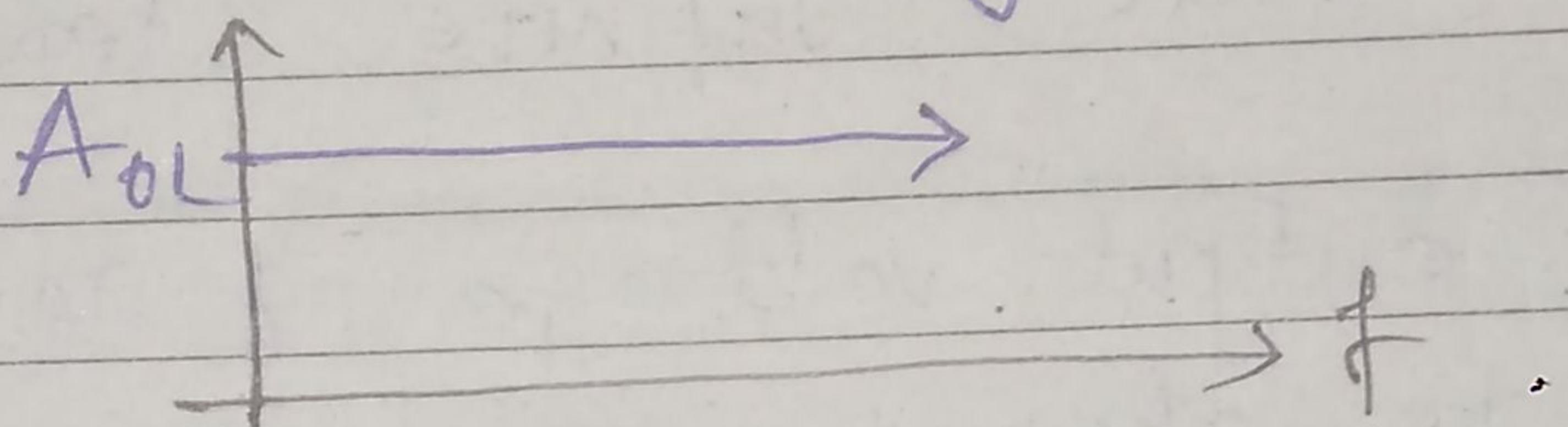


An ideal op-amp should draw zero current from source.

(iii) zero output resistance $R_o = 0$

(iv) Band width - Infinite bandwidth

It should amplify all frequency equally.



(v) Zero offset

zero offset means zero output for zero input.

(vi) Common mode rejection ratio (CMRR)

$$V_1 \text{ & } V_2 : V_d = V_2 - V_1$$

$$V_o = A_d V_d + A_c A_e$$

$$\text{CMRR} = \left| \frac{A_d}{A_c} \right| = \frac{\text{difference signal gain}}{\text{common gain}}$$

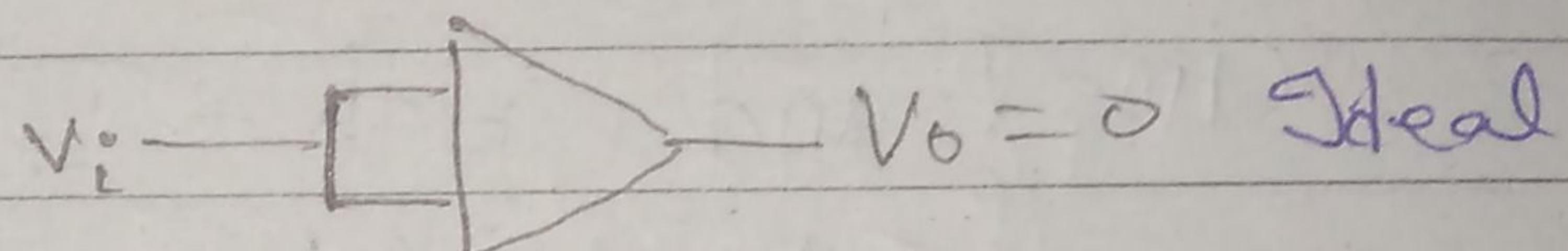
→ op-amp should only amplify difference signal. And it should reject common signal.
i.e. $A_c = 0$ in case of ideal op-amp

$$\text{or } \boxed{\text{CMRR} = \infty}$$

but in practical op-amp output depend also on common mode voltage gain.

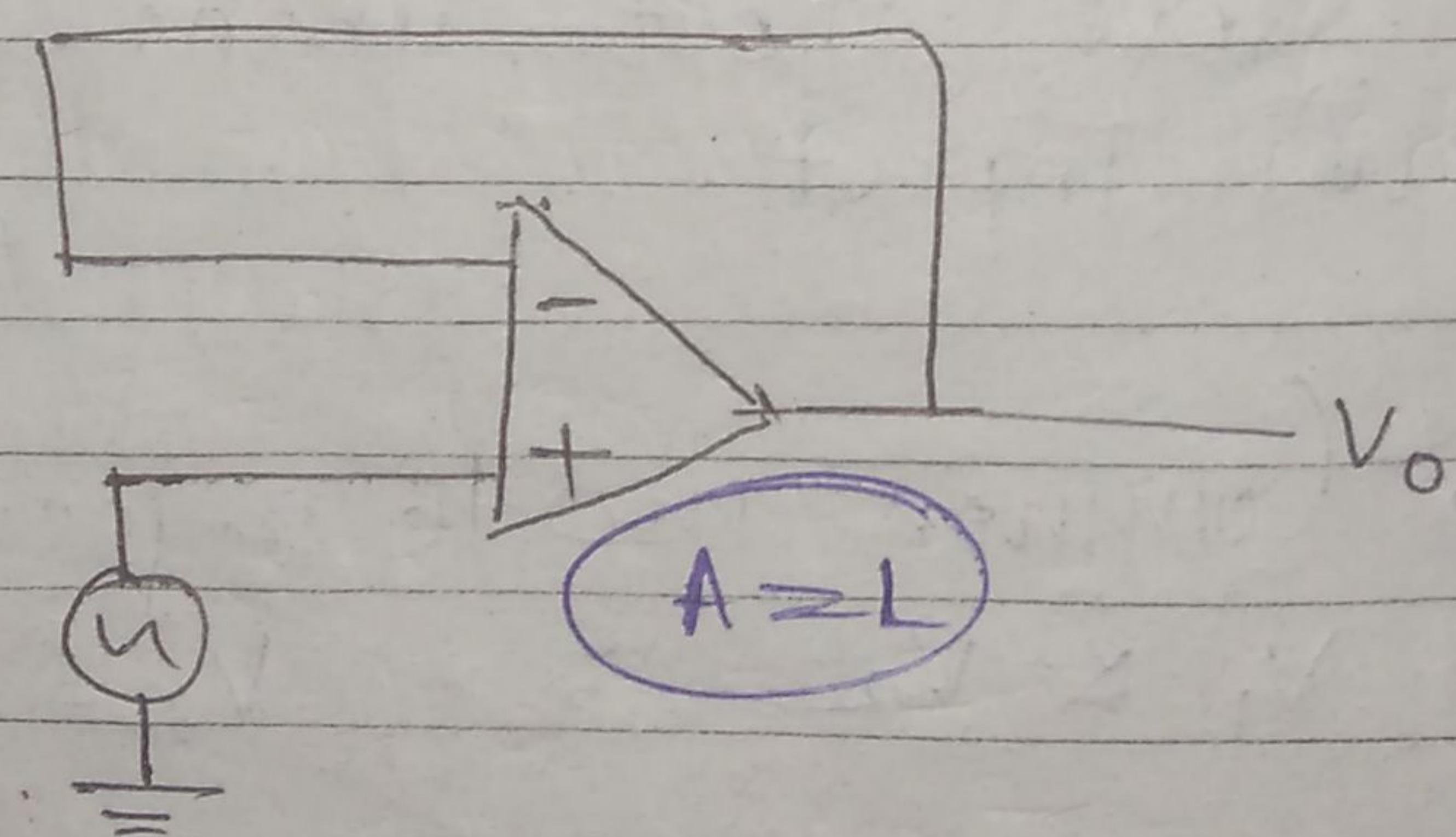
$$V_o = A_d V_d + \textcircled{A_c V_c} \neq 0$$

- for ideal op-amp, output should not depend on common mode voltage
- CMRR is measure of ability of op-amp to reject the voltage which is common to both input.



vii) Slew rate - Infinite slew rate.

The output voltage of op-amp should be able to change instantaneously in respond to change in input, only then op-amp produce undistorted output.



It is maximum rate of change of output voltage, it is the measure of how fast op-amp can change the output in respond to the change in input.

$$S.R = \left(\frac{dV_o}{dt} \right)_{\max}$$

Slew rate is calculated under unity gain condn. ($A=1$).

let $V_i = V_p \sin \omega t$

$V_o = V_i = V_p \sin \omega t$ (\because unity gain)

$$\frac{dV_o}{dt} = V_p \omega_0 \cos \omega_0 t$$

$$SR = \left. \frac{dV_o}{dt} \right|_{\text{max}} = V_p \omega_0 \cos \omega_0 t \Big|_{\text{max}}$$

$$SR = V_p \omega_0 = 2\pi V_p f_0 \text{ volt/sec}$$

Unit of SR \rightarrow volt/ μ sec.

$$\Rightarrow SR = \frac{2\pi V_p f_0}{10^6} \text{ volt}/\mu\text{sec}$$

\rightarrow Under Nat in unity gain,

$$V_o = A V_i$$

$$SR = \frac{2\pi V_p f_0 A}{10^6} \text{ volt}/\mu\text{sec}$$

Ques Op-amp has slew rate of $1\text{V}/\mu\text{sec}$. if the peak input voltage is 10V . Then find the max. input signal frequency for which output remains undistorted.

$$SR = 1\text{V}/\mu\text{sec} \quad \left. \begin{array}{l} \\ \end{array} \right\} \text{for unity gain}$$

$$V_p = 10\text{V}$$

$$\text{As we know that, } SR = \frac{2\pi V_p f_0}{10^6}$$

$$L = \frac{2\pi f \times 10}{10^5}$$

$$f_0 = \frac{10^5}{2\pi} = \frac{10^5 \times 3.5}{22} = 1.6 \times 10^4 \text{ Hz}$$

Ques In the above given problem if the input signal frequency is 20 kHz then find the maximum allowed peak input voltage such that output is undistorted.

$$S.R = L \quad f_0 = 20 \times 10^3$$

$$\Rightarrow L = \frac{2\pi \times 20 \times 10^3 \times 1}{10^5} \text{ Vs}$$

$$N_p = \frac{100}{4\pi} = \frac{25}{\pi}$$

Ques In an op-amp close loop gain is 40dB if slew rate of op-amp is 0.5V/msec. and input signal frequency is 10kHz then find the maximum allowed peak input voltage.

$$A = 40 \text{ dB}$$

$$20 \log(A) = 40$$

$$\log_{10} A = 2$$

$$A = 10^2$$

$$A = 100$$

$$(\log_n m = p)$$

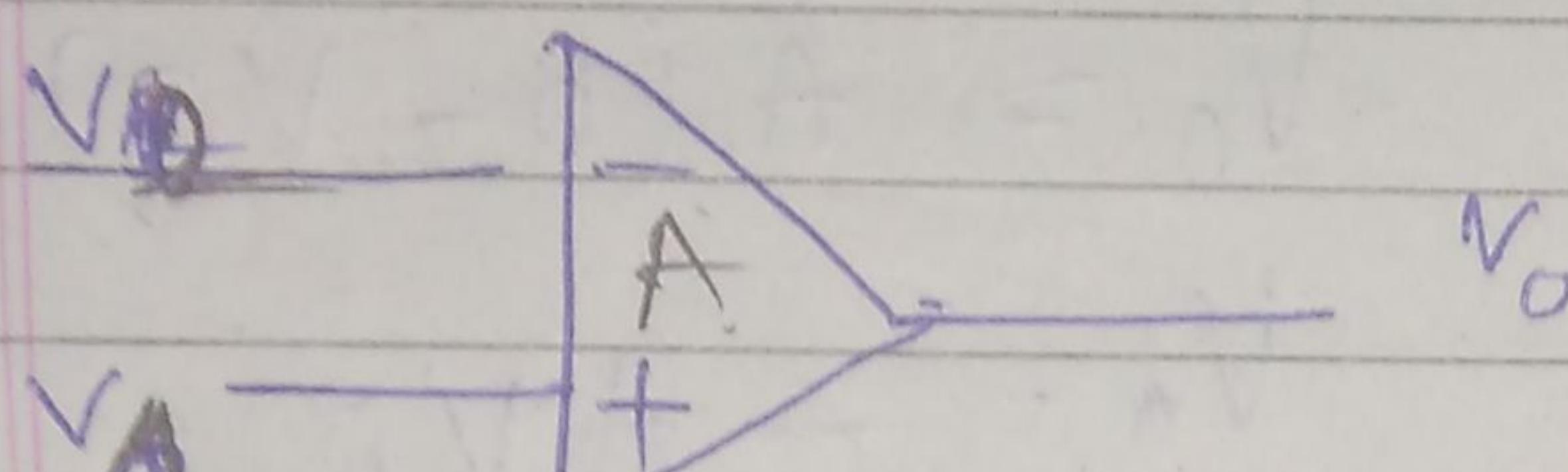
$$\Rightarrow m = n^p$$

$$S.R = \frac{2\pi f_0 V_p \times A}{10^6}$$

$$0.5 = \frac{2\pi \times 10 \times 10^3 \times V_p \times 100}{10^6}$$

$$V_f = \frac{0.5}{2k} = \frac{0.25}{+}$$

Open-loop opp^n of Op-amp | Closed loop opp^n of Op-amp



$$V_0 = A(V_1 - V_2)$$

① $V_2 > V_1$; $V_0 = +V_{sat}$

② $V_2 < V_1$; $V_0 = -V_{sat}$

-ve feedback +ve feedback

① Clipper ① Schmitt

② Amplifier trigger

② waveform

③ Rectifier generator

④ All mathm-③ Oscillator

-atical

operations

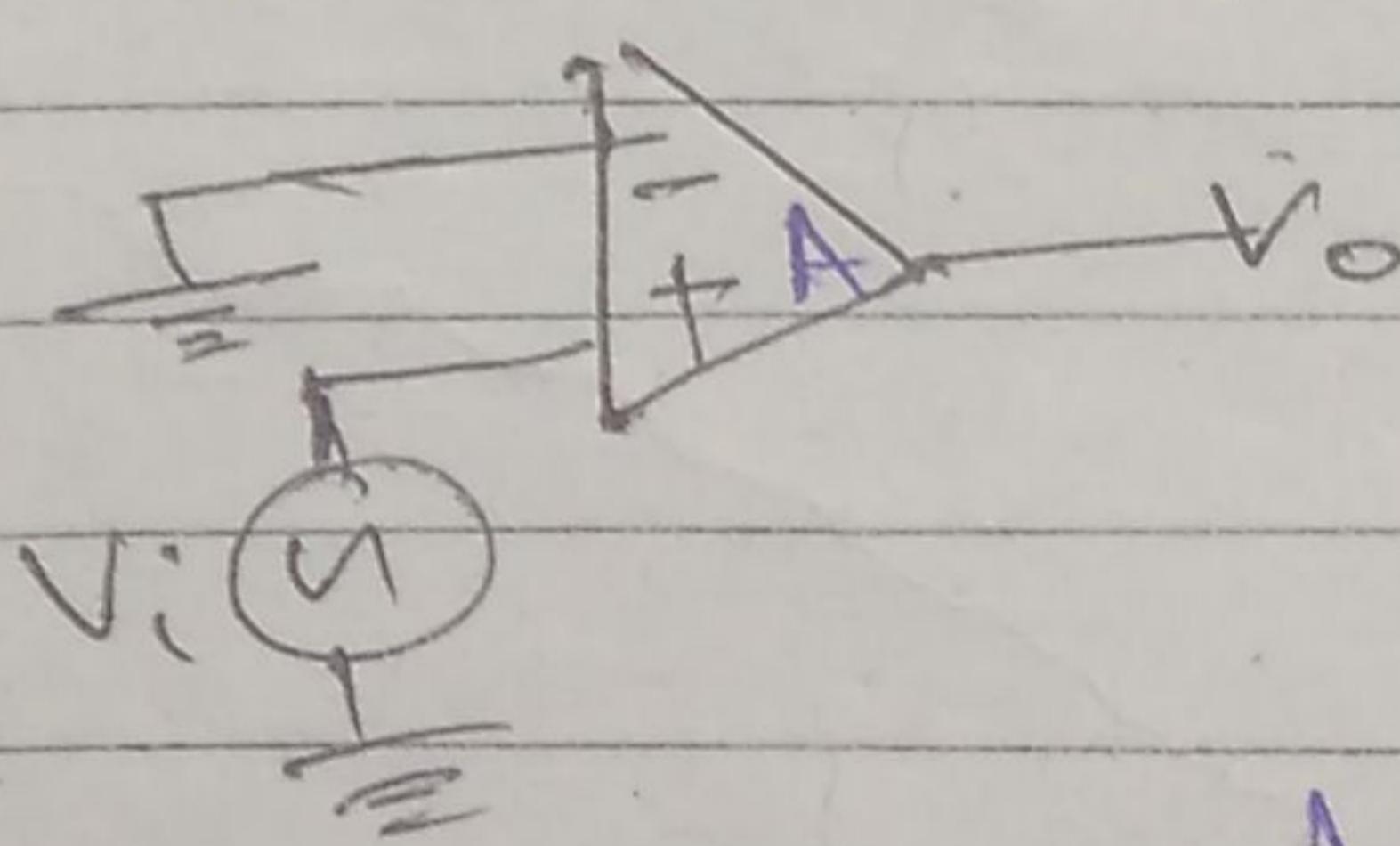
- It is without feedback

- It has less utility.

- It is used in voltage comparator.

Non inverting Amplifier.

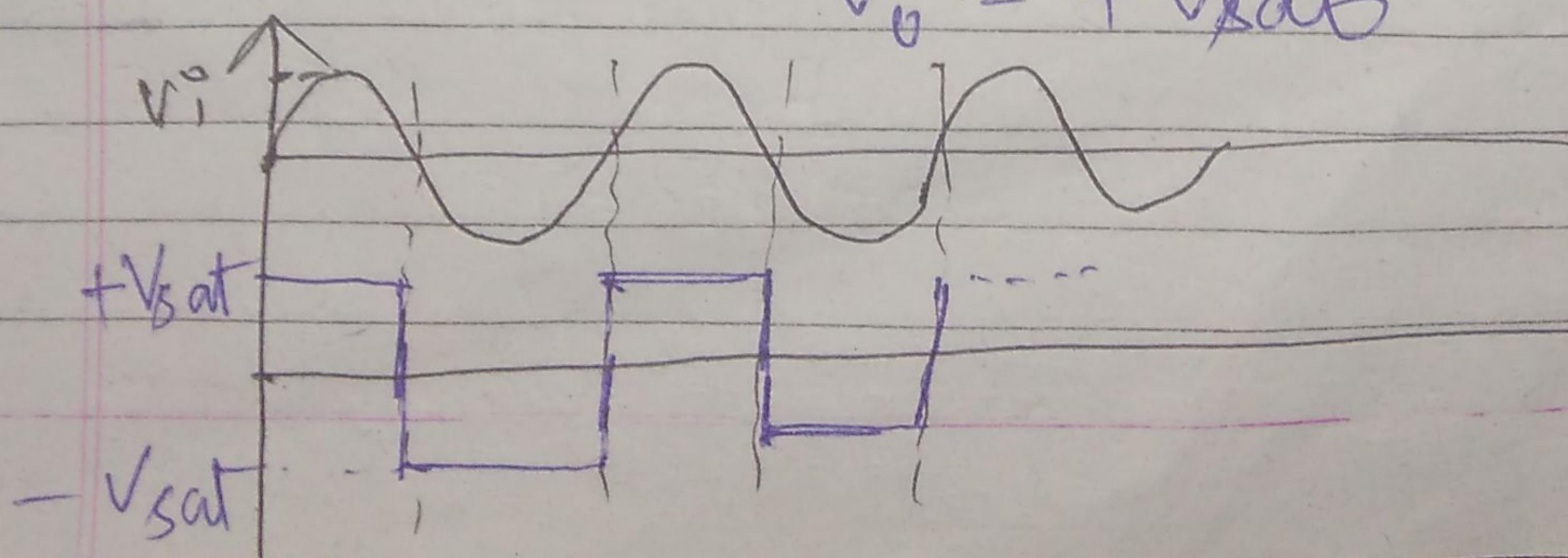
Input at positive (+) terminal.



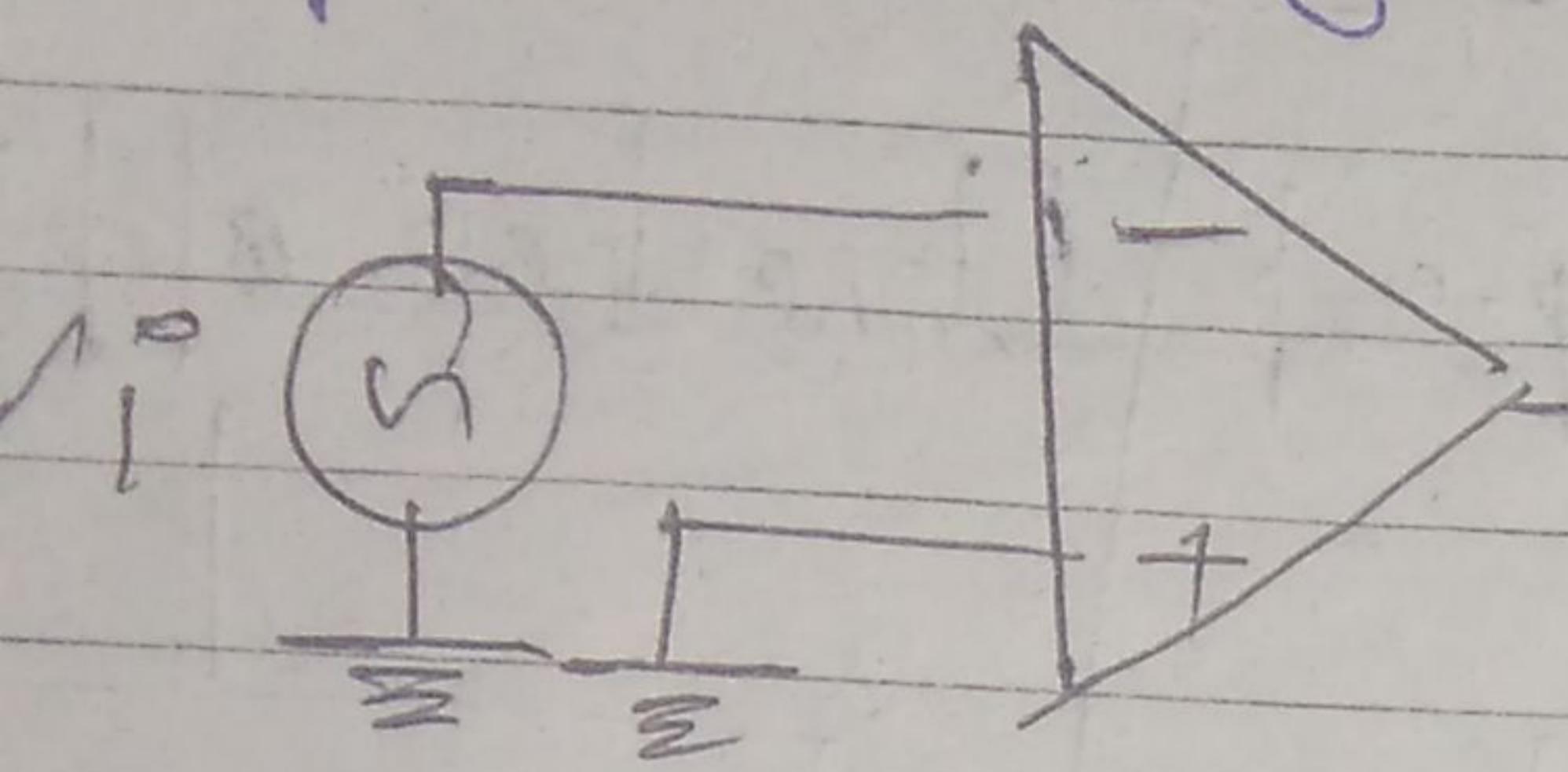
$$V_0 = A(V_1 - 0) = AV_1$$

$$V_0 > 0$$

$$V_0 = +V_{sat}$$



Inverting Op-Amp.
input at negative terminal.

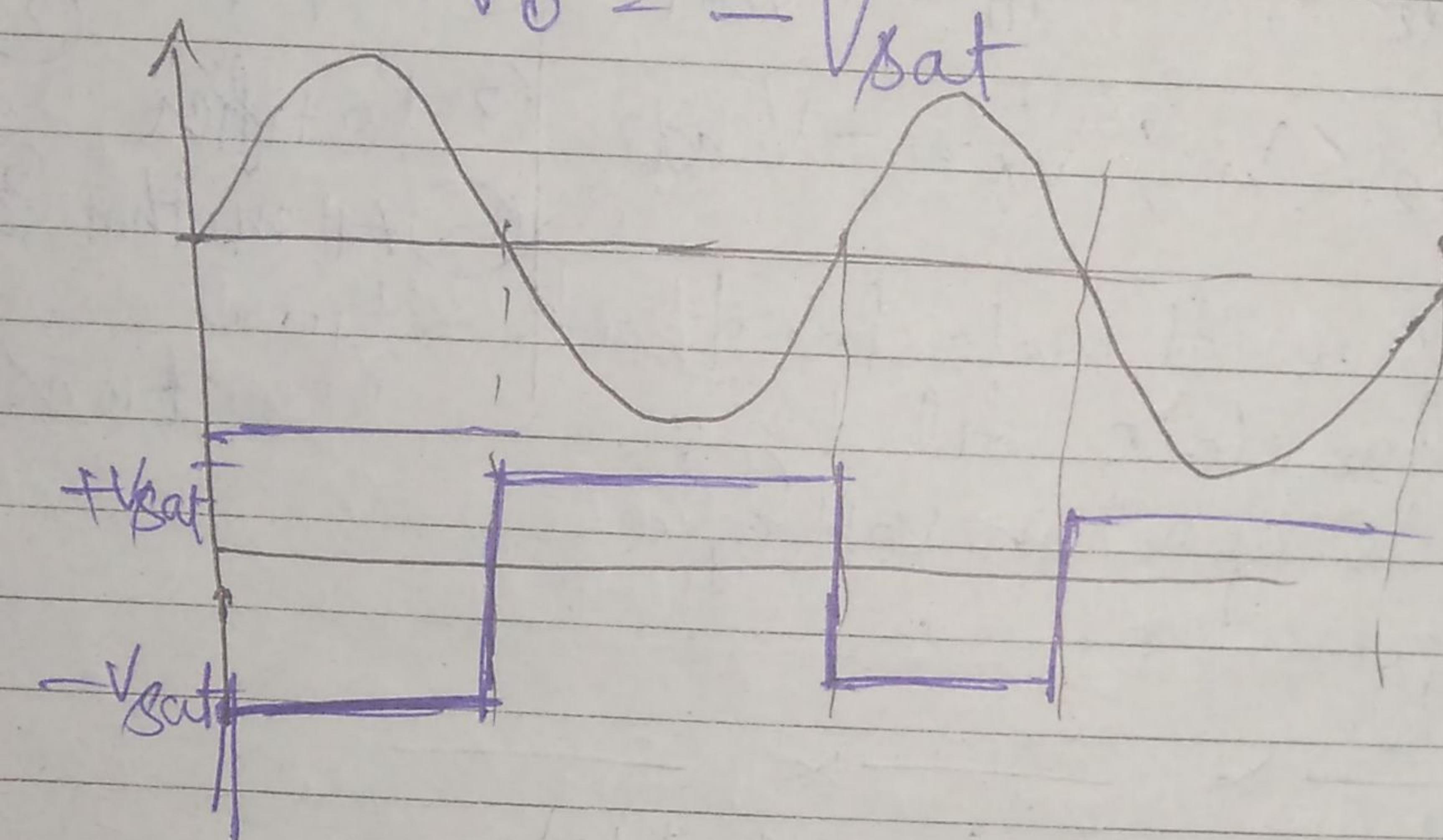


$$V_o = A(V_i - V_o)$$

$$V_o = -AV_i$$

$V_i < 0$

$$V_o = -V_{sat}$$

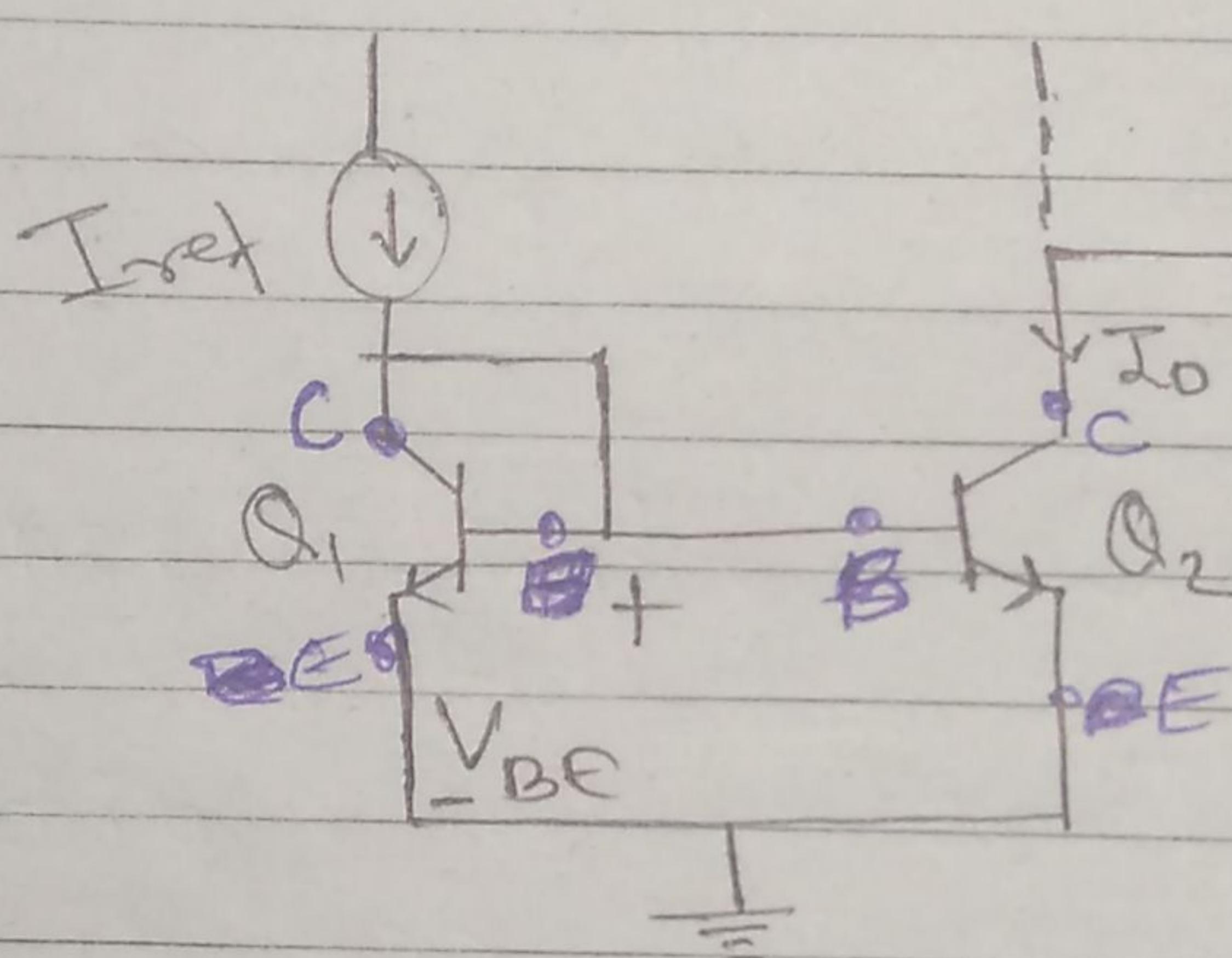


$$\beta = \frac{I_C}{I_B}$$

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Current Mirror

BJT Current Mirror :-



* β is very high

V_{BE} (same)
 Q_1 & Q_2 are matched

Here, 2 BJT Q_1 and Q_2 are matched

⇒ if two BJT are matched
it means

β for both Q_1 & Q_2 are same.

→ let β is sufficiently large so that
base current are assumed to be negligible

→ reference current is (I_{ref}) passed to
base-emitter junction of Q_1 so that
 V_{BE} is developed and same voltage
difference for base-emitter junction
of Q_2

- When θ_2 is matched to θ_1 , i.e., emitter base junction area of θ_1 and θ_2 are same. Then,

Ho = Ice

(unit current gain)

for these O_2 should operate in active season.

$$V_{CE} \geq 0.3V$$

for current amplification

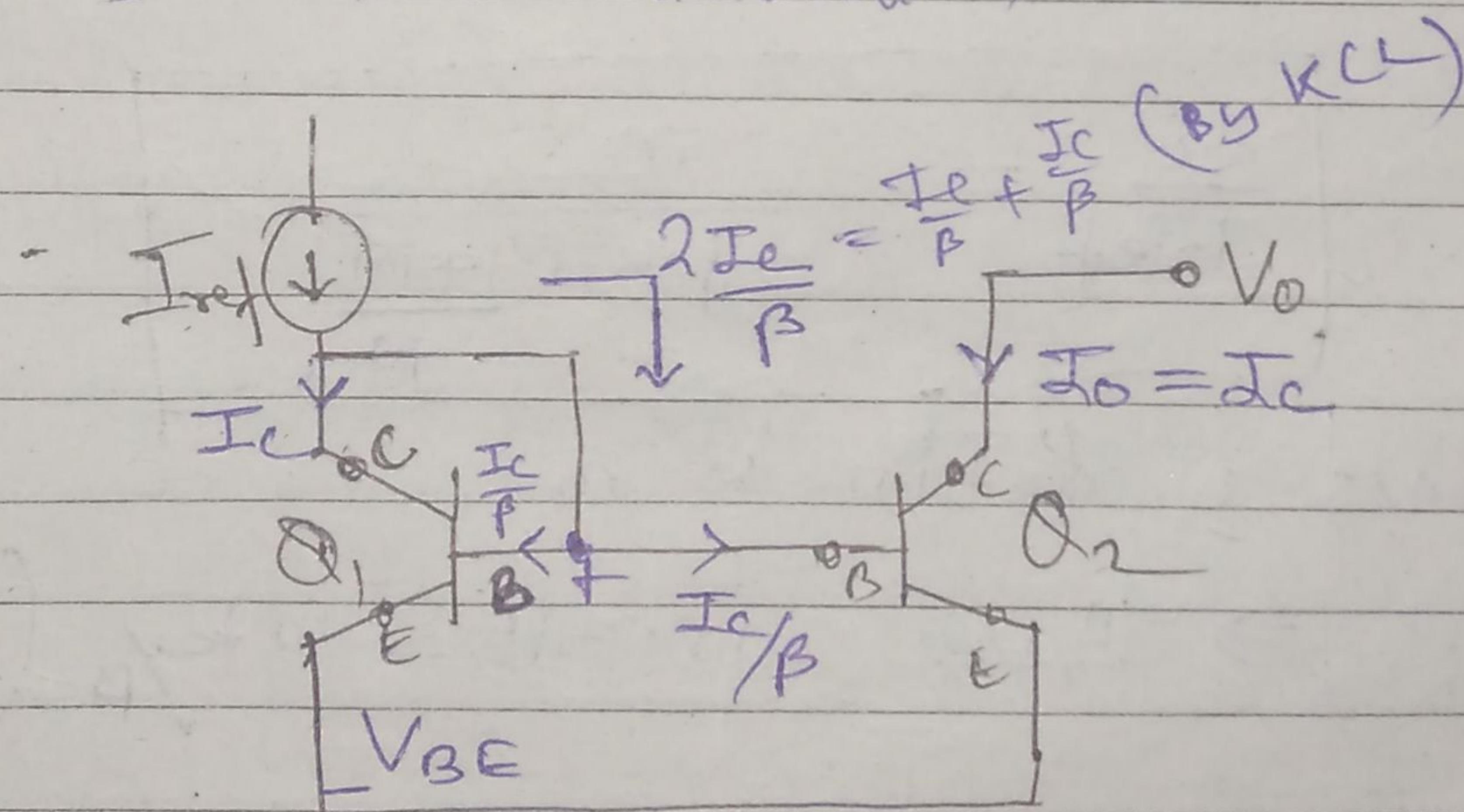
$$I_0 = m \cdot I_{ref}$$

m = transfer ratio

m = Emitter-base J_n area of Q₂

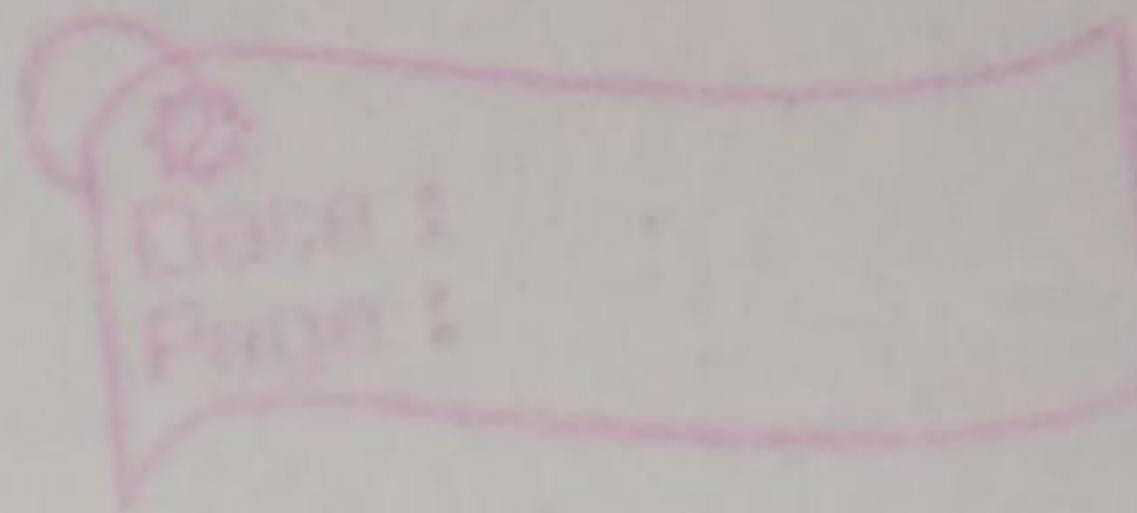
Emitter-Base J_n area of Q_i

- ~~Effect of finite B on transfer ratio~~



$$I_{ref} = I_e + \frac{2I_c}{\beta}$$

$$\bar{\varepsilon} = \text{He} \left(1 + \frac{2}{\beta} \right)$$



Since, $I_o = I_c$

$$I_{ref} = I_o \left(1 + \frac{2}{\beta} \right)$$

$$\frac{I_o}{I_{ref}} = \frac{1}{1 + \frac{2}{\beta}}$$

Current
Transfer
ratio

$$\text{but } \beta \rightarrow \infty \quad \frac{I_o}{I_{ref}} \rightarrow 1$$

→ Hence finite value of β cause an error in current transfer ratio (i.e. I_o/I_{ref}).

This error increases with increase in transfer ratio

* → When transfer ratio is m .

$$\frac{I_o}{I_{ref}} = \frac{m}{1 + \frac{(1+m)}{\beta}}$$

transfer Ratio is m

$$\Rightarrow \text{Base current} = m I_c / \beta \quad (\text{for } \beta_2)$$

$$\Rightarrow I_o = I_c \times m \quad (I_o = m \text{ times } I_c \text{ of } \beta_1)$$

$$I_{ref} = \frac{I_c}{\beta} + m \frac{I_c}{\beta} + I_c$$

$V_{BE} = 0.7$ for BJT

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$$= I_e \left[1 + \frac{(1+m)}{\beta} \right]$$

$$= \frac{I_o}{m} \left[1 + \frac{(1+m)}{\beta} \right]$$

$$\rightarrow \boxed{\frac{I_o}{I_{ref}} = \frac{m}{1 + \frac{(1+m)}{\beta}}}$$

O/p resistance

V_{A2} is the early voltage of Q_2 .

$$R_o = \frac{\Delta V_o}{\Delta I_o} = \frac{V_{A2}}{I_o}$$

① Even after neglecting finite β
 I_o will be equal to I_{ref} when
 Q_2 has same V_{CE} as &

② As, V_o increases I_o also increases

taking β and R_o into account

$$\boxed{I_o = I_{ref} \left(\frac{1+m}{1 + \frac{(1+m)}{\beta}} \right) \left(1 + \frac{V_o - V_{BE}}{V_{A2}} \right)}$$

Ques Consider the a BJT current mirror with a nominal current transfer ratio of unity. Let the transistor have $I_s = 10^{-15} A$, $\beta = 100$, $V_A = 100 V$ for $I_{ref} = 1 mA$ find I_o when $V_o = 5V$

* Current mirror can be used as constant power source.

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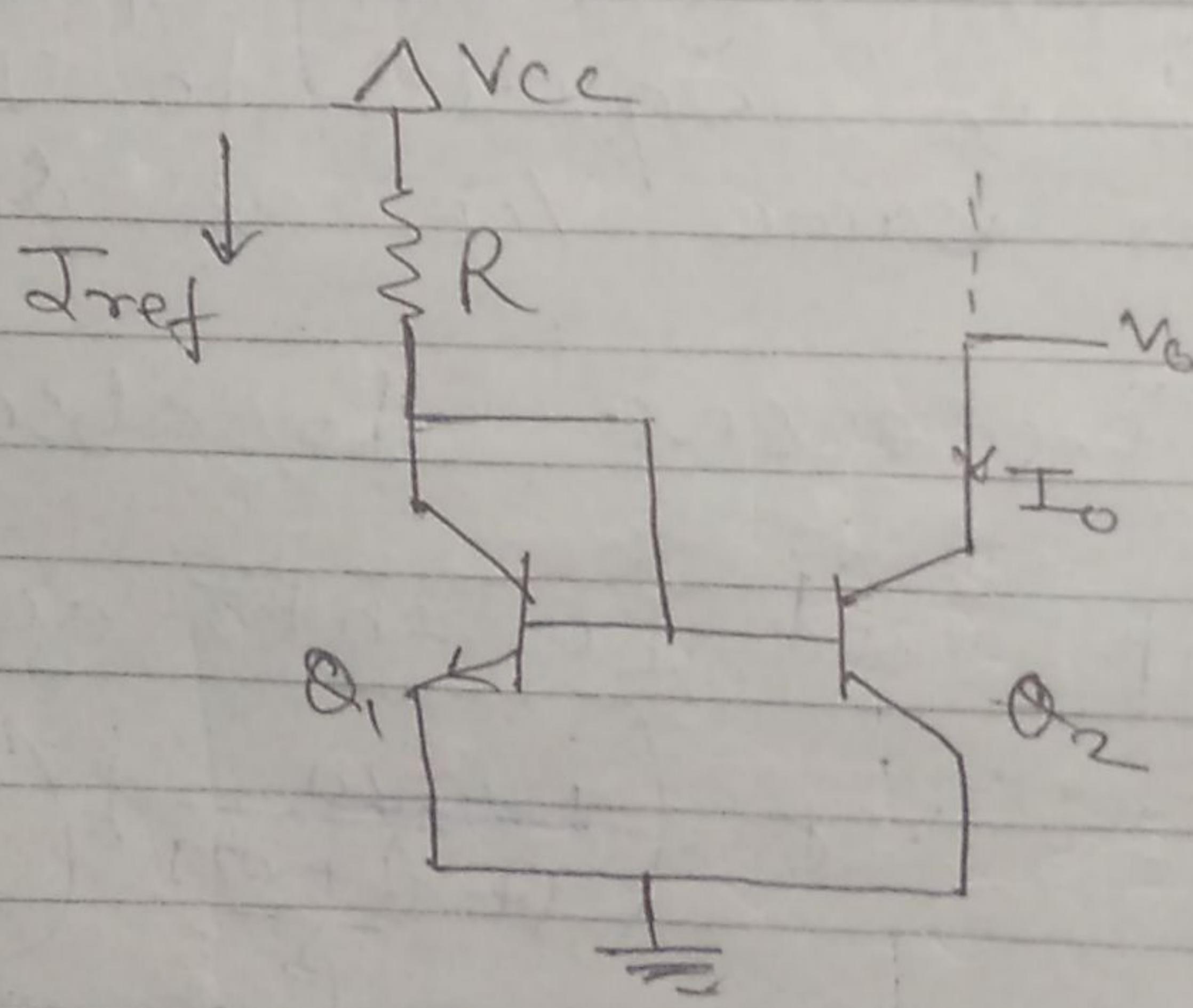
Also find output resistance.

Soln - $m = 1$

$$I_o = I_{ref} \left(1 + \frac{1}{1 + \frac{2}{\beta}} \right) \left(1 + \frac{V_o - V_{BE}}{V_A} \right)$$

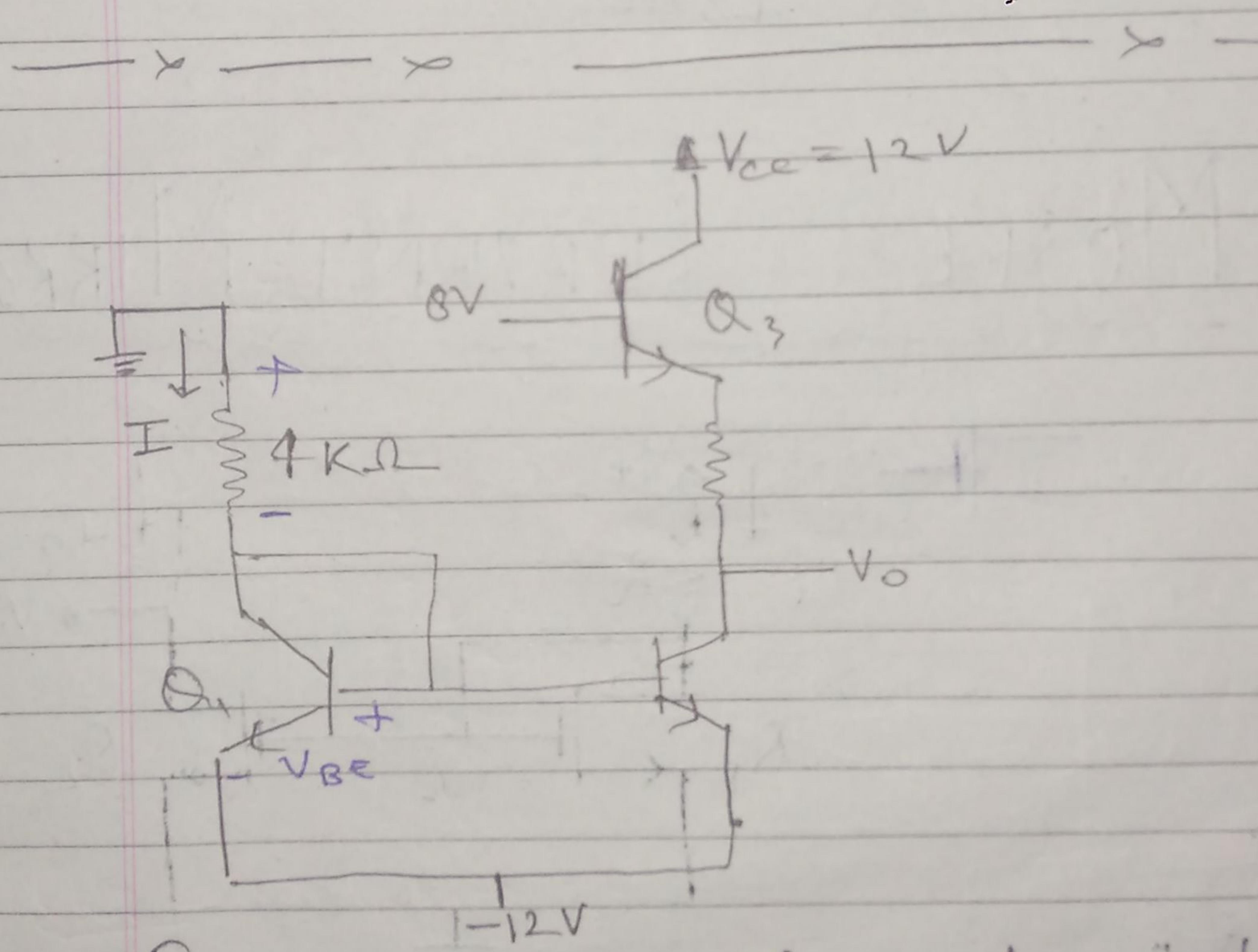
Ques $I_S =$

Ans $I_S = 10^{-15} A$ $\beta = 100$ $V_A = 50V$ $I_o = 0.5mA$
at $V_o = 2V$ power supply $V_{cc} = 5V$



Find I_{ref} , R also find I_o at $V_o = 5V$

nA



In the circuit shown transistors have large β , $V_{BE} = 0.7V$. Find resistance R such that $V_o = 0$

because gate & source is shorted, therefore it is working in saturation region.

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Soln: — $V_{BE} = 0.7V$ $V_o = 0$
 $R = ?$

By KVL in left side

$$I \times 4 \times 10^3 + 0.7 - 12 = 0$$

$$I = \frac{12.0 - 0.7}{4 \times 10^3} = \frac{11.3}{4 \times 10^3} = \frac{11.3}{4} mA$$

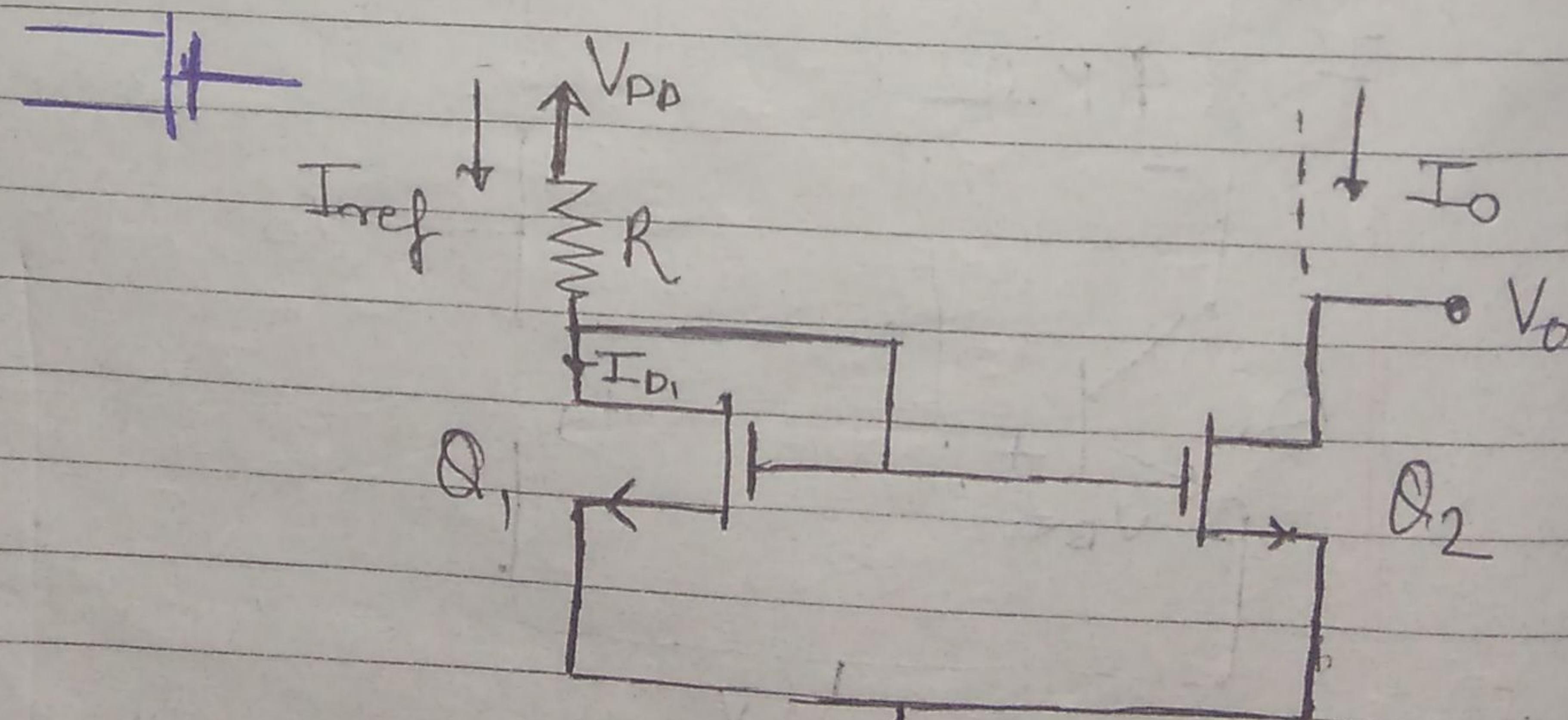
$$= 2.825$$

Now KVL in right side.

$$8 - 0.7 - R \times I = 0$$

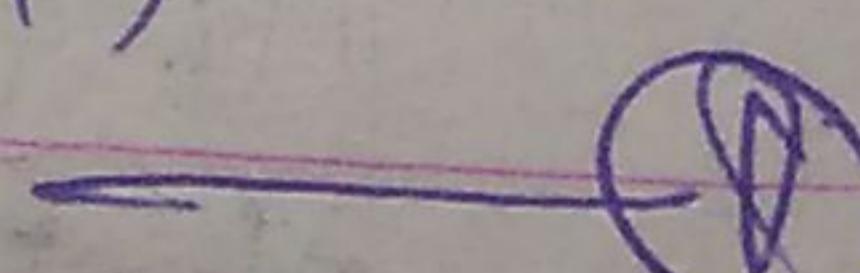
$$R = \frac{7.3 \times 4}{11.3 \times 10^{-3}} = 2.56 k\Omega$$

MOSFET CURRENT MIRROR



for Q_1 ,

$$I_{D1} = \frac{1}{2} k_n \left(\frac{W}{L} \right) (V_{GS} - V_{th})^2$$



$$I_{ref} = I_D \Rightarrow (\because I_A = 0)$$

$$I_{ref} = \frac{V_{DD} - V_{AS}}{R} \quad \text{--- (2)}$$

- Drain of Q_1 is sorted to its gate, therefore Q_1 is working in saturation region.

Here channel length modulation is neglection.

from the fig. since gate current $I_A = 0$ therefore,

$$I_{D1} = I_{ref} = \frac{V_{DD} - V_{AS}}{R}$$

Here current through R is considered as ~~diff~~ reference current.

for Q_2 ,

it has same V_{AS} as Q_1 , if we assume that Q_2 is working in saturation region then its drain current is given by -

$$I_{D2} = \frac{1}{2} K_n' \left(\frac{W}{L} \right)^2 (V_{AS} - V_{th})^2$$

$$I_{D2} = I_0 \quad \text{--- (3)}$$

from (2) and (3)

$$\frac{I_0}{I_{ref}} = \frac{(W/L)^2}{(W/L)} =$$

here, ratio of I_0 & I_{ref} depends on

the aspect ratio of θ_1 & θ_2 .

→ for identical transistor,

$$I_o = I_{ref}$$

and circuit replicate the reference current in the output terminal.

{ for θ_2 in saturation:-

$$V_{DS} \geq V_{ov} \leftarrow \text{overside voltage}$$

$$V_{DS} \geq V_{as} - V_{th}$$

— θ_2 will properly operate for value of V_o as long as possible (V_{ov})

→ Drain current of θ_2 , i.e. I_o , will be equal to I_{ref} in θ_1 at V_o which causes same V_{DS} for both device

$$\boxed{I_o = I_{ref}}$$

(V_{DS} is same)
 $V_{DS} = V_{as}$

$$\text{i.e } V_{DS} = V_{as}$$

$$V_o = V_{as}$$

$$I_o$$

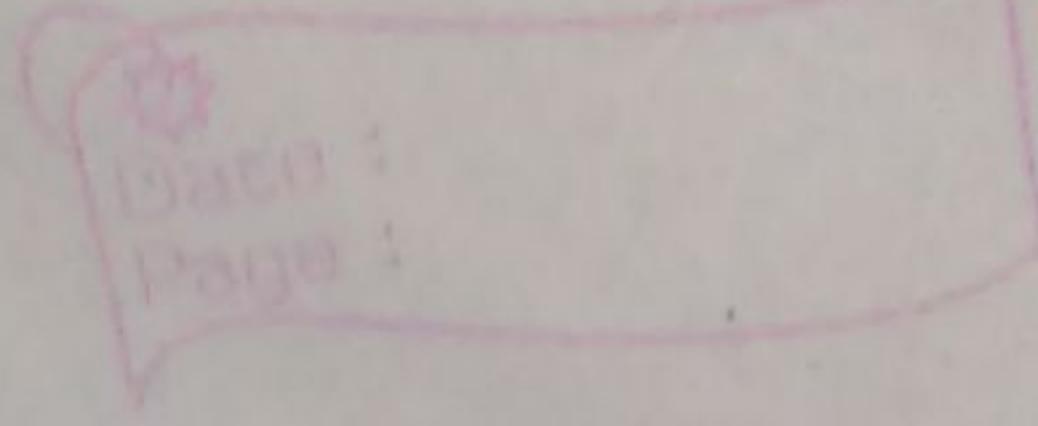
I_{ref}

$$\leftarrow \text{slope} = 1/r_o$$

V_{as} V_{th} V_{DS}

V_o

$V_A \rightarrow$ Early voltage



$$\frac{I_o}{I_{ref}} = \frac{(w/L)_2}{(w/L)_1} \left(1 + \frac{V_0 - V_{AS}}{V_A} \right)$$

Ques Given that $V_{DD} = 3V$
 $I_{ref} = 100 \mu A$
 $I_o = 100 \mu A$

find the value of R if Q_1 and Q_2 are matched and channel length

$1 \mu m$, channel width of $10 \mu m$,

threshold voltage $0.7V$, $k_n' = 200 \mu A/V^2$

what is the lowest possible value of V_0 , $V_A' = 20 V/\mu m$ find output

resistance of current source, also find change in output current resulting from ~~plus~~ ~~minus~~ $\pm 1V$ change in output voltage

$$V_{DD} = 3V$$

$$I_{ref} = 100 \mu A$$

$$I_o = 100 \mu A$$

$$L = 1 \mu m$$

$$W = 10 \mu m$$

$$V_T = 0.7V$$

$$k_n = 200 \mu A/V^2$$

$$(V_0)_{min} 20V/\mu m$$

$$I_{ref} = \frac{1}{2} k_n' \left(\frac{W}{L} \right)_1 (V_{HS} - V_T)^2$$

$$V_{HS} =$$

$$I_{ref} = \frac{V_{DD} - V_{HS}}{R}$$

$$R =$$

$$\rightarrow (V_o)_{min} = V_{ov}$$
$$= V_{AS} - V_T$$
$$= 0.3V$$

$$\rightarrow R_o = \frac{V_A}{I_o}$$

$$V_A = V_A' \times L$$
$$= 20 \Omega$$

$$\Rightarrow R_o = \frac{20}{100 \times 10^{-6}} = 0.2M\Omega$$

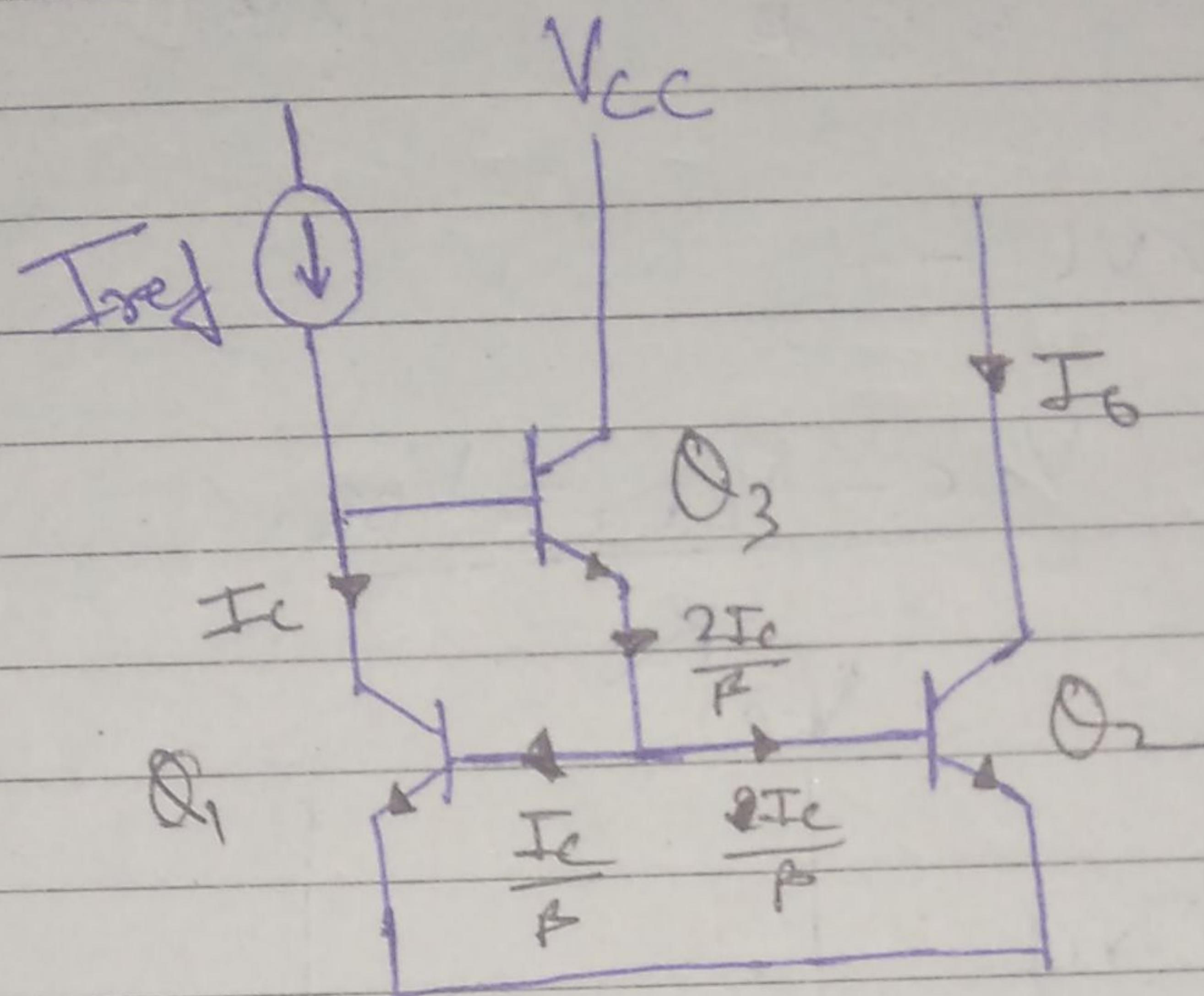
$$\rightarrow \Delta V_o = 1V$$

$$f_o = \frac{\Delta V_o}{\Delta I_o}$$

$$\Delta I_o = \frac{1}{0.2 \times 10^3} = 5mA$$

Bipolar mirror with base

bipolar Mirror with base Compensated Circuit



Emitter current of Q_3 , $I_{E3} = \frac{2I_c}{\beta}$

$$\text{Base current } I_{B3} = \frac{I_{E3}}{1+\beta} = \frac{2I_c}{\beta(1+\beta)}$$

$$I_{ref} = I_c + \frac{2I_c}{\beta(1+\beta)} = I_c \left[1 + \frac{2}{\beta(1+\beta)} \right]$$

$$I_o = I_c$$

$$\therefore \frac{I_o}{I_{ref}} = \frac{1}{1 + \frac{2}{\beta(1+\beta)}} \approx \frac{1}{1 + \frac{2}{\beta^2}}$$

→ Circuit shows bipolar current mirror with a current transfer ratio i.e. much less dependent on β than that of simple current mirror.

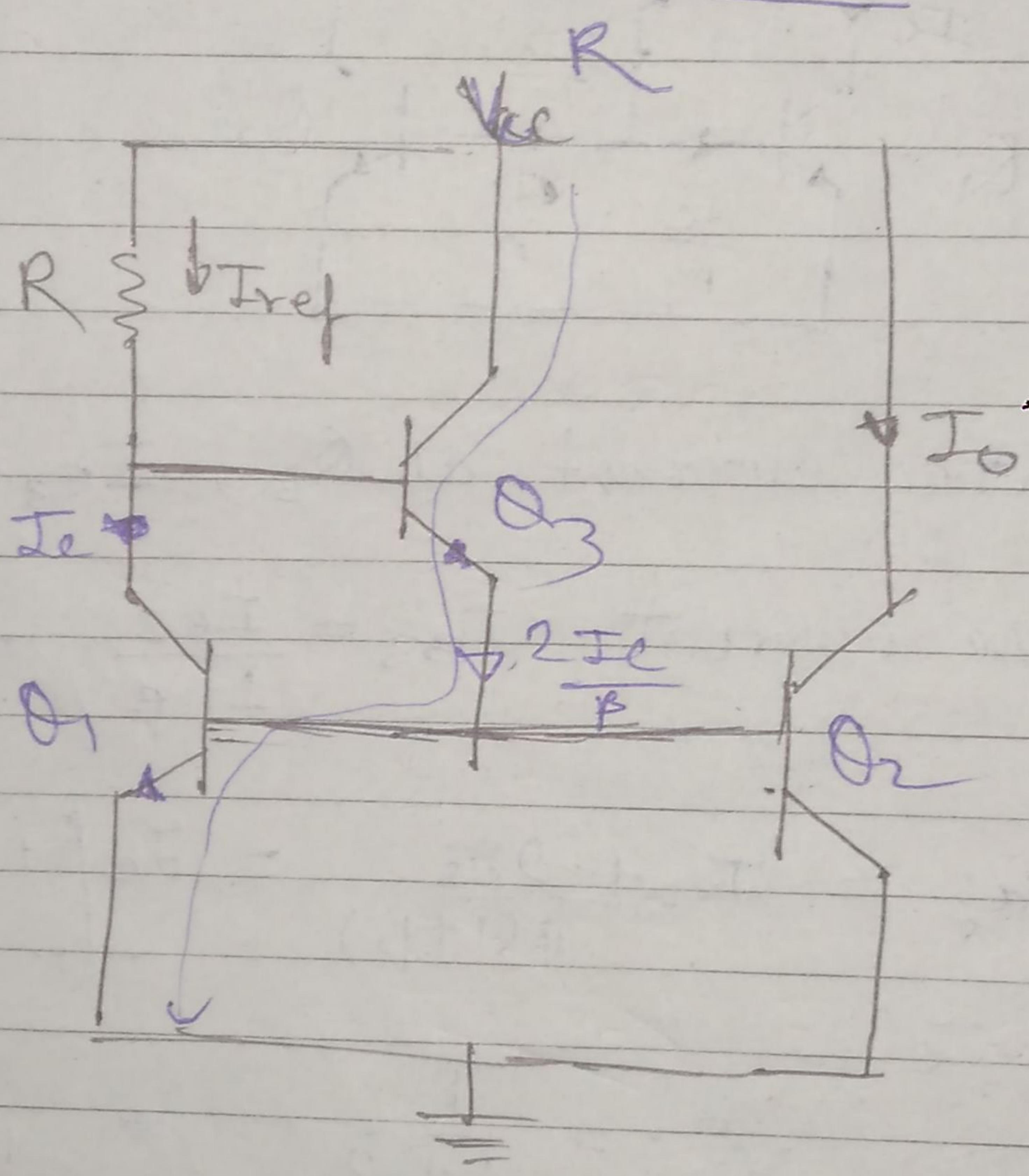
→ The reduced dependence on β has been achieved by including transistor Q_1 .

→ Emitter of Q_3 provides base current for Q_2 and I_o .

Here, error due to finite β has been reduced from $\frac{2}{\beta}$ to $\frac{2}{\beta^2}$

→ Applying KVL -

$$I_{ref} = \frac{V_{cc} - V_{BE3} - V_{BE1}}{R}$$

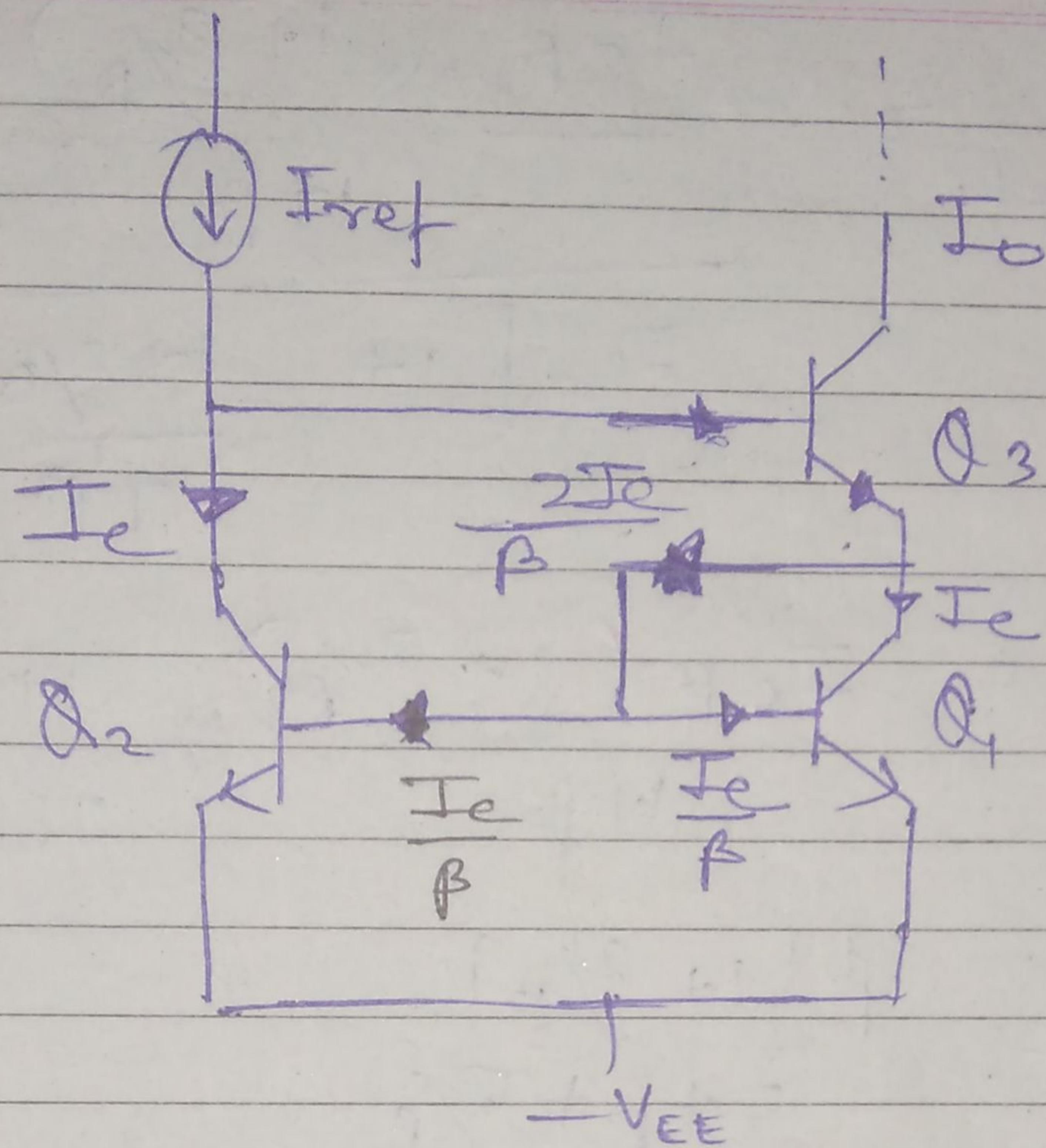


Q

Wilson Current Mirror

$$J_B = \frac{I_E}{1+\beta} \quad n$$

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$$I_{E3} = \frac{2I_e}{\beta} + I_e = I_e \left(\frac{2}{\beta} + 1 \right)$$

$$J_{B3} = \frac{I_E}{1+\beta} = \frac{I_e \left(\frac{2}{\beta} + 1 \right)}{1+\beta}$$

$$I_{c3} = I_o \approx \beta J_{B3} = I_e \beta \left(1 + \gamma_B \right)$$

$$J_{oef} = I_c + J_{B3} \quad \frac{1}{1+\beta}$$

$$= I_e + I_e \left(\frac{\frac{2}{\beta} + 1}{1+\beta} \right)$$

$$= I_e \left(\underbrace{1 + \beta}_{1+\beta} + \left(\frac{\frac{2}{\beta} + 1}{1+\beta} \right) \right)$$

$$= I_e \left(\frac{2 + \beta + \gamma_B}{1+\beta} \right)$$

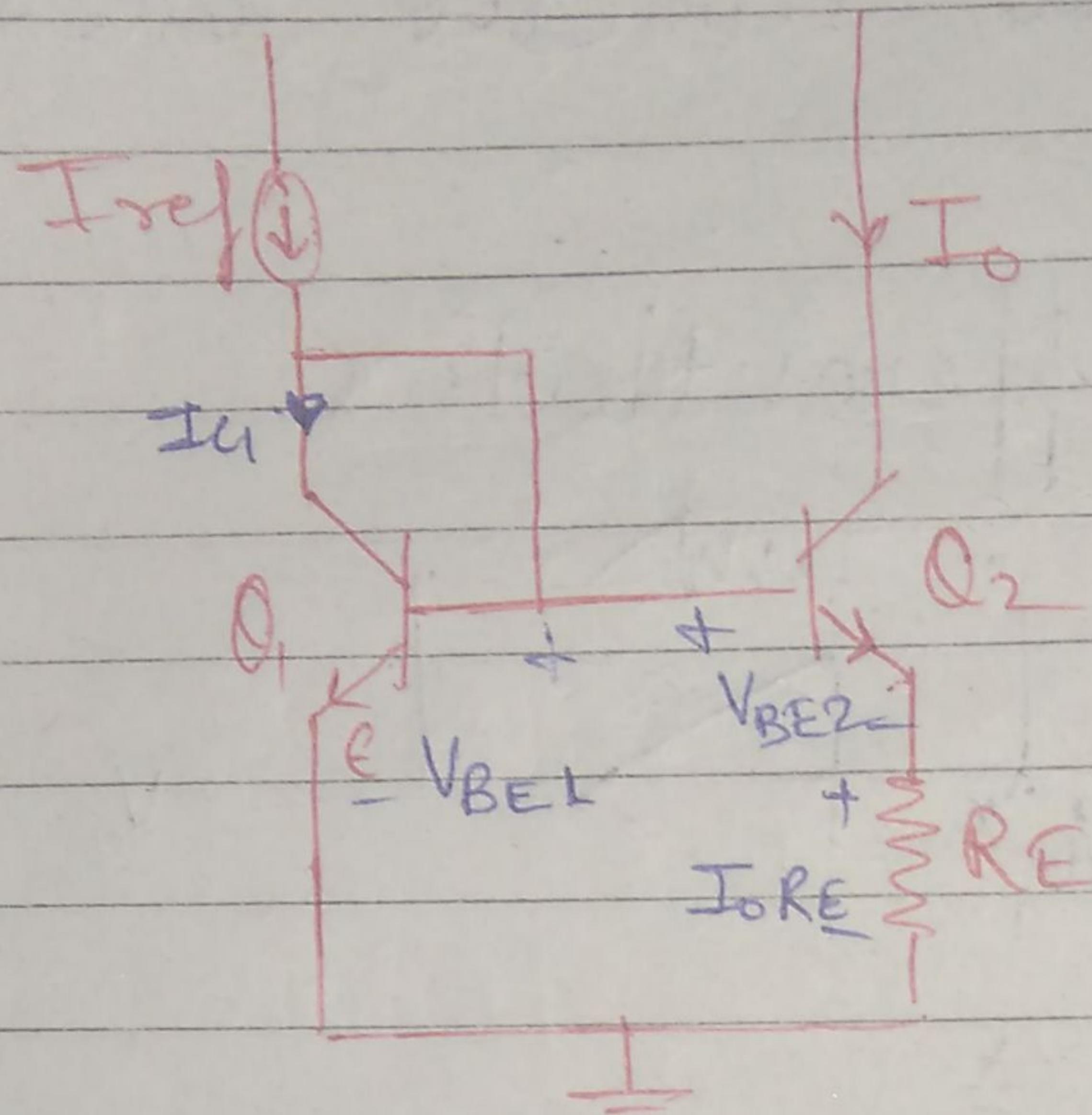
$$= I_e \left(1 + \frac{1 + \gamma_B^2}{1+\beta} \right)$$

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$$\begin{aligned}
 \frac{I_0}{I_{ref}} &= \frac{I_c \beta (1 + 2\gamma/\beta)}{1 + \beta} \\
 &\quad \times \frac{I_c [1 + \frac{1 + 2\gamma/\beta}{1 + \beta}]}{1 + \beta} \\
 &\approx \frac{I_c \beta (1 + 2\gamma/\beta)}{1 + \beta} \times \frac{1 + \beta}{I_c (1 + \beta + 1 + 2\gamma/\beta)} \\
 &= \frac{\beta (1 + 2\gamma/\beta)}{2 + \beta + 2\gamma/\beta} \\
 &\approx \frac{\beta (1 + 2\gamma/\beta)}{\beta + 2(1 + 1/\beta)} = \frac{\beta(\beta+2)}{\beta + (2\beta+2)} \\
 &= \frac{\beta(\beta+2)}{\cancel{\beta^2} + 2\beta + 2} \\
 &\approx \frac{\beta(\beta+2)}{1 + \beta + 2\gamma/\beta} = \frac{\beta+2}{\beta + 2 + 2\gamma/\beta} \\
 \frac{I_0}{I_{ref}} &\approx \frac{1}{1 + \frac{2}{\beta(1+\beta)}} \approx \frac{1}{1 + 2\gamma/\beta^2}
 \end{aligned}$$

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Widlar Current Source



Here, α_1 & α_2 are matched

In Widlar's current source, resistor R_E is connected in the emitter of Q_2 .

* Neglecting base current. (high β)
 $\Rightarrow I_{ref} = I_e, \quad I_o = I_{C2}$

$$\Rightarrow V_{BE1} = V_T \ln \left(\frac{I_{ref}}{I_S} \right)$$

$$V_{BE2} = V_T \ln \left(\frac{I_o}{I_S} \right)$$

$$V_{BE1} - V_{BE2} = V_T \left[\ln \left(\frac{I_{ref}}{I_S} \right) - \ln \left(\frac{I_o}{I_S} \right) \right]$$

$$V_{BE1} - V_{BE2} = V_T \ln \left(\frac{I_{ref} \times I_S}{I_S \times I_o} \right)$$

$$V_{BE1} - V_{BE2} = V_T \ln \left(\frac{I_{ref}}{I_o} \right) \quad \text{--- (1)}$$

Applying KVL in ~~output~~ circuit.

$$V_{BE1} = V_{BE2} + I_{oRE}$$

$$I_o R_E = V_{BE_1} - V_{BE_2}$$

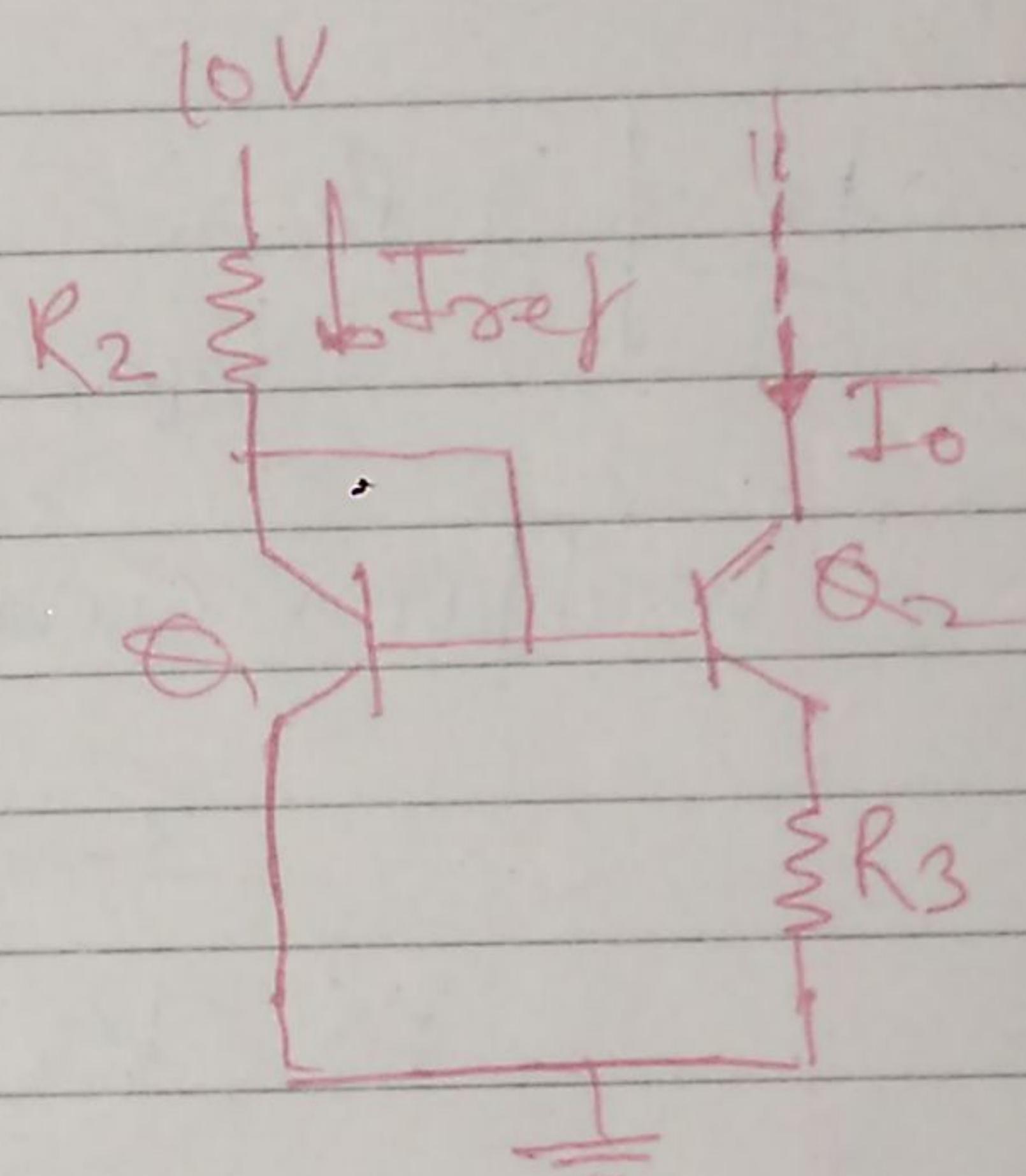
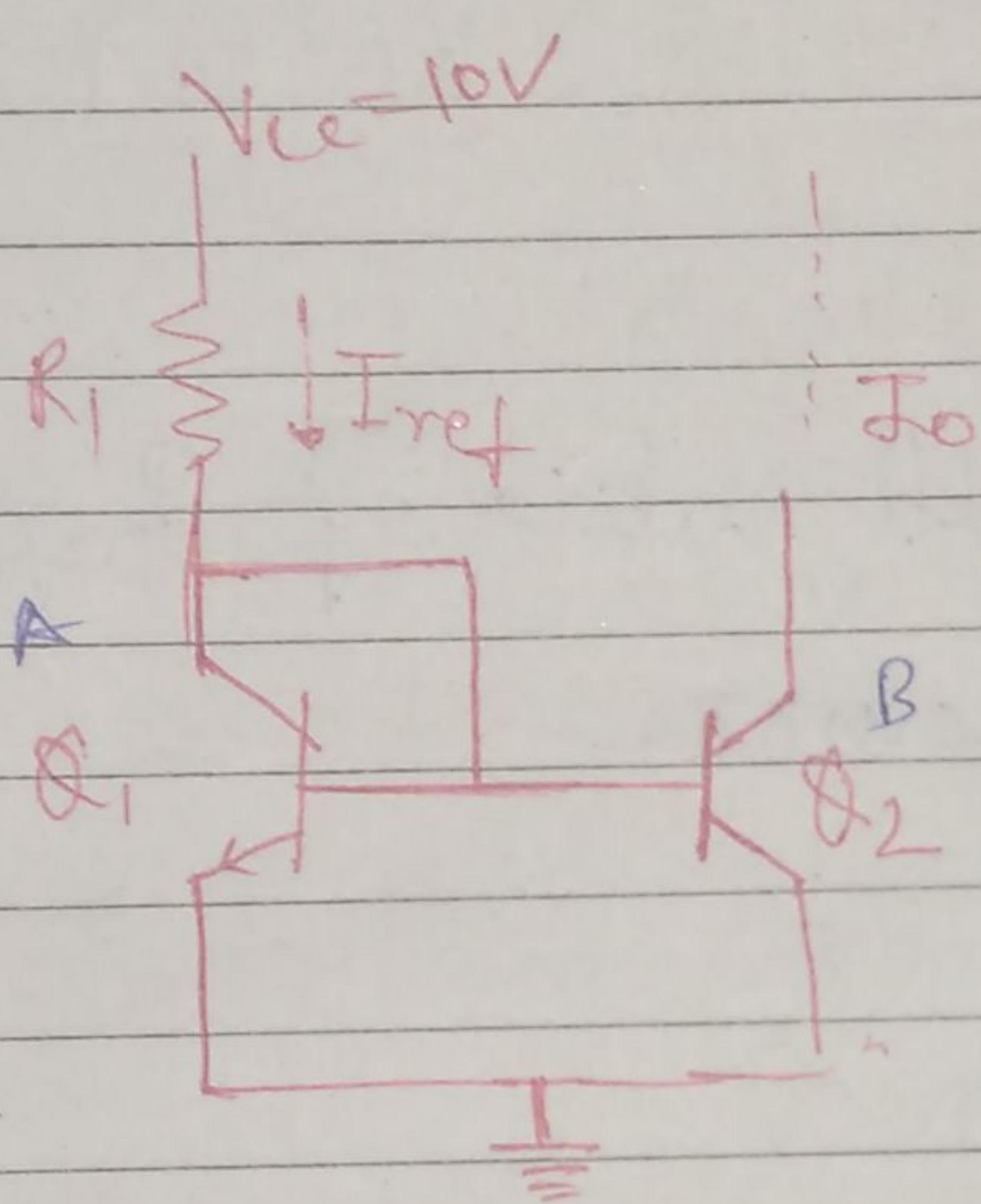
$$I_o R_E = V_T \ln \left(\frac{I_{ref}}{I_o} \right) \quad \text{from ①}$$

Important expression

$$R_o = [1 + g_m (\gamma_{\pi} || R_E)] \gamma_0$$

derivation not required

Ques



②

above circuit shows two methods of generating a constant current, $I_o = 10 \text{ mA}$. Determine the value of required resistor assuming that $V_{BE} = 0.7 \text{ V}$ at current of 1mA and neglecting the effect of finite p.

$$V_{BE_B} = V_{BE_A} + V_T \ln \left(\frac{I_B}{I_A} \right)$$

(Soln) In Fig. 1, Neglecting effect of finite p

$$I_{ref} = I_o = 10 \text{ mA}$$

$$V_{BEI} = 0.7 + V_T \ln \left(\frac{I_{ref}}{I_{TMA}} \right) \xrightarrow{I_{ref} = 0.58V} I_{ref} = 0.58V$$

$V_T = 26mV$

$$R_1 = \frac{V_{cc} - V_{BEI}}{I_{ref}} = \frac{10V - 0.58}{10 \times 10^{-6}} = 942k\Omega$$

$R_1 = 942k\Omega$

(n)

In fig B.

Take suitable value of I_{ref} for
widlar current source

$$I_{ref} = 1mA$$

$$\Rightarrow V_{BEI} = 0.7V$$

$$10 - R_2 \times I_{ref} + V_{BEI} = 0$$

$$R_2 = \frac{10 - 0.7}{1mA} = \frac{9.3}{1 \times 10^{-3}} = 9.3k\Omega$$

$R_2 = 9.3k\Omega$

from expression,

$$R_3 = V_T \ln \left(\frac{I_{ref}}{I_0} \right)$$

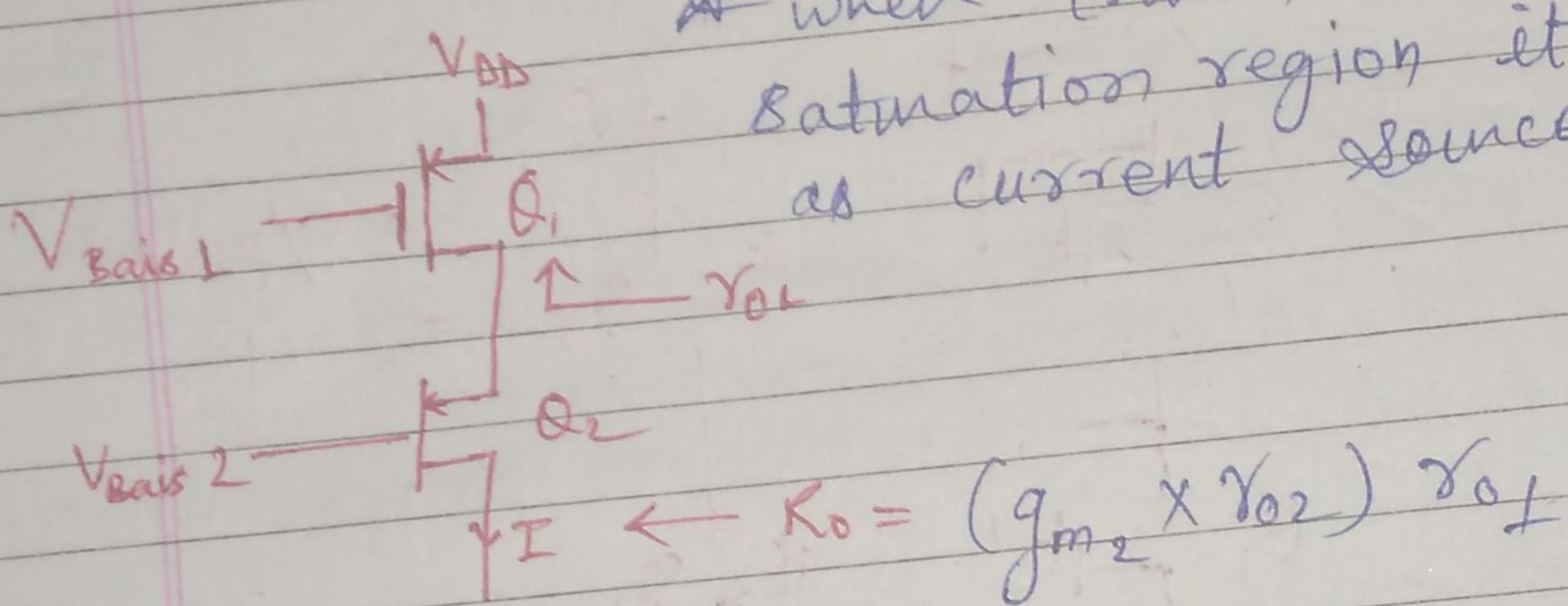
$$R_3 = V_T \ln \left(\frac{I_{ref}}{I_0} \right)$$

Advantage of Widlar Current Source

- ① Widlar circuit allows the generation of small constant current using relatively small resistors.
- ② β_t results in reduced chip area.
- ③ Output resistance is high.

Cascade Current Source

16/08/19



* when transistor work in saturation region it behaves as current source.

* Cascading of current source increases the output resistance.

In the above circuit diagram Q_1 is current source transistor and Q_2 is cascode transistor.

V_{bias1} is ~~set~~ to a value so that Q_1 provides required current I .

function of V_{bias2} is to keep Q_1 and Q_2 in saturation.

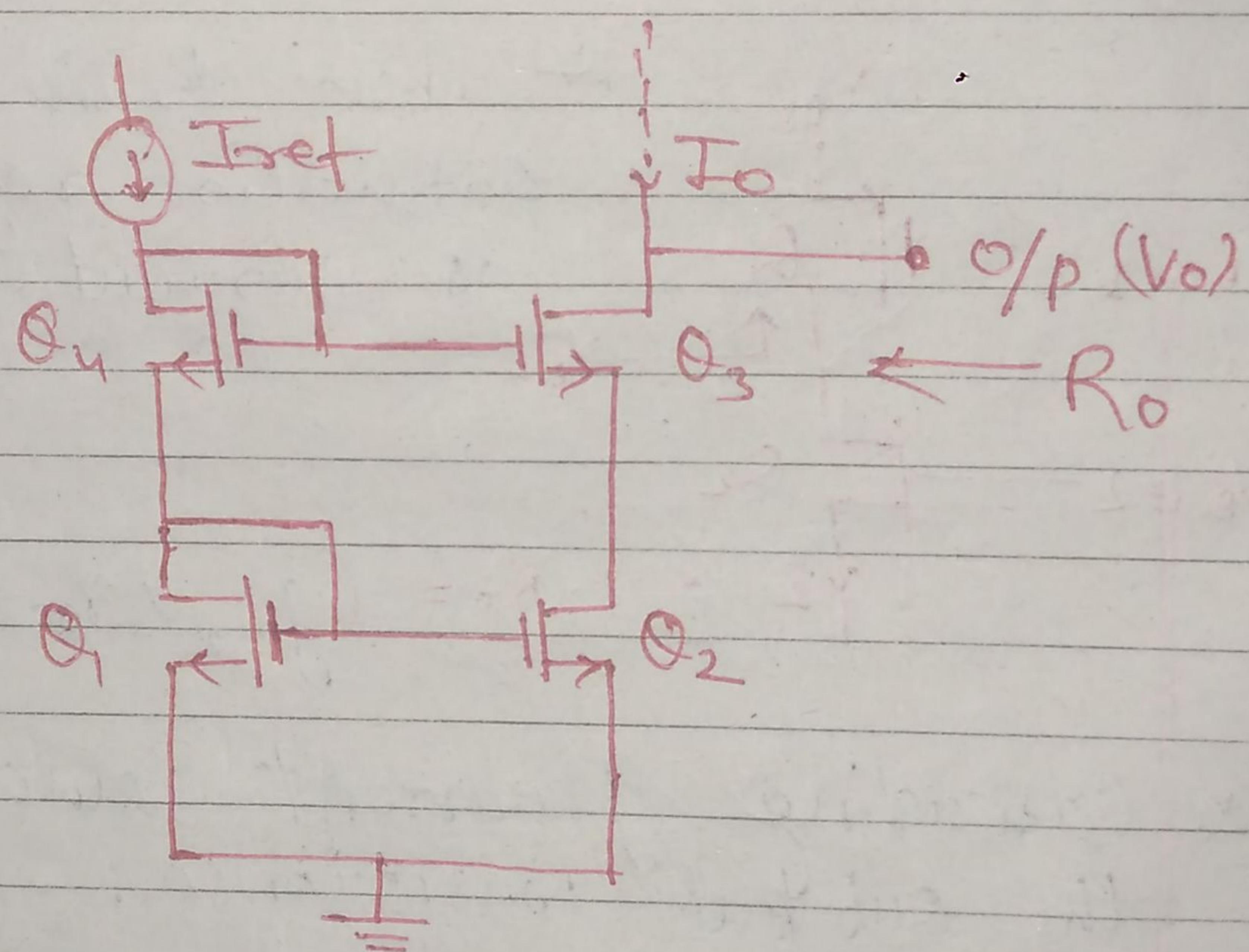
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r_{o2} is the resistance of Q_1 , looking from its drain.

Output resistance of current source is given by.

$$R_o = (g_{m2} \times r_{o2}) r_{o2}$$

Cascode Current Mirror



- * Above diagram shows basic cascode current mirror.
- * Here, Diode connected transistor Q_1 forms simple current mirror Q_1, Q_2 .
- * Another diode connected transistor Q_4 is used to provide suitable bias voltage for the gate of cascode transistor Q_3 .

- * Output Resistance R_o is of cascode current mirror is given by

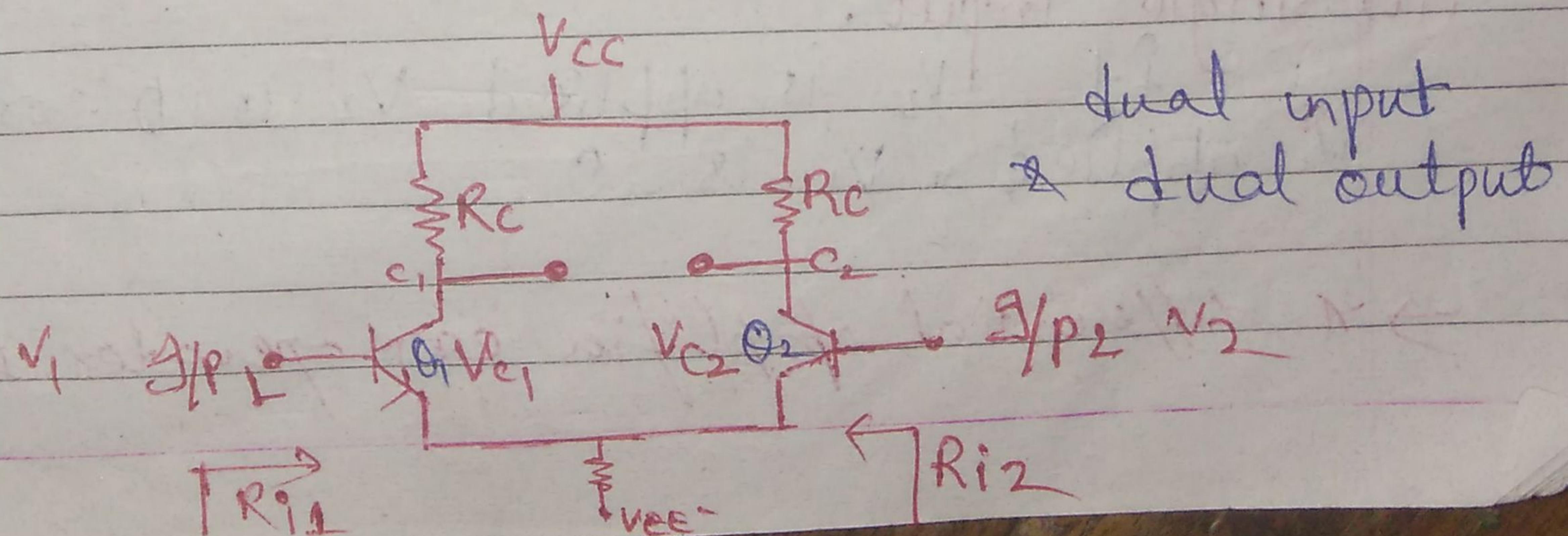
$$R_o = (g_m \gamma_{03}) \gamma_{02}$$

here, cascoding raise the output resistance of current source by the factor of $g_m \gamma_{03}$ (or gain of cascode transistors).

Drawbacks -

- * It consumes relatively large portion of supply voltage while simple MOS mirror operates properly with a voltage as low as overdrive voltage (V_{ov}) across its output transistor.
- * It limits the signal swing at the output of mirror.

Differential Amplifier.



- * It is also called difference amplifier it amplifies the difference between two input signals.
- * B_1 and B_2 are two identical transistors.
- * Output of differential amplifier is of two types

(i) Balanced or differential output

- * It is measured between two collectors since V_{dc} voltage at C₁ and C₂ are equal. balanced output does not contain any DC voltage.

(ii) Unbalanced output

- * It is measured at C₁ or C₂ w.r.t ground.
It contains DC voltage which is undesirable

Input to differential amplifier is of two types

(i) Dual or differential input

Both input V_1 and V_2 are applied simultaneously and net input will be difference of $V_1 + V_2$.

(ii) Single input.

If V_1 is applied V_2 is 0 or if V_2 is applied, V_1 is 0.

→ A differential amplifier can operates in 4 modes

amplifiers
etc.
toys
• types

i) Dual input balanced output mode

$$A_v = \frac{R_c}{r_e} ; r_e = \frac{V_T}{I_E}$$

r_e = Internal resistance of emitter junction of BJT

→ To have stable gain - current I_E should be stable

therefore r_e is replaced by constant current source.

$$R_{i1} = R_{i2} = 2\beta r_e$$

$$R_{o1} = R_{o2} = R_c$$

ii) Dual input unbalanced output mode

$$A_v = \frac{R_c}{2r_e} ; r_e = \frac{V_T}{I_E}$$

$$R_{i1} = R_{i2} = 2\beta r_e$$

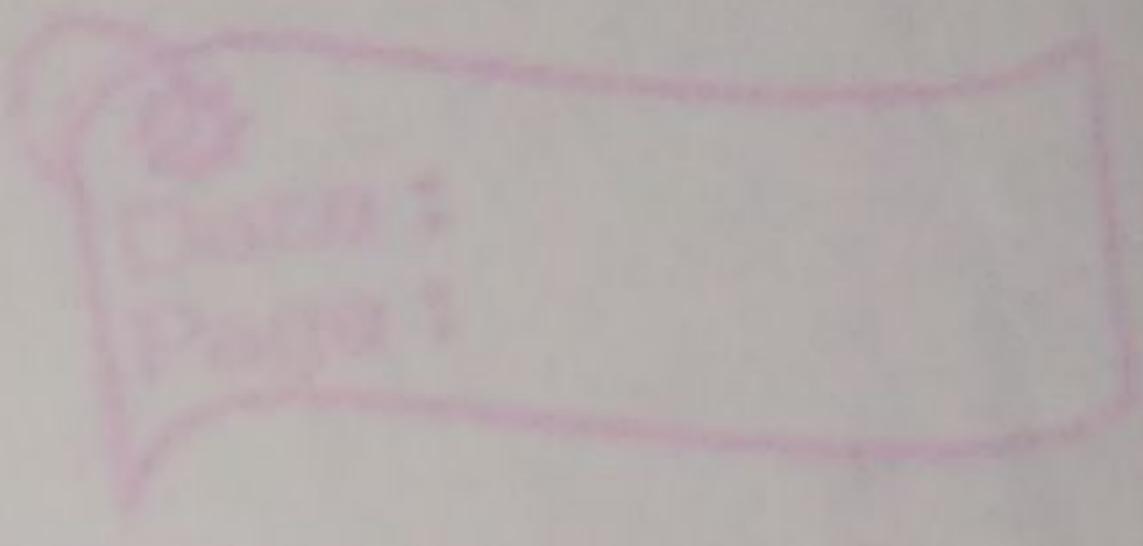
$$R_o = R_{o1} = R_c$$

iii) Single input balanced output mode

$$A_v = \frac{R_c}{r_e} ; r_e = \frac{V_T}{I_E}$$

$$R_i = 2\beta r_e$$

$$R_{o1} = R_{o2} = R_c$$



(iv) Single input unbalance output mode

$$A_v = \frac{R_c}{2\beta r_e} ; \quad \beta_e = \frac{V_T}{I_E}$$

$$R_i = 2\beta r_e$$

$$R_o = R_c$$