Date 28/02/2022

Unit:-3

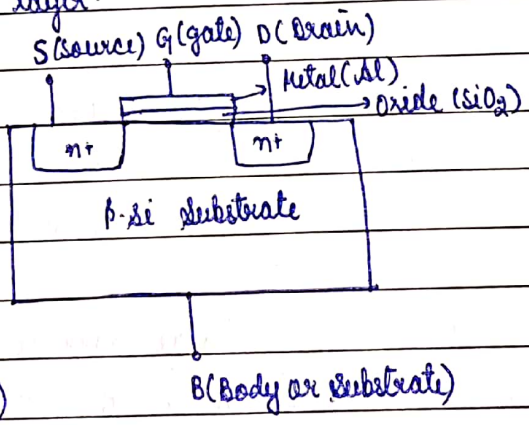
MOSFET

- MOSFET stands for Metal Oxide Semiconductor field emission transistor effect.
- Used in CMOS digital integrated circuit.
- Main advantage over bjt is -
  a) The fabrication technique is simple.
  b) Occupy less space than bjt
  c) power dicipation in case of mosfet is very small as compared to bjt.

MOSFET is a three layer device and four terminal device.
The three layers are-

MOS	Metal (Al)
	Oxide (SiO_2)
	Semiconductor

The first layer is metal layer., second one is oxide and third layer is semiconductor layer.



(n channel)

- A mosfet can be of 2 type-
  a) Enhancement type (Channel has to be created voltage at gate terminal)
  b) Depletion type. (If $V_{GS}=0V$, then also channel is created)

. The enhancement type is of 2 types-

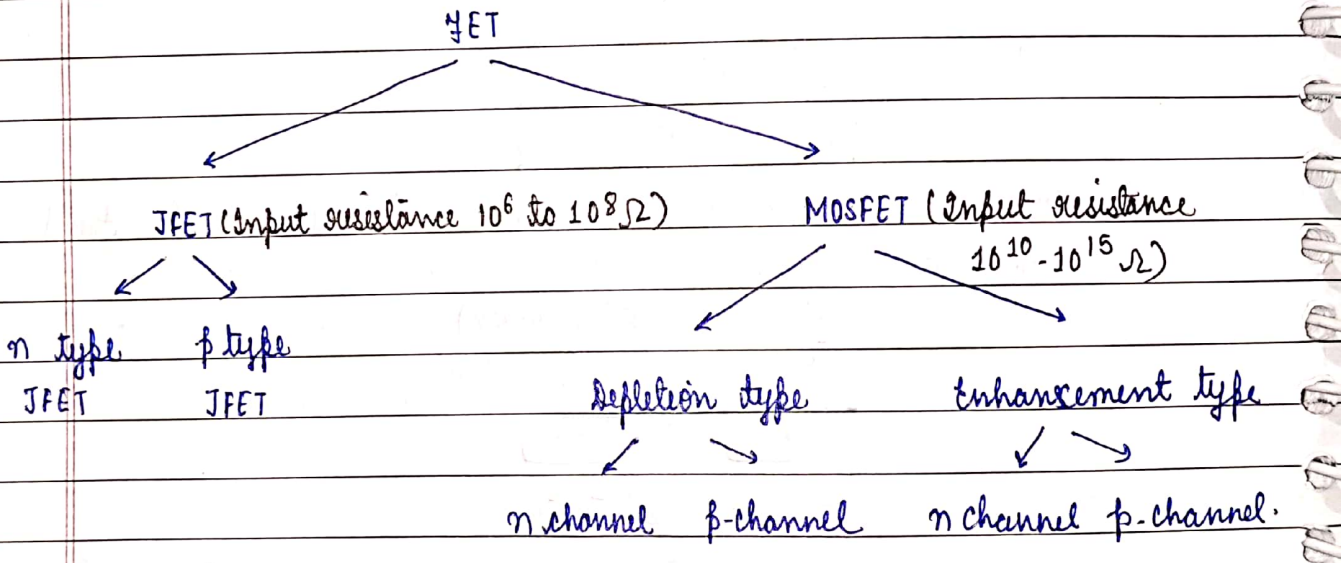
a) n-channel mosfet

b) p-channel mosfet.

In case of N-channel enhancement type mosfet-
Substrate used is p type semiconductor channel is n type.

In case of p channel-
Substrate used is n type and channel will be p type.

tox = thickness of layer (oxide)
L = channel length
W = channel width



. Due to problem of minority charge carriers in which on one hand the main current is affected on the other hand it also caused thermal runaway.

(Imp) Low input impedence (BJT transistor)

. It is a unipolar device means its operation depends only upon the majority charge carriers.

. It requires less power consumption then transistor.

- It's input impedence is very high (MOSFET)
- It's area is also very less so very easy to be used in the IC fabrication.

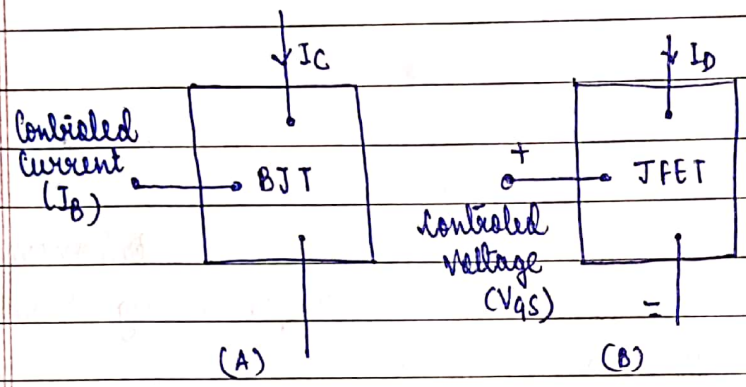
- FET resistance is nearly about 1 mΩ.
- large bandwidth.
- GBW of BJT > GBW of FET.

:Disadvantage:-
offset voltage = 0.
- Smaller gain.

• depletion	enhancement.
• Pre-existing channel	• No pre-existing channel.
• Suitable to operate for both depletion mode and enhancement mode.	• Only operated at enhancement mode.

- (JFET)
It is an unipolar Transistor which act as a voltage control current device.

- FET (Field effect transistor)
- FET is the three terminal unipolar device. It stands for field effect transistor.
- They are used for the application that match to the large extent to the BJT transistor.
- BJT transistor is current controlled device.
  JFET = Voltage Controlled device.



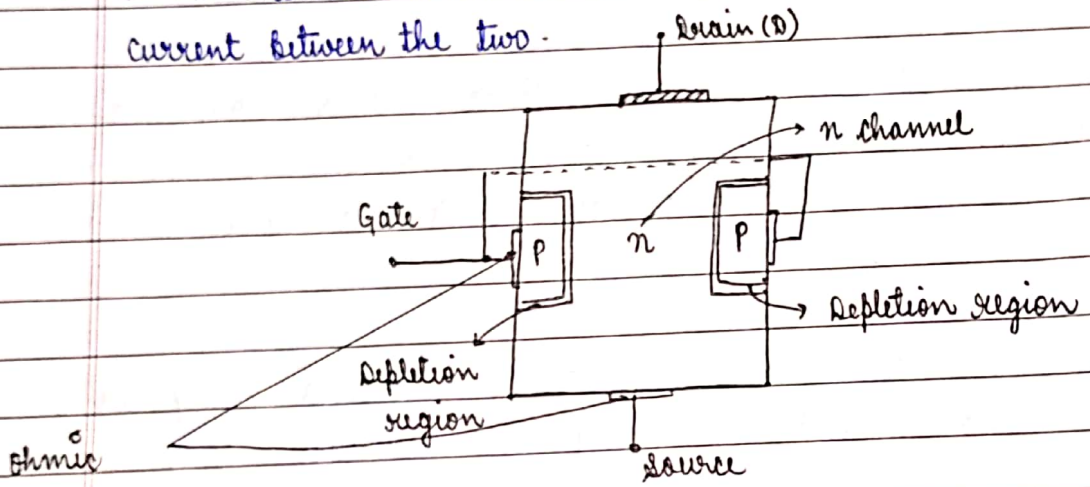
- In figure (A) the current I_C is direct function of level of I_B.
- In figure (B), the current I_D is the function of voltage V_{GS}.
- The device in which current at 2 electrodes is controlled by the action of electric field at pn junction.
- In fet, gate is created by reverse biased junction.
  (MOSFET creates the junction via conductive gate separated from the gate region by a thin insulator)

There are n-channel and p-channel fet. (Bi- denotes the conduction level is a function of two charge carriers).
The fet the conduction depend solely upon electron (n-channel) or holes (in p channel).

- For fet an electric field is established by the charges present that will control the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

- Construction and characteristics of JFET.

→ JFET is 3 terminal device where 1st terminal is capable to control current between the two.



⊗ JFET.

The basic construction of JFET is shown in figure. Major part of the structure is n type material that forms the channel between the embedded p-type material.
The top of the channel is connected through an ohmic contact known as drain., lower end reffered as source. The 2 p-type material are connected through the gate.

∴ The drain and source are connected to the n type channel where as the gate is connected to the 2 embedded p-type material.

∴ Under no potential JFET is under no bias condition with 2 pn junctions.

- The source can be linked to applied voltage from drain to source that will establish the flow of electron from the source. The gate will control the flow of charge to the drain. The drain & source.

i) $V_{GS}=0$ and V_{DS} become positive.

In this case the d a positive voltage V_{DS} has been applied across the channel and gate has been directly attached to the source to have 2 →

① Gate and source terminal are at same potential. ($V_{GS}=0$)

② The depletion region at low end of the p-material is similar to the distribution of the no bias condition.

As V_{DD} or V_{DS} is applied, the e^- will be drawn from the drain terminal to establishing the drain current. The path reveals that drain and source currents are equal to each other ($I_D=I_S$)

Under this condition the flow of charge is solely or unhibited and limited solely by the resistance of n-channel b/w drain & source.