Subject Code: BCS-26

Roll No. 1 0 1 6 0 2 1 1 2 1

B. Tech.
ODD SEMESTER
MINOR TEST 2018 - 2019

**Subject Name: Principles of Operating Systems**

**Time: 2 Hrs.** **Max. Marks: 20**

**Note: Answer all questions.**

**Q.1 Attempt any Three parts of the following. Q. 1(a) is compulsory.**

(a). Consider a program consists of five segments: S0 = 600, S1 = 14 KB, S2= 100KB, S3 =580 KB, and S4 = 96 KB. Assume at that time, the available free space partitions of memory are 1200–1805, 50 –150, 220-234, and 2500-3180. Answer the following questions: 4

I. Draw logical to physical maps and segment table.
II. Allocate space for each segment in memory
III. Calculate the external fragmentation and the internal fragmentation
IV. What are the addresses in physical memory for the following logical addresses:
   i. 0,580
   ii. 1,17
   iii. 2,66
   iv. 3,82
   v. 4,20

(b). After an interrupt occurs, hardware needs to save its current state (content of registers etc.) before starting the interrupt service routine. One issue is where to save this information. Here are two options- 2

I. Put them in some special purpose internal registers which are exclusively used by interrupt service routine.
II. Put them on the stack of the interrupted process.

Briefly discuss the problems with above two options.

(c). The address sequence generated by tracing a particular program executing in a pure demand paging system with 100 bytes per page is- 2

0100, 0200, 0430, 0499, 0510, 0530, 0560, 0120, 0220, 0240, 0260, 0320, 0410.

Suppose that only two frames were allocated to that program and all were empty initially. Find out the number of page faults using LRU and Optimal page replacement algorithms.

(d) Define the following terms in brief 2

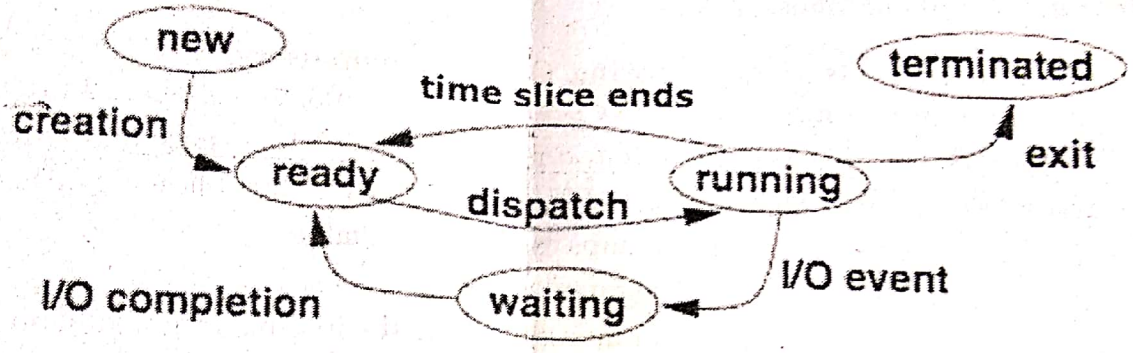
I. Multiprogramming System
II. Multiprocessing System
III. Multitasking System
IV. Realtime System

**Q.2 Attempt any Two parts of the following. Q. 2(a) is compulsory.**

(a). Define monolithic kernel and microkernel in brief. Which of these types of OS structure better satisfies the following requirements? If both are equally as good write both. Justify your answers. 4

- Convenient access to operating system data structures
- Addition of new operating system components.
- Modification of operating system components.
- Security and reliability

(b). Processes go through the following states in their lifetime. 2




Consider the following events and answer the questions that follow. Assume there are 5 processes, all either in the read or running states initially. Assume the processes are using a single processor.

- At time 5: P1 executes a command to read from disk 3.
- At time 15: P3's time slice ends.
- At time 18: P4 executes a command to write to disk 3.
- At time 20: P2 executes a command to read from disk 2.
- At time 24: P3 executes a command to join with P5.
- At time 33: An interrupt occurs indicating that P2's read is complete.
- At time 36: An interrupt occurs indicating that P1's read is complete.
- At time 38: P5 terminates.
- At time 48: An interrupt occurs indicating that P4's write is complete.

For each time 22, 37 and 47, identify which state each process is in. If it is waiting, indicate what it is waiting for?

(c). What is an Operating System? Justify the statement "Operating System can be viewed as a government, resource allocator and a control program". 2

**Q.3 Attempt any Two parts of the following. Q. 3(a) is compulsory.**

(a). Attempt the following questions- 4

I. Consider a new page replacement algorithm in virtual memory with working strategy as following-

- Each page in memory maintains a count which is incremented if the page is referred and no page fault occurs.

- If a page fault occurs, the physical page with zero count or smallest count is replaced by new page and if more than one page with zero count or smallest count then it uses FIFO strategy to replace the page.

Find the number of page faults using above algorithm for the following reference string with Three and Four Frames (assume initially all physical frames are free)
Reference String: A B C D A B E A B C D E B A D .

II. Consider the following two-dimensional array:

int X [64] [64];

Suppose that a system has four-page frames and each frame is 128 words (an integer occupies one word). Programs that manipulate the X array fit into exactly one page and always occupy page 0. The data are swapped in and out of the other three frames. The X array is stored in row-major order (i.e., X [0][1] follows X [0][0] in memory). Which of the two code fragments shown below will generate the lowest number of page faults using LRU? Explain and compute the total number of page faults.

*Fragment A*

```
for (int j=0; j<64; j++)
      for (int i=0; i<64; i++)
            X[i][j] =0;
```

*Fragment B*

```
for (int i=0; i<64; i++)
      for (int j=0; j<64; j++)
            X[i][j] =0;
```

I.

(b). The total access time is 1 nanosecond for a read operation with a TLB hit, 5 nanoseconds for a read operation with a TLB miss, 2 nanoseconds for a write operation with a TLB hit and 10 nanoseconds for a write operation with a TLB miss. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operands write operations. The TLB hit-ratio is 0.9. Find out the average memory access time (in nanoseconds) in executing the sequence of instructions. 2

(c). A Computer system implements 8KB pages and a 32-bit physical address space. Each page table entry contains a valid/invalid bit, a dirty bit and three permission bits, and the translation. If the maximum size of the page table of a process is 24 megabytes. Find out the length of the virtual address supported by the system in bits. 2

BCS-28

Roll No. | | | | | | | | | | |

# B. TECH.
## ODD SEMESTER
## MINOR TEST 2018 – 2019

## Design and Analysis of Algorithms

Time: 2 Hrs. Max. Marks: 20

Note: Answer all questions.

**Q.1 Attempt any Three parts of the following. Q. 1(a) is compulsory.**

(a). (i) Consider the following fragment of code, find its asymptotic time bound: 4

```
for i ← 1 to m
{
  for j ← 1 to i
  {
    set sum ← sum + A[i][j].
  }
}
```

*(ii) Consider the following recurrence:*

$T(n) = 4T(n/2) + n^3$

*Find its asymptotic time bound using Master Method.*

*(b).* *Design an algorithm to find Min. and Max. elements from the given list of numbers simultaneously. You are also required to find the asymptotic time for the designed algorithm.* 2

*(c).* *A thief with knapsack can steal n items. Each item $I_i$ has certain weight $w_i$ and value $v_i$. Maximum capacity of knapsack is W. Design an efficient algorithm which fills the knapsack with maximum possible value. Find out the asymptotic time for the designed algorithm. Find the solution for the following Knapsack problem using your designed algorithm:* 2

| Item($I_i$) | $I_1$ | $I_2$ | $I_3$ |
|---|---|---|---|
| Weight($w_i$) | 80 | 30 | 40 |
| Value($v_i$) | 20 | 15 | 10 |

(d) Design a Radix Sort algorithm to arrange the following sequence of numbers in ascending order: 2

Input: 478, 537, 9, 721, 3, 38, 123, 67

You are also required to analyse the designed algorithm.

**Q.2 Attempt any ~~Three~~ Two parts of the following. Q. 2(a) is compulsory.**

(a). Explain in brief the concept of Heapify with respect to max heap and also write the algorithm. 4

Consider the list

| 5 | 2 | 1 | 7 | 3 | 4 |
|---|---|---|---|---|---|

List--

Construct the Max-heap using bottom up construction of building Max-heap.

(b). Design and analyse Counting Sort algorithm. Consider the following sequence of numbers: 2

6, 5, 11, 4, 3, 7, 8, 10, 9, 1, 16, 15, 4, 2, 11, and 10.

Use designed algorithm to arrange the numbers in ascending order

(c). Explain and write Merge-Sort algorithm. 2

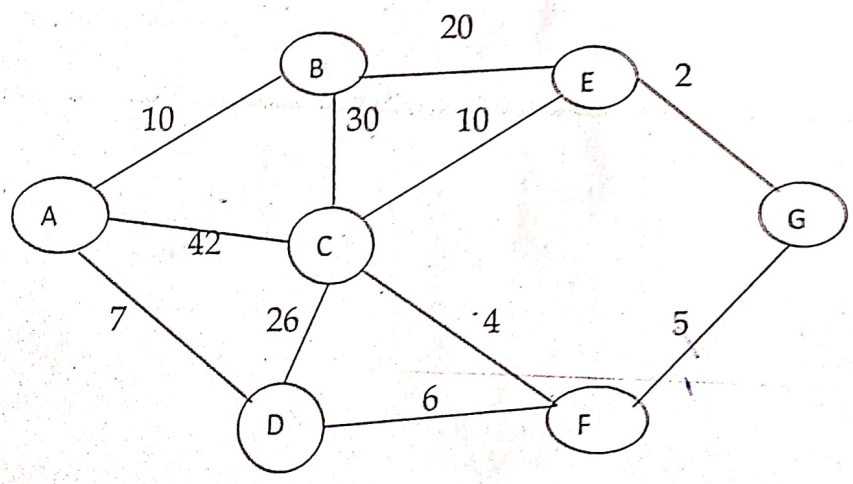
Consider the following sequence of input

5, 2, 4, 6, 1, 3, 2 ,6

Arrange the input sequence in ascending order using Merge-Sort.

**Q.3 Attempt any ~~Three~~ Two parts of the following. Q. 3(a) is compulsory.**

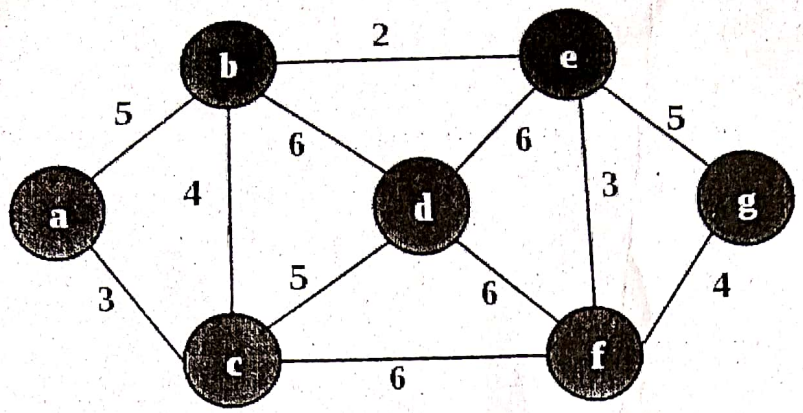
(a). Define minimum cost spanning tree. Write Prim's algorithm to generate a minimum cost spanning tree for any given weighted graph. Generate minimum cost spanning tree for the following graph, using Prim's algorithm 4




2+5+4+42+10

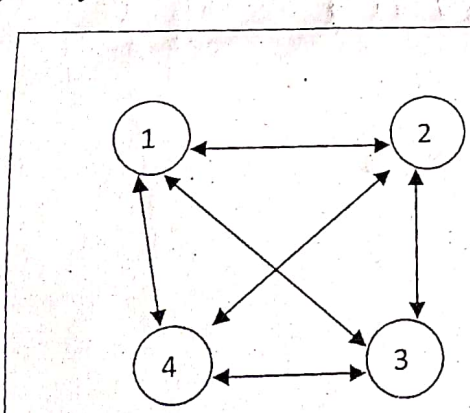
53+10 ⇒ 63

2+5+4+7+10 >

(b). 


Design and analyse an Algorithm for finding shortest path from a fixed node to every other node. Find shortest path from node A to every other node for the graph of above figure using designed Algorithm.

(c). Let G=(V,E) be a directed graph with edge cost cij. The variable cij is defined such that cij>0 for all c and j, and cij= ∞ if (c,j) ε E. Let (V) n and assume n>1. A tour of G is a directed simple cycle that includes every vertex in V. The cost of tour is the sum of cost of the edges on thee tour. The traveling salesman problem is to find a tour of minimum cost. Let g(I,S) be the shortest path starting at vertex I going through all vertices in S and terminating at vertex 1. The function g(1, V-{1}) is the length of an optimal sales person tour. Formulate g(I,S) using dynamic programming solve it for the edge lengths given by matrix: 2




$$\begin{pmatrix} 0 & 10 & 15 & 20 \\ 5 & 0 & 9 & 10 \\ 6 & 13 & 0 & 12 \\ 8 & 8 & 9 & 0 \end{pmatrix}$$

BEC-42

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B. Tech.
SEM-V/VII,ODD SEMESTER
MINOR TEST 2018 - 2019

**Digital Signal Processing**

**Time: 2 Hrs.** **Max. Marks: 30**

**Note: Answer all questions.**

1 **Attempt any Three parts of the following. Q. 1(a) is compulsory.**

(a). What are the basic building blocks for realization of digital system? Develop a direct form I realization of the difference equation 4

$$y(n)= b_0x(n) + b_1x(n-1) + b_2x(n-2) +b_3x(n-3) - a_1y(n-1) - a_2y(n-2) -a_3y(n-3)$$

(b). Compare the direct form I and direct form II realization of IIR systems. Determine the direct form I and II realization for a second-order IIR transfer function. 3

$$H(z)=\frac{1+\frac{1}{3}Z^{-1}}{1-\frac{3}{4}Z^{-1}+\frac{1}{8}Z^{-2}}$$

(c). Design an analog Butterworth filter that has a -10 dB passband attenuation at a frequency of 20 rad/sec and at least 10 dB stopband attenuation at 30 rad/sec. 3

(d) Describe Chebyshev filters. Comment on the passband and stopband characteristics of Chebyshev filter. 3

**Attempt any Three parts of the following. Q. 2(a) is compulsory.**

(a). What are the drawbacks of direct form realization of IIR systems? How do you perform cascaded realization of IIR system? Obtain a cascaded realization of the system characterized by the transfer function 4

$$H(z)=\frac{2(z+2)}{z(z-0.1)(z+0.5)(z+0.4)}$$

(b). Discuss the parallel realization of IIR systems. What are the merits of parallel realization. 3

(c). Determine the parallel realization of the IIR digital filter having transfer functions 3

(i) $H(z)=\frac{3(z^2+5z+4)}{(2z+1)(z+2)}$

(ii) $H(z)=\frac{3z(5z-2)}{\left(z+\frac{1}{2}\right)(3z-1)}$

(d) Consider a causal IIR system with system function 3

$$H(z)=\frac{1+2z^{-1}+3z^{-2}+2z^{-3}}{1+0.9z^{-1}-0.8z^{-2}+0.5z^{-3}}$$

Determine the equivalent lattice- ladder structure and check if the system is stable.

**3 Attempt any Three parts of the following. Q. 3(a) is compulsory.**

(a). Obtained the mapping formula for the impulse invariant transformation. An analog filter have following system function: 4

$$H(s)=\frac{1}{(s+0.2)^2+9}$$

Convert this filter into digital filter using impulse invariant technique. Assume T=1sec.

(b). What is bilinear transformation? Compare bilinear transformation with impulse invariant transformation based on their stability. 3

(c). Convert the analog filter with system function: 3

$$H(s)=\frac{s+0.1}{(s+0.1)^2+9}$$

Into a digital IIR filter using bilinear transformation. The digital filter should have a resonant frequency of $\omega_r = \frac{\Pi}{2}$.

(d) Design a Chebyshev filter with a maximum passband attenuation of 2.5 dB at $\Omega_p$=20 rad/sec and the stopband attenuation of 30 dB at $\Omega_s$=50 rad/sec. 3

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B.Tech.

Semester: ODD (5th)

Minor Examination, 2018-19

Computer Graphics (Code: BCS-27)

Time: 2.00 Hrs | Maximum Marks: 20

1. Attempt any three parts of the following. Question number 1(a) is compulsory.
   (a) Compare DVST with Shadow Mask CRT in terms of theirconstruction and functioning. Comment on their relative performance with justifications. (4)
   (b) How are picture actually stored and displayed on a raster scan display device? (2)
   (c) What are advantages of concatenation of 2D transformations? Prove that concatenation of 2D transformations is not commutative. (2)
   (d) Write notes on positioning techniques. (2)
2. Attempt any two parts of the following. Question number 2(a) is compulsory.
   (a) Explain with suitable example the principle of Bresenham's circle generating algorithm. (4)
   (b) Describe construction and functioning of Light-Pen. (2)
   (c) Write Symmetrical DDA for line drawing. Use it to compute the co-ordinates of points to be plotted to draw a line AB where A(1,3), B(3,7). (2)
3. Attempt any two Parts of the following. Question number 3(a) is compulsory.
   (a) What is event handling? Describe the role of polling task and event queue in the process of event handling. (4)
   (b) Write midpoint subdivision line clipping algorithm and explain it with an example that is suitable enough to cover all the cases of line clipping. (2)
   (c) Explain Polygon clipping algorithm with an example of a concave polygon. Show all intermediate polygons. (2)

**Q. 1** Attempt any **Three** parts of the following. Q. **1 (a)** is compulsory.

(a) How does the study of managerial economics help a business manager in decision making? Illustrate your answer with examples from production and pricing issues. **(04)**

(b) Discuss the nature and scope of managerial economics. How is it related to other disciplines? **(03)**

(c) What is the purpose of demand forecasting? Give short term objectives of demand forecasting. Briefly explain any two methods of forecasting. **(03)**

(d) What are the determinants of demand? Explain. **(03)**

**Q. 2** Attempt any **three** parts of the following. Q. **2 (a)** is compulsory.

(a) What are the operation issues in business management? How does microeconomics contribute to decision-making in the operational issues? **(04)**

(b) In what respects macro economics is different from micro economics? Discuss. **(03)**

(c) What are the major macroeconomic issues related directly to business decision making? What is

BCS-29

Roll No. 2 0 1 6 0 2 1 1 2 1

B.Tech (Computer Sc & Engineering) VI Semester

Minor Test 2018-2019

**Subject: BCS-29 (Advanced Computer Architecture)**

Time: 2 Hrs. Max Marks: 30

**Note: Attempt ALL questions. Each question carries equal marks**

Q1. Attempt any **Three** of the following. Q.1(a) is compulsory. 4+3+3

a) Discuss the Classification of Instruction Set Architectures. Give the code to compute the function f=(a-b)/(c-d*e) through various Instruction Set Architectures.

b) Explain how instruction set, compiler technology, memory hierarchy affect the CPU performance and justify the effects in terms of program length, clock rate and effective CPI.

c) Give various architectural classification schemes for parallel computer. Also discuss the Sima's classification in detail.

d) Consider the execution of an object code with 200,000 instructions on a 40 MHz processor. The program instruction mix is as follows:

| Instruction Type | CPI | Instruction mix |
|---|---|---|
| Arithmetic and logic | 1 | 60% |
| Load/Store with cache hit | 2 | 18% |
| Branch | 4 | 12% |
| Memory reference with cache miss | 8 | 10% |

a. Calculate the average CPI when program is executed on uniprocessor with the above trace result.

b. Calculate the corresponding MIPS rate based in the CPI obtained.

Q2. Attempt any Three of the following. Q.2(a) is compulsory. 4+2+2

a) Consider the following instruction sequence:

S1: A = B + C
S2: C = D + E
S3: F = G + E
S4: C = A + F
S5: M = G + C
S6: A = L + C
S7: A = E + A

a. Analyze the given instruction sequence for parallelism and draw the dependence graph.

b. Identify the degree of parallelism available and give the Data Flow for parallel execution considering two functional units for memory operation and two functional unit for arithmetic operation.

b) Discuss the mismatch between software parallelism and hardware parallelism with the help of suitable example.

c) Explain various types of hazards in implementation of instruction pipeline. Also comment on the techniques to resolve the such hazards.

Q3. Attempt any Three of the following. Q.3(a) is compulsory. 4+2+2

a) Discuss the synchronous and asynchronous models of linear pipeline, its Clocking and Timing Control. Also derive formula to compute the Speedup, Efficiency, and Throughput of linear pipeline.

b) Consider the following reservation table for a four-stage pipeline with a clock cycle $\tau$= 20 ns.

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| S1 | X | | | | | X |
| S2 | | X | | X | | |
| S3 | | | X | | | |
| S4 | | | | X | X | |

I. What are the forbidden latencies and the initial collision vector?

II. Draw the state transition diagram for scheduling the pipeline.

III. Determine the Minimum Average Latency(MAL) associated with the shortest greedy cycle.

c) Design a binary integer multiply pipelines with five stages is for partial product generation. The last stage is a 36-bitr carry-lookahead adder. The middle three stages are made of 16 carry-save adders of appropriate lengths.

I. Prepare a schematic design of the five stage multiply pipeline. All lines widths and inter-stages must be shown.

II. Determine the maximal clock rate of the pipeline if the stage delays are $\tau 1 = \tau 2 = \tau 3 = \tau 4$ =90 ns, $\tau 5$= 45 ns, and the latch delay is 20 ns.

MBA-02

Roll No. | | | | | | | | | | |

**B. Tech.**
**ODD SEMESTER (V)**
**Minor Examination: 2018-19**
**Engineering and Managerial Economics**

**Time: 2 Hrs.** **Max. Marks: 30**

**Note: Answer all questions.**

**Q. 1** Attempt any **Three** parts of the following. Q. **1 (a)** is compulsory.

**(a)** How does the study of managerial economics help a business manager in decision making? Illustrate your answer with examples from production and pricing issues. **(04)**
**(b)** Discuss the nature and scope of managerial economics. How is it related to other disciplines? **(03)**
**(c)** What is the purpose of demand forecasting? Give short term objectives of demand forecasting. Briefly explain any two methods of forecasting. **(03)**
**(d)** What are the determinants of demand? Explain. **(03)**

**Q. 2** Attempt any **three** parts of the following. Q. **2 (a)** is compulsory.

**(a)** What are the operation issues in business management? How does microeconomics contribute to decision-making in the operational issues? **(04)**
**(b)** In what respects macro economics is different from micro economics? Discuss. **(03)**
**(c)** What are the major macroeconomic issues related directly to business decision making? What is their significance in business decision? **(03)**
**(d)** "The job a managerial economist concentrates on taking business decisions and formulating forward plans." Expand this statement. **(03)**

**Q. 3** Attempt any **Three** parts of the following. Q. **3 (a)** is compulsory.

**(a)** What are the possible consequences if a large-scale firm places its product in the market without having estimated the demand for its product? **(04)**
**(b)** What is the law of demand? Explain with the help of demand schedule and demand curve. What are the exceptions to this law? **(03)**
**(c)** Describe the impact of rise in income on normal goods and inferior goods. **(03)**
**(d)** What are the uses of the concept of elasticity of demand? Explain. **(03)**