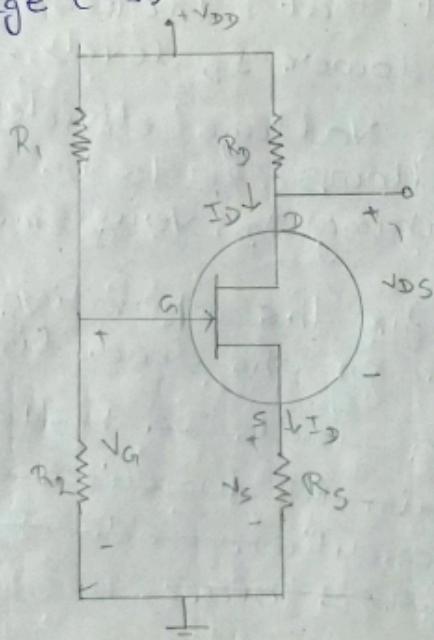


Assignment No:- 02

Q:- Give the advantage of voltage divider bias compared to self bias.

voltage divider bias circuit combines the use of a source resistor (R_s) with a gate bias voltage (V_{GS}). The gate bias voltage is derived from the supply voltage by means of the voltage divider (R_1 and R_2), and the source voltage (V_s) depends upon R_s and I_D .



The gate terminal and the source terminal are both positive with respect to ground, and the gate source voltage (V_{GS}) is the difference between V_G and V_s . Because V_s is larger than V_G , the FET source terminal is at a higher level than the gate. So, the gate is negative with respect to the source, and the gate-channel junctions are biased.

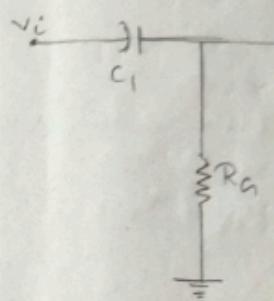
As in the case of a self-biased circuit, the voltage drop across R_S increases if I_D increases. This produces an increase in $-V_{GS}$, which drives I_D back towards its original level. Decrease in I_D causes a reduction in $-V_{GS}$ which tends to increase I_D .

- For the self-bias circuit, it was seen that increasing the resistance of R_S brings $I_{D(max)}$ and $I_{D(min)}$ closer together, but that increased R_S values result in lower I_D levels.
- ~~As~~ Voltage divider Bias circuit allows R_S to be increased without making I_D very small.

- we can fix the operating point anywhere on the load line.
- By using single DC battery we can maintain EB junction in forward bias condition and CB junction in reverse bias

Question:- Explain the self-bias arrangement in FET & calculate the Q-Point.

The self-bias configuration eliminates the need for two DC supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration.



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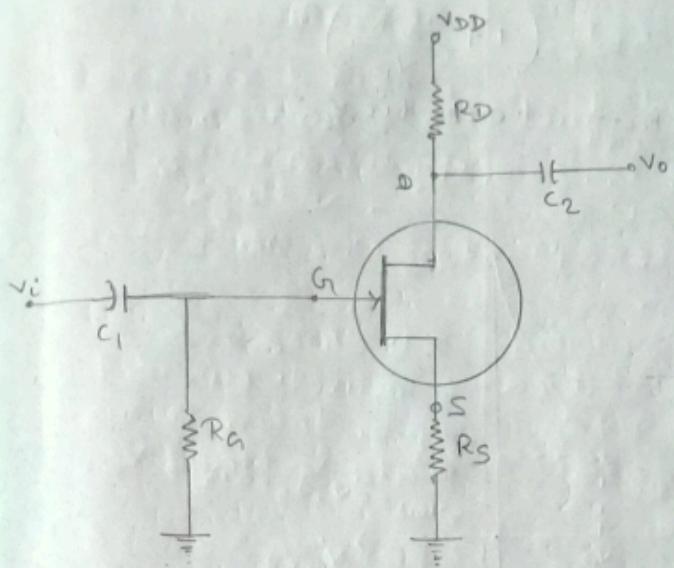
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For the dc analysis, the capacitors can be replaced by open circuit and Resistor R_g Replaced by a short circuit. Since $I_g = 0 \text{ A}$.

The current through R_s is the source current I_s ,

$$I_s = I_D$$

and

$$V_{RS} = I_D R_s$$

for the closed loop

$$-V_{GS} - V_{RS} = 0$$

$$V_{GS} = -V_{RS}$$

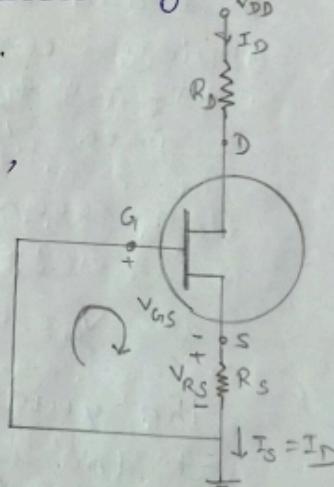
$$V_{GS} = -I_D R_s$$

→ ① DC analysis of the self-bias Configuration

A mathematical solution could be obtained simply by substituting eqn: ① into Shockley's equation as follows:-

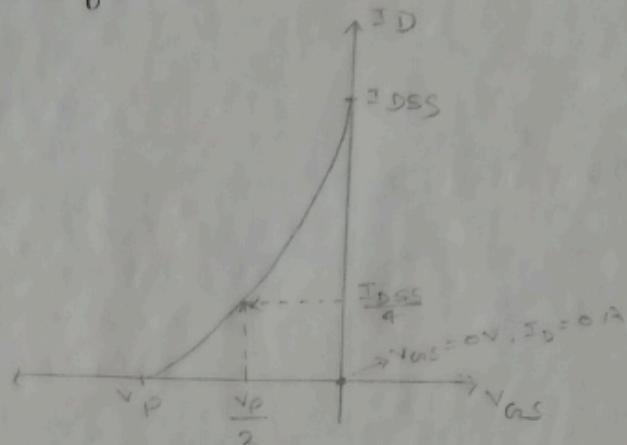
$$I_D = I_{DS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

$$= I_{DSS} \left(1 - \frac{-I_D R_s}{V_p} \right)^2$$



$$I_D = I_{DSS} \left(1 + \frac{V_D R_S}{V_P} \right)^2$$

transfer characteristics:-



Identify two points on the graph that are on the line. the most obvious condition to apply is

$$I_D = 0A$$

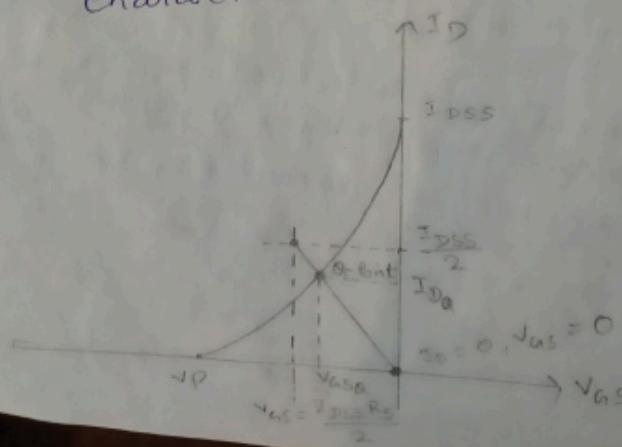
$$\text{since } V_{GS} = -I_D R_S = 0V$$

The second point is

$$I_D = \frac{I_{DSS}}{2}$$

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

the quiescent point obtained at the intersection of the straight line plot and the device characteristic curve.



Question:-

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V_{DS} can be determined by applying Kirchoff's voltage law to the output circuit.

$$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{RS} - V_{RD} = V_{DD} - I_S R_S - I_D R_D$$

$$\text{Since } I_S = I_D$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

$$V_S = I_D R_S$$

Question:- What is the difference between enhancement type & depletion type MOSFET?

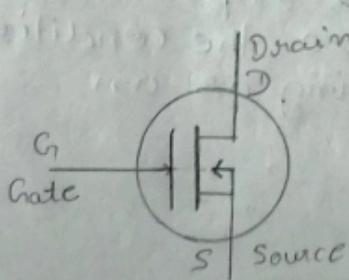
MOSFET:-

MOSFET is known as Metal Oxide Semiconductor field effect Transistor. It is a type of FET that has an insulated metal oxide layer between its gate and channel.

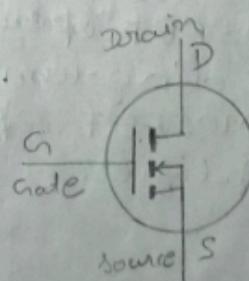
The plus point of the insulated gate is its superior speed and performance with very little leakage current.

MOSFET are two types:-

1. Enhancement type
2. Depletion type



Depletion MOSFET



Enhancement MOSFET

Depletion MOSFET

- The type of MOSFET where the channel depletes with the gate voltage is known as depletion MOSFET.
- It conducts current between its source and drains when there is no gate voltage V_{GS} .
- Applying reverse voltage to the gate reduces the channel width.
- It is a normally ON transistor.
- There is no threshold voltage for switching ON the MOSFET.
- Diffusion or subthreshold current does not exist.

Enhancement MOSFET

where the channel is enhanced or induced using the gate voltage is known as E-MOSFET

It does not conduct current when there is no gate voltage V_{GS} .

Applying reverse voltage does not affect E-MOSFET since there is no channel.

It is normally off transistor.

There is a threshold voltage at which the MOSFET switches ON.

E-MOSFET has sub-threshold current leakage between the

Question:- What are the regions of an MOSFET operations explain with $V-I$ diagram. Also the condition of MOSFET operating as an amplifier.

Operating region of MOSFET :-

A MOSFET is seen to exhibit three operating region.

1. Cut-off region
2. Ohmic region
3. Saturation region.

Cut-off Region:-

Cut-off region is a region in which the MOSFET will be off as there will be no current flow through it. In this region, MOSFET behaves like an open switch and is thus used when they are required to function as electronic switches.

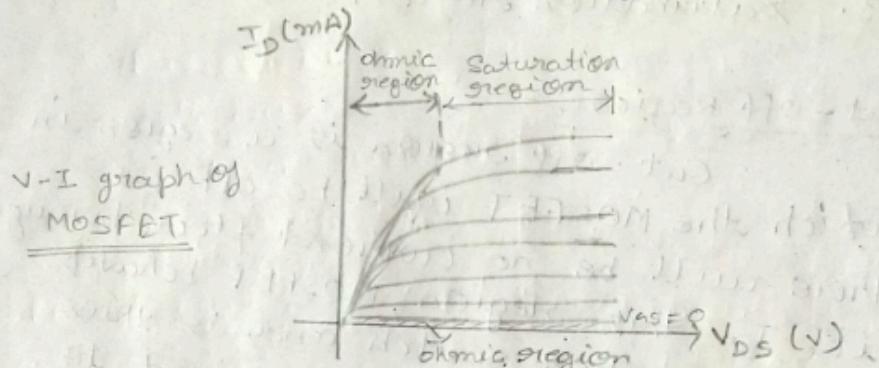
Ohmic or Linear Region:-

Ohmic or linear region is a region where the current I_{DS} increases with an increase in the value of V_{DS} . When MOSFET are made to operate in this region, they can be used as amplifiers.

Saturation Region:-

In saturation region, the MOSFETs have their I_{DS} constant inspite of an increase in V_{DS} and occurs once V_{DS} exceeds the value of Pinch-off voltage V_P .

Under this condition, the device will act like a closed switch through which a saturated value of I_{DS} flows. As a result, this operating region is chosen whenever MOSFET are required to perform switching operations.



MOSFET as an amplifier:-

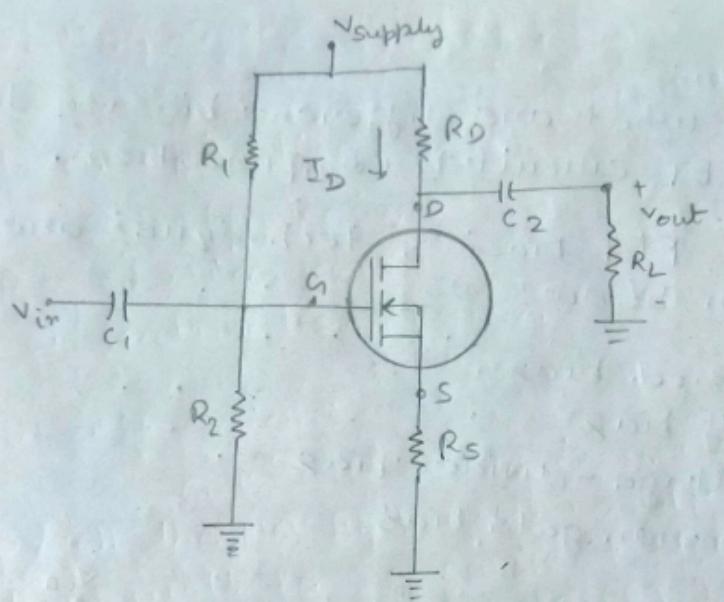
For a MOSFET to operate as a linear amplifier, we need to establish a well-defined quiescent operating point, or Q-point, so it must be biased to operate in its saturation region. The Q-point for the mosfet is represented by the DC values, I_D and V_{GS} that position the operation point centrally on the MOSFETs output characteristics curve.

V_{GS}

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$$V_{GS} = V_{Supply} \times \frac{R_1}{R_1 + R_2}$$

The values of R_1 and R_2 are generally large in order to increase the input impedance of the amplifier and to decrease the ohmic power losses.

Input and output voltage:-

$$V_{in} = V_{GS} \times (1 + g_m R_s)$$

$$V_{out} = -R_D \times I_D = -g_m V_{GS} R_D$$

Voltage gain:-

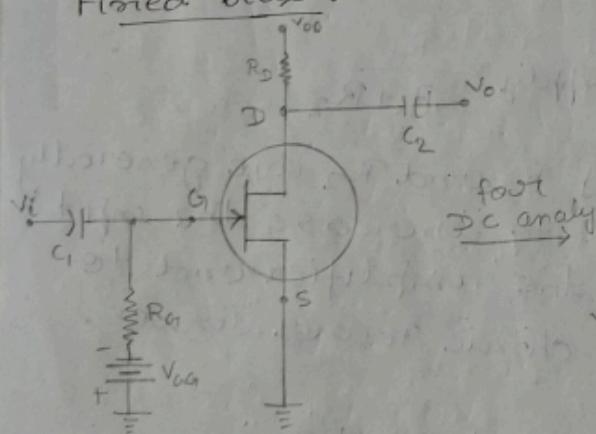
$$A_v = -\frac{R_D}{R_S + \frac{1}{g_m}}$$

Question:-
what are different biasing techniques in FET circuit? compare them.

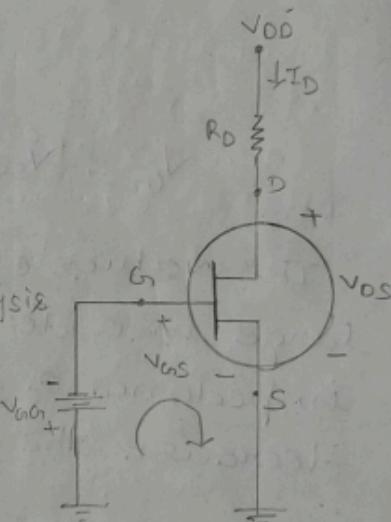
FET biasing techniques are given below:-

1. Fixed bias
2. Self bias
3. Voltage - divider bias
4. Common gate bias

Fixed bias :-



fixed-bias configuration



DC analysis of Fixed-bias

for the dc analysis current through gate (I_g) is zero.

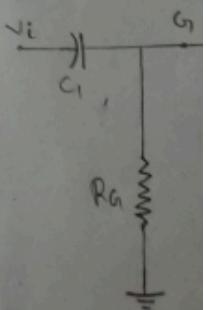
$$I_g \approx 0$$

$$V_{RG} = I_g R_G = 0$$

R_G is replaced by short circuit.

applying KVL at input side.

$$+V_{GGS} + V_{GS} = 0$$



$$V_{GS} = -V_{G1}$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

Drain-to-Source Voltage.

$$V_{DS} = V_{DD} - I_D R_D$$

$$\therefore V_S = 0$$

$$V_{DS} = V_D - V_S$$

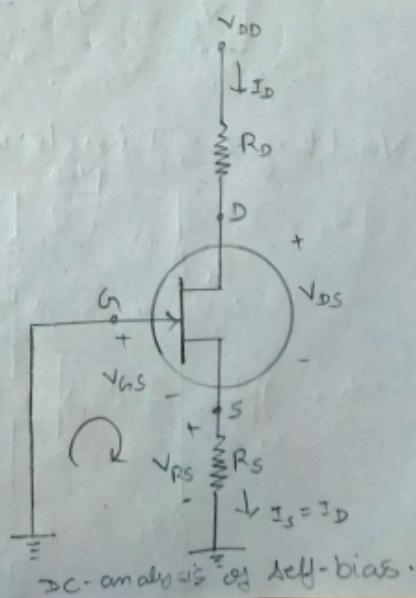
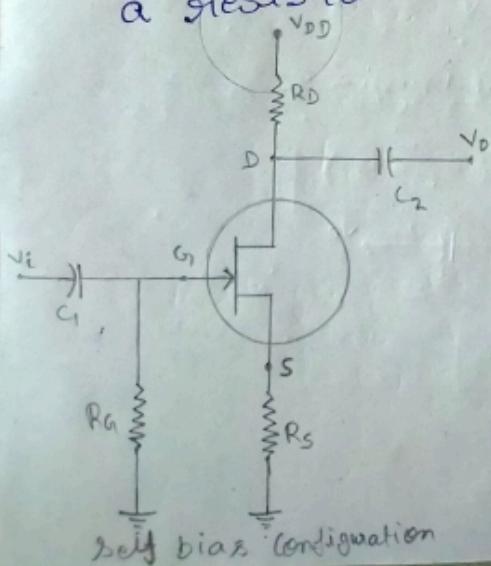
$$V_D = V_{DS}$$

$$V_{GS} = V_G - V_S$$

$$V_G = V_{GS}$$

Self-bias :-

The self-bias configuration eliminates the need for two DC supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S .



since $I_{Gn} = 0A$

$$V_{RGn} = 0$$

R_G will be short circuited.

$$+ V_{GS} + V_{RS} = 0$$

$$\boxed{V_{GS} = -V_{RS}}$$

Voltage across R_S

$$V_{RS} = I_S R_S$$

$$\therefore I_S = I_D$$

$$V_{RS} = I_D R_S$$

$$\boxed{V_{GS} = -I_D R_S}$$

$$V_{DS} = V_{DD} - I_D R_D - I_S R_S$$

$$= V_{DD} - I_D R_D - I_D R_S$$

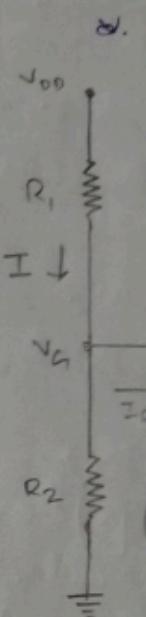
$$\boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)}$$

$$\boxed{V_S = I_D R_S}$$

$$\boxed{V_G = 0V}$$

$$\boxed{V_D = V_{DD} - I_D R_D}$$

for DC and



$$I =$$

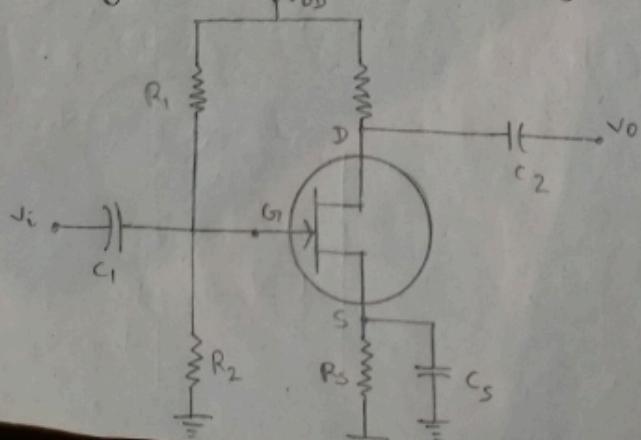
$$V_G =$$

$$\boxed{V_G}$$

using

$$V_G$$

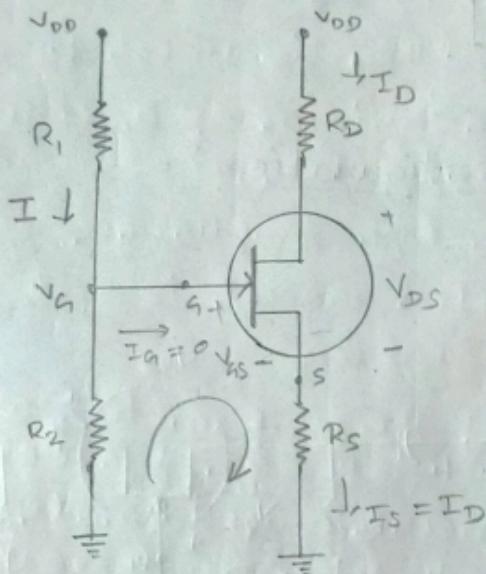
Voltage-Divider Biasing:-



for DC analysis

$$I_G \equiv 0$$

$$\therefore I_{R_1} = I_{R_2}$$



$$I = \frac{V_{DD}}{R_1 + R_2}$$

$$V_G = V_{DD} - IR_1$$

$$= V_{DD} - \frac{R_1 V_{DD}}{R_1 + R_2}$$

$$\boxed{V_G = \frac{R_2 V_{DD}}{R_1 + R_2}}$$

using KV L

$$V_G - V_{GS} - I_S R_S = 0$$

$$V_{GS} = V_G - I_S R_S$$

$$\boxed{V_{GS} = V_G - I_D R_S}$$

$$\left\{ \begin{array}{l} I_S = I_D \\ \because I_G = 0 \end{array} \right.$$

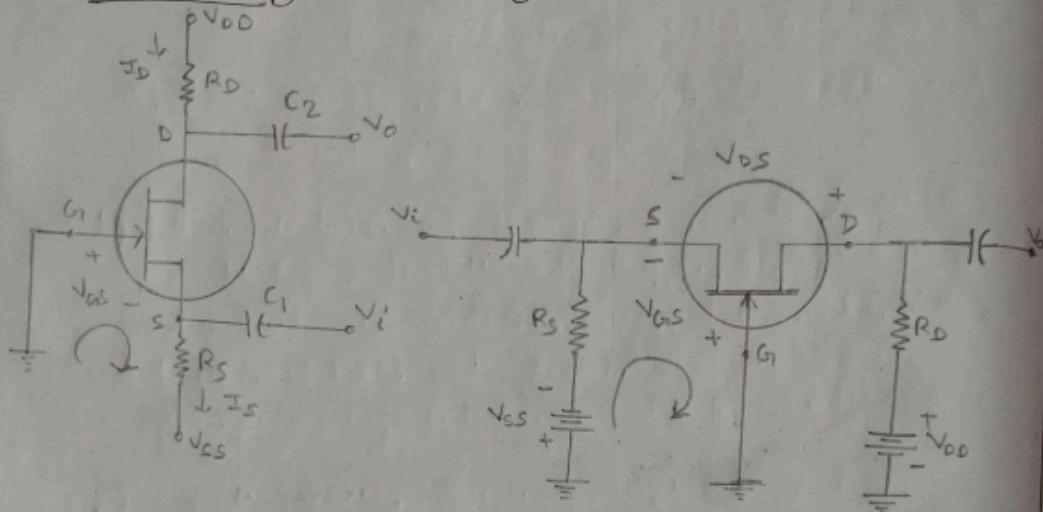
$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

Question:
With
experience
of a
transistor
to
find
the
current
and
voltage
relations.

Common-gate Configuration:



$$V_{SS} - I_S R_S - V_{GS} = 0$$

$$V_{GS} = V_{SS} - I_S R_S$$

$$\boxed{V_{GS} = V_{SS} - I_D R_S} \quad \left\{ I_S = I_D \right.$$

$$I_D = I_S$$

$$\frac{dI_D}{dV_{GS}} = \frac{dI_S}{dV_{GS}}$$

$$= I_{DS}$$

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$$

$$V_{DD} - I_D (R_D + R_S) + V_{SS} - V_{DS} = 0$$

$$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D (R_D + R_S)}$$

$$\boxed{V_D = V_{DD} - I_D R_D}$$

$$\boxed{V_S = -V_{SS} + I_D R_D}$$

$$\frac{dI_D}{dV_{GS}} =$$

$$g_m$$

$$g_m$$

$$g_m$$

Question:-

With suitable diagram derive an expression for maximum transconductance of an MOSFET (n-channel).

Transconductance is the ratio of gate change in gate current due to change in gate to source voltage. It is denoted by g_m . Unit of g_m is 'Siemens'.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_m = \frac{d I_D}{d V_{GS}}$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2, g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

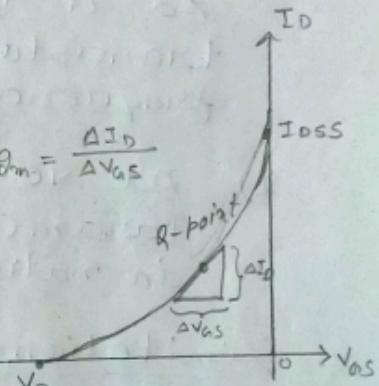
$$\frac{d I_D}{d V_{GS}} = \frac{d}{d V_{GS}} \left[I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \right]$$
$$= I_{DSS} \times 2 \left(1 - \frac{V_{GS}}{V_P}\right) \left(-\frac{1}{V_P}\right)$$

$$\frac{d I_D}{d V_{GS}} = 2 \frac{I_{DSS}}{|V_P|} \left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = \frac{d I_D}{d V_{GS}}$$

$$g_m = \frac{2 I_{DSS}}{|V_P|} \left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_{m0} = \frac{2 I_{DSS}}{|V_P|}$$



Q: why h-Parameter model is not suitable at high frequencies? what is limitation of hybrid π -model?

h-Parameter is used to decide nature and behaviour of a circuit containing transistor.

But for high frequencies analysis of h-Parameter model is not suitable for following reason.

- 1) The value of h-Parameters are not constant at high frequency. So it is necessary to analyze transistor at each and every frequency which is impractical.
- 2) At very high frequency h-Parameters become complex in nature.

Limitations of hybrid π -model :-

1. It is only used for analyzing the small-signal behavior of transistor.
2. It is applied only to device in active mode. D.C. biases are applied to set the Q-point.
3. For higher frequency operation, interelectrode capacitances and other parasitic elements are required.

Question:-

Explain
amplifier
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V_{in} → H → V_{out}

character

Input and

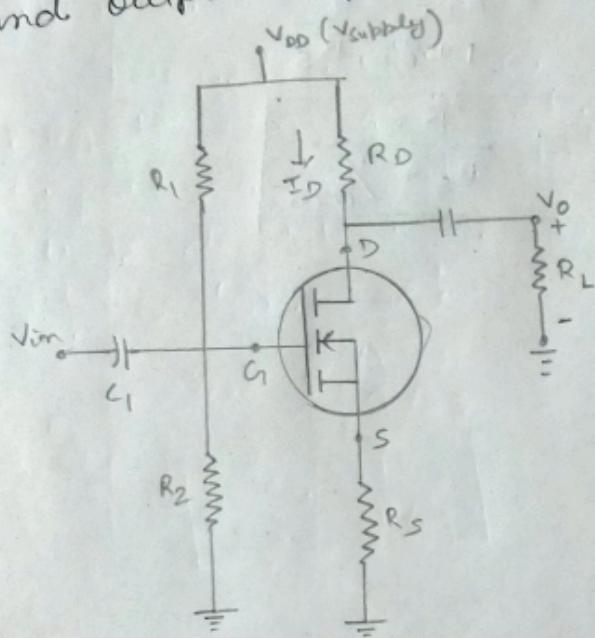
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Question:-

Explain the characteristics of MOSFET amplifier in respect to A_v , g_m , input and output impedance.



MOSFET amplifier :-

characteristics of MOSFET amplifier :-

Input and output voltages :-

$$V_{in} = V_{GS} \times (1 + g_m R_s)$$

$$V_{out} = -R_D \times I_D = -g_m V_{GS} R_D$$

Voltage gain (A_v)

The voltage gain is given from the ratio of output voltage and Input voltage.

$$A_v = \frac{V_o}{V_{in}}$$

$$A_v = -\frac{g_m V_{AS} R_D}{V_{AS} (1 + g_m R_S)}$$
$$= -\frac{g_m R_D}{1 + g_m R_S}$$

$$A_v = -\frac{R_D}{R_S + \frac{1}{g_m}}$$

Combin