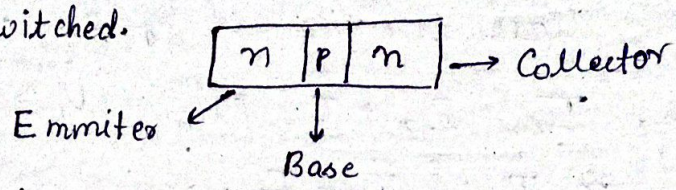
Lecture 11

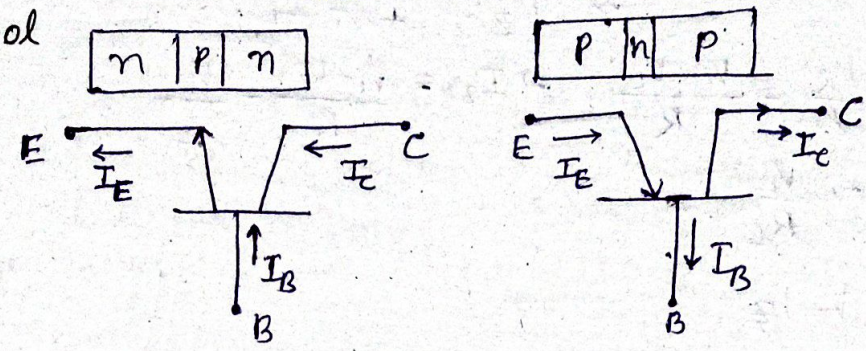
Bipolar Junction Transistor (BJT) is a Bipolar device because electrons and holes both act as charge carrier.

It consists of two p-n Junctions. [n | p | n] [p | n | p]

It is a three terminal bipolar device and centre part is sandwitched.



Symbol



Operation of BJT [E | B | C]

Biasing Voltage defines operation of BJT.

Emmiter Based Junction	Collector Based Junction	Mode of Operation
Forward Base (low R)	Reverse Biasing (high R)	Active region
Forward Bias	Forward Bias	Saturation
Reverse Bias	Reverse Bias	Cutt off Mode

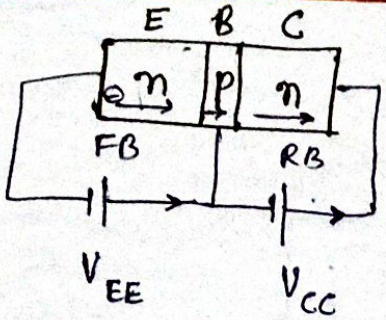
Transistor is used for Amplification and has to operate in Active region for this purpose.

Types of BJT Configuration

(I) Common Base (II) Common Emitter (III) Common Collector

(I) Common Base BJT Configuration Base is common to input and output.

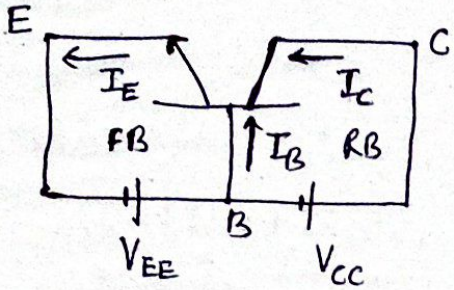
E terminal is heavily doped. B terminal is lightly doped. C terminal is moderately doped. Base terminal is very thin. Collector's width ≥ Emmiter's width.



It is in Active Region.

$I_E = I_B + I_C$

since only 5% $e^{\ominus}$ combines with holes of Base terminal ∴ I_B is very small and remaining $e^{\ominus}$ from E terminal goin collector terminal.



We'll get high value of output Voltage due to high R.

Current amplification factor, $\alpha = \frac{I_C}{I_E}$ Since $I_E = I_B + I_C \Rightarrow I_E > I_C$

∴ $\alpha < 1$.

Actually, $0.9 < \alpha < 0.99$

By ↓ing I_B, α ↑es. If Base region is lightly doped.

Relationship b/w output and input current

$$I_C = \underbrace{\alpha I_E}_{\text{due to Majority Carriers}} + \underbrace{I_{leakage}}_{\text{due to R.B. of collector Based Junction}}$$

when $I_E = 0$, $I_{leakage} = I_{CBO}$

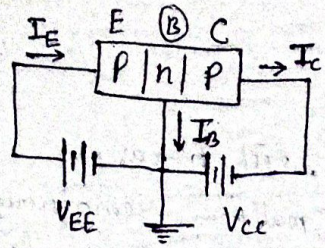
$$I_C = \alpha I_E + I_{CBO}$$

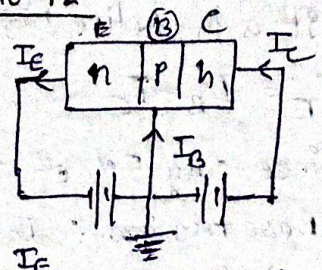
$$I_C = \alpha (I_B + I_C) + I_{CBO}$$

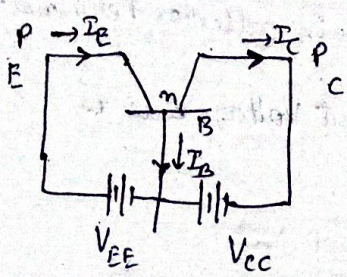
$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

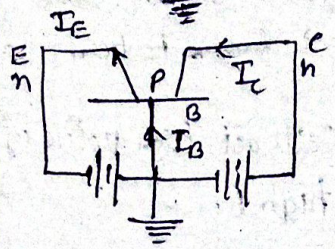
$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}.$$

Lecture 12

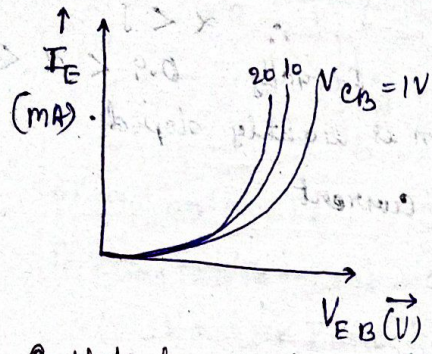








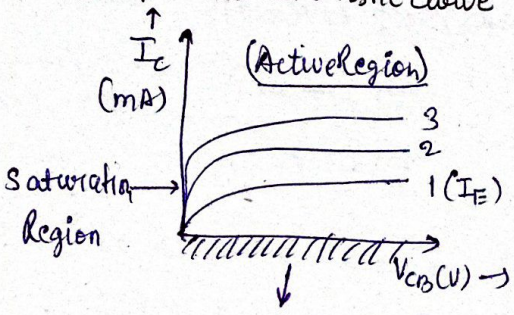
Input characteristic curve is input current vs. input voltage for different values of V_{CB}.



Input Resistance, $r_i = \left.\dfrac{\Delta V_{EB}}{\Delta I_E}\right|_{\text{constant value of } V_{CB}}$

r_i is very small.

Output characteristic curve



Output Resistance, $r_o = \left.\dfrac{\Delta V_{CB}}{\Delta I_C}\right|_{\text{Const val of } I_E}$

ΔI_C is very small; for a large change in V_{CB}, I_C is almost constant so r_o is very high. ($\approx K\Omega$)

Collector current in Common Base conf.

$I_E = I_B + I_C$

$\alpha = \dfrac{I_C}{I_E}$ — current amplification factor

$I_C = \alpha I_E + I_{CBO}$

If $I_E = 0$; $I_C = I_{CBO}$ where I_{CBO} is Reverse leakage current b/w Collector and base when emmiter is open.

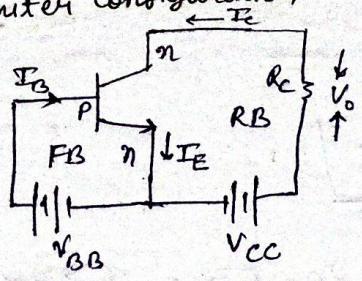
$I_C = \alpha (I_B + I_C) + I_{CBO}$

$= \alpha I_B + \alpha I_C + I_{CBO}$

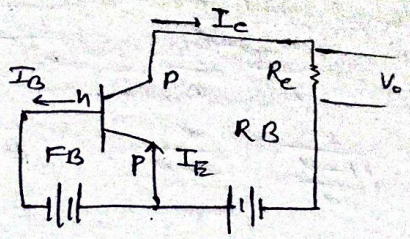
$I_C (1-\alpha) = \alpha I_B + I_{CBO}$

$I_C = \dfrac{\alpha}{1-\alpha} I_B + \dfrac{I_{CBO}}{1-\alpha}$

Common Emmiter Configuration

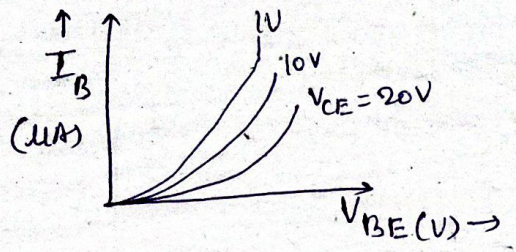


npn CE config.

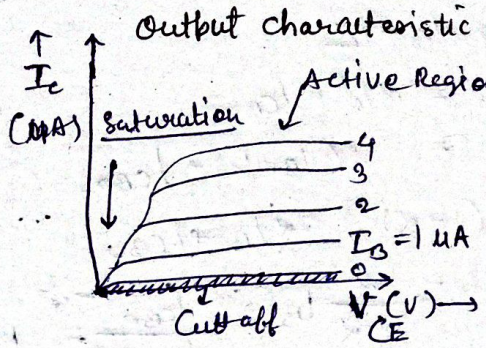


pnp CE config.

Input characteristic curve



Output characteristic curve



$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{\text{constant val of } V_{CE}}$$

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{constant}}$$

As compared to CB conf,

r_i is high b/c I_B is in μA.

lesser r_o as compared to CB Confi.

'β' is current amplification factor in CE configuration.

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{\text{output current}}{\text{Input current}} \qquad \beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = K}$$

$$\alpha_{dc} = \frac{I_C}{I_E}$$

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = K}$$

Relation b/w α and β

$$\beta = \frac{\Delta I_C}{\Delta I_B} \qquad I_E = I_B + I_C$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \qquad \Delta I_B = \Delta I_E - \Delta I_C \quad \text{——— (A)}$$

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_C / \Delta I_C}{\frac{\Delta I_E}{\Delta I_C} - \frac{\Delta I_C}{\Delta I_C}} = \frac{1}{\frac{1}{\alpha} - 1} \qquad \text{——— (B)}$$

$$\beta = \frac{1}{\frac{1-\alpha}{\alpha}} = \frac{\alpha}{1-\alpha} \qquad \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

Since $0.9 < \alpha < 0.99$ $\therefore \beta \approx 20 - 500$; $\beta >> \alpha$

Collector current in CE configuration

$$I_E = I_B + I_C$$

$$I_C = \alpha I_E + I_{CBO}$$

$$= \alpha (I_B + I_C) + I_{CBO}$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha} = \beta I_B + \frac{I_{CBO}}{1-\alpha}$$

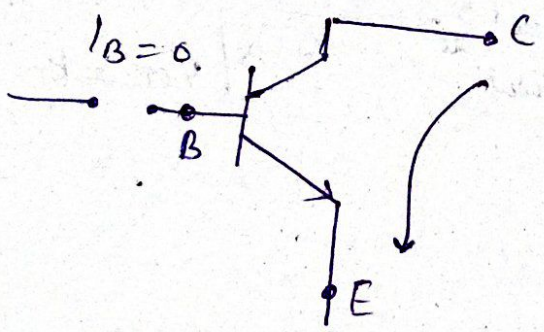
If $I_B = 0$

$$I_C = \frac{I_{CBO}}{1-\alpha}$$

Reverse leakage current b/w collector and Emmiter when Base is open.

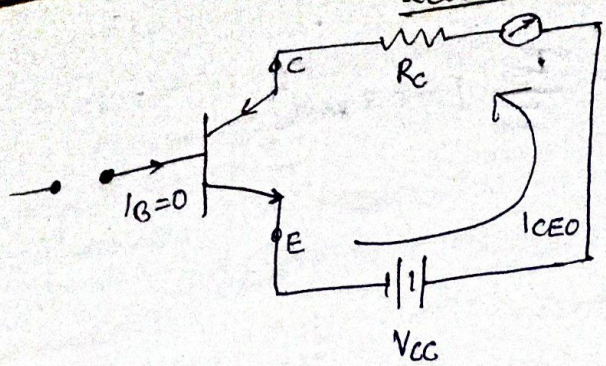
$$I_C = \beta I_B + I_{CEO} \qquad \therefore \boxed{I_{CEO} = \frac{I_{CBO}}{1-\alpha}}$$

$$\therefore I_{CEO} >> I_{CBO}$$



$$I_C = I_{CEO}$$

Lecture 13

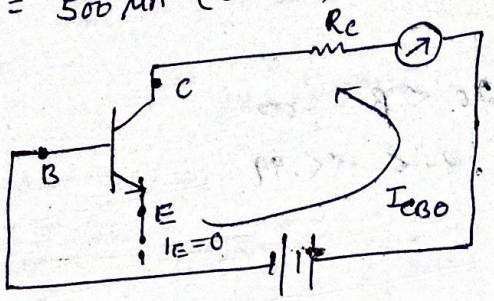


If reverse leakage current, I_{CEO} is very high then transistor is damaged.

Common Emitter Config.

$I_{CEO} = 20\,\mu A$ (Si BJT)

$= 500\,\mu A$ (Ge BJT)



$I_{CBO} = 1\,\mu A$ (Si)

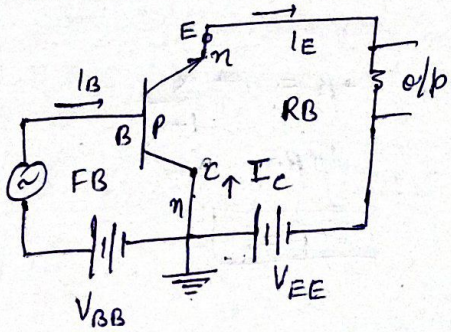
$= 5\,\mu A$ (Ge)

If I_{CBO} is in range, then transistor is in working condition.

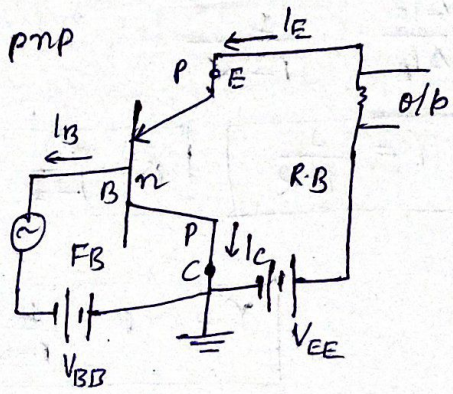
Common base configuration

Common Collector Configuration

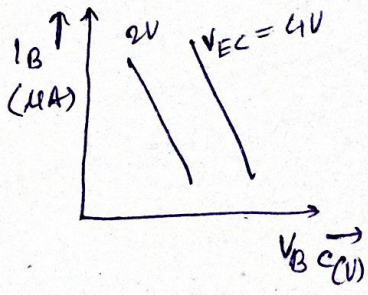
npn



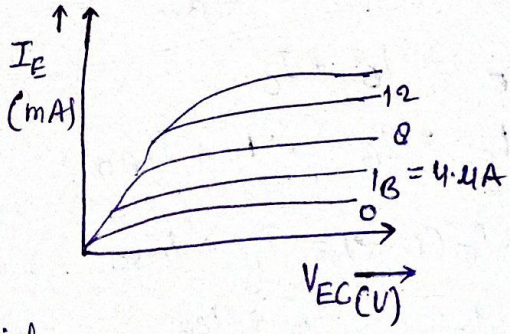
pnp



Input characteristic curve



Output char. Curve



$$r_i = \left.\frac{\Delta V_{BC}}{\Delta I_B}\right|_{V_{EC}=K}$$

r_i is very high.

$$r_o = \left.\frac{\Delta V_{EC}}{\Delta I_E}\right|_{I_B=K}$$

r_o is very small.

Current amplification Factor 'γ'

$$\gamma = \frac{\text{output current}}{\text{Input current}} = \frac{I_{out}}{I_{in}} = \frac{I_E}{I_B} \quad [\text{d.c. signal}]$$

$$\gamma_{ac} = \left.\frac{\Delta I_E}{\Delta I_B}\right|_{V_{EC}=K}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

$\gamma \simeq \beta$

But γ is slightly higher than β.

as $I_E = I_B + I_C$.

$$I_E = I_B + I_C$$

$$I_B = I_E - I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

$$\frac{1}{\Delta I_B} = \frac{1}{\Delta I_E - \Delta I_C}$$

$$\frac{\Delta I_E}{\Delta I_B} = \frac{1}{1-\alpha}$$

$$\boxed{\gamma = \frac{1}{1-\alpha}} \quad \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$$1+\beta = 1 + \frac{\alpha}{1-\alpha}$$

$$1+\beta = \gamma$$

$$\boxed{\gamma - \beta = 1}$$

$$\boxed{\gamma = 1+\beta = \frac{1}{1-\alpha}}$$

$20 < \beta < 500$

$.9 < \alpha < .99$

Collector current in CC Configuration

$$I_C = \alpha I_E + I_{CBO} \quad [\text{CB only}]$$

$$I_E = I_B + I_C$$

$$I_E = I_B + \alpha I_E + I_{CBO}$$

$$I_E(1-\alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B + I_{CBO}}{1-\alpha}$$

$$\boxed{I_E = \gamma[I_B + I_{CBO}]}$$

$$I_C \simeq I_E = \gamma(I_B + I_{CBO})$$

$$= \gamma I_B + I_{CEO}.$$

Lecture 14

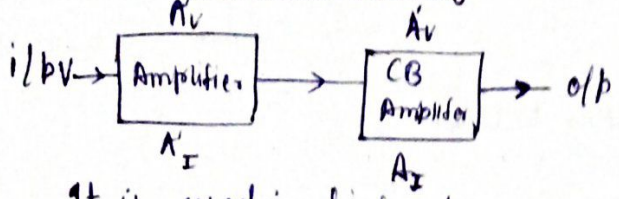
$I_C = \beta I_B + I_{CEO}$ (μA)

$I_C \simeq \beta I_B$ [since I_{CEO} is very small].

$20 < \beta < 500$.

Common Emitter Configuration is generally used in Amplification (Rectification)

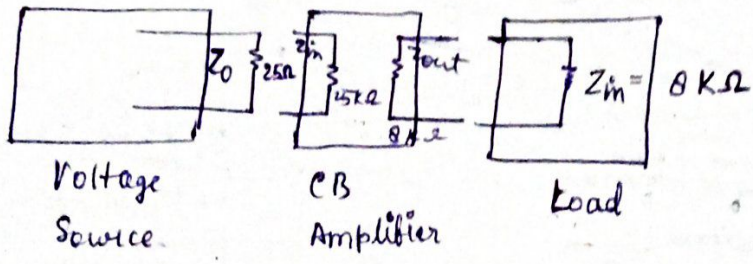
Common Base Config. → $\alpha < 1$, A_V = High.



$A'_V > A_V$ But $V_V < V_V$.

It is used in high frequency Application.

In Impedance matching under high frequency.

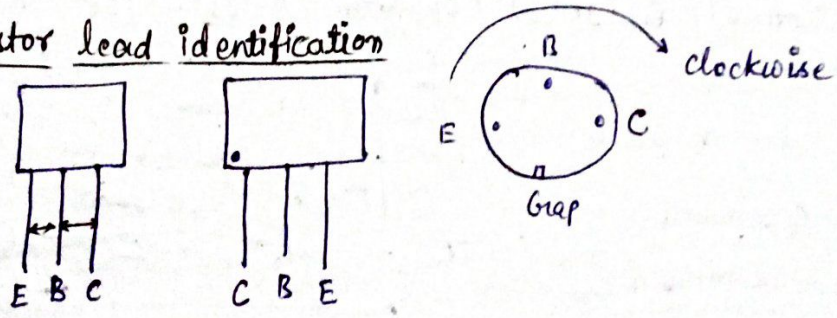


It has low input Resistance and high output Resistance.

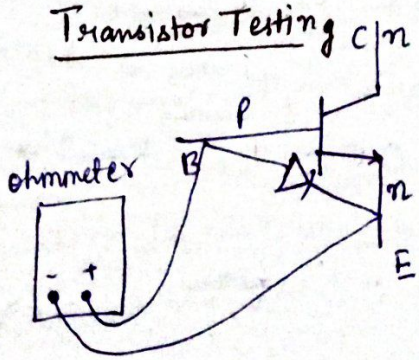
Common Collector Configuration

For impedence matching. r_i = High ; r_o = low.

Transistor lead identification

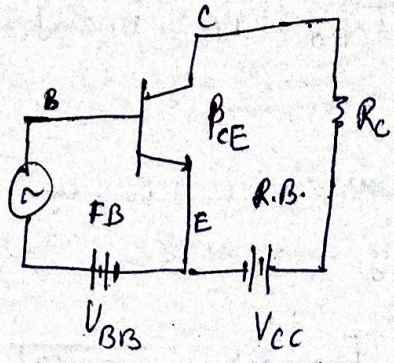


Transistor Testing



. Here is very low But if +ve terminals Connected to Collector and -ve to Base then RB occurs and very high resistance observed.

CE BJT Transistor as Amplifier due to its high A_i, and A_p. r_o/r_i = medium. Under weak frequency.



output

$I_C = \beta I_B + I_{CEO}$

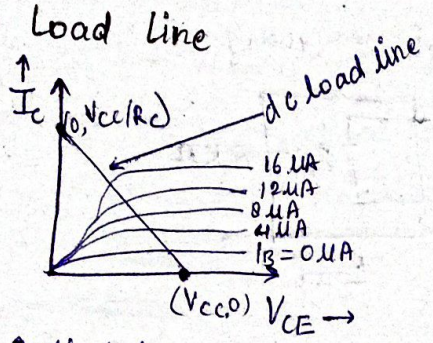
mA μA

$I_C = \beta I_B$

V_{BB} and V_{CE} are Biasing voltage.

Load Line Analysis for Analyzing circuit

DC Load Line



Output char. curve of BJT in CE mode

Apply KVL in R.B. Mesh,

$V_{CC} = I_C R_C + V_{CE}$

$V_{CE} = V_{CC} - I_C R_C$

If $I_C = 0$;

$V_{CE} = V_{CC}$.

If $V_{CE} = 0$;

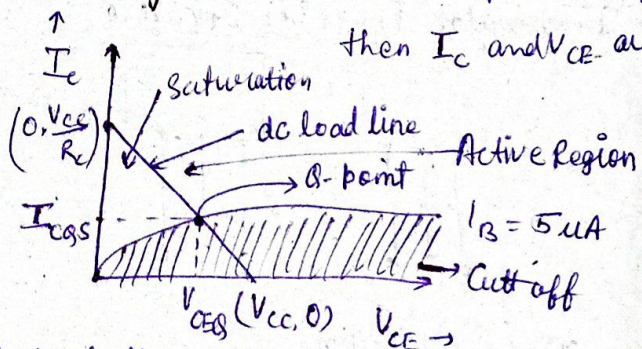
$V_{CC} = I_C R_C$

$I_C = \frac{V_{CE}}{R_C}$

<u>Operating Point</u> I_C and V_{CE} are the operating points.

(Quotient) / Quiescent / Operating / Q-Point If input voltage = 0 then I_C and V_{CE} are the Q-points.

Q should be in middle of Active Region in order to Amplify input signals perfectly.

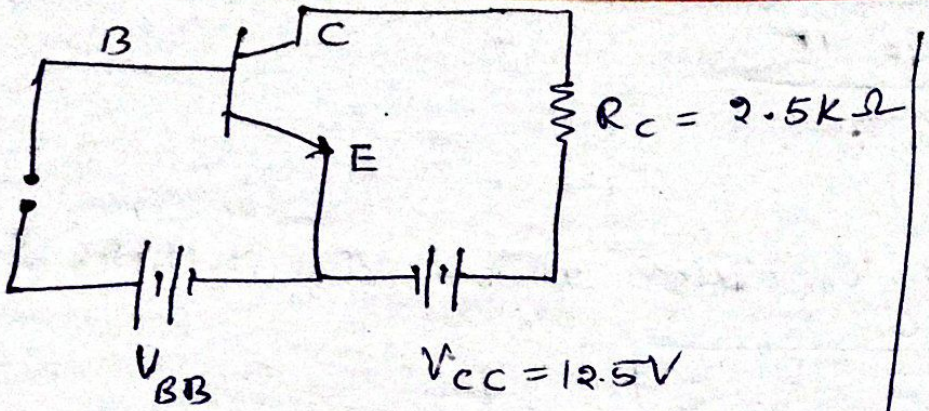


Saturation – $I_C = \frac{V_{CC}}{R_C}$ $V_{CE} = 0$

Cutoff – $I_C = 0$, $V_{CE} = V_{CC}$

Active – $I_C = \beta I_B + I_{CEO}$

$V_{CE} = V_{CC} - I_C R_C$

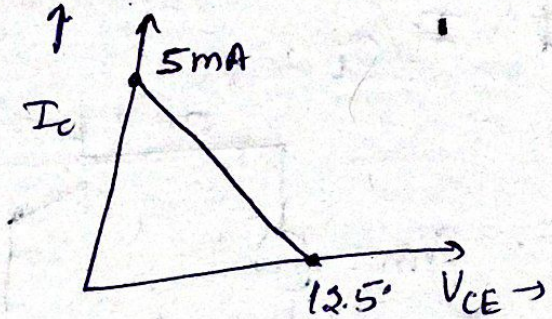


$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C} = \frac{12.5}{2.5}$$

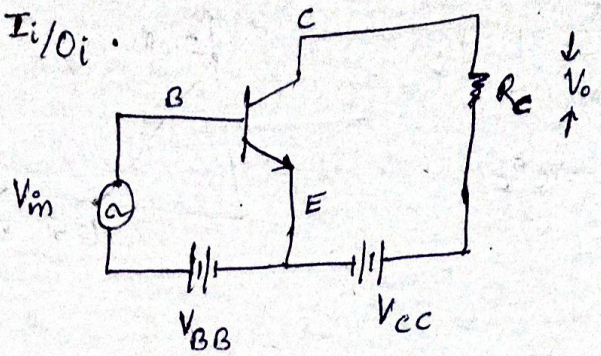
$$= 5\,mA$$



Lecture 15

Transistor Biasing

CE BJT is used in amplifier circuit due to High, A_v, A_I, A_p and I_i/O_i.



Amplifier circuit

Value of I_C, V_{CE} when $V_m = 0$ is k/a Q-point / Operating point it lies in middle of Active Region of DC load line.

$$V_{CC} = V_{CE} + I_C R_C$$

Amplification is faithful when operating point lie in middle of active region.

If Q-point near saturation region, some of +ve half of input is clipped.

If Q-point near cut-off region, some of -ve half of input is clipped and thus amplification is not faithful.

Biasing Voltage is needed in order to fix Q-point. e.g. V_{BB}, V_{CC}.

$$I_C = \beta I_B + I_{CEO}$$
$$= \beta I_B + (\beta+1) I_{CBO}$$
$$=$$

Need for stabilization of Q-point

$\beta, I_B, I_{CBO}, V_{BE}$ are all temperature dependent.

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta+1) I_{CBO}.$$

$\beta\uparrow$, I_{CBO} doubles with $\uparrow$ in T / 10°C, $V_{BE} \downarrow$ by 2.5 mV/°C

Q point shouldn't change with change in

(I) Temp.

(II) change in transistor

(III) Thermal runaway

Biasing Circuit is required to —

(1) fix Q- point.

Stability Factor (S) of any amplifier circuit.

lower the 'S', better will be stabilization of Q-point.

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$

$$S = \left.\frac{\partial I_C}{\partial I_{CBO}}\right|_{\beta \text{ and } I_B (V_{BE}) \text{ are const.}}$$

$$S_\beta = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CBO} \text{ and } V_{BE} \text{ are const.}}$$

$$S_V = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CBO}, \beta \text{ and } V_{BE} (I_B) \text{ are const.}}$$

$S = 1$ for ideal case.

$S < 25$ in practical, then amplification is faithful.

$$I_C = \beta I_B + (\beta+1) I_{CBO} \quad \text{(CE Configuration)}$$

$$S = \frac{\partial I_C}{\partial I_{CBO}} \quad \frac{\partial I_C}{\partial I_C} = \beta \frac{\partial I_B}{\partial I_C} + (\beta+1) \frac{\partial I_{CBO}}{\partial I_C}$$

$$1 = \beta \frac{\partial I_B}{\partial I_C} + \frac{(\beta+1)}{S}$$

$$\Rightarrow \frac{\beta+1}{S} = 1 - \beta \frac{\partial I_B}{\partial I_C}$$

stability factor $\leftarrow$ $\boxed{S = \dfrac{1+\beta}{1-\beta\, \partial I_B / \partial I_C}}$

Requirements of Biasing circuit

(1) choose Q-point in middle of active region even at extreme value of input signal.

(2) Instantaneous Q- pt should n't change with change in tem change in transistor of same family.

Effect on operating point (I) on variation of I_B.

It shift upward with ↑ in I_B.

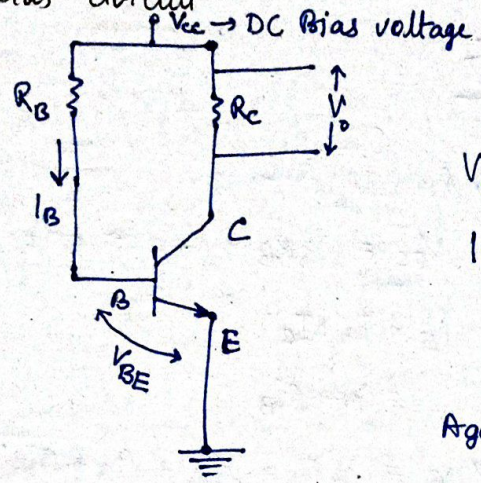
(II) on variation of V_{CC} . $V_{CC_1} > V_{CC_2} > V_{CC_3}$ point shift toward left at a fixed I_B starting from Q_1 for V_{CC_1}.

(III) on variation of R_C $R_{C_1} < R_{C_2} < R_{C_3}$. it also shift toward left

Lecture 16

Biasing circuit is used to stabilise Q-point in middle of active region.

Fixed Bias circuit



Applying KVL,

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

Again applying KVL in output section,

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

Stability factor

$$S = \frac{\partial I_C}{\partial I_{CBO}} = \frac{1+\beta}{1-\beta\, \partial I_B / \partial I_C}$$, But in fixed Bias ckt, $\frac{\partial I_B}{\partial I_C} = 0$

$\boxed{S = 1+\beta}$ → Current amplification factor

$20 < \beta < 500$

Higher will be stability factor, lower will be stabilisation of Q point.

Advantages

It is simple

We only use R_B (Base resistor)

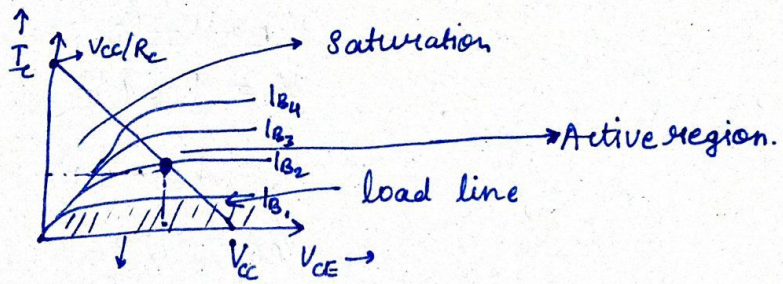
Disadvantages

Higher value of S. For faithful amplification $S < 25$.

Load line Analysis

$$V_{CC} = V_{CE} + I_C R_C$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



In saturation

$$\boxed{\begin{aligned} I_C &= V_{CC}/R_C \\ V_{CE} &= 0 \end{aligned}}$$

In cutt off

$I_C = 0$

$V_{CE} = V_{CC}$

In Active region

$I_C = \beta I_B + I_{CEO}$

$= \beta I_B + (\beta+1) I_C$

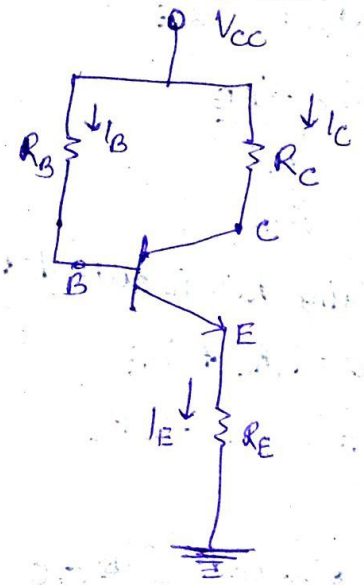
$V_{CE} = V_{CC} - I_C R_C$

If Q point goes in cutoff region, some -ve half portion may be clipped and if in saturation region, some +ve half portion may not be amplified.

Fixed Bias Base resistor circuit

Lecture 17

Emitter Bias circuit



On Applying KVL,

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$I_E = I_B + I_C$$

$$= I_B + \beta I_B$$

$$V_{CC} = I_B R_B + V_{BE} + (I_B + \beta I_B) R_E$$

$$V_{CC} = I_B (R_B + R_E + \beta R_E) + V_{BE}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}}$$

$$I_C = \beta I_B.$$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + I_C R_E$$

$$V_{CC} = I_C (R_C + R_E) + V_{CE}$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

$$V_E = I_E R_E$$

$$V_C = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CE} + V_E$$

$$V_B = V_{CC} - I_B R_B$$

$$V_{BE} = V_B - V_E$$

$$V_B = V_{BE} + V_E$$

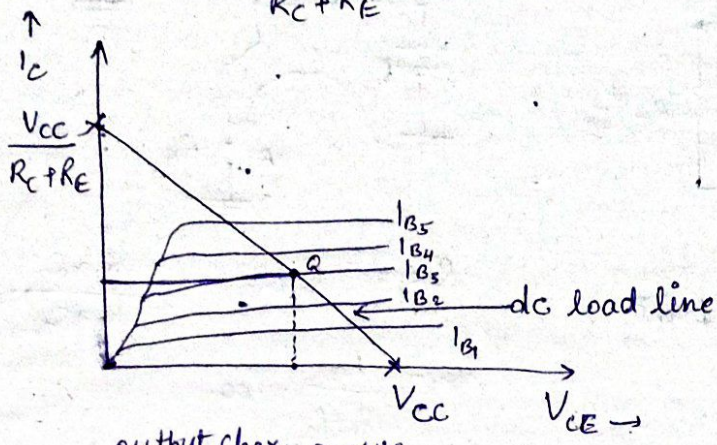
Load line Analysis of Emmitter Bias circuit

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CC} = I_C (R_C + R_E) + V_{CE}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

If $V_{CE} = 0$; $I_C = \dfrac{V_{CC}}{R_C + R_E}$ and if $I_C = 0$; $V_{CE} = V_{CC}$



output char. curve

Stability factor

$$S = \frac{\partial I_C}{\partial I_{CBO}} = \left.\frac{1+\beta}{1-\beta\, \partial I_B / \partial I_C}\right|_{\beta \,\&\, V_{BE}/I_B = K} \qquad \text{—— (I)}$$

$$V_{CC} = I_B (R_B + R_E) + V_{BE} + I_C R_E$$

$$V_{CC} - V_{BE} = I_B (R_B + R_E) + I_C R_E$$

$$\frac{\partial}{\partial I_C}(V_{CC} - V_{BE}) = \frac{\partial}{\partial I_C}\left[I_B (R_B + R_E) + I_C R_E\right]$$

$$0 = \frac{\partial I_B}{\partial I_C}(R_B + R_E) + R_E$$

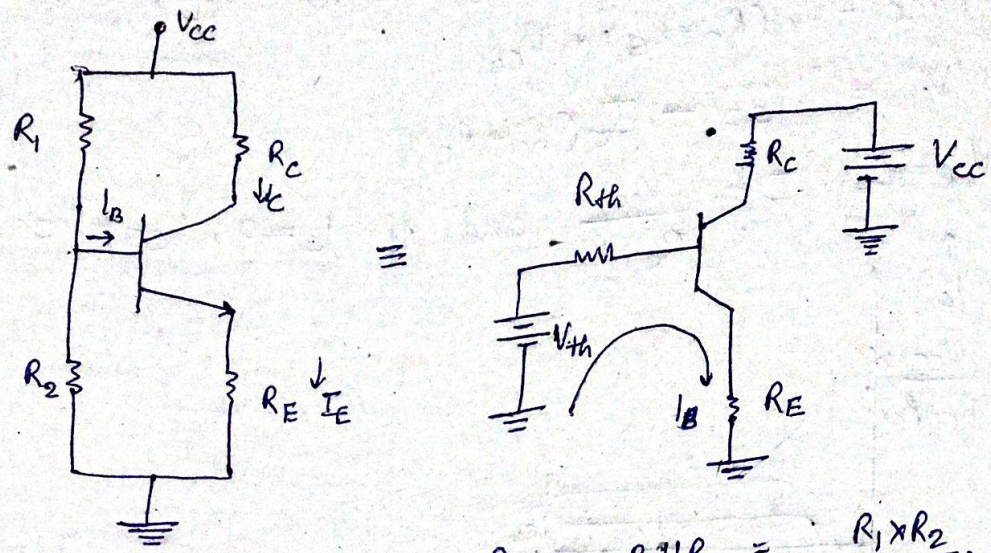
$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E} \qquad \text{—— (II)}$$

$$S = \frac{1+\beta}{1-\beta \times \left(\frac{-R_E}{R_B + R_E}\right)} = \frac{1+\beta}{1+\beta \frac{R_E}{R_B + R_E}} = \frac{(1+\beta)\left(1 + \frac{R_B}{R_E}\right)}{1 + \beta + \frac{R_B}{R_E}}$$

If $R_B/R_E \approx 0$; $\boxed{S = 1}$ and if R_B/R_E is very high, $S \simeq 1+\beta$

Lecture 18

Voltage divider Bias circuit



$$R_{th} = R_1 \| R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

Determining operating point

On Applying KVL,

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E$$
$$= I_B R_{th} + V_{BE} + (I_B + I_C) R_E$$
$$= I_B R_{th} + V_{BE} + (I_B + \beta I_B) R_E$$
$$V_{th} = I_B [R_{th} + (1+\beta) R_E] + V_{BE}$$

$$\boxed{I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1+\beta) R_E}}$$

$$\boxed{I_C = \beta I_B}$$

Applying KVL in outer circuit loop,

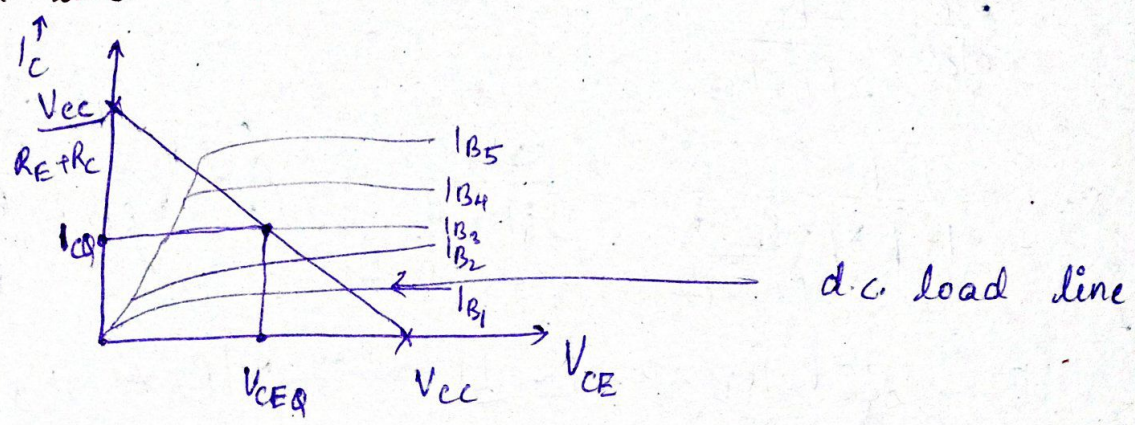
$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$
$$= I_C R_C + V_{CE} + I_C R_E \quad [\because I_E]$$
$$V_{CC} = I_C (R_E + R_C) + V_{CE}$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_E + R_C)}$$

$V_{CE} = V_{CC}$] If $I_C = 0$

$I_C = \dfrac{V_{CC}}{R_E + R_C}$] If $V_{CE} = 0$

Load line Analysis



Stability factor

$$S = \left.\frac{\partial I_C}{\partial I_{CBO}}\right|_{\beta \text{ and } V_{BE}(\text{or } I_B) = K}$$

$$S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}} \quad \text{——— (1)}$$

$$V_{th} = I_B R_{th} + V_{BE} + (I_B + I_C)R_E$$

$$V_{th} = I_B(R_{th} + R_E) + I_C R_E + V_{BE}$$

$$V_{th} - V_{BE} = I_B(R_{th} + R_E) + I_C R_E$$

$$0 = \frac{\partial I_B}{\partial I_C}(R_{th} + R_E) + R_E$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_{th} + R_E} \quad \text{——— (2)}$$

$$S = \frac{1+\beta}{1-\beta\left(\frac{-R_E}{R_{th}+R_E}\right)}$$

$$= \frac{1+\beta}{1+\frac{\beta R_E}{R_{th}+R_E}} = \frac{(1+\beta)\left(1+\frac{R_{th}}{R_E}\right)}{1+\beta+\frac{R_{th}}{R_E}} \quad \text{If } \frac{R_{th}}{R_E} \approx 0$$

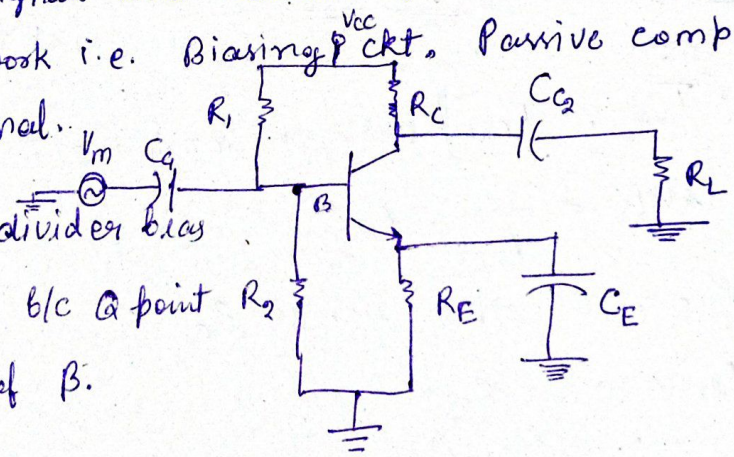
$\boxed{S = 1}$ when $R_{th}/R_E \approx 0$.

$\boxed{S = 1+\beta}$ when R_{th}/R_E is very high.

Lecture 19

Single stage Transistor Amplifier

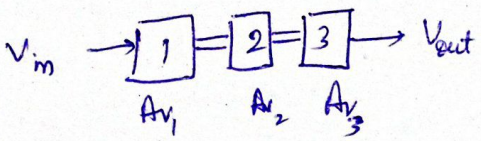
Amplifies weak signals and consist of transistor alongwith associated network i.e. Biasing ckt. Passive components and input signal.



Here, voltage divider bias circuit is used b/c Q point is independent of β.

C_{C_1} and C_{C_2} are coupling capacitor.

C_E is Emitter bypass capacitor. In absence of it, reduction in o/p voltage occurs.



$$\frac{V_o}{V_m} = A_{v_1} \times A_{v_2} \times A_{v_3}$$

$$X_{CE} \le \frac{R_E}{10}$$

i_b = i/p current

$i_c = \beta i_b \quad (20 < \beta < 500)$

In common emmitter mode. phase shift $\phi = 180°$.

$$i_E = I_E + i_e$$
$$i_B = I_B + i_b$$
$$i_C = I_C + i_c$$

Analysis

(1) DC Analysis Requirment
(a) AC i/p signal = 0
(b) All the capacitor removed (or open).

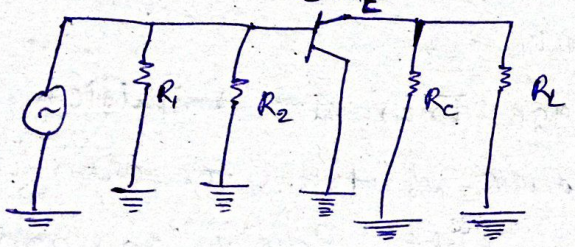
(2) AC Analysis requirements
(a) All dc source = 0 i.e $V_{CC} \rightarrow$ Ground.
(b) All the capacitor should be shorted.

(1) Now, $V_{CC} = I_C R_C + V_{CE} + I_C R_E = I_C (R_C + R_E) + V_{CE}$

So, $V_{CE} = V_{CC}$

$$I_C = \frac{V_{CC}}{R_C + R_E}.$$

(2)



the amplifier ckt looks like it in A.C. analysis.

$$A_V = \frac{\text{output ac voltage}}{\text{input ac voltage}}.$$

$[I_{CQ}, V_{CEQ}]$ are operational points.

$$\text{slope} = \frac{-1}{R_{ac}} = \tan\theta.$$

R_{ac} = AC o/p resistance $= R_C \| R_L$.

$R_{dc} = R_C + R_E$

V_{CEQ}. for load line,

$$OA = V_{CEQ} + I_{CEQ} \times R_{ac}$$

$$OB = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$$

$$R_{ac} = R_C \| R_L.$$

Power gain
voltage gain
current gain
input impedance
output impedance

These all values can be determined by using AC analysis of amplifier circuit.

$$A_V = \frac{\text{output voltage}}{\text{input voltage}} = \frac{i_c \times R_{ac}}{i_b \times R_{in}}$$

$R_{in} = R_1 \| R_2 \| r_i$

$R_{ac} = r_o \| R_c \| R_L$

CE BJT very low i/p R — very high o/p R — sufficient A_i, A_v, A_p

CC BJT very high i/p R — very low o/p R — $A_v < 1$, A_i high, A_p is moderate

CE is generally used in amplification.

CB, α, amplification factor is less than unity.

Voltage divider Bias ckt is used in amplification ckt as its Q point does not get affected by β.

Lecture 20

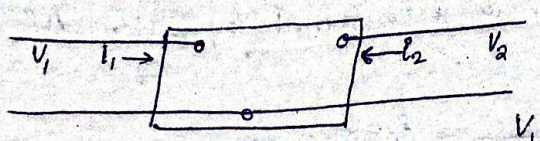
Calculation of various parameters. A_v, A_i, A_p, Z_{in} and Z_{out}

Firstly represent BJT with its ac equi. model.

(1) h-parameter model

hybrid. Transistor is a 3-terminal and 2-port device.

i/p port. o/p port



V_1 and i_2 are dependent variables

V_2 and i_1 are independent variables

$$V_1 = h_{11} i_1 + h_{12} V_2$$

$$i_2 = h_{21} i_1 + h_{22} V_2$$

$h_{11}, h_{12}, h_{21}, h_{22}$ are hybrid parameters.

$h_i \rightarrow h_{11} = \left.\frac{V_1}{i_1}\right|_{V_2=0}$ (with o/p shorted). $\longrightarrow$ Input R/Z. Ω

$h_r \rightarrow h_{12} = \left.\frac{V_1}{V_2}\right|_{i_1=0}$ (with i/p open) $\longrightarrow$ Reverse voltage ratio unitless

$h_f \rightarrow h_{21} = \left.\frac{i_2}{i_1}\right|_{V_2=0}$ (with o/p shorted) $\longrightarrow$ Forward current ratio unitless

$h_o \rightarrow h_{22} = \left.\frac{i_2}{V_2}\right|_{i_1=0}$ (with i/p open). $\longrightarrow$ Output Y ($1/Z$) or G ($1/R$) $\mho$ mho/simens.

CE mode BJT

$h_{11} \rightarrow h_{ie}$

$h_{12} \rightarrow h_{re}$

$h_{21} \rightarrow h_{fe}$

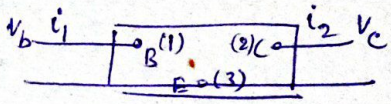
$h_{22} \rightarrow h_{oe}$

CC and CB

subscript

c b

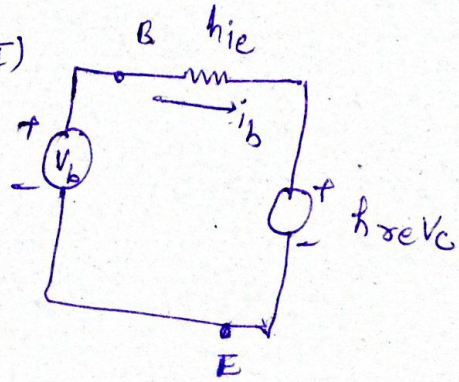
$\therefore$ For CE mode BJT



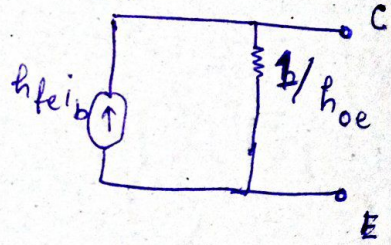
$$V_b = h_{ie} i_b + h_{re} V_c \longrightarrow (I)$$

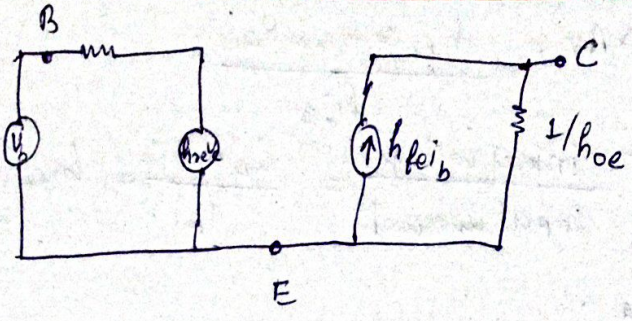
$$I_c = h_{fe} i_b + h_{oe} V_c \longrightarrow (II)$$

(I)

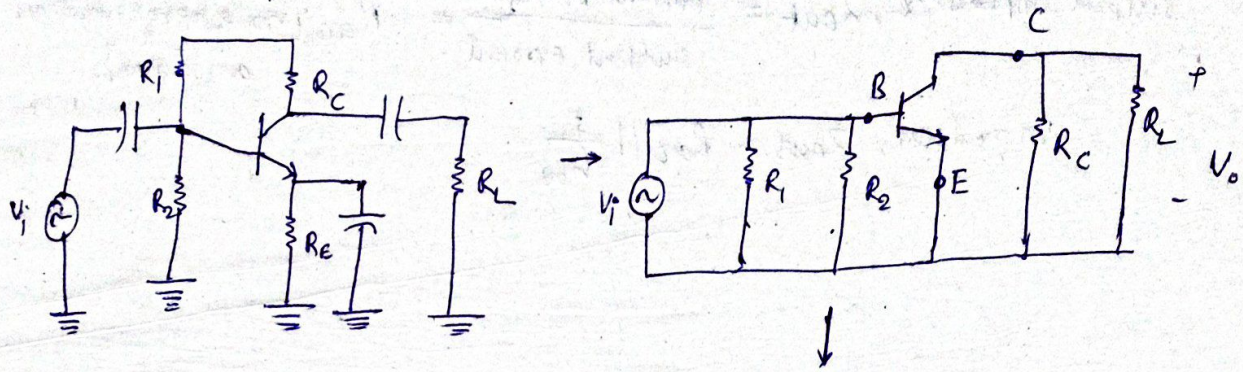


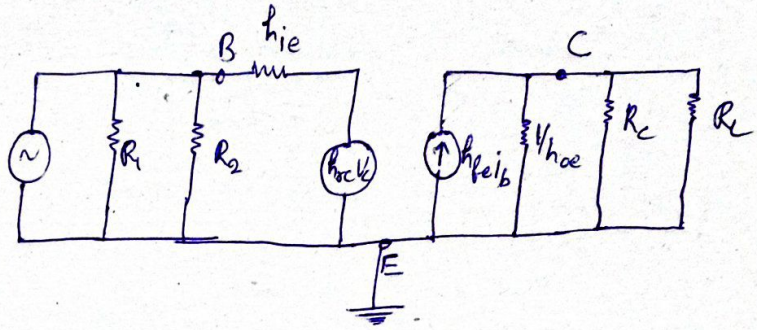
(II)





Equivalent BJT in h-parameter model.





h-parameter model.

BJT in CE mode config.

Typical values:

$h_{ie} = 1K\Omega$

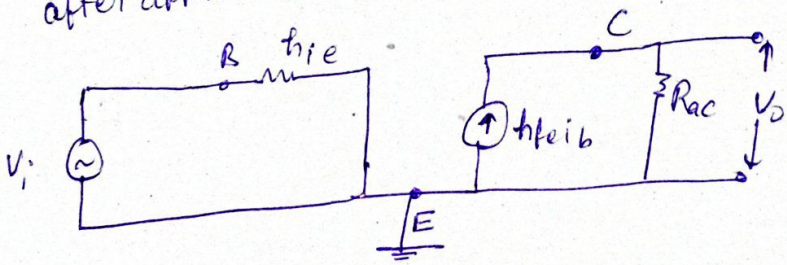
$h_{re} = 2.5 \times 10^{-4}$

$\beta = h_{fe} = 50$

$h_{oe} = 25$ μ siemens $\frac{1}{h_{oe}} = 40K\Omega$.

$R_{ac} = R_C \| R_L \simeq 1K\Omega$.

after approximation analysis, ckt will be



Current gain $= A_i = \frac{\text{output current}}{\text{input current}} = \frac{i_c}{i_b} = \frac{h_{fe} i_b}{i_b} = h_{fe}$

$A_i = h_{fe} = \beta$.

Voltage gain $= A_V = \frac{\text{output voltage}}{\text{input voltage}} = \frac{-h_{fe} i_b \times R_{ac}}{i_b \times h_{ie}} = \frac{-h_{fe} R_{ac}}{h_{ie}} = \frac{h_{fe} R_{ac}}{h_{ie}} \angle 180^\circ$

$A_V = \frac{\beta R_{ac}}{h_{ie}} \angle 180^\circ$

Power gain $= A_p = A_i \times A_v = \dfrac{h_{fe} \times h_{fe} \times R_{ac}}{h_{ie}}$.

input impedance, $Z_{in} = \dfrac{\text{input voltage}}{\text{input current}} = \dfrac{i_b \times h_{ie}}{i_b} = h_{ie}$

$Z_{in} = h_{ie} \parallel R_1 \parallel R_2$.

output impedance, $Z_{out} = \dfrac{\text{output voltage}}{\text{output current}} = R_{ac}$ [in approximation analysis].

In reality, $Z_{out} = R_{ac} \parallel \dfrac{1}{h_{oe}}$