Roll No.

MCA (SEMESTER I) 2022 – 2023
ODD SEMESTER
Major Examination

Subject Code: MCA 113 Subject: **Computer Organization & Architecture**

Time: 03 Hrs Max. Marks: 50

Note: Attempt ALL questions. Each question carries equal Marks.

Q.1 Attempt any five parts of the following: (5 * 2 = 10)

a Find the value of x in the following:
(i) $(23412)_7 = (x)_{10}$ (ii) $(846)_9 \times (573)_9 = (x)_9$

b Convert the following expressions into sum-of-products and product-of sums forms:
(i) (AB + C) (B + C'D)
(ii) X' + X(X + Y')(Y + Z')

c Simplify the following expressions F together with the don't care conditions d in (I) sum-of-products form and (II) products-or-sums forms:
$F(w,x,y,z) = \sum(3, 5,6,7)$
$d(w,x,y,z) = \sum(10, 11, 12, 13, 14, 15)$

d Implement the following function with (i) 16:1 (ii) 8:1 and (iii) 4:1 multiplexer:
$F(A,B,C,D) = \sum(2,4,5,7,10,14)$

e Design an Quad -to-binary priority encoder. Provide an output V to indicate that at least one of the inputs is a 1. The input the with the lowest subscript number has the highest priority. What will be the value of four outputs if inputs D5 and D3 are 1 and the other inputs are all 0's?

f Design a synchronous counter which steers through the following states: S7-S6-S5-S3-S2-S0 using J-K Flip flop.

g Design a combinational circuit that generated the 9's complement of a BCD digit.

Q.2 Attempt any two parts of the following: (2 * 5 = 10)

a What is the disadvantage of binary parallel adder? Explain how a look ahead adder speeds up the addition process. Clearly show the derivations of equations.

b What do you understand by hardwired control unit? Give various methods to design hardwired control unit. Describe one of the design methods for hardwired control unit with suitable diagram.

c i Design 4-bit Arithmetic Circuit that performs Addition, Subtraction, Increment and Decrement operations.

ii The outputs of four register R0, R1, R2, R3 are connected through 4-1 multiplexers to the inputs of the fifth register, R5. Each register is 8 bits long. The required transfer are dictated by four timing variables T0 through T3 as follows:

T0 : R5←R0
T1 : R5←R1
T2 : R5←R2
T3 : R5←R3

Draw a block diagram showing the hardware implementation of register transfers.

Q.3 Attempt any two parts of the following: (2 * 5 = 10)

a Write a program to evaluate the arithmetic statement: -
X = (A-B*C)/(D*E+F/G-H*I+J)
Using Three, Two, One and Zero address Machines.

b Show the basic organization of a CPU in terms of registers and other units for a Single-bus – organization. In such a CPU, show the complete action of the CPU in fetching and executing the instruction.

c c_1 Design a variable length opcode to allow all of the following to be encoded in a 36-bit instruction:

I. Instruction with two 15-bit addresses and one 3-bit register number.

II. Instruction with one 15-bit addresses and one 3-bit register number.

III. Instruction with no address or register.

c_2 Draw a diagram of bus system for four registers of 2-bits each. The bus is to be constructed with multiplexers.

Q.4 Attempt any two parts of the following: (2 * 5 = 10)

a 4K x 16 RAM chips are used to construct 128K x 64 Memory. How many chips will be required? Draw a connection diagram.

b Obtain the truth table of an 8x3 priority encoder. Assume that the three outputs xyz from the priority encoder are used to provide a vector address of the form 101xyz00. List the eight vector addresses starting from the one with the highest priority.

c Discuss the concept and implementation of virtual memory. Also describe a suitable scheme for translation from logical address to physical address.

Q.5 Attempt any two parts of the following: (2 * 5 = 10)

a I A block set associative cache consists of a total of 256 blocks divided into eight block sets. The main memory containing 8192 blocks each consisting of 64 words.

(i) How many bits are there in the main memory address?

(ii) How many bits are there in each of TAG, SET and WORD field?

II What is cache memory? Consider a system having 512K main memory organized as 16K blocks of 32 words each and a cache memory of 16K arranged as 512 blocks of 32 words each. Show how the mapping is done using direct mapping.

b Describe DMA with suitable block diagram. Why does DMA have priority over the CPU when both request a memory transfer? Explain.

c What are the basic advantages of priority interrupt over a non-priority system? Is it possible to have a priority interrupt without a mask register? Discuss.