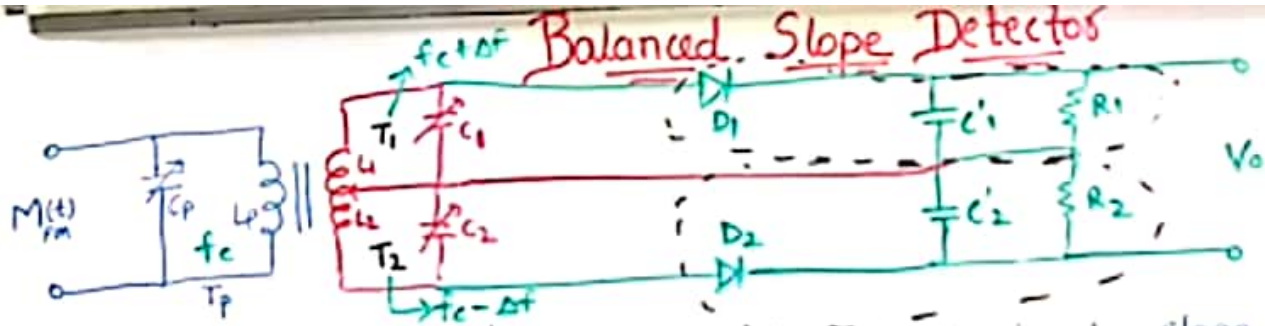
# Balanced Slope Detector




$D_1 \rightarrow$ ...
$D_2 \rightarrow -V$
$V_o(t) \rightarrow |V_{R1}| - |$

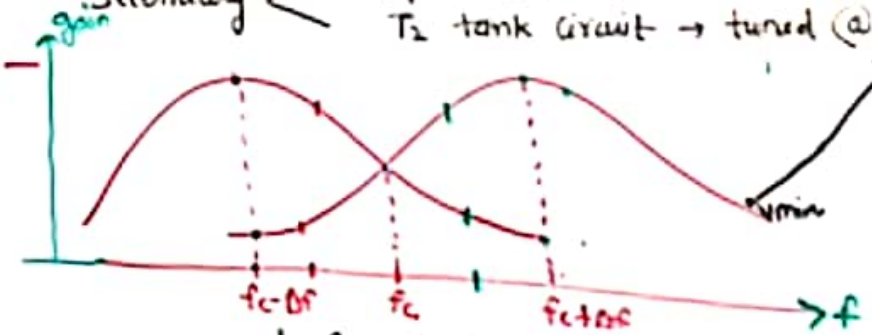
Balanced slope detector → combination of 2 simple slope detector...

Primary tank circuit $T_p$ → tuned @ $f_c$ → frequency de...

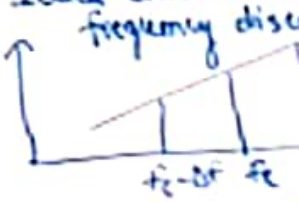
Secondary < $T_1$ tank circuit → tuned @ $f_c + \Delta f$

$T_2$ tank circuit → tuned @ $f_c - \Delta f$

**Working :-**




Ideal characteri...
frequency disc...




**$f = f_c$**

Induced V@ $T_1$ = Induced V@ $T_2$

$V_{D1} = V_{D2}$

$|V_{R1}| = |V_{R2}|$

$V_o(t) = 0$

**$f_c < f < f_c + \Delta f$**

Induced V@ $R_1$ > Induced V@ $R_2$

$V_{D1} > V_{D2}$

$V_o(t) = V_{R1} - V_{R2} > 0$

@ $f_c + \Delta f$ = $V_{max} = V_o(t)$

**$f_c - \Delta f < f < f_c$**

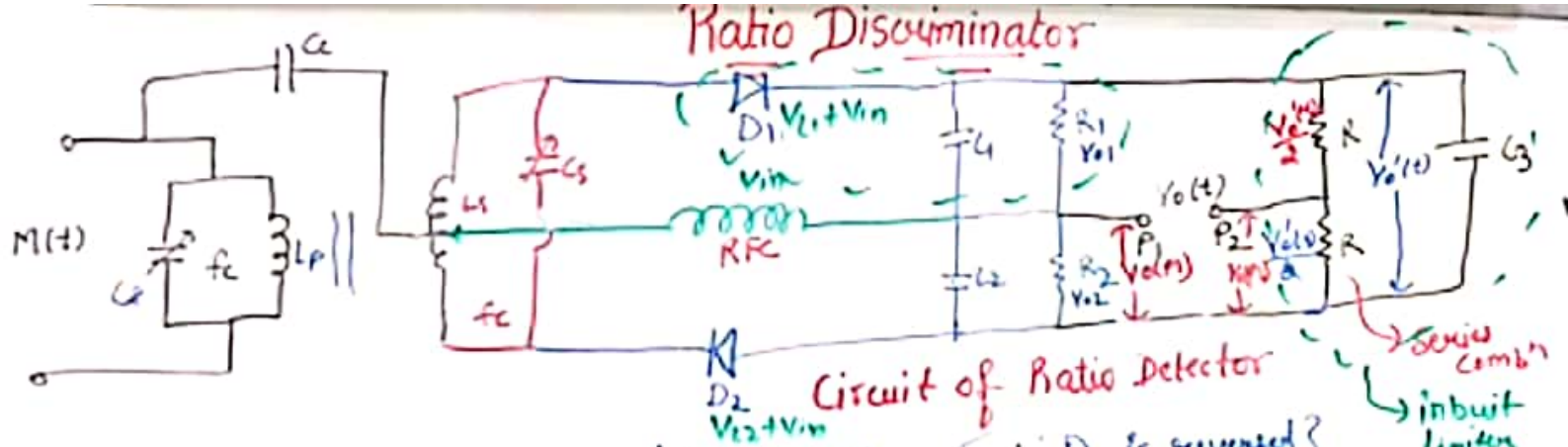
Induced V@ $R_1$ < Induced...

$V_{D1} < V_{D2}$

$V_o(t) = V_{R1} - V_{R2}$

@ $f_c - \Delta f = V_{min}$ ...

# Ratio Discriminator




Circuit of Ratio Detector

$V_o'(t) = V_{o1} + V_{o2}$ { $\because$ $D_2$ is reversed }

$V_o(t) = V_o(P_1) - V_o(P_2)$

$= V_{o2} - \frac{V_o'(t)}{2}$ $= V_{o2} - \frac{V_{o1} + V_{o2}}{2}$

$V_o(t) = \frac{V_{o2} - V_{o1}}{2}$

$\frac{V_{o1}}{V_{o2}}$ → Ratio changes according to v.

$\therefore$ Ratio Detector

| $f = f_c$ | $f > f_c$ | $f < f_c$ |
|---|---|---|
| $V_{o1} = V_{o2}$ | $V_{o2} - V_{o1}$ / 2 | $V_{o2} - V_{o1}$ / 2 |
| $V_o(t) = 0$ | $V_o(t) > 0$ | $V_o(t) < 0$ |

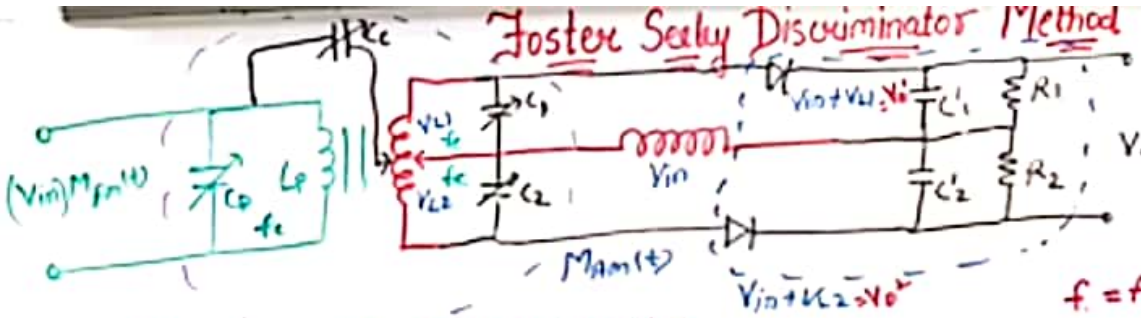
Advantages :-

1. Less affected by noise due to inbuilt limiter.
2. Simple circuit.
3. Larger Bandwidth
4. High linearity.

Disadvantages :-

1. Not be implemented over IC

# Foster Seely Discriminator Method




## Advantages of coupling capacitor

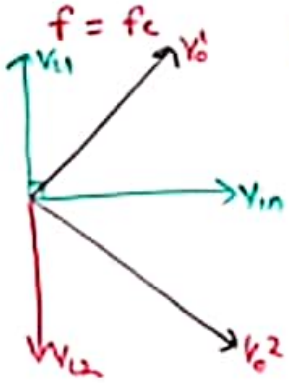
→ Block the DC from primary to secondary

→ couples primary & to center tapped inductor.

f = fc ⇒ the phase b/w primary & secondary V = 90°

f > fc ⇒ the phase b/w primary & secondary V < 90°

f < fc → ——— > 90°

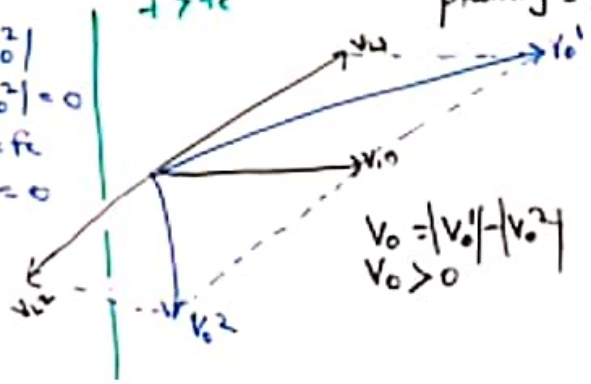



$|V_o'| = |V_o^2|$

$|V_o'| - |V_o^2| = 0$

when f = fc

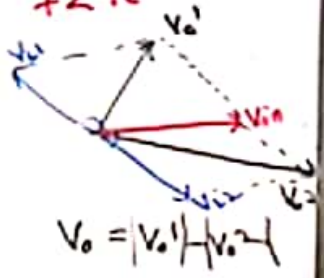
$V_o(t) = 0$




$V_o = |V_o'| - |V_o^2|$

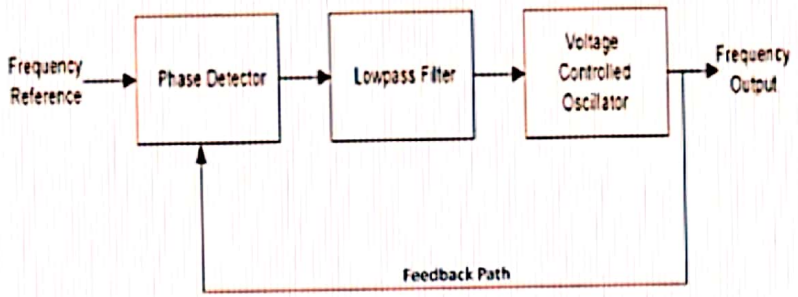
$V_o > 0$

primary = Vin , Secondary = V1




$V_o = |V_o'| - |V_o^2|$

# Block Diagram of PLL




# Phase Detector

- A phase detector is basically a comparator that compares the input frequency f_in with feedback frequency f_out.
- Comparing the input frequency & output frequency it provides a error signal which is basically a Dc voltage.
- The loop is locked when these two signals are of the same frequency and have a fixed phase difference.
- Basically Phase Detector works as an Ex-OR gate.

# Low Pass Filter

- Low-pass filter is used to remove high frequency components and noise from the output of the phase detector.
- Low Pass Filter provides a steady dc level voltage which becomes the input of VCO.

# Voltage Controlled Oscillator (VCO)

- Voltage-controlled oscillator generates frequency controlled by input voltage.
- The dc level output of a low-pass filter is applied as control signal to the voltage-controlled oscillator (VCO).
- The VCO frequency is adjusted till it becomes equal to the frequency of the input signal.
- During this adjustment, PLL goes through three stages-free running, capture and phase lock.

# Stages of PLL Operation

- **Free Running Stage:** When no input is applied at the phase detector, then due to VCO, PLL works in Free Running Stage. The output frequency of this stage is dependent on the free running frequency of VCO.

- **Capture Stage:** When a input frequency is applied at the phase detector, then due to feedback mechanism PLL tries to track the output with respect to input. This stage is called Capture Stage.

# Stages of PLL Operation

- **Phase Locked State:** Due to feedback mechanism, the frequency comparision stops as soon as the output frequency become equal to the input frequency. This stage is called Phase Locked State.