Computer Architecture and Organization
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Lecture - 26
Synchronous DRAM

Welcome to lecture 26. In this lecture we will be discussing about Synchronous DRAM.

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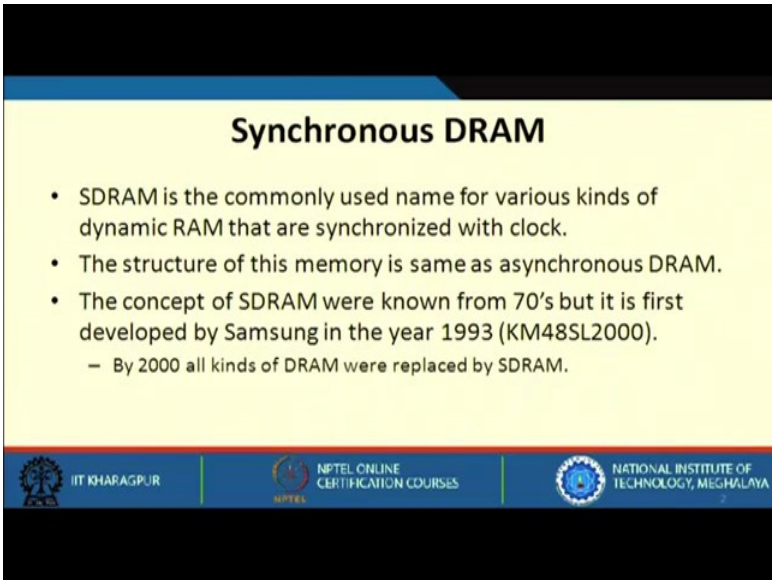

As the name suggests synchronous, so it is synchronized with clock. SDRAM is the commonly used name for various kinds of dynamic RAM that are synchronized with clock. All such kind of DRAM that are synchronized with clock. In the previous lecture we have seen a synchronous DRAM where there is no concept of clock; the module that is connected to the memory has to take care of that, but in this case here it is synchronized with clock.

The structure of this memory is same as a synchronous DRAM. And the concepts were also known from the 70s, but it was developed in the year 1993. And by the year 2000 almost all kinds of dynamic RAM were replaced by SDRAM. So, there was no asynchronous DRAM anymore.

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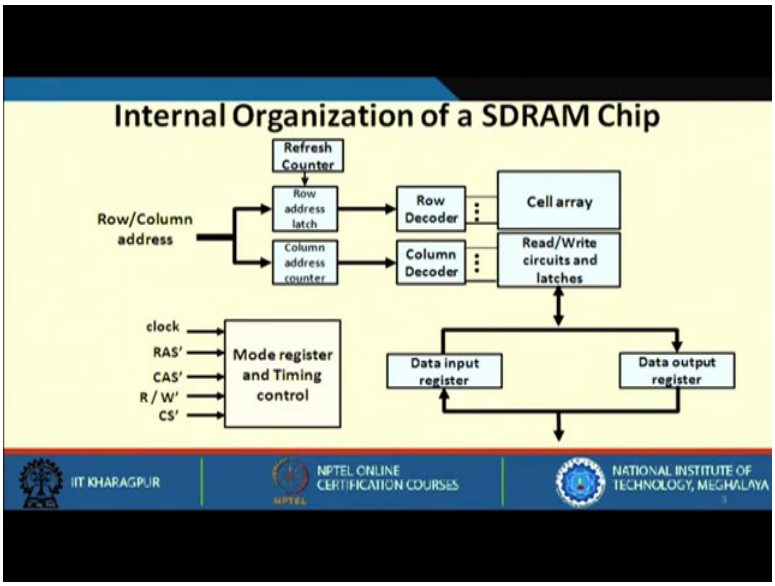

Now let us see the internal organization of SDRAM chip. As I said the internal organization of SDRAM is very similar to a synchronous DRAM, but it is having some more features. So, you can see that the row and column address can be provided. So, once we apply a row address, that particular address go to row decoder and a particular cell get selected, but here you see we have column address counter. So, instead of column address latch there is a counter that will be used to count to the next, next, next column for faster access.

And the read write circuit and these latches are connected to the data input register and data output register. Data input register will be required when we have to transfer a data from a data bus to this particular cell. That will come through data input register. And if you want to output something from this chip to data output register then it will be output. Along with this we have a mode register and timing control where the clock is provided, other signals like RAS and CAS are also provided, and two more signals that is read/write and chip select these are also provided here.

Apart from this we have an inbuilt refresh counter that refreshes the rows of these cells periodically. This overall diagram shows the internal organization of SDRAM that we can say that it is very much similar to a synchronous DRAM with some more features, like we have a data input register data, output register we have a column address counter

instead of column address latch we have a clock involved here and we have a mode register that we will be seeing what is the purpose of that particular register.

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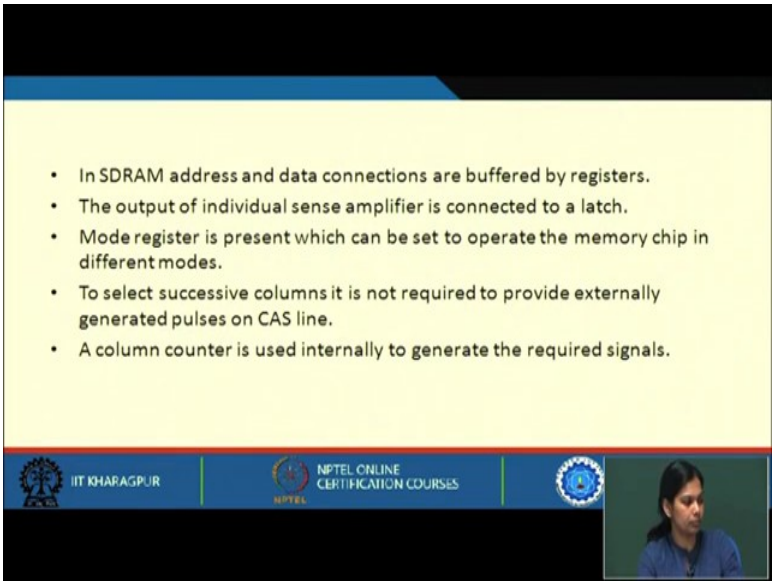

In SDRAM the address and data connections are buffered by registers, we have seen that. The output of individual sense amplifiers is connected to a latch. Mode register is present and what it does is it can be set to operate the memory chip in different modes. We will be seeing that this mode register is very much important and it can be used for speeding up, we are always trying to make memory faster such that the memory processor speed gap can be minimized.

So, these are few things that are added in synchronous DRAM to make this happen. So, mode register is present which can be set to operate the memory chip in various modes. To select successive columns it is not required to provide externally pulses generated on CAS line. What do you mean by that? You recall our previous discussion where we said that one row can be selected and for selecting the data from different columns we give a column address then we give the next column address, and so on.

For giving a column address we have a column counter that will help internally to generate the required signals. This column counter will be used internally which will be helpful in generating the signals to select various columns.

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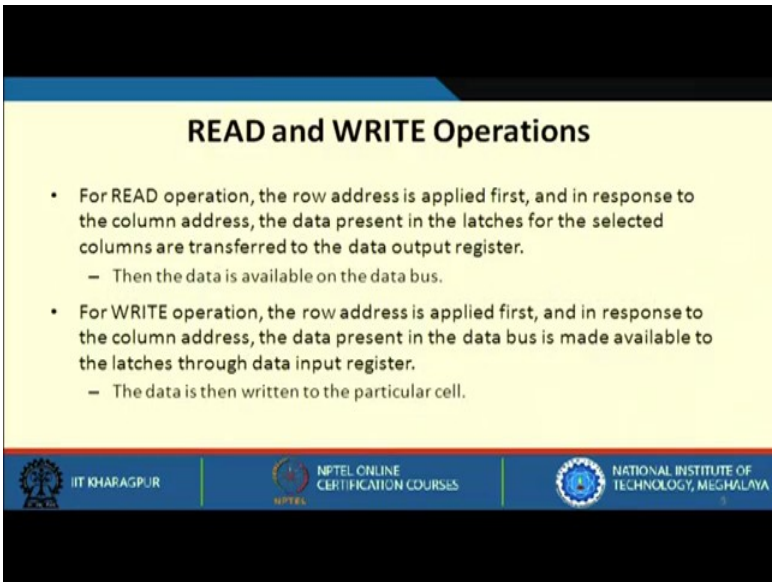

Now, let us see what happens for READ and WRITE operation. For READ operation the row address is applied first, and in response to the column address the data present in the latches of the selected columns are transferred to the data output registers, and then the data is available in the data bus. So, what happens in the same way for reading a cell value we apply a column address, we apply a row address first, and then we apply a column address. In response to that particular column address the column data are selected and it is stored in the data output register. In this data output register it is transferred to the data lines finally, then the data will be available on the data lines; that is the data bus and then it goes to the processor.

Similarly, for write operation the row address is applied first and in response to the column address, the data present in the data bus is made available to the latches through the data input register. And then finally, the data is written to the particular cell. So, for reading and for writing the required cell needs to be selected. After the cell gets selected the particular data will be read through this data output register or will be written to this data input register.

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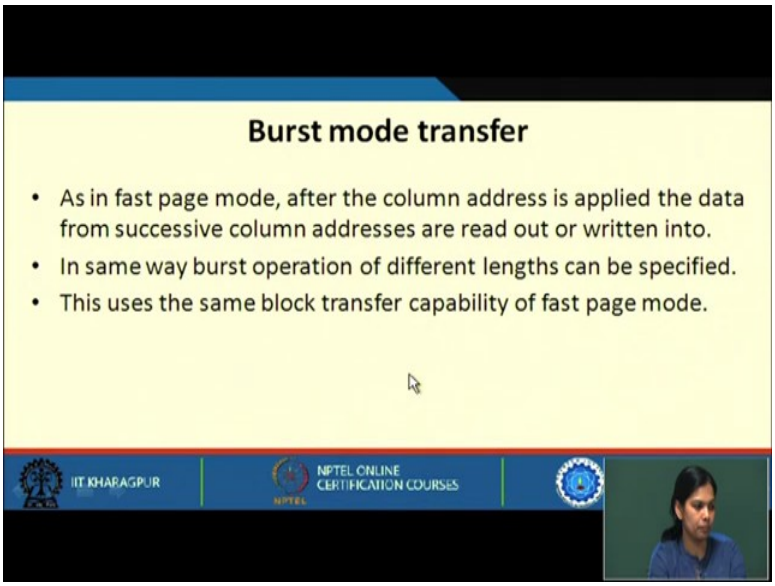

Now let us see; what is this burst mode transfer. We already discussed about fast page mode where we select a particular row and a particular column and then we need not have to select that particular row again, rather next data can be available just by incrementing the column addresses. So, here also we will see that how this burst mode transfer happens. As in fast page mode, after the column addresses are applied the data from successive column addresses are read out or written into.

In the same way burst operation of different lengths can be specified. Burst operation means burst of data; a set of words are transferred. So, here we can specify how many words we want to transfer. For the burst mode transfer different lengths can be specified. This uses the same block transfer capability of the fast page mode. So, whatever we discussed in the fast page mode this block transfer mode also uses the same feature.

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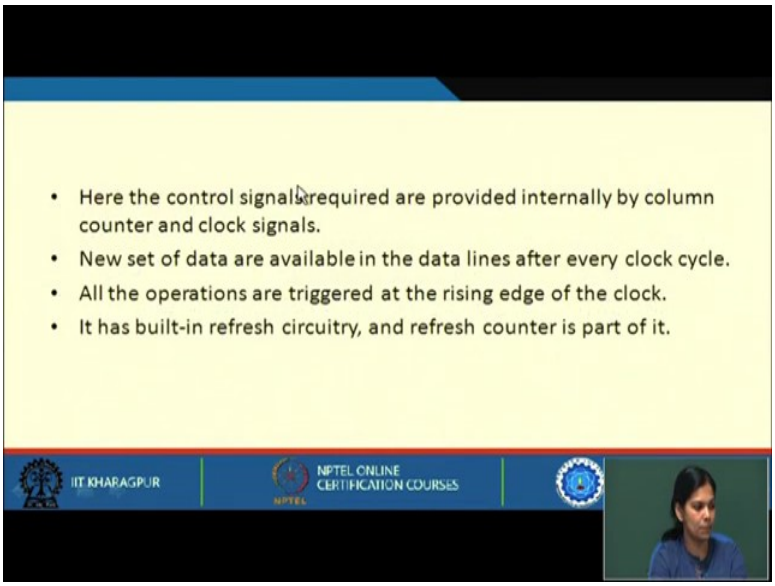

So, what happens here the control signals required are provided internally by the column counter and clock signals, as a clock is also associated with it. So the control signals that are required for this purpose are provided internally by the column counter and the clock signal. New set of data are available in the data lines after every clock cycle.

All operations are triggered at the rising edge of the clock, but we will see that with advancement this has changed, and we could do data transfer both in the rising edge as well as in the falling edge. It also has a built in refresh circuitry and refresh counter is part of it. So, there is a built in refresh circuitry that refreshes the different rows of the cells of the memory chip.

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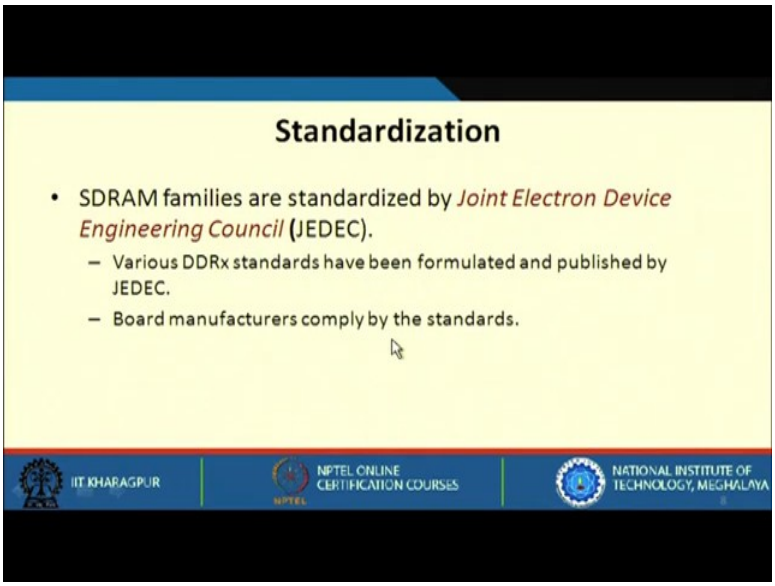

Now, we must know that the standardization of this SDRAM. So, see when some products are generally built, so there must be some standardization so that different companies when they build that particular system they can be used by others. So, there should be standardization; so we standardize.

SDRAM families are standardized by Joint Electron Device Engineering Council, we call it JECED. So, various DDRX - DDR stands for double data rate, x stands for it can be 2, it can be 3, can be 4, and so on. So, various DDRX standards have been formulated and published by JECED, and board manufacturers who are building these memory chips must comply with these standards. So, whichever chip is produced must be complied with JECED standard.

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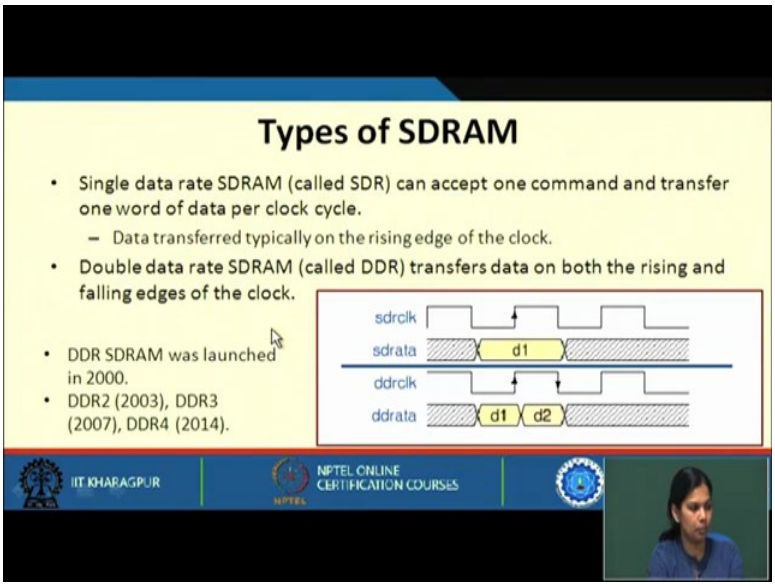

Now, let us see various types of SDRAM. When SDRAM came into market it was single data rate SDRAM it is called SDR. What it can do? It can accept one command and transfer one word of data per clock cycle. That is why it is called single data rate. Data transferred typically on the rising edge of the clock.

Now, you see this diagram where it shows SDR clock, so clock is coming and you see this is the SDR data; so here this data is transferred in the rising edge of the clock, only one data is transferred. So, this is called single data rate. Let us move on with double data rate SDRAM, which is called DDR and it transfers data on both rising edge and falling edge of the clock. So, we see that within a clock two data are transferred one on the rising edge another on the falling edge.

So, these types of SDRAM are called double data rate RAM. DDR SDRAM was launched in 2000 and then with time various versions of DDR SDRAM came into market. So, DDR2 came in 2003, DDR3 came in 2007, DDR4 took 7 more years to come. And people are also saying that DDR5 is going to come in the future.

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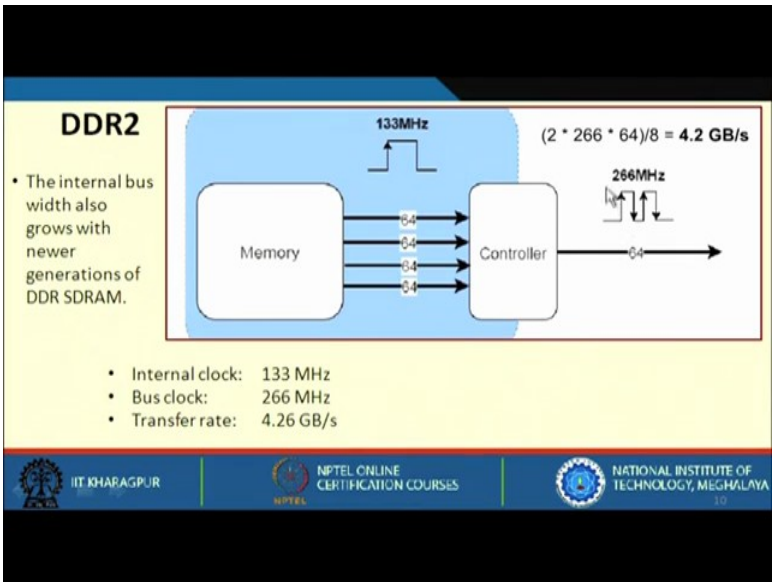

Now let us see; what is DDR2. Now we see that this is our memory and internally there is 64-bit data bus; so the internal bus width also grows with the newer generation of DDR RAM. So, with newer generation we see that the internal data bus also grows and the clock speed is 133 MHz. This is the internal clock of the memory. It has got a controller. And in double data rate RAM this bus clock must be twice this. So, if the bus clock has to be twice this it should be 266.

Now, and the data transfer will takes space both twice in the falling edge and in the rising edge as well as in the falling edge. Now let us see how this calculation is actually happening. So, internal clock is 133 MHz, the bus clock is double of that and we have to calculate the transfer rate.

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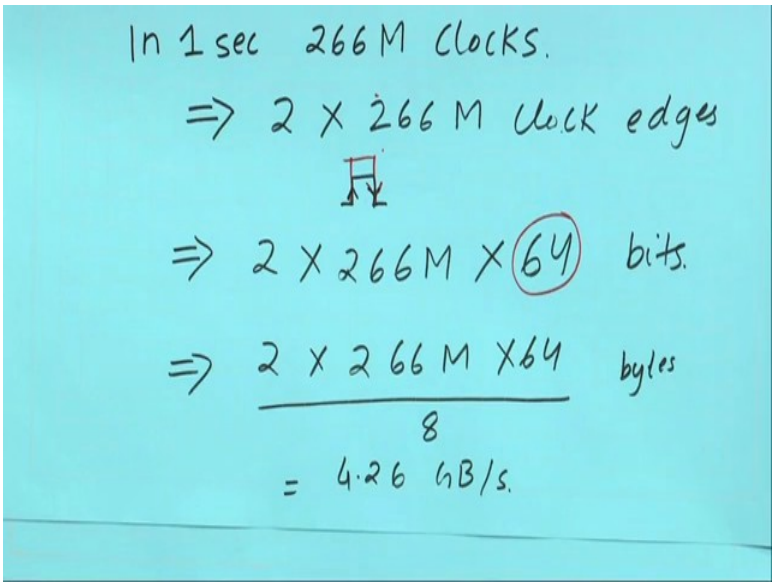

Now, in in 1 second it is 266 MHz, 266 M clocks will be coming. So, if 266 M clocks will be coming and in each clock there is a rising edge and there is a falling edge. So, 2 x 266M clock edges will be there. And in each rising edge and in each falling edge 64 bits of data will be transferred. So, a total of 2 x 266M x 64 bits will be transferred.

So, the transfer rate comes down to 4.26 GBps in case of DDR2.

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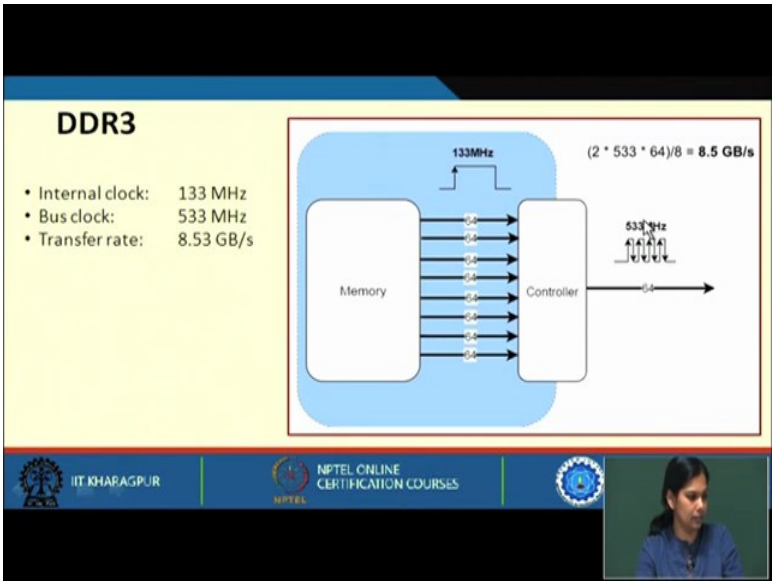

Now, let us see what happens in DDR3. Now DDR3 the internal clock is still this, but now this bus clock has become 533 MHz; means you have how many clocks in between

you have 4 clocks here. So, the width is 64, but you need to have more number of data internal bus between memory and controller. So, we have 8 here.

So, in the same way we can calculate it. So, it will be 2 x 533 MHz now, and each time there will be 64 bit of data will be transferred. If you divide by 8 you will get 8.53 GB per second. So, from DDR2 to DDR3 it was 4.26, now it is 8.53.

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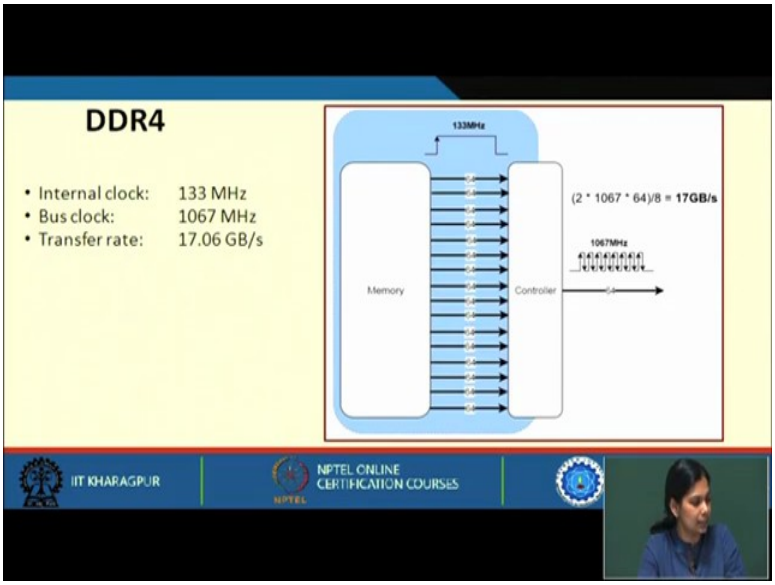

Similarly in DDR4; this is 4 times and then you have 16 such data buses in between. And here you will multiply 2 x 1067 x 64 because each time 64 bits of data will be transferred divided by 8 that is roughly coming around to 17.06 GB per second.

So, as we move on the transfer rate is increasing; transfer rate is becoming faster.

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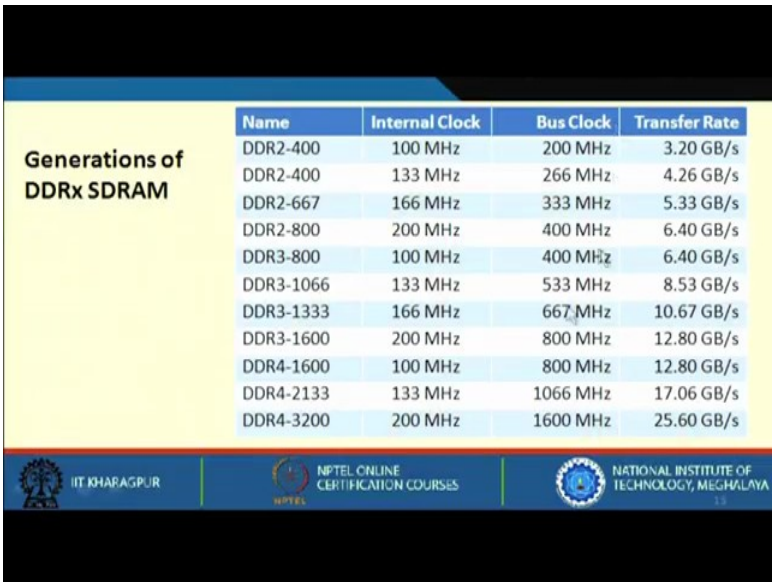

So, across generation we can see that the internal clock frequency has increased. And as the internal clock frequency has increased in the same way bus clock has also increased. And in turn finally, this transfer rate has become very fast, so we have very high transfer rate.

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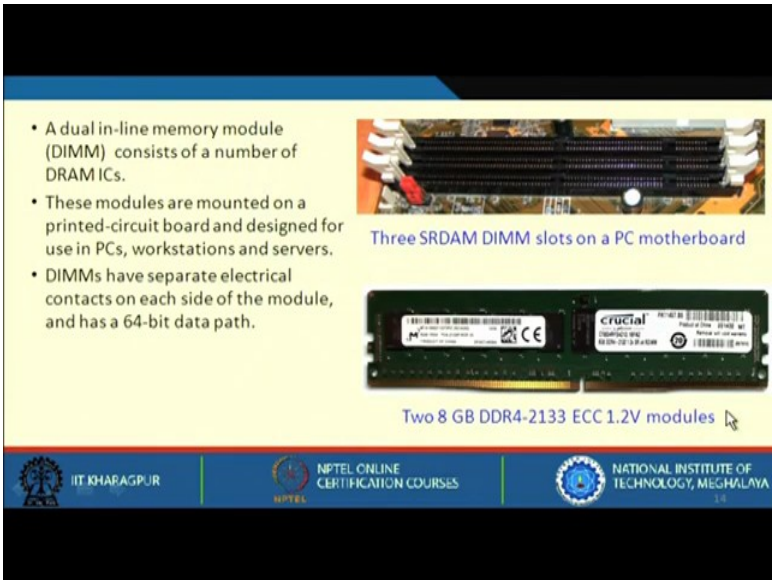

This is a dual in line memory module. These are the slots where these memory modules can fit in. A dual in line memory module consists of number of DRAM ICs. So, you can have number of DRAM ICs put in these places and these modules are mounted on a PCB

and designed for use in PCs, workstations or servers. Inside the PC will be finding that there are some slots that can be put in there.

So, this dual in line memory module have separate electrical contacts on each side of the module and has a 64 bit data paths. So, on each side of the module on this side as well as on the other side it has 64 bit data path.

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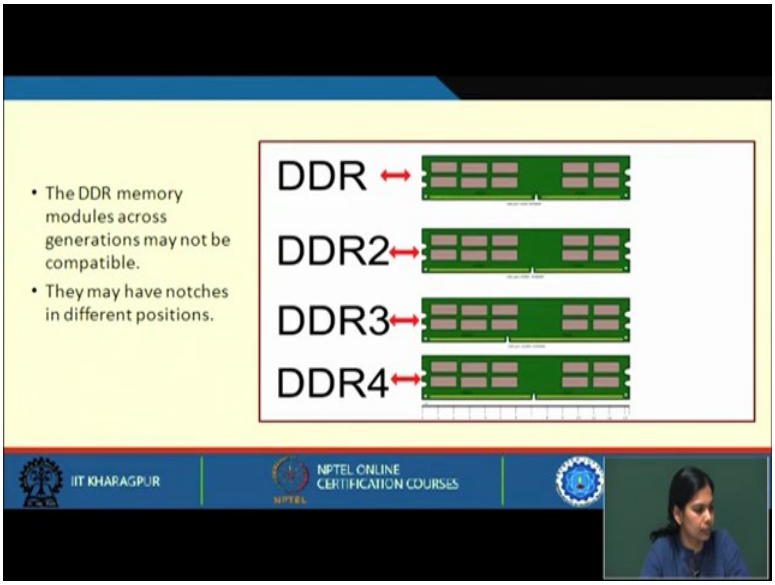

Now, this is one thing we must know that the DDR memory modules across generations may not be compatible. So, you see that this, and this, so DDR2 and DDR4 are compatible almost, but DDR3 is not compatible; they may have notches in different positions. So, the notches may not be in the same positions. So, if a particular slot where we are using DDR3 we may not be able to use DDR4.

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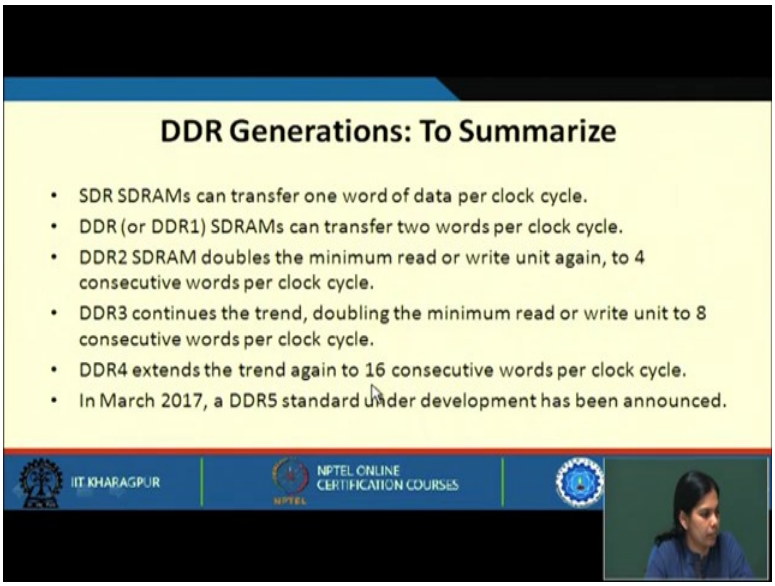

Now to summarize what we discussed about various DDR generations. SDR SDRAM can transfer one word of data per clock cycle. DDR SDRAM can transfer two words per clock cycle; that is double data rate. DDR2 SDRAM doubles the minimum read or write unit again to four consecutive words per clock cycle. In DDR3 it is 8 consecutive words per clock cycle. And DDR4 extends the trend again to 16 consecutive words per clock cycle.

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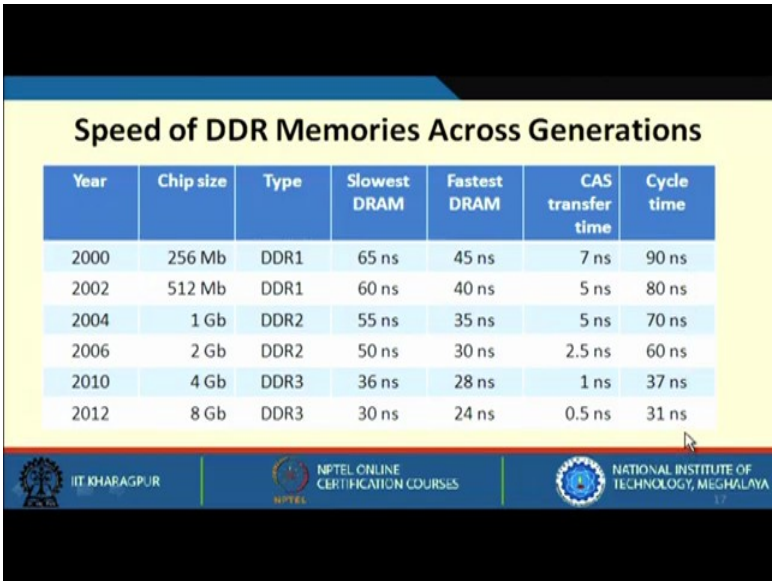

So, this is the speed of DDR memories across generations. Across years we have data till 2012; this is how the chip size has grown, these are the types of DDR memories that we were using, and this is the slowest DRAM that were available, and this is the fastest DRAM that are available. And you see finally, the CAS transfer time because CAS is very important through which will actually determine finally the transfer rate, because we are once we select a row then we just give different columns address to get the data. And finally, the total cycle time comes to this. So, DDR3 with 8 GB chip size has got a cycle time of 31 nanosecond.

So, by this we came to end of lecture 36 where we discussed about synchronous DRAM and the various kind of synchronous DRAM that are there in market that are used today to bridge the speed gap between processors and memory. We will see further that how we can now build larger memories from smaller memory chips, in the next lecture.

Thank you.