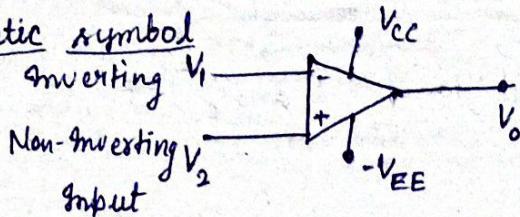


## Lecture 21

operational amplifiers (op-amps)

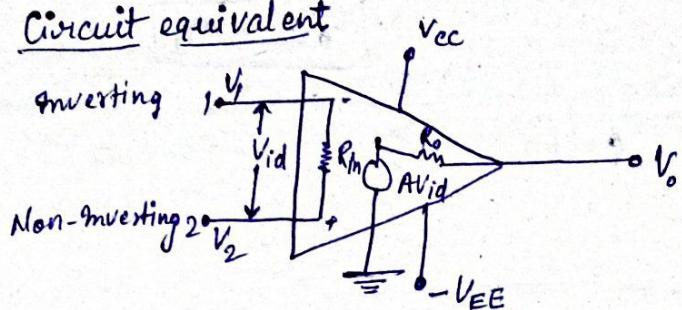
Many mathematical operations can be performed by using it.

Schematic symbol



It is a multistage amplifier, having very high input resistance, very low output resistance, Direct coupling is done, have very high bandwidth (0 Hz - 1 MHz), very high voltage gain. It behaves as Voltage Controlled Voltage Source (VCVS).

Circuit equivalent



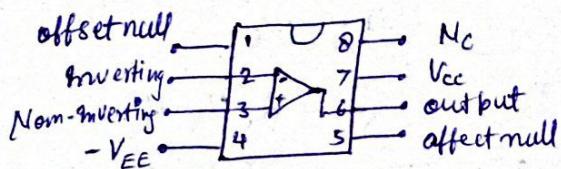
$$V_{id} = V_2 - V_1$$

differential input voltage

$$V_o = A V_{id} \approx A(V_2 - V_1)$$

$$A \approx 10^5$$

IC 741  $\rightarrow$  8-pin op-amp.



offset null is used to cancell / nullify the output voltages due to manufacturing defect.

Pin configuration of IC 741.

characteristics of ideal operational amplifiers

1. Voltage gain =  $\infty$

$$\text{slew rate} = \frac{dV_o}{dt}_{\max}$$

2.  $R_{in} = \infty$

3.  $R_{out} = 0$

4. B.W =  $\infty$

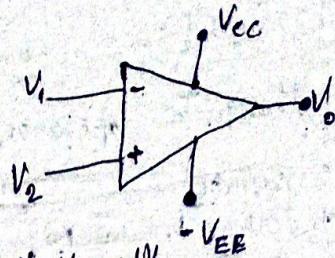
5. Common mode Rejection Ratio =  $\infty$

6. Slew rate =  $\infty$

7. Perfectly match

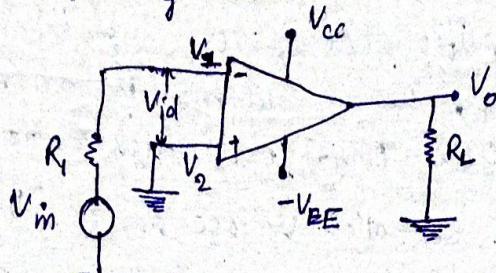
# Open Loop Configurations (in op-amps)

1. Inverting mode
2. Non-Inverting mode
3. Differential mode



Here,  $V_0$  is disconnected to both  $V_1$  and  $V_2$ .

1. Inverting mode

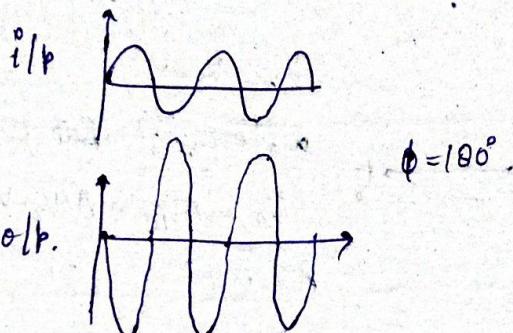


$$V_o = -AV_1$$

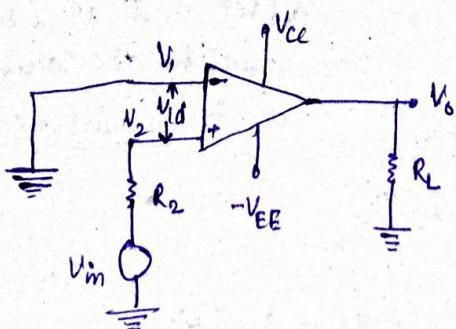
$$V_m \approx V_1$$

$$\begin{aligned} V_o &= A(V_{id}) \\ &= A(V_2 - V_1) \\ &= A(0 - V_1) \end{aligned}$$

$$\boxed{V_o = -AV_1}$$



2. Non-Inverting mode

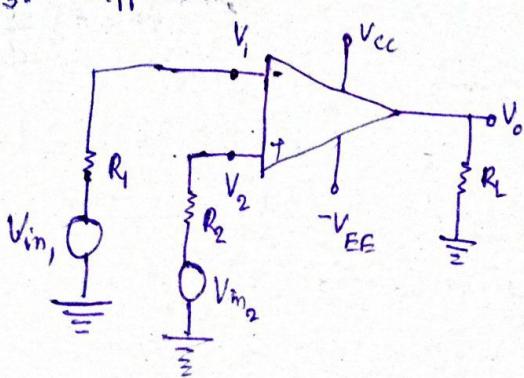


$$V_m = V_2$$

$$\begin{aligned} V_o &= A(V_2 - V_1) \\ &= A(V_2 - 0) \end{aligned}$$

$$\boxed{V_o = AV_2}$$

3. Differential mode



$$V_{m1} = V_1$$

$$V_{m2} = V_2$$

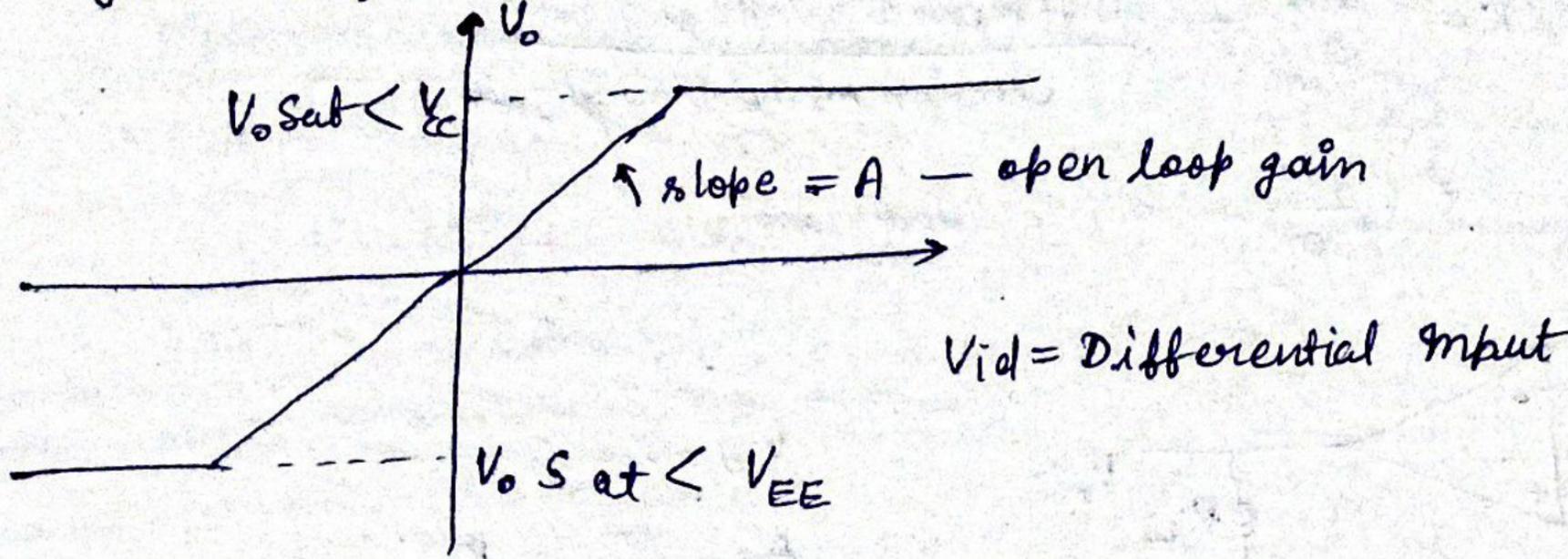
$$V_o = A(V_2 - V_1)$$

$$V_o = A(V_{m2} - V_{m1})$$

$$A \sim 10^5$$

$$V_o = A(V_2 - V_1) = AV_{id}$$

ideal Voltage transfer curve



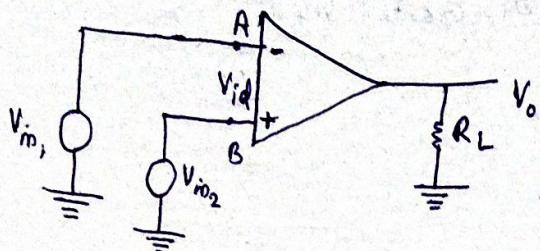
$V_{id}$  = Differential input

## Lecture 22

CMRR (Common mode rejection ratio) =  $\infty$  for an ideal op amp.

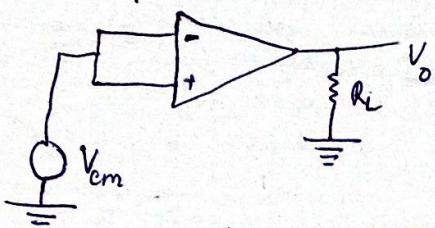
$$\text{CMRR} = \frac{A_d}{A_{cm}} = \frac{\text{Differential Voltage gain}}{\text{Common mode Voltage gain}}$$

$$= \frac{10^5}{0} = \infty \text{ (in ideal case).}$$



$$V_{id} = V_B - V_A$$

$$A_d = \frac{V_o}{V_{id}} = \frac{V_o}{V_B - V_A}$$



$$A_{cm} = \frac{V_o}{V_{cm}} = \frac{V_o}{V_{id}} \approx 0 \quad [\text{in ideal case}]$$

Higher the CMRR, better will be operational amplifier.

As it rejects the noise (i.e. common mode signal).

$$\text{Slew rate} = \frac{dV_o}{dt} \Big|_{\text{max}} = V/m_s = V_m \times 2\pi f_{\text{max}}$$

$$V_o = V_m \sin \omega t$$

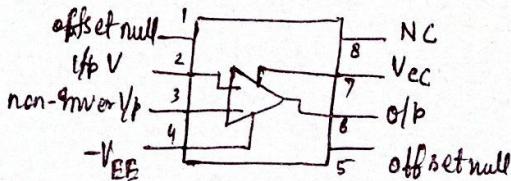
$$\frac{dV_o}{dt} = \omega V_m \cos \omega t$$

$$\frac{dV_o}{dt} \Big|_{\text{max}} = V_m \times \omega$$

$$f_{\text{max}} = \frac{\text{slew rate}}{V_m \times 2\pi} \quad \text{— maximum operational frequency of amp.}$$

If  $f > f_{\text{max}}$ , output will be distorted.

Input offset Voltage



offset Null is the Voltage applied between input of op amp. to get null output Voltage.

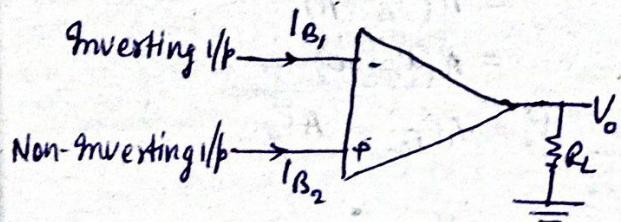
Maximum value of Input offset Voltage is 6mV. in IC741

Due to mismatching there is some output Voltage. To null this we use offset Null.

When input is connected to ground then to nullify Voltage.

Potentiometer is Connected across offset null and parallelly to  $V_{EE}$  and maintaining it.

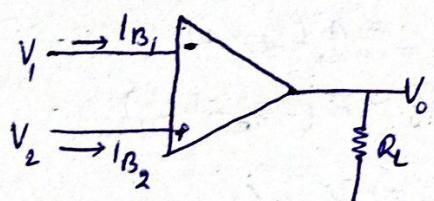
### Input offset current



Maximum value of I<sub>OC</sub> in IC741 = 200nA

$$I_{OC} = |I_{B_2} - I_{B_1}|$$

### Input Bias Current

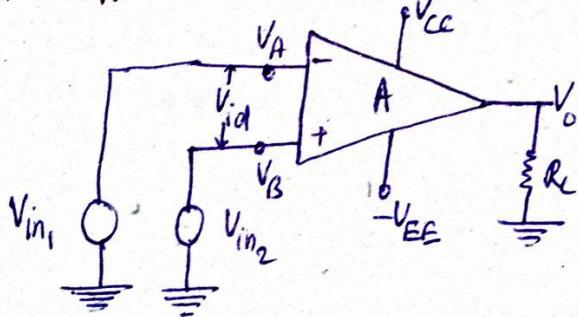


$$I_B = \frac{I_{B_1} + I_{B_2}}{2} = \text{avg. value of input current}$$

$$I_{B\max} = 500 \text{ nA.}$$

### Open loop Configurations in op. amps.

- (1) Inverting Amplifier
- (2) Non Inverting Amplifier
- (3) Differential Amplifier.

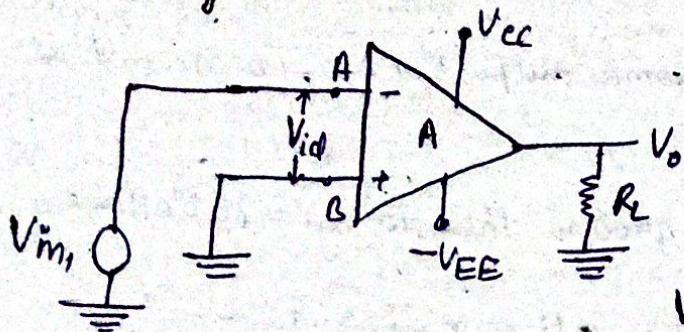


$$\begin{aligned} V_{out} &= A V_{id} \\ &= A(V_B - V_A) \\ &= A(V_{in_2} - V_{in_1}) \\ A &\sim 10^5 \end{aligned}$$

## Linear application

Open loop Conf is generally used to create square waves.

### (1) Inverting Amplifier



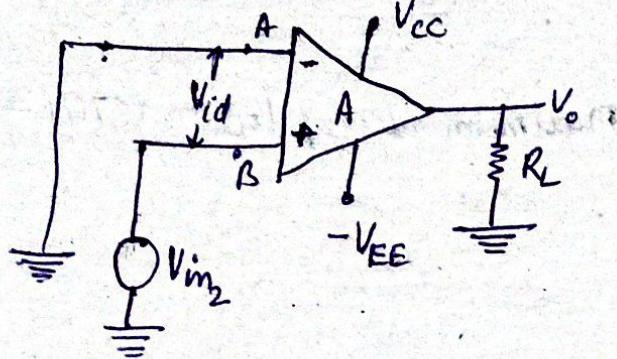
$$A_d = \frac{V_o}{V_{id}} = \frac{A V_{id}}{V_{id}} = A \left( \frac{V_B - V_A}{V_{id}} \right)$$

$$V_o = A (0 - V_{in1})$$

$$V_o = -AV_{in1} = -AV_A$$

$$V_o = -V_{sat} \text{ [small value of } V_{in1}]$$

### (2) Non Inverting Amplifier



$$V_o = A V_{id}$$

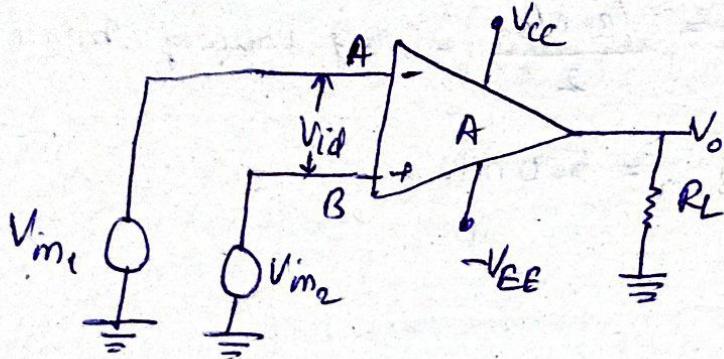
$$= A (V_B - V_A)$$

$$= A (V_{in2} - 0)$$

$$V_o = AV_{in2} = AV_B$$

$$V_o = +V_{sat} \text{ [small value of } V_{in2}]$$

### (3) Differential op Amps.



$$V_o = A V_{id}$$

$$= A (V_B - V_A)$$

$$V_o = A (V_{in2} - V_{in1})$$

$$V_o = \pm V_{sat} \text{ (smaller value of } V_{in})$$

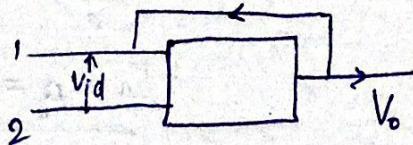
Output Voltage goes to saturation Voltage even for smaller input Voltage in open loop operational Amplifier. So, They are not used for linear application.

## Lecture 23

### Op-Amps

For linear applications, open loop op-amps are not used.

### Closed loops op-Amps



Feedback means giving some output Voltage to input.

Two types of Feedback

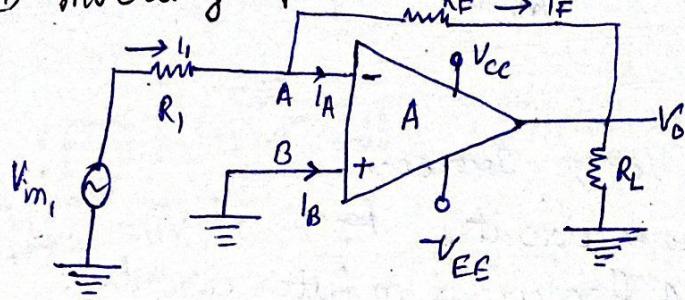
- (I) +ve (II) -ve

-ve feedback is used in closed loop op-Amps. i.e. input and feedback signal is in opposite phase.

### Types of closed loop op-Amps

- (I) Inverting
- (II) Non-inverting
- (III) Differential

#### (I) Inverting Op-Amp in Closed Loop



For ideal case

$$A = \frac{V_{out}}{V_{id}} = \infty = \frac{V_{out}}{V_B - V_A}$$

$$\Rightarrow V_B - V_A = 0 \Rightarrow V_B = V_A = 0. \quad [ \because V_B = 0 ]$$

$$R_{in} = \infty \text{ (ideal case)} \Rightarrow I_A = I_B = 0$$

$\therefore A$  is virtual ground.

$$I_I = I_F$$

$$\frac{V_{in} - V_A}{R_I} = \frac{V_A - V_o}{R_F} \Rightarrow \frac{V_{in}}{R_I} = \frac{-V_o}{R_F} \Rightarrow \frac{V_o}{V_{in}} = -\frac{R_F}{R_I} \quad A_F = \frac{V_o}{V_{in}}$$

$$\Rightarrow A_F = -\frac{R_F}{R_I}. \quad V_o = -\frac{R_F}{R_I} \times V_{in}$$

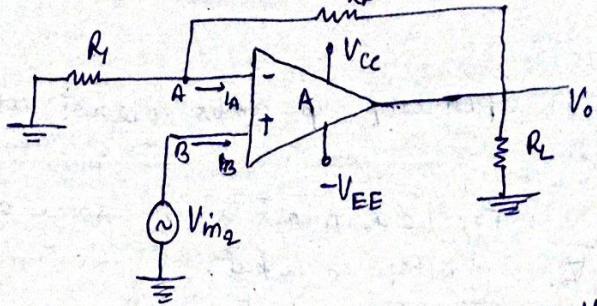
Closed loop gain  
of inverting op-amp

$$= A_F \times V_{in}$$

$$\text{If } R_F = R_I \Rightarrow V_o = -V_{in}$$

This can be used for sign/Phase changer circuit. (Voltage follower  
It is also a VCVS. feedback amplifier)

## (2) Non-inverting op-Amp (Closed loop)



$$i_A = i_B = 0 \quad [R_{in} = \infty, \text{ideal case}]$$

$$A = \frac{V_o}{V_{in2}} = \infty = \frac{V_o}{V_B - V_A}$$

$$V_B - V_A = 0$$

By Virtual ground concept  $V_B = V_A = 0$   $+ V_{in2} = V_{in2}$

$$I_1 = I_F$$

$$\frac{\delta(V_o) - V_A}{R_F} = \frac{V_A - V_o}{R_F}$$

$$\frac{\delta V_{in2}}{R_F} = \frac{V_{in2} - V_o}{R_F}$$

$$V_{in2} R_1 - V_o R_F = -V_{in2} R_F$$

$$V_o R_F = V_{in2} (R_1 + R_F)$$

$$V_o = \frac{R_1 + R_F}{R_1} \times V_{in2}$$

$$\frac{V_o}{V_{in2}} = 1 + \frac{R_F}{R_1}$$

$$A_F = 1 + \frac{R_F}{R_1}$$

$$V_o = A_F \times V_{in2}$$

It is Voltage controlled Voltage source.

This is a voltage follower circuit.  $A_F = 1 \quad V_o = V_{in2}$  If  $R_F = 0$

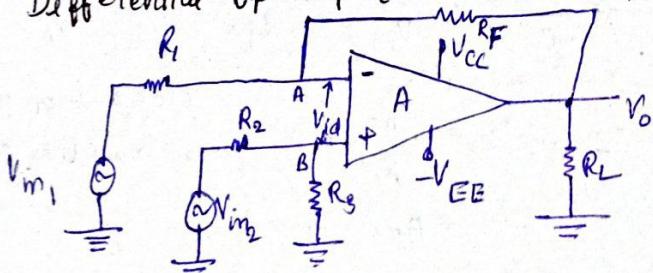
It can be used as a Buffer circuit in filter circuit.

This is also k/a isolation circuit. As  $R_{in}$  is very high  
 $R_{out}$  is very low.

It is Voltage series feedback amp.

$$A_F = 1$$

## (3) Differential op-Amp (in closed loop).



If  $R_1 = R_2$ ;  $R_F = R_3$  then

$$V_{o2} = \left( \frac{R_1 + R_F}{R_1} \right) \left( \frac{R_F}{R_1 + R_F} \right) V_{in2} = \frac{R_F}{R_1} \times V_{in2}$$

$$\therefore V_o = \frac{R_F}{R_1} (V_{in2} - V_{in1}) = -\frac{R_F}{R_1} (V_{in1} - V_{in2})$$

$$V_o = A_F (V_{in1} - V_{in2})$$

By using superposition thm -

$$\text{If } V_{in2} = 0$$

$$V_{o1} = -\frac{R_F}{R_1} \times V_{in1}$$

$$V_o = V_{o1} + V_{o2}$$

$$V_o = -\frac{R_F}{R_1} \times V_{in1} + V_{o2}$$

$$\text{If } V_{in1} = 0$$

$$V_{o2} = \frac{R_3 \times V_{in2}}{R_2 + R_3}$$

$$\left( \frac{R_3}{R_2 + R_3} \right) \left( \frac{R_1 + R_F}{R_1} \right) V_{in2} = V_{o2} = \left( 1 + \frac{R_F}{R_1} \right) \left( \frac{R_3}{R_2 + R_3} \right) V_{in2}$$

So in this case, output of this amp is similar to that of inverting amp. in closed loop.

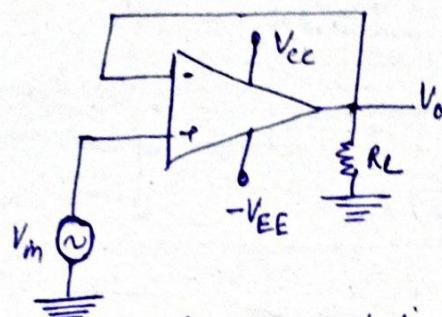
This amp. can be used in 3 modes

- (1) Single ended
- (2) Differential
- (3) Common mode  $V_o = 0$ .

## Lecture 24

Application of op-Amp

(1) Unity gain or Voltage follower op-Amp.

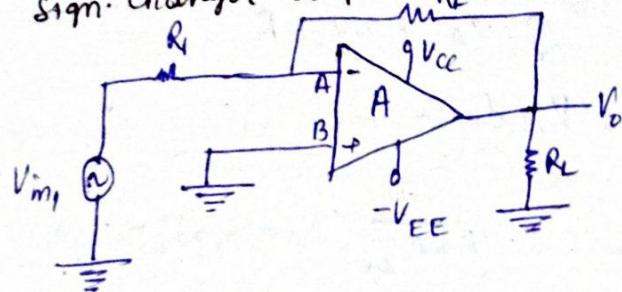


$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_{in}$$

$$V_o = V_{in}$$

If acts as a Buffer or isolation circuit. in filter design

(2) Sign. changer or phase changer

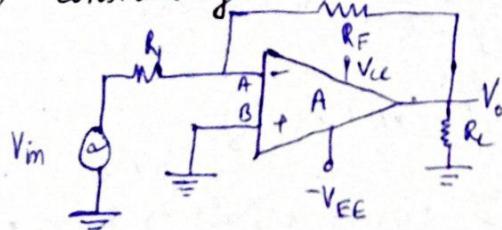


$$V_o = -\frac{R_F}{R_1} \times V_{in}$$

$$\text{If } R_F = R_1 = R$$

$$V_o = -V_{in}, \quad \boxed{A_F = -1} \quad \frac{V_o}{V_{in}} = -1$$

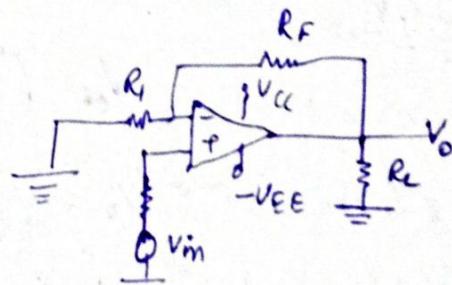
(3) Constant gain multiplier



$$V_o = -\frac{R_F}{R_1} \times V_{in}$$

$$\text{If } \frac{R_F}{R_1} = n$$

$$\Rightarrow V_o = -n V_{in}$$

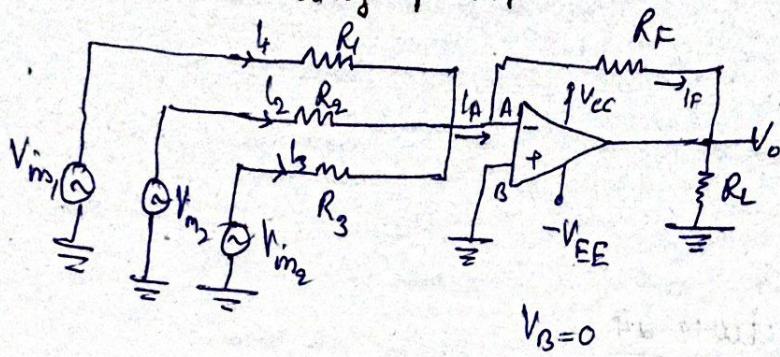


$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_{in}$$

$$V_o = (1 + n) V_{in}$$

(4) Adders or Summaryamps.  
Summing

Inverting op-amp



$$I_A = I_B = 0$$

$$I_F = I_2 + I_1 + I_3$$

$A = \infty$  in ideal case

$$V_{id} = 0$$

$$V_B = V_A = 0$$

$$V_B = V_A = 0$$

$\therefore A$  is at virtual ground.

$$\frac{V_A - V_o}{R_F} = \frac{V_{in_1} - V_A}{R_1} + \frac{V_{in_2} - V_A}{R_2} + \frac{V_{in_3} - V_A}{R_3}$$

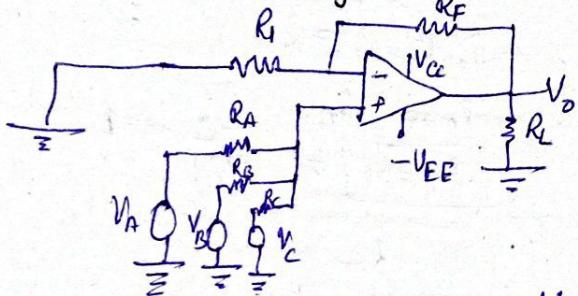
$$\frac{-V_o}{R_F} = \frac{V_{in_1}}{R_1} + \frac{V_{in_2}}{R_2} + \frac{V_{in_3}}{R_3}$$

$$V_o = -R_F \left( \frac{V_{in_1}}{R_1} + \frac{V_{in_2}}{R_2} + \frac{V_{in_3}}{R_3} \right)$$

$$\text{If } R_1 = R_2 = R_3 = R_F$$

$$V_o = -(V_{in_1} + V_{in_2} + V_{in_3})$$

Non-Inverting op-amp.



$$\text{If } R_A = R_B = R_C = R$$

$$V_N \text{ (due to } V_A)$$

$$V_N = \frac{(R/2)}{(R + R/2)} (V_A + V_B + V_C)$$

$$V_o = \left( 1 + \frac{R_F}{R_1} \right) \times \frac{1}{3} (V_A + V_B + V_C)$$

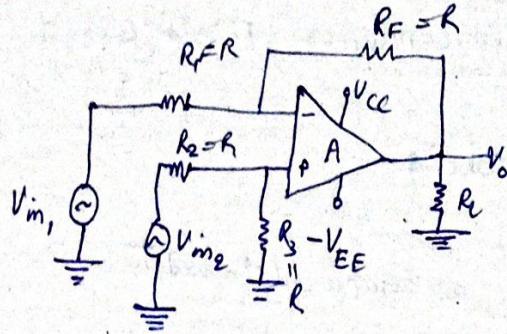
$$[\text{as } n = 3] \quad V_o = V_A + V_B + V_C = V_o = \frac{1}{3} \left( \frac{R_1 + R_F}{R_1} \right) (V_A + V_B + V_C)$$

$$\text{If } n = 1 \quad \boxed{V_o = \frac{V_A + V_B + V_C}{3}}, \quad \text{if } \frac{1 + R_F}{R_1} = n = \text{no. of inputs to non-inverting terminal}$$

It behave as  
averaging circuit.

$$V_o = \frac{n}{3} (V_A + V_B + V_C)$$

(5) Subtractor Circuit amp.



If  $R_1 = R_2$ ;  $R_F = R_3$  then

$$V_o = -\frac{R_F}{R_1} (V_{in_2} - V_{in_1})$$

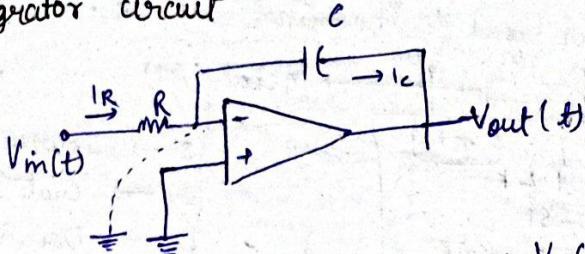
$$= \frac{R_F}{R_1} (V_{in_2} - V_{in_1})$$

$$\text{If } R_1 = R_2 = R_3 = R_F = R,$$

$$V_o = V_{in_2} - V_{in_1}$$

Lecture 25

(6) Integrator circuit



$$i_R = i_C$$

$$i_R = \frac{V_{in}(t)}{R} = i_C$$

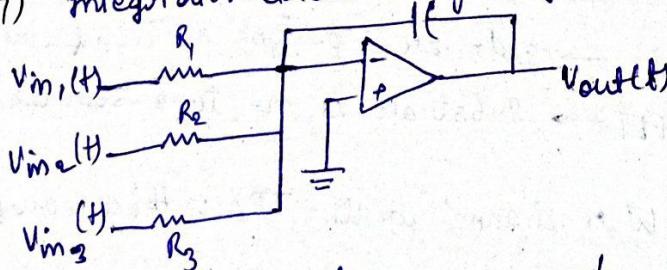
$$V_{out}(t) = -V_C(t)$$

$$V_C(t) = V_C(0) + \frac{1}{C} \int_0^t i_C dt$$

$$= V_C(0) + \frac{1}{C} \int_0^t \frac{V_{in}(t)}{R} dt$$

$$= 0 + \frac{1}{RC} \int_0^t V_{in}(t) dt \quad [\text{If } V_C(0) = 0]$$

(7) Integrator circuit having many inputs



$$V_{out}(t) = - \left[ \frac{1}{R_1 C} \int_0^t V_{in_1}(t) dt + \frac{1}{R_2 C} \int_0^t V_{in_2}(t) dt + \frac{1}{R_3 C} \int_0^t V_{in_3}(t) dt \right].$$

$$V_{out}(t) = -\frac{1}{R_1 C} \int_0^t V_{in_1}(t) dt$$

$$-\frac{1}{R_2 C} \int_0^t V_{in_2}(t) dt +$$

$$-\frac{1}{R_3 C} \int_0^t V_{in_3}(t) dt$$

By virtual ground concept

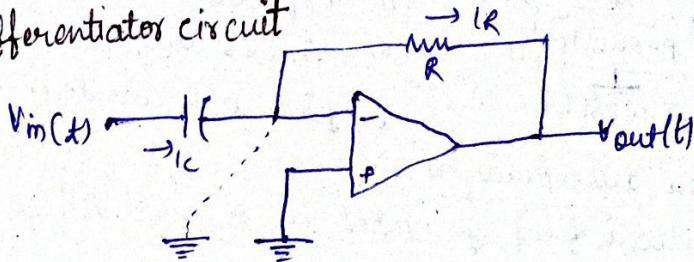
$$i_C = i_R$$

$$i_C = C \frac{d V_{in}(t)}{dt} \quad \text{--- (1)}$$

$$i_R = -\frac{V_{out}(t)}{R} \quad \text{--- (2)}$$

$$V_{out}(t) = -RC \frac{d}{dt} V_{in}(t).$$

(8) Differentiator circuit



Lecture 26  
**MOSFET      Metal Oxide Semiconductor Field Effect  
 Transistor**

It is used in CMOS, digital ICs.

**Advantages**

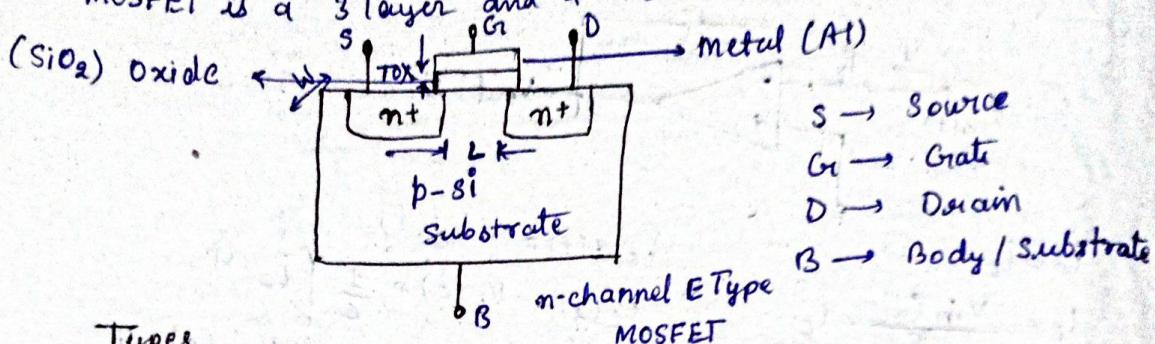
Fabrication Process is easy as compared to BJT.

It occupies less space than BJT.

Power dissipation is small as compared to BJT

MOSFET is used as switching device in LSI and VLSI.

MOSFET is a 3 layer and 4 terminal device.



**Types**

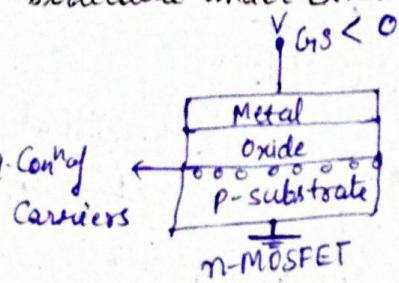
- (I) Enhancement type : Channel has to be created by apply  $V_{GS}$ .
- (II) Depletion type : If  $V_{GS} = 0$  V then channel is already ready.

**Types of Enhancement type**

- (I) n - channel MosFet  $\rightarrow$  substrate is p - type semiconductor.
- (II) p - channel MOSFET  $\rightarrow$  substrate is n - type semiconductor.

L is channel length, W is channel width, TOX is thickness of Oxide.

**MOS structure under External Bias**



Depending on applied Voltage

- (I) Accumulation
- (II) Depletion
- (III) Inversion

vacancies are created.

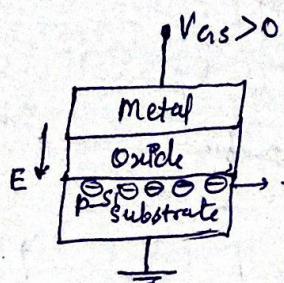
Since conduction takes place in

device by electric field generated by external Voltage applied,

It is, FET i.e. MOSFET.

If  $V_{GS} < 0V$ , then accumulation of holes takes place at oxide-substrate interface layer. This is Accumulation region.

If  $V_{GS} > 0V$  (small) i.e.  $V_{GS} < V_T$

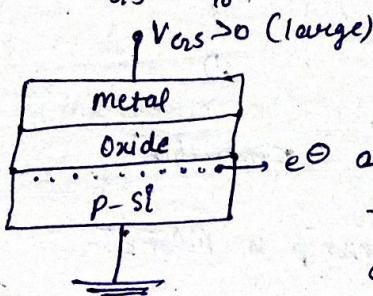


Holes move downward leaving behind fixed-ve acceptor ions.

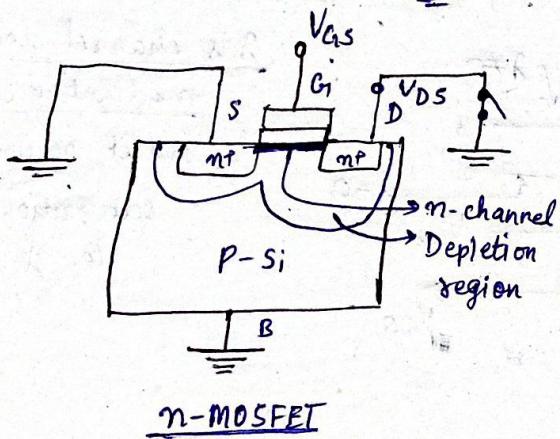
Thus depletion region is created

in which no any free charge exist near oxide substrate interface layer.

If  $V_{GS} \geq 0V$  (large) i.e.  $V_{GS} > V_T$



thus inversion region is created and channel is created and conduction takes place b/w S and D terminal of MOSFET



Drain current  $I_D = f_n(V_{GS}, V_{DS}, V_{BS})$

$V_{GS} \geq V_T$  then channel is created and  $I_D$  flows.

$V_T$  is threshold Voltage of Device

If  $V_{GS} \geq V_T$

and (ii)  $V_{DS} = 0V$ ,  $I_D = 0$  (Cut off mode)

(iii)  $V_{DS}$  is +ve but small

$I_D = +ve$   $I_D \propto V_{DS}$  (Linear mode of operation)

(iv) channel depth towards drain  $\downarrow$  when  $V_{DS} \uparrow$  and it vanishes

if  $V_{DS} = V_{DS}(\text{sat})$ . pinch off point.

This is saturation mode and pinch off condition occurs.

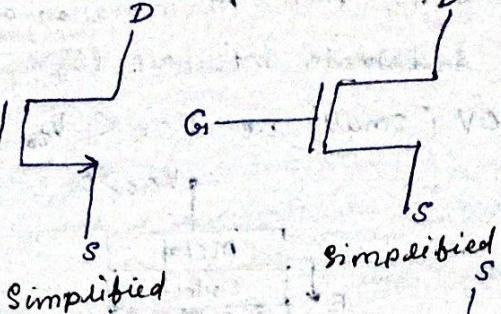
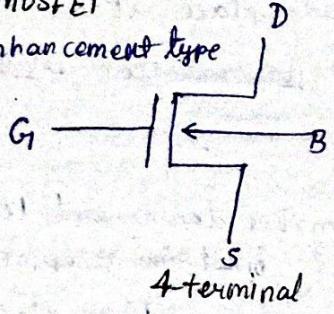
(v) if  $V_{DS} > V_{DS}(\text{sat})$ , pinch off point moves toward

source terminal and length of channel  $\downarrow$  as.

and Depletion depth  $\uparrow$  toward drain terminal.

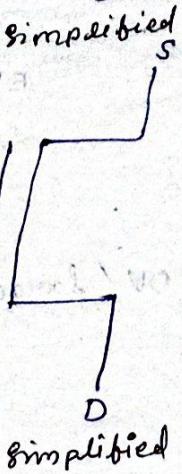
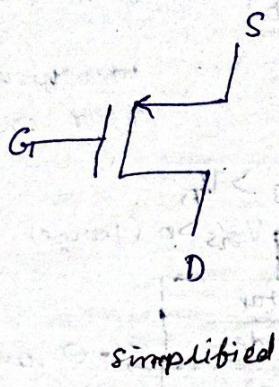
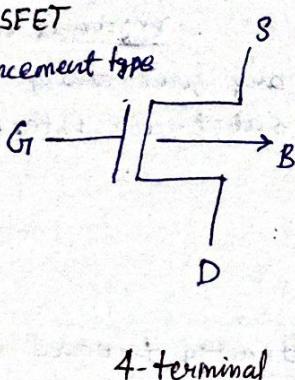
$$L_{eff} = L - AL$$

$n$ -MOSFET  
Enhancement type

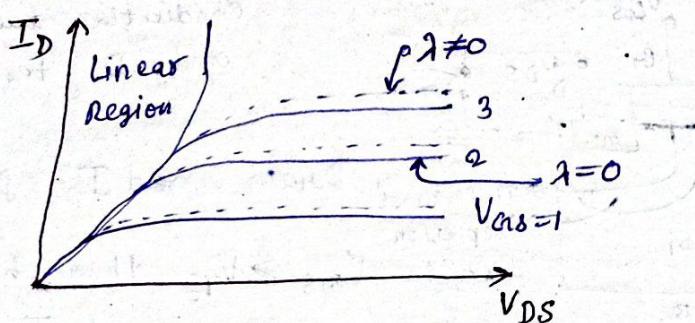


$p$ -MOSFET

Enhancement type



### Current - Voltage Relationship in MOSFET



$\lambda$  is channel length modulation coefficient and it occurs only in saturation mode.  
i.e.  $\lambda \neq 0$ .

Linear region ( $\lambda=0$ ):

$$I_D \propto V_{DS}$$

when  $V_{GS} \geq V_T$ ,  $V_{DS} < V_{GS} - V_T$

$$I_D(\text{lin}) = \frac{\mu_n C_{ox}}{2} \times \frac{W}{L} \left[ 2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right]$$

$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2} \frac{W}{L'} (V_{GS} - V_T)^2 ; L' = L - \Delta L$$

$$1 - \frac{\Delta L}{L} \approx 1 - 2V_{DS}$$

$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$I_D(\text{cutoff}) = 0$$

$\mu_n \rightarrow$  mobility of  $e^-$

$C_{ox} \rightarrow$  Gate oxide capacitance per unit area

Substrate effect

If  $V_{BS} \neq 0V$ , then  $V_T$  varies. It is k/a Substrate Bias effect.

$V_{T0}$  → threshold voltage when  $V_{BS} = 0V$

Considering Channel length modulation and Substrate Bias effects

$I_D = 0$ . when  $V_{GS} < 0V$ .

n-channel MOSFET

$$I_D = \frac{4nCox}{2} \frac{W}{L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad \begin{array}{l} V_{GS} \geq V_T \\ V_{DS} < V_{GS} - V_T \end{array}$$

$$I_D (\text{sat}) = \frac{4nCox}{2} \frac{W}{L} (V_{GS} - V_{DS})^2 (1 + \gamma V_{DS}) \quad \begin{array}{l} V_{GS} \geq V_T \\ V_{DS} \geq V_{GS} - V_T \end{array}$$

For p-channel MOSFET, the system constraints are changed with same eqn. i.e. becomes opposite.

## Lecture 27

### Number System

- (1) Binary
- (2) Octal
- (3) Decimal
- (4) Hexadecimal

No. Systems	Base	Symbols Used	Examples
Binary no. system	2	0, 1	101.111
Octal no. system	8	0, 1, 2, 3, 4, 5, 6, 7	47.65
Decimal no. system	10	0, 1, 2, 3, 4, 5, 6, 7, 8, 9	89.75
Hexadecimal no. system	16	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F	1A.F

### (A) Conversion of Number system

$$D \rightarrow B \quad (2)_{10} \rightarrow (10)_2$$

$\uparrow$   
 digit              bit

Combination of 4 bit  $\rightarrow$  Nibble  
 "                  8 bit  $\rightarrow$  1 byte

$$(4.6)_{10} \rightarrow (100.)_2$$

1001

D  $\rightarrow$  octal

$$(4.8)_{10} \rightarrow (4.631)_8$$

D  $\rightarrow$  Hexadecimal

$$(16.1)_{10} \rightarrow (10.19)_{16}$$

### (B) Binary no. System

$$B \rightarrow \text{octal} \quad (1010.1101)_2 \rightarrow (12.64)_8$$

$$B \rightarrow \text{Decimal} \quad (1010.1101)_2 \rightarrow (10.75)_{10}$$

$$B \rightarrow \text{Hexadecimal} \quad (1010.1101)_2 \rightarrow A.D$$

## Lecture 2B

Decimal	Binary	Octal	Hexadecimal
0	0	0	0
1	1	1	1
2	10	2	2
3	11	3	3
4	100	4	4
5	101	5	5
6	110	6	6
7	111	7	7
8		10	8
9	1000	11	9
10	1001	12	A
11	1010	13	B
12	1011	14	C
13	1100	15	D
14	1101	16	E
15	1110	17	F
	<u>1111</u>		

(C) Octal no. system

$$0 \rightarrow \text{Decimal} \quad (17)_8 \rightarrow (15)_{10}$$

$$0 \rightarrow \text{Binary} \quad (17)_8 \rightarrow (001\ 111)_2$$

$$0 \rightarrow \text{Hexadecimal} \quad (17)_8 \rightarrow (0F)_{16} \rightarrow (F)_{16}$$

(D) Hexadecimal no. system

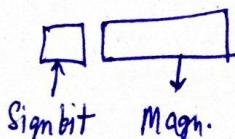
$$H \rightarrow \text{Decimal} \quad (1A)_{16} \rightarrow (26)_{10}$$

$$H \rightarrow \text{Binary} \quad (1A)_{16} \rightarrow (0001\ 1010)_2$$

$$H \rightarrow \text{Octal} \quad (1A)_{16} \rightarrow (32)_8$$

Signed Binary number

(I) Sign-Magnitude Representation



$$\begin{array}{|c|c|} \hline \text{S} & \text{M} \\ \hline \end{array} \begin{array}{|c|c|} \hline \text{S} & \text{M} \\ \hline \end{array}$$

$$\begin{array}{|c|c|} \hline 0 & 101 \\ \hline \end{array} \quad \begin{array}{|c|c|} \hline 1 & 101 \\ \hline \end{array}$$

## 2. 1's complement representation

$$+5 = \boxed{0}101$$

$$-5 = \boxed{1}010$$

↓ the most significant bit.

## 3. 2's complement representation

$$+5 = \boxed{0}101 \quad 1's\; Complement\; 1\; (in\; LSB)$$

$$-5 = \boxed{1}011 \rightarrow \text{LSB}$$

MSB for +ve →  $\boxed{0}$

MSB for -ve →  $\boxed{1}$

## Primary Arithmetic operation

### Addition

$$0+0=0$$

$$0+1=1$$

$$1+0=1$$

$$1+1=0,1$$

### Subtraction

$$0-0=0$$

$$0-1=1,2$$

$$1-0=1$$

$$1-1=0$$

## Arithmetic operation by using one's complement

$$\begin{array}{r} 7 \\ -5 \\ \hline \end{array} \quad 0111$$

$$\begin{array}{r} 0101 \\ +1010 \\ \hline \end{array} \rightarrow 1+1=2$$

$$\begin{array}{r} 2 \\ 10 \\ \hline \end{array} \quad +1010 \rightarrow -5$$

$$\begin{array}{r} 1,0001 \\ +1 \\ \hline \end{array} \quad \Rightarrow 1+1=2.$$

$$\begin{array}{r} +1 \\ \hline 0010 \end{array}$$

$$\begin{array}{r} 5 \\ -7 \\ \hline \end{array} \quad 0101$$

$$\begin{array}{r} 7 \\ -2 \\ \hline \end{array} \quad 0111$$

$$\begin{array}{r} -2 \\ -10 \\ \hline \end{array} \quad 1000$$

If carry is generated  
then add it to LSB.

If carry is not generated  
then Result is  $-(1's\; Complement)$

$$\begin{array}{r} 0101 \\ +1000 \\ \hline 1101 \end{array}$$

$$\text{Result} = -[\text{1's complement of } 1101]$$

$$= -[0010] = -2$$

Arithmetic operations using 2's complement

$$\begin{array}{r} 7 \\ -5 \\ \hline 2 \end{array} \quad \begin{array}{r} 0111 \\ 0101 \\ 1011 \text{ [2's complement]} \\ \hline \end{array} \quad \begin{array}{r} 0111 \\ + 1011 \\ \hline 10010 \end{array}$$

Carry is ignored

$$\begin{array}{r} 5 \\ -7 \\ \hline -2 \\ -10 \end{array} \quad \begin{array}{l} \rightarrow 0101 \\ \cdot 0111 \\ 1000 \rightarrow 1's \\ 1001 \rightarrow 2's \end{array}$$

$$\begin{array}{r} 0101 \\ 1001 \\ \hline 1110 \end{array}$$

If carry is not generated then  
Result is

$$-[0001]$$

$$+ 1$$

$$-\boxed{0010}$$

9's complement and 10's complement representation

↑  
1's complement (in Binary)

↓  
2's complement (Binary)

$$\begin{array}{r} 7 \\ + 4 \\ \hline \boxed{11} \end{array} \Rightarrow 1+1=2.$$

$$\begin{array}{r} 7 \\ -5 \\ \hline 2 \end{array}$$

$$\begin{array}{r} 5 \\ -7 \\ \hline -2 \end{array}$$

$$\begin{array}{r} 5 \\ 2 \\ \hline 7 \end{array}$$

$$\begin{aligned} &= -(9's \text{ comp of } 7) \\ &= -2 \end{aligned}$$

Operations using 10's complement

$$\begin{array}{r} 7 \\ -5 \\ \hline 2 \end{array} \quad \begin{array}{r} 7 \\ 5 \\ \hline \boxed{12} \end{array}$$

Ignore it

$$\begin{array}{r} 5 \\ -7 \\ \hline -2 \end{array} \quad \begin{array}{r} 5 \\ + 3 \\ \hline 8 \end{array}$$

$$10's \text{ comp} = 9's \text{ comp} + 1 \text{ (at LSB)}$$

$$-[10's \text{ comp of } 8] = -2: \text{ Ans}$$

## Lecture 29

Logic Gates is an integrating circuit used in designing digital circuit, digital expression/function.

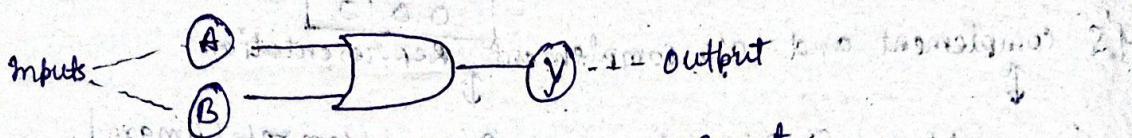
**Basic Gates:**

(1) AND gate

(2) OR gate

(3) NOT gate

(1) OR gate is an integrating device have 2 or more input and one output.



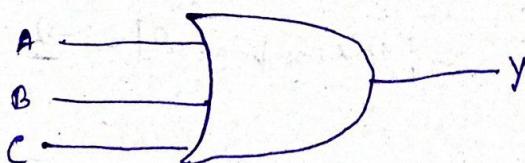
Logic symbol of a 2 input OR gate

$$y = A + B \rightarrow \text{logic expression}$$

logic OR

Truth Table

inputs		outputs	
A	B	$y = A + B$	
0 → logic '0' or low ≈ 0V	0	0	0
0	1	1	1
1 → logic '1' or high ≈ 5V	0	1	1
1	1	1	1



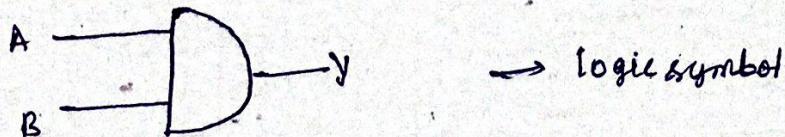
logic symbol of 3 input OR gate

$$y = A + B + C$$

Truth Table

inputs			Output	
A	B	C	$y = A + B + C$	
0	0	0	0	0 0 0 1
0	0	1	1	1 0 1 1
0	1	0	1	1 1 0 1
0	1	1	1	1 1 1 1

(2) AND gate

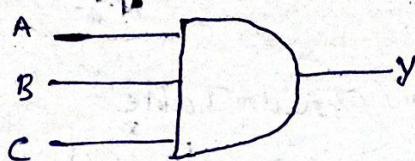


$y = A \cdot B = AB$  → logic expression  
logic OR or logic multiplication

A	B	$y = AB$
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table

two input AND gate



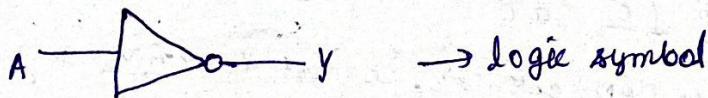
logic symbol

$$y = A \cdot B \cdot C$$

Truth Table

A	B	C	$y = A \cdot B \cdot C$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(3) NOT gate



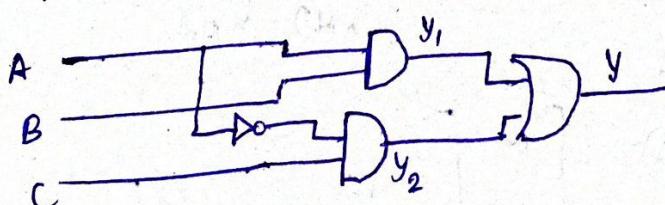
$y = \bar{A}$  or  $A'$  → logic expression

$$\begin{array}{l} 0' \rightarrow 1 \\ 1' \rightarrow 0 \end{array}$$

Truth Table

A	$y = \bar{A}$
0	1
1	0

$$Y = AB + \bar{A}C$$



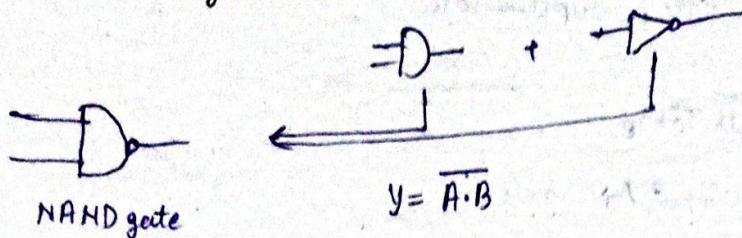
$$Y = y_1 + y_2$$

$$= AB + \bar{A}C$$

## Universal Gates

- NAND gate
- NOR gate

(1) NAND gate  $\Rightarrow$  AND gate + NOT gate

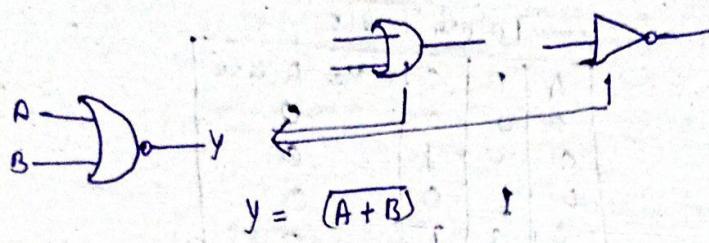


Truth Table

		X	Y = \overline{A \cdot B}
A	B	A \cdot B	
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

N.g.

(2) NOR gate  $\Rightarrow$  OR gate + NOT gate



Truth Table

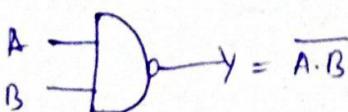
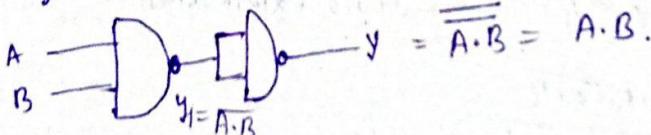
		X	Y = \overline{A + B}
A	B	A + B	
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

N.g.

By Connecting two inputs of NAND gate

it is converted to NOT gate

By Connecting NOT gate to NAND gate it is converted to AND gate



$$= \overline{\overline{A}} + \overline{\overline{B}}$$

$$= \bar{\bar{A}} + \bar{\bar{B}}$$

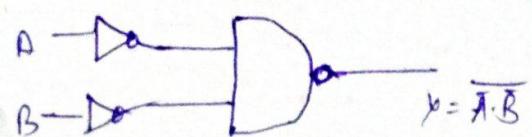
$\boxed{Y = A + B} \rightarrow \text{OR gate}$

DeMorgan's Thm

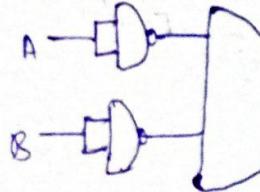
$$1. (A + B + C + D \dots)' = A' \cdot B' \cdot C' \cdot D' \dots$$

$$2. (A \cdot B \cdot C \cdot D \dots)' = A' + B' + C' + \dots$$

NAND  $\rightarrow$  OR



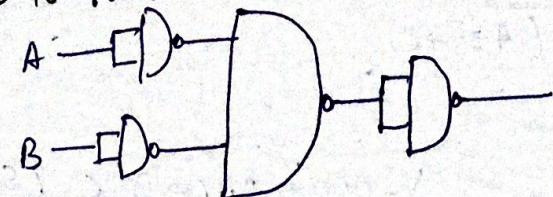
$$=$$



$$Y = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}}$$

$$= A + B$$

NAND to NOR

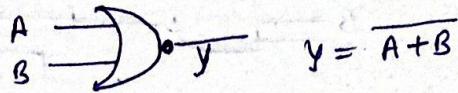


$$Y = \overline{A+B}$$

### Lecture 30 (Thirty)

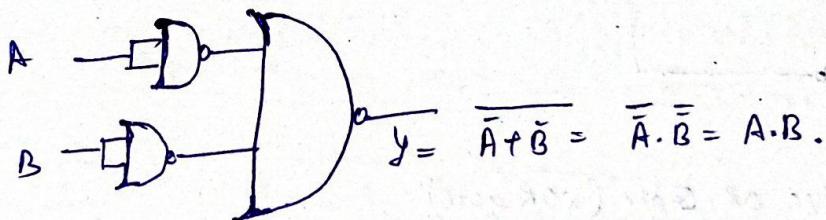
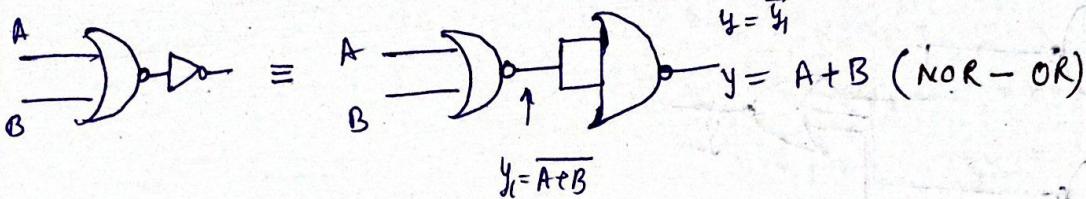
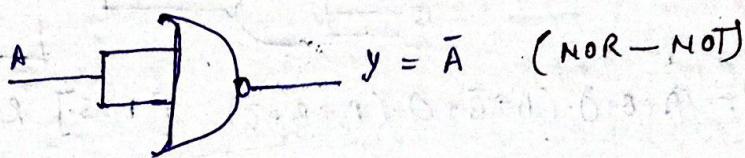
Conversion of NOR gate to BASIC gates

(1) AND :



(2) OR

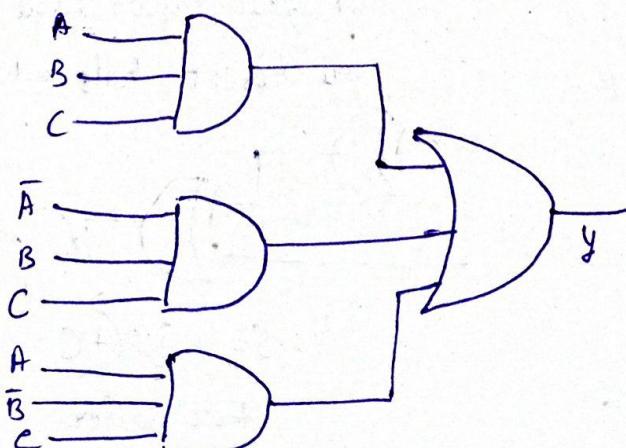
(3) NOT



1. AND-OR representation

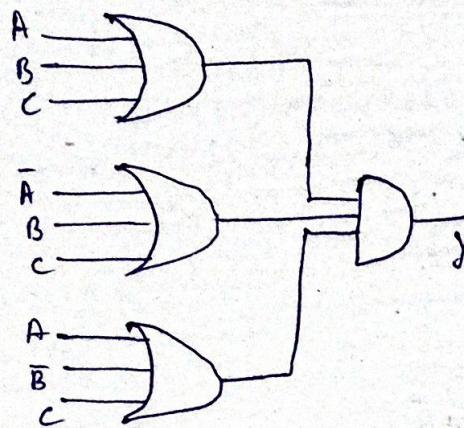
2. OR- AND representation

$$A, B, C \quad Y = AB + \bar{A}BC + A\bar{B}C \quad [ \text{sum of Product form} ]$$



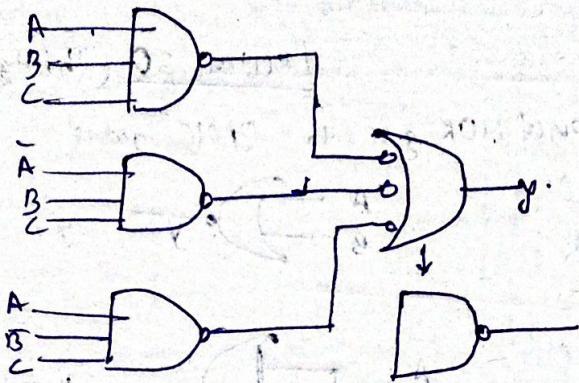
## 2. OR- AND Representation

$$Y = (A+B+C) \cdot (\bar{A}+B+C) \cdot (A+\bar{B}+C)$$



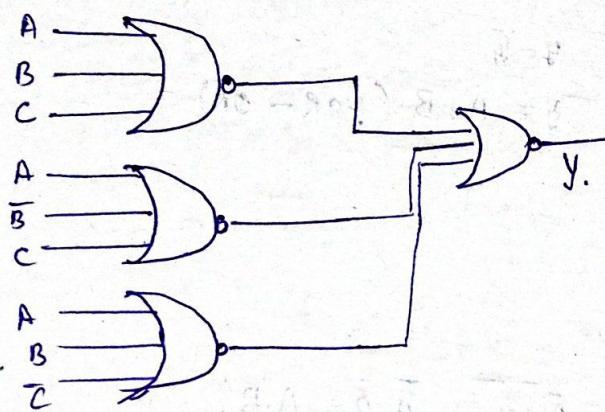
$$Y = ABC + \bar{A}BC + A\bar{B}C \quad (\text{SOP})$$

Represent it by only using NAND gate



$$Y = (A+B+\bar{C}) \cdot (A+\bar{B}+C) \cdot (A+B+\bar{C})$$

[ POS ] Represent it by only NOR gate



## Exclusive OR Gate (XOR gate)



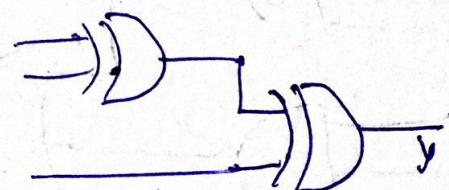
$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

XOR gate

Truth Table

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

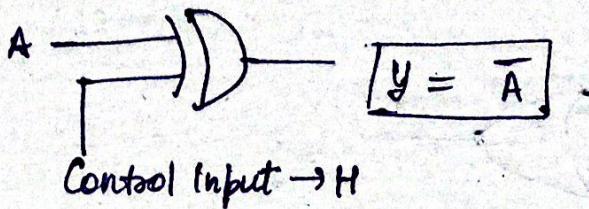
XOR gate can be used to represent half adder.



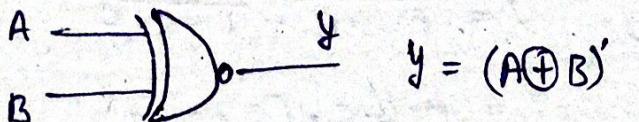
$$Y = S = A \oplus B \oplus C$$

Full adder

## Applications of XOR gate - Controlled Inverters



## Exclusive NOR gate (XNOR gate)



$$Y = A \odot B = AB + \bar{A}\bar{B}$$

$$A \cdot \bar{A} = 0$$

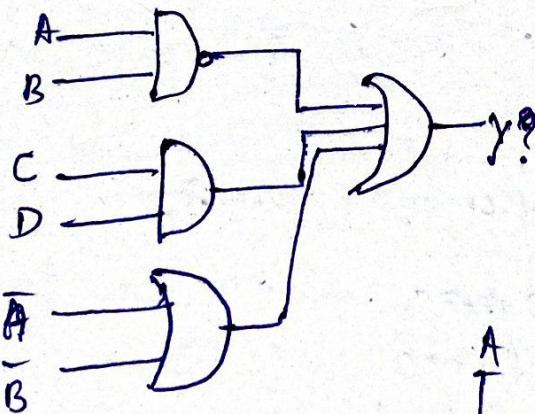
$$A \cdot A = A$$

Truth table

A	B	$y = A \odot B$	$A + \bar{A} = 1$
0	0	1	$1 + 1 = 1$
0	1	0	$1 + 0 = 1$
1	0	0	$1 \cdot 0 = 0$
1	1	1	

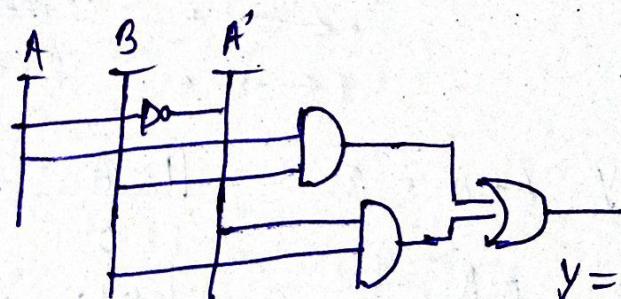
→ Truth Table

- 1. for 1-bit Comparator Ckt.
- 2. Even parity checker



$$y = (A \cdot B)' + C \cdot D + (\bar{A} + \bar{B})$$

Design  $y = AB + A'B'$



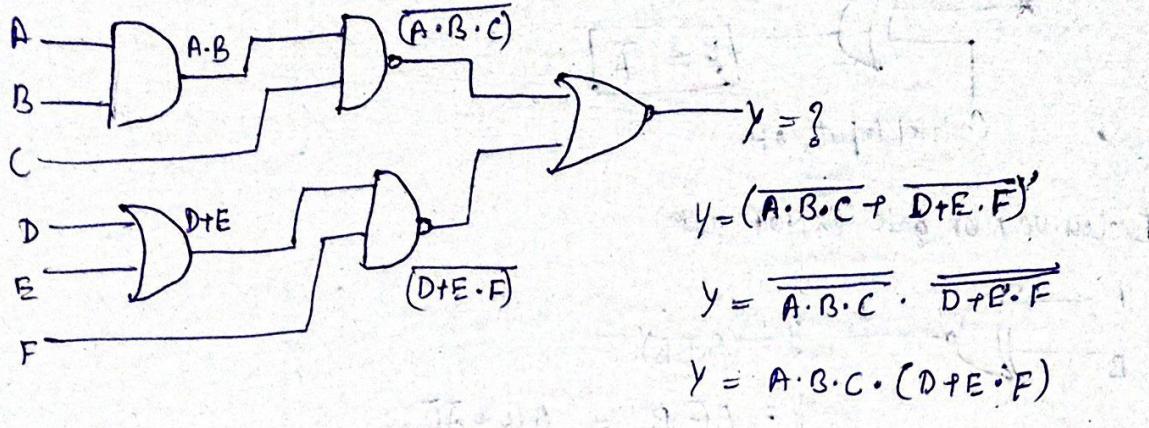
$$y = AB + A'B'$$

DeMorgan's theorem

$$(A + B)' = A' \cdot B'$$

$$(A \cdot B)' = A' + B'$$

## Lecture 31



By Demorgan's thm

### Boolean Algebra

- (1) Commutative, (2) Associative Property

$$A + B = B + A$$

$$A + (B + C) = (A + B) + C$$

$$A \cdot B = B \cdot A$$

$$A \cdot (B \cdot C) = (A \cdot B) \cdot C$$

3. Distributive Property

- $A + B \cdot C = (A + B) \cdot (A + C)$

$$A \cdot (B + C) = A \cdot B + A \cdot C$$

### Duality Principle

You can get dual of any expression by converting

$$\begin{array}{ccc} \cdot & \leftrightarrow & + \\ + & \leftrightarrow & \cdot \\ 0 & \leftrightarrow & 1 \\ 1 & \leftrightarrow & 0 \end{array}$$

Let  $y = A + A = A$

$$\begin{aligned} 1 + A &= 1 \\ 1 + 0 &= 1 \\ 1 + 1 &= 1 \end{aligned}$$

$$\begin{aligned} 0 \cdot A &= 0 \\ 1 + A &= 1 \end{aligned}$$

Dual

: Dual of  $y$ :  $\underline{A \cdot A = A}$

$$\boxed{A + \bar{A} = 1}$$

$$\boxed{A \cdot \bar{A} = 0}$$

$$A + B C = (A + B)(A + C)$$

$$0 + 1 = 1$$

$$0 \cdot 1 = 0$$

$$\bar{\bar{A}} = A$$

$$1 + 0 = 1$$

$$1 \cdot 0 = 0$$

Reduce  $y = AB + A\bar{B}$

$$= A(B + \bar{B})$$

$$y = A(1) = A$$

$$y = \bar{A}B + AB + ABC$$

$$= B(A + \bar{A}) + ABC$$

$$= B + ABC$$

$$= B(1 + AC)$$

$$= B$$

A → Reduce the following logic functions by boolean algebra —

$$\textcircled{1} \quad Y = A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C} + ABC$$

$$\textcircled{2} \quad Y = (A+B+C)(A+\bar{B}+C)(\bar{A}+B+\bar{C})$$

B → Write the dual of following logic expressions —

$$\textcircled{1} \quad y = A \cdot B + A \cdot C \quad \textcircled{4} \quad A + \bar{A} = 1$$

$$\textcircled{2} \quad y = A + 0 = A$$

$$\textcircled{3} \quad A \cdot \bar{A} = 0$$

C - Write complement of following and Reduce the same —

$$Y = \overline{(A+B+C)(\bar{A}+\bar{B}+\bar{C})(\bar{A}+B+\bar{C})}$$

$$Y = \overline{ABC + \bar{A}BC + AB\bar{C} + \bar{A}\bar{B}\bar{C}}$$

$$A - \textcircled{1} \quad Y = A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C} + ABC$$

$$= BC(A+\bar{A}) + \bar{B}\bar{C}(A+\bar{A}) = BC + \bar{B}\bar{C} = 1.$$

$$\textcircled{2} \quad (A+B+C)(A+\bar{B}+C)(\bar{A}+B+\bar{C})$$

$$= (AA + A\bar{B} + AC + BA + BB + BC + CA + CB + CC)(\bar{A}+B+\bar{C})$$

$$= (A(B+\bar{C}) + C(\bar{B}+B) + AC + A+C)(\bar{A}+B+\bar{C})$$

$$= (A+C + AC + A+C)(\bar{A}+B+\bar{C})$$

$$= (A+C + AC)(\bar{A}+B+\bar{C})$$

$$= \cancel{AA} + AB + A\bar{C} + \cancel{CA} + CB + \cancel{CC} + A\bar{A}C + A\bar{B}C + \cancel{AC}^0$$

$$= AB + C(\bar{A}+B) + A\bar{C} + AC(\bar{A}+B)$$

$$= A(B+\bar{C}) + C(\bar{A}+B)[1+A]$$

$$= A(B+\bar{C}) + C(\bar{A}+B).$$

$$B - \textcircled{1} \quad y = (A+B) \cdot (A+C) \quad \textcircled{2} \quad A \cdot 1 = A \quad \textcircled{3} \quad A + \bar{A} = 1 \quad \textcircled{4} \quad A \cdot \bar{A} = 0$$

$$C - \textcircled{1} \quad y' = (A+B+C)(\bar{A}+\bar{B}+C)(\bar{A}+B+\bar{C}) = (\cancel{AA}) + AB + A\bar{C} + B\bar{A} + BB + B\bar{C} + C\bar{A} + CB + \cancel{CC}^0 (A+\bar{B}+C)$$

$$= (B+B+\bar{B}+\bar{A}\bar{C}+\bar{C})(\bar{A}+\bar{B}+\bar{C})$$

$$= B(\bar{A}+\bar{C}) + (\bar{B}+\bar{C})(A\bar{C} + \bar{A}C),$$

$$\textcircled{11} \quad y' = ABC + \bar{A}BC + AB\bar{C} + \bar{A}\bar{B}\bar{C}$$

$$= AB(C+\bar{C}) + \bar{A}(BC+\bar{B}\bar{C}) = AB + \bar{A}.$$

## Lecture 32

### SOP & POS

Sum of Products

Sum terms

$$A + B + C$$

logic OR  $\rightarrow$  '+'

Variables  $\rightarrow A, B, C$

Product of sums

$$\bar{A} + B + C$$

$\uparrow$  OR operator.

also K/a Max.

terms ( $M_i$ )

Product of sum term

$$= (A + B + C) \cdot (\bar{A} + B + C) \cdot (\bar{A} + \bar{B} + \bar{C})$$

Product term

$$ABC$$

also K/a Min terms  $\cdot (m_i)$

Variables  $\rightarrow A, B, C$

$$\bar{A} \bar{B} \bar{C}$$

$$\bar{A} BC$$

logic AND  $\rightarrow$

Sum of Product terms

$$ABC + \bar{A}BC + A\bar{B}\bar{C}$$

Sum of Product terms for two variables

Variables  $\rightarrow A, B$

$$A$$

$$B$$

Product/min term

$$0$$

$$0$$

$$A'B' \rightarrow m_0$$

$$0$$

$$1$$

$$A'B \rightarrow m_1$$

$$1$$

$$0$$

$$AB' \rightarrow m_2$$

$$1$$

$$1$$

$$AB \rightarrow m_3$$

for 3 Variables

Variables  $\rightarrow A, B, C$

$$A \quad B \quad C$$

$m_i$  (min term)

$$0 \quad 0 \quad 0$$

$$A'B'C' = m_0$$

$$0 \quad 0 \quad 1$$

$$A'B'C = m_1$$

$$0 \quad 1 \quad 0$$

$$A'B'C' = m_2$$

$$0 \quad 1 \quad 1$$

$$A'B'C = m_3$$

$$1 \quad 0 \quad 0$$

$$A'B'C' = m_4$$

$$1 \quad 0 \quad 1$$

$$A'B'C = m_5$$

$$1 \quad 1 \quad 0$$

$$A'BC' = m_6$$

$$1 \quad 1 \quad 1$$

$$ABC = m_7$$

### Max term (for two variables)

A	B	$M_i$ (Max term)
0	0	$A + B = M_0$
0	1	$A + B' = M_1$
1	0	$A' + B = M_2$
1	1	$A' + B' = M_3$

### Max term (for 3 Variables)

A	B	C	$M_i$
0	0	0	$A + B + C \rightarrow M_0$
0	0	1	$A + B + C' = M_1$
0	1	0	$A + B' + C \rightarrow M_2$
0	1	1	$A + B' + C' = M_3$
1	0	0	$A' + B + C \rightarrow M_4$
1	0	1	$A' + B + C' = M_5$
1	1	0	$A' + B' + C \rightarrow M_6$
1	1	1	$A' + B' + C' = M_7$

For 2 Variable functions

$m_0, m_1, m_2, m_3 \dots \rightarrow$  min terms

$$\sum_{i=0}^3 m_i = m_0 + m_1 + m_2 + m_3 = SOP$$

$$\sum_{i=0}^7 m_i = SOP \text{ (for 3 Variables)}$$

i=0

$m_0, M_1, M_2, M_3 \rightarrow$  max terms

POS  $\rightarrow M_0 \cdot M_1 \cdot M_2 \cdot M_3$

$$PI(M_0, M_1, M_2, M_3)$$

POS  $\rightarrow PI(M_0, M_1, \dots, M_7) [ \text{for 3 Variables} ]$

## Canonical SOP

$$\textcircled{1} \quad Y = AB + BC + \bar{A}C$$

$$= AB(C + \bar{C}) + BC(A + \bar{A}) + \bar{A}C(B + \bar{B})$$

$$= ABC + A\bar{B}\bar{C} + BCA + B\bar{C}\bar{A} + \bar{A}CB + \bar{A}\bar{C}\bar{B}$$

$$= ABC + AB\bar{C} + A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$$

$$= ABC + AB\bar{C} + \bar{A}BC + \bar{A}\bar{B}C$$

$$= 111 + 110 + 011 + 001$$

$$\text{SOP} = \Sigma m(7, 6, 3, 1) = \Sigma m(1, 3, 6, 7)$$

$$\textcircled{11} \quad Y = ABC + AB + A\bar{B}$$

$$= ABC + AB(C + \bar{C}) + A\bar{B}(C + \bar{C})$$

$$= ABC + ABC + A\bar{B}C + A\bar{B}\bar{C}$$

$$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$$

$$= 111 + 110 + 101 + 100 = m_7 + m_6 + m_5 + m_4$$

$$\text{SOP} = \Sigma m(7, 6, 5, 4) = \Sigma m(4, 5, 6, 7)$$

Canonical POS and Canonical SOP are complement of each other.

Write the  $Y$  in canonical SOP & POS.

$$\begin{array}{cccc} A & B & C & Y \end{array} \quad Y(A, B, C) = \begin{array}{l} \text{in SOP} \\ \text{in POS} \end{array}$$

$$0 \quad 0 \quad 0 \quad 1$$

$$0 \quad 0 \quad 1 \quad 1$$

$$0 \quad 1 \quad 0 \quad 1$$

$$0 \quad 1 \quad 1 \quad 1$$

$$1 \quad 0 \quad 0 \quad 0$$

$$1 \quad 0 \quad 1 \quad 0$$

$$1 \quad 1 \quad 0 \quad 0$$

$$1 \quad 1 \quad 1 \quad 0$$

$$Y(A, B, C) = \Sigma m(0, 1, 2, 3) \rightarrow \text{SOP}$$

$$= \overline{\text{m}}[4, 5, 6, 7] \rightarrow \text{POS}$$

$$Y(A, B, C) = AB + A\bar{B} + ABC$$

$$= AB(C + \bar{C}) + A\bar{B}(C + \bar{C}) + ABC$$

$$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + ABC$$

$$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$$

$$= 111 + 110 + 001 + 000$$

$$= \Sigma m(7, 6, 1, 0) \rightarrow \text{SOP or } \Sigma m(0, 1, 6, 7)$$

$$= \overline{\text{m}}[2, 3, 4, 5] \rightarrow \text{POS}$$

## Lecture 33

Karnaugh Map (K-Map) used to reduce Boolean function.

It is modified model of Truth table.

A	B	Y
0	0	$m_0$
0	1	$m_1$
1	0	$m_2$
1	1	$m_3$

A	B	$\bar{B}$	B
0	0	$m_0$	$m_1$
1	0	$m_2$	$m_3$

A	B	$\bar{B}$	B
0	0	1	0
1	0	0	1

The no. of cell in K-Map =  $2^n$

n is no. of variables

← K-Map representation for 2 Variable in SOP form.

### 3 Variable K-Map for SOP expression

A, B, C → Variables

A	$\bar{B} \bar{C}$	$\bar{B} C$	$B \bar{C}$	$BC$
0	000	001	111	100
1	100	101	111	110

no. of cells =  $2^3 = 8$ .

OR		C	0	1
AB				
00	000	001		
01	010	011		
11	110	111		
10	100	101		

OR		C	0	1
AB				
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	1	0	1

### 4 Variables K-Map

no. of cells =  $2^4 = 16$

CD		00	01	11	10
AB		$m_0$	$m_1$	$m_2$	$m_3$
00	0000	0001	$m_2$	$m_3$	
01	0100	0101	$m_4$	$m_5$	$m_6$
11	1102	1103	$m_8$	$m_9$	$m_{10}$
10	1000	1001	$m_{12}$	$m_{13}$	$m_{14}$

CD		00	01	11	10
AB		0	0	0	0
00	0	0	0	0	0
01	0	0	0	0	0
11	1	1	1	1	1
10	1	1	1	1	1

For 3 Variables

BC		00	01	10	11
A		0	0	0	0
0	0	0	0	0	0
1	0	1	1	1	1

SOP ( $m_i$ )

BC		00	01	11	10
A		0	1	1	1
0	1	1	1	1	1
1	1	0	0	0	0

POS ( $M_i$ )

## 4 Variable K-Map [POS Form]

AB		CD			
00		01	11	10	
00	M <sub>0</sub>	M <sub>1</sub>	M <sub>3</sub>	M <sub>2</sub>	
01	M <sub>5</sub>	M <sub>6</sub>	M <sub>7</sub>	M <sub>8</sub>	
11	M <sub>2</sub>	M <sub>3</sub>	M <sub>5</sub>	M <sub>4</sub>	
10	M <sub>8</sub>	M <sub>10</sub>	M <sub>11</sub>	M <sub>9</sub>	

A		B+C			
0		00	01	11	10
0	M <sub>0</sub>	M <sub>1</sub>	M <sub>3</sub>	M <sub>2</sub>	
1	M <sub>4</sub>	M <sub>5</sub>	M <sub>7</sub>	M <sub>6</sub>	

A		B	0	1
0	M <sub>0</sub>	M <sub>4</sub>		
1	M <sub>2</sub>	M <sub>3</sub>		

3 Variable

4 Variable

Working Rule for Plotting K-Map

$$\text{Let } Y(A, B, C) = AB + A'BC$$

Convert Y into canonical SOP

$$\begin{aligned} Y &= AB(C+C') + A'BC \\ &= ABC + ABC' + A'BC \\ &= \begin{matrix} 111 & 110 & 011 \\ M_7 & M_6 & M_3 \end{matrix} \end{aligned}$$

A		BC		
0		00	01	10
0	0	0	1	0
1	0	0	1	1

Lecture 34

POS f<sup>n</sup>

$$y = (A+B) \cdot \bar{A}$$

Convert Y into canonical POS

$$\begin{aligned} &= A+B \cdot \bar{A} + B \cdot \bar{B} \\ &= (A+B) \cdot (\bar{A}+\bar{B}) \cdot (\bar{A}+\bar{B}) \\ &\quad \begin{matrix} 00 & 10 & 11 & 11 \\ 0 & 0 & 1 & 1 \end{matrix} \end{aligned}$$

A		B	0	1
0	0	0	1	
1	0	1	0	0

A		BC			
0		00	01	11	10
0	0	0	0	0	
1	1	1	1	1	

$$y(A, B, C, D) = (A+B+C+D) \cdot (A+\bar{B}+C) \cdot (A+\bar{B}+\bar{C}+\bar{D})$$

Canonical POS form

$$= (A+B+C+D) \cdot (A+\bar{B}+C+\bar{D}) \cdot (A+\bar{B}+\bar{C}+D)$$

$$= (A+B+C+D) \cdot (A+\bar{B}+C+D) \cdot (A+\bar{B}+C+\bar{D}) \cdot (A+\bar{B}+\bar{C}+\bar{D})$$

0 0 0 0    0 1 0 0    0 1 0 1    0 1 1 1

		C+D			
		A+B	A+D	B+C	B+D
		0+0	0+1	1+1	1+0
		0	1	1	1
		0	0	0	1
		1	1	1	1
		1	1	1	1

A	BC				SOP
	00	01	10	11	
0	1	1	1	1	
1	1	1	1	1	

SOP

$$y = 1 ; y = 0 \text{ if 0 is present in all cells}$$

A	BC			
	00	01	11	10
0	1	1	0	0
1	1	1	0	

$$y = \bar{B}$$

AB	CD			
	00	01	10	11
00	1	0	1	1
01	1	0	0	1
10	0	0	1	1
11	1	1	1	1

$$y = \bar{D} + A\bar{B}$$

$$Y(A, B, C, D) = \sum m(0, 2, 4, 5, 6, 7, 12, 15)$$

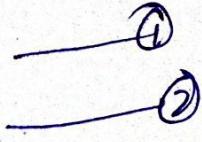
$$Y(A, B, C, D) = \prod M(1, 3, 5, 7, 9, 10, 14)$$

A	BC				POS
	00	01	11	10	
0	0	0	0	1	
1	0	0	1	1	

$$Y = B$$

A+B	CD			
	00	01	1+	10
00	0	0	1	0
01	0	1	1	1
1+	0	1	1	1
10	0	1	1	1

$$Y = (C+D) \cdot (A+B)$$



①

AB	CD	00	01	11	10
00		1	0	0	1
01		1	1	1	1
11		0	0	0	0
10		1	0	1	0

A+B	CD	00	01	11	10
00		1	0	0	1
01		1	0	0	1
11		1	0	0	1
10		1	1	1	0

$$Y(A, B, C) = \sum m(0, 1, 3, 5, 7)$$

$\swarrow BC$

A	BC	00	01	11	10
0		1	1	1	0
1		0	1	1	0

$$y = \bar{A}\bar{B} + C$$

$$Y(A, B, C, D) = \sum m(0, 1, 3, 5, 7, 12, 15)$$

$\swarrow CD$

AB	CD	00	01	11	10
00		1	1	1	0
01		0	1	1	0
11		1	0	1	0
10		0	0	0	0

$$\swarrow AB\bar{C}\bar{D}$$

$\swarrow \bar{A}\bar{B}\bar{C}$        $\therefore Y = \bar{A}\bar{B}\bar{C} + \bar{A}D + AB\bar{C}\bar{D} + BCD$