MUSTAFA GHANIM

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EDUCATION

University of Arizona, Tucson AZ, USA *August 2022 - Present*
PhD in Electrical and Computer Engineering. Current GPA: 4.00/4.00
Özyeğin University, Istanbul, Turkey *September 2019 - December 2021*
MSc in Electrical-Electronics Engineering. GPA: 4.00/4.00
Thesis: *An Efficient Algorithm for Disparity Map Compression Based on Spatial Correlations and Its Low-cost Hardware Architecture.*
Istanbul Technical University, Istanbul, Turkey *August 2015 - August 2019*
Bachelor of Science, Electronics and Communication Engineering. GPA: 3.71/4.00
Senior Design Project: *Design and Implementation of FPGA-based Quadrotor Controller.*
Ranked in Faculty High Honor List.

WORK EXPERIENCE

University of Arizona, Tucson AZ, USA August 2022 - present
Graduate Research and Teaching Assistant

- Research assistant at Reconfigurable Computing Lab:
  - Supported carrier frequency offset estimation and clock dilation apps on heterogeneous systems by utilizing runtime environment APIs.
  - Developed and validated a TensorFlow-based deep neural network for detecting anomalous applications in a heterogeneous runtime environment, enhancing system security and reliability.
  - Supported developing an optimized version of a runtime manager for DSSoCs with a minimal context switching overhead.
- Teaching assistant of Fundamentals of Computer Organization and Electronic Circuits courses.

Özyeğin University, Istanbul, Turkey September 2019 - August 2022
Graduate Research and Teaching Assistant

- Research assistant at nEMESysLab (Embedded Systems/Microelectronic Lab).
  - Disparity (depth) map estimation in MATLAB using local block matching based on Rank, Census, and Complete Rank transforms.
  - Developed a novel, lossless, and low-cost disparity compression algorithm with two variants based on spatial correlations:
    * Designed MATLAB scripts that model the proposed algorithms, including their encoders, memory packetizers, and decoders.
    * Verilog-RTL design and verification of the proposed disparity frame encoders, memory packetizers, and decoders.
    * Verilog-RTL design and verification of an area-efficient 3x3 median filter.
    * Accurate dynamic power analysis based on switching activities.
- Teaching assistant of Mechanical Physics and Digital Systems courses.

AntSis Electronics, Gebze, Turkey June 2019 - August 2019
Research and Development Intern

- Video processing with Microblaze using Vivado Block Design and SDK.
- Integrated an FMC chip on UltraScale MPSoC to generate different color patterns for testing UHD display quality.

Arçelik Cooking Appliances, Bolu, Turkey July 2018 - August 2018
Research and Development Intern

- Conducted electrical safety tests to ensure compliance with international standards for induction hobs.
- Designed, simulated, and optimized power electronic circuits to improve performance and reduce power consumption. Also contributed to the initial development phase of next-generation induction hobs.

ITU Embedded Systems Lab, Istanbul, Turkey June 2017 - July 2017
Research and Development Intern

- Developed face recognition system on Intel Galileo. Additionally, tested communication protocols between different embedded systems.

TECHNICAL SKILLS

Programming Languages	C, C#, C++, CUDA, Pthreads, OpenMP, Python, Verilog, Assembly,
Software & Tools	Latex, Excel Solver, MATLAB, Simulink, HDL Coder, ISE/Vivado, Linux, HFSS, LTspice, Synopsys & Cadence ASIC, Wireshark

PROJECTS

Digital Design and Embedded Systems:

- Accelerated the adaptive median filter using multithreading.
- Designed and verified a real-time 128-bit two-input multiplication system through UART on Spartan-3E.
- Controlled mouse, keyboard, 7-segment display, and VGA on Spartan-3E.
- Designed an embedded system for fruit detection based on conductivity.
- Developed a parallel-serial-parallel communication system with Picoblaze on FPGA.
- Converted a Simulink flight controller model into Verilog-RTL and efficiently implemented it on a low-cost FPGA. To optimize resource usage, resource-sharing techniques, and approximated complex functions were employed within the model.
- Designed a microcontroller-based ultra-sonic radar.

Analog Circuits and RF Engineering:

- Designed and simulated an Op-Amp with high gain and high bandwidth.
- Designed and simulated an optimized ultra-wideband microstrip antenna.

Machine Learning and Signal Processing:

- Colorized grayscale images using Conventional Neural Networks.
- Performed music transcription with Non-negative Matrix Factorization.
- Classified gender and emotional state from images with machine learning.
- Detected voice activity by training a statistical model on filter bank features.
- Classified multiple objects with very high accuracy (>95%) using SIFT and BoW methods.
- Optimized economic dispatch and environmentally friendly unit commitment for multiple electric generators.
- Detected momentum for S&P 500 stock market.

Computer Networks:

- Designed and simulated the Distributed Coordination Function (DCF) for IEEE 802.11.
- Conducted statistical analysis of the Internet topology at the Autonomous System (AS) level.

LANGUAGES

- Arabic: Native.
- English: Working proficiency, IELTS Academic average score: 7.00.
- Turkish: Fluent.

ACADEMIC ACHIEVEMENTS

Awards: Anemone Culture Association recognition award (1st rank in bachelor studies, 2017).
Publications: Akçay, L., Göncü, E., Esen, M. M., Uslu, S., Ghanim, M., Yolcu, N. B., Öztürk, H. S., Sagman, M. B., Hüner, Y., Karakaslı, G., Gayretli, M. G., & Yalçın, B. Ö. (2019, October). Design and implementation of RISC processor with different CMOS technologies. Poster presented at ITU Processor Design Workshop, Istanbul. doi: http://dx.doi.org/10.13140/RG.2.2.34502.83524.
Under Review: Ghanim, M., Tasdizen, O., Ugurdag, H. F. (2022). *An efficient algorithm for disparity map compression based on spatial correlations and its low-cost hardware architecture.* Manuscript submitted for publication.
Service: Manuscript peer-reviewer at *Digital Signal Processing: A Review Journal.*