

MiCAP-Pro User Guide

1 Introduction :

MiCAP-Pro is a high speed custom reconfiguration controller used for DCS designed for the Zynq-SoC platform. The repository contains the following directories:

- hw: In this directory, it contains all the necessary hardware code of the MiCAP-Pro.
- sw: In this directory, it contains all the necessary software drivers of the MiCAP-Pro.

2 Hardware integration:

The MiCAP-Pro can be used as a *pcore* along with the AXI-DMA engine. It can be imported in any XPS project of the DCS. The hardware source code is located at:

`“/hw/axi_stream_generator_v1_00_a/”`.

The user can copy this folder into the user’s pcores directory of the XPS project. Next, press the re-scan button in IP catalog of the XPS. The “*axi_stream_generator_v1_00_a*” should be visible under USER tab of the IP catalog. The user can now use as an user IP and instantiate the MiCAP-Pro core for the DCS.

The connections between the AXI-DMA engine and the stream generator is shown in Figure 1.

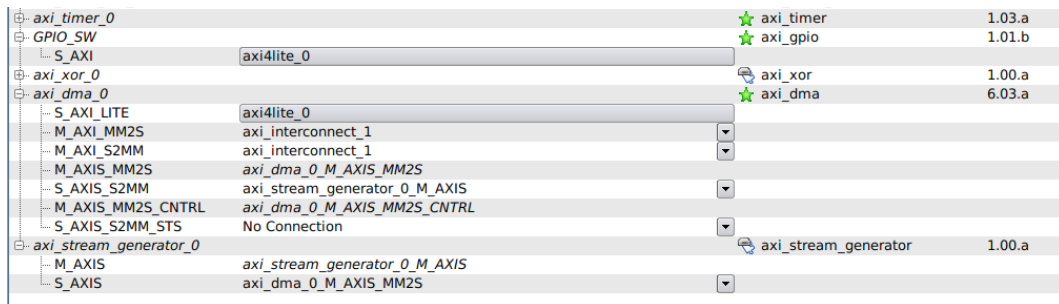


Figure 1: Connections between Stream generator and AXI-DMA engine

The user should also instantiate a GPIO core and make the connections as shown in Figure 2

3 Software integration:

Once the bitstream is generated (as guided in the TLUT tool flow), copy all the files present in the directory “/sw” to the swReconfiguration directory of the XPS project. The user can make use of the function “micap_reconfigure ();” to execute the micro-reconfiguration. An example test code is shown in “testReconfiguration.c”.

[-] External Ports				
[-] axi4lite_0				
[-] axi_interconnect_1				
[-] processing_system7_0				
[-] axi_bram_ctrl_0_bram_block				
[-] axi_bram_ctrl_0				
[-] axi_dma_0				
[-] GPIO_SW				
[-] (BUS_IF) S_AXI	Connected to BUS axi4lite_0			
[-] S_AXI_ACLK	processing_system7_0::FCLK_CLK0		I	CLK
[-] (IO_IF) gpio_0	Not connected to External Ports			
[-] GPIO_IO_O	axi_stream_generator_0::GPIO_I		O	[31:0]
[-] GPIO2_IO_I	axi_stream_generator_0::GPIO_O		I	[31:0]
[-] GPIO_IO_I			I	[31:0]
[-] GPIO_IO_T			O	[31:0]
[-] GPIO2_IO_O			O	[31:0]
[-] GPIO2_IO_T			O	[31:0]
[-] GPIO_IO			I0	[31:0]
[-] GPIO2_IO			I0	[31:0]
[-] axi_stream_generator_0				
[-] GPIO_I	GPIO_SW::[gpio_0]::GPIO_IO_O		I	[31:0]
[-] GPIO_O	GPIO_SW::[gpio_0]::GPIO2_IO_I		O	[31:0]
[-] (BUS_IF) M_AXIS	Connected to BUS axi_stream_generator_0_M_AXIS			
[-] (BUS_IF) S_AXIS	Connected to BUS axi_dma_0_M_AXIS_MM2S			
[-] axi_timer_0				
[-] axi_xor_0				

Figure 2: Connections between Stream generator and GPIO