Designing with RN-21/22, RN-41 Bluetooth Modules

Files included in this ZIP:

- ***Ref-design-schematic.pdf –*** reference design schematic for modules**.**
- ***RN41-pads.jpg -*** PAD locations for RN-41**.**
- ***RN41-pads.dxf -*** DXF CAD file with PCB shape of RN-41**.**
- ***RN21-pads.dxf -*** DXF CAD file with PCB shape of RN-21/22**.**
- ***Ant_Design.pdf*** - PCB layout information for designing external ANT.
- **YAGEO CHIP ANT.pdf-** recommended CHIP ANT option for RN-21/22**.**
- **SMA.pdf-** recommended SMA connector option for RN-21/22**.**
- ***Module-flash.pdf –*** how to use the SPI bus header to upgrade the modules.

DESIGN ISSUES:

1. RESET circuit. A power on reset circuit with delay is OPTIONAL on the reset pin of the module. Often a microcontroller or embedded CPU IO is available to generate reset. If not, there are many low cost power supervisor chips available to. An example is in the reference design, the MCP810T, or MCP101 are good choices. The RN21 and 22 modules contain a 1k pull down to ground. The RN41 contains a 1k pullup to VCC. The polarity of reset on RN21/22 is ACTIVE HIGH. The polarity of reset on the RN41 is ACTIVE LOW. Just leaving the pin unconnected should be adequate in most cases to provide a clean reset, however, depending on the user power supply ramp and stability it is recommended to apply a clean reset to the modules.

2. Factory reset PIO4. It is a good idea to connect this pin to a switch, or jumper, or resistor, so it can be accessed. This pin can be used to reset the module to FACTORY DEFAULTS and is often critical in situations where the module has been mis-configured.

3. CONNECTION status. PIO5 is available to drive an LED, and blinks at various speeds to indicate status. PIO2 is an output which directly reflects the connection state, it goes HIGH when connected, and LOW otherwise.

4. Using SPI bus for flash upgrade. While not required, this bus is very useful for configuring advanced parameters of the Bluetooth modules, and is required for upgrading the firmware on modules. The suggested ref-design shows a 6pin header which can be implemented to gain access to this bus. A minimum-mode version could just use the SPI signals (4pins) and pickup ground and VCC from elsewhere on the design.

PCB LAYOUT ISSUES:

1. LAYOUT: RN-41 with onboard ANT. See the RN41-pads.jpg, and RN-41.pdf datasheet. Care must be taken to provide for a proper ground plane to the pins of the module, especially near the ANT (pins 25,27), and that NO signal or GROUND traces enter the ANT area. If possible, design the PCB so that the ANT portion of the module protrudes past the PCB board edge.

2. LAYOUT: RN21/22 with CHIP ANT. See the enclosed datasheet on the recommend Chip-ANT.pdf for layout guidelines.

3. LAYOUT: RN21 or 22 with external SMA connector. See Ant_Design.pdf