

ESP32-S3-R8

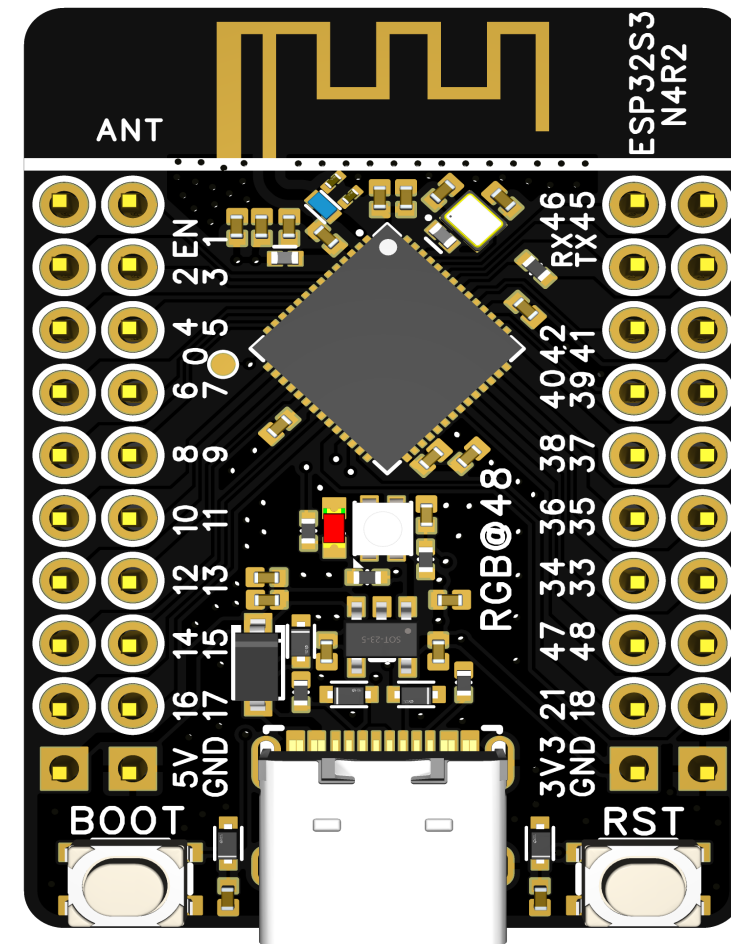


Table 2-14. Pin Mapping Between Chip and In-package Flash/ PSRAM

Pin No.	Pin Name	Single SPI		Dual SPI		Quad SPI / QPI		Octal SPI / OPI	
		Flash	PSRAM	Flash	PSRAM	Flash	PSRAM	Flash	PSRAM
33	SPICLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK	CLK
32	SPICSS0 <sup>1</sup>	CS#		CS#		CS#		CS#	
28	SPICSS1 <sup>2</sup>		CE#		CE#		CE#		CE#
35	SPID	DI	SI/SIO0	DI	SI/SIO0	DI	SI/SIO0	DQ0	DQ0
34	SPIQ	DO	SO/SIO1	DO	SO/SIO1	DO	SO/SIO1	DQ1	DQ1
31	SPWP	WP#	SIO2	WP#	SIO2	WP#	SIO2	DQ2	DQ2
30	SPIHD	HOLD#	SIO3	HOLD#	SIO3	HOLD#	SIO3	DQ3	DQ3
38	GPIO33							DQ4	DQ4
39	GPIO34							DQ5	DQ5
40	GPIO35							DQ6	DQ6
41	GPIO36							DQ7	DQ7
42	GPIO37							DQS/DM	DQS/DM

<sup>1</sup> CS0 is for in-package flash

<sup>2</sup> CS1 is for in-package PSRAM

When you use GPIO33, GPIO34, GPIO35, GPIO36, GPIO37, please pay attention to the FLASH mode and PSRAM mode

Table 2-9. Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Pull-up	1
GPIO3	Floating	-
GPIO45	Pull-down	0
GPIO46	Pull-down	0

Please do not change the initial state of strapping pins before the board is powered on.

Strapping Pins: GPIO0 GPIO3 GPIO45 GPIO46

中文  
S3-勘误表 : [https://www.espressif.com.cn/sites/default/files/documentation/esp32-s3\\_errata\\_cn.pdf](https://www.espressif.com.cn/sites/default/files/documentation/esp32-s3_errata_cn.pdf)

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S3-Hardware Design Guidelines : [https://www.espressif.com.cn/sites/default/files/documentation/esp32-s3\\_hardware\\_design\\_guidelines\\_en.pdf](https://www.espressif.com.cn/sites/default/files/documentation/esp32-s3_hardware_design_guidelines_en.pdf)

esp-idf : <https://github.com/espressif/esp-idf>

If you have any questions, you can contact WeAct Studio

QQ群 : 146605098

GitHub : <https://github.com/WeActStudio/WeActStudio.ESP32S3-MINI>

Gitee :