

Chapter 10
Instruction and Register Encodings

CHAPTER 10. INSTRUCTION AND REGISTER ENCODINGS

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10. INSTRUCTION AND REGISTER ENCODINGS

10.1 Instruction Set Encodings

Tables 10-1 to 10-3 illustrate the bit-level encoding of the DSP3210 instruction set.

Table 10-1 Instruction Encodings

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0a & 1a. Reserved	0	0	0	0	0																											
0b & 1b. Cond Branch	1	0	0	0	0			C				rB												N								
2a. Reserved	0	0	0	0	1	0																										
2b. Reserved	1	0	0	0	1	0																										
3a. Loop Counter	0	0	0	0	1	1		rM			rB												N									
3b. Do Instr. (Immed)	1	0	0	0	1	1	0	B	M							K						L										
3c. Do Instr. (Reg)	1	0	0	0	1	1	1	B	M						K								rM									
4a. Call Reg with 16-bit N	0	0	0	1	0	0		rM			rB											N										
4b. Shift and Or	1	0	0	1	0	0		rD			rS											N										
5a. 16-bit 3 Opnd Add	0	0	0	1	0	1		rD			rS3											N										
5b. 32-bit 3 Opnd Add	1	0	0	1	0	1		rD			rS3											N										
6a. 16-bit ALU Reg Src	0	0	0	1	1	0	0	F			rD			rS1		C						rS2										
6b. 32-bit ALU Reg Src	1	0	0	1	1	0	0	F			rD			rS1		C						rS2										
6c. 16-bit ALU Immed	0	0	0	1	1	0	1	F			rD											N										

Table 10-1 Instruction Encodings (cont.)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6d. 32-bit ALU Immed	1	0	0	1	1	0	1		F		rD													N								
7a. MOVE - DA	0	0	0	1	1	1	0	T	W		rH												L									
7b. MOVE - I/O	1	0	0	1	1	1	0	T	W		rH									1									iorH			
7c. MOVE - Pnt Inc	1	0	0	1	1	1	0	T	W		rH			rP	0									rl								
7d. MOVE - Mem - I/O	1	0	0	1	1	1	1	T	W		iorH			rP	0								rl									
8a. Uncond Branch	1	0	1					Ne		rB										N												
8b. 24-Bit Immed Load	1	1	0					Ne		rD										N												
8c. Call 24-Bit Immed	1	1	1					Ne		rM										N												
1. DAU - M/A	0	0	1		M		F	S	N		X			Y						Z												
2. DAU - M/A	0	1	0		M		F	S	N		X			Y						Z												
3. DAU - M/A	0	1	1		M		F	S	N		X			Y						Z												
4. DAU - M/A	0	0	1	1	1	0	F	S	N		X			Y						Z												
5. DAU - Spec. Func.	0	1	1	1	1	1	G		N	0	0	0	0	0	0	0	0	0	Y										Z			

Table 10-2 CA Instruction Field Encodings

CA - W Field						CA - F Field					
W	Bytes				Operation	F	ALU/BS Function				
	3	2	1	0							
000	0	0	0	D	unsigned char	0000	+ addition				
001	S	S	S	D	signed char	0001	<<n shift left by n				
010	0	0	D	D	unsigned short	0010	- subtract {N} - rD				
011	S	S	D	D	signed short	0011	# carry reverse add				
100	0	0	D	0	unsigned high char	0100	- subtract rD - {N, rS}				
101	-	-	-	-	reserved	0101	reserved				
110	-	-	-	-	reserved	0110	&~ and with complement				
111	D	D	D	D	long	0111	- compare (no store)				
CA - rB, rM, rH, rD, rS, rS1, rS2, rS3, rP, rI											
CODE		CAU Register	CODE		CAU Register	CA - T Field					
00000	0 (r0)	10000	Reserved					T	Operation		
00001	r1	10001	r15					0	Data is moved to a register		
00010	r2	10010	r16					1	Data is moved from a register		
00011	r3	10011	r17								
00100	r4	10100	r18								
00101	r5	10101	r19								
00110	r6	10110	-n								
00111	r7	10111	+n								
01000	r8	11000	r20								
01001	r9	11001	r21								
01010	r10	11010	r22								
01011	r11	11011	Reserved								
01100	r12	11100	Reserved								
01101	r13	11101	Reserved								
01110	r14	11110	pcsh								
01111	pc	11111	Reserved								
CA - R Field											
R	I/O Register	R	I/O Register								
00000	ps	01010	spc								
00001	Reserved	01011	Reserved								
0001x	Reserved	01100	pcw								
001xx	Reserved	01101	Reserved								
01000	emr	01110	dauc								
01001	Reserved	01111	ctr								
		1xxxx	Reserved								

Table 10-2 CA Instruction Field Encodings (cont.)

C Field - CAU & DAU Condition Codes			
Condition	Code	Flags	Meaning
false	0 0 0 0 0	none	always false
true	0 0 0 0 1	none	always true
pl	0 0 0 0 1 0	n=0	result is nonnegative (plus)
mi	0 0 0 0 1 1	n=1	result is negative (minus)
ne	0 0 0 1 0 0	z=0	result not equal to zero
eq	0 0 0 1 0 1	z=1	result equal to zero
vc	0 0 0 1 1 0	v=0	overflow clear, no overflow
vs	0 0 0 1 1 1	v=1	overflow set, overflow
cc	0 0 1 0 0 0	c=0	carry clear, no carry
cs	0 0 1 0 0 1	c=1	carry set, carry
ge	0 0 1 0 1 0	n^v=0	greater than or equal to zero
lt	0 0 1 0 1 1	n^v=1	less than zero
gt	0 0 1 1 0 0	z (n^v)=0	greater than zero
le	0 0 1 1 0 1	z (n^v)=1	less than or equal to zero
hi	0 0 1 1 1 0	c z=0	greater than (unsigned)
ls	0 0 1 1 1 1	c z=1	less than (unsigned)
auc	0 1 0 0 0 0	U=0	underflow clear, no underflow
aus	0 1 0 0 0 1	U=1	underflow set, underflow
age	0 1 0 0 1 0	N=0	greater than or equal to zero
alt	0 1 0 0 1 1	N=1	less than zero
ane	0 1 0 1 0 0	Z=0	not equal to zero
aeq	0 1 0 1 0 1	Z=1	equal to zero
avc	0 1 0 1 1 0	V=0	overflow clear, no overflow
avs	0 1 0 1 1 1	V=1	overflow set, overflow
agt	0 1 1 0 0 0	N Z=0	greater than zero
ale	0 1 1 0 0 1	N Z=1	less than or equal to zero
	0 1 1 0 1 x		Reserved
	0 1 1 1 x x		Reserved

C Field - I/O Condition Codes			
Condition	Code	Flags	Meaning
ibe	1 0 0 0 0 0	ibf=0	input buffer empty
ibf	1 0 0 0 0 1	ibf=1	input buffer full
obf	1 0 0 0 1 0	obe=0	output buffer FULL
obe	1 0 0 0 1 1	obe=1	output buffer empty
	1 0 0 1 0 0		Reserved
	1 0 0 1 0 1		Reserved
	1 0 0 1 1 0		Reserved
	1 0 0 1 1 1		Reserved
syc	1 0 1 0 0 0	sy=0	SY (I/O sync) cleared
sys	1 0 1 0 0 1	sy=1	SY (I/O sync) set
fbc	1 0 1 0 1 0	fb=0	Serial I/O frame boundary clear
fbs	1 0 1 0 1 1	fb=1	Serial I/O frame boundary set
ir0c	1 0 1 1 0 0	ir0n=0	Interrupt Request 0 clear (logic 0)
ir0s	1 0 1 1 0 1	ir0n=1	Interrupt Request 0 set (logic 1)
ir1c	1 0 1 1 1 0	ir1n=0	Interrupt Request 1 clear (logic 0)
ir1s	1 0 1 1 1 1	ir1n=1	Interrupt Request 1 set (logic 1)
	1 1 x x x x		Reserved

Table 10-3 DA Instruction Field Encodings

DA - G Field	
G	Operation
0000	ic
0001	oc
0010	float16
0011	int16
0100	round
0101	ifalt
0110	ifaeq
0111	ifagt
1000	float32
1001	int32
1010	Reserved
1011	Reserved
1100	ieee (DSP to IEEE)
1101	dsp (IEEE to DSP)
1110	seed
1111	Reserved

DA - X, Y, Z Fields	
p	Operation
0000	Selects register-direct
0001	r1
0010	r2
0011	r3
0100	r4
0101	r5
0110	r6
0111	r7
1000	r8
1001	r9
1010	r10
1011	r11
1100	r12
1101	r13
1110	r14
1111	Not allowed

DA - X, Y, Z Fields	
I	Operation (p≠0000)
000	0
001	r15
010	r16
011	r17
100	r18
101	r19
110	-4(f), -2(i), -1(b)
111	+4(f), +2(i), +1(b)

DA - X, Y, Z Field	
M	Operation (p=0000)
000	a0 – X, Y fields only
001	a1 – X, Y fields only
010	a2 – X, Y fields only
011	a3 – X, Y fields only
100	Reserved
101	Reserved
110	Reserved
111	No write - Z field only

DA - M Field	
M	Operation
000	a0
001	a1
010	a2
011	a3
100	0.0
101	1.0
110	Not Allowed
111	Not Allowed

DA - N Field	
N	Operation
00	a0
01	a1
10	a2
11	a3

DA - S and F Fields	
S/F	Operation
0	+
1	-

10.2 Register Encodings

Tables 10-4 to 10-8 illustrate the bit-level encoding for the IO registers of the DSP3210. Tables 10-9 to 10-12 illustrate the bit-level encoding for the MMIO registers of the DSP3210.

Table 10-4 ps Register Encoding

Bit	15	14	13	12	11	10-	9	8	7	6	5	4	3	2	1	0
Field	0	0	ir1	ir0	fb	sy	obe	ibf	v	U	Z	N	c	v	z	n

Bit(s)	Field	Function
0	n	CAU n flag; means that the ALU result is negative.
1	z	CAU z flag; means that the ALU result is zero.
2	v	CAU v flag; means that the ALU result overflowed.
3	c	CAU c flag; means that the ALU result had a carry out of the MSB.
4	N	DAU N flag; means that the DAU result is negative.
5	Z	DAU Z flag; means that the DAU result is zero.
6	U	DAU U flag; means that the DAU result underflowed.
7	V	DAU V flag; means that the DAU result overflowed.
8	ibf	Serial input buffer full flag; means that the serial input buffer is full.
9	obe	Serial output buffer empty flag; means that the serial output buffer is empty.
10	sy	Serial sync set flag; means that the SY pin is high (logic one).
11	fb	Serial frame boundary flag; means that the SIO is at a frame boundary.
12	ir0	Pin IR0N is high (logic one).
13	ir1	Pin IR1N is high (logic one).
15—14	-	Reserved - read as zero.

Table 10-5 dauc Register Encoding

Bit	7	6	5	4	3	2	1	0
Field	0	COND	ROUND				CONV	

Bit(s)	Field	Encoding	Function
3—0	CONV	x0x0	μ -law input conversion.
		x0x1	A-law input conversion.
		x1xx	Unsigned linear byte input conversion.
		0x0x	μ -law output conversion.
		0x1x	A-law output conversion.
		1xxx	Unsigned linear byte output conversion.
5—4	ROUND	x0	Round-to-nearest on float-to-integer conversions.
		01	Truncate towards $-\infty$ on float-to-integer conversion.
		11	Truncate towards 0 on float-to-integer conversion.
6	COND	0	DA instructions <i>ifalt</i> , <i>ifaeq</i> , and <i>ifagt</i> have unconditional Z-writes.
		1	DA instructions <i>ifalt</i> , <i>ifaeq</i> , and <i>ifagt</i> have conditional Z-writes.
7	0	0	Must be set to zero; Read as zero.

Table 10-6 ctr Register Encoding

Bit	7	6	5	4	3	2	1	0
Field	0	0	N-5	N-4	N-3	N-2	N-1	N0

Bit(s)	Field	Meaning
0	N0	Current DAU N Flag
1	N-1	DAU N Flag computed for Instruction -1 (previous DA instruction that set flags)
2	N-2	DAU N Flag computed for Instruction -2
3	N-3	DAU N Flag computed for Instruction -3
4	N-4	DAU N Flag computed for Instruction -4
5	N-5	DAU N Flag computed for Instruction -5
7-6	-	Reserved - read as zero

Table 10-7 emr Register Encoding

Bit	15	14	132	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	EXT1	OFRM	IFRM	OBE	IBF	Res	TIMER	EXT0	Res	NAN	U/V	AERR	Reserved	SL		

Each bit in this register corresponds to one of the maskable sources for an exception. A value of 1 in a position enables the corresponding interrupt source; a value of 0 disables the source. On reset all bits are set to 0 (zero).

Bit(s)	Field	Function	Priority
0	SL	If 1, select processor level to be visible on IACK[1—0]. Encoding: 00 - Base level 01 - Interrupt level 10 - Error level 11 - Double error level	-
1-3		Reserved	-
4	AERR	Addressing Error	Highest
5	U/V	DAU Underflow/Overflow	
6	NAN	IEEE NAN	
7		Reserved	
8	EXT0	Interrupt pin 0 (IR0N) request	
9	TIMER	TIMER counted to zero	
10		Reserved	
11	IBF	SIO input buffer full	
12	OBE	SIO output buffer empty	
13	IFRM	SIO input DMA frame complete	
14	OFRM	SIO output DMA frame complete	
15	EXT1	Interrupt pin 1 (IR1N) request	Lowest

Table 10-8 pcw Register Encoding

Bit	15	14	132	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	P/BN	BRC	D/SN	R/WN	C/PN	M/IN	B/LN	SBD		PBD		WB		WA		

Table 10-8 pcw Register Encoding (cont.)

Bit(s)	Field	Function																													
1,0	WA	These bits configure the number of wait-states that are generated for transactions in partition A. Set to {1,1} on reset.																													
		<table border="1"> <tr><td>pcw 1.0</td><td>00</td><td>0-or-more wait-states</td></tr> <tr><td></td><td>01</td><td>1-or-more wait-states</td></tr> <tr><td></td><td>10</td><td>2-or-more wait-states</td></tr> <tr><td></td><td>11</td><td>3-or-more wait-states</td></tr> </table>			pcw 1.0	00	0-or-more wait-states		01	1-or-more wait-states		10	2-or-more wait-states		11	3-or-more wait-states															
pcw 1.0	00	0-or-more wait-states																													
	01	1-or-more wait-states																													
	10	2-or-more wait-states																													
	11	3-or-more wait-states																													
3,2	WB	These bits configure the number of wait-states that are generated for transactions in partition B. Set to {1,1} on reset.																													
		<table border="1"> <tr><td>pcw 3.2</td><td>00</td><td>0-or-more wait-states</td></tr> <tr><td></td><td>01</td><td>1-or-more wait-states</td></tr> <tr><td></td><td>10</td><td>2-or-more wait-states</td></tr> <tr><td></td><td>11</td><td>3-or-more wait-states</td></tr> </table>			pcw 3.2	00	0-or-more wait-states		01	1-or-more wait-states		10	2-or-more wait-states		11	3-or-more wait-states															
pcw 3.2	00	0-or-more wait-states																													
	01	1-or-more wait-states																													
	10	2-or-more wait-states																													
	11	3-or-more wait-states																													
6—4	PBD	These bits configure the page size for asserting the page break detect (PBD) signal. A2—A9 are always masked, A17—A31 are always unmasked, A10—A16 masking is controlled by the PBD field when comparing the last address to external memory. Set to {0,0,0} on reset.																													
		<table border="1"> <tr><th>pcw 6.5.4</th><th>Page Size</th><th>DRAM size</th></tr> <tr><td>000</td><td>256 words</td><td>64k x n</td></tr> <tr><td>001</td><td>512 words</td><td>256k x n</td></tr> <tr><td>010</td><td>1k words</td><td>1M x n</td></tr> <tr><td>011</td><td>2k words</td><td>4M x n</td></tr> <tr><td>100</td><td>4k words</td><td>16M x n</td></tr> <tr><td>101</td><td>8k words</td><td>64M x n</td></tr> <tr><td>110</td><td>16k words</td><td>256M x n</td></tr> <tr><td>111</td><td>32k words</td><td>1G x n</td></tr> </table>			pcw 6.5.4	Page Size	DRAM size	000	256 words	64k x n	001	512 words	256k x n	010	1k words	1M x n	011	2k words	4M x n	100	4k words	16M x n	101	8k words	64M x n	110	16k words	256M x n	111	32k words	1G x n
pcw 6.5.4	Page Size	DRAM size																													
000	256 words	64k x n																													
001	512 words	256k x n																													
010	1k words	1M x n																													
011	2k words	4M x n																													
100	4k words	16M x n																													
101	8k words	64M x n																													
110	16k words	256M x n																													
111	32k words	1G x n																													
7	SBD	This bit enables(1)/disables(0) sequential address break detection and can be used with a page size of 256 only. Set to one on reset.																													
8	B/LN	Configures the byte ordering. If 0, little endian byte ordering is selected. If 1, big endian byte ordering is selected. Set to one on reset.																													
9	M/IN	Configures the MS0—MS3 pins. If 0, Intel style signaling is selected. If 1, Motorola style signaling is selected. Set to one on reset.																													
10	C/PN	Selects between one of two memory maps. If 1, μ Computer mode is selected and on-chip memory is at location zero. If 0, μ Processor mode is selected and external memory is at location zero. Reset value based on the state of bio[7] during reset.																													
11	R/WN	Configures the RW pin. If 0, RW pin is active high for write transactions. If 1, RW pin is active high for read transactions. Reset value based on the state of bio[6] during reset.																													
12	D/SN	Configures the operation of pins AEN/MRN and DEN/MWN. If 0, SRAM interface signaling selected (MRN and MWN). If 1, DRAM system bus interface signaling selected (AEN and DEN). Reset value based on the state of bio[5] during reset.																													
13	BRC	Reset value based on the state of bio[4] during reset. Controls Boot ROM routine. Also, when written with a one, modification of the pcw is disabled.																													
15—14	P/BN	Configures the PBD/BLMN signal. Set to {0,0} on reset.																													
		<table border="1"> <tr><td>pcw 15.14</td><td>00</td><td>BLMN is selected</td></tr> <tr><td></td><td>01</td><td>PBD is selected; addresses to partition A are monitored.</td></tr> <tr><td></td><td>10</td><td>PBD is selected; addresses to partition B are monitored.</td></tr> <tr><td></td><td>11</td><td>PBD is selected; addresses to partitions A and B are monitored.</td></tr> </table>			pcw 15.14	00	BLMN is selected		01	PBD is selected; addresses to partition A are monitored.		10	PBD is selected; addresses to partition B are monitored.		11	PBD is selected; addresses to partitions A and B are monitored.															
pcw 15.14	00	BLMN is selected																													
	01	PBD is selected; addresses to partition A are monitored.																													
	10	PBD is selected; addresses to partition B are monitored.																													
	11	PBD is selected; addresses to partitions A and B are monitored.																													

Table 10-9 ioc Register Encoding

Bit	31–24	23–20	19	18	17	16	15	14	13	12–10	9	8	7 6	5	4	3	2	1	0
Field	Res	ICN	OSZ	ISZ	OUT	IN	SAN	IIC	BO	OLEN	AOL	AOC	ILEN	AIL	AIC	SLEN	BC	ASY	

Bit(s)	Field	Function																																																
0	ASY	If 0, SY is external. If 1, SY is internal. When generated internally, SY = {ICK, OCK}/{256, 512, 1024}, based on ioc[1] and ioc[3,2].																																																
1	BC	If 0, ICK is used to derive the internal load and SY signals. If 1, OCK is used to derive the internal load and SY signals.																																																
3,2	SLEN	These bits select the frequency ratio of the on-chip load signal to the on-chip SY signal.																																																
		<table border="1"> <thead> <tr> <th>ioc[3]</th> <th>ioc[2]</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>ratio = 32</td> </tr> <tr> <td>0</td> <td>1</td> <td>ratio = 8</td> </tr> <tr> <td>1</td> <td>0</td> <td>ratio = 16</td> </tr> <tr> <td>1</td> <td>1</td> <td>ratio = 32</td> </tr> </tbody> </table>																	ioc[3]	ioc[2]		0	0	ratio = 32	0	1	ratio = 8	1	0	ratio = 16	1	1	ratio = 32																	
ioc[3]	ioc[2]																																																	
0	0	ratio = 32																																																
0	1	ratio = 8																																																
1	0	ratio = 16																																																
1	1	ratio = 32																																																
4	AIC	If 0, ICK is external. If 1, ICK is generated internally with a frequency specified by ioc[23–20].																																																
5	AIL	If 0, ILD is external. If 1, ILD is generated internally with a frequency of {ICK,OCK}/32, based on ioc[1].																																																
7,6	ILEN	These bits specify the length of the serial input data.																																																
		<table border="1"> <thead> <tr> <th>ioc[7]</th> <th>ioc[6]</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>input length is 32 bits (prior to ILD)</td> </tr> <tr> <td>0</td> <td>1</td> <td>input length is 8 bits (after ILD)</td> </tr> <tr> <td>1</td> <td>0</td> <td>input length is 16 bits (after ILD)</td> </tr> <tr> <td>1</td> <td>1</td> <td>input length is 32 bits (after ILD)</td> </tr> </tbody> </table>																	ioc[7]	ioc[6]		0	0	input length is 32 bits (prior to ILD)	0	1	input length is 8 bits (after ILD)	1	0	input length is 16 bits (after ILD)	1	1	input length is 32 bits (after ILD)																	
ioc[7]	ioc[6]																																																	
0	0	input length is 32 bits (prior to ILD)																																																
0	1	input length is 8 bits (after ILD)																																																
1	0	input length is 16 bits (after ILD)																																																
1	1	input length is 32 bits (after ILD)																																																
8	AOC	If 0, OCK is external. If 1, OCK is internally generated with a frequency specified by ioc[23–20].																																																
9	AOL	If 0, OLD is external. If 1, OLD is internally generated: (1) with a frequency of {ICK,OCK}/32, based on ioc[1] if ioc[13]=0, or (2) in a burst-mode if ioc[13]=1.																																																
12–10	OLEN	These bits specify the length of serial output data.																																																
		<table border="1"> <thead> <tr> <th>ioc[12]</th> <th>ioc[11]</th> <th>ioc[10]</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>reserved</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>output length is 8 bits</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>output length is 16 bits</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>output length is 32 bits</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>output length is 24 bits</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>reserved</td> </tr> <tr> <td>1</td> <td>1</td> <td>x</td> <td>reserved</td> </tr> </tbody> </table>																	ioc[12]	ioc[11]	ioc[10]		0	0	0	reserved	0	0	1	output length is 8 bits	0	1	0	output length is 16 bits	0	1	1	output length is 32 bits	1	0	0	output length is 24 bits	1	0	1	reserved	1	1	x	reserved
ioc[12]	ioc[11]	ioc[10]																																																
0	0	0	reserved																																															
0	0	1	output length is 8 bits																																															
0	1	0	output length is 16 bits																																															
0	1	1	output length is 32 bits																																															
1	0	0	output length is 24 bits																																															
1	0	1	reserved																																															
1	1	x	reserved																																															
13	BO	If 0, the internal OLD is {ICK,OCK}/32, based on ioc[1]. If 1, the internal OLD is burst-mode, generated as a function of the status of the obuf and OSR.																																																
14	IIC	If 0, the ICK is true (not inverted). If 1, the ICK is inverted.																																																
15	SAN	If 0, clear sanity bit. If 1, set sanity bit.																																																
16	IN	If 0, the LSB is received first during serial inputs. If 1, the MSB is received first during serial inputs.																																																
17	OUT	If 0, the LSB is transmitted first during serial outputs. If 1, the MSB is transmitted first during serial outputs (can't be used with 24-bit output length).																																																
18	ISZ	If 0, the input DMA transfer size is 32-bits. If 1, the input DMA size is specified by ILEN.																																																
19	OSZ	If 0, the output DMA transfer size is 32-bits. If 1, the output DMA size is specified by OLEN.																																																
23–20	ICN	These bits specify the divide-down rate of the internal clock generator. The internal clock generator has an additional fixed divide-down by four, i.e., if bits 23–20 represent N, the divide-down rate is N*4. If ICN = 0, the active clock generator is disabled.																																																
31–24		Reserved; Read as zero.																																																

Table 10-10 dmac Register Encoding

Bit	7	6	5	4	3	2	1	0
Field	IRB	IRS	IDE	ICS	ORB	ORS	ODE	OCS

Bit(s)	Field	Function
0	OCS	If 0, don't change output DMA settings, dmac[1,2], when the dmac register is loaded. If 1, change output DMA settings when the dmac register is loaded to new values specified in bits 1,2.
1	ODE	If 0, disable output DMA. If 1, enable output DMA and request DMA cycle when OBE is asserted, obuf is empty.
2	ORS	If 0, stop output DMA when the number of DMA transfers (OCOUNTER) reaches the number specified in OCNT. If 1, reload the current output DMA pointer and the current output transfer count registers, ODP and OCNT, respectively, when the number of DMA transfers (OCOUNTER) reaches the number specified in OCNT and keep output DMA enabled.
3	ORB	If 0, request output DMA cycles based on OBE and dmac[1]. If 1, request output DMA cycles based on OBE, dmac[1], and if the DSP3210 has ownership of the bus interface. If the DSP3210 is not the current bus master, the BRN is asserted. When the bus is granted, the DMA cycle is requested.
4	ICS	If 0, don't change input DMA settings, dmac[4,5], when the dmac register is loaded. If 1, change input DMA settings when the dmac register is loaded to new values specified in bits 4,5.
5	IDE	If 0, disable input DMA. If 1, enable input DMA and request DMA cycle when IBF is asserted, ibuf is full.
6	IRS	If 0, stop input DMA when the number of DMA transfers (ICOUNTER) reaches the number specified in ICNT. If 1, reload the current input DMA pointer and the current input transfer count registers, IDP and ICNT, respectively, when the number of DMA transfers (ICOUNTER) reaches the number specified in ICNT and keep output DMA enabled.
7	IRB	If 0, request input DMA cycles based on IBF and dmac[4]. If 1, request DMA cycles based on IBF, dmac[4], and if the DSP3210 has ownership of the bus interface. If the DSP3210 is not the current bus master, the BRN is asserted. When the bus is granted, the DMA cycle is requested.

Table 10-11 tcon Register Encoding

Bit	7	6	5	4	3	2	1	0
Field	SRC		OUT	H/LN	T/PN	R/SN	E/HN	

Bit(s)	Field	Function														
0	E/HN	Hold/enable count-down operation of counter 0 - Hold the count 1 - Enable the count-down operation of counter														
1	R/SN	Select between continuous and one-time operation 0 - Stop counting when the count reaches zero 1 - Automatic reload of the counter from the initial count register when the count reaches zero														
2	T/PN	Select pulse or toggle operation of the output when the count reaches zero 0 - For the external output, a pulse is generated when the count reaches zero 1 - For the external output, the output is the output of a toggle flip-flop which is toggled when the count reaches zero														
3	H/LN	When tcon[2] is set to zero, pulse, select low active or high active pulse 0 - When tcon[2] is set to zero, the pulse is one CKI clock period wide and is low active (1->0->1) 1 - When tcon[2] is set to zero, the pulse is one CKI clock period wide and is active high (0->1->0)														
4	OUT	If the BIO1 pin is configured as an output, 0 - the BIO1 pin has the value specified by the BIO1 field in the BIO register 1 - the BIO1 pin is selected to be the timer output														
5—7	SRC	Selects the clock source for the timer <u>tcon 7,6,5</u> <table> <tr> <td>000</td> <td>Counter clock is CKI/2</td> </tr> <tr> <td>001</td> <td>Counter clock is CKI/4</td> </tr> <tr> <td>010</td> <td>Reserved</td> </tr> <tr> <td>011</td> <td>Reserved</td> </tr> <tr> <td>100</td> <td>Counter clock is from external source(pin BIO0) - rising edge</td> </tr> <tr> <td>101</td> <td>Counter clock is from external source (pin BIO0) - falling edge</td> </tr> <tr> <td>11x</td> <td>Reserved</td> </tr> </table>	000	Counter clock is CKI/2	001	Counter clock is CKI/4	010	Reserved	011	Reserved	100	Counter clock is from external source(pin BIO0) - rising edge	101	Counter clock is from external source (pin BIO0) - falling edge	11x	Reserved
000	Counter clock is CKI/2															
001	Counter clock is CKI/4															
010	Reserved															
011	Reserved															
100	Counter clock is from external source(pin BIO0) - rising edge															
101	Counter clock is from external source (pin BIO0) - falling edge															
11x	Reserved															

Table 10-12 bioc Register Encoding

Bit	7	6	5	4	3	2	1	0
Field	B7	B6	B5	B4	B3	B2	B1	B0

Each bit in the bioc register corresponds to one of the pins in the BIO port, B0—BIO0, B1—BIO1, ..., B7—BIO7. A value of 0 in the bit indicates that the associated pin is configured as an input; a value of 1 indicates that the pin is configured as an output. On reset all bits are set to zero (input).

Table 10-13 bio Register Encoding

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	BF7		BF6		BF5		BF4		BF3		BF2		BF1		BF0	

Each pair of bits (field) in the bio register corresponds to one of the bio pins in the BIO port, BF0—BIO0, BF1—BIO1, ..., BF7—BIO7. When the bio register is written, the value of each output register bit is changed according to the following encoding of the bit field:

BF bit pair: bit 1.0

- 00 Keep the previous value in the bio output register bit
- 01 Set the bio output register bit to zero
- 10 Set the bio output register bit to one
- 11 Complement the value in the bio output register bit

The transfer function is described below, where Qt is the previous value and Qt+1 is the new value:

Qt	Bit1	Bit0	Qt+1	
0	0	0	0	previous
0	0	1	0	false
0	1	0	1	true
0	1	1	1	toggle
1	0	0	1	previous
1	0	1	0	false
1	1	0	1	true
1	1	1	0	toggle

When the bio register is read, the value of both the corresponding bio pin and the bio output register bit are read according to the following encoding of the bit field:

- bit 0 Bio pin value
- bit 1 Bio output register value

Chapter 11

Physical Specifications

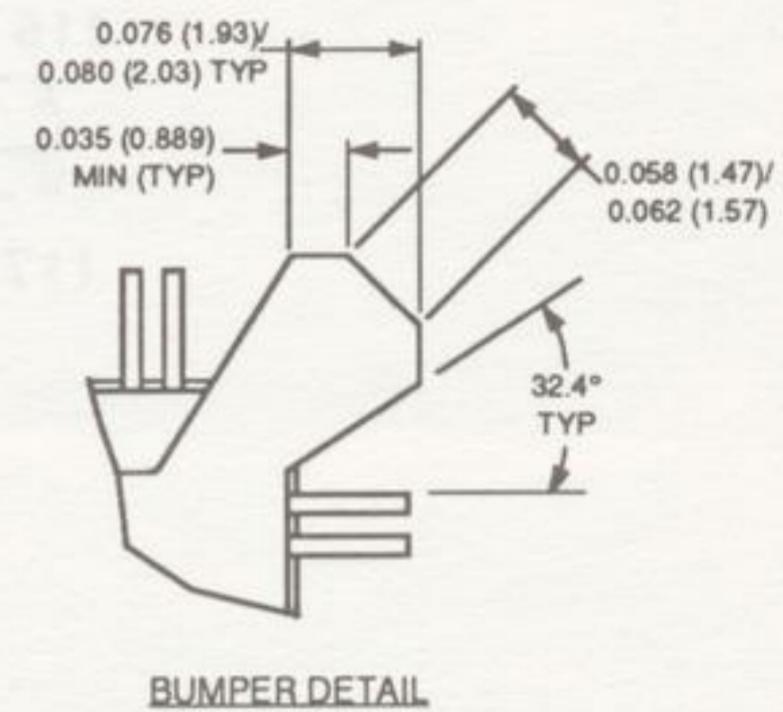
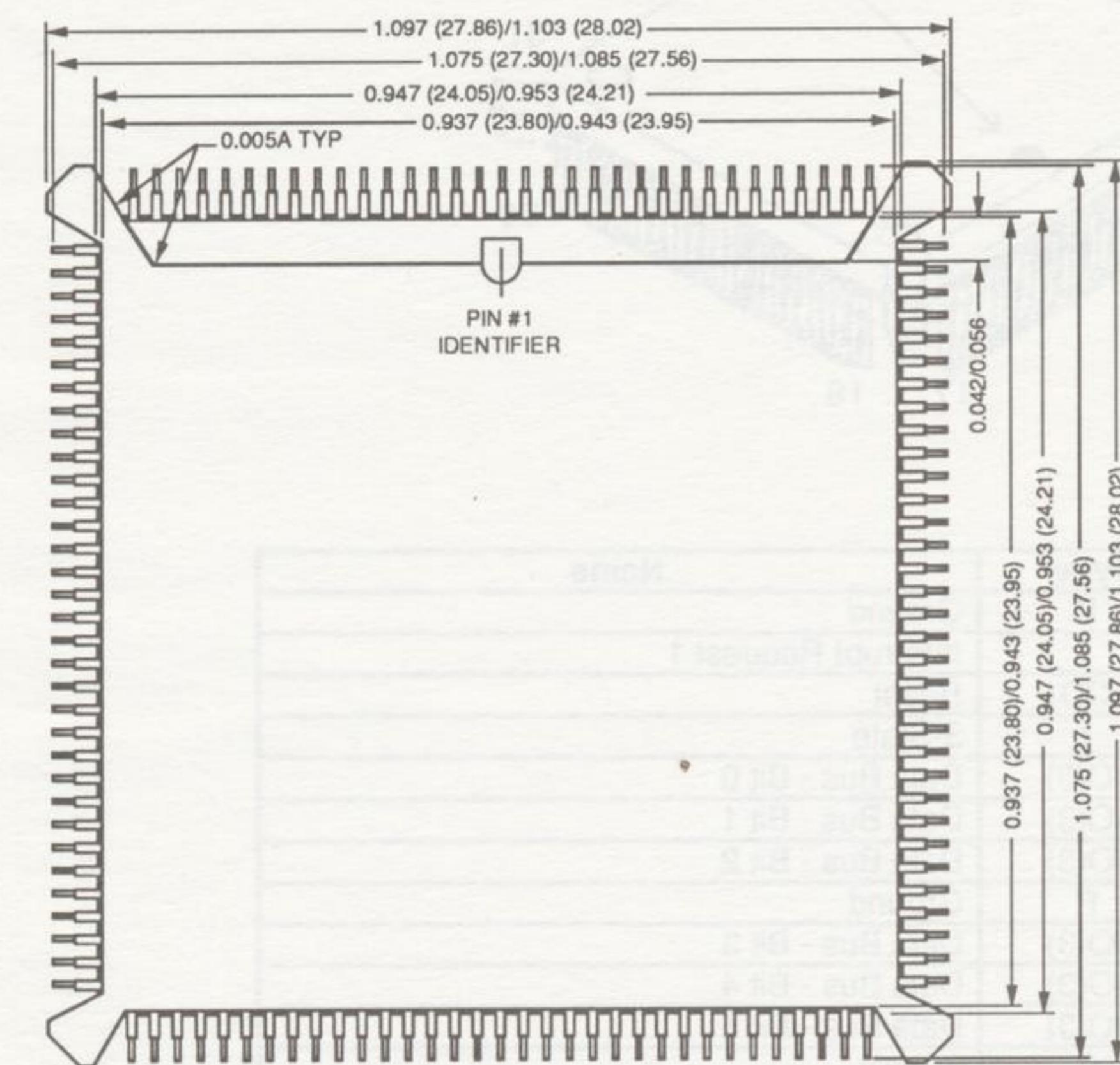
CHAPTER 11. PHYSICAL SPECIFICATIONS

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Table 11-1 Pin Descriptions	11-2

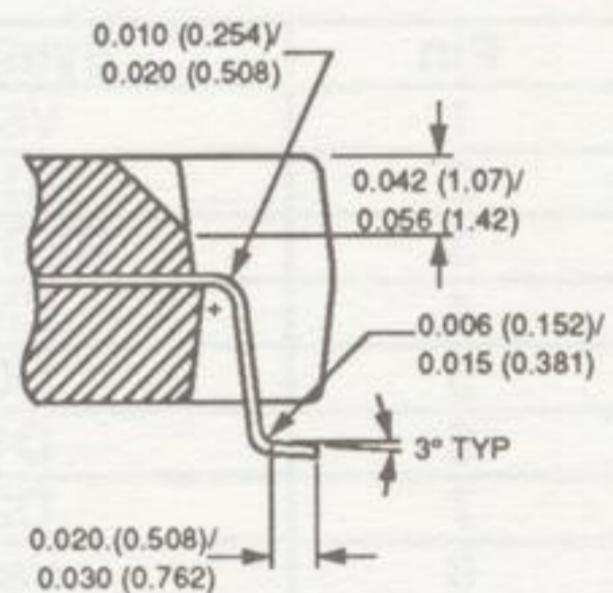
11. PHYSICAL SPECIFICATIONS

DSP3210 132-Pin PQFP (Plastic Quad Flat Package)

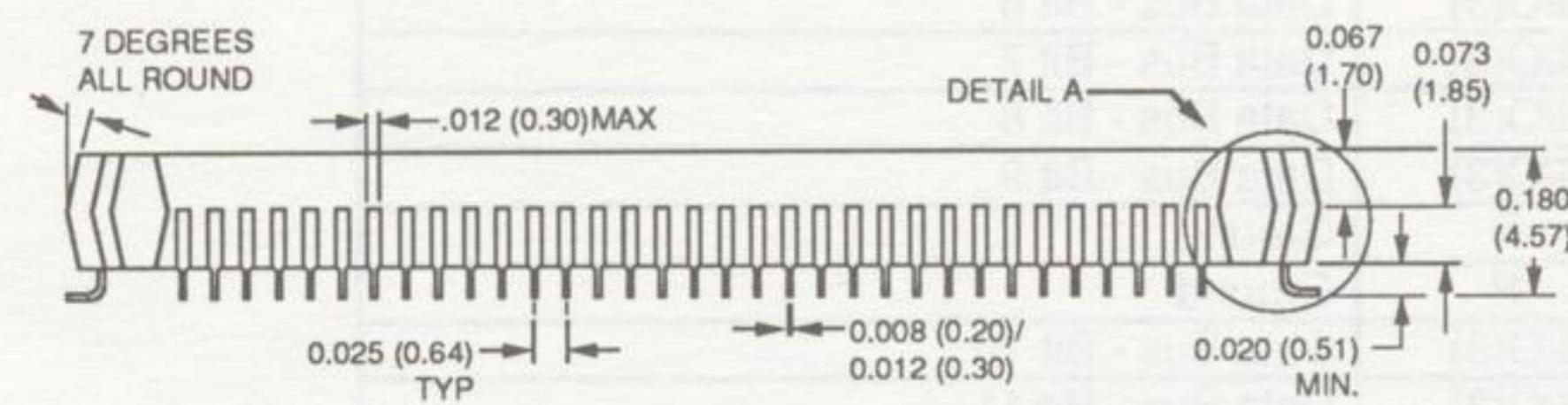
Dimensions are in inches and (millimeters).



BUMPER DETAIL



DETAIL A



11.1 Pin Assignments

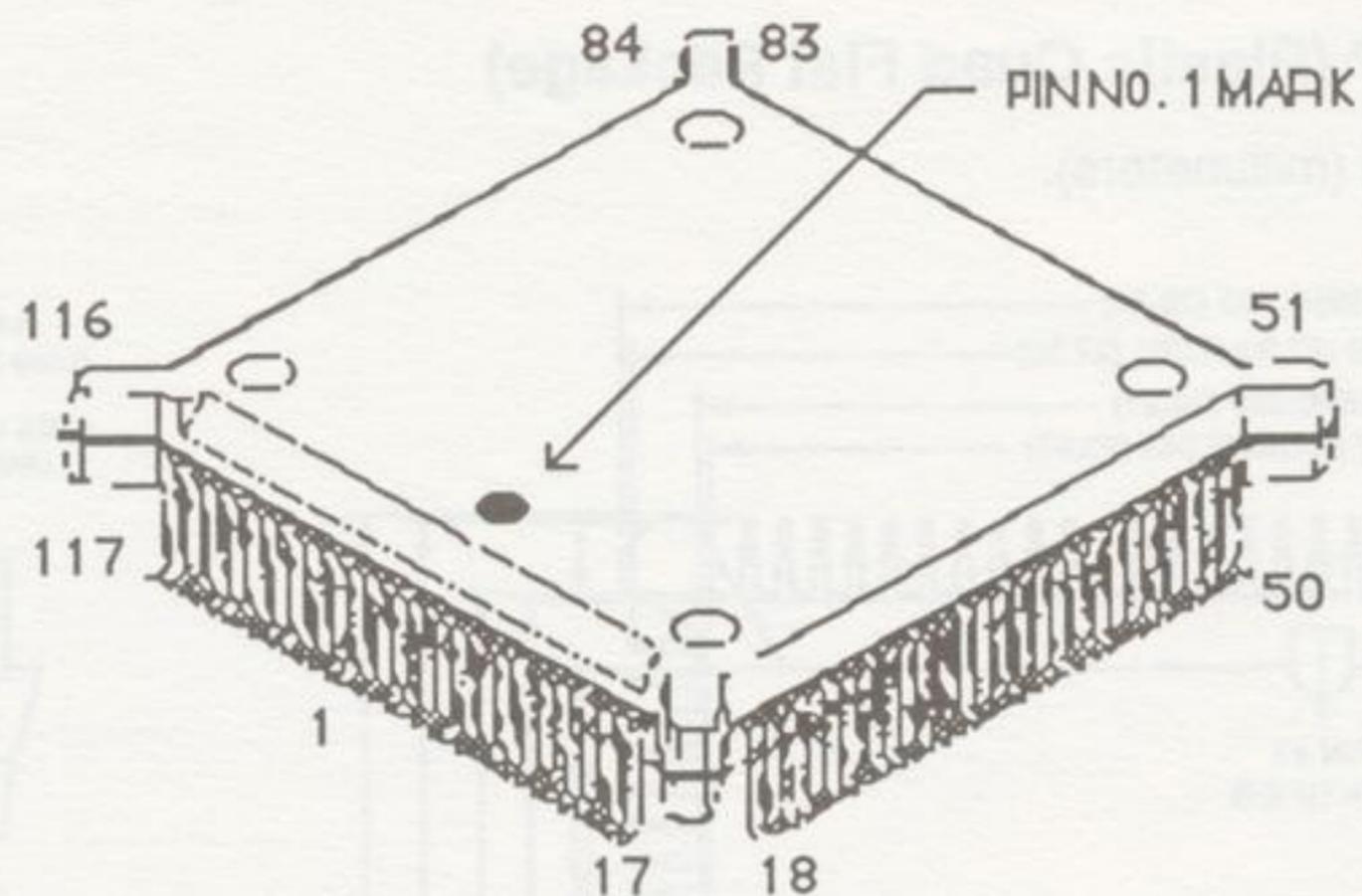


Table 11-1 Pin Descriptions

Pin	Symbol	Type*	Name
1	Vss	P	Ground
2	IR1N	I	Interrupt Request 1
3	RESTN	OD	Reset
4	ZN	I	3-State
5	D0	I/O(3)	Data Bus - Bit 0
6	D1	I/O(3)	Data Bus - Bit 1
7	D2	I/O(3)	Data Bus - Bit 2
8	Vss	P	Ground
9	D3	I/O(3)	Data Bus - Bit 3
10	D4	I/O(3)	Data Bus - Bit 4
11	D5	I/O(3)	Data Bus - Bit 5
12	VDD	P	Supply
13	D6	I/O(3)	Data Bus - Bit 6
14	D7	I/O(3)	Data Bus - Bit 7
15	D8	I/O(3)	Data Bus - Bit 8
16	D9	I/O(3)	Data Bus - Bit 9
17	Vss	P	Ground
18	Vss	P	Ground
19	D10	I/O(3)	Data Bus - Bit 10
20	D11	I/O(3)	Data Bus - Bit 11
21	D12	I/O(3)	Data Bus - Bit 12
22	D13	I/O(3)	Data Bus - Bit 13
23	VDD	P	Supply
24	D14	I/O(3)	Data Bus - Bit 14
25	D15	I/O(3)	Data Bus - Bit 15

* I = Input, O = Output, P = Power, OD = Open Drain, NC = No connection, (3) = 3-state.

Table 11-1 Pin Descriptions (continued)

Pin	Symbol	Type*	Name
26	DEN/MWN	I/O(3)	Data Enable/Write Strobe
27	Vss	P	Ground
28	DLE	I	Data Latch Enable
29	D16	I/O(3)	Data Bus - Bit 16
30	D17	I/O(3)	Data Bus - Bit 17
31	D18	I/O(3)	Data Bus - Bit 18
32	D19	I/O(3)	Data Bus - Bit 19
33	VDD	P	Supply
34	Vss	P	Ground
35	D20	I/O(3)	Data Bus - Bit 20
36	D21	I/O(3)	Data Bus - Bit 21
37	D22	I/O(3)	Data Bus - Bit 22
38	D23	I/O(3)	Data Bus - Bit 23
39	D24	I/O(3)	Data Bus - Bit 24
40	D25	I/O(3)	Data Bus - Bit 25
41	Vss	P	Ground
42	D26	I/O(3)	Data Bus - Bit 26
43	D27	I/O(3)	Data Bus - Bit 27
44	D28	I/O(3)	Data Bus - Bit 28
45	VDD	P	Supply
46	D29	I/O(3)	Data Bus - Bit 29
47	D30	I/O(3)	Data Bus - Bit 30
48	D31	I/O(3)	Data Bus - Bit 31
49	RW	O(3)	Read/Write
50	Vss	P	Ground
51	Vss	P	Ground
52	BGACKN	O(3)	Bus Grant Acknowledge
53	BRN	O(3)	Bus Request
54	ASN	O(3)	Address Strobe
55	CSN	O(3)	Cycle Start
56	BGN	I	Bus Grant
57	BERRN	I	Bus Error
58	SRDYN	I	Synchronous Ready
59	Vss	P	Ground
60	VDD	P	Supply
61	LOCKN	O(3)	Bus Lock
62	PBD/BLMN	O(3)	Page Break Detect/Block Move
63	MS3	O(3)	Memory Select 3
64	MS2	O(3)	Memory Select 2
65	MS1	O(3)	Memory Select 1
66	MS0	O(3)	Memory Select 0

* I = Input, O = Output, P = Power, OD = Open Drain, NC = No connection, (3) = 3-state.

Table 11-1 Pin Descriptions (continued)

Pin	Symbol	Type*	Name
67	Vss	P	Ground
68	A31	O(3)	Address Bus - Bit 31
69	A30	O(3)	Address Bus - Bit 30
70	A29	O(3)	Address Bus - Bit 29
71	A28	O(3)	Address Bus - Bit 28
72	A27	O(3)	Address Bus - Bit 27
73	VDD	P	Supply
74	Vss	P	Ground
75	A26	O(3)	Address Bus - Bit 26
76	A25	O(3)	Address Bus - Bit 25
77	A24	O(3)	Address Bus - Bit 24
78	A23	O(3)	Address Bus - Bit 23
79	A22	O(3)	Address Bus - Bit 22
80	A21	O(3)	Address Bus - Bit 21
81	A20	O(3)	Address Bus - Bit 20
82	A19	O(3)	Address Bus - Bit 19
83	Vss	P	Ground
84	Vss	P	Ground
85	AEN/MRN	I/O(3)	Address Enable/Read Strobe
86	A18	O(3)	Address Bus - Bit 18
87	VDD	P	Supply
88	A17	O(3)	Address Bus - Bit 17
89	A16	O(3)	*Address Bus - Bit 16
90	A15	O(3)	Address Bus - Bit 15
91	A14	O(3)	Address Bus - Bit 14
92	Vss	P	Ground
93	A13	O(3)	Address Bus - Bit 13
94	A12	O(3)	Address Bus - Bit 12
95	A11	O(3)	Address Bus - Bit 11
96	A10	O(3)	Address Bus - Bit 10

* I = Input, O = Output, P = Power, OD = Open Drain, NC = No connection, (3) = 3-state.

Table 11-1 Pin Descriptions (continued)

Pin	Symbol	Type*	Name
97	A9	O(3)	Address Bus - Bit 9
98	VDD	P	Supply
99	Vss	P	Ground
100	A8	O(3)	Address Bus - Bit 8
101	A7	O(3)	Address Bus - Bit 7
102	A6	O(3)	Address Bus - Bit 6
103	A5	O(3)	Address Bus - Bit 5
104	A4	O(3)	Address Bus - Bit 4
105	A3	O(3)	Address Bus - Bit 3
106	Vss	P	Ground
107	A2	O(3)	Address Bus - Bit 2
108	CKI	I	Clock In
109	BIO7	I/O(3)	Bit I/O - Bit 7
110	BIO6	I/O(3)	Bit I/O - Bit 6
111	VDD	P	Supply
112	BIO5	I/O(3)	Bit I/O - Bit 5
113	BIO4	I/O(3)	Bit I/O - Bit 4
114	BIO3	I/O(3)	Bit I/O - Bit 3
115	BIO2	I/O(3)	Bit I/O - Bit 2
116	Vss	P	Ground
117	Vss	P	Ground
118	BIO1	I/O(3)	Bit I/O - Bit 1
119	BIO0	I/O(3)	Bit I/O - Bit 0
120	SY	I/O(3)	Sync
121	ICK	I/O(3)	Input Clock
122	VDD	P	Supply
123	DI	I	Serial Data In
124	DO	O(3)	Serial Data Out
125	OCK	I/O(3)	Output Clock
126	Vss	P	Ground
127	ILD	I/O(3)	Input Load
128	OLD	I/O(3)	Output Load
129	IACK0	O(3)	Interrupt Acknowledge 0
130	IACK1	O(3)	Interrupt Acknowledge 1
131	IR0N	I	Interrupt Request 0
132	VDD	P	Supply

* I = Input, O = Output, P = Power, OD = Open Drain, NC = No connection, (3) = 3-state.

Chapter 12

Electrical Specifications

CHAPTER 12. ELECTRICAL SPECIFICATIONS

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12. ELECTRICAL AND TIMING SPECIFICATIONS

12.1 Electrical Specifications

Table 12-1 Electrical Requirements and Characteristics

The parameters below are valid for the following conditions: TA = 0 to 70 °C; VDD = 5 V ± 5%; VSS = 0 V

Description	Symbol	Min	Max	Unit
Input Voltage except CKI: Low High	VIL	—	0.8	V
	VIH	2.0	—	V
Input Voltage for CKI: Low High	VIIC	—	0.4	V
	VIHC	2.4	—	V
Output Voltage: (IOL = 6 mA) Low (TTL) (IOL = 5 μA) Low (CMOS) (IOL = -2 mA) High (TTL) (IOL = -5 μA) High (CMOS)	VOL	—	0.4	V
	VOL	—	0.2	V
	VOH	2.4	—	V
	VOH	VDD - 0.2	—	V
Output Current: (VOL = 0.4 V) Low (VOH = 2.4 V) High	IOL	—	6.0	mA
	IOH	-2.0	—	mA
Input Leakage except ZN: a a	IIL	-5	—	μA
	IIH	—	5	μA
Input Leakage for ZN: (VIL = 0 V) Low (VIH = 5.5V) High	IIL	-100	—	μA
	IIH	—	5	μA
Output Hi-Z Current: (Vapplied = 0.0 V) Low (Vapplied = 5.25 V) High	IOZL	-10	—	μA
	IOZH	—	10	μA
Input, Output, IOput capacitance	CI	—	10	pF
Power Supply Current*	IDD	—	220	mA
Power Dissipation†	PD	—	1.20	W

* Current in the input buffers is highly dependent on the input voltage level. At full CMOS levels, essentially no DC current is drawn, but for levels near the threshold of 1.4 V, high and unstable levels of current may flow. There are 56 input buffers on the chip. If all inputs are connected to a dc voltage of 1.4 V, an additional current in the range of 100 mA can be drawn.

† The power dissipation listed is for internal power dissipation only. Total power dissipation can be calculated based on the system configuration by adding C * VDD² * f for each output, where C is the load capacitance, and f is the output frequency.

12.1.1 Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

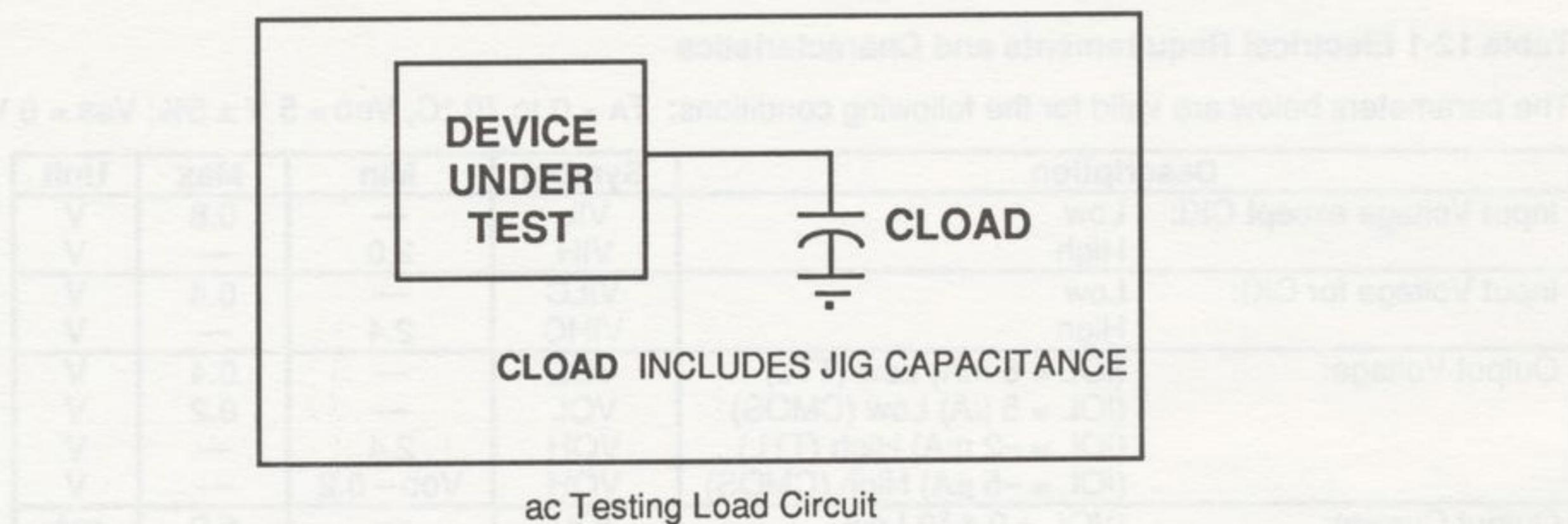
VOLTAGE RANGE ON ANY PIN WITH RESPECT TO GROUND	-0.5 to + 6 V
AMBIENT TEMPERATURE RANGE	-40 to +120 °C
STORAGE TEMPERATURE RANGE	-65 to +150 °C

Warning: All CMOS devices are prone to latch-up if excessive current is injected to/from the substrate. To prevent latch-up at power-up, no input pin should be subjected to input voltages greater than VIL, or less than VSS - 0.5 V before VDD is applied. After power-up, input should not be greater than VDD + 0.5 V or less than VSS - 0.5 V.

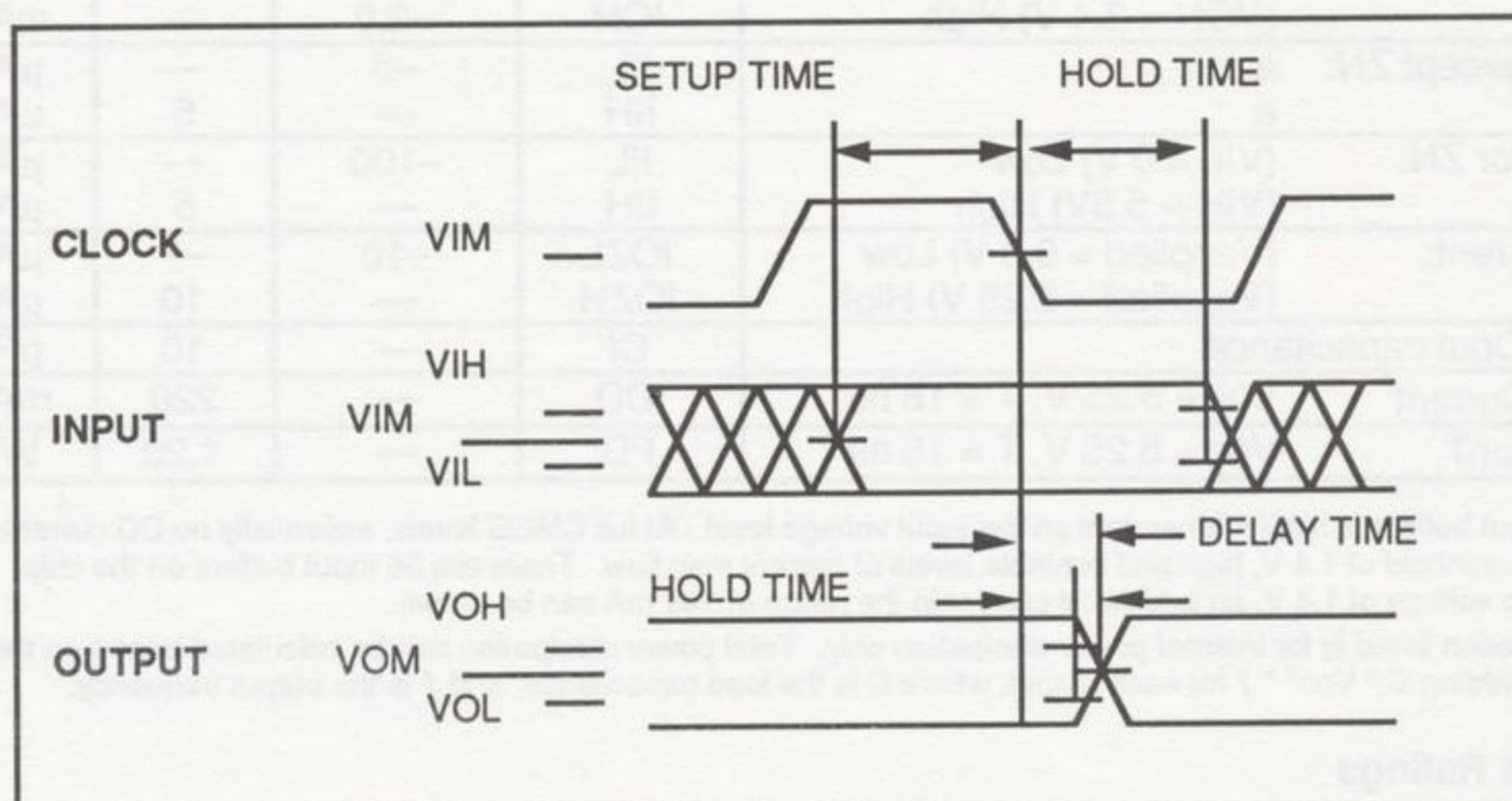
Handling Precautions: All MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. Although input protection circuitry has been incorporated into the devices to minimize the effect of this static buildup, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting. AT&T employs a human body model for ESD susceptibility testing. Since the failure voltage of electronic devices is dependent on the current and voltage and, hence, the resistance and capacitance, it is important that standard values be employed to establish a reference by which to compare test data. Values of 100 pF and 1500 Ω are the most common and are the values used in the AT&T human body model test circuit. The breakdown voltage for the DSP3210 is greater than 2000 V, according to the human body model. ESD data for the charge device model is available on request.

12.2 Timing Specifications

The characteristics listed are valid under the following conditions: VDD = 5 V ± 5%; Vss = 0 V; TA = 0 to 70 °C.



ac Testing Load Circuit



ac Testing Input, Output Waveform

Test conditions for inputs (unless otherwise specified):

- Rise and fall times of 4 ns or less
- Timing reference level for setup times is VIM = 1.5V
- Timing reference levels for hold times is VIH, VIL

Test conditions for outputs (unless otherwise specified):

- CLOAD = 50 pF unless otherwise stated
- Timing reference level for delay times is VOM = 1.5 V
- Timing reference levels for hold times is VOH, VOL

Tables 12-2 to 12-18 are the timing specifications for the 55 MHz DSP3210.

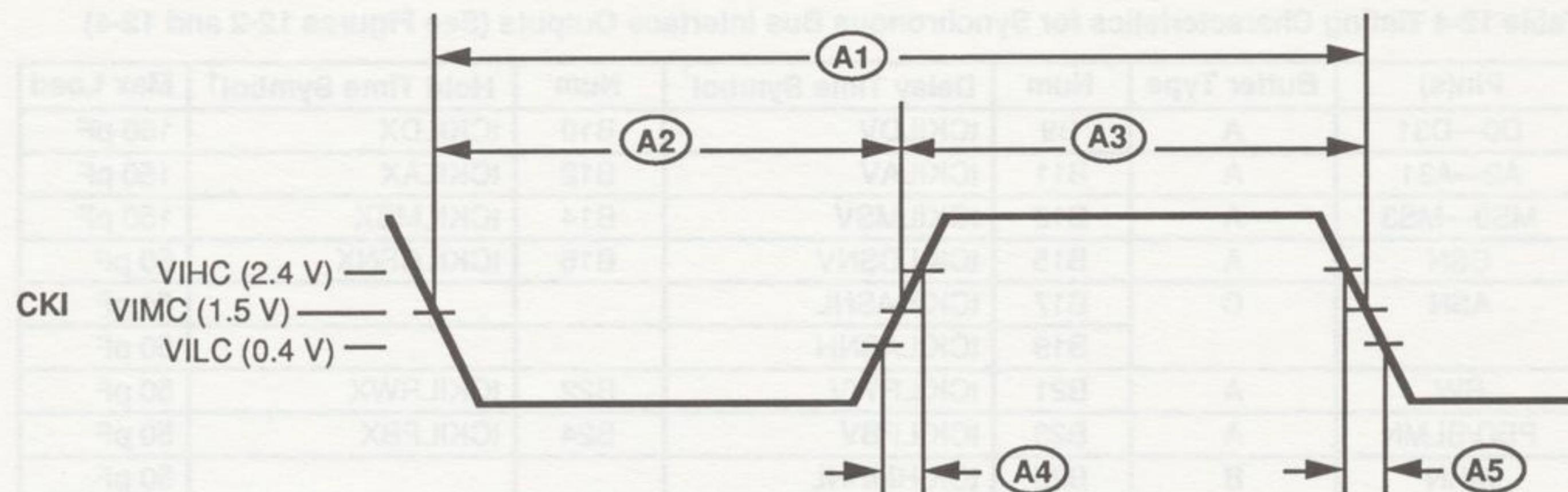


Table 12-2 Timing Requirements for CKI (See Figure 12-1)

Num*	Symbol	Description	55 MHz		
			Min	Max	Unit
A1	tCKILCKIL	Clock In Period†	18	—‡	ns
A2	tCKILCKIH	Clock In Low	8.1	—	ns
A3	tCKIHCKIL	Clock In High	8.1	—	ns
A4	tCKIRISE	Clock In Rise Time	—	4	ns
A5	tCKIFALL	Clock In Fall Time	—	4	ns

* This column in all timing requirements and/or characteristic tables refers to the internal alpha-numeric symbol in the timing diagrams.

† tCKILCKIL is referred to as T for specifications that are a function of the period of CKI.

‡ This device is static. However, the maximum period guaranteed by test is 50 ns.

Table 12-3 Timing Requirements for Synchronous Bus Interface Inputs (See Figures 12-2 and 12-4)

Num	Symbol	Description	Min	Max	Unit
B1	tSRNVCKIL	SRDYN Setup to CKI Low	6	—	ns
B2	tCKILSRNX	SRDYN Hold after CKI Low	3	—	ns
B3	tBENVCKIL	BERRN Setup to CKI Low	6	—	ns
B4	tCKILBRNX	BERRN Hold after CKI Low	3	—	ns
B5	tBGNVCKIL	BGN Setup to CKI Low	6	—	ns
B6	tCKILBGNX	BGN Hold after CKI Low	3	—	ns
B7	tDVCKIL	DATAin Setup to CKI Low	0	—	ns
B8	tCKILDX	DATAin Hold after CKI Low	6	—	ns

Table 12-4 Timing Characteristics for Synchronous Bus Interface Outputs (See Figures 12-2 and 12-4)

Pin(s)	Buffer Type	Num	Delay Time Symbol*	Num	Hold Time Symbol†	Max Load
D0—D31	A	B9	tCKILDV	B10	tCKILDX	150 pF
A2—A31	A	B11	tCKILAV	B12	tCKILAX	150 pF
MS0—MS3	A	B13	tCKILMSV	B14	tCKILMSX	150 pF
CSN	A	B15	tCKILCSNV	B16	tCKILCSNX	50 pF
ASN	C	B17	tCKIHASNLL			50 pF
		B19	tCKILASNHH			50 pF
RW	A	B21	tCKILRWV	B22	tCKILRWX	50 pF
PBD/BLMN	A	B23	tCKILPBV	B24	tCKILPBX	50 pF
MRN	B	B25	tCKIHMRLNL			50 pF
		B27	tCKILMRNHH			50 pF
MWN	B	B29	tCKIHMWNV			50 pF
LOCKN	A	B31	tCKILLONV	B32	tCKILLONX	50 pF
BRN	A	B33	tCKILBRNV	B34	tCKILBRNX	50 pF
BGACKN	B	B35	tCKILBGANL	B36	tCKILBGANHX	50 pF
		B37	tCKIHBGANH	B38	tCKIHBGANLX	50 pF

* Description for all Delay Time Symbols in this table is: CKI (Low, High) to Signal (Valid, High, Low).

† Description for all Hold Time Symbols in this table is: Signal Value Held after CKI (Low, High).

Synchronous Delay Times (B9,B11,...B35,B37)		Min			Max			Unit
Buffer Type		A	B	C	A	B	C	
VOM	50 pF	—	—	—	15	14	13	ns
	100 pF	—	NA	NA	18	NA	NA	ns
	150 pF	—	NA	NA	21	NA	NA	ns
VOL	50 pF	—	—	—	17	16	15	ns
	100 pF	—	NA	NA	22	NA	NA	ns
	150 pF	—	NA	NA	27	NA	NA	ns
VOH	50 pF	—	—	—	17	16	15	ns
	100 pF	—	NA	NA	20	NA	NA	ns
	150 pF	—	NA	NA	23	NA	NA	ns
Synchronous Hold Times (B10,B12,...B36,B38)		Min			Max			Unit
Buffer Type		A	B	C	A	B	C	
VOL	50,100,150 pF	5	4	4	—	—	—	ns
VOH	50,100,150 pF	5	5	5	—	—	—	ns

Note: NA = Not Applicable.

Table 12-5 Timing Relationships for Synchronous Bus Interface Operation (See Figure 12-2)

Note: All signals referred to in this table are equally loaded with 50 pF. Signal timing relationships with respect to DATAin supercede B7 and B8 timing requirements.

Num	Symbol	Description	Min	Max	Unit
B39	tCKILDE	Data Bus Low-Z after CKI Low	0	—	ns
B40	tCKILDZ	Data Bus Hi-Z after CKI Low	—	12	ns
B41	tAVDINV	Address * Valid to DATAin Valid	—	$2 * T - 11 + N * T$	ns
B42	tAVASNL	Address Valid to Address Strobe Low	$0.5 * T - 3^{\dagger}$	$0.5 * T$	ns
B43	tASNLASNH	Address Strobe Width	$1.5 * T - 2 + N * T$	—	ns
B44	tASNHAX	Address Hold after Address Strobe High	0	—	ns
B45	tASNLDINV	Address Strobe Low to DATAin Valid	—	$1.5 * T - 9 + N * T$	ns
B46	tDINASNH	DATAin Setup to Address Strobe High	8	—	ns
B47	tASNHDX	DATAin Hold after Address Strobe High	-2	—	ns
B48	tASNHDZ	Data Bus Hi-Z after Address Strobe High	-3.0	2	ns
B49	tAVMRNL	Address Valid to Read Strobe Low	$0.5 * T - 4$	—	ns
B50	tMRNLMRNH	Read Strobe Width	$1.5 * T - 4 + N * T$	—	ns
B51	tMRNHRMRNL	Read Strobe High to Read Strobe Low	$0.5 * T - 2$	—	ns
B52	tMRNLDINV	Read Strobe Low to DATAin Valid	—	$1.5 * T - 11 + N * T$	ns
B53	tDINVMGNH	DATAin Setup to Read Strobe High	10	—	ns
B54	tMRNHDX	DATAin Hold after Read Strobe High	-4	—	ns
B55	tMRNHDE	Read Strobe High to Data Bus Low-Z	$T - 4$	—	ns
B56	tRWVDE	Read-Write Asserted to Data Bus Low-Z	$T - 4$	—	ns
B57	tAVMWNL	Address Valid to Write Strobe Low	$0.5 * T - 4$	—	ns
B58	tMWNLMWNH	Write Strobe Width	$T + M * T^{\ddagger}$	—	ns
B59	tMWNHAX	Address Hold after Write Strobe High	$0.5 * T - 4$	—	ns
B60	tDVMWNH	Data Bus Valid to Write Strobe High: 0—1 Configured Wait-States 2—3 Configured Wait-States	$0.5 * T - 2$ $0.5 * T - 2 + (M - 1) * T$	— —	ns ns
B61	tMWNHDZ	Data Bus Hi-Z after Write Strobe High	$0.5 * T - 4$	$0.5 * T + (N - M) * T + 2$	ns
B77	tASNLDV	Address Strobe Low to Data Bus Valid: 0 ws 1—3 ws	—	$0.5 * T + 2$ $1.5 * T + 2$	ns ns

* Address refers to A2—A31 and MS0—MS3.

† T = tCKILCKIL; N = number of wait-states (programmed plus external).

‡ M = Number of wait-states configured in pcw.

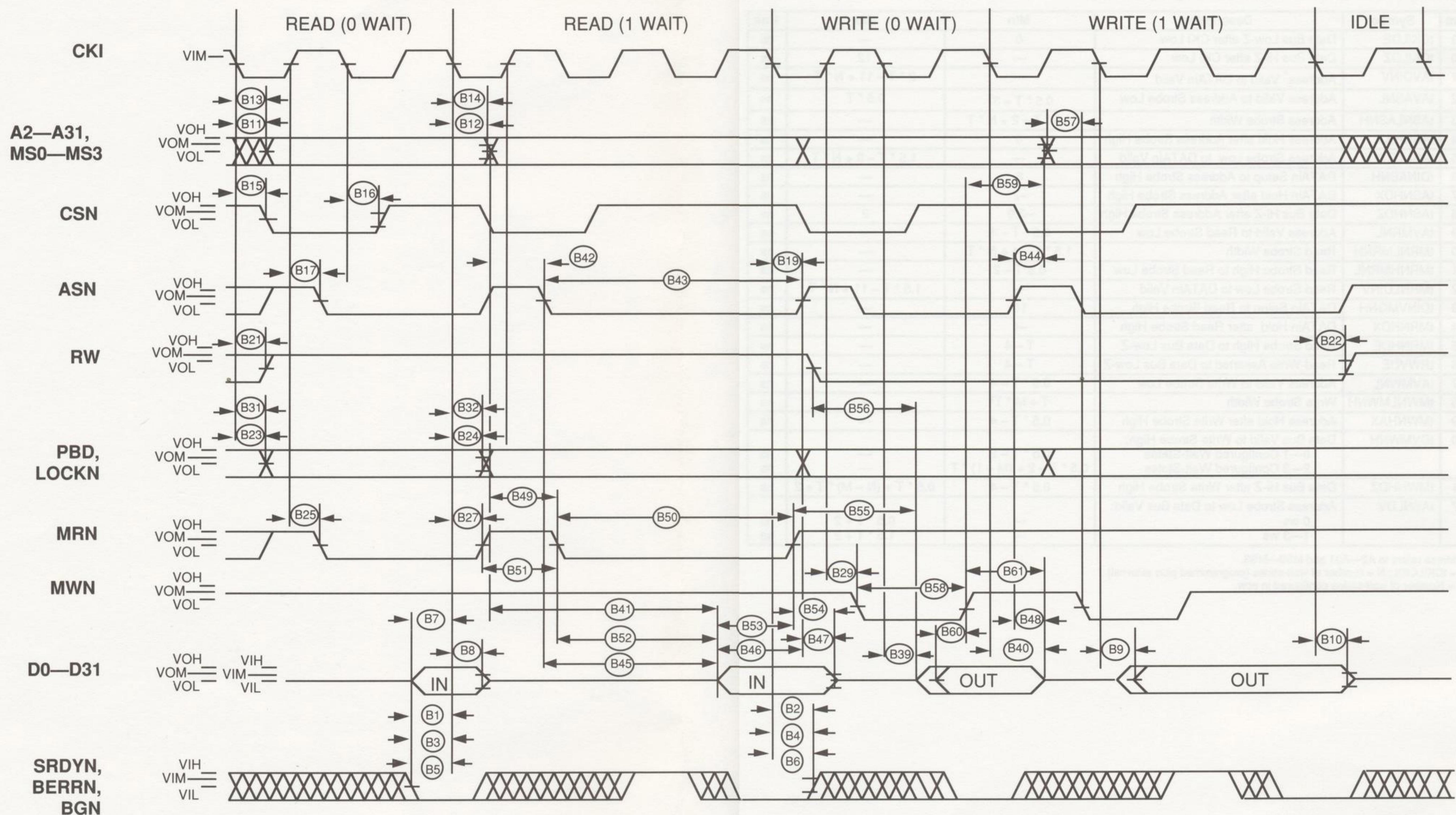


Figure 12-2 Synchronous Bus Interface Timing

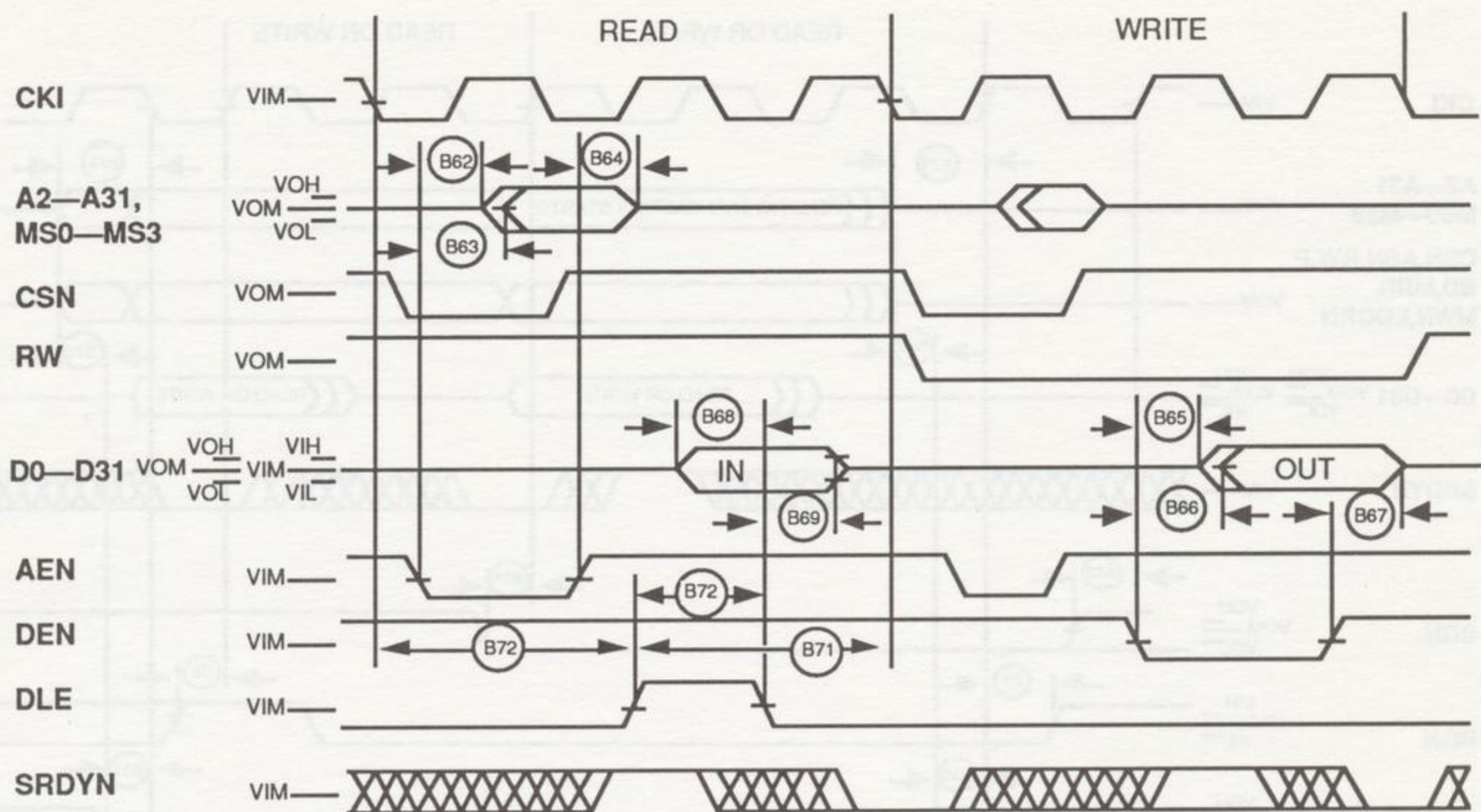


Figure 12-3 Asynchronous Bus Interface Timing

Table 12-6 Timing Relationships for Asynchronous Bus Interface Operation (See Figure 12-3)

Num	Symbol	Description	Min	Max	Unit
B62	taENLAE	Address* Enable Low to Address Low-Z	0	—	ns
B63	taENLAV: 50 pF 100 pF 150 pF	Address Enable Low to Address Valid	—	12 16 19	ns ns ns
B64	taENHAZ	Address Enable High to Address High-Z	—	7	ns
B65	tDENLDE	Data Enable Low to Data Bus Low-Z	0	—	ns
B66	tDENLDV: 50 pF 100 pF 150 pF	Data Enable Low to Data Bus Valid	—	12 16 19	ns ns ns
B67	tDENHDZ	Data Enable High to Data Bus High-Z	—	7	ns
B68	tDVDLEL	DATAin Setup to Data Latch Enable Low	2	—	ns
B69	tDVDLEL	DATAin Hold after Data Latch Enable Low	4	—	ns
B70	tDLEHDLEL	Data Latch Enable Width	8	—	ns
B71	tDLEHCKIL	Data Latch Enable High to CKI Low when Asserted during State Ending Read Transaction (Bus Interface State Machine is in State E and SRDYN is Asserted)	3	—	ns
B72	tCKILDLEH	CKI Low to Data Latch Enable High after State Ending Read Transaction	6	—	ns

* Address refers to A2—A31 and MS0—MS3.

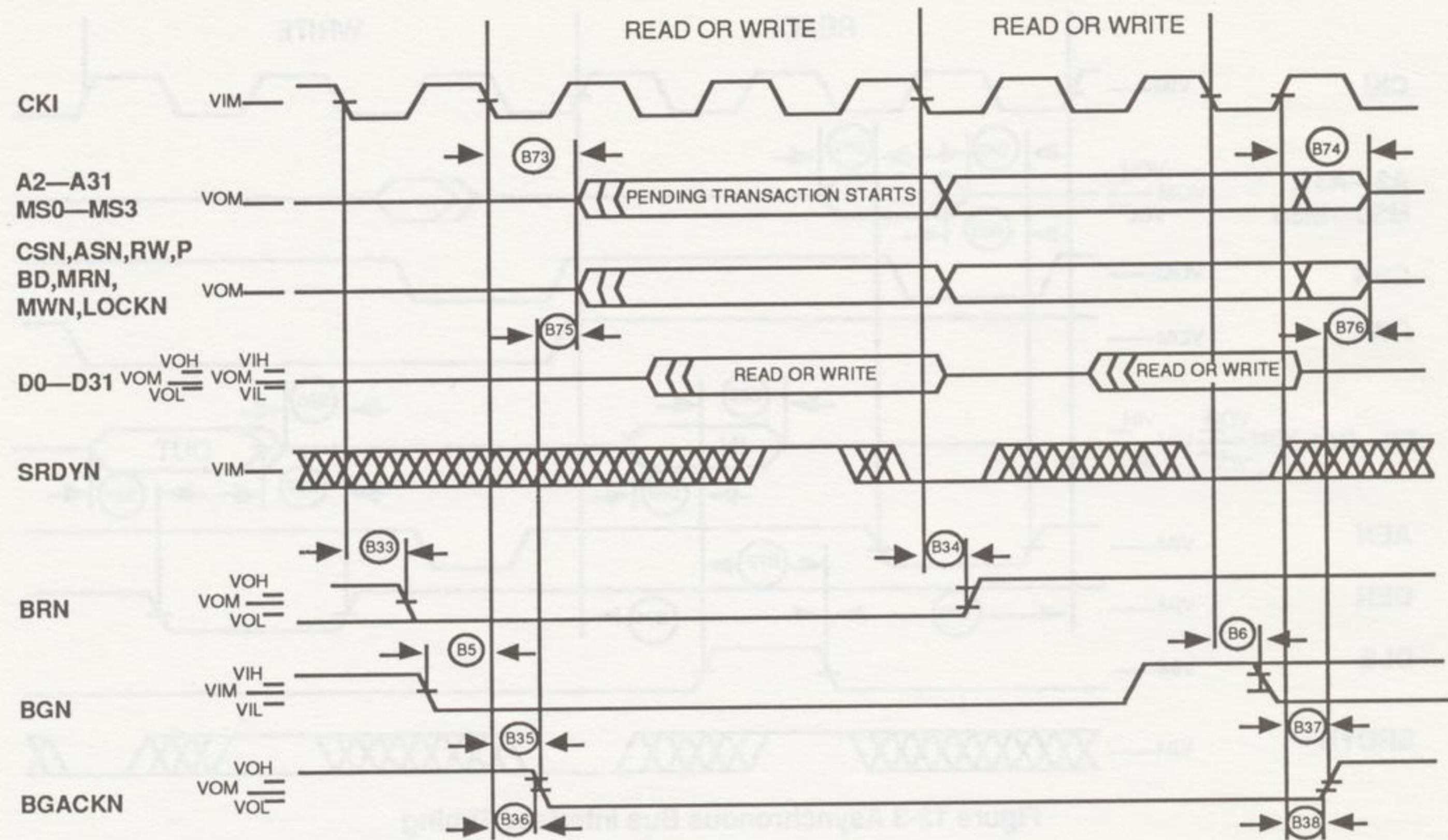


Figure 12-4 Bus Arbitration Timing

Table 12-7 Timing Characteristics for Bus Arbitration (See Figure 12-4)

Num	Symbol	Description	Min	Max	Unit
B73	tCKILBISE	CKI Low to Bus Interface Signals * Low-Z	4	—	ns
B74	tCKILDZ	CKI High to Bus Interface Signals High-Z	4	12	ns
B75	tBGANLBISE	BGACKN Low to Bus Interface Signals Low-Z	-4	—	ns
B76	tBGANHBISZ	BGACKN High to Bus Interface Signals High-Z	-4	2	ns

* Bus Interface Signals are defined to be A2—A31, MS0—MS3, CSN, ASN, RW, PBD, MRN, MWN, and LOCKN.

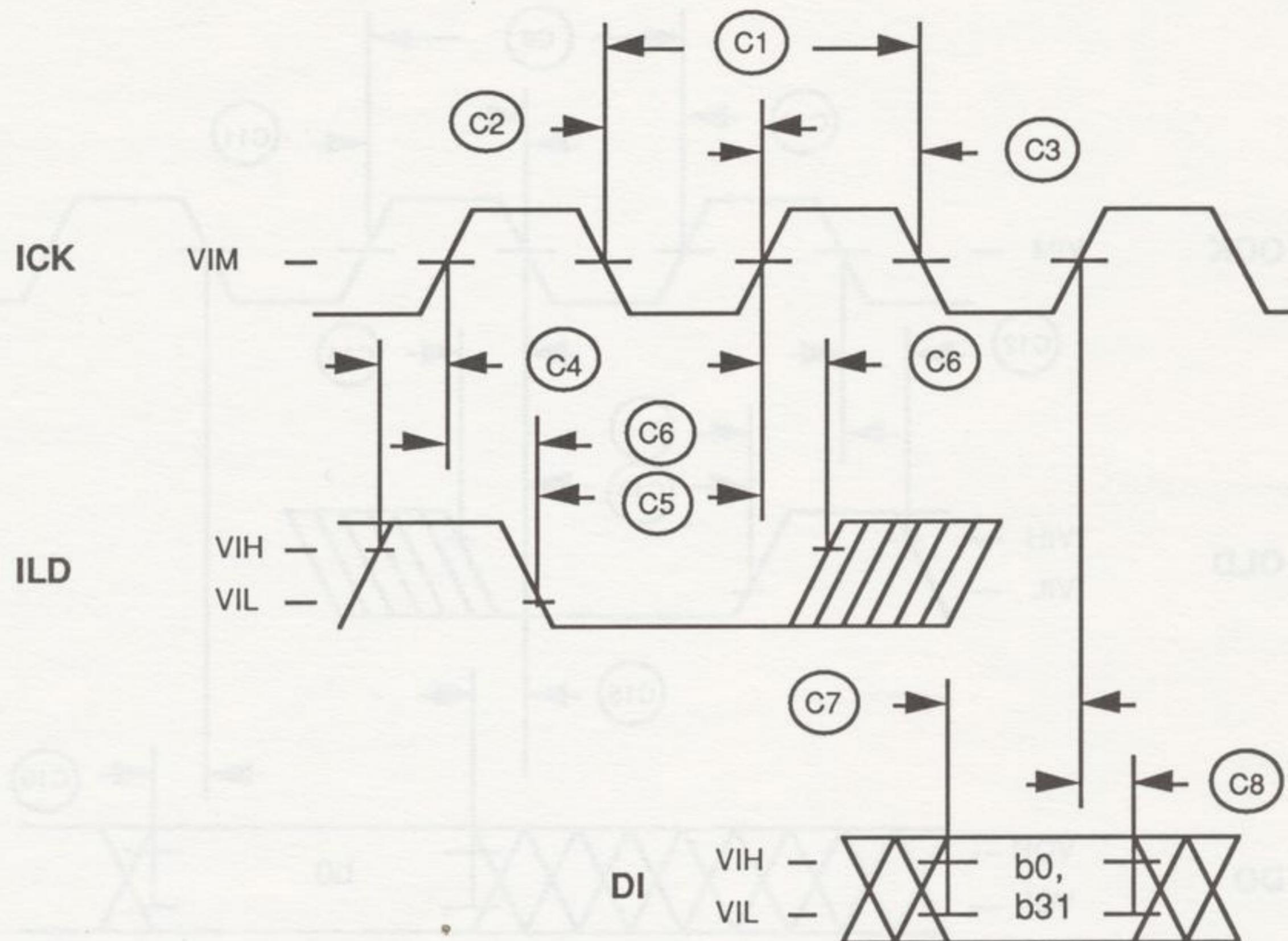


Figure 12-5 Serial Input Timing

Table 12-8 Timing Requirements for Serial Inputs (See Figure 12-5)

Num	Symbol	Description	Min	Max	Unit
C1	tICKLICKL	Serial Input Clock Period	40	—*	ns
C2	tICKLICKH	Serial Input Clock Low Time	18	—	ns
C3	tICKHICKL	Serial Input Clock High Time	18	—	ns
C4	tILDHICKH	Input Load High Setup Time	8	—	ns
C5	tILDLICKH	Input Load Low Setup Time	8	—	ns
C6	tICKHILDX	Input Load Hold Time	0	—	ns
C7	tDIVICKH	Serial Input Data Setup	8	—	ns
C8	tICKHDIX	Serial Input Data Hold	0	—	ns

* This device is static. However, the maximum period guaranteed by test is 200 ns.

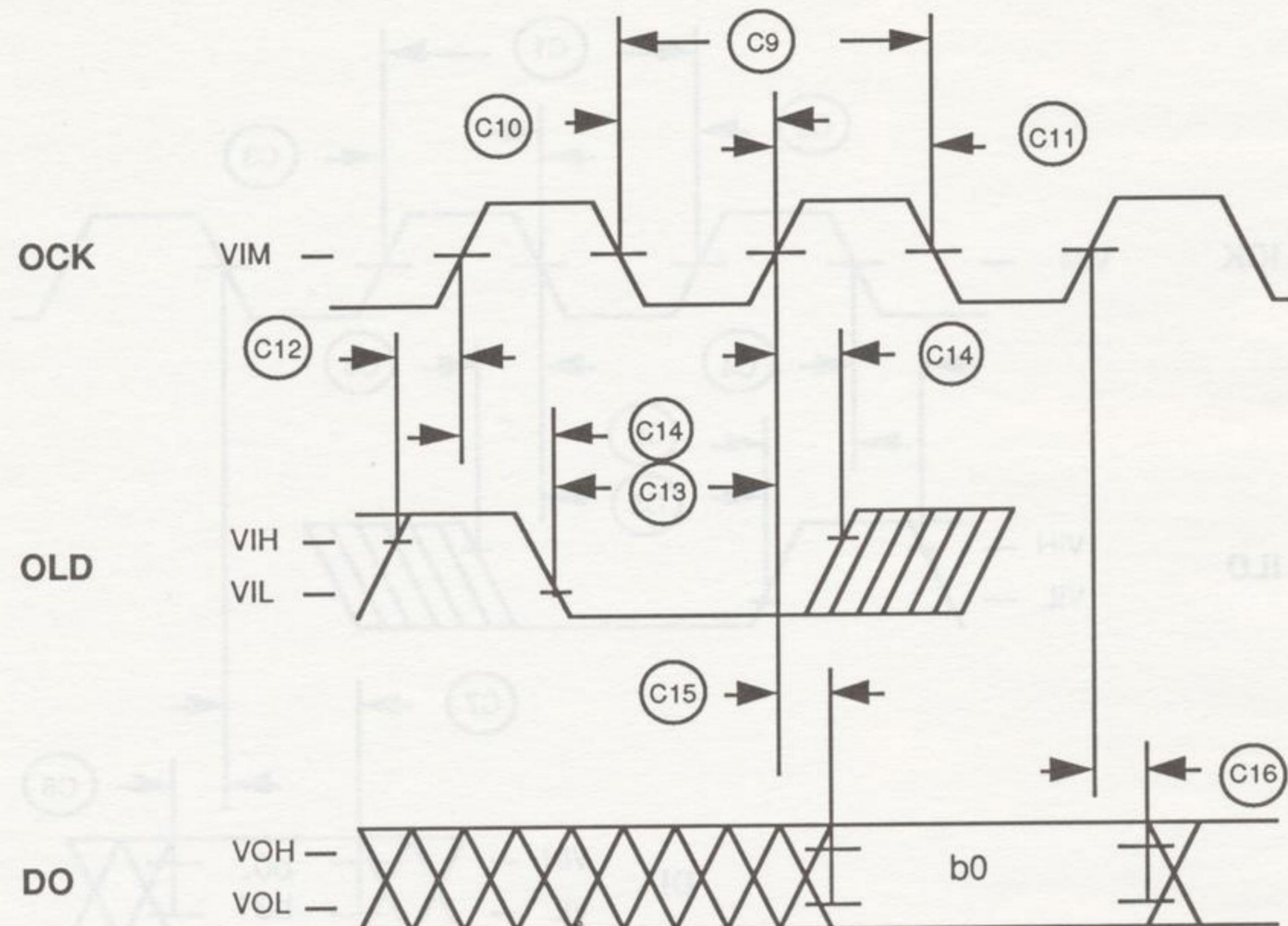


Figure 12-6 Serial Output Timing

Table 12-9 Timing Requirements for Serial Outputs (See Figure 12-6)

Num	Symbol	Description	Min	Max	Unit
C9	tOCKLOCKL	Serial Output Clock Period	40	—*	ns
C10	tOCKLOCKH	Serial Output Clock Low Time	18	—	ns
C11	tOCKHOCKL	Serial Output Clock High Time	18	—	ns
C12	tOLDHOCKH	Output Load High Setup Time	8	—	ns
C13	tOLDLOCKH	Output Load Low Setup Time	8	—	ns
C14	tOCKHOLDX	Output Load Hold Time	0	—	ns

* This device is static. However, the maximum period guaranteed by test is 200 ns.

Table 12-10 Timing Characteristics for Serial Outputs (See Figure 12-6)

Num	Symbol	Description	Min	Max	Unit
C15	tOCKHDOV	Serial Output Data Delay	—	23	ns
C16	tOCKHDOX	Serial Output Data Hold	2	—	ns

Table 12-11 Timing Requirements for Serial Clock Generation (See Figure 12-7)

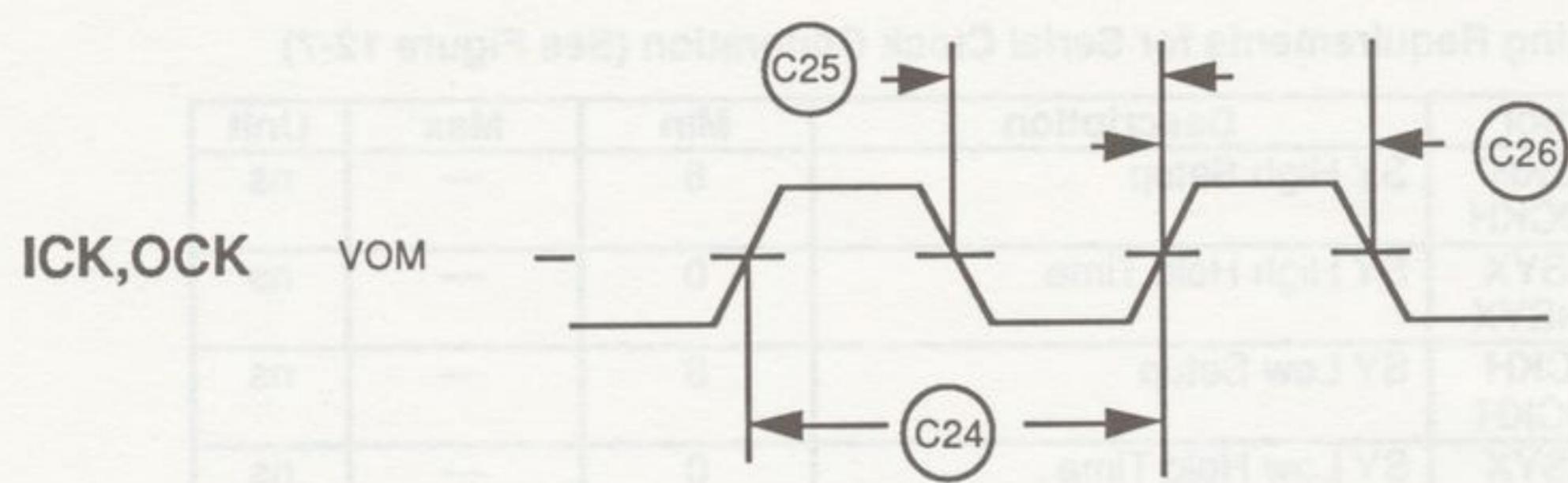
Num	Symbol	Description	Min	Max	Unit
C17	tSYHICKH* tSYHOCKH	SY High Setup	8	—	ns
C18	tICKHSYX tOCKHSYX	SY High Hold Time	0	—	ns
C19	tSYLICKH tSYLOCKH	SY Low Setup	8	—	ns
C20	tICKHSYX tOCKHSYX	SY Low Hold Time	0	—	ns

* ICK or OCK as selected by IOC[1].

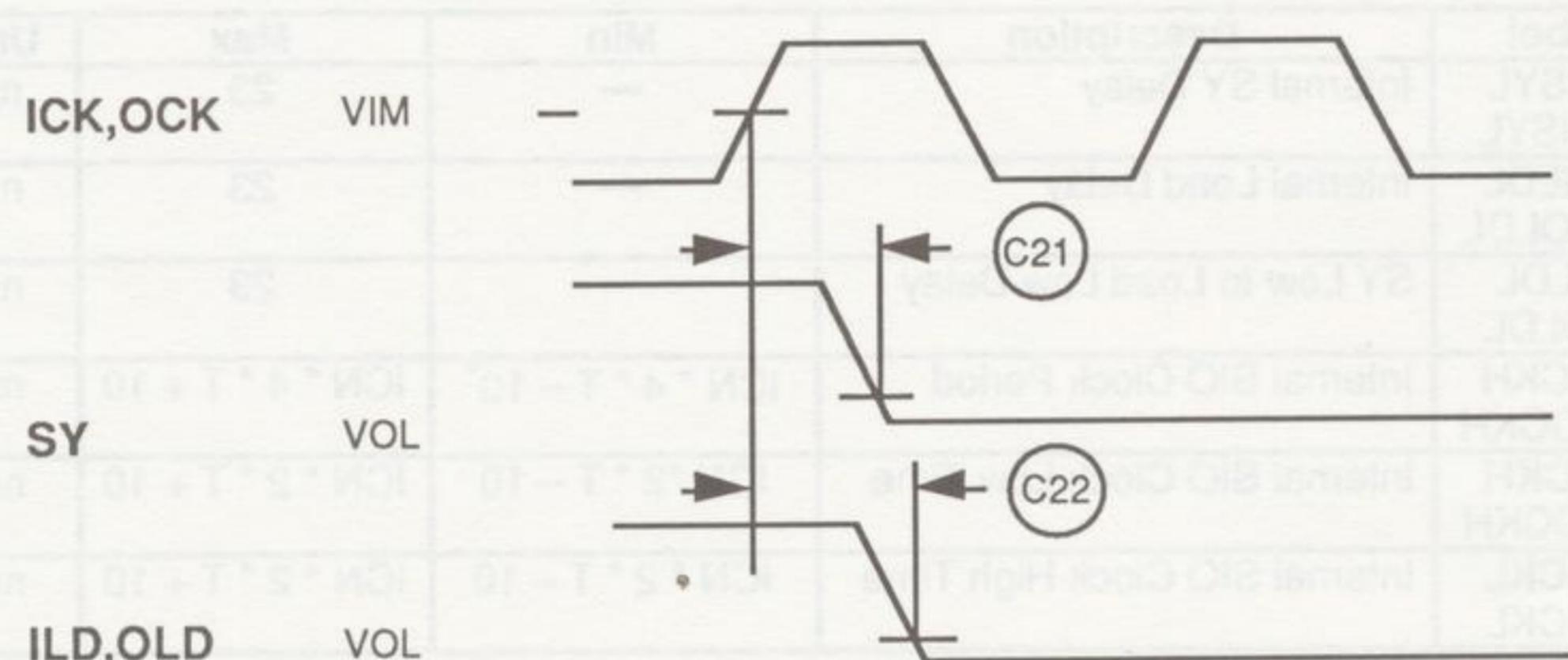
Table 12-12 Timing Characteristics for Serial Clock Generation (See Figure 12-7)

Num	Symbol	Description	Min	Max	Unit
C21	tICKHSYL tOCKHSYL	Internal SY Delay	—	23	ns
C22	tICKHIDL tOCKHOLDL	Internal Load Delay	—	23	ns
C23	tSYLILDL tSYLOLDL	SY Low to Load Low Delay	—	23	ns
C24	tICKHICKH tOCKHOCKH	Internal SIO Clock Period	ICN * 4 * T - 10*	ICN * 4 * T + 10	ns
C25	tICKLICKH tOCKLOCKH	Internal SIO Clock Low Time	ICN * 2 * T - 10	ICN * 2 * T + 10	ns
C26	tICKHICKL tICKHICKL	Internal SIO Clock High Time	ICN * 2 * T - 10	ICN * 2 * T + 10	ns

* ICN refers to the value of the four bit field IOC[23—20]. When ICN=0, the period of the clock is infinity. (The clock is disabled from counting.)



a. internal ICK/OCK



b. internal ILD/OLD/SY. external ICK/OCK

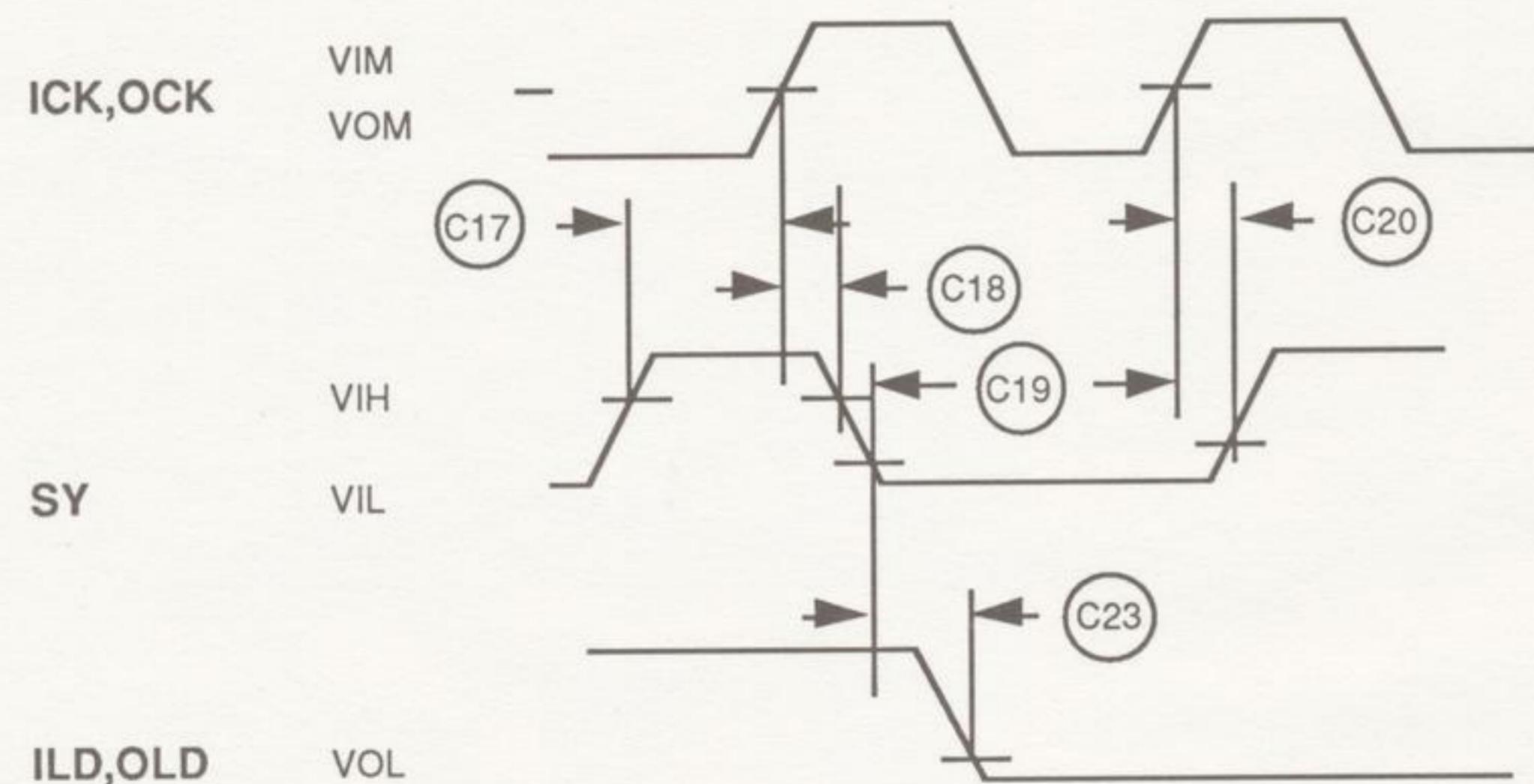
c. external SY. internal ILD/OLD
external or internal ICK/OCK

Figure 12-7 ac Serial Clock Generator Timing

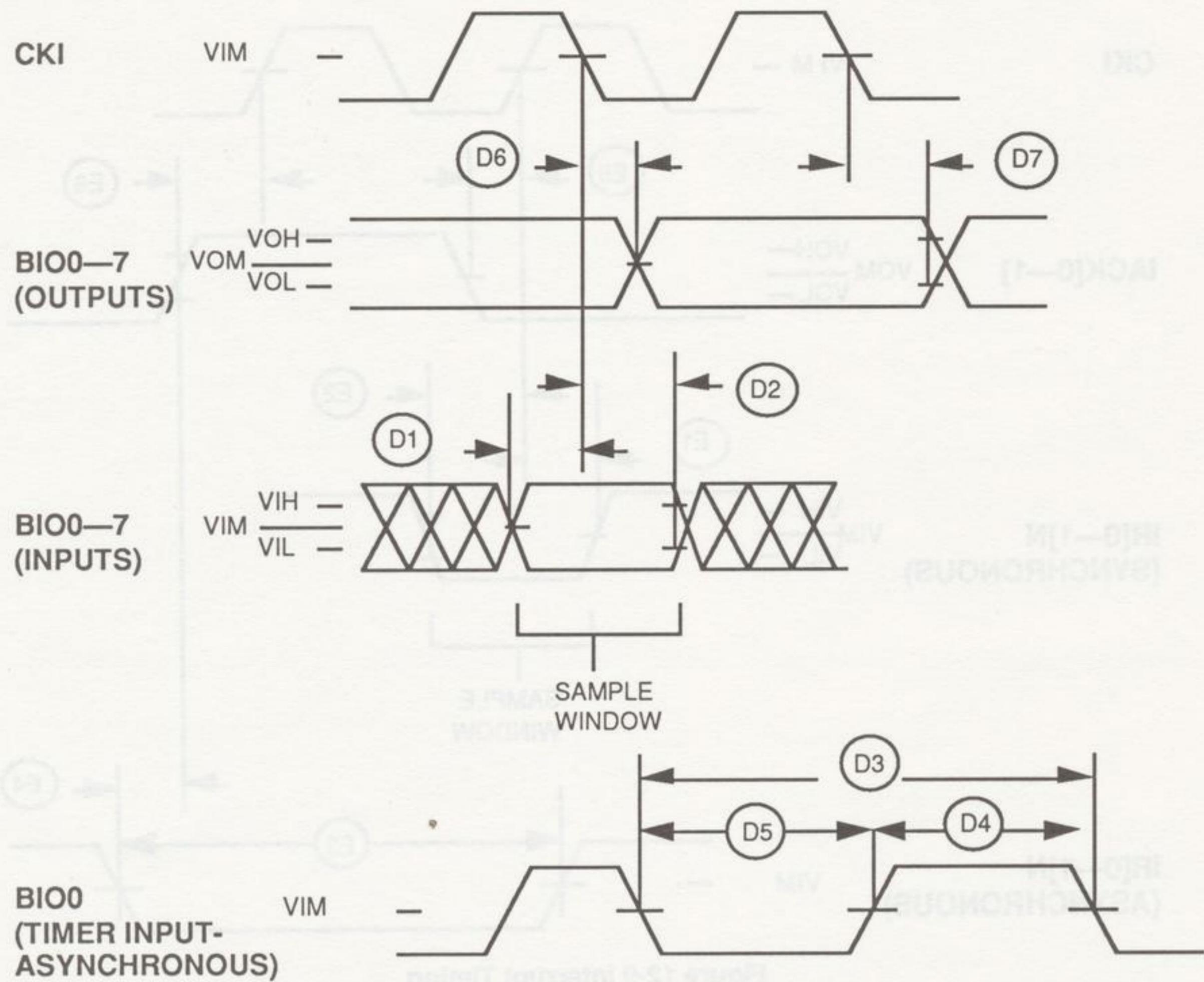


Figure 12-8 Bit I/O Timing

Table 12-13 Timing Requirements for Bit I/O (See Figure 12-8)

Num	Symbol	Description	Min	Max	Unit
D1	tBIOVCKIL	BIO Setup Time	4	—	ns
D2	tCKILBIOX	BIO Hold Time	2	—	ns
D3	tBIO0HBIO0H	Timer Clock Period	$2T + 10$	—	ns
D4	tBIO0HBIO0L	Timer Clock High Time	$T + 5$	—	ns
D5	tBIO0LBIO0H	Timer Clock Low Time	$T + 5$	—	ns

Table 12-14 Timing Characteristics for Bit I/O (See Figures 12-8)

Num	Symbol	Description	Min	Max	Unit
D6	tCKILBIOV	BIO Delay	—	16	ns
D7	tCKILBIOX	BIO Hold	4	—	ns

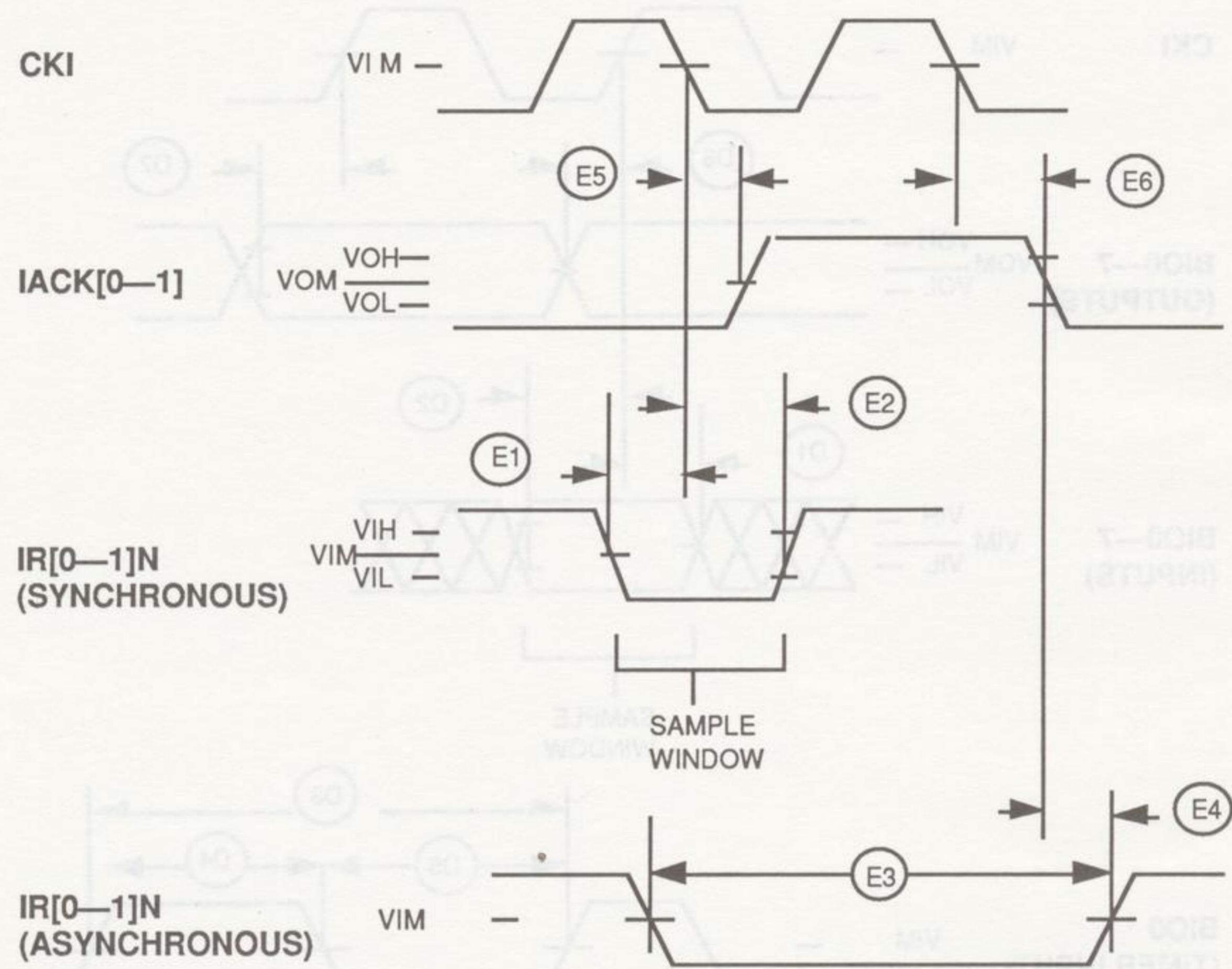


Figure 12-9 Interrupt Timing

Table 12-15 Timing Requirements for Interrupts (See Figure 12-9)

Num	Symbol	Description	Min	Max	Unit
E1	tIRLCKIL	Interrupt Asserted Setup Time (Synchronous)	4	—	ns
E2	tCKILIRX	Interrupt Asserted Hold Time (Synchronous)	2	—	ns
E3	tIRLIRH	Interrupt Asserted Pulse Width (Asynchronous)	T + 5	—	ns
E4	tIACKHIRH	Interrupt Acknowledge to Interrupt Negation	—	2T	ns

Table 12-16 Timing Characteristics for Interrupts (See Figure 12-9)

Num	Symbol	Description	Min	Max	Unit
E5	tCKILIACKL	Interrupt Acknowledge Delay	—	16	ns
E6	tCKILIACKX	Interrupt Acknowledge Hold	4	—	ns

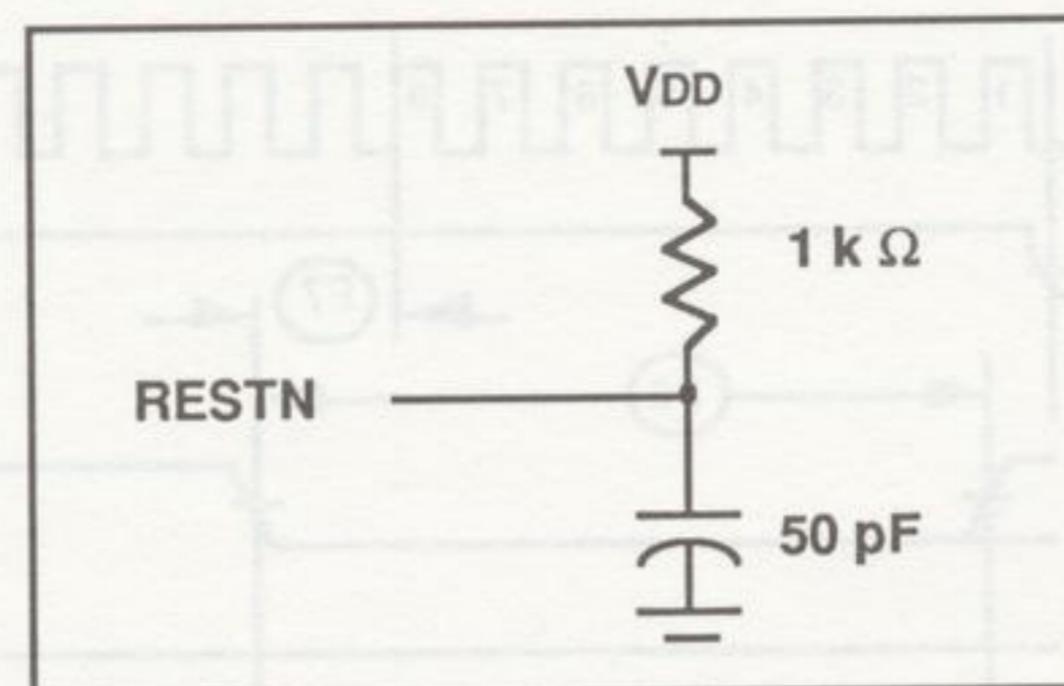


Figure 12-10 RESTN Test Load Circuit

Table 12-17 Timing Requirements for Reset (See Figures 12-10 to 12-12)

Num	Symbol	Description	Min	Max	Unit
F1	tBIOVRESTH	BIO Setup to RESTN High*	8	—	ns
F2	tRESTHBIOX	BIO Hold After RESTN High	—	0	ns
F3	tRESTHZNH	ZN High After RESTN High	—	8T†	ns
F4	tRESTLRESTH	RESTN In Pulse Width	8T + 10	—	ns
F5	tRESTLRESTH	RESTN In Pulse Width	8T + 10	—	ns

* Only BIO[4:7] are latched into the device when RESTN makes a zero-to-one transition.

† ZN may be asserted at any time. This maximum specification permits correct DSP3210 operation in the run mode.

Table 12-18 Timing Characteristics for Reset and ZN (See Figures 12-10 to 12-12)

Num	Symbol	Description	Min	Max	Unit
F6	tRESTPU	Power-on RESTN Output Pulse Width	7T - 10	7T + 60	ns
F7	tCKILRESTV	Power-on RESTN Output Delay	—	60	ns
F8	tRESTLBIOZ	Power-on RESTN Low to BIO High-Z (Inputs)	—	9	ns
F9	tRESTLBISZ	Power-on RESTN Low to Bus Interface Signals High-Z*	—	9	ns
F10	tRESTHBISE	RESTN High to Bus Interface Signals Low-Z	—	12T + 12	ns
F11	tRESTLSOBZ	Power-on RESTN Low to Output and Biput Signals High-Z†	—	9	ns
F12	tRESTLSOBE	Power-on RESTN Low to Output and Biput Signals Low-Z	—	8T + 12	ns
F13	tZNLSOBZ	ZN Low to Output and Biput Signals High-Z	—	18	ns
F14	tZNHSOBE	ZN High to Output and Biput Signals Low-Z	—	18	ns
F15	tRESTILBIOZ	RESTN In Low to BIO High-Z (Inputs)	—	17	ns
F16	tRESTILBISZ	RESTN In Low to Bus Interface Signals High-Z	—	4T + 12	ns

* Bus Interface Signals are defined to be A2—A31, MS0—MS3, CSN, ASN, RW, PBD, MRN, MWN, and LOCKN.

† Outputs and Biputs are defined to be BRN, BGACKN, BIO[0—7], ICK, ILD, DO, OCK, OLD, SY, and IACK[0—1].

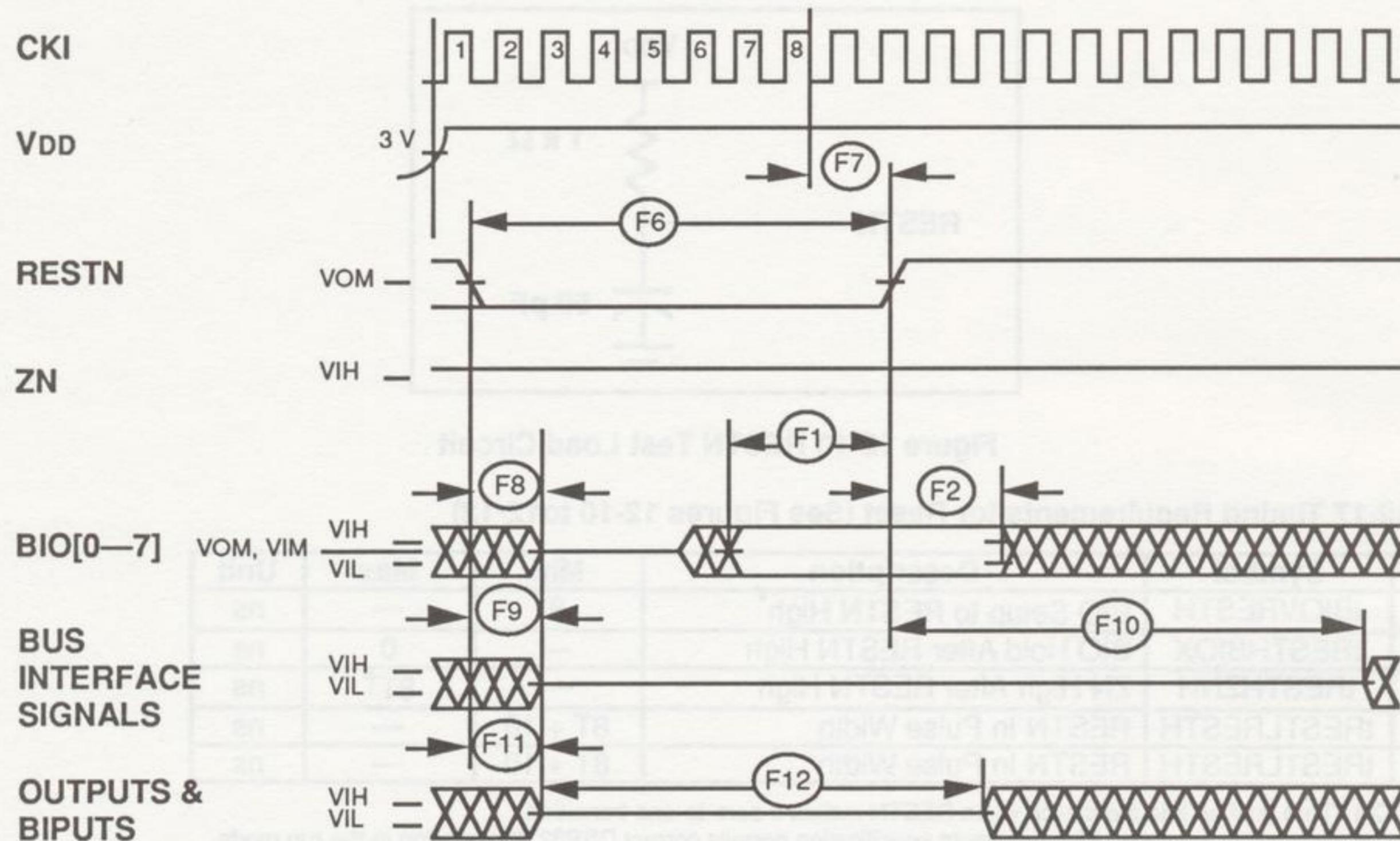


Figure 12-11 Power-on Reset Timing

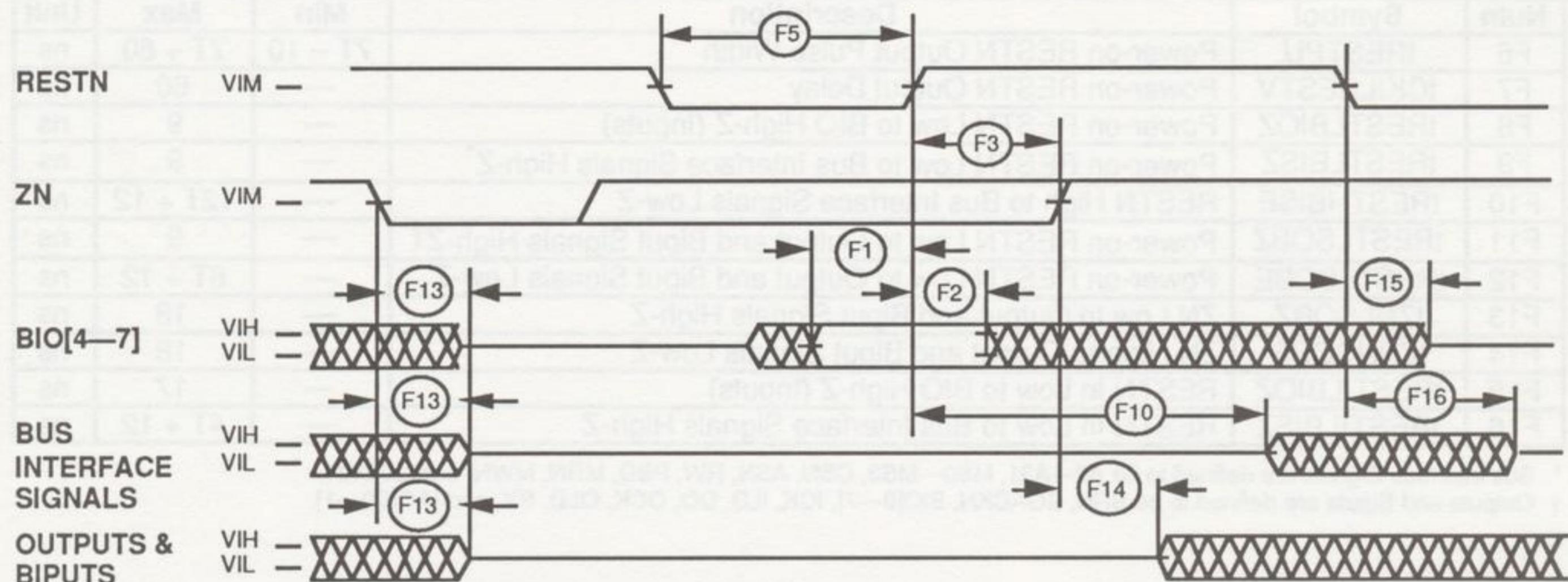


Figure 12-12 Externally Controlled Reset and ZN Timing

Appendix A

APPENDIX A

BOOT ROM CODE	A-1
Table A-1 Operation of Boot ROM Routines	A-1
Figure A-1 EPROM Data Organization	A-2
Listing A-1 Boot ROM Code	A-2

BOOT ROM CODE

Program execution always begins with the instruction at location 0x0. This physical address is either in Boot ROM or external memory depending on the state of pcw[10], C/PN, when the DSP3210 is reset. Note that pcw[10—13] are initialized during the reset state with the logic states applied to bio[7—4], respectively. If C/PN is initialized to a one, execution begins from the first location in the Boot ROM. If C/PN is initialized to a zero, execution begins from location zero of external memory A.

When Computer mode is selected, the Boot ROM code is run on reset. The Boot ROM program uses pcw[13], BRC, to select between two routines stored in the ROM. Table A-1 lists a summary of the operations performed by each routine. The routine selected when pcw[13] = 0 is used to redirect the starting address of the DSP3210. The routine selected when pcw[13] = 1 is used to load a program from a external 8-bit wide memory, such as an EPROM, and execute it. The EPROM must be 8-bits wide and be mapped to external memory address 0x60000000. Figure A-1 shows the organization of data in the byte-wide EPROM when using little endian byte ordering.

A listing of the assembly code is provided in Listing A-1. Note that the fill code at the end of the ROM is for future expansion and should not be used.

Table A-1 Operation of Boot ROM Routines

pcw[13]	Operations
0	<ul style="list-style-type: none"> (1) Enables interrupt 1. (2) Enters wait-for-interrupt mode, and when interrupt 1 is acknowledged*. (3) Changes memory map to Processor mode. (4) Disables interrupt 1. (5) Reads location 0 (external memory) for branch vector and writes back a zero to location 0. (6) Returns from interrupt by loading pcsh with branch vector so that the DSP3210 starts executing from the branch vector.
1	<ul style="list-style-type: none"> (1) Read four bytes, organized as the least significant byte of the first four word addresses, from external memory starting at 0x60000000 into a 32-bit integer (define this as the count). (2) Read the next four bytes, organized as the least significant byte of the first four word addresses, from external memory starting at 0x60000010 into a 32-bit pointer (define this as the address). (2) If count is zero, branch to address. (3) If count is non-zero, read count number of bytes from external memory starting at 0x60000020 and write them to address to form words and then branch to address.

- * For the code to operate correctly, the chip must enter the wait-for-interrupt mode before taking the interrupt. Note that the emr register enables interrupt 1 prior to the waiti instruction. If an interrupt is asserted between the enabling of interrupt 1 and the waiti instruction, the interrupt will be taken with the wrong memory map. The time from RESTN making a low-to-high transition to the program reaching the waiti instruction is $64 * T$, where T is a CKI period.

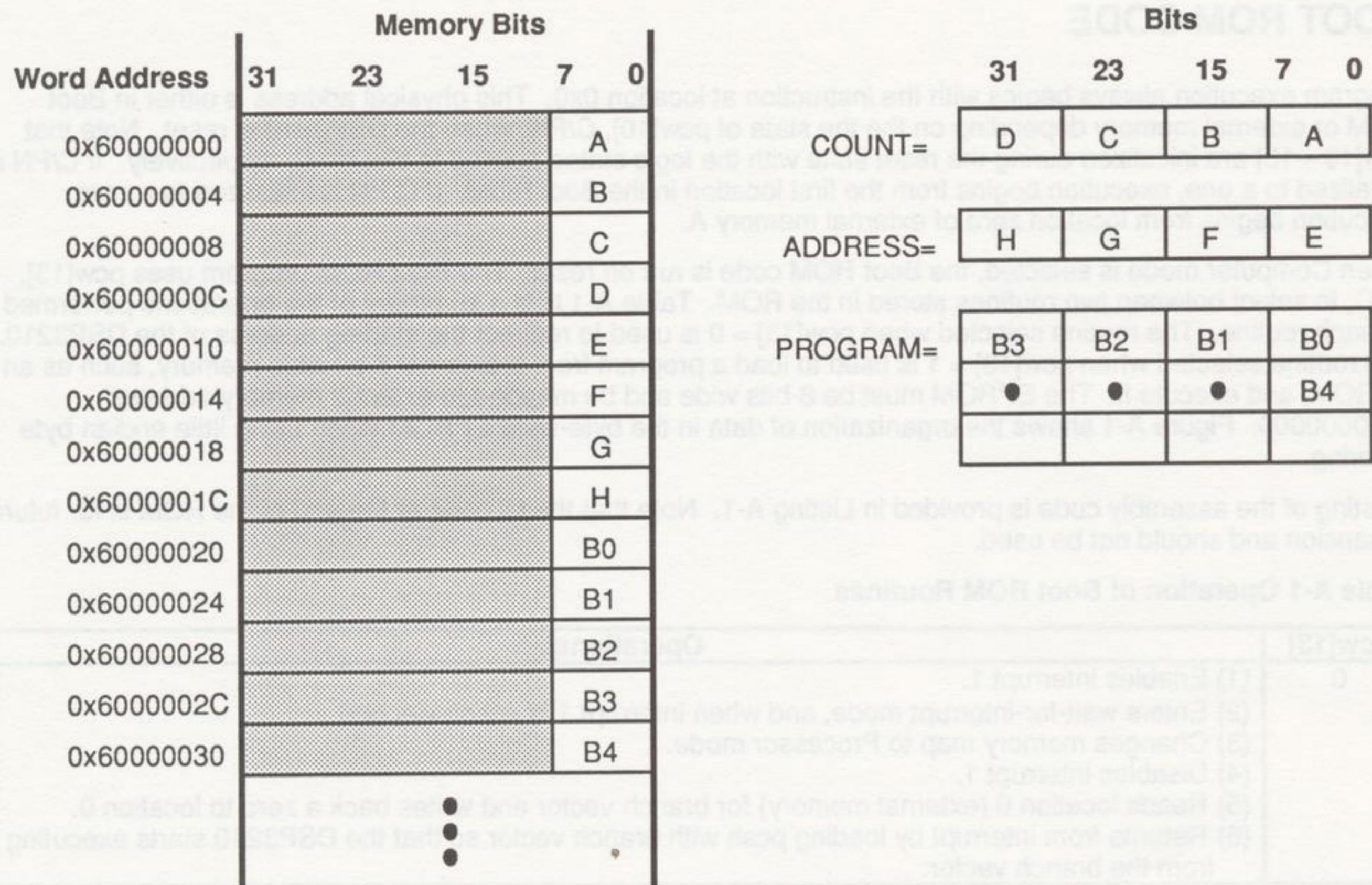


Figure A-1 EPROM Data Organization (Little Endian Byte Ordering)

Listing A-1 Boot ROM Code

```
/*
 * DSP3210 Boot ROM
 */


```

This code is mask programmed into the BOOT ROM of the DSP3210.

SYNOPSIS:

The DSP3210 is reset via the RESTN pin and comes up in Computer mode by setting PCW bit 10 (C/PN) to 1 via the BIO7 pin. In addition, PCW bit 13 is set to either a 0 or 1 via the BIO4 pin. PCW bit 13 is used to determine which boot procedure to execute.

PCW Bit 13 = 0 Procedure:

The DSP3210 sets up r22 to point to 0x5003000 which is the address of the BOOT ROM in Processor mode. Next, the EMR register is set to enable External Interrupt 1. The DSP3210 then sets bit 10 of the PCW register to 0 without changing the other bits in PCW. Finally, the DSP3210 goes into Wait for Interrupt Mode with its memory map set for Processor mode.

When the system host decides to start the DSP3210, it places a vector to the DSP3210 external memory boot procedure into physical location zero. The system host then pulses IREQ1 pin (External Interrupt 1 Request) on the DSP3210 and begins polling physical location zero.

The DSP3210 acknowledges the interrupt via the IACK1 pin and vectors to location 0x50030078 which is in the BOOT ROM. The DSP3210 then clears the EMR register to prevent any further interrupts. Next, it loads the PCSH, pc shadow, register from location zero (which is now in external memory).

The DSP3210 then writes a zero into location zero. Finally, the DSP3210 performs a return from interrupt which executes a NOP from the Shadow Instruction register followed by the instruction which was fetched from the vector supplied by the host in physical location zero.

PCW Bit 13 = 1 Procedure:

The DSP3210 fetches 8 words starting from external memory 0x60000000. The least significant byte (LSB) of the first four words make up the address where the DSP3210 will branch to upon completing the boot procedure.

The LSB of the next four words contain the number of bytes which are to be copied from the location following these eight words into the memory range specified by the starting address.

Upon completion of the copy operation, the DSP3210 transfers program control to the starting address. Note that the memory map remains in the computer mode.

```
/*
 *      I/O Registers Defines
 */

#define      ps      ior00
#define      emr     ior08
#define      spc      ior10
#define      pcw      ior12
#define      dauc     ior14

/*
 *      PSEUDO Instructions
 */

#define      waiti    spc = r0
#define      bkpt     spc = (short) r0
#define      reset     spc = (byte) r0

.rsect ".brom", TEXT

/*
 *      3210 Exception Vector Table
 */

pcgoto boot_begin      /* Reset */
r1 = (short) pcw
pcgoto boot_error       /* Bus Error */
nop
pcgoto boot_error       /* Illegal Opcode */
nop
pcgoto boot_error       /* Reserved */
nop
pcgoto boot_error       /* Address Error */
nop
pcgoto boot_error       /* DAU Overflow/Underflow */
nop
pcgoto boot_error       /* NAN */
nop
pcgoto boot_error       /* Reserved */
nop
pcgoto boot_error       /* External Interrupt 0 */
nop
pcgoto boot_error       /* Timer */
nop
pcgoto boot_error       /* Reserved */
```

```

    nop          /* SIO Input Buffer */
    pcgoto boot_error      /* SIO Output Buffer */
    nop          /* SIO DMA Input Frame */
    nop          /* SIO DMA Output Frame */
    pcsh = (long) *r0      /* External Interrupt 1 */
    emr = (short) r0
    ireturn
    nop

boot_begin:
    r2 = r0 <<| 0x6000
    r1 & 0x2000
    if(eq) pcgoto system_boot
    r3 = (ushort24) 0xE000
    do 7 {
        r4 = *r2++
        nop
        *r3++ = (byte) r4
    }
    r5 = *0xE004 /* fetch number of bytes */
    r1 = *0xE000 /* fetch start address */
    if(eq) pcgoto boot_end /* check number of bytes */
    r3 = r1
    r5 = r5 - 1
    do r5 {
        r4 = *r2++
        nop
        *r3++ = (byte) r4
    }
boot_end:
    goto r1 + 0
    nop

system_boot:
    r22 = r0 <<| 0x5003
    r2 = (ushort24) 0x8000
    emr = (short) r2
    r1 = r1 & (~0x0400)
    waiti
    pcw = r1
    *r0 = r0

boot_error:
    bkpt /* signal error */
    pcgoto .
    nop

/* Fill remaining locations of the Boot ROM with their address */

    fitbits (. - boot_rom + 0x50030000)
    fitbits (. - boot_rom + 0x50030000)
    fitbits (. - boot_rom + 0x50030000)

    .
    .

```

Glossary

2's Complement Integer - A method used in some systems to represent positive and negative integers. Positive integers are identical to standard binary numbers; however, negative integers are the complement of a standard binary number plus one.

3-state - To place an output in the high-impedance state.

A-law - A European standard for the compression and expansion of the dynamic range of a signal.

Addressing Modes - Various common modes for addressing in the DSP3210 include immediate, memory direct, register direct, and register indirect.

ALU - Arithmetic logic unit

Arithmetic Logic Unit (ALU) - On-chip unit that performs arithmetic operations.

Assembler - A program that translates symbolically represented characters into a form (binary) the computer can interpret.

Bit I/O (BIO) - Input or output pins used for status and control.

Boot ROM - Preprogrammed Read-Only Memory that contains instructions that initialize operation of the DSP3210.

Bus Interface - A general-purpose parallel data port that can be used for interfacing to microprocessor buses, I/O buses, memory, or memory-mapped devices.

Byte - An 8-bit quantity that may appear at any address in memory.

CA - Control arithmetic.

CAU - Control arithmetic unit.

CISC - Complex Instruction Set Computer.

Companding - The process of compressing and expanding a signal.

Control Arithmetic (CA) Instructions - Instructions executed in the CAU that perform address generation, integer data arithmetic and logic functions, instruction flow control, and data movement.

Control Arithmetic Unit (CAU) - Execution unit that performs 16- or 32-bit, integer arithmetic for logic and control functions.

DA - Data arithmetic.

Data Arithmetic (DA) Instructions - 32-bit floating-point instructions that perform multiply/accumulate operations for signal-processing algorithms. DA instructions also contain special functions for

performing data type and format conversions and rounding.

Data Arithmetic Unit (DAU) - Primary execution unit that performs 32-bit floating-point arithmetic for signal-processing functions.

Data Arithmetic Unit Control (DAUC) Register - A register that controls the type of conversions performed in the DAU on input and output data and controls rounding modes.

DAU - Data arithmetic unit.

DAUC - Data arithmetic unit control.

Direct Memory Access (DMA) - High-speed data transfer operation where an I/O channel transfers information directly to or from memory.

DMA - Direct memory access.

DMAC - Direct Memory Access Controller

EMR - Exception mask register.

Exception Vector Table - Sixteen pairs of 32-bit words that control the program flow based on the source of an exception.

Exception Vector Table Pointer (EVTP) - A register that locates the starting address of the exception vector table.

Fast Fourier Transform (FFT) - A complex procedure for transforming a time-domain waveform into its frequency-domain components.

FFT - Fast Fourier transform.

Floating-Point Arithmetic - A method of arithmetic in the computer that keeps track of the binary point.

Frame Boundary - The first time the output buffer is full following a high-to-low transition on the SY pin, provided IOC[15] is equal to zero at that time. Frame boundary is generated by the on-chip clock generator and is useful for certain TDM interfaces.

Halfword - A 16-bit quantity that may appear at any address in memory.

I/O - Input/output.

I/O Control (IOC) Register - A register used to configure the serial I/O interface to external devices. It is used to set various I/O configurations, bit lengths, internal or external clock, and internal or external synchronization.

IBUF - Input buffer.

Immediate Mode - An addressing mode in which the operand is supplied by the instruction.

Indexed Mode - An addressing mode in which the address part of the instruction is modified by an auxiliary (index) register during the execution of that instruction. This mode is achieved with the instruction $rD = rS + N$ followed by $*rD$.

Input Buffer (IBUF) - A register used to accept serial input from an external device.

Input Shift Register (ISR) - An input register for converting serial input data to parallel data.

Interrupt - A means by which external devices may request service by the microprocessor.

IOC - Input/output control.

ISR - Input shift register.

Link Editor - Software support tool used for maintaining libraries, defining sections of on-chip and off-chip memory, and recognizing holes in memory.

Memory Direct Mode - An addressing mode in which the instruction contains the address of an operand in memory.

Memory Indirect Mode - An addressing mode in which a memory location contains the address of the data, rather than the data itself. This mode is achieved with the instruction $rD = \text{MEMORY}$ followed by $*rD$.

Memory Mapped I/O (MMIO) - Instruction referencing method for on-chip peripherals.

Multimedia - The processing of multiple forms of data, including sound, speech, data, images, and video.

OBUF - Output buffer.

OSR - Output shift register.

Output Buffer (OBUF) - A register used to pass data to the output shift register.

Output Shift Register (OSR) - A register for converting parallel data from the output buffer into a serial data stream.

PCW - Processor control word.

Pipelining - Overlapping the execution of instructions to increase performance.

Processor Status (PS) Register - Register that displays flags for the CAU, DAU, and I/O.

Register Direct Mode - An addressing mode in which the instruction specifies a register that contains the operand.

Register Indirect Mode - An addressing mode in which the instruction contains the name of a pointer register (rP) that contains the address of the operand.

Register Mapped I/O (IO) - Instruction referencing method for DSP3210 core control registers.

Relative Mode - An addressing mode in which the absolute address is obtained by means of address modification. Address modification is performed by the addition of a given number to the address part of an instruction known as the relative address. This mode is attained by moving the program counter (pc) to another CAU register and then performing a register indirect operation. In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest eight bits plus one.

RISC - Reduced Instruction Set Computer.

Serial I/O (SIO) - A group of registers that allows interfacing with other devices using few, if any, external chips. It converts serial input data and parallel output data into serial data.

Simulator - A highly specific program that allows accurate simulations of the logical operation of the DSP3210 device.

SIO - Serial input/output.

Stack - An area of reserved memory used for storing the program counter and the contents of registers during a program interrupt.

Time-Division Multiplexed (TDM) - A procedure for transmitting two or more signals over a common channel through the use of successive time intervals for different devices.

Timer - Programmable counter.

TSC - Timer/Status and Control

Word - A 32-bit quantity that may appear at any address in memory.

μ -law - A United States standard for compressing and expanding the dynamic range of a signal.

μ P - Microprocessor.

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CA Arithmetic/Logic Instructions		
Instruction*	CAU Flag	Instr. Ref.
rD = [(short)] rS3+N	nzvc	ADD
rD = (long) rS << N	nz00	SHIFT-OR
rD = [(short)] rD - N	nzvc	SUBTRACT
rD = [(short)] N - rD	nzvc	SUBTRACT
rD = [(short)] rD & N	nz00	ADD
rD = [(short)] rD N	nz00	OR
rD = [(short)] rD ^ N	nz00	EXCLUSIVE OR
rD = [(short)] rD # N	nz0c	ADD-CARRY REV
rD = [(short)] rD << N	nz00	SHIFT LEFT
rD = [(short)] rD >> N	nz00	SHIFT RIGHT
rD = [(short)] rD \$>> N	nz00	SHIFT RIGHT-ARITH
[(short)] rD - N	nzvc	COMPARE
[(short)] rD & N	nz00	BIT TEST
[if(COND)] rD = [(short)] rS1 + rS2	nzvc	ADD
[if(COND)] rD = [(short)] rS1 - rS2	nzvc	SUBTRACT
[if(COND)] rD = [(short)] rS1 & rS2	nz00	ADD
[if(COND)] rD = [(short)] rS1 &~ rS2	nz00	AND-COMPLEMENT
[if(COND)] rD = [(short)] rS1 rS2	nz00	OR
[if(COND)] rD = [(short)] rS1 ^ rS2	nz00	EXCLUSIVE OR
[if(COND)] rD = [(short)] rS1 # rS2	nz0c	ADD-CARRY REV
[if(COND)] rD = [(short)] rS1 << rS2	nz00	SHIFT LEFT
[if(COND)] rD = [(short)] rS1 >> rS2	nz00	SHIFT RIGHT
[if(COND)] rD = [(short)] rS1 \$>> rS2	nz00	SHIFT RIGHT-ARITH
[if(COND)] [(short)] rS1 - rS2	nzvc	COMPARE
[if(COND)] [(short)] rS1 & rS2	nz00	BIT TEST
[if(COND)] rD = [(short)] rS/2	nz00	SHIFT RIGHT-ARITH
[if(COND)] rD = [(short)] rS>>1	nz00	SHIFT RIGHT
[if(COND)] rD = [(short)] rS<<1	nz00	SHIFT LEFT
[if(COND)] rD = [(short)] rS*2	nzvc	ADD
[if(COND)] rD = [(short)] rS>>>1	nz0c	ROTATE RIGHT
[if(COND)] rD = [(short)] rS<<<1	nzvc	ROTATE LEFT
[if(COND)] rD = [(short)] -rS	nzvc	SUBTRACT
[if(COND)] rD = [(short)] rS	nzvc	ADD
[if(COND)] rD1 = [(short)] rS {+, -}1	nzvc	INCR/DECR
[if(COND)] sp = (long) sp {++, --}	nzvc	INCR/DECR

- * The size of arithmetic/logic and data move operations can be specified to be long (32-bits), or short (16-bits). Long is the default and does not have to be specified.



AT&T DSP3210 Programmer's Reference Card

Note: {} and [] are not part of the instruction syntax. Parentheses () are part of the syntax and must appear where shown in an instruction. Lower-case letters are part of the syntax and upper-case letters are replaced by immediate data, register names, or expressions.

DA Multiply/Accumulate Instructions		
Instruction	DAU Flag	Instr. Reference
[Z=] aN = [-]aM {+,-}Y*X	NZVU	FMULT-ACC-STORE
aN = [-]aM {+,-}(Z=Y)*X	NZVU	FMULT-ACC-TAP
[Z=] aN = [-]Y {+,-}aM*X	NZVU	FMULT-ADD-STORE
[Z=] aN = [-]Y *X	NZVU	FMULT-STORE
aN = [-] (Z=Y)*X	NZVU	FMULT-TAP
[Z=] aN = [-]Y {+,-} X	NZVU	FMULT-STORE
[Z=] aN = [-]Y	NZVU	FLOAD-STORE
aN = [-] (Z=Y) {+,-} X	NZVU	FADD-TAP

Replacement for DA Multiply/Accumulate Instructions	
Replace	Value
aN, aM	a0-a3
X, Y	*{r1-r14}, *{r1-r14}++, *{r1-r14}--, *{r1-r14}++{r15-r19}, a0-a3
Z	*{r1-r14}, *{r1-r14}++, *{r1-r14}--, *{r1-r14}++{r15-r19}

DA Special Function Instructions		
Instruction	DAU Flag	Instr. Reference
[Z=] aN = ic(Y)	NZ00	IC
[Z=] aN = oc(Y)	—	OC
[Z=] aN = float16(Y)	NZ00	FLOAT16
[Z=] aN = float32(Y)	NZ00	FLOAT32
[Z=] aN = int16(Y)	—	INT16
[Z=] aN = int32(Y)	—	INT32
[Z=] aN = round(Y)	NZVU	ROUND
[Z=] aN = ifalt(Y)	—	IFALT
[Z=] aN = ifaeq(Y)	—	IFAEQ
[Z=] aN = ifagt(Y)	—	IFAGT
[Z=] aN = dsp(Y)	NZVU	DSP
[Z=] aN = ieee(Y)	—	IEEE
[Z=] aN = seed(Y)	NZ0U	SEED

Restriction 1 - Z-pointer may only be used as Z-pointer in the following instruction.

Restriction 2 - CAU or IO register store cannot follow a DA instruction with a Y field memory reference.

Restriction 3 - CAU register loads cannot be referenced in the following instruction.

Replacement for DA Special Function Instructions	
Replace	Value
aN	a0-a3
Y	*{r1-r14}, *{r1-r14}++, *{r1-r14}--, *{r1-r14}++{r15-r19}, a0-a3 (Y may not be a0—a3 for <i>dsp</i> function.)
Z	*{r1-r14}, *{r1-r14}++, *{r1-r14}--, *{r1-r14}++{r15-r19}

CA Control Instructions		
Instruction	CAU Flag	Instr. Reference
if (COND) goto {N, rB, rB+N}*	—	GOTO-COND
if (rM-->=0) goto {N, rB, rB+N}*	—	GOTO-LOOP
goto {N, rB, rB+N, M, rB+M}*	—	GOTO
nop	—	NOP
call {N, rB, rB+N, M} (rM)*	—	CALL
return (rM)	—	RETURN
{do,dolock} K, {L, rM}	—	DO
doblock {L, rM}	—	DO
ireturn	—	IRETURN
sfrst	—	SFRST
waiti	—	WAITI

*When using pc as rB, goto and call instructions may be written with the syntax *pcgoto label* or *pccall label*, respectively. The linker computes the appropriate N value to encode.

Replacement for CA Control Instructions	
Replace	Value
rB	pc, r0—r22
rM	r1—r22
N	16-bit signed integer
M	24-bit unsigned integer
COND	One of the DSP3210 Condition Codes

(COND) - Conditions					
CAU	Flag	DAU	Flag	IO	Flag
false	NA	ane	Z=0	ibe	ibf=0
true	NA	aeq	Z=1	ibf	ibf=1
pl	n=0	age	N=0	obe	obe=1
mi	n=1	alt	N=1	obf	obe=0
ne	z=0	avc	V=0	syc	sy=0
eq	z=1	avs	V=1	sys	sy=1
vc	v=0	auc	U=0	fbc	fb=0
vs	v=1	aus	U=1	fb	fb=1
cc	c=0	agt	N Z=0	ir0s	ir0n=1
cs	c=1	ale	N Z=1	ir0c	ir0n=0
ge	n^v=0			ir1s	ir1n=1
lt	n^v=1			ir1c	ir1n=0
gt	z (n^v)=0				
le	z (n^v)=1				
hi	c z=0				
ls	c z=1				

Replacement for CA Arithmetic/Logic Instructions	
Replace	Value
rD	r0—r22
rD1	r0—r20, r22
rS, rS1, rS2	r0—r22
rS3	r0—r22, pc, pcsh
N	16-bit signed integer
COND	One of the DSP3210 Condition Codes

CA Data Move Group Instructions		
Instruction**	CAU Flag	Instr. Ref.
rD= (short) N	nz00	SET
rD= (ushort24) M	—	SET24
{MEM, *L, iorD} = {(byte),(hbyte),(short),(long)} rS	—	STORE
rD = {(char),(byte),(hbyte)} {MEM,*L}	nz00	LOAD
rD = {(short),(ushort)} {MEM,*L}	nz00	LOAD
rD = (long) {MEM, *L}	nz00	LOAD
rD = {(char),(byte),(hbyte)} iorS	nz00	LOAD
rD = {(short),(ushort)} iorS	nz00	LOAD
rD = (long) iorS	nz00	LOAD
MEM = {(byte),(short),(long)} iorS	—	STORE -IOR
iorD = {(byte),(short),(long)} MEM	—	LOAD-IOR

** The size of data move operations can be specified to be long (32-bits), short (16-bits), or byte (8-bits). Long is the default and does not have to be specified.

Replacement for CA Data Move Instructions	
Replace	Value
rS	r0—r22, pc, pcsh
rD	r0—r22
MEM	*{r0-r22}, *{r0-r22}++, *{r0-r22}--, *{r0-r22}++{r0-r22}
iorS, iorD	ior{0, 8, 10, 12, 14, 15}
N	16-bit number
L	16-bit number (unsigned)
M	24-bit number (unsigned)

Latency 1 - DA instruction writes may not be referenced until four instructions later.
 Latency 2 - An accumulator may not be used as a multiplier input until three instructions later.
 Latency 3 - goto, call, and return instructions are delayed by one instruction.
 Latency 4 - DAU conditions are established no sooner than four instructions prior to the test.

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