32MHz, 64-Channel Serial to Parallel Converter with Push-Pull Outputs

Features

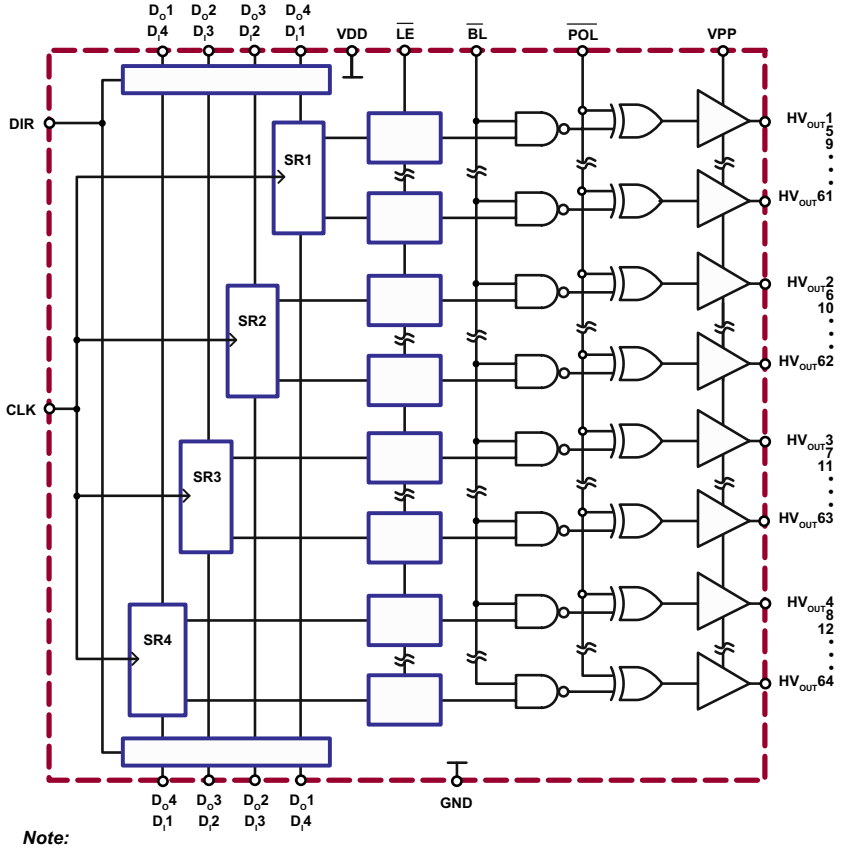
- HVCMOS® technology
- 5.0V CMS Logic
- Output voltage up to +80V
- Low power level shifting
- 32MHz equivalent data rate
- Latched data outputs
- Foreward and reverse shifting options (DIR pin)
- Diode to VPP allows efficient power recovery
- Outputs may be hot switched

General Description

The HV57708 is a low voltage serial to high voltage parallel converter with push-pull outputs. The device has been designed for use as a driver for EL displays. It can also be used in any application requiring multiple output high voltage current sourcing and sinking capability such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

The device has 4 parallel 16-bit registers, permitting data rates 4x the speed of one (they are clocked together). There are also 64 latches and control logic to perform the polarity select and blanking of the outputs. $HV_{OUT}1$ is connected to the first stage of the first shift register through the polarity and blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to GND, and CW shifting when connected to VDD. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register ($HV_{OUT}64$). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift registers to the latches occurs when the $\overline{LE}$ input is high. The data in the latches is stored when the $\overline{LE}$ is low.

Functional Block Diagram



Note:
Each SR (shift register) provides 16 outputs. SR1 supplies every fourth output starting with 1; SR2 supplies every fourth output with 2, etc.

Ordering Information

Part Number	Package Option	Packing
HV57708PG-G	80-Lead PQFP	66/Tray

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

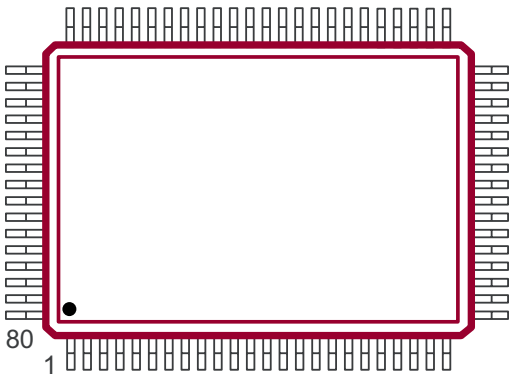
Parameter	Value
Supply voltage, V_{DD}	-0.5V to +7.5V
Output voltage , V_{PP}	-0.5V to +90V
Logic input levels	-0.3V to V_{DD} +0.3V
Ground current[1]	1.5A
Continuous total power dissipation[2]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

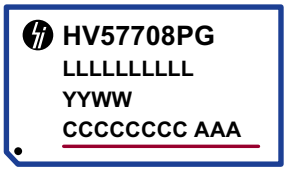
1. *Limited by the total power dissipated in the package.*
2. *For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.*

Pin Configuration



80-Lead PQFP

Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
C = Country of Origin
A = Assembler ID
—— = "Green" Packaging

Package may or may not include the following marks: Si or

80-Lead PQFP

Typical Thermal Resistance

Package	θ_{ja}
80-Lead PQFP	37°C/W

Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	Output voltage	8.0	80	V
V_{IH}	High-level input voltage	V_{DD} -0.5V	-	V
V_{IL}	Low-level input voltage	0	0.5	V
f_{CLK}	Clock frequency per register	-	8.0	MHz
T_A	Operating free-air temperature	-40	+85	°C

Notes:

Power-up sequence should be the following:

1. Apply ground.
2. Apply V_{DD}.
3. Set all inputs (D_{IN}, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.
5. The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics *(Over recommended operating conditions unless otherwise noted)*

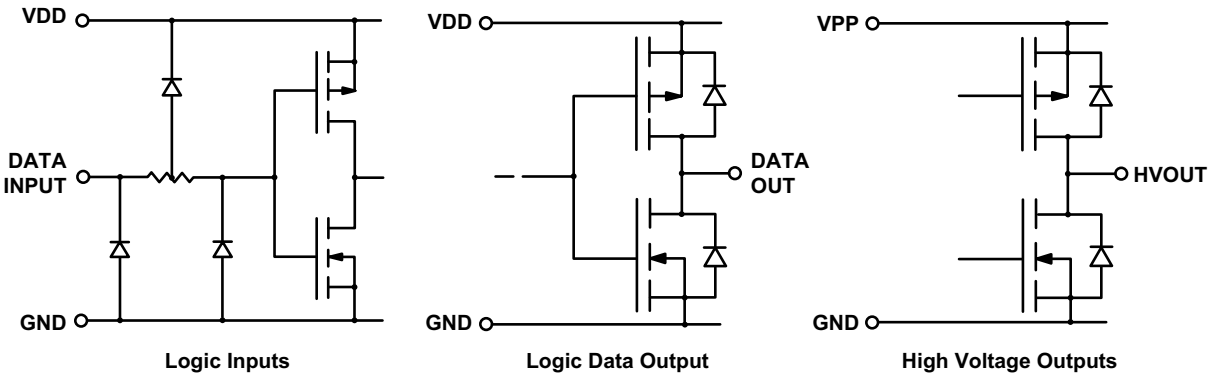
Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	15	mA	$V_{DD} = V_{DD}$ max, f_{CLK} = 8.0MHz
I_{PP}	High voltage supply current		-	100	µA	Outputs high
			-	100	µA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current		-	100	µA	All $V_{IN} = V_{DD}$
V_{OH}	High level output	HV_{OUT}	65	-	V	I_O = -15mA, V_{PP} = +80V
		Data out	V_{DD} -0.5	-	V	I_O = -100µA
V_{OL}	Low level output	HV_{OUT}	-	7.0	V	I_O = 12mA, V_{PP} = +80V
		Data out	-	0.5	V	I_O = 100µA
I_{IH}	High-level logic input current		-	1.0	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		-	-1.0	µA	V_{IL} = 0V
V_{OC}	High voltage clamp diode		-	1.0	V	I_{OC} = 1.0mA

AC Electrical Characteristics *(T_A = 85°C max. Logic signal inputs and Data inputs have t_r, $t_f \leq$ 5ns [10% and 90% points])*

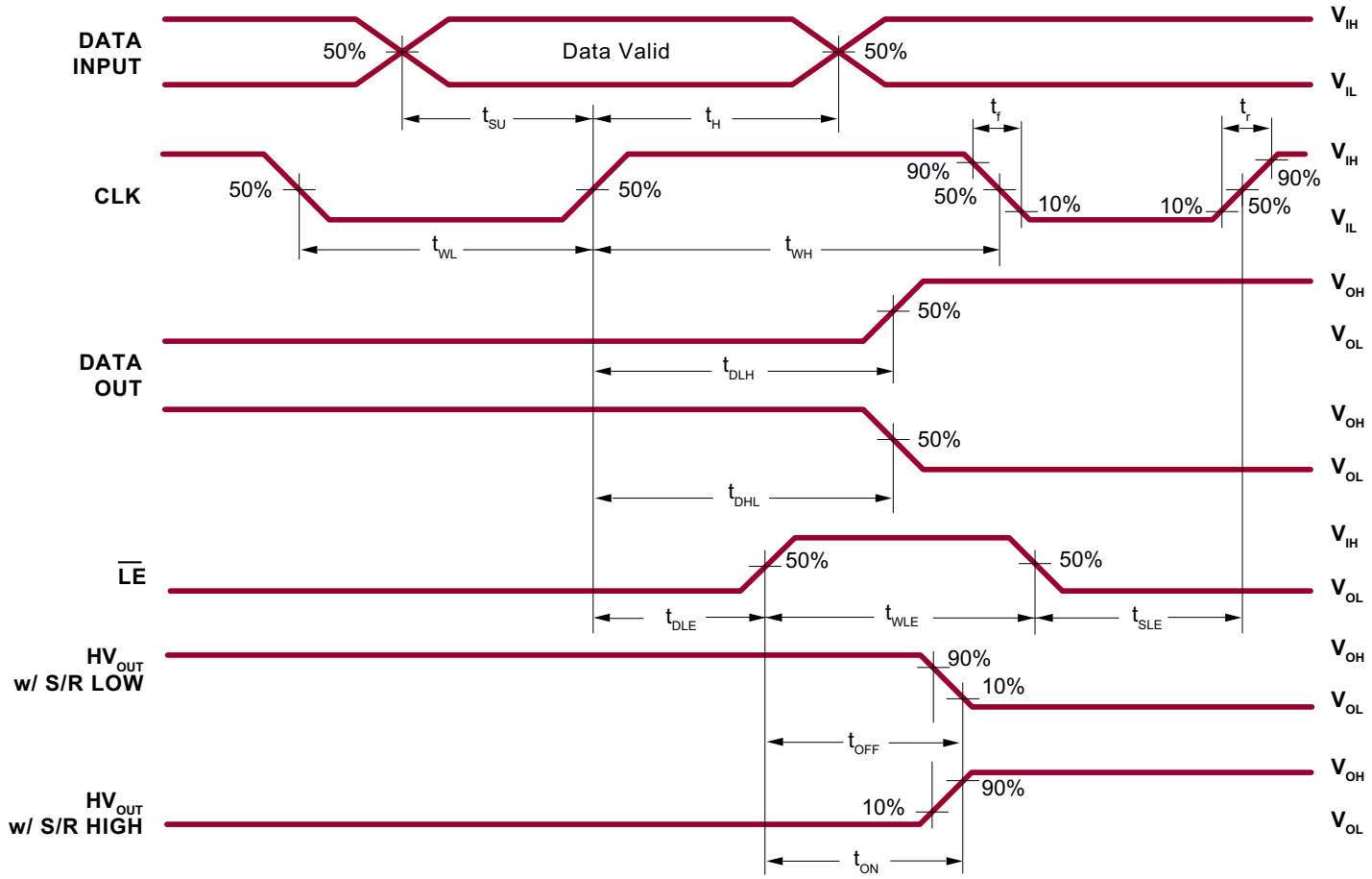
Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	8.0	MHz	Per register
t_{WL}, t_{WH}	Clock width high or low	62	-	ns	---
t_{SU}	Data set-up time before clock rises	10	-	ns	---
t_H	Data hold time after clock rises	15	-	ns	---
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}	-	500	ns	C_L = 15pF
t_{DHL}	Delay time clock to data high to low	-	70	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high	-	70	ns	C_L = 15pF
t_{DLE}*	Delay time clock to $\overline{LE}$ low to high	25	-	ns	---
t_{WLE}	$\overline{LE}$ pulse width	25	-	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock rises	0	-	ns	---

** t_{DLE} is not required but is recommended to produce stable HV outputs and thus minimize power dissipation and current spikes (allows internal SR output to stabilize).*

Input and Output Equivalent Circuits



Switching Waveforms

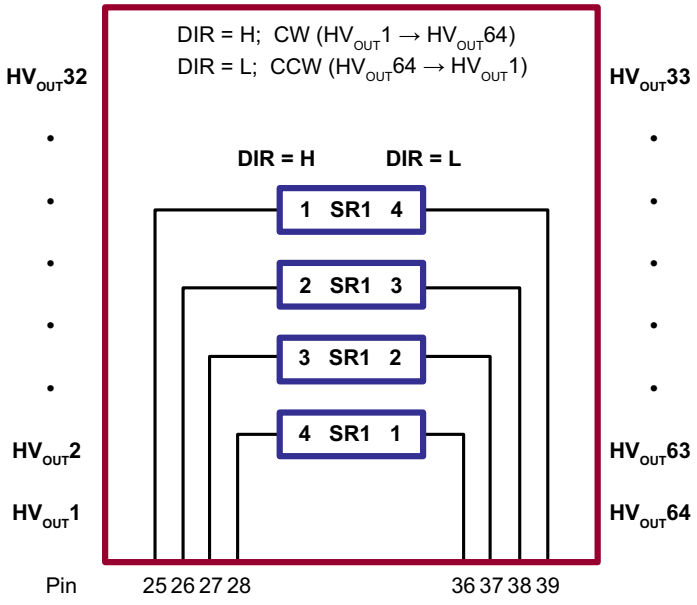


Function Table

Function	Inputs						Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg	HV Outputs	Data Out
All O/P high	X	X	X	L	L	X	-	H	-
All O/P low	X	X	X	L	H	X	-	L	-
O/P normal	X	X	X	H	H	X	-	No inversion	-
O/P inverted	X	X	X	H	L	X	-	Inversion	-
Data falls through (latches transparent)	L	_↑‾	H	H	H	X	L	L	-
	H	_↑‾	H	H	H	X	H	H	-
	L	_↑‾	H	H	L	X	L	H	-
	H	_↑‾	H	H	L	X	H	L	-
Data stored/ latches loaded	X	X	L	H	H	X	*	Stored Data	-
	X	X	L	H	L	X	*	Inversion of stored data	-
I/O relation	$D_{I/O}$1-4A	_↑‾	H	H	H	H	$Q_n \rightarrow Q_{n+1}$	New H or L	$D_{I/O}$1-4B
	$D_{I/O}$1-4A	_↑‾	L	H	H	H	$Q_n \rightarrow Q_{n+1}$	Previous H or L	$D_{I/O}$1-4B
	$D_{I/O}$1-4B	_↑‾	L	H	H	L	$Q_n \rightarrow Q_{n-1}$	Previous H or L	$D_{I/O}$1-4A
	$D_{I/O}$1-4B	_↑‾	H	H	H	L	$Q_n \rightarrow Q_{n-1}$	New H or L	$D_{I/O}$1-4A

Note:
** = dependent on previous stage's state. See Pin configuration for DIN and DOUT pin designation for CW and CCW shift.*

Shift Register Operation



Pin Function

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	HV_{OUT}24/41	21	HV_{OUT}4/61	41	HV_{OUT}64/1	61	HV_{OUT}44/21
2	HV_{OUT}23/42	22	HV_{OUT}3/62	42	HV_{OUT}63/2	62	HV_{OUT}43/22
3	HV_{OUT}22/43	23	HV_{OUT}2/63	43	HV_{OUT}62/3	63	HV_{OUT}42/23
4	HV_{OUT}21/44	24	HV_{OUT}1/64	44	HV_{OUT}61/4	64	HV_{OUT}41/24
5	HV_{OUT}20/45	25	D_{IN}1/D_{OUT}4(A)	45	HV_{OUT}60/5	65	HV_{OUT}40/25
6	HV_{OUT}19/46	26	D_{IN}2/D_{OUT}3(A)	46	HV_{OUT}59/6	66	HV_{OUT}39/26
7	HV_{OUT}18/47	27	D_{IN}3/D_{OUT}2(A)	47	HV_{OUT}58/7	67	HV_{OUT}38/27
8	HV_{OUT}17/48	28	D_{IN}4/D_{OUT}1(A)	48	HV_{OUT}57/8	68	HV_{OUT}37/28
9	HV_{OUT}16/49	29	$\overline{LE}$	49	HV_{OUT}56/9	69	HV_{OUT}36/29
10	HV_{OUT}15/50	30	CLK	50	HV_{OUT}55/10	70	HV_{OUT}35/30
11	HV_{OUT}14/51	31	$\overline{BL}$	51	HV_{OUT}54/11	71	HV_{OUT}34/31
12	HV_{OUT}13/52	32	VDD	52	HV_{OUT}53/12	72	HV_{OUT}33/32
13	HV_{OUT}12/53	33	DIR	53	HV_{OUT}52/13	73	HV_{OUT}32/33
14	HV_{OUT}11/54	34	GND	54	HV_{OUT}51/14	74	HV_{OUT}31/34
15	HV_{OUT}10/55	35	$\overline{POL}$	55	HV_{OUT}50/15	75	HV_{OUT}30/35
16	HV_{OUT}9/56	36	D_{OUT}4/D_{IN}1(B)	56	HV_{OUT}49/16	76	HV_{OUT}29/36
17	HV_{OUT}8/57	37	D_{OUT}3/D_{IN}2(B)	57	HV_{OUT}48/17	77	HV_{OUT}28/37
18	HV_{OUT}7/58	38	D_{OUT}2/D_{IN}3(B)	58	HV_{OUT}47/18	78	HV_{OUT}27/38
19	HV_{OUT}6/59	39	D_{OUT}1/D_{IN}4(B)	59	HV_{OUT}46/19	79	HV_{OUT}26/39
20	HV_{OUT}5/60	40	VPP	60	HV_{OUT}45/20	80	HV_{OUT}25/40

Note:

Pin designation for DIR = H/L.

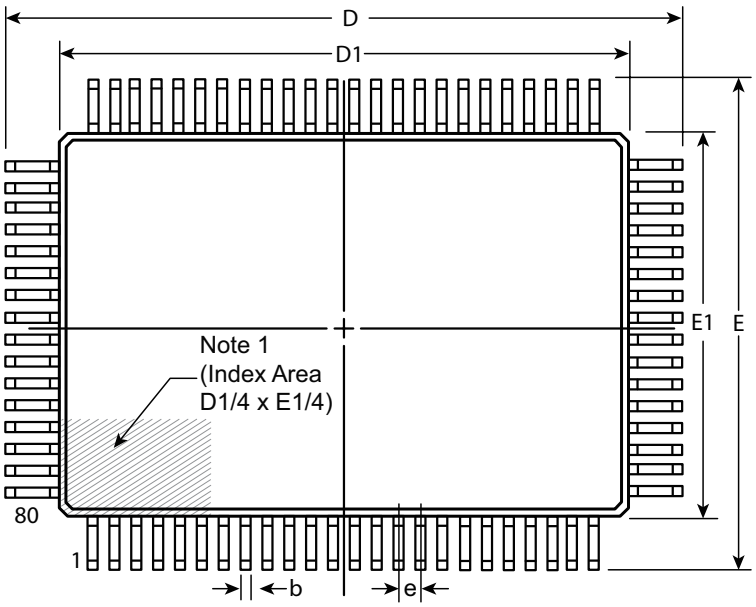
Example: For DIR = H, pin 41 is HV_{OUT}64.

For DIR = L, pin 41 is HV_{OUT}1.

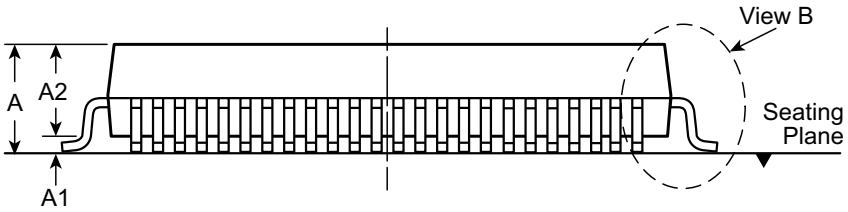
For CW/CCW Shift see function table $Q_N \rightarrow Q_{N+1}$.

80-Lead PQFP Package Outline (PG)

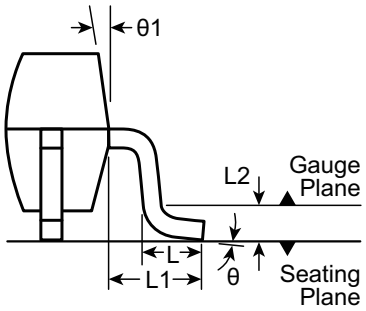
20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Top View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CB-1, Issue B, Sept.1995.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
***Supertex Doc. #:** DSPD-80PQFPPG, Version C041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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