



EDDP User Manual

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Introduction

Refer to <https://wiki.trenz-electronic.de/display/PD/EDDP+User+Manual> for online version of this manual and additional technical documentation of the product.

Electronic Drive Development Platform (EDDP) provides all necessary software and hardware components for development and evaluation of motor control applications. While these components (both software and hardware) can also be used separately, this manual describes EDDP usage with default reference hardware platform (EDDP Kit) only.



Hardware components/boards delivered in EDDP Kit are not intended to be used in final products. All software and hardware parts of the EDDP are intended for developers evaluating Motor Control Applications with Xilinx FPGA and/or SoC devices.

Requirements for Functional Test

It is possible to run the default control firmware and GUI to verify the that the hardware is functional.

Following items are required in addition to EDDP Kit:

- Micro-USB Cable for the USB console of the Controller Board.
- Ethernet-based LAN with a DHCP server.
- RJ45 ethernet Cable.
- Computer with web browser to access the Web UI.
- Card reader supporting micro-SD Cards.
- Access to internet (to download SD Card images).



In order to pass EMC radiated emission (EN 55011) class B requirements option "Spread Spectrum" must be activated (standard setting).



Software version that was used in EMC test: (Visible in the GUI main screen) 2017-7-31 (SVN Tag 5745).

Requirements for Development

Requirements for development with SDSoC:

- All items listed under Requirements for Functional Test.
- Basic knowledge of Xilinx All Programmable FPGA and/or SoC devices, basic knowledge of Xilinx SDK and C/C++ programming in order to be able to adapt the firmware to your requirements.
- A PC capable of running Xilinx SDSoC 2017.1 development environment.
- Valid Xilinx SDSoC license or voucher.

Requirements for development with HLS:

- All items listed under Requirements for Functional Test.
- Basic knowledge of Xilinx All Programmable FPGA and/or SoC devices, basic knowledge of Xilinx SDK and C/C++ programming in order to be able to adapt the firmware to your requirements.
- A PC capable of running Xilinx Vivado 2017.1

Installation



Micro-SD is delivered without Linux images to avoid any issues related to US export control regulations.

Hardware Assembly

When delivered as full EDDP Kit several components are pre-assembled.

Motor Adapter Board

The default (Reference) Motor with Encoder is connected to the Driver Board using special "Adapter Board" (TEC0060). In the EDDP Kit the Motor is pre-assembled:

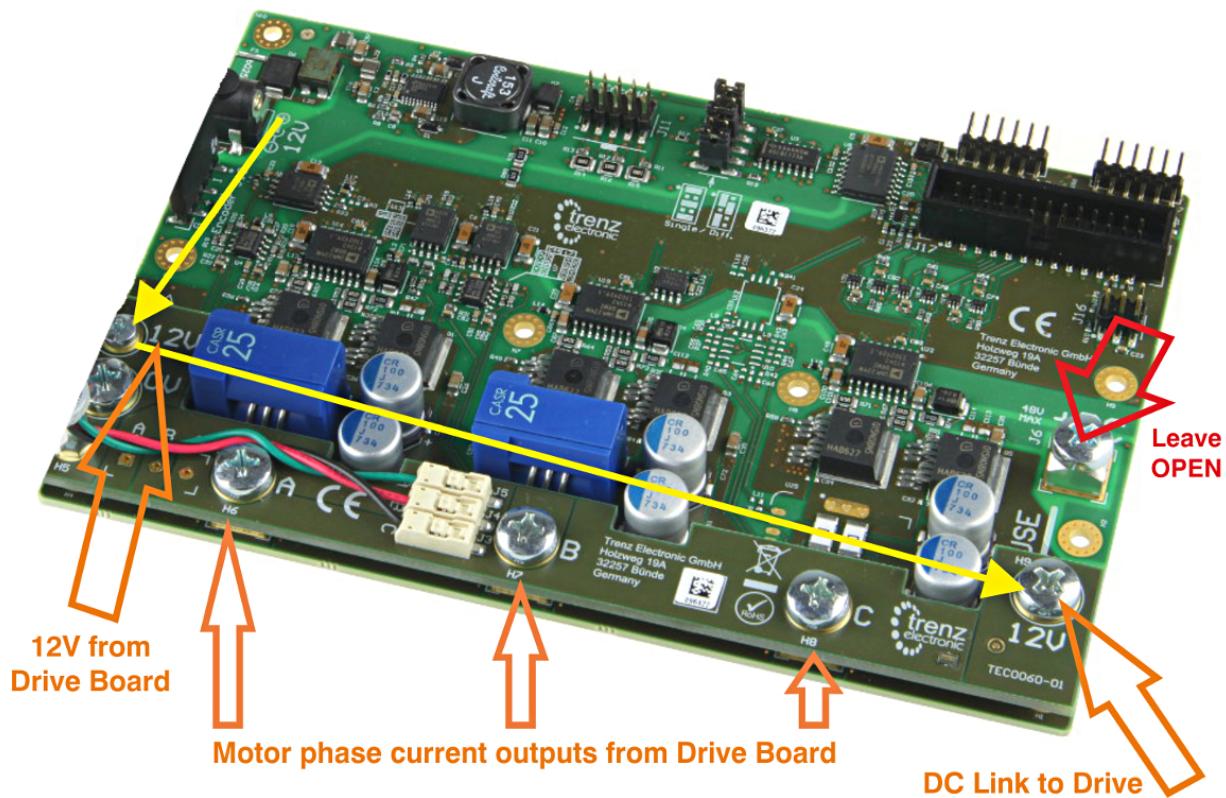


Figure 1: Top view of the EDDP Board.

The Adapter board is mounted to Driver Board using 5 x M6 screws (Labels 0V, A, B, C, 12V on Adapter Board) and with M3 screws and spacer - marked 12V at the left. This Adapter board "forwards" (the yellow arrow) the Drive board pre-driver supply (12V) to the DC Link main terminal on the Drive board, so that separate DC Link power supply is not needed allowing easy evaluation of the complete system.

Note terminal marked+DC must be left open when using the Adapter board!

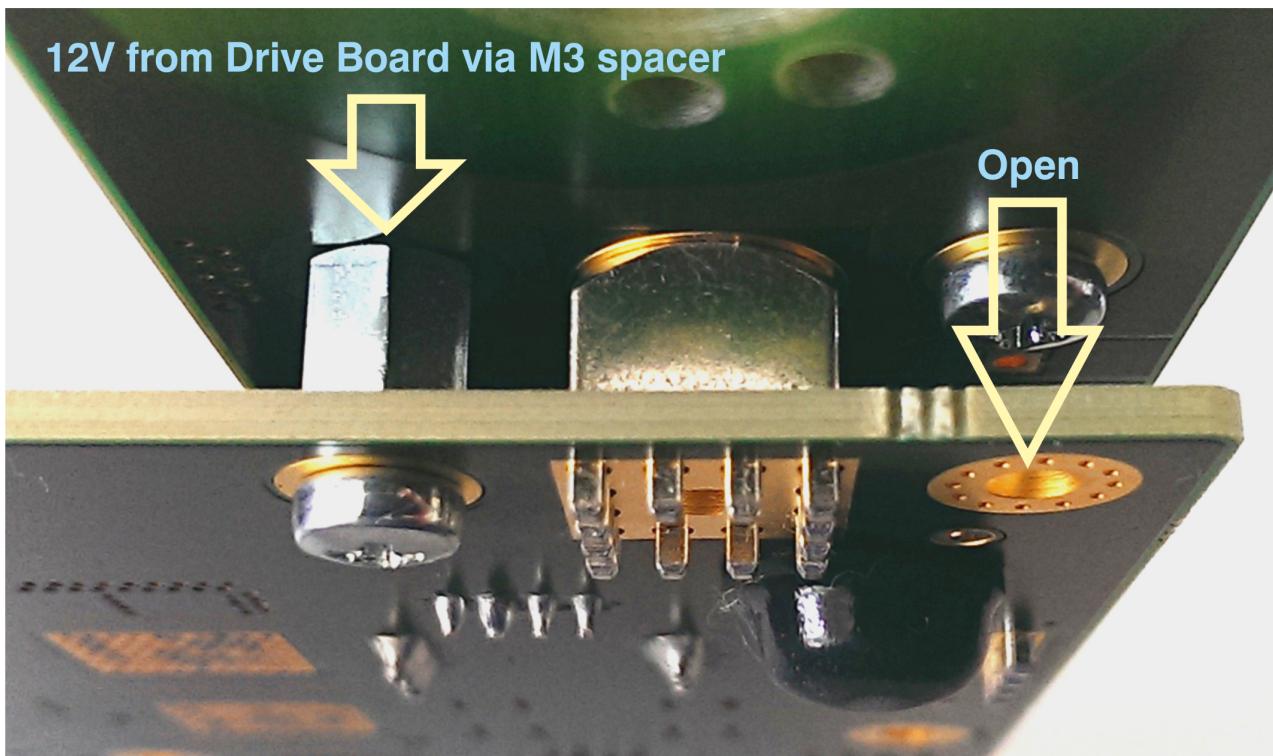


Figure 2: M3 spacer and two M3 screws connect 12V from Drive board to Adapter board.

Motor Connection

When delivered as full EDDP Kit the reference Motor wires are already connected to Adapter board.
Instructions for manual assembly below:

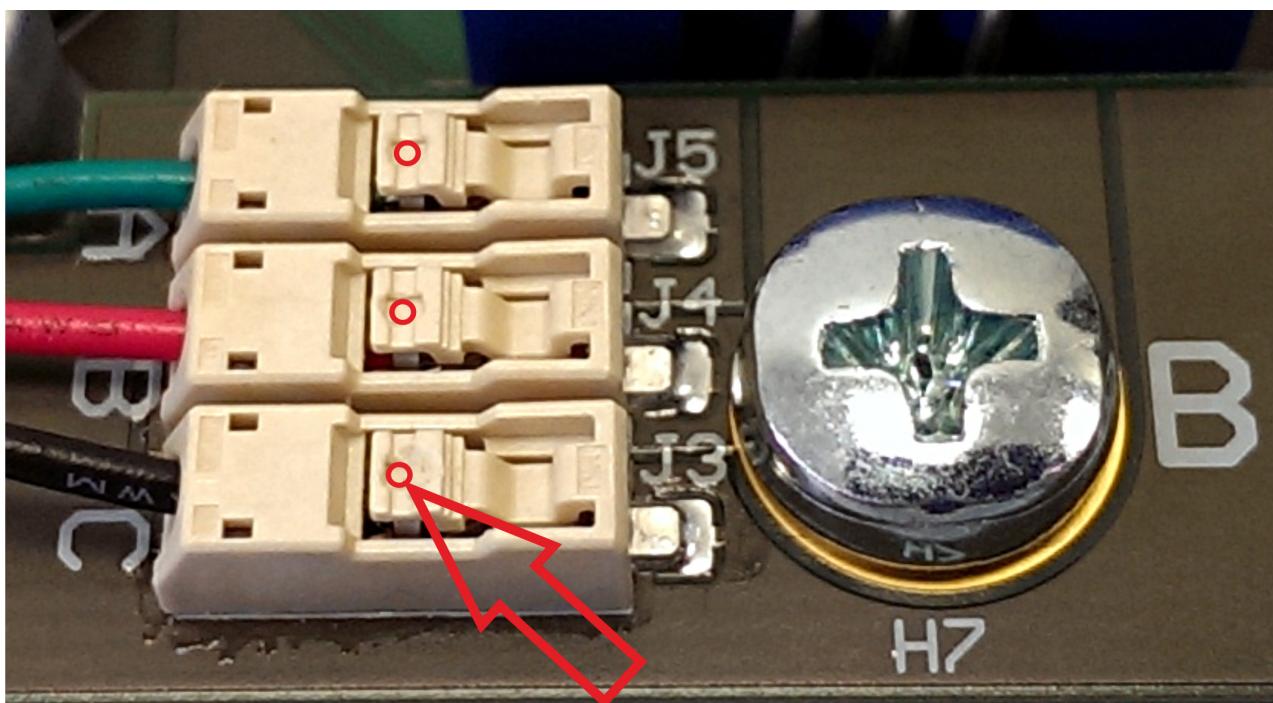


Figure 3: Red dots and arrow mark the place where wire terminal can be released for insertion or removal.

Use a ball-point pen or similar tool to apply gentle force at the dot. Please do not try to remove the wires by pulling them out! Do not apply force in any other region of the white plastic except as marked, it is easy to damage the plastic.

Encoder Connection

One 6-pin Pmod cable is included with the EDDP Kit. It is already assembled between encoder and Drive Board. Instructions for manual assembly are below:

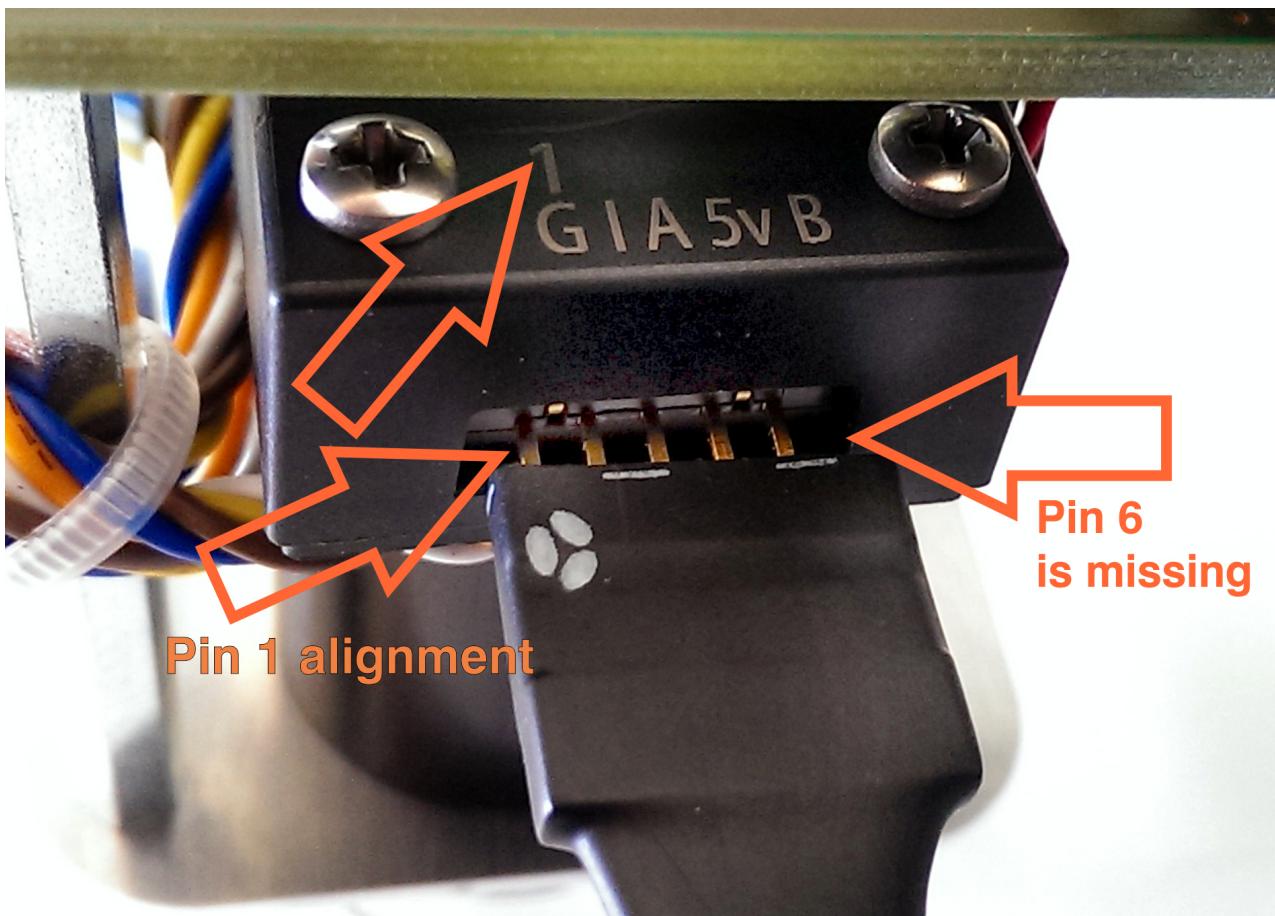


Figure 4: Pmod cable alignment to Encoder connector.

Notice that there are 5 pins in Encoder header while PMoD female connector has 6 terminals. Red Arrow marks the "empty" terminal at PMoD Cable.

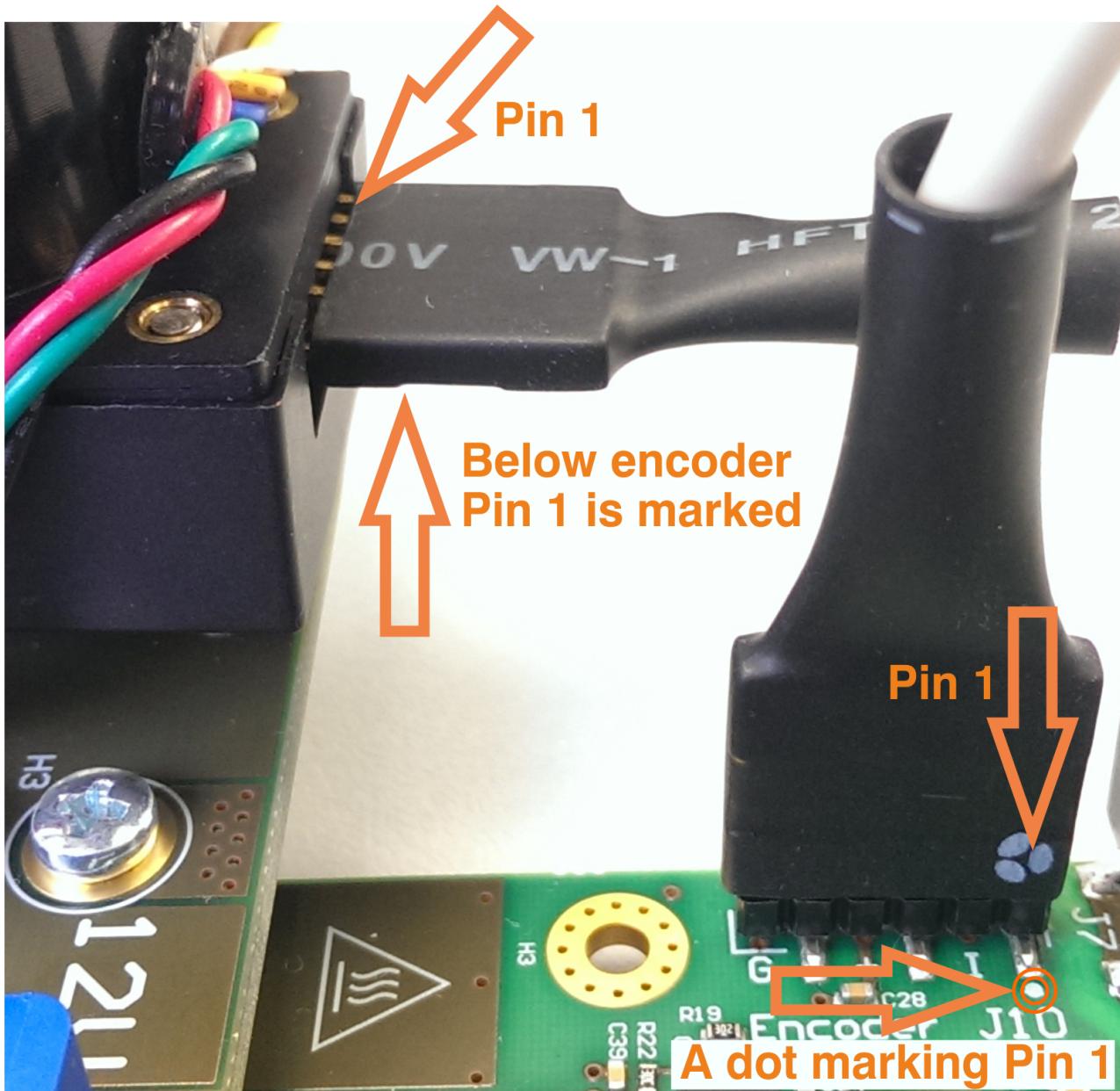


Figure 5: Pmod cable installation.

Pin 1 markings are indicated with the arrows, on the Drive Board a white dot marks 6-pin Pmod header pin 1. This pin should be aligned to Encoder Pin marked "G" and "1" visible when looking from the bottom up. Please note that Encoder header has 5 terminals while the driver board and Pmod cable have 6 terminals.

EDDP System Components

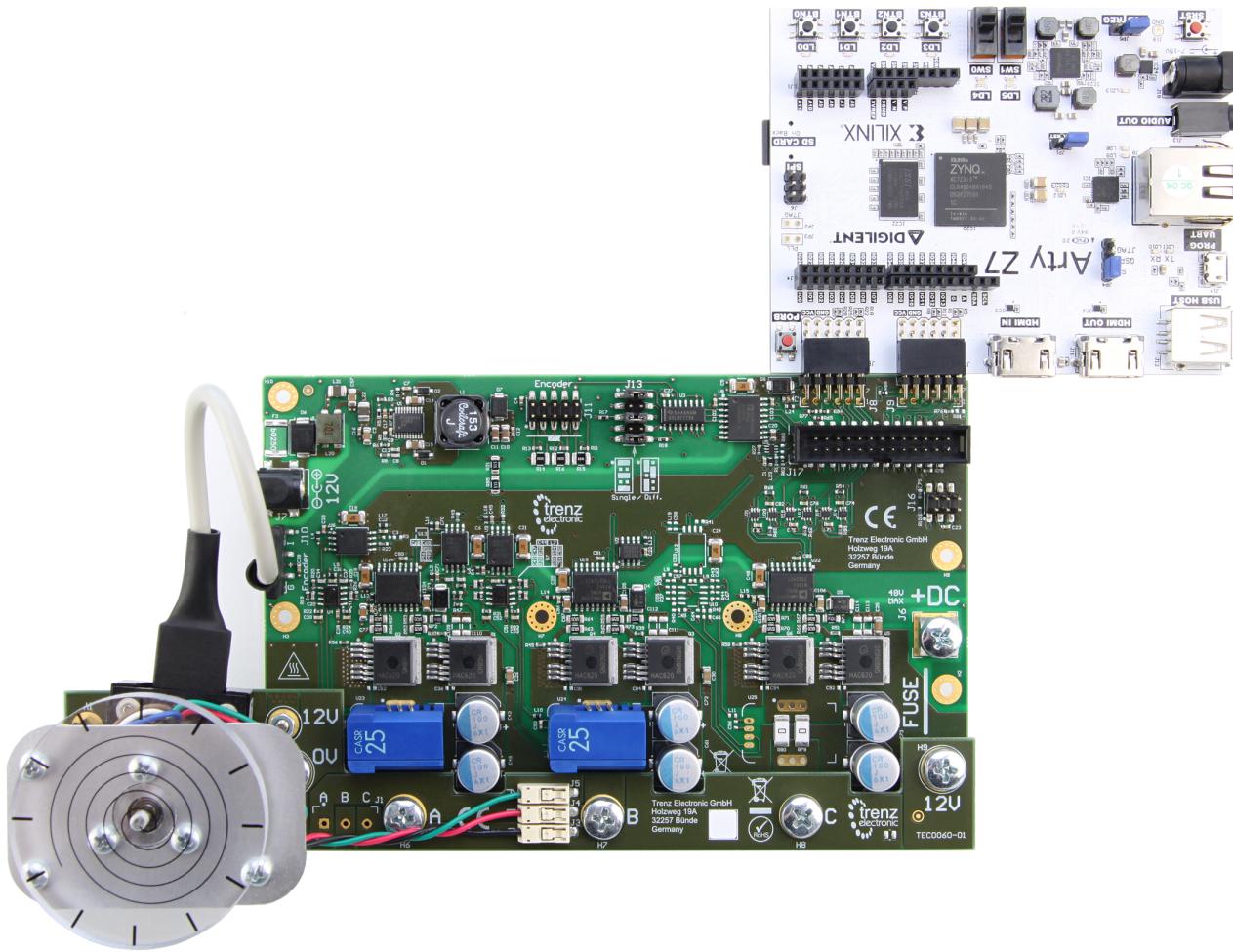


Figure 6: EDDP Kit assembly.

EDDP Kit Content

1. Control Board: ARTY-Z-7010
2. EDPS Driver Board: TEC0053
3. EDPS Motor Adapter Board: TEC0060
4. EDPS Reference Motor with Encoder: BLRW-111D-24V-10000-1000-SI
5. Plastic DEMO load for Motor
6. One 6 Pin PMoD cable
7. Two 12V Power Supplies
8. Screws and other accessories used to mount the motor
9. One spare M6 Screw
10. Plastic cover for Driver Board use without TEC0060
11. 30A Fuse for Driver Board use without TEC0060
12. Micro SD Card
13. Quickstart Guide



The Motor is pre-mounted to the Driver board using the Adapter Board and accessories.

Control Board

The default Control Board is the Digilent [ARTY-Z 7010](#), which is delivered as part of the EDDP Kit. This manual contains information relevant to the actual use of the ARTY-Z as a Control Board within the EDDP only; all technical data and user guides and manuals for the Controller Board are provided by the controller board manufacturer ([Digilent Inc.](#)). Use of the other Control boards with the EDPS Driver board is also outside the scope of this manual. Primary support for other control boards is currently provided by [QDESYS](#).

Software

The software delivered on the SD card configures the FPGA on the ARTY-Z board with the Field-Oriented Control algorithm and starts the web server to serve the Web User Interface (Web UI).

To access the EDDP Web UI, enter IP address of the Controller Board to the web browser address field. The following page appears:



Figure 7: EDDP web UI.

To start the motor, click the button "Motor". The motor will make 3 rotations in order to make sure that encoder finds the initial position before starting in correct mode and the button will turn red. To stop the motor, click the button "Motor" again; the button will turn green.

The gauges show the stator current I_q and the motor speed in RPM.

To see the charts live, enable checkbox "Live charts". The following charts are available:

- I_a, I_b - shows stator currents I_a, I_b , the calculated current I_c and motor speed.
- I_d, I_q - shows stator currents I_d, I_q and motor speed.
- V_d, V_q - shows stator voltages V_d and V_q .

The radio buttons "Current" and "Speed" permit switching the control modes.

The sliders permit selecting the target speed and target current when in the appropriate mode. The direction radio buttons "Forward" and "Reverse" will be changed accordingly when the sign of the value is changed.

The radio buttons "Forward" and "Reverse" can be used to change the direction; the target slider will be changed accordingly.

Motor/Encoder

The default motor is supplied in the EDDP Kit; see the chapter Reference Motor for details. Use of custom motors is outside the scope of this manual.

Functional description

A 3-phase permanent-magnet synchronous motor with attached encoder and mechanical load is mounted to a EDPS Driver Board TEC0053 by using an Adapter Board TEC0060. The Driver Board is connected to a Control Board ARTY-Z7 through PMOD connectors. A Host PC running a Web Browser connects to the Control Board through a Network. On the Driver Board, the 3-phase power stage drives the motor according to the PWM signal. The current transducers on the Driver Board transform the phase currents on 2 (optionally 3) phases into voltages, which, along with the DC Link voltage, are converted by ADC-s into a delta-sigma bitstream. The encoder signals and the sigma-delta bitstream are passed through the galvanic isolation to the Control Board. The PWM signal and ADC clock from the Control Board are passed through the galvanic isolation as well. On the Control Board, the FPGA configuration is determined with the SDSoc Application built on top of the SDSoc Hardware Platform and the ARM Cortex-A9 CPU is running the Embedded Linux Code. The SDSoc Hardware Platform provides a stream-oriented interface of the underlying hardware to the FOC algorithm. The streams are as follows:

1. The data stream to the FOC algorithm consists of the concatenated stream of rotor angle and motor speeds and the stream of discrete ADC samples.
2. The stream of PWM duty cycles from the FOC algorithm, which are converted to the PWM signals for the power stage.
3. The stream of monitor data from the FOC algorithm, which is captured and written to the DMA buffer in the main memory. This monitor data stream can consist either of phase current data, stator current data or stator voltage data.

The SDSoc Application provides the FOC algorithm. The FOC algorithm operates on the AXI4 Stream to and from the SDSoc Hardware Platform and provides a set of AXI registers to control and monitor the status of the FOC algorithm. The control registers determine the FOC algorithm operating parameters and the source of the monitor data stream.

The Embedded Linux Code, running on the ARM Cortex-A9 CPU consists of the following:

1. The Linux OS manages the hardware and provides execution environment for the programs to run in, which includes a TCP/IP network stack. The drivers included provide access to the control and status registers of the FOC algorithm and to the DMA buffer of the monitor data stream.
2. The Network API is a server program, which provides an API built on top of Websockets protocol to control and monitor the FOC algorithm and to capture the monitor data stream.
3. The Web Server, which is used to host the Web UI.

The Web UI running in a web browser on the Host PC enables use of the EDDP Kit from anywhere in the network.

Block Diagram

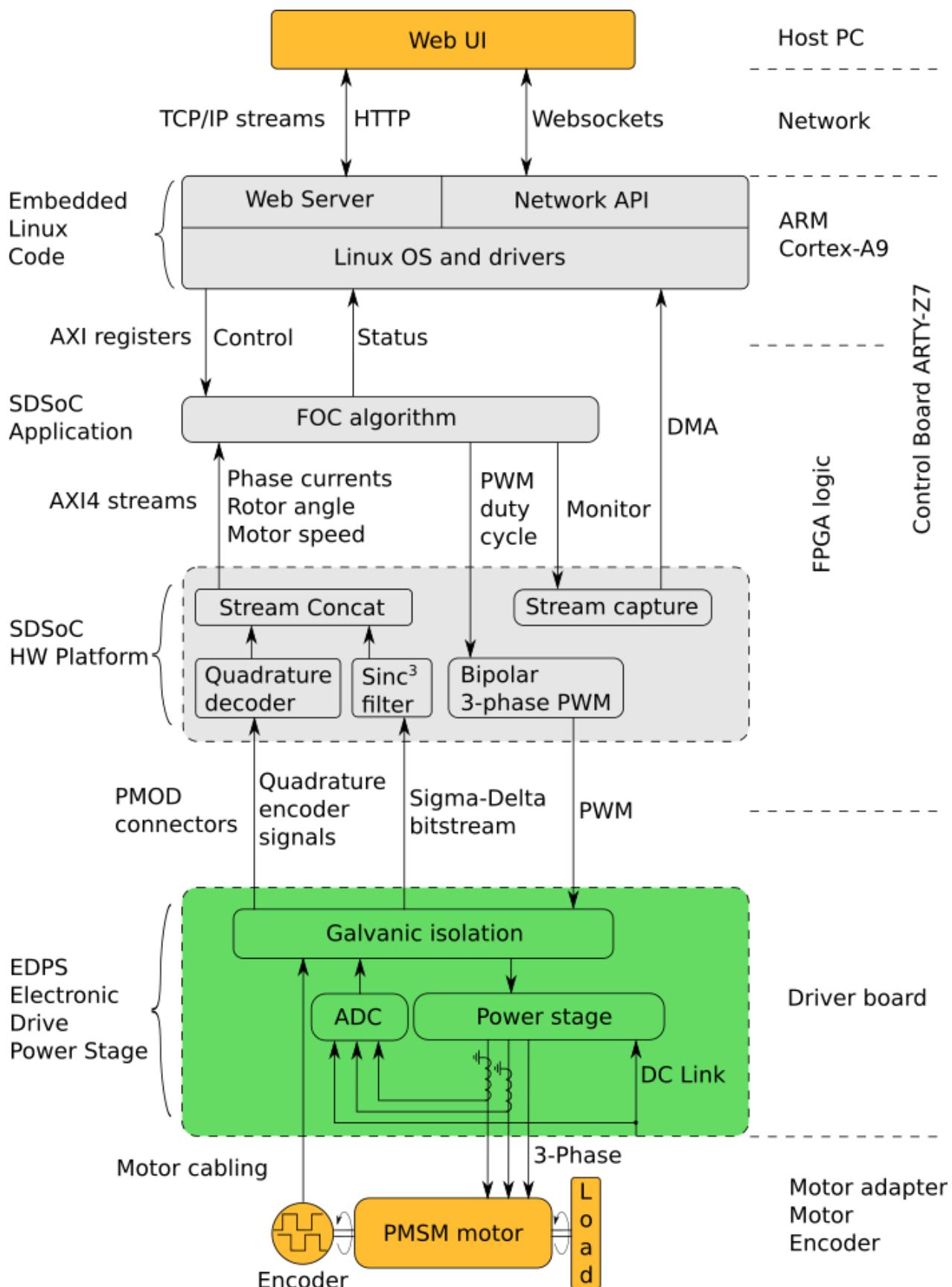


Figure 8: Block diagram of the EDDP.

List of the additional documents

Title	Description
FOC SDSoc	Implementation of a Field-Oriented Control algorithm in C++ with Vivado SDSoc
SDSoC Hardware Platform ARTY-Z7	A basis for building Vivado SDSoc applications running on an Arty-Z7 board connected to a TEC0053 board
AXI4-Stream AD7403	An IP core for filtering the delta-sigma bitstream read from one or more ADC-s of type of AD7403 to an AXI4-Stream of samples
AXI4-Stream Encoder	An IP core for converting impulses from a relative index encoder with an index signal to an AXI4-Stream of position and speed data
AXI4-Stream PWM	An IP core for generating PWM signals according to the input AXI4-Stream
AXI4-Stream Concat	An IP core for concatenating AXI4-Streams
Web GUI	A Web UI to control and monitor an EDPS board over the Network API
Network API	A communication protocol, based on Websockets, to control an EDPS board
Embedded Linux Code	A server program interfacing to an EDPS board and implementing the Network API and the functions of a Web Server

Table 1: List of the additional documents.

References

All resource links for other relevant documents and websites are available from Trenz EDDP Web Hub:

<http://trenz.org/EDDP>

Document Change History

Date	Revision	Contributors	Description
2017-09-21	v.175	Jan Kumann	General formatting changes and small corrections.
2017-08-14	v.10	Antti Lukats, Andrei Errapart	Initial document.

Table 2: Document change history.

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REACH, RoHS and WEEE

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