Abbreviations

C2M = miss&dirty&valid

M2C = (miss&~dirty)|(~valid)

H = hit&valid

CR

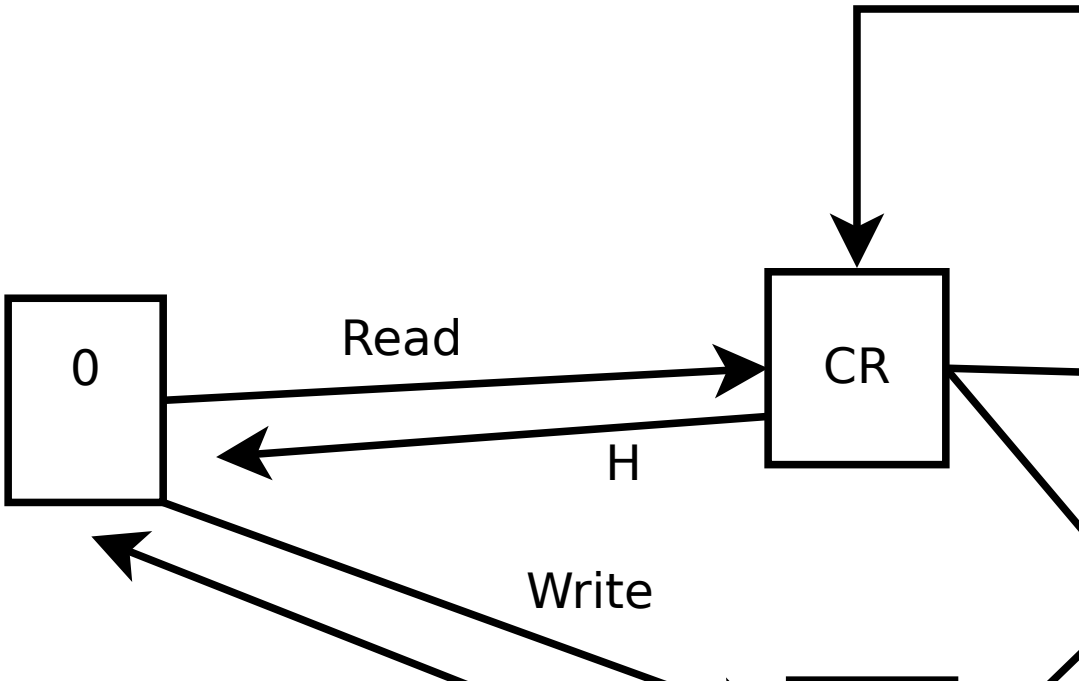
wo
cor
wri
wri

CW

wr
wc
co
wr

index is always = address[10:3]
valid_in is always = 1
tag_in is always = address[15:11]
enable is always = 1

Main FSM

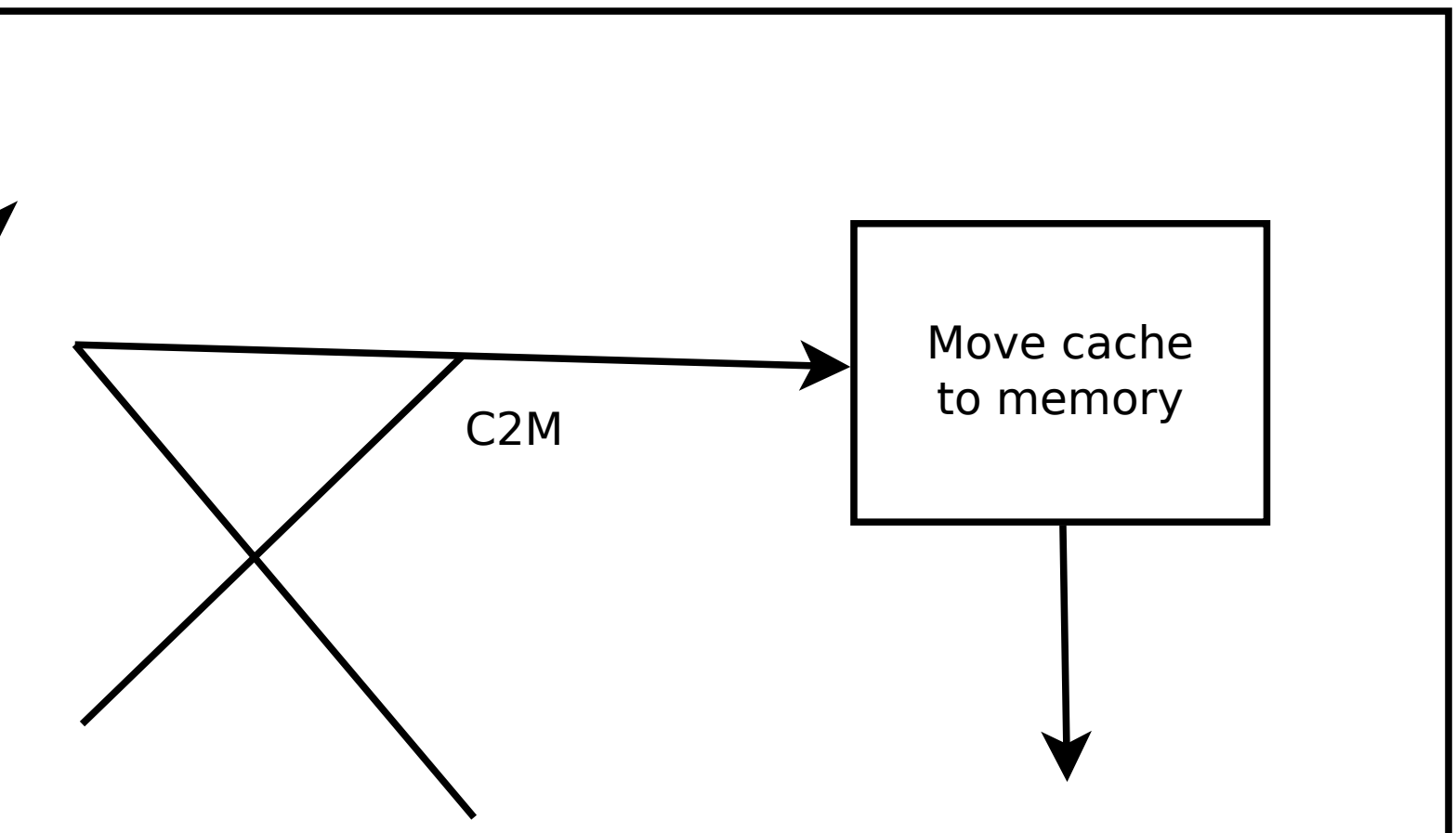


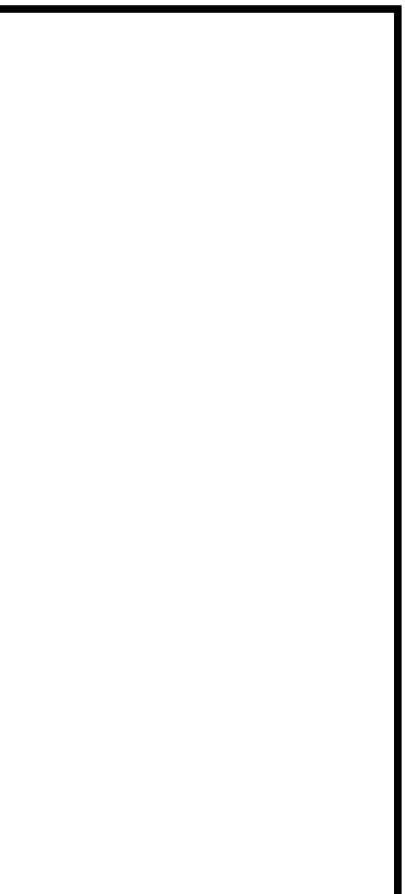
word = address[2:1]
comp = 1
write = 0
writesrc = x

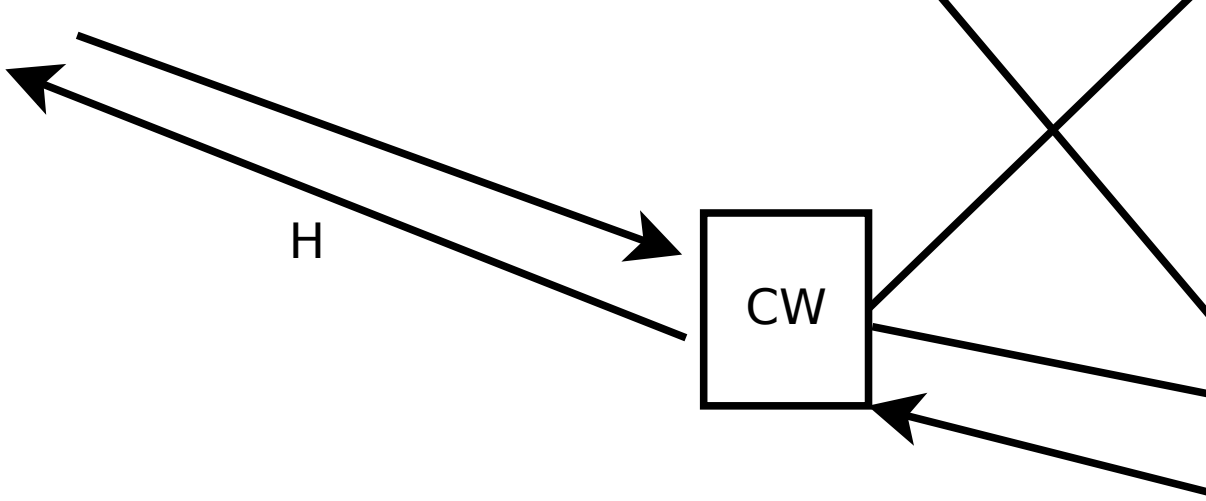
AR
comp = 0
write = 0
writesrc = x

writesrc=DataIn
word = address[2:1]
comp = 1
write = 1

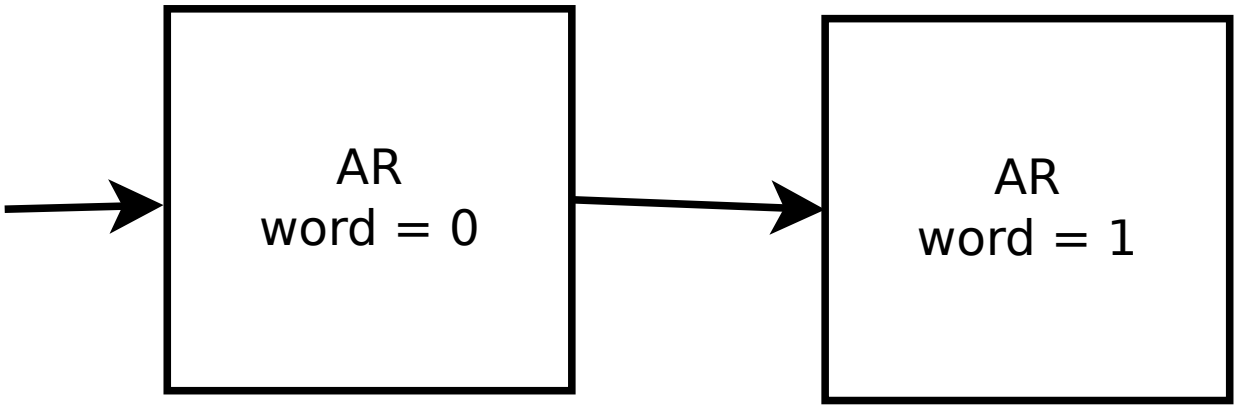
AW
writesrc=memory
comp = 0
write = 1



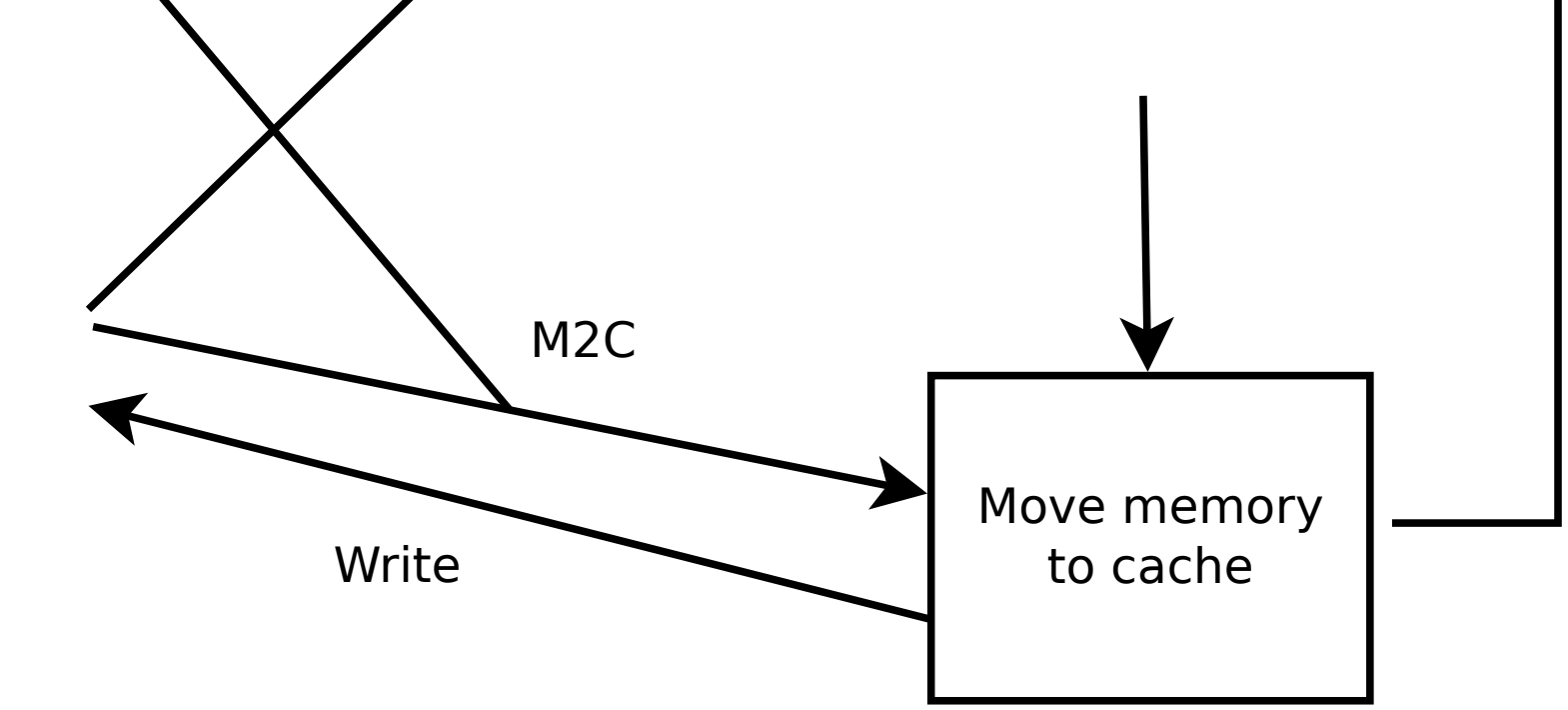

Read

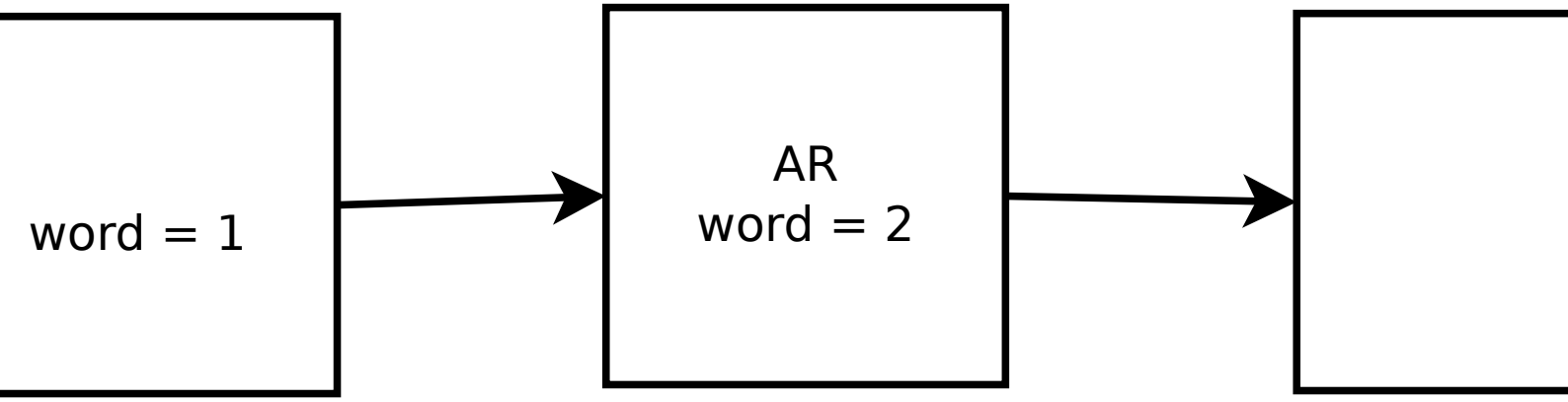


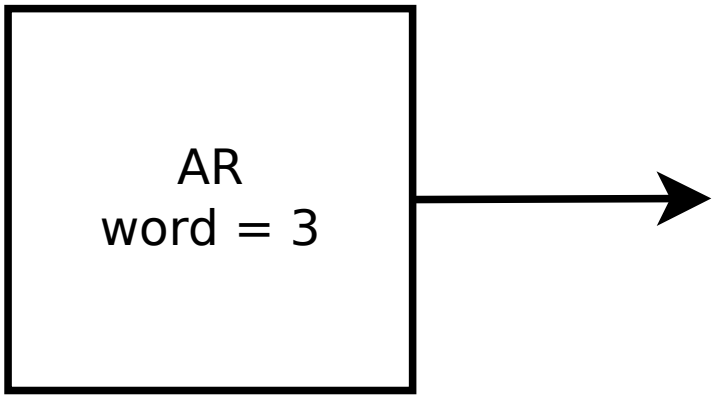
Cache to Memory

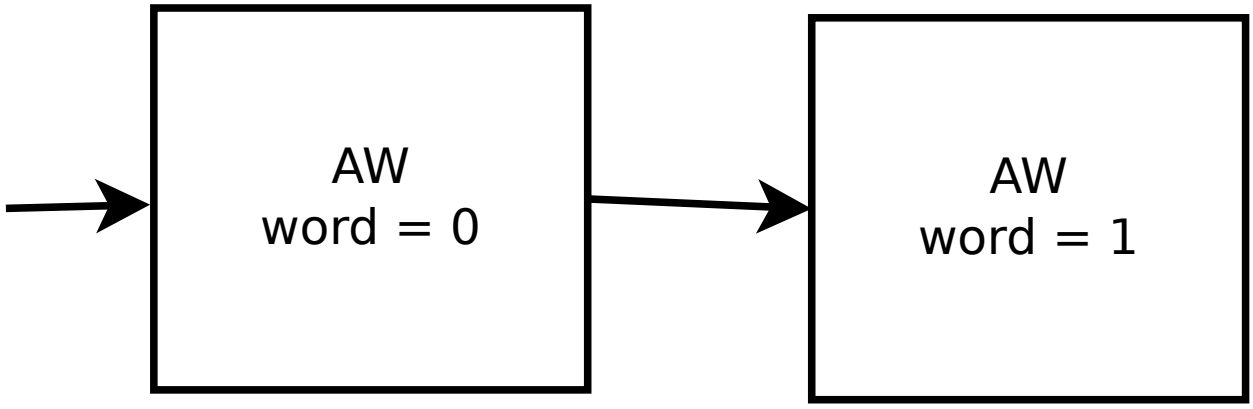


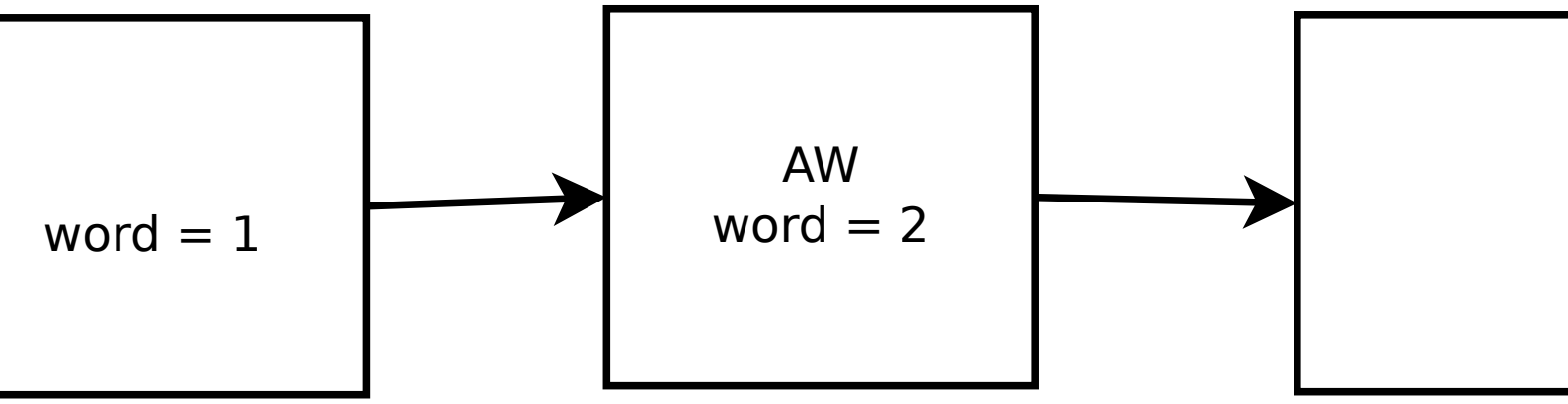
Memory to Cache

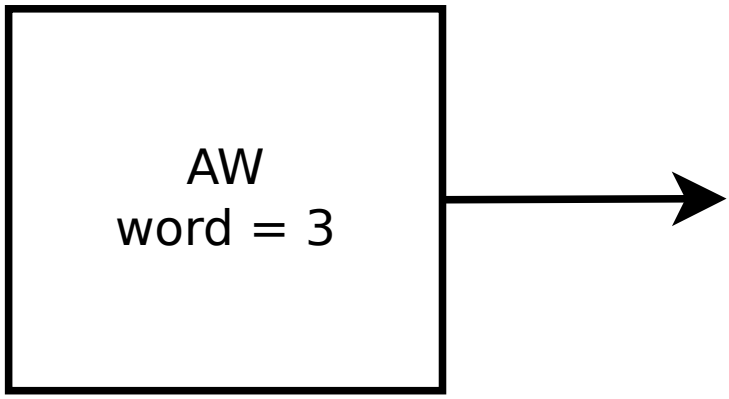

M2C
Write
Move memory
to cache


word = 1
AR
word = 2


AR
word = 3


AW
word = 0
AW
word = 1


word = 1
AW
word = 2


AW
word = 3