

AC107/AC107S 2-Channel High Performance Voice Capture ADCs with I2C/I2S

1 Features

- 103 dB dynamic range(A-weight) @ 0 dB boost gain
- - 85 dB THD+N @ 0 dB boost gain
- ADC sample rates supported: 8kHz~96kHz
- Two fully differential microphone inputs
- One digital microphone SCLK output @1.024M~3.072M
- PLL support a wide clock input for 6/12MHz, 6.144MHz, 5.6448MHz, 13MHz, 16MHz, 19.2MHz and 24MHz
- Programmable low noise Microphone Bias 1.8V~3.0V
- <20mW 2-ADC for low power consumption application

13MHz, 19.2MHz, 24.576MHz and other non standard audio system clocks. The audio sample 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz is supported.

The AC107 integrates stereo synchronized ADCs with independent programmable mic bias voltage and mic boost amplifier to deliver valid channel data that channel crosstalk can be eliminated. The analog input port MIC1P/N ~MIC2P/N is designed as two differential microphone pin or single-ended line-in pin. Independent digital volume controllers are provided in each channel.

2 Applications

- Smart Voice Assistant Systems
- Voice Recorders
- Digital Cameras and video cameras
- Voice Conferencing System

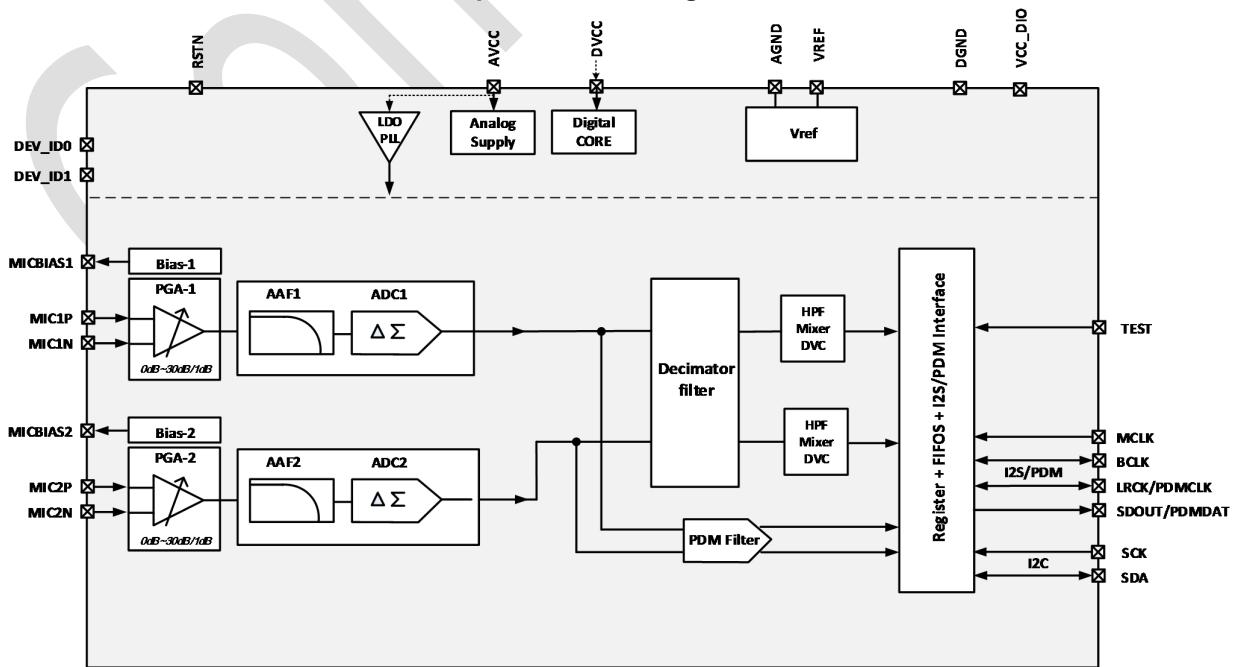
The AC107 can transit its 2 channels output data over the I2S port by standard I2S or PCM format. Also, one to eight device can be combined to transit up to 16 channels output data by a single TDM line. Furthermore, A new format called encoding mode can be used to transit 16 channels data when the I2S format of AP is normal protocol types.

The AC107 is controlled through TWI (2-wire serial interface, I2C compatible). The clock supports up to 400 KHz rate. It works only in the slave mode.

Device Information

| Part Number | Package | Body Size |
|-------------|---------|-------------|
| AC107 | QFN-20 | 3.0mm*3.0mm |
| AC107S | QFN-24 | 4.0mm*4.0mm |

Simplified Block Diagram



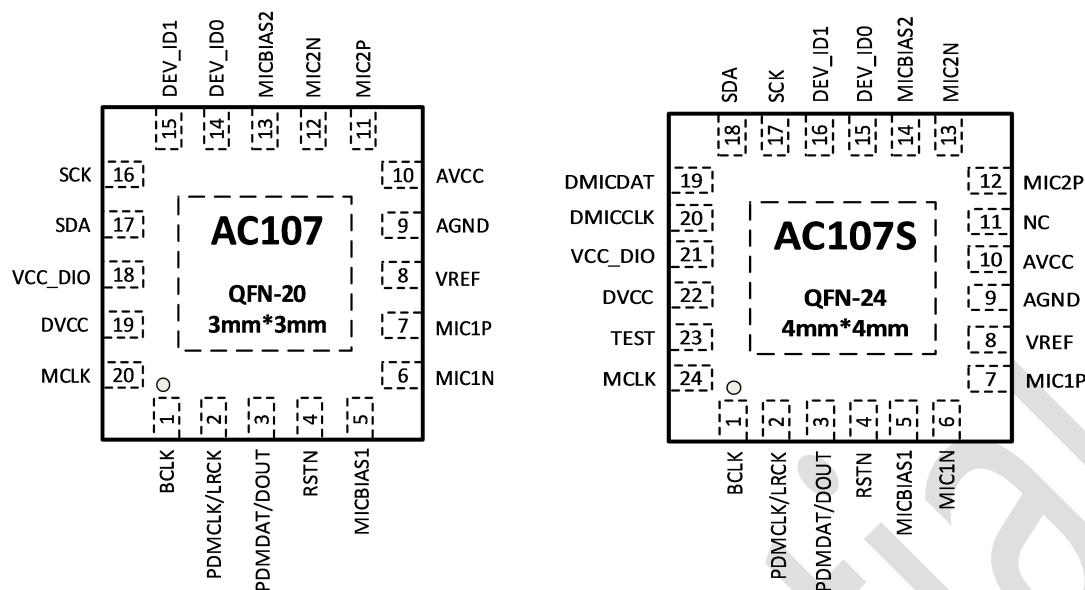
4 Revision History

| Revision | Date | Description |
|----------|---------------|---------------------------------------|
| V1.0 | Dec.12, 2018 | Initial internal release |
| V1.1 | Mar. 22, 2019 | Add power consumption |
| V1.2 | Apr. 26, 2019 | Add marking information and carrier |
| V1.23 | May. 8,2019 | Change carrier from tray to tape reel |

Contents

| | |
|---|-----------|
| 1 FEATURES..... | 1 |
| 2 APPLICATIONS..... | 1 |
| 3 DESCRIPTION..... | 1 |
| 4 REVISION HISTORY..... | 2 |
| 5 PIN CONFIGURATION AND FUNCTIONS..... | 3 |
| 6 SPECIFICATIONS..... | 4 |
| 6.1 ABSOLUTE MAXIMUM RATINGS..... | 4 |
| 6.2 ESD RATINGS..... | 4 |
| 6.3 RECOMMENDED OPERATING CONDITIONS..... | 4 |
| 6.4 THERMAL INFORMATION..... | 4 |
| 6.5 ANALOG CHARACTERISTICS..... | 5 |
| 6.6 ELECTRICAL CHARACTERISTICS..... | 6 |
| 7 DETAILED DESCRIPTIONS..... | 7 |
| 7.1 OVERVIEW..... | 7 |
| 7.2 FUNCTIONAL BLOCK DIAGRAM..... | 7 |
| 7.3 FEATURE DESCRIPTION..... | 8 |
| 7.4 BASIC SETUP SEQUENCES..... | 19 |
| 7.5 REGISTER MAPS..... | 20 |
| 8 APPLICATION INFORMATION..... | 46 |
| 9 PCB LAYOUT GUIDELINES..... | 47 |
| 10 PACKAGE AND ORDERING INFORMATION..... | 48 |
| 10.1 PACKAGE INFORMATION..... | 48 |
| 10.2 MARKING INFORMATION..... | 50 |
| 10.3 CARRIER..... | 51 |
| 11 Reflow Profile..... | 52 |

5 Pin Configuration and Functions



PIN DESCRIPTION

| Pin Number | | Name | I/O | Description |
|------------|--------|---------------|-----|---|
| AC107 | AC107S | | | |
| 1 | 1 | BCLK | IO | I2S interface serial bit clock |
| 2 | 2 | LRCK/PDMCLK | IO | I2S interface synchronous clock/PDM interface synchronous clock |
| 3 | 3 | SDOUT/PDMDATA | O | I2S interface serial data output/PDM interface serial data output |
| 4 | 4 | RSTN | I | Chip rest pin |
| 5 | 5 | MICBIAS1 | O | Bias voltage output for MIC1 |
| 6 | 6 | MIC1N | I | Negative differential input for MIC1 |
| 7 | 7 | MIC1P | I | Positive differential input for MIC1 |
| 8 | 8 | VREF | O | Internal reference voltage |
| 9 | 9 | AGND | G | Analog Ground |
| 10 | 10 | AVCC | P | The analog part Power input |
| -- | 11 | NC | -- | Not connected |
| 11 | 12 | MIC2P | I | Positive differential input for MIC2 |
| 12 | 13 | MIC2N | I | Negative differential input for MIC2 |
| 13 | 14 | MICBIAS2 | O | Bias voltage output for MIC2 |
| 14 | 15 | DEV_ID0 | I | |
| 15 | 16 | DEV_ID1 | I | TWI interface device ID control |
| 16 | 17 | SCK | I | TWI interface serial clock input |
| 17 | 18 | SDA | IO | TWI interface serial data(Open-drain) |
| -- | 19 | DMICDAT/SDIN | IO | Digital MIC stereo data input/I2S interface serial data input |
| -- | 20 | DMICCLK | IO | Digital MIC CLK output |
| 18 | 21 | VCC_DIO | P | Digital power for digital I/O buffer |
| 19 | 22 | DVCC | P | The digital part Power input |
| -- | 23 | TEST | I | Scan test for QAQC |
| 20 | 24 | MCLK/SYNCCLK | IO | I2S interface master input clock/synchronous clock output |
| EPAD | EPAD | GND | G | Digital Ground |

Note: O for output, I for input, I/O for input/output, P for power, and G for ground

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range(unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------------------------|---------|------|-------------|------|
| Supply voltage range | DVCC | -0.3 | 2.4 | V |
| | AVCC | -0.3 | 3.9 | V |
| | VCC_DIO | -0.3 | 3.9 | V |
| Output voltage range | MBIAS | -0.3 | 3.0 | V |
| Digital Input voltage to ground | | -0.3 | VCC_DIO+0.3 | V |
| Analog input voltage to ground | | -0.3 | AVCC+0.3 | V |
| Operating Temperature, T_A | | -40 | 85 | °C |
| Junction temperature, T_J | | -- | 125 | °C |
| Storage temperature, T_{stg} | | -65 | 150 | °C |

(1) Current test performance: Pins stressed per JEDEC JESD78D(Class I, Level A) and passed with I/O pin injection current as defined in JEDEC.

(2) Over voltage performance: Supplies stressed per JEDEC JESD78D(Class I, Level A) and passed voltage injection as defined in JEDEC.

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|---|------------|------|
| $V_{(ESD)}$ | Human body model(HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ± 4000 | V |
| | Charged device model(CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ± 500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|-----------|---|--------------|-------|-------|------|
| DVCC | Input power for digital domain cell control | 1.62 | 1.8 | 1.98 | V |
| AVCC | Input power for analog part | 3.0 | 3.3 | 3.63 | V |
| VCC_DIO | Digital power for digital I/O buffer | 1.62 | 3.3 | 3.63 | V |
| Vi | Analog full-scale 0-dB input voltage | 0.934 | 0.955 | 1.122 | Vrms |
| V_{IH} | High Level Input Voltage | VCC_DIO=3.3V | 2.4 | 3.3 | 3.63 |
| | | VCC_DIO=1.8V | 1.4 | 1.8 | 1.98 |
| V_{IL} | Low Level Input Voltage | -0.3 | 0 | 0.7 | V |
| V_{OH} | High Level Output Voltage | 2.7 | 3.3 | 3.63 | V |
| V_{OL} | Low Level Output Voltage | -0.3 | 0 | 0.4 | V |
| C_{OUT} | Digital output load capacitance | | | 10 | pF |

6.4 Thermal Information

| | THERMAL METRIC ⁽¹⁾ | AC107 | UNIT |
|---------------|--|-------|------|
| θ_{JA} | Junction-to-ambient thermal resistance | 31.9 | °C/W |
| θ_{JC} | Junction-to-case(top) thermal resistance | 18.2 | |
| θ_{JB} | Junction-to-board thermal resistance | 10.1 | |

(1) Thermal metrics are calculated refer to JEDEC document JESD51-2.

6.5 Analog Characteristics

At 25°C, AVCC=3.3V, DVCC=1.8V, VCC_DIO=3.3V, 24-bit audio data, 1kHz sine wave input

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------------------------|----------------------------|-----|------|------|------|
| AUDIO ADC | | | | | |
| DR(A-weighted) | PGA gain = 0dB, @Fs=16KHz | | 103 | | dB |
| THD+N | | | -85 | | dB |
| DR(A-weighted) | PGA gain = 12dB, @Fs=16KHz | | 102 | | dB |
| THD+N | | | -84 | | dB |
| DR(A-weighted) | PGA gain = 24dB, @Fs=16KHz | | 94 | | dB |
| THD+N | | | -82 | | dB |
| DR(A-weighted) | PGA gain = 30dB, @Fs=16KHz | | 89 | | dB |
| THD+N | | | -81 | | dB |
| DR(A-weighted) | PGA gain = 0dB, @Fs=48KHz | | 103 | | dB |
| THD+N | | | -82 | | dB |
| DR(A-weighted) | PGA gain = 24dB, @Fs=48KHz | | 92 | | dB |
| THD+N | | | -80 | | dB |
| Crosstalk (L/R) | 10mV, 1KHz, 30dB Gain | | -100 | | dB |
| MICBIAS | | | | | |
| Output Scale | | 1.8 | 3 | AVCC | V |
| Bias Current | | | 4 | | mA |
| Noise Level(A-weighted) | | 1.7 | 4 | | uV |

6.6 Electrical Characteristics

At 25°C, AVCC=3.3V, DVCC=1.8V, VCC_DIO=3.3V, MCLK=12.288MHz, I2S, 32bit

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit | |
|--------------------------|-----------------------------|-------------------|-----|-------|-----|------|--|
| POWER CONSUMPTION | | | | | | | |
| 1-ADC | PGA gain = 0dB, @Fs = 16KHz | I _{1.8V} | | 0.271 | | mA | |
| | | I _{3.3V} | | 1.682 | | mA | |
| 2-ADC | PGA gain = 0dB, @Fs = 16KHz | I _{1.8V} | | 0.319 | | mA | |
| | | I _{3.3V} | | 3.094 | | mA | |
| 1-ADC | PGA gain = 0dB, @Fs = 48KHz | I _{1.8V} | | 0.6 | | mA | |
| | | I _{3.3V} | | 1.881 | | mA | |
| 2-ADC | | I _{1.8V} | | 0.745 | | mA | |
| | | I _{3.3V} | | 3.483 | | mA | |
| 1-ADC | PGA gain = 0dB, @Fs = 96KHz | I _{1.8V} | | 1.166 | | mA | |
| | | I _{3.3V} | | 2.169 | | mA | |
| 2-ADC | | I _{1.8V} | | 1.448 | | mA | |
| | | I _{3.3V} | | 4.106 | | mA | |

7 Detailed Descriptions

7.1 Overview

The AC107 is a highly integrated 2-channel ADC with I2S/TDM output transition. It's designed for multi-microphone array in high definition voice capture and recognition application platforms.

The integrated digital PLL supports a large range of input/output frequencies, and it can generate required system clocks from common reference clock such as 6-/12-MHz, 6.144-/12.288-MHz, 5.6448-/11.2896-MHz, 13MHz, 19.2MHz, 24.576MHz and other non standard audio system clocks. The audio sample 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz is supported.

The AC107 integrates stereo synchronized ADCs with independent programmable mic bias voltage and mic boost amplifier to deliver valid channel data that channel crosstalk can be eliminated. The analog input port MIC1P/N ~MIC2P/N is designed as two differential microphone pin or single-ended line-in pin. Independent digital volume controllers are provided in each channel.

The AC107 can transit its 2 channels output data over the I2S port by standard I2S or PCM format. Also, one to eight device can be combined to transit up to 16 channels output data by a single TDM line. Furthermore, A new format called encoding mode can be used to transit 16 channels data when the I2S format of AP is normal protocol types.

The device includes several DSP features such as high-pass filter, mixer, and volume control.

AC107 is controlled through TWI (2-wire serial interface). The clock supports up to 400 KHz rate. It works only in the slave mode.

The device is available in a 20-pin 3mm*3mm QFN package or in a 24-pin 4mm*4mm QFN package.

7.2 Functional Block Diagram

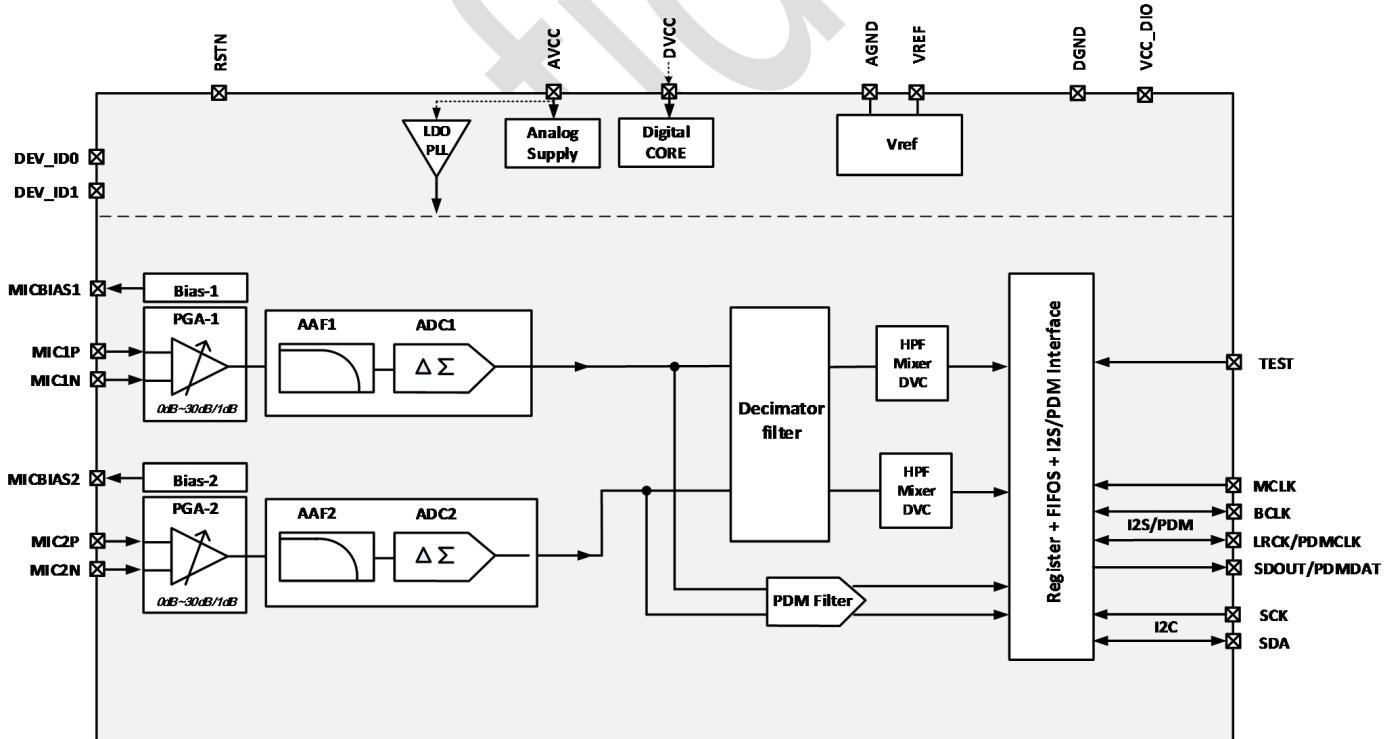


Figure 7-1. AC107 Block Diagram

7.3 Feature Description

7.3.1 Power

AC107 has a clear power management to make sure analog circuit work in a high performance status. All the supply voltages are illustrated in the below figure.

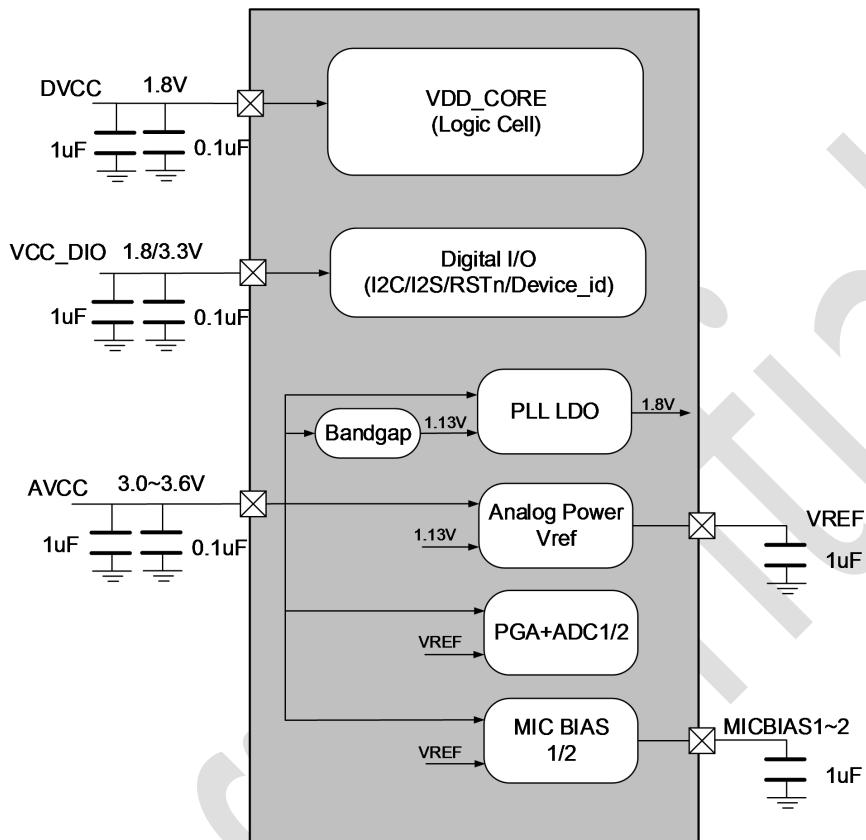


Figure 7-2. Power Management

DVCC is the digital power input for the logic cell control. AVCC is the analog power supply rail input to the analog circuit, which usually needs a clear LDO to make sure analog circuit work in a high performance status. VREF is designed to be a low noise voltage as analog power reference. VDD_DIO is digital I/O power for TWI, I2S ,Device_IDx and RSTN.

The power supplies are designed to operate from 3.0 V to 3.63 V for AVCC, from 1.62 V to 1.98 V for DVCC and from 1.62 V to 3.63 V for VCC_DIO. Any value out of these ranges must be avoided to ensure the correct behavior of the device. The power supplies must be well regulated. Placing a decoupling capacitor close to the AC107 improves the performance of the device. A low equivalent-series-resistance (ESR) ceramic capacitor with a value of 0.1 μ F is a typical choice. If the AC107 is used in highly noise-sensitive circuits, it is recommended to add a small LC filter on the AVCC connections.

When the AC107 is not working, it need to set the supply properly to prevent power leakage. It's best to power off all the supply.

7.3.2 Reset

There are a Power-Reset circuit in AC107 used to reset all the circuit and register to a standby state after power up. The Power-Reset circuit make all the supply power need no specific timing.

The power reset and soft reset diagram is below:

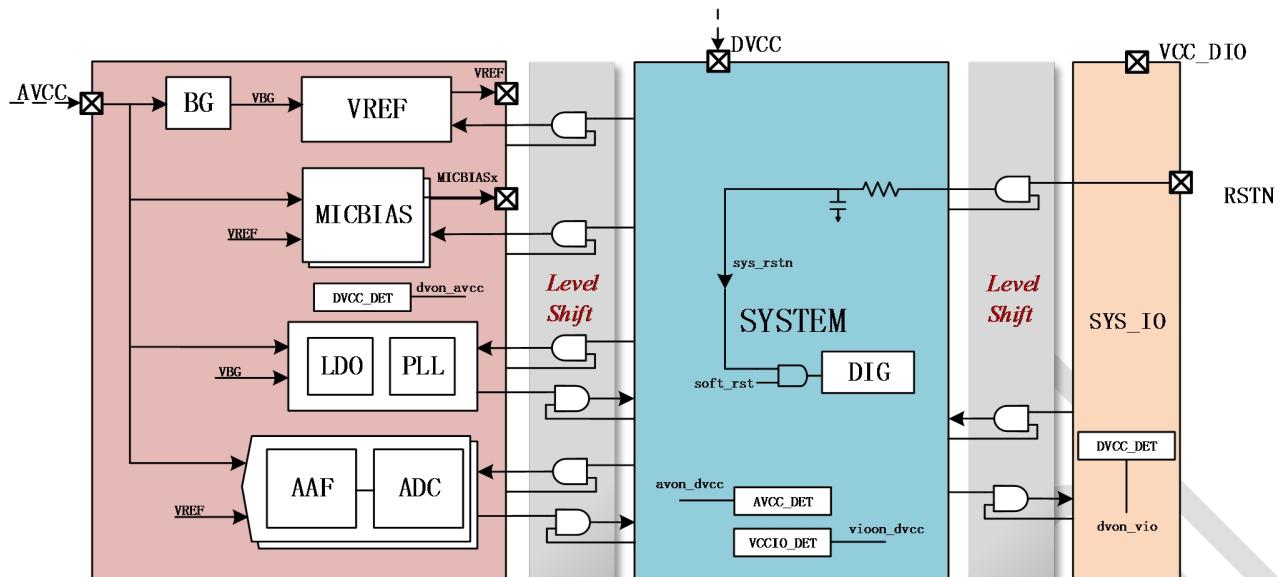


Figure 7-3. Reset Management

7.3.3 Clock

The system clock(SYSLCK) of AC107 must be $256 \times fs$ ($fs = 48\text{KHz}$ or 44.1KHz). So the system should arrange the divider to generate 12.288MHz for audio clock series of 48KHz or 11.2896MHz for series of 44.1KHz .

SYSLCK , which always provided by externally clock or internal PLL , can be selected from MCLK/I2S_BCLK or PLL, while the PLL reference clock can be selected from MCLK , I2S_BCLK or PDMCLK. SYSLCK is the clock reference of ADC, DVC, MIXER, HPF and I2S module except TWI. If MCLK&BCLK are both not 12.288MHz for ADC 48KHz series sample rate or 11.2896MHz for ADC 44.1KHz series sample rate, SYSLCK must be selected from PLL. SYSLCK always need to be configured in these cases.

SCK pin is always an external clock input pin and the clock is used as the reference of the TWI clocking zone.

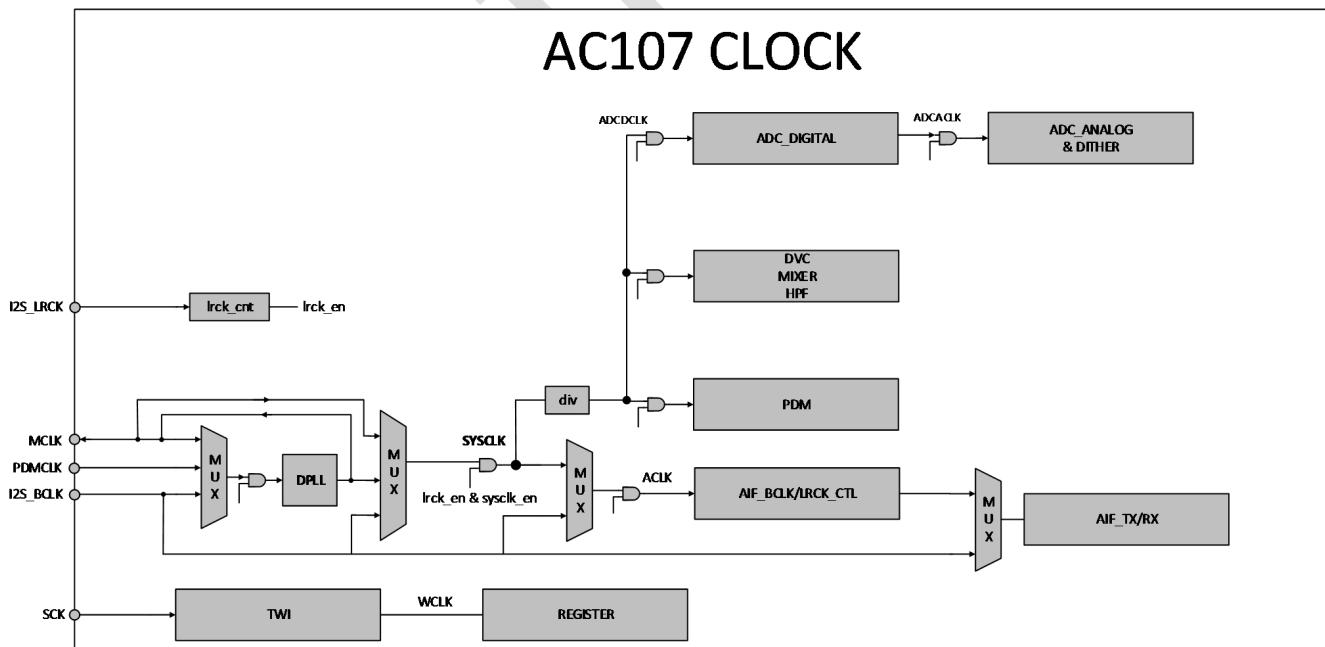


Figure 7-4. Clock Management Unit

The clock management related registers are *Reg[0x20]~Reg[0x22]*.

7.3.4 PLL

A Phase-Locked Loop (PLL) is designed to cover a flexible input clock range from 400KHz to 24MHz. The clock sources of the PLL can be set to MCLK , BCLK or PDMCLK by setting register *Reg[0x20]*. The PLL output is always used to provide the system clock (SYSCLK) for AC107 when 12.288MHz or 11.2896MHz cannot be provided from MCLK and BCLK. The PLL transmit formula as below:

$$F_{OUT} = (F_{IN} * N) / ((M_1 + 1) * (M_2 + 1) * (K_1 + 1) * (K_2 + 1)) ;$$

Table 7-1. clock setting for SYSCLK=12.288MHz

| FIN | M1 | M2 | Fref | N | Fvco | K1 | K2 | FOUT |
|------------|-----------|-----------|-------------|----------|-------------|-----------|-----------|-------------|
| 400K | 0 | 0 | 400K | 983 | 393.2M | 15 | 1 | 12287500 |
| 512K | 0 | 0 | 512K | 960 | 491.52M | 19 | 1 | 12288000 |
| 768K | 0 | 0 | 768K | 640 | 491.52M | 19 | 1 | 12288000 |
| 800K | 0 | 0 | 800K | 768 | 614.4M | 24 | 1 | 12288000 |
| 1.024M | 0 | 0 | 1.024M | 480 | 491.52M | 19 | 1 | 12288000 |
| 1.6M | 0 | 0 | 1.6M | 384 | 614.4M | 24 | 1 | 12288000 |
| 2.048M | 0 | 0 | 2.048M | 240 | 491.52M | 19 | 1 | 12288000 |
| 3.072M | 0 | 0 | 3.072M | 160 | 491.52M | 19 | 1 | 12288000 |
| 4.096M | 0 | 0 | 4.096M | 120 | 491.52M | 19 | 1 | 12288000 |
| 6M | 4 | 0 | 1.2M | 512 | 614.4M | 24 | 1 | 12288000 |
| 6.144M | 1 | 0 | 3.072M | 160 | 491.52M | 19 | 1 | 12288000 |
| 12M | 9 | 0 | 1.2M | 512 | 614.4M | 24 | 1 | 12288000 |
| 13M | 12 | 0 | 1M | 639 | 639M | 25 | 1 | 12288462 |
| 15.36M | 9 | 0 | 1.536M | 320 | 491.52M | 19 | 1 | 12288000 |
| 16M | 9 | 0 | 1.6M | 384 | 614.4M | 24 | 1 | 12288000 |
| 19.2M | 11 | 0 | 1.6M | 384 | 614.4M | 24 | 1 | 12288000 |
| 19.68M | 15 | 1 | 615K | 999 | 614.385M | 24 | 1 | 12287700 |
| 24M | 9 | 0 | 2.4M | 256 | 614.4M | 24 | 1 | 12288000 |

Table 7-2. clock setting for SYSCLK=11.2896 MHz

| FIN | M1 | M2 | Fref | N | Fvco | K1 | K2 | FOUT |
|------------|-----------|-----------|-------------|----------|-------------|-----------|-----------|-------------|
| 400K | 0 | 0 | 400K | 1016 | 406.4M | 17 | 1 | 11288889 |
| 512K | 0 | 0 | 512K | 882 | 451.584M | 19 | 1 | 11289600 |
| 768K | 0 | 0 | 768K | 588 | 451.584M | 19 | 1 | 11289600 |
| 800K | 0 | 0 | 800K | 508 | 406.4M | 17 | 1 | 11288889 |
| 1.024M | 0 | 0 | 1.024M | 441 | 451.584M | 19 | 1 | 11289600 |
| 1.6M | 0 | 0 | 1.6M | 254 | 406.4M | 17 | 1 | 11288889 |
| 2.048M | 1 | 0 | 1.024M | 441 | 451.584M | 19 | 1 | 11289600 |
| 3.072M | 0 | 0 | 3.072M | 147 | 451.584M | 19 | 1 | 11289600 |
| 4.096M | 3 | 0 | 1.024M | 441 | 451.584M | 19 | 1 | 11289600 |
| 6M | 1 | 0 | 3M | 143 | 429M | 18 | 1 | 11289474 |
| 6.144M | 1 | 0 | 3.072M | 147 | 451.584M | 19 | 1 | 11289600 |
| 12M | 3 | 0 | 3M | 143 | 429M | 18 | 1 | 11289474 |
| 13M | 12 | 0 | 1M | 429 | 429M | 18 | 1 | 11289474 |
| 15.36M | 14 | 0 | 1.024M | 441 | 451.584M | 19 | 1 | 11289600 |
| 16M | 24 | 0 | 640K | 882 | 564.48M | 24 | 1 | 11289600 |
| 19.2M | 4 | 0 | 3.84M | 147 | 564.48M | 24 | 1 | 11289600 |
| 19.68M | 13 | 1 | 703K | 771 | 541.90M | 23 | 1 | 11289643 |

| | | | | | | | | |
|-----|----|---|------|-----|---------|----|---|----------|
| 24M | 24 | 0 | 960K | 588 | 564.48M | 24 | 1 | 11289600 |
|-----|----|---|------|-----|---------|----|---|----------|

7.3.5 TWI Interface

TWI is a 2-wire (SCK/SDA) half-duplex serial communication interface, supporting only slave mode. SCK is used for clock and SDA is used for data. SCK clock supports up to 400KHz rate and SDA data is an open drain structure.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCK is high. The first byte transferred is the slave 7-bit address followed by a R/W bit. The 7-bit chip address changed by external two Pins DEV_ID0 and DEV_ID1. The chip address is defined by Table 7-3 below. The R/W bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the R/W bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCK is high.

Table 7-3. The Chip Slave address

| 7-bit Address | DEV_ID1 | DEV_ID0 |
|----------------|---------|---------|
| 0x36(011 0110) | 0 | 0 |
| 0x37(011 0111) | 0 | 1 |
| 0x38(011 1000) | 1 | 0 |
| 0x39(011 1001) | 1 | 1 |

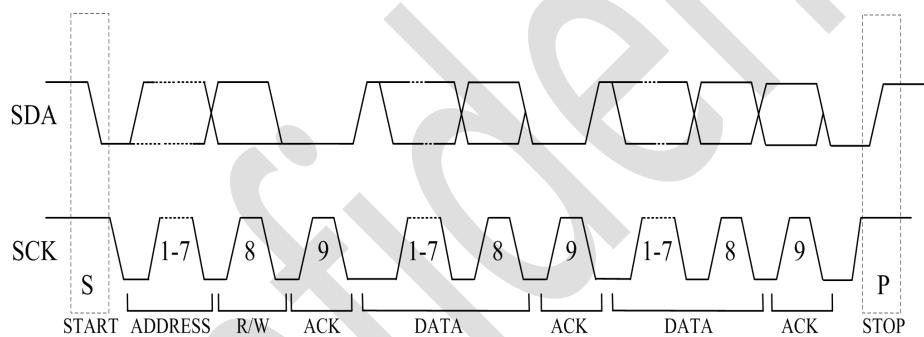


Figure 7-5. TWI Interface

The formats of “write” and “read” instructions are shown in below.

| | | | | | | | | |
|---|----------------|----|---|---------------|---|---------------|---|---|
| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
| S | Device Address | Wr | A | Reg addr byte | A | Reg data byte | A | P |

Write Word Protocol

| | | | | | | | | | | | | |
|---|----------------|----|---|---------------|---|---|----------------|----|---|---------------|---|---|
| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 1 |
| S | Device Address | Wr | A | Reg addr byte | A | S | Device Address | Rd | A | Reg data byte | N | P |

Read Word Protocol

S: Start Condition

Slave Address: 7-bit Device Address

P: Stop Condition

Command Code: 8-bit Register Address

A: 0 for ACK, 1 for NACK

Data Byte: 8-bit Register data

Wr: 0 for Write Command

: Master-to-Slave

Rd: 1 for Read Command

: Slave-to-Master

Figure 7-6. TWI Read and Write

7.3.6 I2S/PCM Interface

There are only one I2S/PCM output engine which can be configured as master mode or slave mode in AC107. The I2S/PCM interfaces provide flexible transit protocol to support varied formats processors.

The serial data is normally driven on negative edge of BCLK. MSB bit of data is normally transmitted first. In the general case, the digital audio interface uses three pins as below:

- BCLK: Bit clock for data synchronization
- LRCK: Left/Right data alignment clock
- SDOUT: output data for ADC1~ADC2 data

I2S audio interface support three different data protocol types below.

- I2S/PCM normal mode
- I2S/PCM TDM mode
- I2S/PCM Encoding mode

I2S/PCM normal mode support four different data format types below. Normal mode is used to transmit 2 channel data on left and right channel simultaneously.

- I2S justified mode
- Left justified mode
- Right justified mode
- PCM short/long frame mode

I2S/PCM TDM mode support four different data format types below. TDM mode is used to transmit up to 16 channel data on timeslot0~timeslot15 when eight AC107 work simultaneously.

- I2S justified TDM mode
- Left justified TDM mode
- Right justified TDM mode
- PCM short/long frame TDM mode

I2S/PCM Encoding mode support four different data format types below. Encoding mode is used to transmit up to 16 channel data using normal I2S format by setting the I2S rate to multi-times of ADC. For example, when the sample rate of ADCs is 16KHz , I2S/PCM Encoding mode can transit 8 channel data by setting I2S LRCK to 16KHz*(8/2).

And the last 4 bits of the sample data indicate the channel number.

- I2S justified Encoding mode
- Left justified Encoding mode
- Right justified Encoding mode
- PCM short/long frame Encoding mode

The timing of I2S in Master mode shows below:

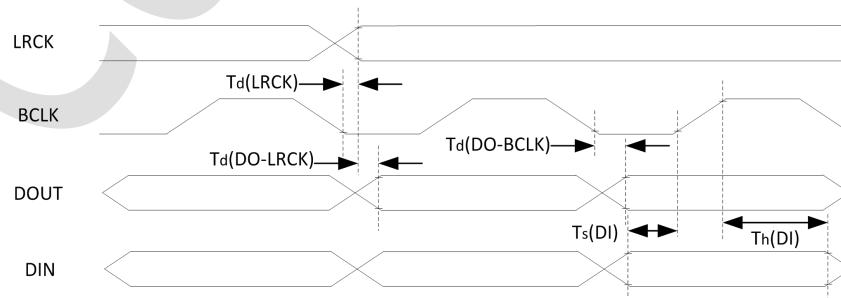
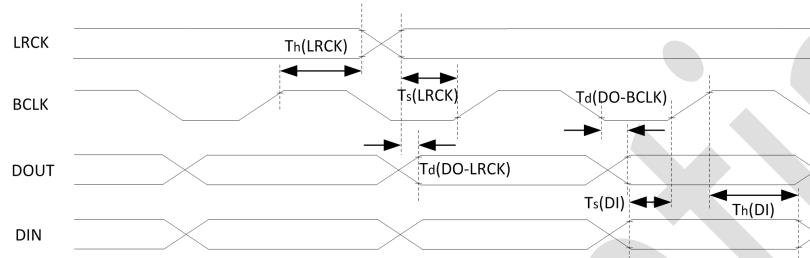


Figure 7-7. I2S Master Mode Timing

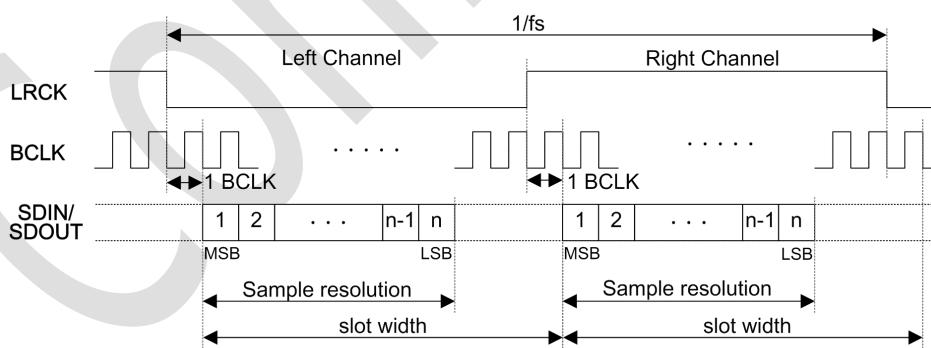
Table 7-4. I2S Timing in Master Mode

| PARAMETER | | MIN | MAX | UNITS |
|-------------|-----------------------------|-----|-----|-------|
| Td(LRCK) | LRCK delay | | 10 | ns |
| Td(DO-LRCK) | LRCK to DOUT delay(For Ljf) | | 10 | ns |
| Td(DO-BCLK) | BCLK to DOUT delay | | 10 | ns |
| Ts(DI) | DIN setup | 4 | | ns |
| Th(DI) | DIN hold | 4 | | ns |
| Tr | BCLK Rise time | | 8 | ns |
| Tf | BCLK Fall time | | 8 | ns |

The timing of I2S in slave mode shows below:


Figure 7-8. I2S Slave Mode Timing
Table 7-5. I2S Timing in Slave Mode

| PARAMETER | | MIN | MAX | UNITS |
|-------------|-----------------------------|-----|-----|-------|
| Ts(LRCK) | LRCK setup | 4 | | ns |
| Th(LRCK) | LRCK hold | 4 | | ns |
| Td(DO-LRCK) | LRCK to DOUT delay(For Ljf) | | 10 | ns |
| Td(DO-BCLK) | BCLK to DOUT delay | | 10 | ns |
| Ts(DI) | DIN setup | 4 | | ns |
| Th(DI) | DIN hold | 4 | | ns |
| Tr | BCLK Rise time | | 4 | ns |
| Tf | BCLK Fall time | | 4 | ns |


Figure 7-9. I2S Justified mode

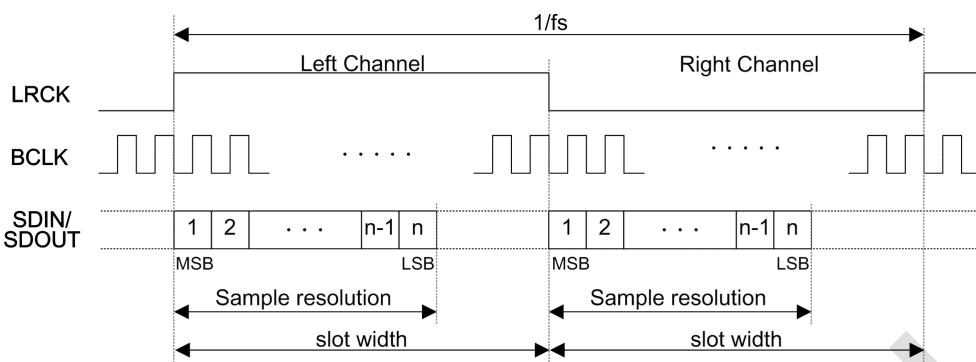


Figure 7-10. Left Justified mode

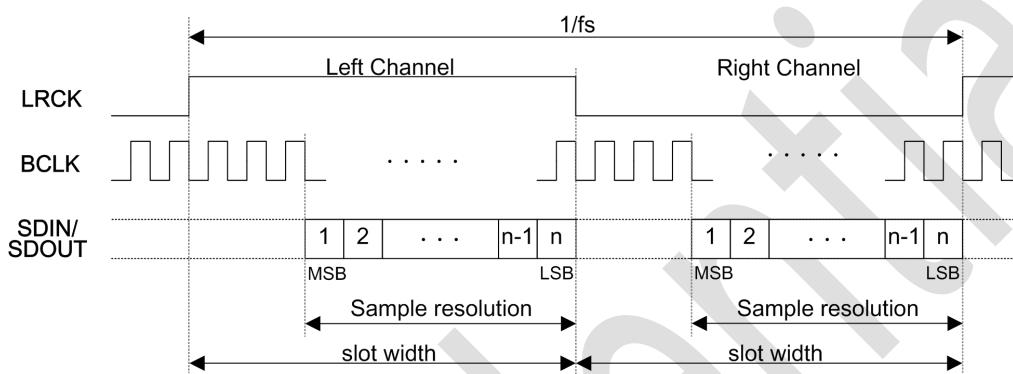


Figure 7-11. Right Justified mode

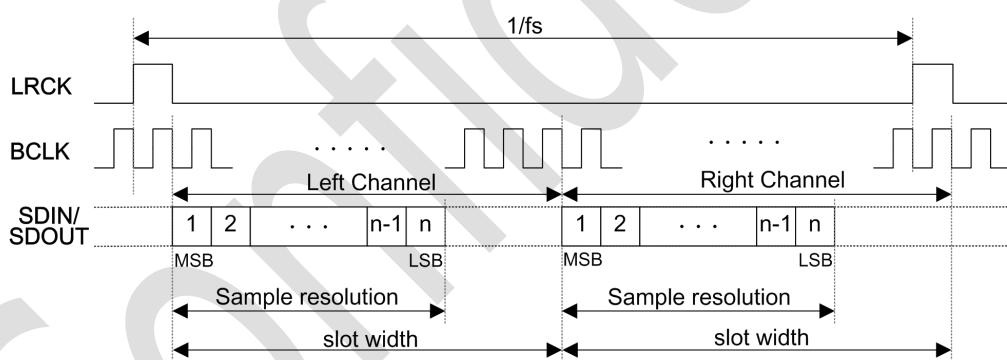


Figure 7-12. PCM mode A(Offset=1)

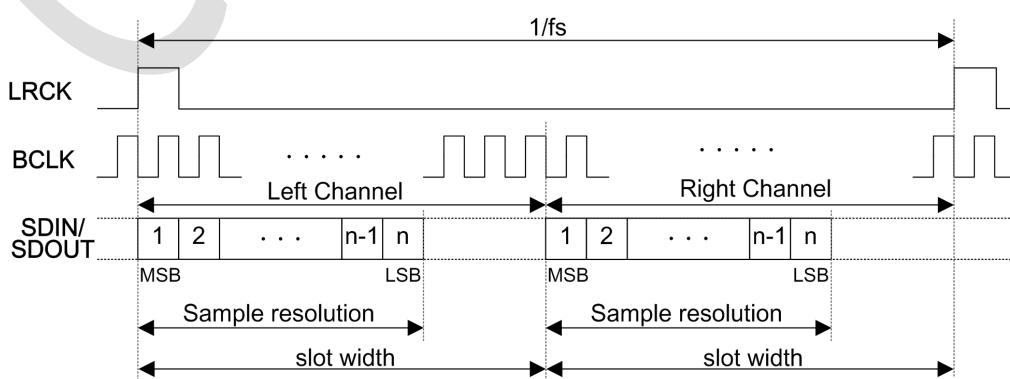
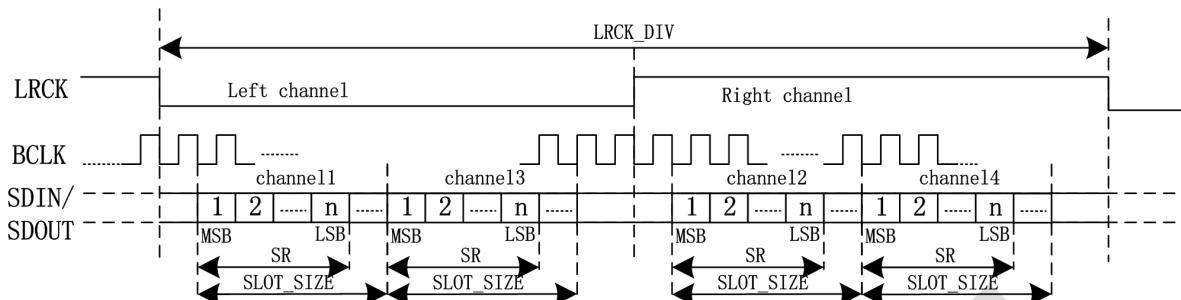
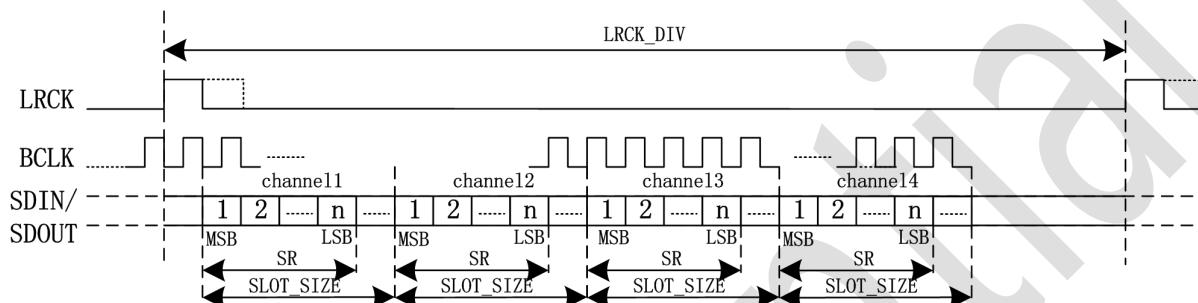
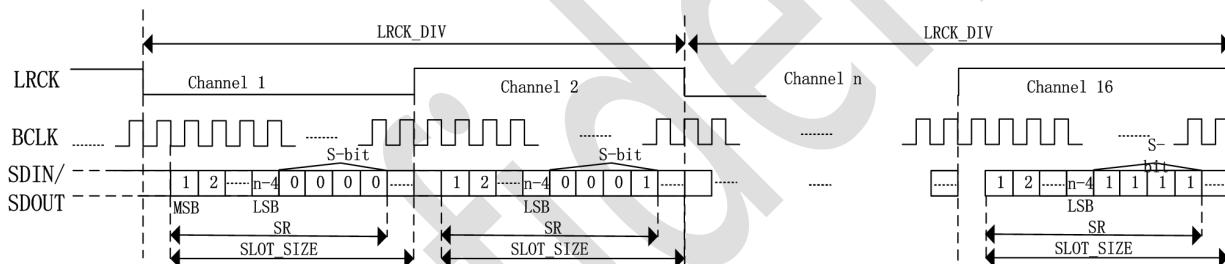
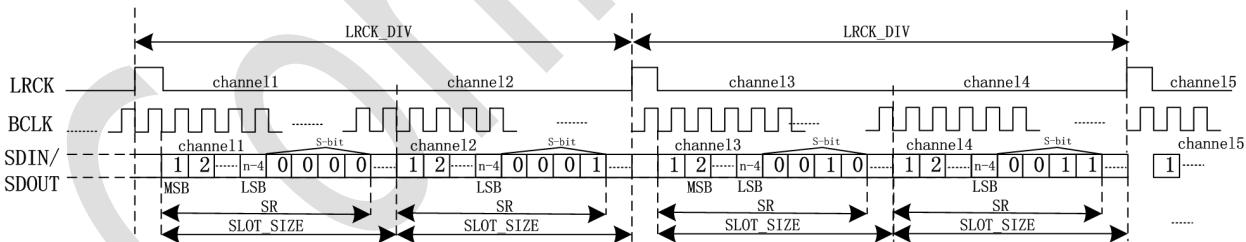


Figure 7-13. PCM mode B(Offset=0)

Figure 7-14. I2S TDM mode

Figure 7-15. PCM TDM mode

Figure 7-16. I2S Encoding mode

Figure 7-17. PCM Encoding mode

The I2S/PCM management related registers are *Reg[0x30]~Reg[0x3D]*.

7.3.7 Analog Microphone Input

MIC1P/N, MIC2P/N provide differential input to the ADC1,ADC2 record path. MICIN is high impedance, low capacitance input suitable for connection to a wide range of differential microphones of different dynamics and sensitive. There are two independent AAF(Anti-Alias Filter) and PGA(Pre-Gain Amplifier) for the two differential microphone inputs. The gain for each pre-amplifier can be set independently using MIC1BOOST, MIC2BOOST. Two MICBIASx ($x=1\sim 2$) provide reference voltage for electret condenser type(ECM) microphones.

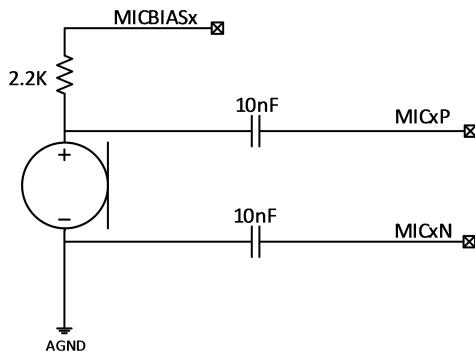


Figure 7-18. Suggested Single-Ended Mic Input

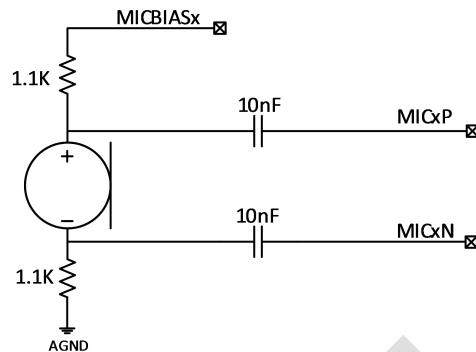


Figure 7-19. Suggested Differential Mic Input

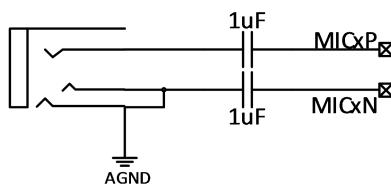


Figure 7-20. Suggested Single-Ended Line-in

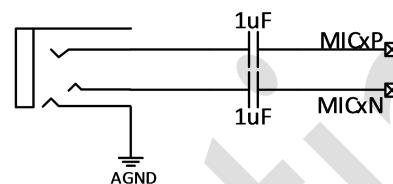


Figure 7-21. Suggested Differential Line-in

7.3.8 Analog ADC Data Path

The analog ADC data path includes separate programmable Pre-gain amplifier(PGA), anti-aliasing low-pass filter (AAF) and delta-sigma modulator (DSM). The PGA is designed to amplify input signals to the maximum full-scale signal. The AAF is designed to minimize the noise folded down to the audio band by the oversampling ADC, AAF ensure at least 60 dB attenuation at the modulator switching frequency. The DSM oversampling frequency runs at 128fs. The analog ADC data path related registers are *Reg[0xA0]~Reg[0xA9]*.

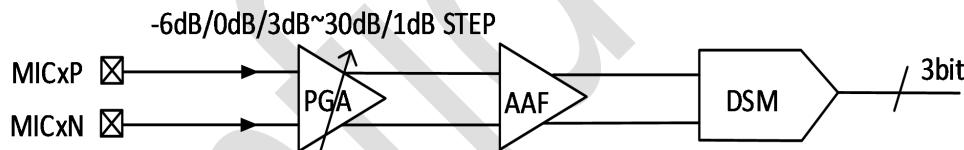


Table 7-6. PGA Gain Setting

| PGA Gain Setting | | | | | |
|-----------------------------|----------------------|------------------------------|--------------------------------|-----------------------------|--------------------------|
| pga_gain [4:0] (decimal) | Gain Setting (dB) | Output-Referred Gain (dB) | Max Input Level (Vrms diff) | Output Level (Vrms diff) | Input Resistance (kΩ) |
| 0 | -6 | 0 | 2.000 | 2 | 16 |
| 1 | 0 | 6 | 1.000 | 2 | 8 |
| 2 | 0 | 6 | 1.000 | 2 | 8 |
| 3 | 0 | 6 | 1.000 | 2 | 8 |
| 4 | 3 | 9 | 0.710 | 2 | 100/75/50/25 |
| 5 | 4 | 10 | 0.632 | 2 | 100/75/50/25 |
| ... | ... | ... | ... | 2 | 100/75/50/25 |
| N-5 | N-6 | N | $2/[10^{(N/20)}]$ | 2 | 100/75/50/25 |
| ... | ... | ... | ... | 2 | 100/75/50/25 |
| 31 | 30 | 36 | 0.032 | 2 | 100/75/50/25 |

NOTE: The PGA output referred gain = gain setting + 6 dB due to the single-ended to differential conversion.

7.3.9 Digital Data Path

The digital data path is provided with digital audio data source select, DSM decimation filter, HPF, volume controller and data mixing to two I2S output paths. Then the digital output of the DSM is decimated down to the required sample rate and then DC cancellation, digital amplification are implemented. Finally a digital selector and mixer is available to map any analog input into any channel or combine multiple channels into any single channel. It's separately controlled by the register *Reg[0x61]~Reg[0x7F]*.

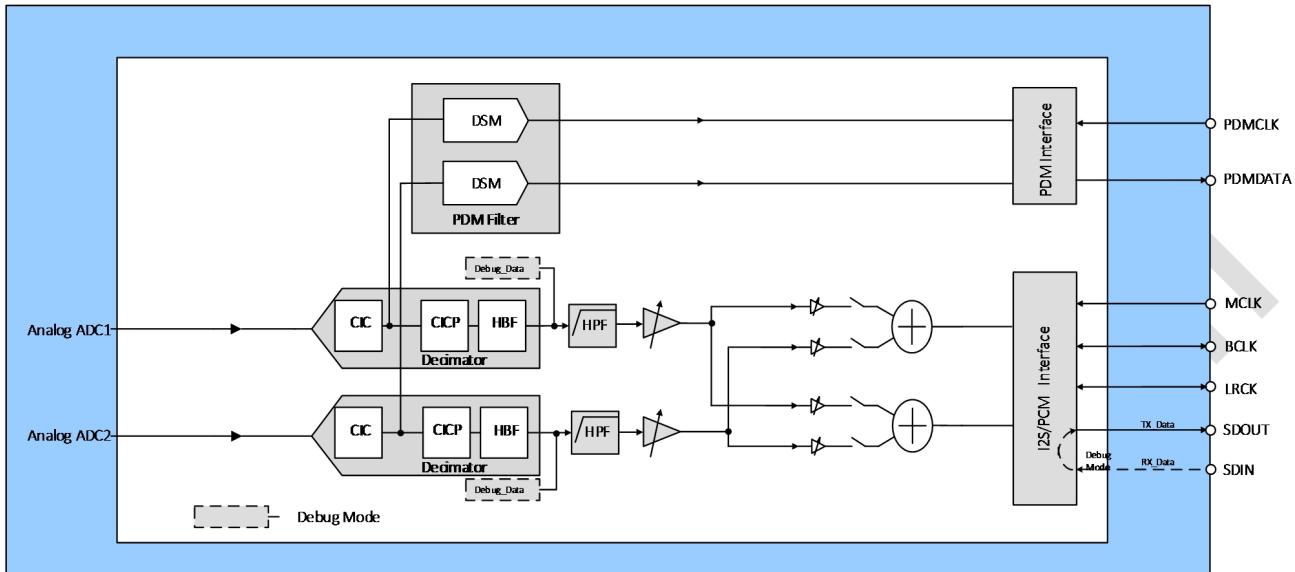


Figure 7-22. Digital Data Path

7.3.10 Digital Microphone Interface

One digital microphone interface is used for dual DMICs (Only supported on AC107S). The circuit share decimation filter with audio ADC. DMICCLK can be output 64fs when the DMIC over sample rate is 32kHz~48kHz and 128fs when the DMIC over sample rate is 8kHz~24kHz (fs = ADC sample rate).

Table 7-7. Digital Microphone Clock

| Fs(kHz) | 8 | 12 | 11.025 | 16 | 22.05 | 24 | 32 | 44.1 | 48 |
|-----------|------|------|--------|------|--------|------|------|--------|------|
| n | 128 | 128 | 128 | 128 | 128 | 128 | 64 | 64 | 64 |
| Freq(kHz) | 1024 | 1536 | 1411.2 | 2048 | 2822.4 | 3072 | 2048 | 2822.4 | 3072 |

Digital Microphone power usually falls between the range 1.6V-3.6V, typical 1.8V. And the Clock frequency is between the the range 1.024MHz-3.072MHz.

Digital Microphone timing as below:

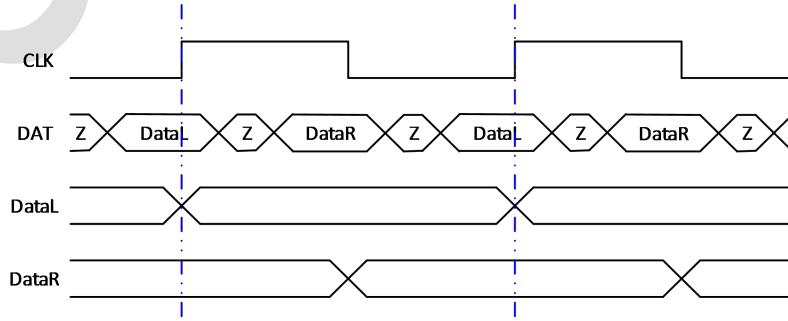


Figure 7-23. Digital Mixer Path

Digital Microphone application as below:

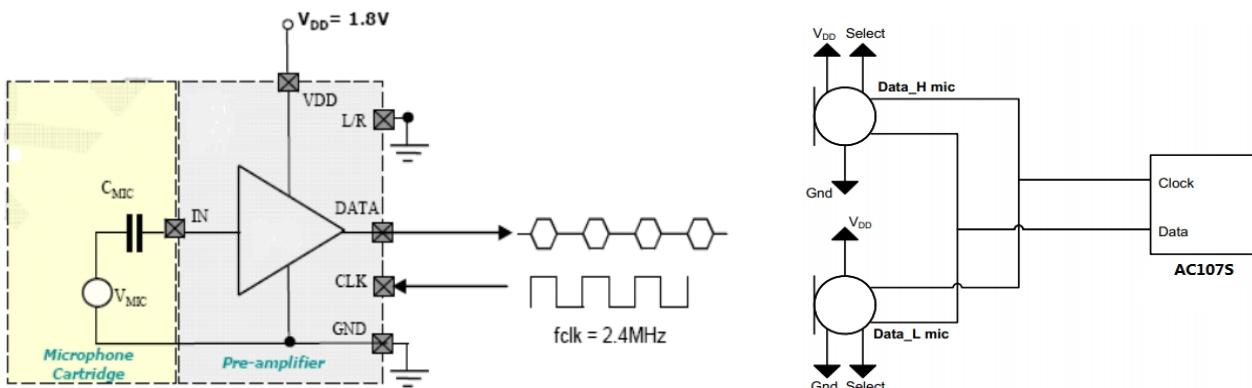


Figure 7-24. Digital Microphone Application

7.3.11 PDM Output Interface

AC107 supports a single bit PDM(Pulse Density Modulation) output interface to transit the ADC channel data. The ADC1 data outputs during the clock low period and then turns high impedance during the high period. The ADC2 data operates in a similar way, but outputs valid data on the high clock phase. The key thing here is that the High Z state needs to occur before valid data to ensure no bus contention occurs. Also note there is a small window to sample data. It is essential that every valid data bit is sampled to avoid errors. PDM output timing as below:

Table 7-8. PDM output Timing requirement

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|--------------------------------------|------------------------------------|---|---------------|-----|---------------|-------|
| Clock Frequency Range | f_{CLOCK} | | 1.024 | - | 3.072 | MHz |
| Digital power for digital I/O buffer | V_{IO} | | 1.64 | 1.8 | 2.86 | V |
| Logic Input High | V_{IH} | | 0.65 V_{IO} | - | $V_{IO}+0.3$ | V |
| Logic Input Low | V_{IL} | | -0.3 | - | 0.35 V_{IO} | V |
| Clock Duty Cycle | $f_{CLOCK} \leq 2.475 \text{ MHz}$ | | 40 | - | 60 | % |
| | | $2.475\text{MHz} \leq f_{CLOCK} \leq 3.072 \text{ MHz}$ | 48 | 50 | 52 | % |
| Delay Time for Data Assertion | t_{DD} | | 18 | 28 | 40 | ns |
| Delay Time for High Z | t_{DZ} | | 3 | - | 16 | ns |

Table 7-9. PDM input clock

| $F_s(\text{kHz})$ | 8 | 12 | 11.025 | 16 | 22.05 | 24 | 32 | 44.1 | 48 |
|-------------------|------|------|--------|------|--------|------|------|--------|------|
| PDMCLK(kHz) | 1024 | 1536 | 1411.2 | 2048 | 2822.4 | 3072 | 2048 | 2822.4 | 3072 |

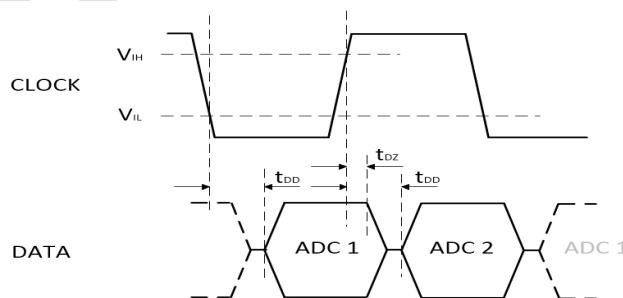


Figure 7-25. PDM Timing Diagram

7.4 Basic Setup Sequences

AC107 configuration: I2S Slave, I2S Justified mode, MCLK=12.288MHz, BCLK=1.024MHz, LRCK=16KHz, 2 channel, 32bit Slot width, 24bit Sample resolution.

2-ADC 16KHz Record setup sequence:

```
Reg[0x00] = 0x12; //reset to default status  
Reg[0x01] = 0x80; //verf enable, verf fast startup enable  
Reg[0x02] = 0x55; //MICBIAS enable  
Reg[0x21] = 0x07; //Module clock enable<I2S, ADC digital, ADC analog>  
Reg[0x22] = 0x03; //Module reset de-asserted<I2S, ADC digital>  
Reg[0xA4] = 0x40;//enable ADC1 analog part  
Reg[0xA9] = 0x40;//enable ADC2 analog part  
Reg[0x20] = 0x01;//system clock enable  
Reg[0x30] = 0x15; //I2S TX enable & I2S slave  
Reg[0x33] = 0x1F; //set LRCK_PERIODL=32*BCLK width  
Reg[0x34] = 0x15; //set I2S format: I2S Justified mode  
Reg[0x35] = 0x75;//set Slot width=32-bit, Sample resolution=24-bit  
Reg[0x38] = 0x01; //set I2S TX Channel (slot) number: 2  
Reg[0x39] = 0x03; //I2S TX Channel 1 ~ Channel 2 (slot) enable  
Reg[0x3C] = 0x02; //I2S TX mapping  
Reg[0x60] = 0x03; //set ADC Sample Rate: 16KHz  
Reg[0x61] = 0x07; //enable ADC digital part  
Reg[0x66] = 0x03; //enable HPF  
Reg[0xA2] = 0x19;//ADC1 Analog PGA Gain: 24dB  
Reg[0xA7] = 0x19;//ADC2 Analog PGA Gain: 24dB  
Reg[0x01] = 0xA0; //verf enable, verf fast startup disable
```

7.5 Register Maps

| Register Name | Offset | Description |
|-------------------|--------|--|
| CHIP_AUDIO_RST | 0x00 | Soft Reset Register |
| PWR_CTRL1 | 0x01 | Power Control 1 Register |
| PWR_CTRL2 | 0x02 | Power Control 2 Register |
| PLL_CTRL1 | 0x10 | PLL Configure Control 1 Register |
| PLL_CTRL2 | 0x11 | PLL Configure Control 2 Register |
| PLL_CTRL3 | 0x12 | PLL Configure Control 3 Register |
| PLL_CTRL4 | 0x13 | PLL Configure Control 4 Register |
| PLL_CTRL5 | 0x14 | PLL Configure Control 5 Register |
| PLL_CTRL6 | 0x16 | PLL Configure Control 6 Register |
| PLL_CTRL7 | 0x17 | PLL Configure Control 7 Register |
| PLL_LOCK_CTRL | 0x18 | PLL Configure Control 8 Register |
| SYSCLK_CTRL | 0x20 | System Clock Control Register |
| MOD_CLK_EN | 0x21 | Module Clock Enable Control Register |
| MOD_RST_CTRL | 0x22 | Module Reset Control Register |
| I2S_CTRL | 0x30 | I2S Control Register |
| I2S_BCLK_CTRL | 0x31 | I2S BCLK Configure Register |
| I2S_LRCK_CTRL1 | 0x32 | I2S LRCK Configure 1 Register |
| I2S_LRCK_CTRL2 | 0x33 | I2S LRCK Configure 2 Register |
| I2S_FMT_CTRL1 | 0x34 | I2S Format Configure 1 Register |
| I2S_FMT_CTRL2 | 0x35 | I2S Format Configure 2 Register |
| I2S_FMT_CTRL3 | 0x36 | I2S Format Configure 3 Register |
| I2S_TX_CTRL1 | 0x38 | I2S TX Control 1 Register |
| I2S_TX_CTRL2 | 0x39 | I2S TX Control 2 Register |
| I2S_TX_CTRL3 | 0x3A | I2S TX Control 3 Register |
| I2S_TX_CHMP_CTRL1 | 0x3C | I2S TX Channel Mapping Control 1 Register |
| I2S_TX_CHMP_CTRL2 | 0x3D | I2S TX Channel Mapping Control 2 Register |
| I2S_RX_CTRL1 | 0x50 | I2S RX Control 1 Register |
| I2S_RX_CTRL2 | 0x51 | I2S RX Control 2 Register |
| I2S_RX_CTRL3 | 0x52 | I2S RX Control 3 Register |
| I2S_RX_CHMP_CTRL1 | 0x54 | I2S RX Channel Mapping Control 1 Register |
| I2S_RX_CHMP_CTRL2 | 0x55 | I2S RX Channel Mapping Control 2 Register |
| PDM_CTRL | 0x59 | PDM Control Register |
| ADC_SPRC | 0x60 | ADC Sample Rate Select Register |
| ADC_DIG_EN | 0x61 | ADC Digital Part Enable Register |
| HPF_EN | 0x66 | Digital HPF Enable Register |
| ADC1_DVOL_CTRL | 0x70 | ADC1 Digital Channel Volume Control Register |
| ADC2_DVOL_CTRL | 0x71 | ADC2 Digital Channel Volume Control Register |
| ADC1_DMIX_SRC | 0x76 | ADC1 Digital Mixer Source Control Register |
| ADC2_DMIX_SRC | 0x77 | ADC2 Digital Mixer Source Control Register |
| ADC_DIG_DEBUG | 0x7F | ADC Digital Debug Control Register |

| | | |
|-----------------|------|-------------------------------------|
| ADC_ANA_DEBUG2 | 0x81 | ADC Analog Debug Control 2 Register |
| I2S_PADDRV_CTRL | 0x82 | I2S Pad Drive Control Register |
| DIG_ADC_CTRL | 0x83 | ADC Digital Control Register |
| ANA_ADC1_CTRL1 | 0xA0 | ADC1 Analog Control 1 Register |
| ANA_ADC1_CTRL2 | 0xA1 | ADC1 Analog Control 2 Register |
| ANA_ADC1_CTRL3 | 0xA2 | ADC1 Analog Control 3 Register |
| ANA_ADC1_CTRL4 | 0xA3 | ADC1 Analog Control 4 Register |
| ANA_ADC1_CTRL5 | 0xA4 | ADC1 Analog Control 5 Register |
| ANA_ADC2_CTRL1 | 0xA5 | ADC2 Analog Control 1 Register |
| ANA_ADC2_CTRL2 | 0xA6 | ADC2 Analog Control 2 Register |
| ANA_ADC2_CTRL3 | 0xA7 | ADC2 Analog Control 3 Register |
| ANA_ADC2_CTRL4 | 0xA8 | ADC2 Analog Control 4 Register |
| ANA_ADC2_CTRL5 | 0xA9 | ADC2 Analog Control 5 Register |
| ADC_DITHER_CTRL | 0xAA | ADC Dither Control Register |

Reg 00h_Chip Soft Reset Register

| Default: 0x4B | | | Register Name: CHIP_AUDIO_RST |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:0 | R/W | 0x4B | Reading this register will indicate device type and version. Writing this register 0x12 resets all register to their default state. |

Reg 01h_Power Control 1 Register

| Default: 0x00 | | | Register Name: PWR_CTRL1 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7 | R/W | 0 | VREF_ENABLE VREF Enable 0 = Disable 1 = Enable |
| 6 | R/W | 0 | VREF_LPMODE VREF Low Power Mode Control 0: Normal 1: Low Power |
| 5 | R/W | 0 | VREF_FSU_DISABLE VREF Fast Start Up Disable 0: Enable 1: Disable |
| 4:3 | R/W | 0 | VREF_RESCTRL VREF Output Resistor Control 00: 1M Ohm 01: 2.2k Ohm 10: 10M Ohm |

| | | | |
|-----|-----|---|---|
| | | | 11: 100k Ohm |
| 2:0 | R/W | 0 | IGEN_TRIM Tune bias current generator for all audio input channels 000=Nominal (5uA) 001=-4.8% 010=-9.1% 011=-13% 100=+25% 101=+17.6% 110=+11% 111=+5.2% |

Reg 02h_Power Control 2 Register

| Default: 0x11 | | | Register Name: PWR_CTRL2 |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7 | R/W | 0 | VREF_SEL VREF Source Selection 0: From BandGap 1: From AVCC |
| 6 | R/W | 0 | MICBIAS2_EN MICBIAS2 Enable 0: Disable 1: Enable |
| 5:4 | R/W | 1 | MICBIAS2_VCTRL MICBIAS2 Voltage Control 00: 1.8V 01: 2.1V 10: 2.4V 11: 3V |
| 3 | / | / | / |
| 2 | R/W | 0 | MICBIAS1_EN MICBIAS1 Enable 0: Disable 1: Enable |
| 1:0 | R/W | 1 | MICBIAS1_VCTRL MICBIAS1 Voltage Control 00: 1.8V 01: 2.1V 10: 2.4V 11: 3V |

Reg 10h_PLL Configure Control 1 Register

| Default: 0x48 | | | Register Name: PLL_CTRL1 |
|---------------|------------|---------|--------------------------|
| Bit | Read/Write | Default | Description |

| | | | |
|-----|-----|-----|---|
| 7 | / | / | / |
| 6:4 | R/W | 0x4 | PLL_IBIAS PLL internal bias current tuning 0: min ... 7: max |
| 3 | R/W | 0x1 | PLL_NDET PLL loop divider factor detection 0: Disable 1: Enable |
| 2 | R | 0x0 | PLL_Locked status 0: Not locked or not enabled 1: Enabled and locked |
| 1 | R/W | 0x0 | PLL_COM_EN PLL Common voltage Enable 0: Disable 1: Enable |
| 0 | R/W | 0x0 | PLL_EN PLL Enable 0: Disable 1: Enable The PLL output FOUT= FIN*N/((M1+1)*(M2+1)*(K1+1)*(K2+1)); |

Reg 11h_PLL Configure Control 2 Register

| Default: 0x00 | | | Register Name: PLL_CTRL2 |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:6 | / | / | / |
| 5 | R/W | 0x0 | PLL_PREDIV2 PLL pre-divider factor M2 Factor=0, M2=0 Factor=1, M2=1 |
| 4:0 | R/W | 0x0 | PLL_PREDIV1 PLL pre-divider factor M1 Factor=0, M1=0 Factor=1, M1=1 ... Factor=31, M1=31 |

Reg 12h_PLL Configure Control 3 Register

| Default: 0x03 | | | Register Name: PLL_CTRL3 |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:2 | / | / | / |
| 1:0 | R/W | 0x3 | PLL_LOOPDIV_MSB The 2-High Bit of PLL Loop Divider Factor N. |

| | | | |
|--|--|--|---|
| | | | Factor=0, N=0 Factor=1, N=1 ... Factor=1023, N=1023 Factor N is equal to [PLL_LOOPDIV_MSB, PLL_LOOPDIV_LSB] |
|--|--|--|---|

Reg 13h_PLL Configure Control 4 Register

| Default: 0x0D | | | Register Name: PLL_CTRL4 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:0 | R/W | 0x0D | PLL_LOOPDIV LSB The 8-Low Bit of PLL PLL Loop Divider Factor N. Factor=0, N=0 Factor=1, N=1 ... Factor=1023, N=1023 Factor N is equal to [PLL_LOOPDIV_MSB, PLL_LOOPDIV_LSB] |

Reg 14h_PLL Configure Control 5 Register

| Default: 0x00 | | | Register Name: PLL_CTRL5 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:6 | / | / | / |
| 5 | R/W | 0x0 | PLL_POSTDIV2 PLL post-divider factor K2 Factor=0, K2=0 Factor=1, K2=1 |
| 4:0 | R/W | 0x0 | PLL_POSTDIV1 PLL post-divider factor K1 Factor=0, K1=0 Factor=1, K1=1 ... Factor=31, K1=31 |

Reg 16h_PLL Configure Control 6 Register

| Default: 0x0F | | | Register Name: PLL_CTRL6 |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:6 | R/W | 0x0 | PLL_LDO PLL internal ldo voltage tuning 00: 1.8V 01: 2.0V 10: 2.2V 11: 2.4V |
| 5 | / | / | / |
| 4:0 | R/W | 0xF | PLL_CP PLL pll cp current tuning |

| | | | |
|--|--|--|--------------------------|
| | | | 0: min ... 31: max |
|--|--|--|--------------------------|

Reg 17h_PLL Configure Control 7 Register

| Default: 0xD0 | | | Register Name: PLL_CTRL7 |
|----------------------|-------------------|----------------|--|
| Bit | Read/Write | Default | Description |
| 7:6 | R/W | 0x3 | PLL_CAP PLL loop filter capacitance tuning 0: min ... 3: max |
| 5:4 | R/W | 0x1 | PLL_RES PLL loop filter resistance tuning 0: min ... 3: max |
| 3:0 | / | / | / |

Reg 18h_PLL Configure Control 8 Register

| Default: 0x00 | | | Register Name: PLL_LOCK_CTRL |
|----------------------|-------------------|----------------|--|
| Bit | Read/Write | Default | Description |
| 7 | / | / | / |
| 6:4 | R/W | 0x0 | HOLD_TIME SYSCLK hold time T T=0, Bypass T=1, 1 LRCK width ... T=7, 7 LRCK width |
| 3:2 | R/W | 0x0 | LOCK_LEVEL1 PLL lock level1 00: 21-29 clock cycles 01: 22-28 clock cycles 1x: 20-30 clock cycles |
| 1 | R/W | 0x0 | LOCK_LEVEL2 PLL lock level2 0: 24-26 clock cycles 1: 23-27 clock cycles |
| 0 | R/W | 0x0 | PLL_LOCK_EN PLL clk lock enable 0: disable 1: enable |

Reg 20h_System Clock Control Register

| Default: 0x00 | | | Register Name: SYSCLK_CTRL |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7 | R/W | 0x0 | PLLCLK_EN PLLCLK Enable 0: Disable 1: Enable |
| 6 | / | / | / |
| 5:4 | R/W | 0x0 | PLLCLK_SRC PLL Clock Source Select 0: MCLK 1: BCLK 2: PDMCLK 3: Reserved |
| 3:2 | R/W | 0x0 | SYSCLK_SRC System Clock Source Select 0: MCLK 1: BCLK 2: PLL 3: Reserved |
| 1 | / | / | / |
| 0 | R/W | 0x0 | SYSCLK_EN SYSCLK Enable 0: Disable 1: Enable |

Reg 21h_Module Clock Enable Control Register

| Default: 0x00 | | | Register Name: MOD_CLK_EN |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:3 | / | / | / |
| 2:0 | R/W | 0x0 | Module clock enable control 0-Clock disable 1-Clock enable BIT2- ADC analog BIT1- ADC digital BIT0- I2S |

Reg 22h_Module Reset Control Register

| Default: 0x00 | | | Register Name: MOD_RST_CTRL |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:5 | / | / | / |
| 4 | R/W | 0x0 | Connect Globe Enable to I2S reset control 0: Enable |

| | | | |
|-----|-----|-----|---|
| | | | 1: Disable |
| 3:2 | / | / | / |
| 1:0 | R/W | 0x0 | Module reset control 0-Reset asserted 1-Reset de-asserted BIT1- ADC digital BIT0- I2S |

Reg 30h_I2S Control Register

| Default: 0x00 | | | Register Name: I2S_CTRL |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7 | R/W | 0x0 | BCLK_IOEN 0: Input 1: Output |
| 6 | R/W | 0x0 | LRCK_IOEN 0: Input 1: Output |
| 5 | R/W | 0x0 | MCLK_IOEN 0: Input 1: Output PLL_test |
| 4 | R/W | 0x0 | SDO_EN 0: Disable, Hi-Z state 1: Enable |
| 3 | / | / | / |
| 2 | R/W | 0x0 | TXEN Transmitter Block Enable 0: Disable 1: Enable |
| 1 | R/W | 0x0 | RXEN Receiver Block Enable 0: Disable 1: Enable |
| 0 | R/W | 0x0 | GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable |

Reg 31h_I2S BCLK Configure Register

| Default: 0x00 | | | Register Name: I2S_BCLK_CTRL |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:6 | / | / | / |
| 5 | R/W | 0x0 | EDGE_TRANSFER 0: SDO drive data and SDI sample data at the different BCLK edge |

| | | | |
|-----|-----|-----|--|
| | | | 1: SDO drive data and SDI sample data at the same BCLK edge |
| 4 | R/W | 0x0 | BCLK_POLARITY 0: normal mode, negative edge drive 1: invert mode, positive edge drive |
| 3:0 | R/W | 0x0 | BCLKDIV BCLK Divide Ratio from SYSCLK 0: reserved 1: Divide by 1 2: Divide by 2 3: Divide by 4 4: Divide by 6 5: Divide by 8 6: Divide by 12 7: Divide by 16 8: Divide by 24 9: Divide by 32 10: Divide by 48 11: Divide by 64 12: Divide by 96 13: Divide by 128 14: Divide by 176 15: Divide by 192 This bit is only used in master mode |

Reg 32h_I2S_LRCK Configure 1 Register

| Default: 0x00 | | | Register Name: I2S_LRCK_CTRL1 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:5 | / | / | / |
| 4 | R/W | 0x0 | LRCK_POLARITY When apply in I2S / Left-Justified / Right-Justified mode: 0: Left channel when LRCK is low 1: Left channel when LRCK is high When apply in PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge |
| 3:2 | / | / | / |
| 1:0 | R/W | 0x0 | LRCK_PERIODH The 2-High bit of LRCK period value. It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM mode: Number of BCLKs within (Left + Right) channel width I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) N+1 For example: n = 7: 8 BCLKs width |

| | | | |
|--|--|--|--|
| | | | <p>...</p> <p>n = 1023: 1024 BCLKs width</p> <p>This bit is must be configured in master or slave mode</p> |
|--|--|--|--|

Reg 33h_I2S LRCK Configure 2 Register

| Default: 0x00 | | | Register Name: I2S_LRCK_CTRL2 |
|----------------------|-------------------|----------------|---|
| Bit | Read/Write | Default | Description |
| 7:0 | R/W | 0x0 | <p>LRCK_PERIODL The 8-Low bit of LRCK period value. It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM mode: Number of BCLKs within (Left + Right) channel width I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) N+1 For example: n = 7: 8 BCLKs width ... n = 1023: 1024 BCLKs width This bit is must be configured in master or slave mode</p> |

Reg 34h_I2S Format Configure 1 Register

| Default: 0x00 | | | Register Name: I2S_FMT_CTRL1 |
|----------------------|-------------------|----------------|--|
| Bit | Read/Write | Default | Description |
| 7 | R/W | 0x0 | <p>ENCD_FMT Encoding Mode coding format Selection 0: 0,1,...,N-1 1: 1,2,...,N N is the channel (slot) number</p> |
| 6 | R/W | 0x0 | <p>ENCD_SEL Encoding Mode Selection 0: disable 1: enable</p> |
| 5:4 | R/W | 0x0 | <p>MODE_SEL Mode Selection 0: PCM mode (offset 0: PCM_B; offset 1: PCM_A) 1: Left-Justified mode (offset 0: LJ mode; offset 1: I2S mode) 2: Right-Justified mode 3: Reserved</p> |
| 3 | / | / | / |
| 2 | R/W | 0x0 | <p>TX_OFFSET TX offset tune, TX data offset to LRCK 0: no offset 1: data is offset by 1 BCLKs to LRCK</p> |
| 1 | R/W | 0x0 | TX_SLOT_HIZ |

| | | | |
|---|-----|-----|---|
| | | | 0: normal mode for the last half cycle of BCLK in the slot 1: turn to hi-z state for the last half cycle of BCLK in the slot |
| 0 | R/W | 0x0 | TX_STATE 0: transfer level 0 when not transferring slot 1: turn to hi-z state (TDM) when not transferring slot |

Reg 35h_I2S Format Configure 2 Register

| Default: 0x55 | | | Register Name: I2S_FMT_CTRL2 |
|----------------------|-------------------|----------------|---|
| Bit | Read/Write | Default | Description |
| 7 | / | / | / |
| 6:4 | R/W | 0x5 | SW Slot Width Select 0: Reserved 1: Reserved 2: Reserved 3: 16-bit 4: 20-bit 5: 24-bit 6: 28-bit 7: 32-bit |
| 3 | / | / | / |
| 2:0 | R/W | 0x5 | SR Sample Resolution 0: Reserved 1: Reserved 2: Reserved 3: 16-bit 4: 20-bit 5: 24-bit 6: 28-bit 7: 32-bit |

Reg 36h_I2S Format Configure 3 Register

| Default: 0x60 | | | Register Name: I2S_FMT_CTRL3 |
|----------------------|-------------------|----------------|--|
| Bit | Read/Write | Default | Description |
| 7 | R/W | 0x0 | TX MLS MSB / LSB First Select 0: MSB First 1: LSB First |
| 6:5 | R/W | 0x3 | SEXT Sign Extend in slot [sample resolution < slot width] 0: Zeros or audio gain padding at LSB position 1: Sign extension at MSB position 2: Reserved |

| | | | |
|-----|-----|-----|---|
| | | | 3: Transfer 0 after each sample in each slot |
| 4 | / | / | / |
| 3 | R/W | 0x0 | SDOUT Mute 0: normal transfer 1: force DOUT to output 0 |
| 2 | R/W | 0x0 | LRCK_WIDTH LRCK width 0: LRCK = 1 BCLK width (short frame) 1: LRCK = 2 BCLK width (long frame) (this bit is only used in PCM mode) |
| 1:0 | R/W | 0x0 | TX_PDM PCM Data Mode 0: Linear PCM 1: reserved 2: 8-bits u-law 3: 8-bits A-law (this bit is only used in PCM mode) |

Reg 38h_I2S TX Control 1 Register

| Default: 0x00 | | | Register Name: I2S_TX_CTRL1 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:4 | / | / | / |
| 3:0 | R/W | 0x0 | TX_CHSEL TX Channel (slot) number Select for each output 0: 1 channel (slot) ... 7: 8 channels (slots) 8: 9 channels (slots) ... 15: 16 channels (slots) |

Reg 39h_I2S TX Control 2 Register

| Default: 0x00 | | | Register Name: I2S_TX_CTRL2 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:0 | R/W | 0x0 | TX_CHEN_LOW TX Channel1 ~Channel8 (slot) enable, bit[7:0] refer to slot [8:1]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state 0: disable 1: enable |

Reg 3Ah_I2S TX Control 3 Register

| Default: 0x00 | | | Register Name: I2S_TX_CTRL3 |
|---------------|------------|---------|-----------------------------|
| Bit | Read/Write | Default | Description |
| 7:0 | R/W | 0x0 | TX_CHEN_HIGH |

| | | | |
|--|--|--|---|
| | | | TX Channel9 ~Channel16(slot) enable, bit[7:0] refer to slot [16:9]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state 0: disable 1: enable |
|--|--|--|---|

Reg 3Ch_I2S TX Channel Mapping Control 1 Register

| Default: 0x00 | | | Register Name: I2S_TX_CHMP_CTRL1 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7 | R/W | 0x0 | TX_CH8_MAP TX Channel8 Mapping 0: 1st adc sample 1: 2th adc sample |
| 6 | R/W | 0x0 | TX_CH7_MAP TX Channel7 Mapping 0: 1st adc sample 1: 2th adc sample |
| 5 | R/W | 0x0 | TX_CH6_MAP TX Channel6 Mapping 0: 1st adc sample 1: 2th adc sample |
| 4 | R/W | 0x0 | TX_CH5_MAP TX Channel5 Mapping 0: 1st adc sample 1: 2th adc sample |
| 3 | R/W | 0x0 | TX_CH4_MAP TX Channel4 Mapping 0: 1st adc sample 1: 2th adc sample |
| 2 | R/W | 0x0 | TX_CH3_MAP TX Channel3 Mapping 0: 1st adc sample 1: 2th adc sample |
| 1 | R/W | 0x0 | TX_CH2_MAP TX Channel2 Mapping 0: 1st adc sample 1: 2th adc sample |
| 0 | R/W | 0x0 | TX_CH1_MAP TX Channel1 Mapping 0: 1st adc sample 1: 2th adc sample |

Reg 3Dh_I2S TX Channel Mapping Control 2 Register

| Default: 0x00 | | | Register Name: I2S_TX_CHMP_CTRL2 |
|---------------|------------|---------|----------------------------------|
| Bit | Read/Write | Default | Description |

| | | | |
|---|-----|-----|---|
| 7 | R/W | 0x0 | TX_CH16_MAP TX Channel16 Mapping 0: 1st adc sample 1: 2th adc sample |
| 6 | R/W | 0x0 | TX_CH15_MAP TX Channel15 Mapping 0: 1st adc sample 1: 2th adc sample |
| 5 | R/W | 0x0 | TX_CH14_MAP TX Channel14 Mapping 0: 1st adc sample 1: 2th adc sample |
| 4 | R/W | 0x0 | TX_CH13_MAP TX Channel13 Mapping 0: 1st adc sample 1: 2th adc sample |
| 3 | R/W | 0x0 | TX_CH12_MAP TX Channel12 Mapping 0: 1st adc sample 1: 2th adc sample |
| 2 | R/W | 0x0 | TX_CH11_MAP TX Channel11 Mapping 0: 1st adc sample 1: 2th adc sample |
| 1 | R/W | 0x0 | TX_CH10_MAP TX Channel10 Mapping 0: 1st adc sample 1: 2th adc sample |
| 0 | R/W | 0x0 | TX_CH9_MAP TX Channel9 Mapping 0: 1st adc sample 1: 2th adc sample |

Reg 50h_I2S RX Control 1 Register

| Default: 0x00 | | | Register Name: I2S_RX_CTRL1 |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:4 | / | / | / |
| 3:0 | R/W | 0x0 | RX_CHSEL RX Channel (slot) number Select for each input 0: 1 channel (slot) ... 7: 8 channels (slots) 8: 9 channels (slots) ... 15: 16 channels (slots) |

Reg 51h_I2S RX Control 2 Register

| Default: 0x03 | | | Register Name: I2S_RX_CTRL2 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:0 | R/W | 0x3 | <p>RX_CHEN_LOW RX Channel1 ~Channel8 (slot) enable, bit[7:0] refer to slot [8:1]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state 0: disable 1: enable</p> |

Reg 52h_I2S RX Control 3 Register

| Default: 0x00 | | | Register Name: I2S_RX_CTRL3 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:0 | R/W | 0x0 | <p>RX_CHEN_HIGH RX Channel9 ~Channel16(slot) enable, bit[7:0] refer to slot [16:9]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state 0: disable 1: enable</p> |

Reg 54h_I2S RX Channel Mapping Control 1 Register

| Default: 0x00 | | | Register Name: I2S_RX_CHMP_CTRL1 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7 | R/W | 0x0 | <p>RX_CH8_MAP RX Channel8 Mapping 0: 1st adc sample 1: 2th adc sample</p> |
| 6 | R/W | 0x0 | <p>RX_CH7_MAP RX Channel7 Mapping 0: 1st adc sample 1: 2th adc sample</p> |
| 5 | R/W | 0x0 | <p>RX_CH6_MAP RX Channel6 Mapping 0: 1st adc sample 1: 2th adc sample</p> |
| 4 | R/W | 0x0 | <p>RX_CH5_MAP RX Channel5 Mapping 0: 1st adc sample 1: 2th adc sample</p> |
| 3 | R/W | 0x0 | <p>RX_CH4_MAP RX Channel4 Mapping 0: 1st adc sample 1: 2th adc sample</p> |
| 2 | R/W | 0x0 | <p>RX_CH3_MAP RX Channel3 Mapping</p> |

| | | | |
|---|-----|-----|---|
| | | | 0: 1st adc sample 1: 2th adc sample |
| 1 | R/W | 0x0 | RX_CH2_MAP RX Channel2 Mapping 0: 1st adc sample 1: 2th adc sample |
| 0 | R/W | 0x0 | RX_CH1_MAP RX Channel1 Mapping 0: 1st adc sample 1: 2th adc sample |

Reg 55h_I2S RX Channel Mapping Control 2 Register

| Default: 0x00 | | | Register Name: I2S_RX_CHMP_CTRL2 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7 | R/W | 0x0 | RX_CH16_MAP RX Channel16 Mapping 0: 1st adc sample 1: 2th adc sample |
| 6 | R/W | 0x0 | RX_CH15_MAP RX Channel15 Mapping 0: 1st adc sample 1: 2th adc sample |
| 5 | R/W | 0x0 | RX_CH14_MAP RX Channel14 Mapping 0: 1st adc sample 1: 2th adc sample |
| 4 | R/W | 0x0 | RX_CH13_MAP RX Channel13 Mapping 0: 1st adc sample 1: 2th adc sample |
| 3 | R/W | 0x0 | RX_CH12_MAP RX Channel12 Mapping 0: 1st adc sample 1: 2th adc sample |
| 2 | R/W | 0x0 | RX_CH11_MAP RX Channel11 Mapping 0: 1st adc sample 1: 2th adc sample |
| 1 | R/W | 0x0 | RX_CH10_MAP RX Channel10 Mapping 0: 1st adc sample 1: 2th adc sample |
| 0 | R/W | 0x0 | RX_CH9_MAP RX Channel9 Mapping 0: 1st adc sample |

| | | |
|--|--|-------------------|
| | | 1: 2th adc sample |
|--|--|-------------------|

Reg 59h_PDM Control Register

| Default: 0x00 | | | Register Name: PDM_CTRL |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:2 | / | / | / |
| 1 | R/W | 0x0 | PDM_TIMING PDM timing control 0: Latch ADC1 data on rising clock edge. Latch ADC2 data on falling clock edge. 1: Latch ADC1 data on falling clock edge. Latch ADC2 data on rising clock edge. |
| 0 | R/W | 0x0 | PDM_EN PDM interface Enable 0: Disable 1: Enable When PDM_EN = 1, LRCK is used for PDMCLK input and SDOUT is used for PDMDATA output. |

Reg 60h_ADC Sample Rate Select Register

| Default: 0x00 | | | Register Name: ADC_SPRC |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:4 | / | / | / |
| 3:0 | R/W | 0x0 | ADC_FS_I2S ADC Sample Rate synchronized with I2S clock zone 0000: 8KHz 0001: 11.025KHz 0010: 12KHz 0011: 16KHz 0100: 22.05KHz 0101: 24KHz 0110: 32KHz 0111: 44.1KHz 1000: 48KHz Other: Reserved |

Reg 61h_ADC Digital Part Enable Register

| Default: 0x00 | | | Register Name: ADC_DIG_EN |
|---------------|------------|---------|-------------------------------------|
| Bit | Read/Write | Default | Description |
| 7:4 | R/W | 0x0 | REQ_WIDTH 0:min ... 15:max |
| 3 | R/W | 0x0 | REQ_EN |

| | | | |
|---|-----|-----|---|
| | | | 0: Disable 1: Enable |
| 2 | R/W | 0x0 | DG_EN ADC Digital part globe enable 0: Disable 1: Enable |
| 1 | R/W | 0x0 | ENAD2 ADC2 digital part enable 0: Disable 1: Enable |
| 0 | R/W | 0x0 | ENAD1 ADC1 digital part enable 0: Disable 1: Enable |

Reg 66h_Digital HPF Enable Register

| Default: 0x03 | | | Register Name: HPF_EN |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:2 | / | / | / |
| 1 | R/W | 0x1 | DIG_ADC2_HPF_EN Digital ADC2 channel HPF enable 0: Disable 1: Enable |
| 0 | R/W | 0x1 | DIG_ADC1_HPF_EN Digital ADC1 channel HPF enable 0: Disable 1: Enable |

Reg 70h_ADC1 Digital Channel Volume Control Register

| Default: 0xA0 | | | Register Name: ADC1_DVOL_CTRL |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:0 | R/W | 0xA0 | DIG_ADCL1_VOL ADC1 Digital channel volume Control (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB 0xFF = 71.25dB |

Reg 71h_ADC2 Digital Channel Volume Control Register

| Default: 0xA0 | | | Register Name: ADC2_DVOL_CTRL |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7:0 | R/W | 0xA0 | <p>DIG_ADCL2_VOL ADC2 Digital channel volume Control (-119.25dB To 71.25dB, 0.75dB/Step)</p> <p>0x00: Mute 0x01: -119.25dB 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB 0xFF = 71.25dB</p> |

Reg 76h_ADC1 Digital Mixer Source Control Register

| Default: 0x01 | | | Register Name: ADC1_DMIX_SRC |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:4 | / | / | / |
| 3:2 | R/W | 0x0 | <p>ADC1_DMXL_GC ADC1 channel digital mixer gain control 0: 0dB 1: -6dB Bit3: ADC2 data Bit2: ADC1 data</p> |
| 1:0 | R/W | 0x1 | <p>ADC1_DMXL_SRC ADC1 channel digital mixer source select 0: Disable 1: Enable Bit1: ADC2 data Bit0: ADC1 data</p> |

Reg 77h_ADC2 Digital Mixer Source Control Register

| Default: 0x02 | | | Register Name: ADC2_DMIX_SRC |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:4 | / | / | / |
| 3:2 | R/W | 0x0 | <p>ADC2_DMXL_GC ADC2 channel digital mixer gain control 0: 0dB 1: -6dB Bit3: ADC2 data Bit2: ADC1 data</p> |
| 1:0 | R/W | 0x2 | <p>ADC2_DMXL_SRC ADC2 channel digital mixer source select 0: Disable 1: Enable Bit1: ADC2 data</p> |

| | | |
|--|--|-----------------|
| | | Bit0: ADC1 data |
|--|--|-----------------|

Reg 7Fh_ADC Digital Debug Control Register

| Default: 0x00 | | | Register Name: ADC_DIG_DEBUG |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:4 | / | / | / |
| 3 | R/W | 0x0 | I2S_LPB_DEBUG RX-> TXdata loopback 0: disable 1: enable |
| 2:0 | R/W | 0x0 | ADC_PTN_SEL ADC Pattern Select 000: Normal 001: 0x5A5A5A(24-bit) 010: 0x123456 (24-bit) 011: zero data 1xx: I2S_RX data When this bit selected, the digital path data source will be changed to internal rom data |

Reg 81h_ADC Analog Debug Control 2 Register

| Default: 0x11 | | | Register Name: ADC_ANA_DEBUG2 |
|---------------|------------|---------|---|
| Bit | Read/Write | Default | Description |
| 7 | / | / | / |
| 6:4 | R/W | 0x1 | Pad Select for DEV_ID1 PIN. 000: IO Disable 001: DEV_ID1 other: Reserved |
| 3 | / | / | / |
| 2:0 | R/W | 0x1 | Pad Select for DEV_ID0 PIN. 000: IO Disable 001: DEV_ID0 other: Reserved |

Reg 82h_I2S Pad Drive Control Register

| Default: 0x55 | | | Register Name: I2S_PADDRV_CTRL |
|---------------|------------|---------|--|
| Bit | Read/Write | Default | Description |
| 7:6 | R/W | 0x1 | Pad programmable drive control for MCLK. 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |
| 5:4 | R/W | 0x1 | Pad programmable drive control for BCLK. 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |

| | | | |
|-----|-----|-----|---|
| 3:2 | R/W | 0x1 | Pad programmable drive control for LRCK. 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |
| 1:0 | R/W | 0x1 | Pad programmable drive control for SDOUT. 00: Level 0 01: Level 1 10: Level 2 11: Level 3 |

Reg A0h_ADC1 Analog Control 1 Register

| Default:0x00 | | | Register Name: ANA_ADC1_CTRL1 |
|--------------|-----|---------|--|
| Bit | R/W | Default | Description |
| 7:5 | R/W | 0x0 | RX1_PGA_OI_CTRL Channel 1 PGA Output Current Driver Strength Control 0 = 30I 4 = 50I 1 = 25I 5 = 45I 2 = 40I 6 = 60I 3 = 35I 7 = 55I I = Bias current of OTA, default = 5uA |
| 4:2 | R/W | 0x0 | RX1_PGA_AMP_IB_SEL Channel 1 PGA Bias Current Control 0 = 5 uA 4 = 3 uA 1 = 5.5 uA 5 = 3.5 uA 2 = 6 uA 6 = 4 uA 3 = 6.5 uA 7 = 4.5 uA |
| 1:0 | R/W | 0x0 | RX1_PGA_IN_VCM_CTRL Channel 1 PGA High-gain Common-Mode Voltage Control 0 = 1.65V 1 = 1.45V 2 = 1.39V 3 = 1.29V when PGA work on low-gain(0/-6dB), the Common-Mode Voltage is fixed 1.65V. |

Reg A1h_ADC1 Analog Control 2 Register

| Default:0x00 | | | Register Name: ANA_ADC1_CTRL2 |
|--------------|-----|---------|--|
| Bit | R/W | Default | Description |
| 7:6 | / | / | / |
| 5:3 | R/W | 0x0 | RX1_PGA_OI_NM_CTRL Channel 1 PGA High Gain Output Current Driver Strength Control 0 = 21 I 4 = 33 I 1 = 24 I 5 = 36 I 2 = 15 I 6 = 27 I 3 = 18 I 7 = 30 I I = Bias current of OTA, default = 5uA |
| 2:0 | R/W | 0x0 | RX1_PGA_NMAMP_IB_SEL Channel 1 PGA High Gain Bias Current Control |

| | | | |
|--|--|--|--|
| | | | 0 = 5 uA 4 = 3 uA 1 = 5.5 uA 5 = 3.5 uA 2 = 6 uA 6 = 4 uA 3 = 6.5 uA 7 = 4.5 uA |
|--|--|--|--|

Reg A2h_ADC1 Analog Control 3 Register

| Default:0x00 | | | Register Name: ANA_ADC1_CTRL3 |
|---------------------|------------|----------------|---|
| Bit | R/W | Default | Description |
| 7 | / | / | / |
| 6:5 | R/W | 0x0 | RX1_PGA_CTRL_RCM Channel 1 high-gain PGA input impedance control 0 = 100 kΩ 1 = 75 kΩ 2 = 50 kΩ 3 = 25 kΩ when PGA work on 0dB/-6dB, the input impedance is 8K/16K. |
| 4:0 | R/W | 0x0 | RX1_PGA_GAIN_CTRL Channel 1 PGA gain settings: 0 = -6 dB 16 = 15 dB 1 = 0 dB 17 = 16 dB 2 = 0 dB 18 = 17 dB 3 = 0 dB 19 = 18 dB 4 = 3 dB 20 = 19 dB 5 = 4 dB 21 = 20 dB 6 = 5 dB 22 = 21 dB 7 = 6 dB 23 = 22 dB 8 = 7 dB 24 = 23 dB 9 = 8 dB 25 = 24 dB 10 = 9 dB 26 = 25 dB 11 = 10 dB 27 = 26 dB 12 = 11 dB 28 = 27 dB 13 = 12 dB 29 = 28 dB 14 = 13 dB 30 = 29 dB 15 = 14 dB 31 = 30 dB |

Reg A3h_ADC1 Analog Control 4 Register

| Default:0x00 | | | Register Name: ANA_ADC1_CTRL4 |
|---------------------|------------|----------------|---|
| Bit | R/W | Default | Description |
| 7:5 | R/W | 0x0 | RX1_DSM_OTA_IB_SEL Channel 1 DSM Integrator Bias Current Control 0 = 6 uA 4 = 4 uA 1 = 6.5 uA 5 = 4.5 uA 2 = 7 uA 6 = 5 uA 3 = 7.5 uA 7 = 5.5 uA |

| | | | |
|-----|-----|-----|---|
| 4:2 | R/W | 0x0 | RX1_DSM_COMP_IB_SEL Channel 1 DSM Comparator Bias Current Control 0 = 6 uA 4 = 4 uA 1 = 6.5 uA 5 = 4.5 uA 2 = 7 uA 6 = 5 uA 3 = 7.5 uA 7 = 5.5 uA |
| 1:0 | R/W | 0x0 | RX1_DSM_OTA_CTRL Channel 1 DSM Integrator Driver Strength Control 0 = 100% enabled 1 = 80% enabled 2 = 60% enabled 3 = 40% enabled |

Reg A4h_ADC1 Analog Control 5 Register

| Default:0x00 | | | Register Name: ANA_ADC1_CTRL5 |
|--------------|-----|---------|--|
| Bit | R/W | Default | Description |
| 7 | / | / | / |
| 6 | R/W | 0x0 | RX1_GLOBAL_EN Channel 1 Global Enable 0 = Disable 1 = Enable |
| 5 | R/W | 0x0 | RX1_DSM_DISABLE Channel 1 DSM Disable 0 = Enable 1 = Disable |
| 4 | R/W | 0x0 | RX1_DSM_DEMOFF Channel 1 DSM DEM Control 0 = Enable DEM 1 = Disable DEM |
| 3 | R/W | 0x0 | RX1_SEL_OUT_EDGE ADC clocking edge Select 0 = DSM output is clocked on falling edge of input clock 1 = DSM output is clocked on rising edge of input clock |
| 2 | R/W | 0x0 | RX1_DSM_VRP_LPMODE Channel 1 VREFP Low Power Mode 0 = Normal 1 = Low Power Mode |
| 1:0 | R/W | 0x0 | RX1_DSM_VRP_OUTCTRL Channel 1 VREFP Output Strength Control 0 = 100% 1 = 75% 2 = 50% 3 = 25% |

Reg A5h_ADC2 Analog Control 1 Register

| Default:0x00 | | | Register Name: ANA_ADC2_CTRL1 |
|--------------|-----|---------|---|
| Bit | R/W | Default | Description |
| 7:5 | R/W | 0x0 | <p>RX2_PGA_OI_CTRL Channel 2 PGA Output Current Driver Strength Control 0 = 30I 4 = 50I 1 = 25I 5 = 45I 2 = 40I 6 = 60I 3 = 35I 7 = 55I I = Bias current of OTA, default = 5uA</p> |
| 4:2 | R/W | 0x0 | <p>RX2_PGA_AMP_IB_SEL Channel 2 PGA Bias Current Control 0 = 5 uA 4 = 3 uA 1 = 5.5 uA 5 = 3.5 uA 2 = 6 uA 6 = 4 uA 3 = 6.5 uA 7 = 4.5 uA</p> |
| 1:0 | R/W | 0x0 | <p>RX2_PGA_IN_VCM_CTRL Channel 2 PGA High-gain Common-Mode Voltage Control 0 = 1.65V 1 = 1.45V 2 = 1.39V 3 = 1.29V when PGA work on low-gain(0/-6dB), the Common-Mode Voltage is fixed 1.65V.</p> |

Reg A6h_ADC2 Analog Control 2 Register

| Default:0x00 | | | Register Name: ANA_ADC2_CTRL2 |
|--------------|-----|---------|---|
| Bit | R/W | Default | Description |
| 7:6 | / | / | / |
| 5:3 | R/W | 0x0 | <p>RX2_PGA_OI_NM_CTRL Channel 2 PGA High Gain Output Current Driver Strength Control 0 = 21 I 4 = 33 I 1 = 24 I 5 = 36 I 2 = 15 I 6 = 27 I 3 = 18 I 7 = 30 I I = Bias current of OTA, default = 5uA</p> |
| 2:0 | R/W | 0x0 | <p>RX2_PGA_NMAMP_IB_SEL Channel 2 PGA High Gain Bias Current Control 0 = 5 uA 4 = 3 uA 1 = 5.5 uA 5 = 3.5 uA 2 = 6 uA 6 = 4 uA 3 = 6.5 uA 7 = 4.5 uA</p> |

Reg A7h_ADC2 Analog Control 3 Register

| Default:0x00 | | | Register Name: ANA_ADC2_CTRL3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|---------|------------|---|---|---------|------------|---|--------|------------|---|--------|------------|---|--------|------------|---|--------|------------|---|--------|------------|---|--------|------------|---|--------|------------|---|--------|------------|---|--------|------------|----|--------|------------|----|---------|------------|----|---------|------------|----|---------|------------|----|---------|------------|----|---------|------------|
| Bit | R/W | Default | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | / | / | / | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6:5 | R/W | 0x0 | <p>RX2_PGA_CTRL_RCM Channel 2 high-gain PGA input impedance control 0 = 100 kΩ 1 = 75 kΩ 2 = 50 kΩ 3 = 25 kΩ</p> <p>when PGA work on 0dB/-6dB, the input impedance is 8K/16K.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4:0 | R/W | 0x0 | <p>RX2_PGA_GAIN_CTRL Channel 2 PGA gain settings:</p> <table> <tbody> <tr><td>0</td><td>= -6 dB</td><td>16 = 15 dB</td></tr> <tr><td>1</td><td>= 0 dB</td><td>17 = 16 dB</td></tr> <tr><td>2</td><td>= 0 dB</td><td>18 = 17 dB</td></tr> <tr><td>3</td><td>= 0 dB</td><td>19 = 18 dB</td></tr> <tr><td>4</td><td>= 3 dB</td><td>20 = 19 dB</td></tr> <tr><td>5</td><td>= 4 dB</td><td>21 = 20 dB</td></tr> <tr><td>6</td><td>= 5 dB</td><td>22 = 21 dB</td></tr> <tr><td>7</td><td>= 6 dB</td><td>23 = 22 dB</td></tr> <tr><td>8</td><td>= 7 dB</td><td>24 = 23 dB</td></tr> <tr><td>9</td><td>= 8 dB</td><td>25 = 24 dB</td></tr> <tr><td>10</td><td>= 9 dB</td><td>26 = 25 dB</td></tr> <tr><td>11</td><td>= 10 dB</td><td>27 = 26 dB</td></tr> <tr><td>12</td><td>= 11 dB</td><td>28 = 27 dB</td></tr> <tr><td>13</td><td>= 12 dB</td><td>29 = 28 dB</td></tr> <tr><td>14</td><td>= 13 dB</td><td>30 = 29 dB</td></tr> <tr><td>15</td><td>= 14 dB</td><td>31 = 30 dB</td></tr> </tbody> </table> | 0 | = -6 dB | 16 = 15 dB | 1 | = 0 dB | 17 = 16 dB | 2 | = 0 dB | 18 = 17 dB | 3 | = 0 dB | 19 = 18 dB | 4 | = 3 dB | 20 = 19 dB | 5 | = 4 dB | 21 = 20 dB | 6 | = 5 dB | 22 = 21 dB | 7 | = 6 dB | 23 = 22 dB | 8 | = 7 dB | 24 = 23 dB | 9 | = 8 dB | 25 = 24 dB | 10 | = 9 dB | 26 = 25 dB | 11 | = 10 dB | 27 = 26 dB | 12 | = 11 dB | 28 = 27 dB | 13 | = 12 dB | 29 = 28 dB | 14 | = 13 dB | 30 = 29 dB | 15 | = 14 dB | 31 = 30 dB |
| 0 | = -6 dB | 16 = 15 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | = 0 dB | 17 = 16 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | = 0 dB | 18 = 17 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | = 0 dB | 19 = 18 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | = 3 dB | 20 = 19 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | = 4 dB | 21 = 20 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | = 5 dB | 22 = 21 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | = 6 dB | 23 = 22 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | = 7 dB | 24 = 23 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | = 8 dB | 25 = 24 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | = 9 dB | 26 = 25 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | = 10 dB | 27 = 26 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | = 11 dB | 28 = 27 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | = 12 dB | 29 = 28 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | = 13 dB | 30 = 29 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 15 | = 14 dB | 31 = 30 dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Reg A8h_ADC2 Analog Control 4 Register

| Default:0x00 | | | Register Name: ANA_ADC2_CTRL4 |
|--------------|-----|---------|---|
| Bit | R/W | Default | Description |
| 7:5 | R/W | 0x0 | <p>RX2_DSM_OTA_IB_SEL Channel 2 DSM Integrator Bias Current Control 0 = 6 uA 4 = 4 uA 1 = 6.5 uA 5 = 4.5 uA 2 = 7 uA 6 = 5 uA 3 = 7.5 uA 7 = 5.5 uA</p> |
| 4:2 | R/W | 0x0 | <p>RX2_DSM_COMP_IB_SEL Channel 2 DSM Comparator Bias Current Control 0 = 6 uA 4 = 4 uA 1 = 6.5 uA 5 = 4.5 uA 2 = 7 uA 6 = 5 uA</p> |

| | | | |
|-----|-----|-----|--|
| | | | 3 = 7.5 uA 7 = 5.5 uA |
| 1:0 | R/W | 0x0 | RX2_DSM_OTA_CTRL Channel 2 DSM Integrator Driver Strength Control 0 = 100% enabled 1 = 80% enabled 2 = 60% enabled 3 = 40% enabled |

Reg A9h_ADC2 Analog Control 5 Register

| Default:0x00 | | | Register Name: ANA_ADC2_CTRL5 |
|--------------|-----|---------|--|
| Bit | R/W | Default | Description |
| 7 | / | / | / |
| 6 | R/W | 0x0 | RX2_GLOBAL_EN Channel 2 Global Enable 0 = Disable 1 = Enable |
| 5 | R/W | 0x0 | RX2_DSM_DISABLE Channel 2 DSM Disable 0 = Enable 1 = Disable |
| 4 | R/W | 0x0 | RX2_DSM_DEMOFF Channel 2 DSM DEM Control 0 = Enable DEM 1 = Disable DEM |
| 3 | R/W | 0x0 | RX2_SEL_OUT_EDGE Channel 2 ADC clocking edge Select 0 = DSM output is clocked on falling edge of input clock 1 = DSM output is clocked on rising edge of input clock |
| 2 | R/W | 0x0 | RX2_DSM_VRP_LPMODE Channel 2 VREFP Low Power Mode 0 = Normal 1 = Low Power Mode |
| 1:0 | R/W | 0x0 | RX2_DSM_VRP_OUTCTRL Channel 2 VREFP Output Strength Control 0 = 100% 1 = 75% 2 = 50% 3 = 25% |

Reg AAh_ADC Dither Control Register

| Default:0x00 | | | Register Name: ADC_DITHER_CTRL |
|--------------|-----|---------|--------------------------------|
| Bit | R/W | Default | Description |
| 7:6 | / | / | / |
| 5:4 | R/W | 0x0 | DSM_DITHER_CTRL |

| | | | |
|-----|-----|-----|--|
| | | | Control of the input pin: dsm_dither_sign and dsm_dither_data 00: single-stage shaped pseudorandom dither signal 01: original pseudorandom dither signal 10: offset voltage of the positive direction 11: offset voltage of the negative direction |
| 3 | R/W | 0x0 | DSM_DITHER_EN Dither Enable 0 = Disable 1 = Enable |
| 2:0 | R/W | 0x0 | DSM_DITHER_LVL Dither level control(Dither level is positive related to the ctrl bits) 000 have no level 1 is the mim level and 7 is the max level |

8 Application Information

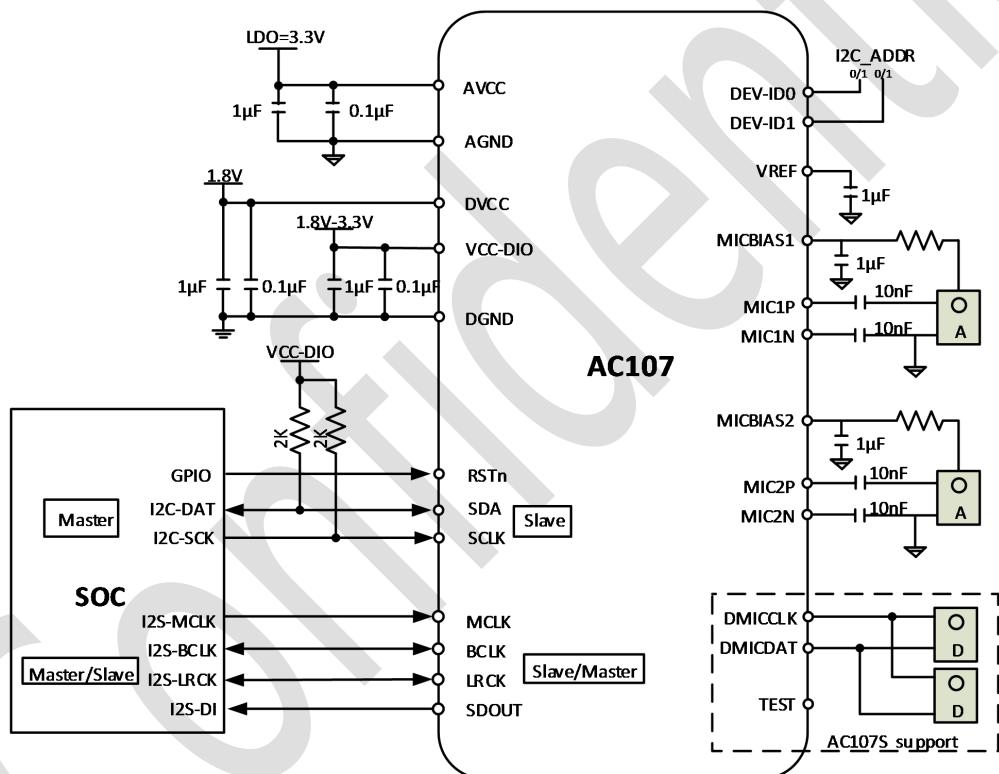


Figure 8-1. Typical Application Diagram

9 PCB Layout Guidelines

Each system design and PCB layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the AC107 performance:

1. The decoupling capacitors for the power supplies must be placed close to the device terminals. Figure 8-1 shows the recommended decoupling capacitors for the AC107.
2. For analog differential audio signals, they must be routed differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to avoid undesirable crosstalk.
3. Analog and digital grounds must be separated to prevent possible digital noise from affecting the analog performance of the board.

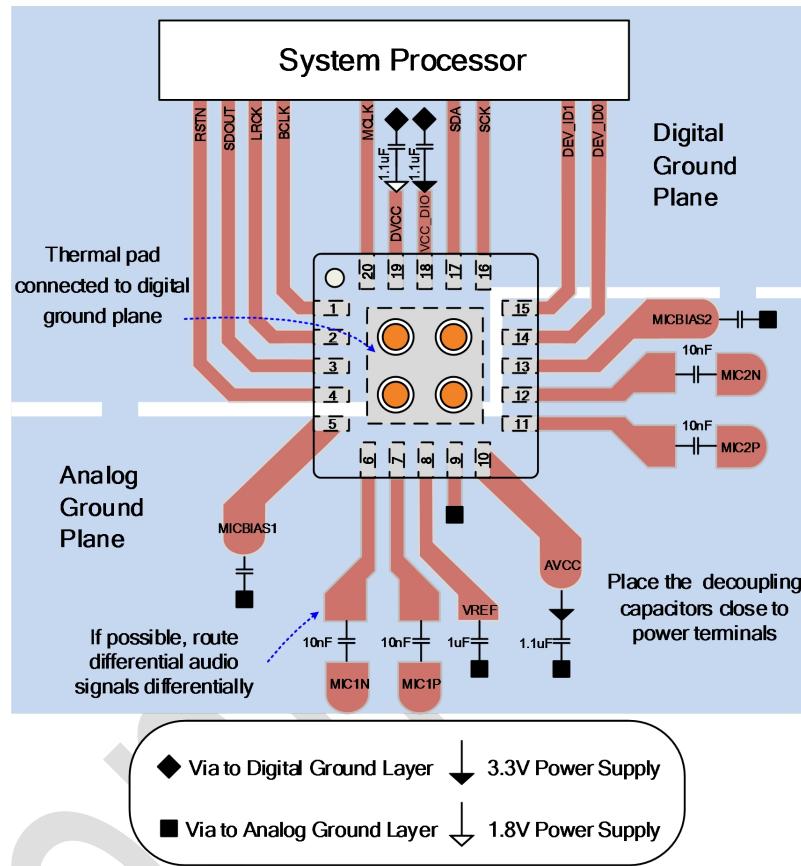


Figure 9-1. AC107 Recommended PCB layout

10 Package And Ordering Information

10.1 Package Information

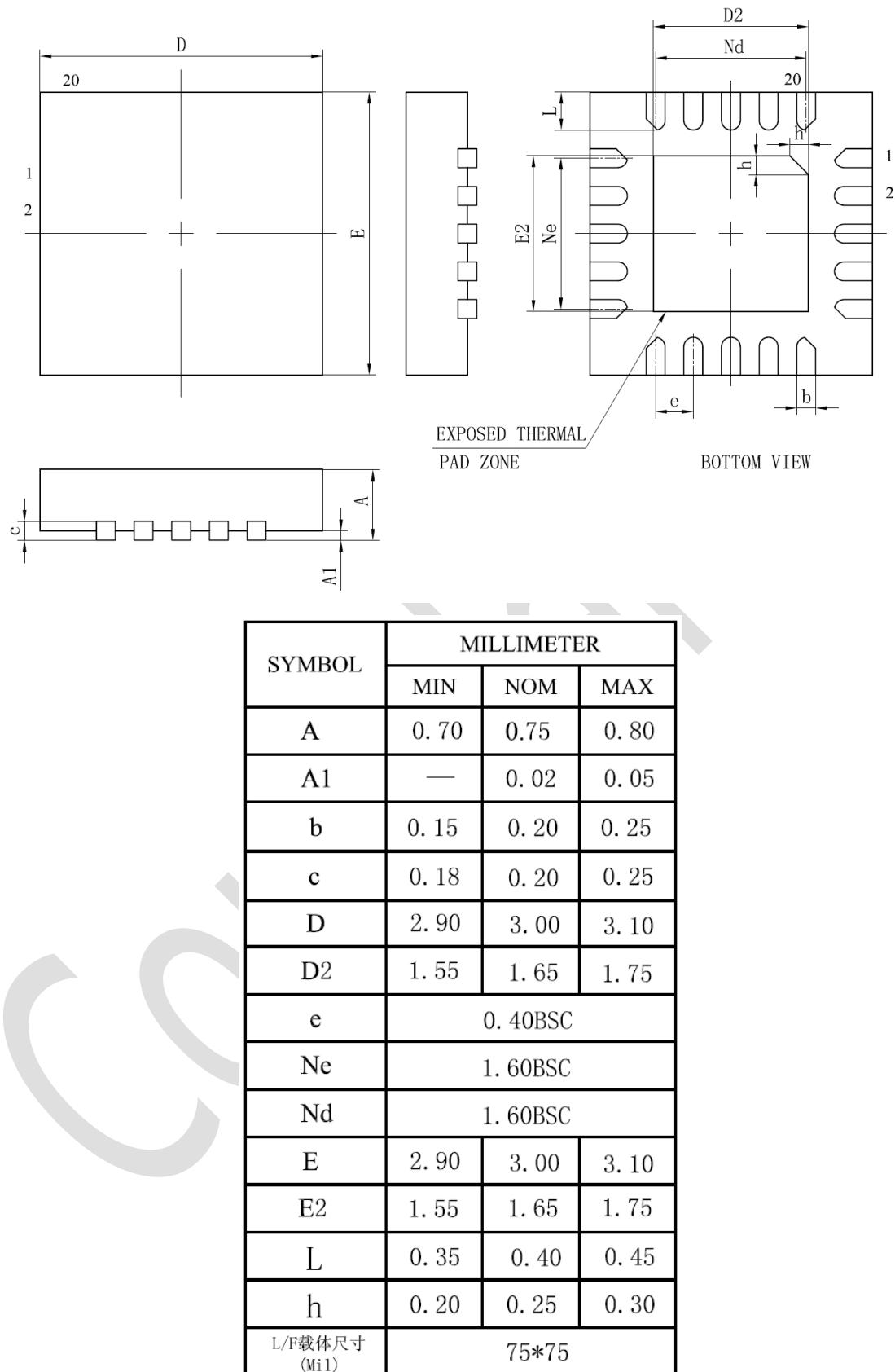
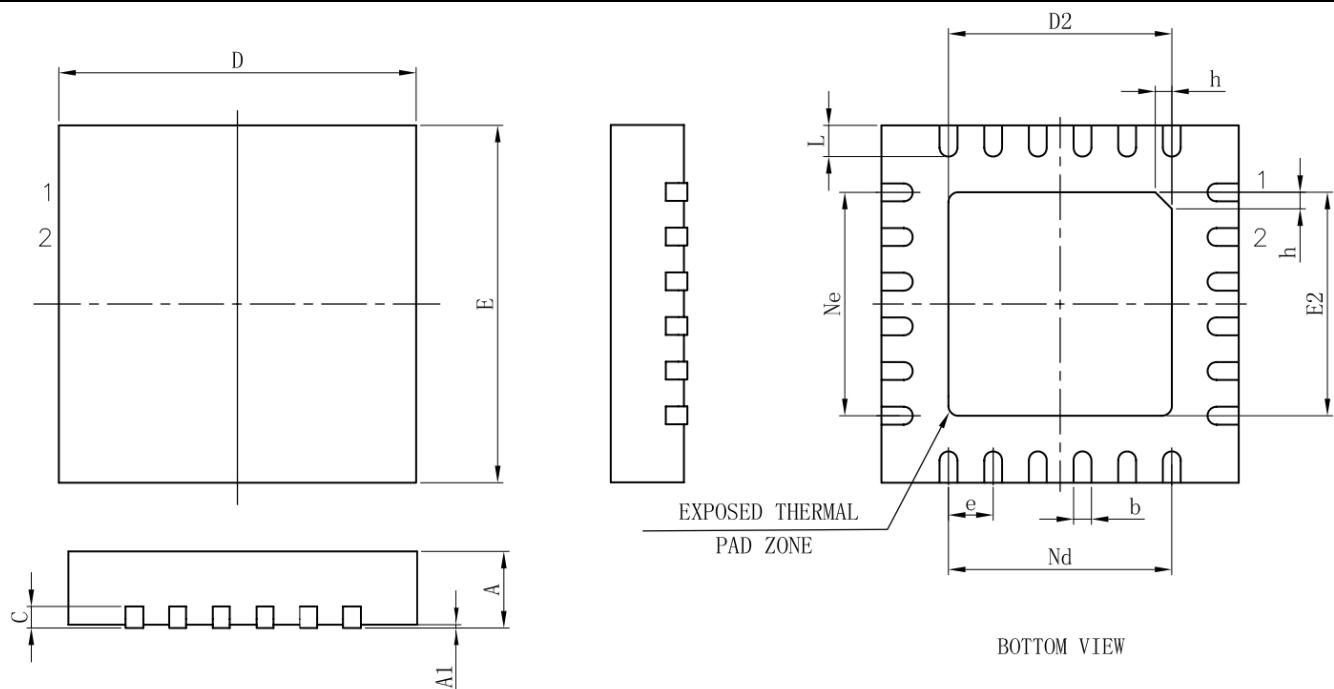


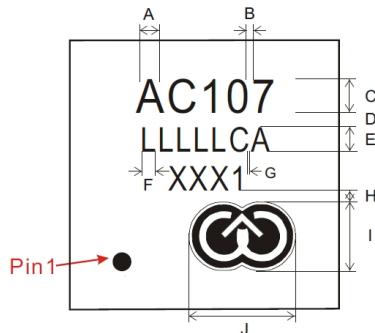
Figure 10-1. AC107 Package Dimension: 20 QFN



| SYMBOL | MILLIMETER | | |
|---------|------------|------|------|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | — | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| c | 0.18 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.40 | 2.50 | 2.60 |
| e | 0.50BSC | | |
| Ne | 2.50BSC | | |
| Nd | 2.50BSC | | |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.40 | 2.50 | 2.60 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.30 | 0.35 | 0.40 |
| L/F载体尺寸 | 110x110 | | |

Figure 10-2. AC107S Package Dimension: 24 QFN

10.2 Marking Information



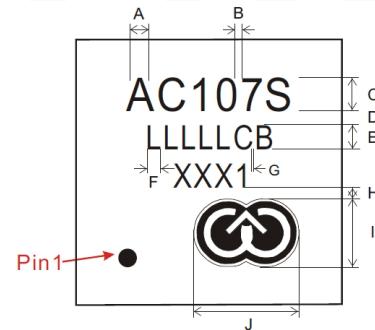
| A | B | C | D | E | F | G | H | I | J |
|------|------|-----|------|------|------|------|-----|-----|-----|
| 0.25 | 0.06 | 0.4 | 0.15 | 0.28 | 0.15 | 0.06 | 0.1 | 1.0 | 1.5 |

Unit: mm Size tolerance: $\pm 0.1\text{mm}$

Figure 10-3. AC107 Marking

Table 10-1. AC107 Marking Definitions

| No. | Marking | Description | Fixed/Dynamic |
|-----|---|---------------|---------------|
| 1 | AC107 | Product name | Fixed |
| 2 | LLLLCA | Lot number | Dynamic |
| 3 | XXX1 | Date code | Dynamic |
| 4 |  | X-POWERS logo | Fixed |
| 5 | White dot | Package pin 1 | Fixed |



| A | B | C | D | E | F | G | H | I | J |
|-----|------|-----|-----|------|-----|-----|-----|-----|-----|
| 0.3 | 0.15 | 0.5 | 0.2 | 0.35 | 0.2 | 0.1 | 0.2 | 1.1 | 1.7 |

Unit: mm Size tolerance: $\pm 0.1\text{mm}$

Figure 10-4. AC107S Marking

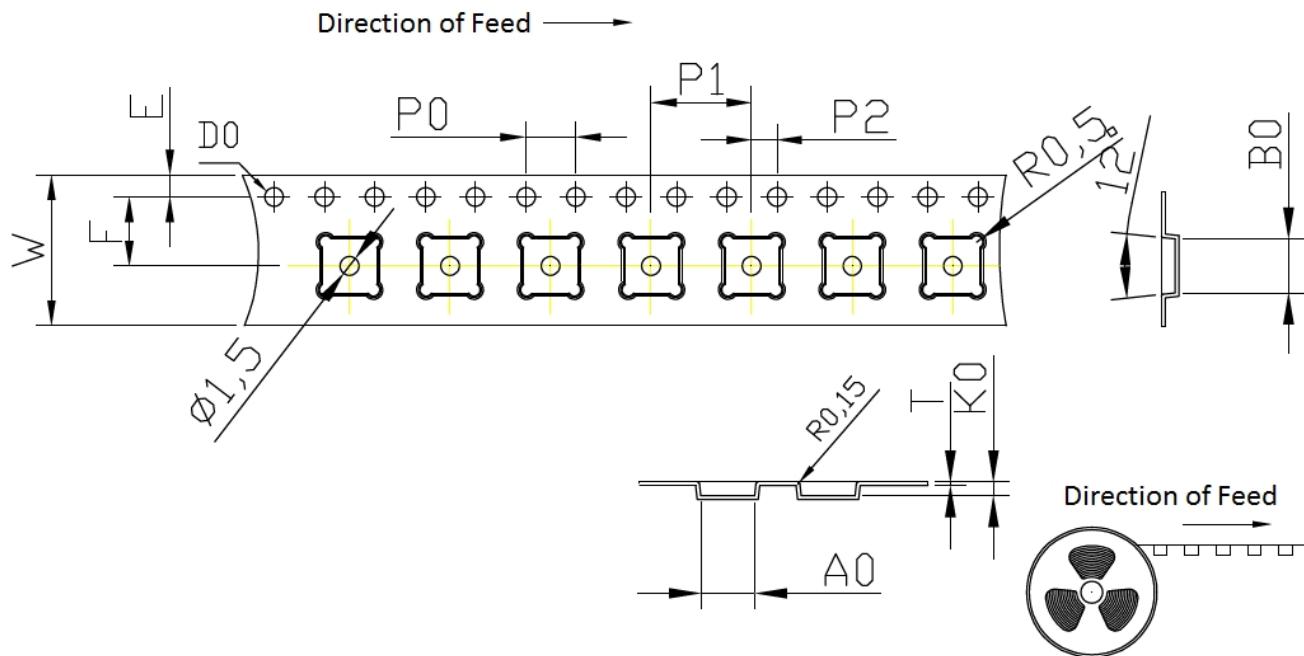
Table 10-2. AC107S Marking Definitions

| No. | Marking | Description | Fixed/Dynamic |
|-----|---|---------------|---------------|
| 1 | AC107S | Product name | Fixed |
| 2 | LLLLCB | Lot number | Dynamic |
| 3 | XXX1 | Date code | Dynamic |
| 4 |  | X-POWERS logo | Fixed |
| 5 | White dot | Package pin 1 | Fixed |

10.3 Carrier

Table 10-3. Reel Carrier Information

| Item | Color | Size |
|--------------------|---------------|------------------------|
| Reel | Blue | 13 inches |
| Aluminum foil bags | Silvery white | 440mm x 370mm x 0.15mm |
| Inside Box | White | 336mm x 336mm x 48mm |
| Outside Box | White | 423mm x 358mm x 365mm |


Figure 10-5. Tape Dimension Drawing
Table 10-4. Tape Dimension

| Device | W(mm) | A0(mm) | B0(mm) | K0(mm) | P0(mm) | P1(mm) |
|--------|---------------|----------------|----------------|------------------------|----------------|----------------|
| AC107 | 12 ± 0.30 | 3.30 ± 0.1 | 3.30 ± 0.1 | $1.10^{+0.10}_{-0.05}$ | 4.0 ± 0.1 | 8.00 ± 0.1 |
| AC107S | 12 ± 0.30 | 4.30 ± 0.1 | 4.30 ± 0.1 | $1.10^{+0.05}_{-0.00}$ | 4.0 ± 0.1 | 8.00 ± 0.1 |
| Device | P2(mm) | F(mm) | E(mm) | D0(mm) | T(mm) | |
| AC107 | 2.0 ± 0.1 | 5.5 ± 0.1 | 1.75 ± 0.1 | $1.5^{+0.10}_{-0.00}$ | 0.3 ± 0.05 | |
| AC107S | 2.0 ± 0.1 | 5.5 ± 0.1 | 1.75 ± 0.1 | $1.5^{+0.10}_{-0.00}$ | 0.3 ± 0.05 | |

Table 10-5. Packing Quantity Information

| Type | Quantity | Part Number |
|-----------|----------|-------------|
| Tape Reel | 3000pcs | AC107 |
| Tape Reel | 3000pcs | AC107S |

11 REFLOW PROFILE

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

Figure 11-1 shows the typical reflow profile of AC107 device sample.

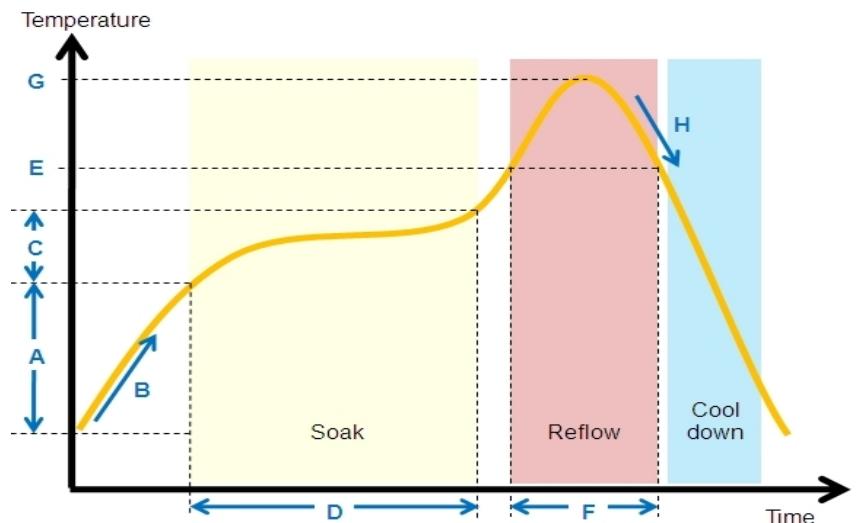


Figure 11-1 AC107 Typical Reflow Profile

Reflow profile conditions of AC107 device sample is given in Table 11-1.

Table 11-1 AC107 Reflow Profile Conditions

| QTI typical SMT reflow profile conditions (for reference only) | | |
|--|-----------------------------------|--------------------|
| | Step | Reflow condition |
| Environment | N2 purge reflow usage (yes/no) | Yes, N2 purge used |
| | If yes, O2 ppm level | O2 < 1500 ppm |
| A | Preheat ramp up temperature range | 25°C -> 150°C |
| B | Preheat ramp up rate | 1.5~2.5 °C/sec |
| C | Soak temperature range | 150°C -> 190°C |
| D | Soak time | 80~110 sec |
| E | Liquidus temperature | 217°C |
| F | Time above liquidus | 60-90 sec |
| G | Peak temperature | 240-250°C |
| H | Cool down temperature rate | ≤4°C/sec |

DECLARATION

THIS DOCUMENTATION IS THE ORIGINAL WORK AND COPYRIGHTED PROPERTY OF X-POWERS TECHNOLOGY ("X-POWERS"). REPRODUCTION IN WHOLE OR IN PART MUST OBTAIN THE WRITTEN APPROVAL OF X-POWERS AND GIVE CLEAR ACKNOWLEDGMENT TO THE COPYRIGHT OWNER.

THE PURCHASED PRODUCTS, SERVICES AND FEATURES ARE STIPULATED BY THE CONTRACT MADE BETWEEN X-POWERS AND THE CUSTOMER. PLEASE READ THE TERMS AND CONDITIONS OF THE CONTRACT AND RELEVANT INSTRUCTIONS CAREFULLY BEFORE USING, AND FOLLOW THE INSTRUCTIONS IN THIS DOCUMENTATION STRICTLY. X-POWERS ASSUMES NO RESPONSIBILITY FOR THE CONSEQUENCES OF IMPROPER USE (INCLUDING BUT NOT LIMITED TO OVERVOLTAGE, OVERCLOCK, OR EXCESSIVE TEMPERATURE).

THE INFORMATION FURNISHED BY X-POWERS IS PROVIDED JUST AS A REFERENCE OR TYPICAL APPLICATIONS, ALL STATEMENTS, INFORMATION, AND RECOMMENDATIONS IN THIS DOCUMENT DO NOT CONSTITUTE A WARRANTY OF ANY KIND, EXPRESS OR IMPLIED. X-POWERS RESERVES THE RIGHT TO MAKE CHANGES IN CIRCUIT DESIGN AND/OR SPECIFICATIONS AT ANY TIME WITHOUT NOTICE.

NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THE THIRD PARTIES WHICH MAY RESULT FROM ITS USE. NO LICENSE IS GRANTED BY IMPLICATION OR OTHERWISE UNDER ANY PATENT OR PATENT RIGHTS OF X-POWERS.

THIRD PARTY LICENCES MAY BE REQUIRED TO IMPLEMENT THE SOLUTION/PRODUCT. CUSTOMERS SHALL BE SOLELY RESPONSIBLE TO OBTAIN ALL APPROPRIATELY REQUIRED THIRD PARTY LICENCES. X-POWERS SHALL NOT BE LIABLE FOR ANY LICENCE FEE OR ROYALTY DUE IN RESPECT OF ANY REQUIRED THIRD PARTY LICENCE. X-POWERS SHALL HAVE NO WARRANTY, INDEMNITY OR OTHER OBLIGATIONS WITH RESPECT TO MATTERS COVERED UNDER ANY REQUIRED THIRD PARTY LICENCE.