Google Summer of Code

Documentation

Index

Creating projects and design flow on Xilinx Vivado

Software Version : Xilinx Vivado 2018.1
Product Family : Zynq-7000
Project part : xc7z020clg400-1
Target Language : VHDL
Link to github repository

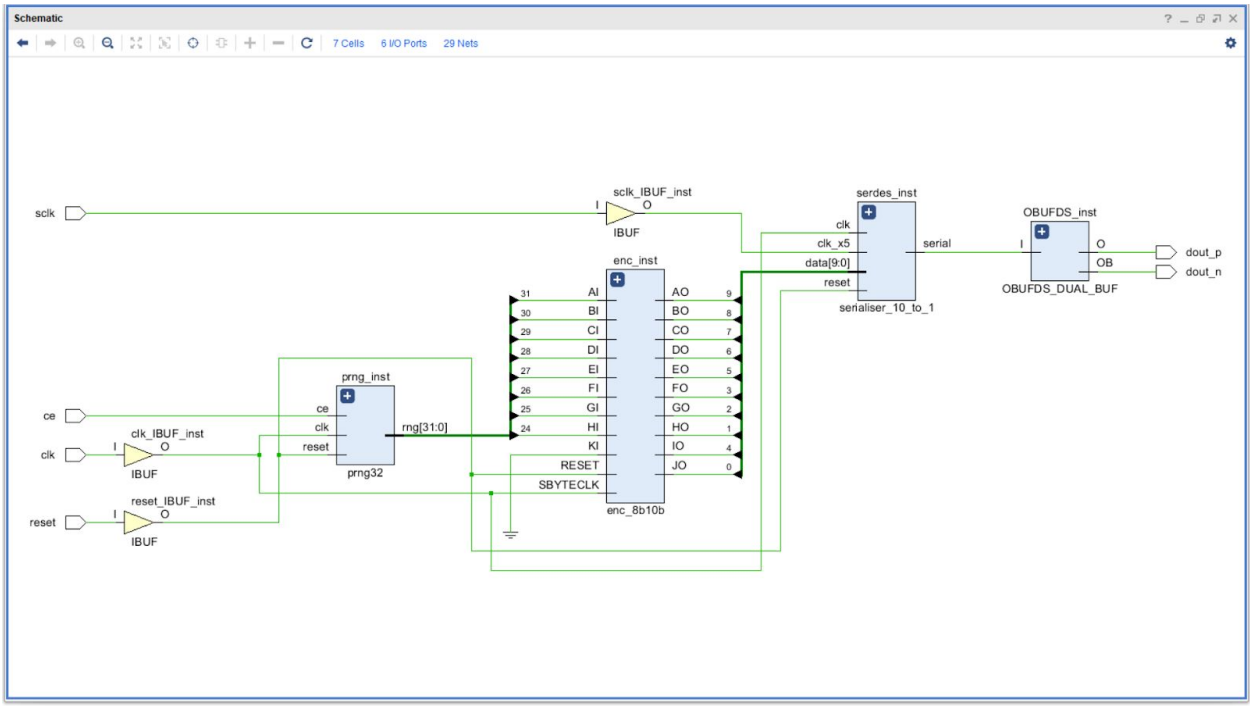
Creating projects and design flow on Lattice Diamond

Software Version : Lattice Diamond Version (64-bit) 3.10.2.115
Device : LCMXO2-1200HC-5TG144C (Commercial)
Package Type : TQFP144
Performance Grade : 5
Synthesis Tool : Lattice LSE
Target Language : VHDL

Link to github repository

Schematics of Transmitter for Zynq

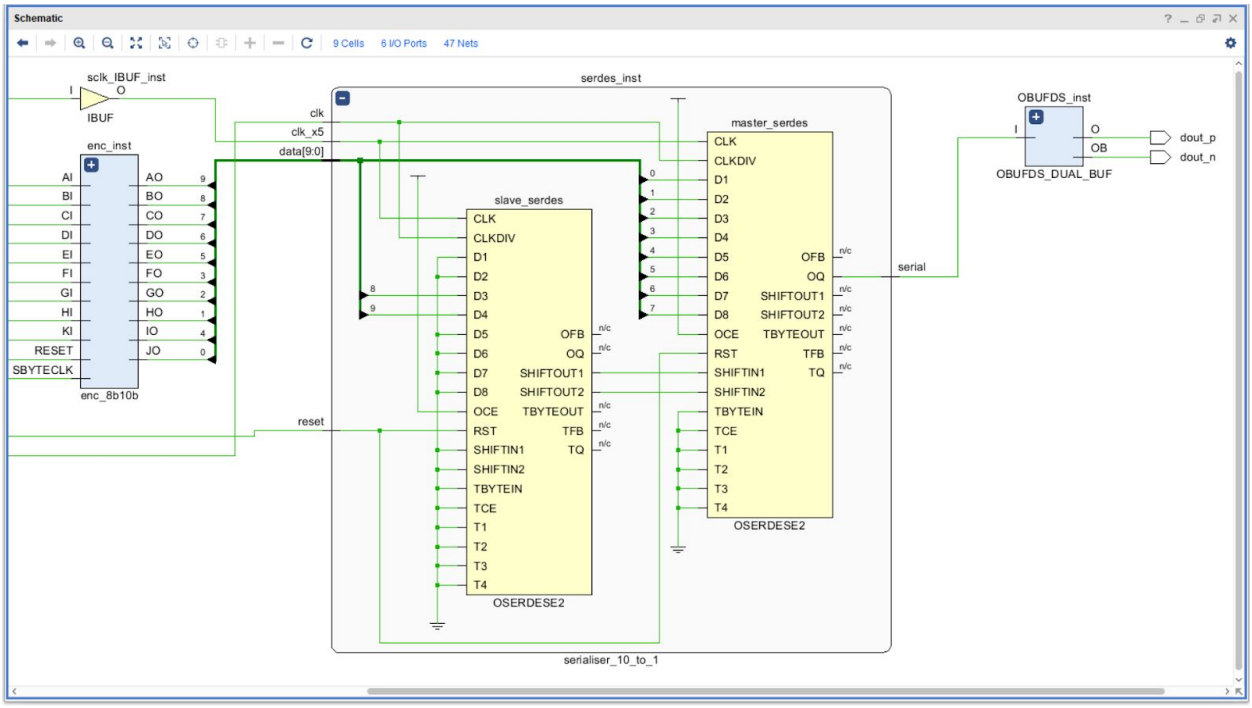
Link to the schematic



prng_inst : Instantiation of LFSR PRNG. Link to code.
enc_inst : Instantiation of 8b10b encoder. Link to code.
OBUFDS_inst : Instantiation of primitive OBUFDS. Link to xilinx library guide.

The design has to be reset first. Serial clock (“sclk”) that is supplied during testing phase is 100MHz and “clk” is 20MHz. A clock divider can be incorporated into the design to avoid supplying two separate clocks. The 8 bit parallel data from prng module is encoded with 8b10b encoding scheme which makes it necessary for us to find means to serialize 10 bits of data.

Schematic of serializer



In the design for the transmitter a pair of OSERDESE2 primitives have been used in a master slave configuration in DDR mode for 10:1 serialization ratio.

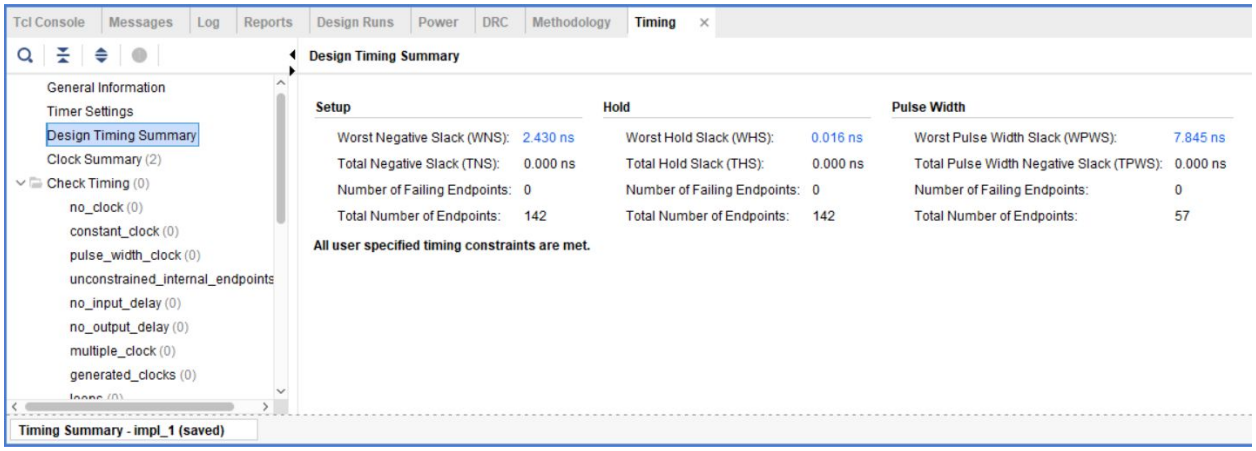
serdes_inst : Instantiation of serializer module. Link to code.

The output of the serializer is converted into a differential signal (LVDS) by the primitive OBUFDS.

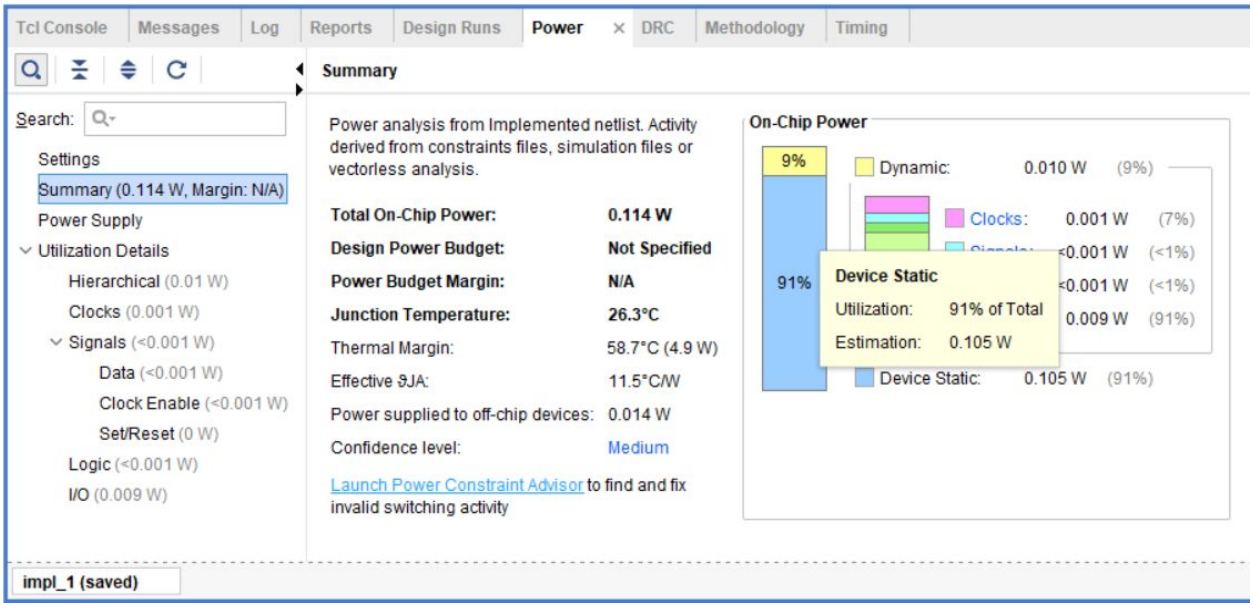
Link to Vivado project.

Analysis of Design

Timing Analysis



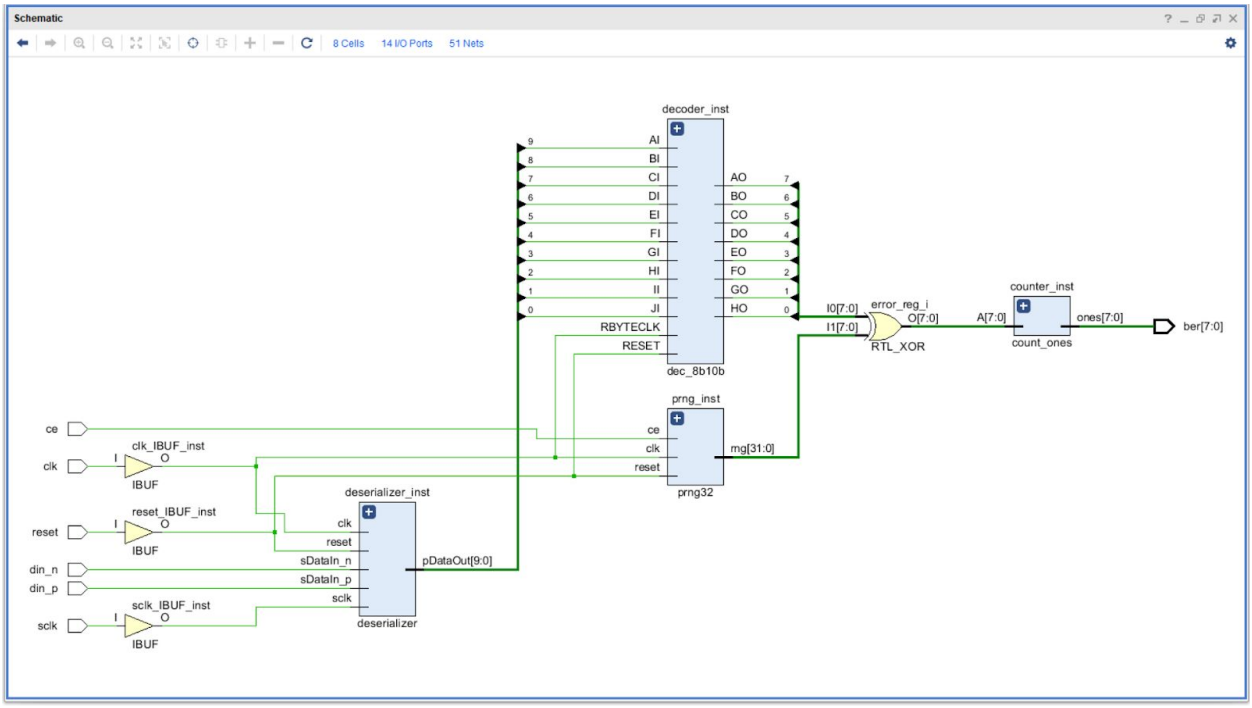
Power Consumption



Schematics of Receiver for Zynq

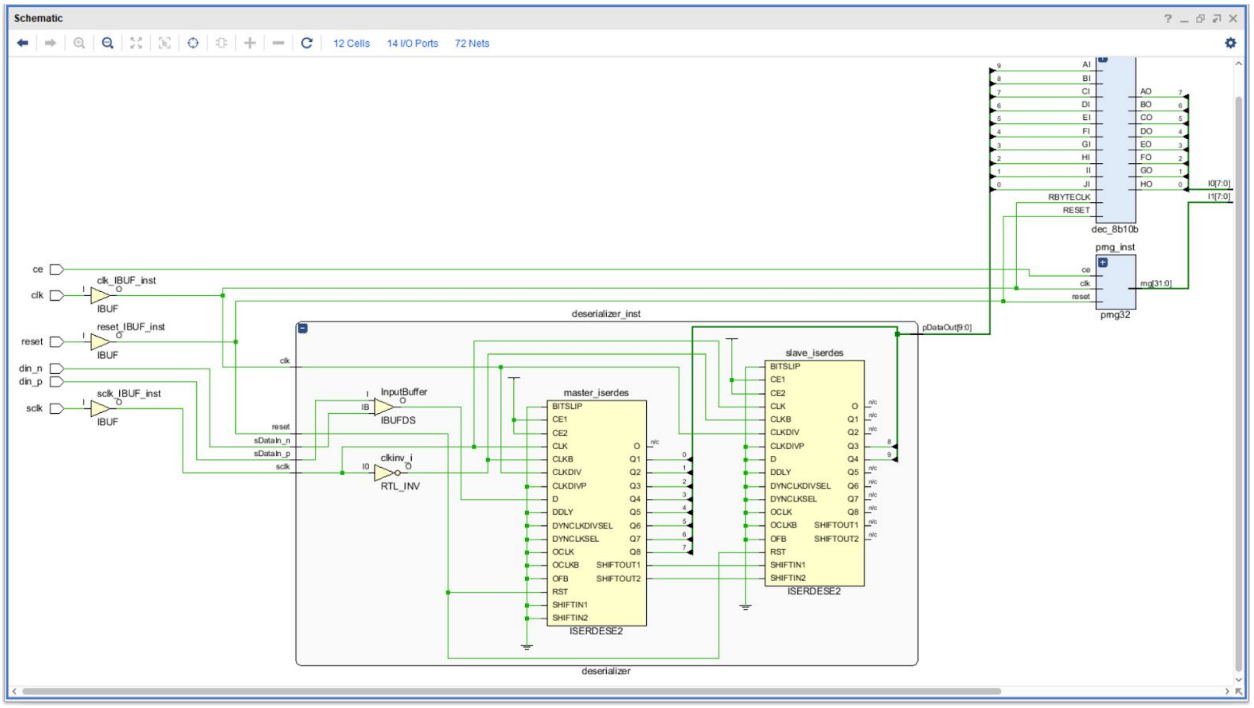
Link to the schematic

The deserializer module consists of a pair of ISERDESE2 primitives in a master slave configuration for 10:1 deserialization and the 10 bit data consequently gets decoded by 8b10b decoding scheme. This data, for BER calculation purposes is xored with data from the same LFSR PRNG module with the same seed and the “counter_inst” module counts the number of wrongly transmitted bits. The designed can be improved by removing the “ce” input pin and modify the “decoder_inst” so that it can supply the “ce” signal to the PRNG.



decoder_inst : Instantiation of 8b10b decoder. Link to code.
counter_inst : Instantiation of counter module. Link to code.

Schematic of deserializer

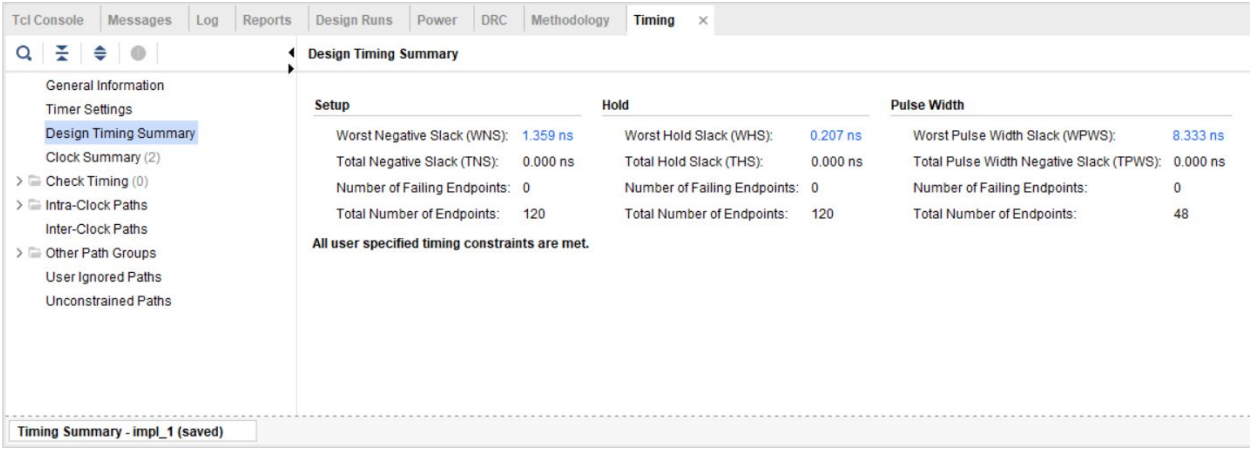


deserializer_inst : Instantiation of deserializer module. Link to code.

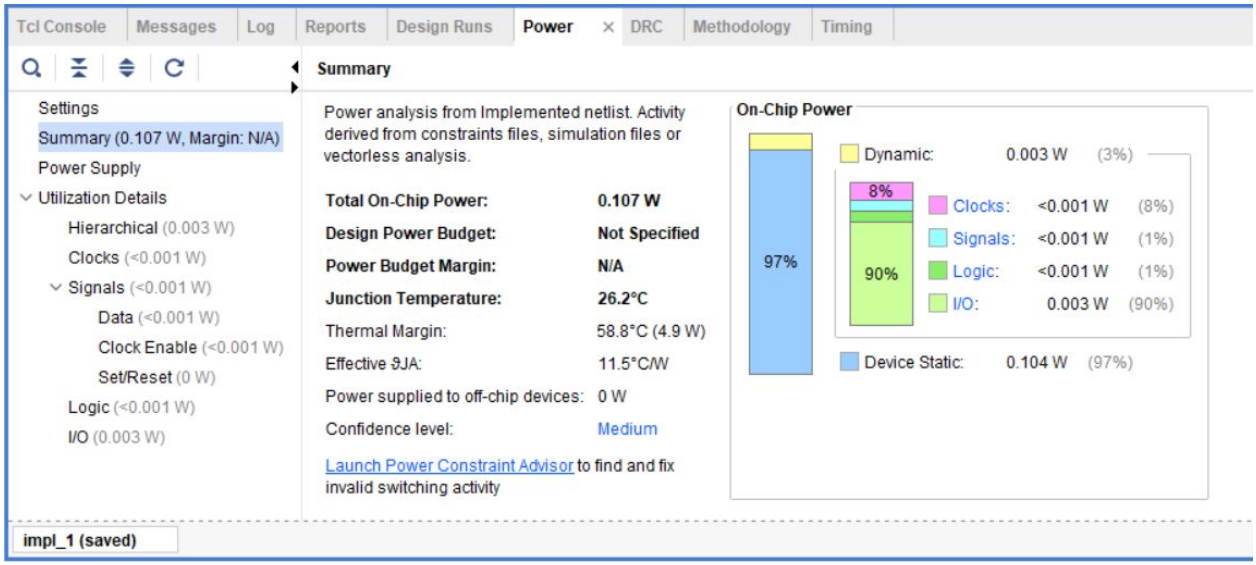
The design has to be reset first. Serial clock (“sclk”) that is supplied during testing phase is 100MHz and “clk” is 20MHz. A clock divider can be incorporated into the design to avoid supplying two separate clocks.
Link to Vivado project.

Analysis of Design

Timing Analysis



Power Consumption



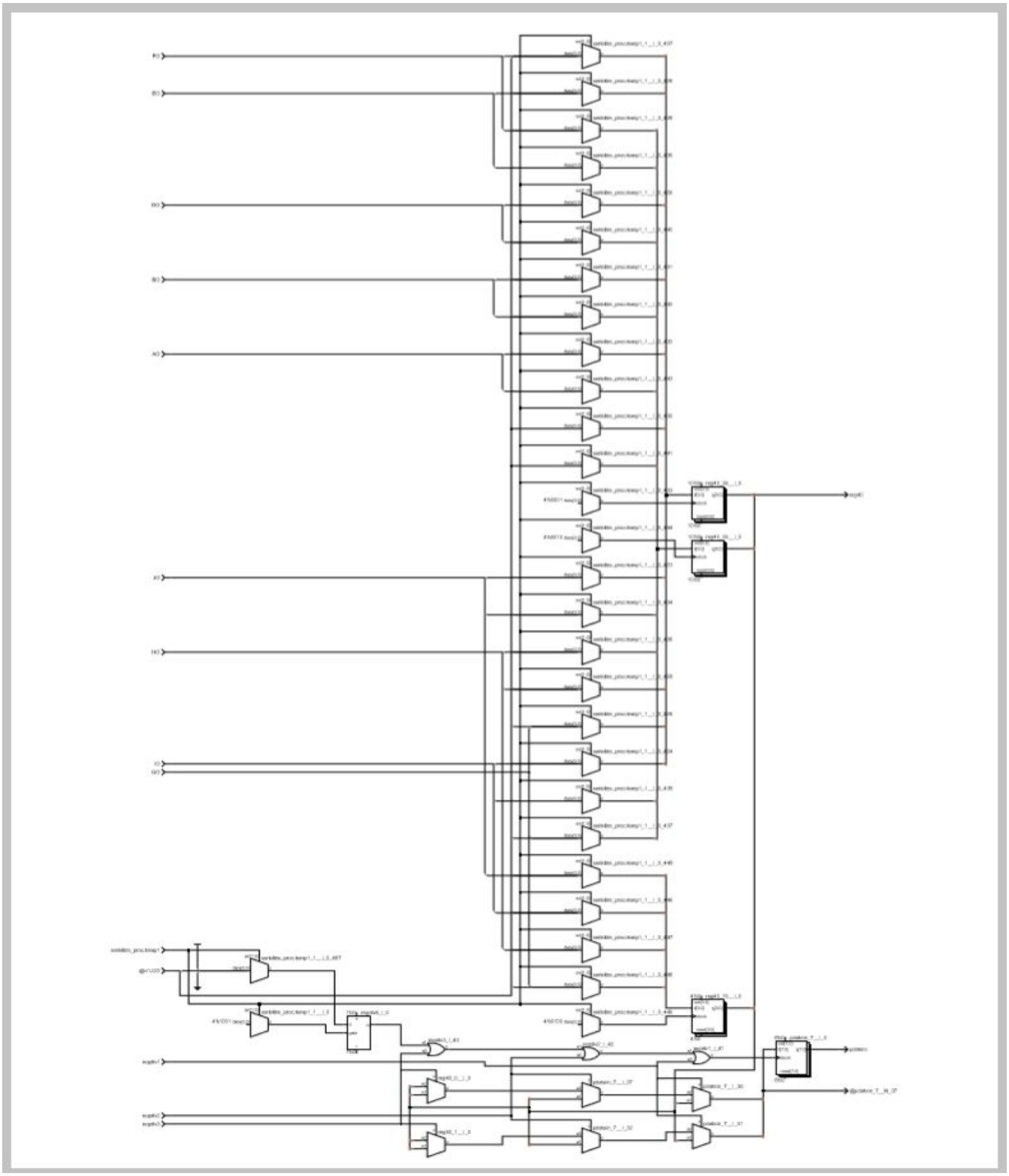
Schematics of transmitter for MachXO2

Generating random numbers is achieved by using the same LFSR PRNG module and the first 8 bits are encoded using the 8b10b encoding scheme. Since MachXO2 doesn't have a primitive with 10:1 SERDES ratio the 10 bit data, we try to match it 8 bits using a register of length equal to the least common multiple which in this case is 40. The 10 bits are stored in the 40 bit register and the 8 bits are sent to the serializer. There is clock domain crossing and the design can be improved with synchronizer circuits as the clock frequency is 1.25 times the parallel clock. This is because the time taken to store four 10 bit words in the 40 bit register must equal reading of 5 bytes.

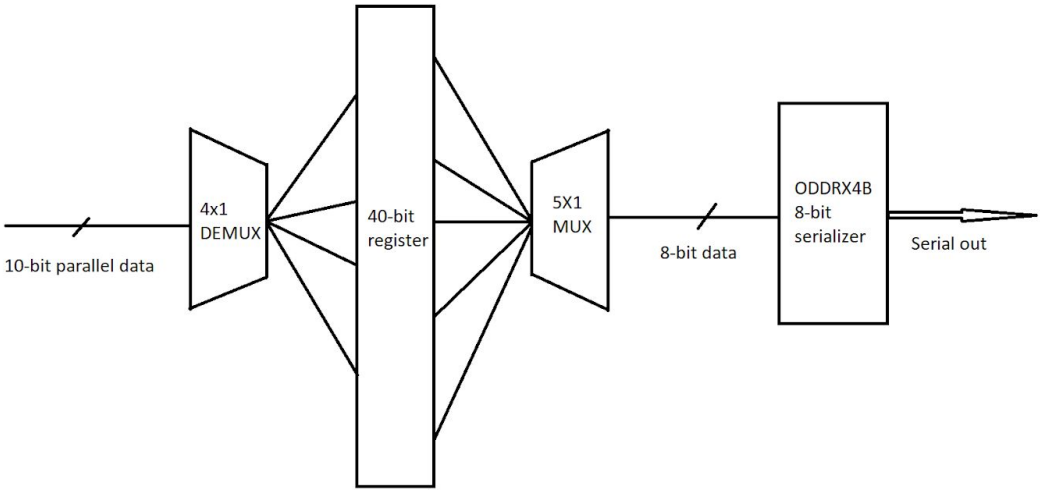
Link to Lattice library guide.
Link to code.
Link to Diamond project.
Link to output log of project.

This design has been tested at 100MHz serial clock and 20MHz parallel clock. "fclk" clock frequency is 31.25MHz. There are setup time and hold time violations in the design which have to be resolved before testing it on the actual hardware.

Schematic of serializer



Serialization process



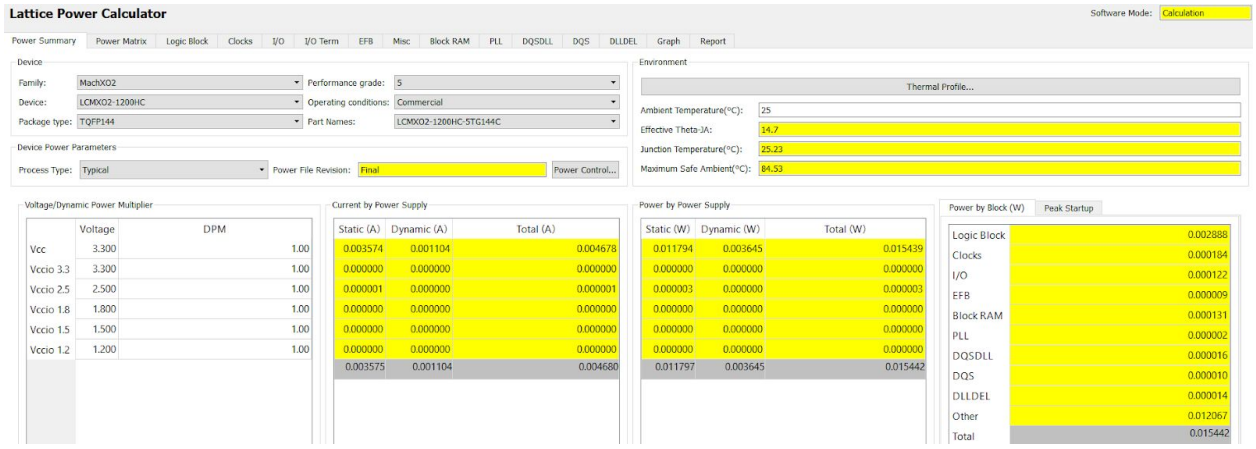
Analysis of Design

Timing Analysis

Delay Table												
Source	Destination	Weighted Slack	Arrival	Required	Data Delay	Route %	Levels	Clock Skew	Setup/Hold	Jitter	Color	
prng_inst/sr_i21	prng_inst/sr_i21	0.379	0.379	0	0.366	36.1	2	0	-0.013	0		
prng_inst/sr_i9	prng_inst/sr_i9	0.379	0.379	0	0.366	36.1	2	0	-0.013	0		
prng_inst/sr_i2	prng_inst/sr_i2	0.379	0.379	0	0.366	36.1	2	0	-0.013	0		
prng_inst/sr_i11	prng_inst/sr_i11	0.379	0.379	0	0.366	36.1	2	0	-0.013	0		
prng_inst/sr_i17	prng_inst/sr_i17	0.379	0.379	0	0.366	36.1	2	0	-0.013	0		
prng_inst/sr_i10	prng_inst/sr_i10	0.379	0.379	0	0.366	36.1	2	0	-0.013	0		
prng_inst/sr_i8	prng_inst/sr_i8	0.379	0.379	0	0.366	36.1	2	0	-0.013	0		
prng_inst/sr_i20	prng_inst/sr_i20	0.379	0.379	0	0.366	36.1	2	0	-0.013	0		
prng_inst/sr_i5	prng_inst/sr_i5	0.379	0.379	0	0.366	36.1	2	0	-0.013	0		
prng_inst/sr_i16	prng_inst/sr_i16	0.379	0.379	0	0.366	36.1	2	0	-0.013	0		
Data Path Details												
Name	Fanout	Delay		Source	Destination	Resource						
REG_DEL		0	0.133	R7C15D.CLK	R7C15D.Q1	prng_inst/SLICE_65						
ROUTE		3	0.132	R7C15D.Q1	R7C15D.A1	prng_inst/rng_21						
CTOF_DEL		0	0.101	R7C15D.A1	R7C15D.F1	prng_inst/SLICE_65						
ROUTE		1	0	R7C15D.F1	R7C15D.DI1	prng_inst/rng_31_N_77_21						
		Total=0.366										
Source Clock												
Name	Fanout	Delay		Source	Destination	Resource						
ROUTE		53	0.644	TCLKDIV0.CDIVX	R7C15D.CL	clk						
		Total=0.644										
Destination Clock												
Name	Fanout	Delay		Source	Destination	Resource						
ROUTE		53	0.644	TCLKDIV0.CDIVX	R7C15D.CL	clk						
		Total=0.644										

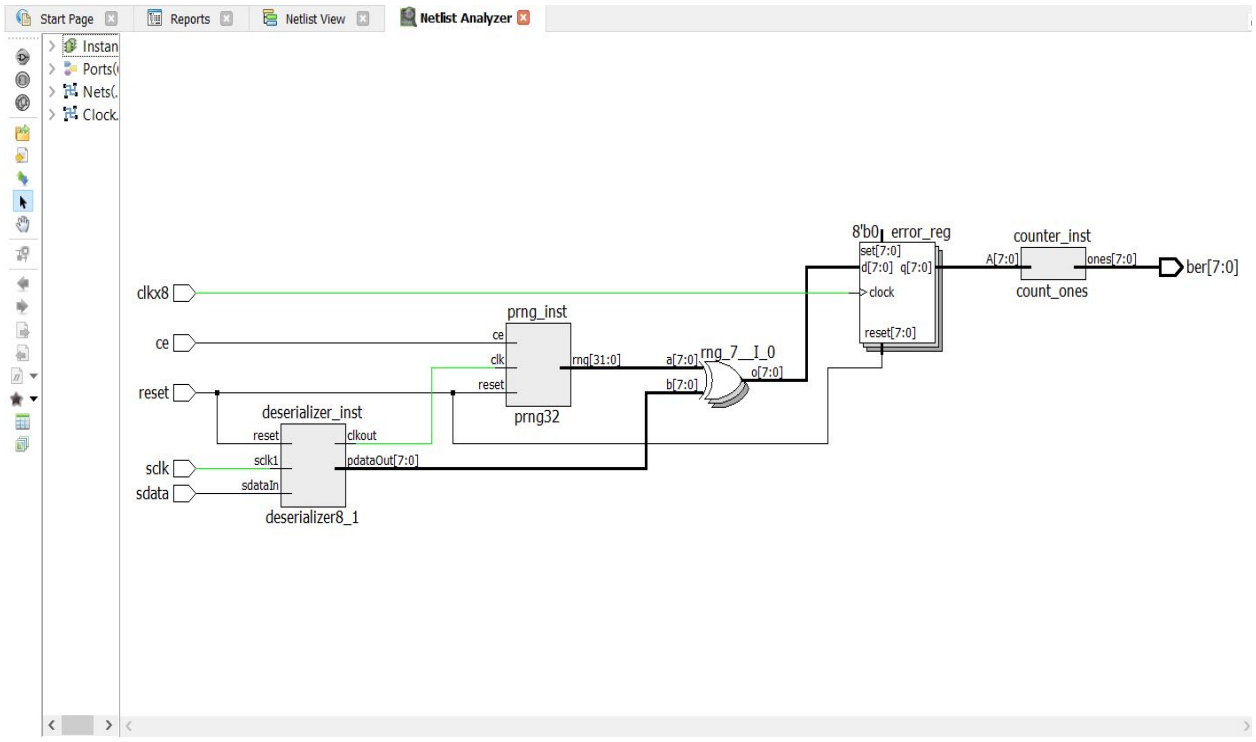
Link to timing analysis spreadsheet.

Power Consumption



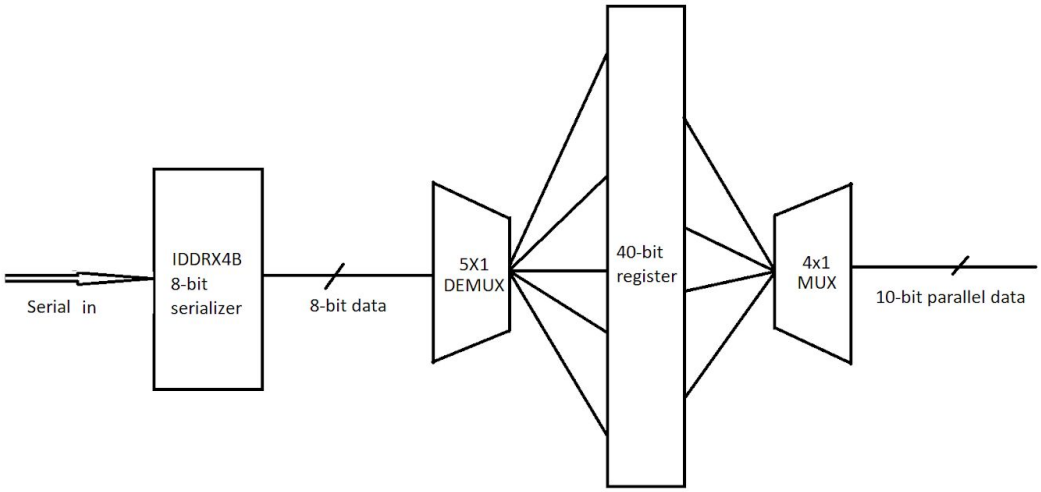
Link to power consumption analysis file.

Schematics of Receiver for MachXO2



Link to Lattice library guide.
Link to code.
Link to Diamond project.
Link to output log of project.

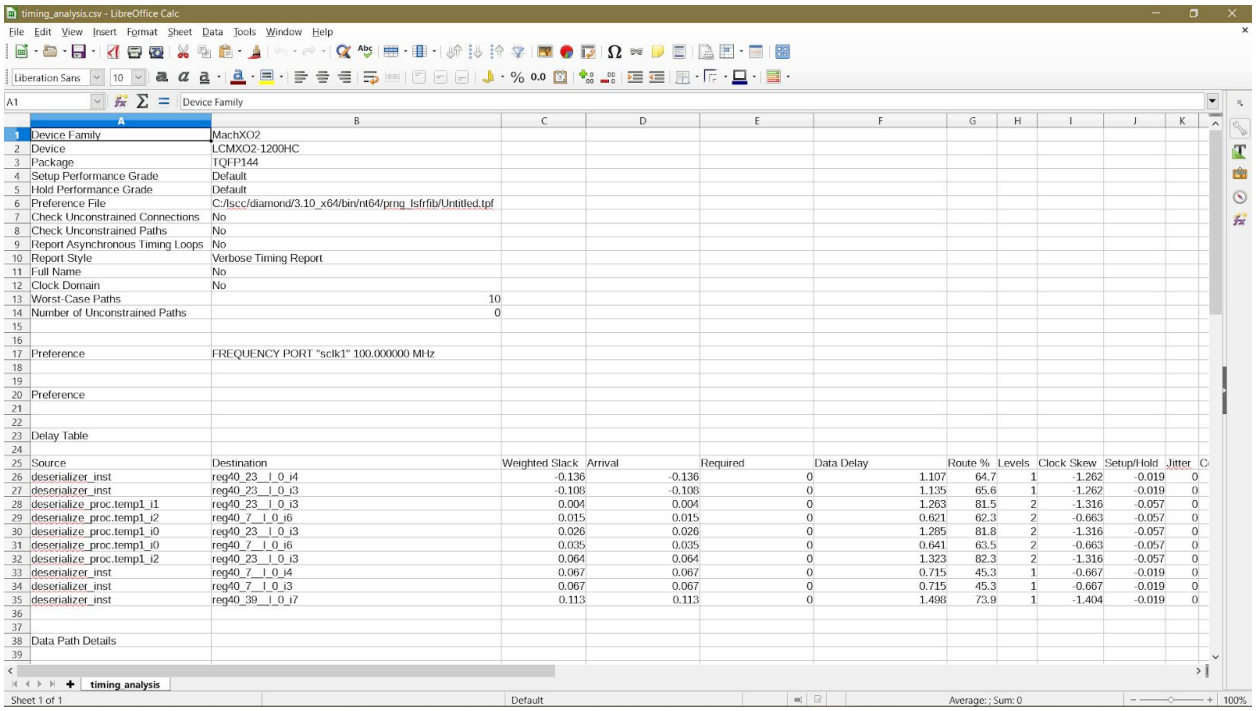
The SERDES design of the receiver is similar to the transmitter, albeit reverse in mechanism. Decoding and BER calculation modules are equivalent to their Zynq counterparts.



Addition of synchronous circuits would make the design much more stable and reliable as the “fclk” supplied to the 4x1 MUX has 1.25 times the frequency of parallel clock. The primitive “IDDRX4B” is a DDR deserializer with 8:1 SERDES ratio. There are setup time and hold time violations in the design which have to be resolved before this design can be tested on the actual hardware.

Analysis of Design

Timing Analysis



timing_analysis.csv - LibreOffice Calc

File Edit View Insert Format Sheet Data Tools Window Help

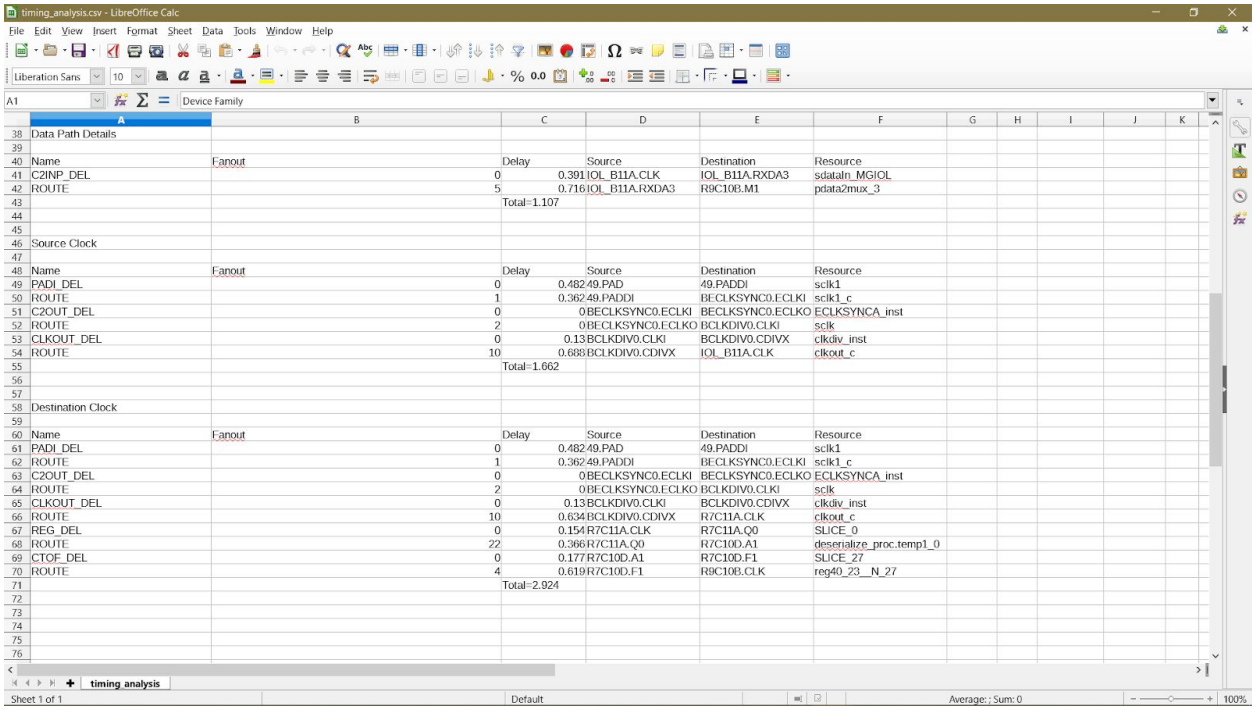
Liberation Sans 10

A1 Device Family

	A	B	C	D	E	F	G	H	I	J	K
1	Device Family	MachXO2									
2	Device	LCMXO2-1200HC									
3	Package	TQFP144									
4	Setup Performance Grade	Default									
5	Hold Performance Grade	Default									
6	Preference File	C:/lscc/diamond/3.10_x64/bin/nt64/prng_lsfrib/Untitled.tpf									
7	Check Unconstrained Connections	No									
8	Check Unconstrained Paths	No									
9	Report Asynchronous Timing Loops	No									
10	Report Style	Verbose Timing Report									
11	Full Name	No									
12	Clock Domain	No									
13	Worst-Case Paths		10								
14	Number of Unconstrained Paths		0								
15											
16											
17	Preference	FREQUENCY PORT "sclk1" 100.000000 MHz									
18											
19											
20	Preference										
21											
22											
23	Delay Table										
24											
25	Source	Destination	Weighted Slack	Arrival	Required	Data Delay	Route %	Levels	Clock Skew	Setup/Hold	Jitter
26	deserializer_inst	reg40_23__I_0_i4	-0.136	-0.136	0	1.107	64.7	1	-1.262	-0.019	0
27	deserializer_inst	reg40_23__I_0_i3	-0.108	-0.108	0	1.135	65.6	1	-1.262	-0.019	0
28	deserialize_proc.temp1_i1	reg40_23__I_0_i3	0.004	0.004	0	1.263	81.5	2	-1.316	-0.057	0
29	deserialize_proc.temp1_i2	reg40_7__I_0_i6	0.015	0.015	0	0.621	62.3	2	-0.663	-0.057	0
30	deserialize_proc.temp1_i0	reg40_23__I_0_i3	0.026	0.026	0	1.285	81.8	2	-1.316	-0.057	0
31	deserialize_proc.temp1_i0	reg40_7__I_0_i6	0.035	0.035	0	0.641	63.5	2	-0.663	-0.057	0
32	deserialize_proc.temp1_i2	reg40_23__I_0_i3	0.064	0.064	0	1.323	82.3	2	-1.316	-0.057	0
33	deserializer_inst	reg40_7__I_0_i4	0.067	0.067	0	0.715	45.3	1	-0.667	-0.019	0
34	deserializer_inst	reg40_7__I_0_i3	0.067	0.067	0	0.715	45.3	1	-0.667	-0.019	0
35	deserializer_inst	reg40_39__I_0_i7	0.113	0.113	0	1.498	73.9	1	-1.404	-0.019	0
36											
37											
38	Data Path Details										
39											

timing_analysis

Sheet 1 of 1 Default Average: ; Sum: 0 100%



timing_analysis.csv - LibreOffice Calc

File Edit View Insert Format Sheet Data Tools Window Help

Liberation Sans 10

A1 Device Family

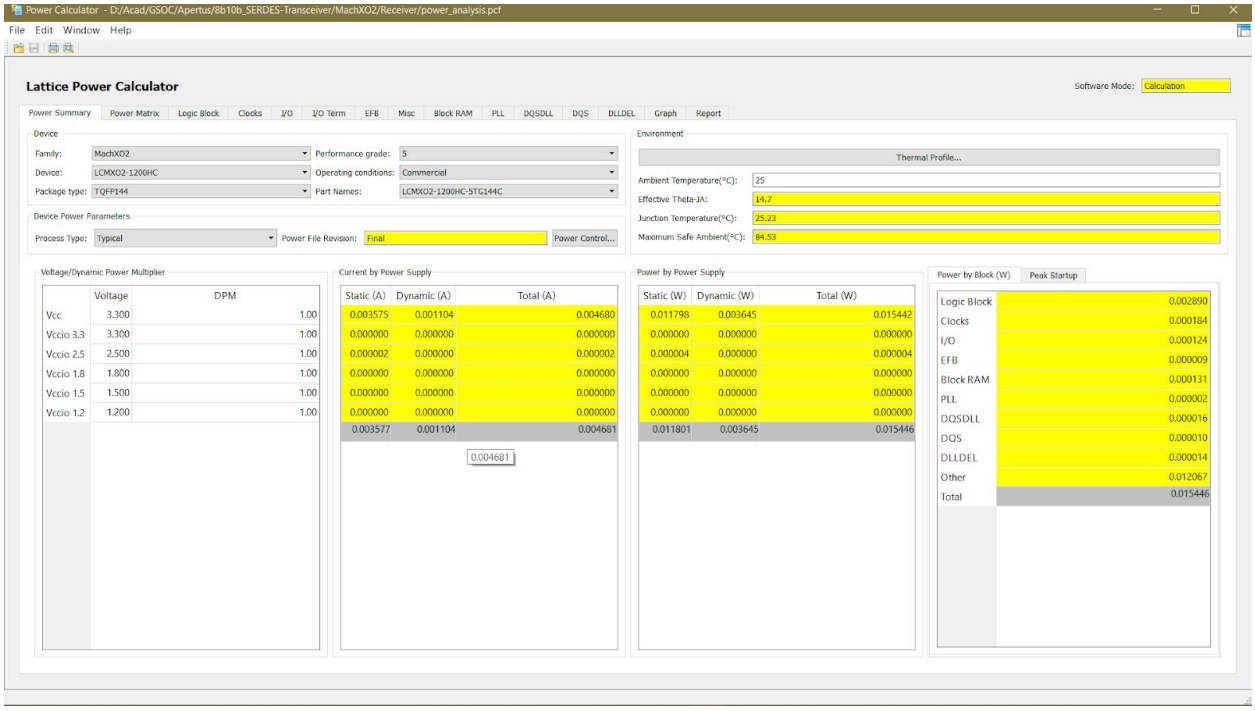
	A	B	C	D	E	F	G	H	I	J	K
38	Data Path Details										
39											
40	Name	Fanout	Delay	Source	Destination	Resource					
41	C2INP_DEL	0	0.391	IOL_B11A.CLK	IOL_B11A.RXDA3	sdataIn_MGIOL					
42	ROUTE	5	0.716	IOL_B11A.RXDA3	R9C10B.M1	pdata2mux_3					
43			Total=1.107								
44											
45											
46	Source Clock										
47											
48	Name	Fanout	Delay	Source	Destination	Resource					
49	PADI_DEL	0	0.482	49.PAD	49.PADDI	sclk1					
50	ROUTE	1	0.362	49.PADDI	BECLKSYNC0.ECLKI	sclk1_c					
51	C2OUT_DEL	0	0	BECLKSYNC0.ECLKI	BECLKSYNC0.ECLKO	ECLKSYNCA_inst					
52	ROUTE	2	0	BECLKSYNC0.ECLKO	BCLKDIV0.CLKI	sclk					
53	CLKOUT_DEL	0	0.13	BCLKDIV0.CLKI	BCLKDIV0.CDIVX	clkdiv_inst					
54	ROUTE	10	0.688	BCLKDIV0.CDIVX	IOL_B11A.CLK	clkout_c					
55			Total=1.662								
56											
57											
58	Destination Clock										
59											
60	Name	Fanout	Delay	Source	Destination	Resource					
61	PADI_DEL	0	0.482	49.PAD	49.PADDI	sclk1					
62	ROUTE	1	0.362	49.PADDI	BECLKSYNC0.ECLKI	sclk1_c					
63	C2OUT_DEL	0	0	BECLKSYNC0.ECLKI	BECLKSYNC0.ECLKO	ECLKSYNCA_inst					
64	ROUTE	2	0	BECLKSYNC0.ECLKO	BCLKDIV0.CLKI	sclk					
65	CLKOUT_DEL	0	0.13	BCLKDIV0.CLKI	BCLKDIV0.CDIVX	clkdiv_inst					
66	ROUTE	10	0.634	BCLKDIV0.CDIVX	R7C11A.CLK	clkout_c					
67	REG_DEL	0	0.154	R7C11A.CLK	R7C11A.Q0	SLICE_0					
68	ROUTE	22	0.366	R7C11A.Q0	R7C10D.A1	deserialize_proc.temp1_0					
69	CTOF_DEL	0	0.177	R7C10D.A1	R7C10D.F1	SLICE_27					
70	ROUTE	4	0.619	R7C10D.F1	R9C10B.CLK	reg40_23__N_27					
71			Total=2.924								
72											
73											
74											
75											
76											

timing_analysis

Sheet 1 of 1 Default Average: ; Sum: 0 100%

[Link] to timing analysis spreadsheet.

Power Analysis



Link to power consumption analysis file.