Documentation

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Creating projects and design flow on Xilinx Vivado

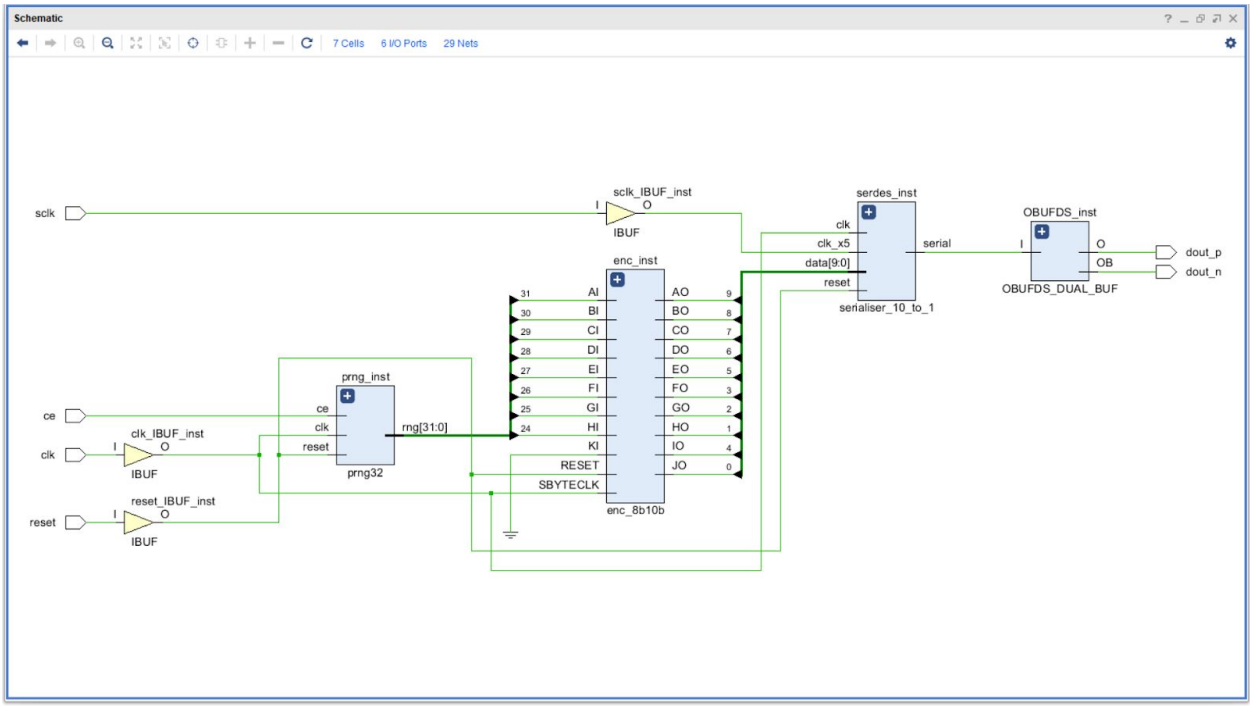
Software Version : Xilinx Vivado 2018.1
Product Family : Zynq-7000
Project part : xc7z020clg400-1
Target Language : VHDL
Link to github repository

Creating projects and design flow on Lattice Diamond

Software Version : Lattice Diamond Version (64-bit) 3.10.2.115
Device : LCMXO2-1200HC-5TG144C (Commercial)
Package Type : TQFP144
Performance Grade : 5
Synthesis Tool : Lattice LSE
Target Language : VHDL
Link to github repository

Schematics of Transmitter for Zynq

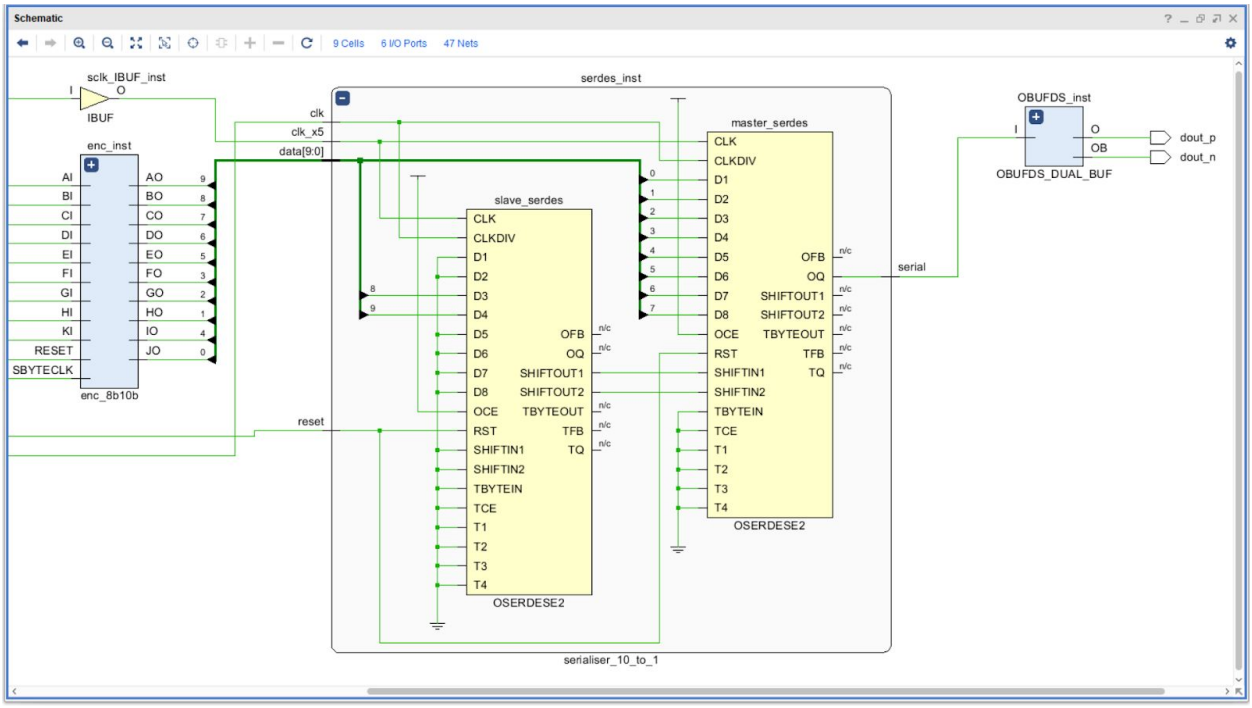
Link to the schematic



prng_inst : Instantiation of LFSR PRNG. Link to code.
enc_inst : Instantiation of 8b10b encoder. Link to code.
OBUFDS_inst : Instantiation of primitive OBUFDS. Link to xilinx library guide.

The design has to be reset first. Serial clock (“sclk”) that is supplied during testing phase is 100MHz and “clk” is 20MHz. A clock divider can be incorporated into the design to avoid supplying two separate clocks. The 8 bit parallel data from prng module is encoded with 8b10b encoding scheme which makes it necessary for us to find means to serialize 10 bits of data.

Schematic of serializer



In the design for the transmitter a pair of OSERDESE2 primitives have been used in a master slave configuration in DDR mode for 10:1 serialization ratio.

serdes_inst : Instantiation of serializer module. Link to code.

The output of the serializer is converted into a differential signal (LVDS) by the primitive OBUFDS.

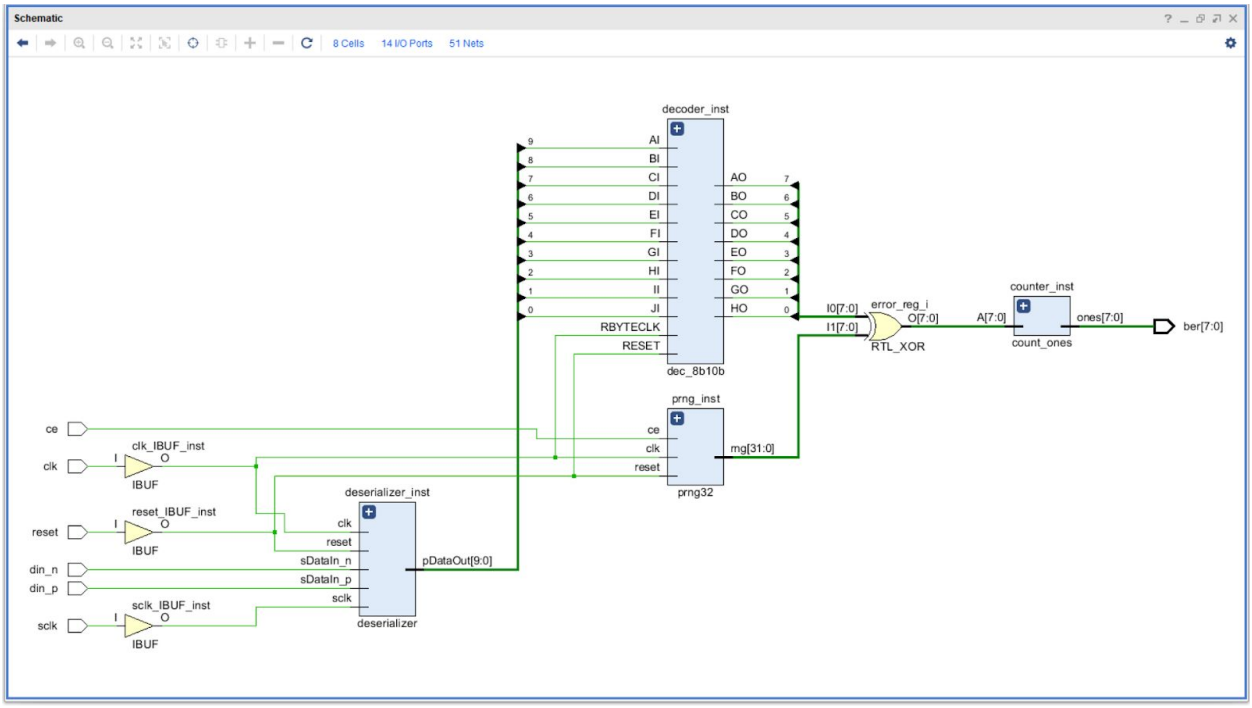
Link to Vivado project

Schematics of Receiver for Zynq

Link to the schematic

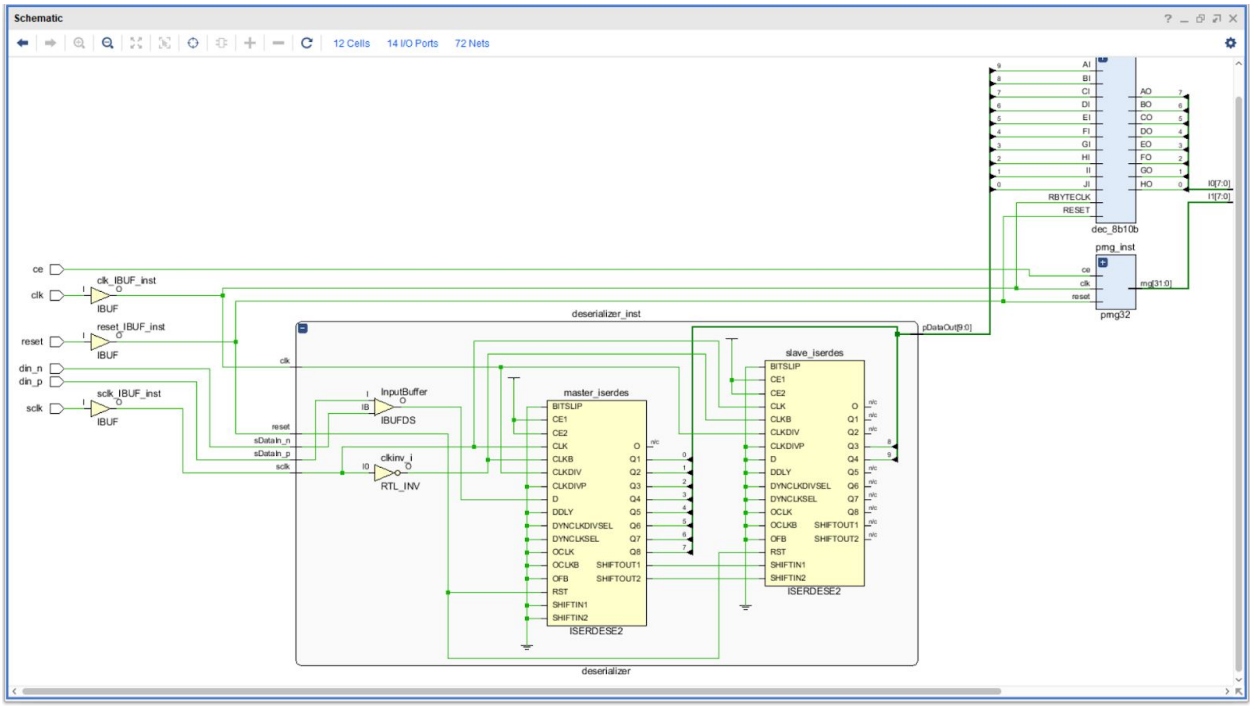
The deserializer module consists of a pair of ISERDESE2 primitives in a master slave configuration for 10:1 deserialization and the 10 bit data consequently gets decoded by 8b10b decoding scheme. This data, for BER calculation purposes is xored with data from the same LFSR PRNG module with the same seed and the “counter_inst” module counts the number of wrongly transmitted bits. The designed can be improved by

removing the “ce” input pin and modify the “decoder_inst” so that it can supply the “ce” signal to the PRNG.



decoder_inst : Instantiation of 8b10b decoder. Link to code.
counter_inst : Instantiation of counter module. Link to code.

Schematic of deserializer

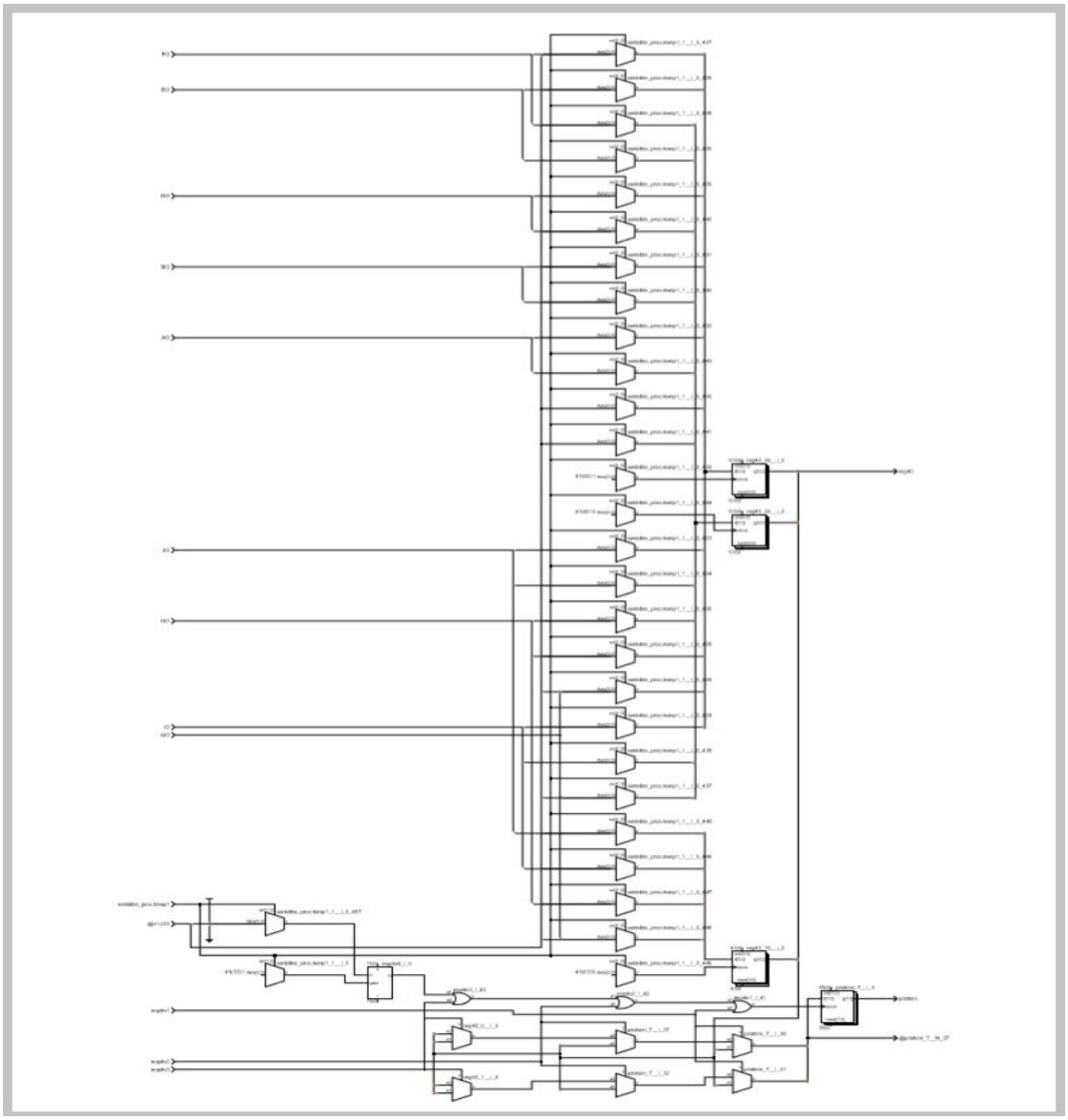


deserializer_inst : Instantiation of deserializer module. Link to code.

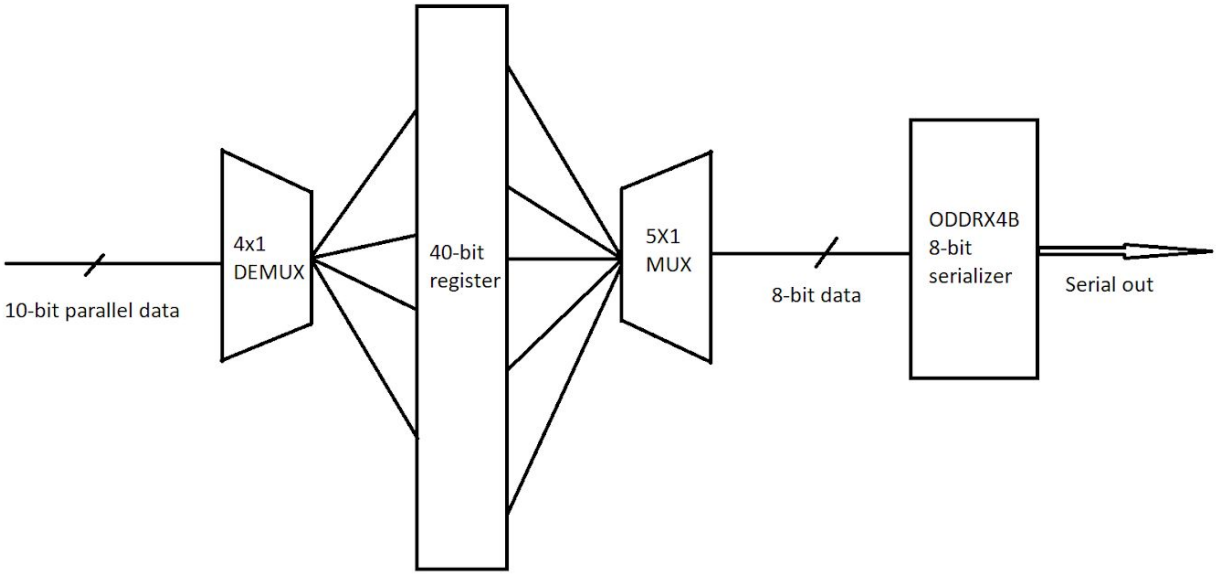
The design has to be reset first. Serial clock (“sclk”) that is supplied during testing phase is 100MHz and “clk” is 20MHz. A clock divider can be incorporated into the design to avoid supplying two separate clocks.

Link to Vivado project.

Schematics of transmitter for MachXO2



Generating random numbers is achieved by using the same LFSR PRNG module and the first 8 bits are encoded using the 8b10b encoding scheme. Since MachXO2 doesn't have a primitive with 10:1 SERDES ratio the 10 bit data, we try to match it 8 bits using a register of length equal to the least common multiple which in this case is 40. The 10 bits are stored in the 40 bit register and the 8 bits are sent to the serializer. There is clock domain crossing and the design can be improved with synchronizer circuits as the clock frequency is 1.25 times the parallel clock. This is because the time taken to store four 10 bit words in the 40 bit register must equal reading of 5 bytes.



Link to code.

Link to Diamond project.

This design has been tested at 100MHz serial clock and 20MHz parallel clock. "fclk" clock frequency is 31.25MHz.

Schematics of Receiver for MachXO2