YM2149

Software-Controlled Sound Generator (SSG)

■ OVERVIEW

The SSG (Software-Controlled Sound Generator) is an NMOS-LSI device designed to be capable of music generation. It only requires the microprocessor or microcomputer (CPU) to initialize its register array, thus reducing the load on the CPU. Music generation is carried out by the three sequence square wave generator, noise generator, and envelope generator according to the set parameters. This allows for the generation of music, special effects, warnings, and various other types of sounds.

■ FEATURES

- 5V single power supply
- Easy connection to 8 bit or 16 bit CPU
- Simple connection to external system through 2 sequence 8 bit I/O port
- Wide voicing range of 8 octaves
- Smooth attenuation by 5 bit envelope generator
- Built-in 5 bit D/A convertor
- Input of double frequency clock can be handled by built-in clock frequency divider
- TTL compatible level
- Low power consumption (typical 125mW)
- 40 pin plastic DIL package
- Pin compatible with AY-3-8910 manuafactured by GI

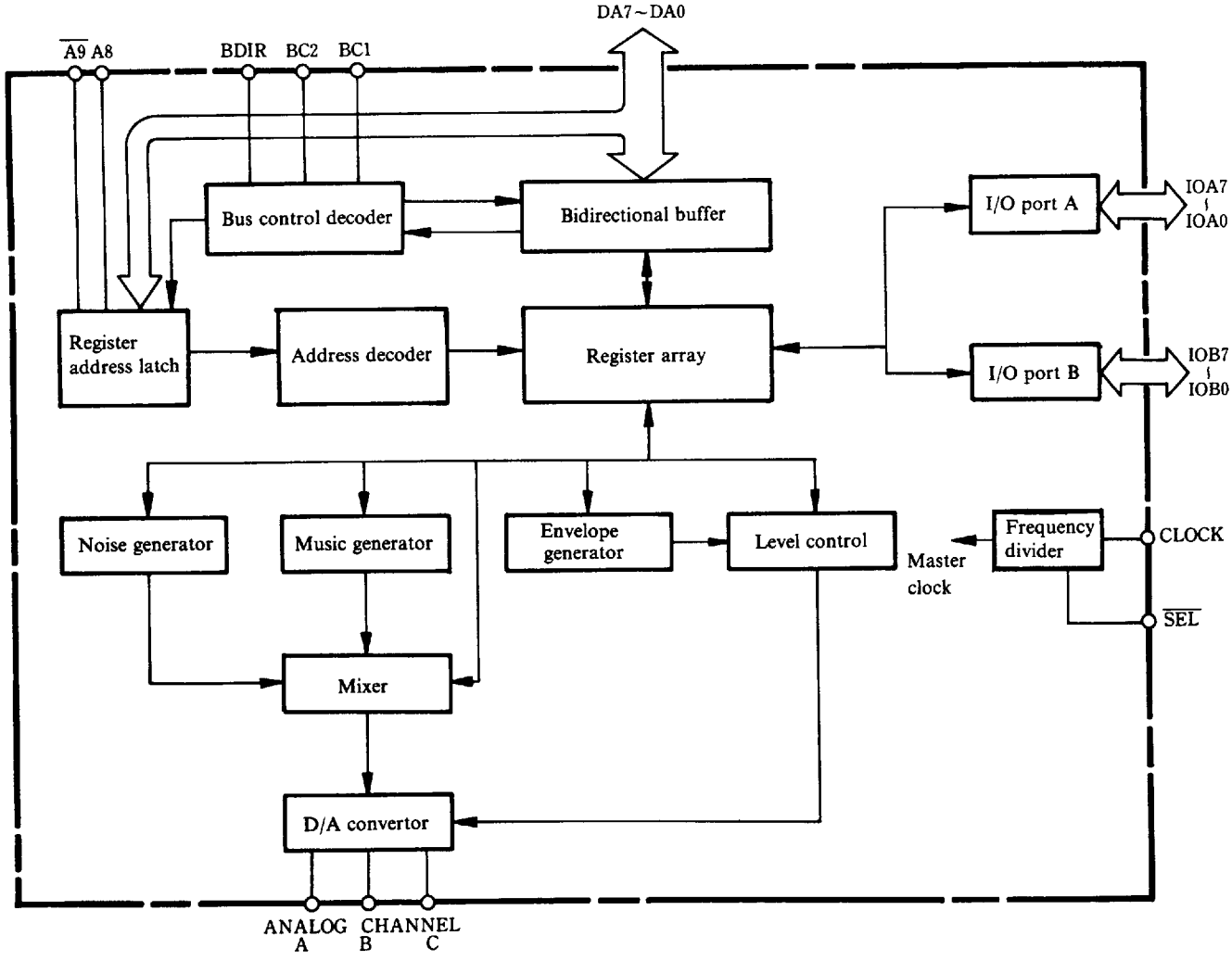
YAMAHA CORPORATION

YM2149 CATALOG
CATALOG No.: LSI-2121492
1992. 9

■ PIN LAYOUT

Vss(GND)	1	40	Vcc(+5V)
N.C	2	39	TEST1
ANALOG CHANNEL B	3	38	ANALOG CHANNEL C
ANALOG CHANNEL A	4	37	DA0
N.C	5	36	DA1
IOB7	6	35	DA2
IOB6	7	34	DA3
IOB5	8	33	DA4
IOB4	9	32	DA5
IOB3	10	31	DA6
IOB2	11	30	DA7
IOB1	12	29	BC1
IOB0	13	28	BC2
IOA7	14	27	BDIR
IOA6	15	26	$\overline{SEL}$
IOA5	16	25	A8
IOA4	17	24	$\overline{A9}$
IOA3	18	23	$\overline{RESET}$
IOA2	19	22	CLOCK
IOA1	20	21	IOA0

■ BLOCK DIAGRAM



■ DESCRIPTION OF PINS

1. DA7 ~ DA0
   This is an 8 bit bidirectional data bus which is used for moving data and addresses between the SSG and CPU. In the read and write modes, DA7 ~ DA0 corresponds to B7 ~ B0 of the register array. In the address mode, DA3 ~ DA0 is usde for the register address, and DA7 ~ DA4 is used together with $\overline{A9}$ and A8 for the upper address.

2. A8 and $\overline{A9}$
   These are the upper address input pins. A8 has pullup resistance while $\overline{A9}$ has pulldown resistance. When the voltage level at A8 while the level at $\overline{A9}$and DA7 - DA4 is low, the address mode is selected allowing for the fetching of a register address. Connect A8 and $\overline{A9}$ to +5V and ground respectively when not in use.

3. $\overline{RESET}$
   Reset is effective when the voltage level is low, and the contents of all registers in the array are reset to "0". This pin has pullup resistance.

4. CLOCK
   Supplies the master clock to the sound generator and envelope generator. This is equipped with a 1/2 frequency divider which allows for the use of a frequency which is 1/2 of the input clock, as the master clock.

5. $\overline{SEL}$
   When $\overline{SEL}$ is driven to the high level, the input clock is taken as the master clock. When the voltage level of $\overline{SEL}$ is low, the input clock is divided by 2 to obtain the master clock. This pin has pullup resistance, allowing for full pin compatibility with the AY-3-8910 manufactured by AI, when this pin is not connected to anything.

6. BDIR, BC1, and BC2
   Controls the external bus (DA7 ~ DA0) and internal bus of the SSG. The following four modes can be set by the bus control decoder. The bus control is redundant, control is possible even when BC5 is connected to +5V.

BDIR	BC2	BC1	Mode
0	0	0	Inactive
0	0	1	Address
0	1	0	Inactive
0	1	1	Read
1	0	0	Address
1	0	1	Inactive
1	1	0	Write
1	1	1	Address

Table 1 Bus Control Decoder

BDIR	BC2	BC1	Mode
0	1	0	Inactive
0	1	1	Read
1	1	0	Write
1	1	1	Address

Table 2 Bus control decoder with no redundancy

Inactive mode: DA7 ~ DA0 has high impedance.
Address mode: DA7 ~ DA0 set to input mode, and address is fetched from register array.

Write mode: DA7 ~ DA0 set to input mode, and data is written to register currently being addressed.

Read mode: DA7 ~ DA0 set to output mode, and contents of register currently being addressed are output.

7. ANALOG CHANNEL A, B, C
   Each of the three channels is equipped with a D/A convertor which converts the calculated digital values to analog signals for output.

8. IOA7 ~ IOA0, IOB7 ~ IOB0
   These are two 8 bit I/O ports. These ports allow the SSG to be placed between an external system and the CPU for the transfer of data. These pins have a pullup resistance.

9. TEST1
   Output pin for testing the device. Do not connect to anything.

10. VCC
    +5V power pin

11. VSS
    Ground pin

■ DESCRIPTION OF FUNCTIONS

All functions of the SSG are controlled by the 16 internal registers. The CPU need only write data to the internal registers of the SSG. The SSG itself generates the sound.
Sound is generated by the following blocks:

- Music generator: Square waves having a different frequency are generated for each channel (A, B, and C).
- Noise generator: Pseudo-random waveforms are generated (variable frequency).
- Mixer: Music and noise output are mixed for the three channels (A, B, and C).
- Level control: Constant level or variable level is given for each of the three channels (A, B, and C). Constant levels are controlled by the CPU, and variable levels by the envelope generator.
- Envelope generator: Generates various types of attenuation (single burst attenuated and repeated attenuation)
- D-A convertor: Sound is output on each of the three channels (A, B, and C) at the level determined by the level control.

The CPU can read the contents of the internal registers with no effect on sound.

1. Register Array

$\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	0	0	0	0
						≀			
0	1	0	0	0	0	1	1	1	1

Upper addresses (chip select) Lower addresses (register address)

Of the ten bit address, the lower addresses DA3~DA0 are used to select the 16 internal registers (register array). The upper addresses are used for chip selection. $\overline{A9}$ and A8 is programmed to 01 while DA7 through DA4 are set to 0000. When the upper addresses match this program in the address mode, a register address (lower four bits DA3 through DA0) is fetched from the register address latch. When the value set in the upper addresses is different from the program value, the bidirectional bus formed from DA7 through DA0 is driven to high impedance. A register address which has been fetched is retained until the nexxt address is fetched, and is not affected by the read, write, or inactive mode.

The contents of the register array are shown in Table 3.

Register \ Bit		B7	B6	B5	B4	B3	B2	B1	B0
R0	Frequency of channel A	8 bit fine tone adjustment							
R1						4 bit rough tone adjustment			
R2	Frequency of channel B	8 bit fine tone adjustment							
R3						4 bit rough tone adjustment			
R4	Frequency of channel C	8 bit fine tone adjustment							
R5						4 bit rough tone adjustment			
R6	Frequency of noise				5 bit noise frequency				
R7	I/O port and mixer Settings	I/O		Noise			Tone		
		IOB	IOA	C	B	A	C	B	A
R8	Level of channel A				M	L3	L2	L1	L0
R9	Level of channel B				M	L3	L2	L1	L0
RA	Level of channel C				M	L3	L2	L1	L0
RB	Frequency of envelope	8 bit fine adjustment							
RC		8 bit rough adjustment							
RD	Shape of envelope					CONT	ATT	ALT	HOLD
RE	Data of I/O port A	8 bit data							
RF	Data of I/O port B	8 bit data							

(Register numbers are indicated in hexadecimal notation)
Table 3 Register Array

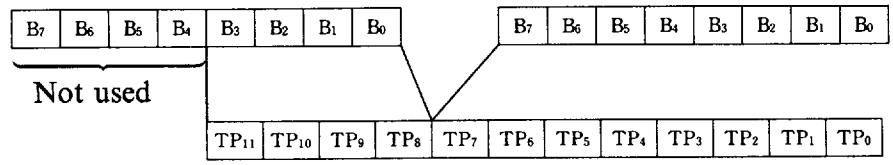
(1) Setting of music frequencies (controlled by registers R0 ~ R5)

The frequencies of the square wave generated by the music generators for the three channels (A, B, and C) are controlled by registers R0 through R5. R0 and R1 control channel A, R2 and R3 are used for channel B, and R4 and R5 control channel C. The oscillation frequency fT is obtained in the following manner from value of the register TP (decimal).

$$f_T = \frac{f_{Master}}{16TP}$$

f_{Master} is the frequency of the master clock (this is the input click frequency when $\overline{SEL}$ is high, and 1/2 of this frequency when low).

Rough tone adjustment register	Channel	Fine tone adjustment register
R1	A	R0
R3	B	R2
R5	C	R4



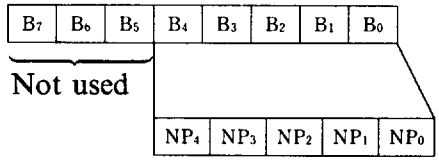
12 bit oscillation frequency setting value (TP)

(2) Setting of noise generator (controlled by register R6)

The noise frequency fN is obtained from the register value NP (decimal) in the following manner.

$$f_N = \frac{f_{Master}}{16NP}$$ (f_{Master} is the frequency of the master clock).

Noise frequency register R6

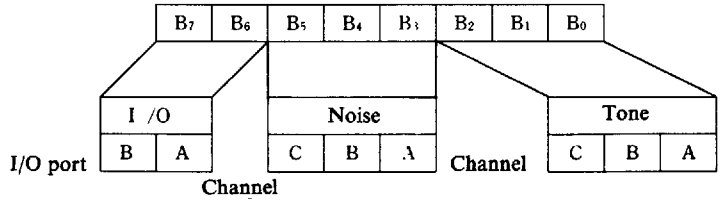


5 bit noise frequency setting value (NP)

(3) Settings of mixer and I/O ports (controlled by register R7)

The mixer is used to combine music and noise components. The combination is determined by bits B5 ~ B0 of register R7. Sound is output when a "0" is written to the register. Thus, when both the noise and tone are "0", the output is combined by the mixer (refer to Fig. 4). When the noise is "0" and the tone is "1", only the noise signal is output (refer to Fig. 3). When the noise is "1" and the tone is "0", music (square wave) is output (refer to Fig. 2). Nothing is output when both the noise and tone are "1". Selection of input/output for the I/O ports is determined by bits B7 and B6 of register R7. Input is selected when "0" is written to the register bits.

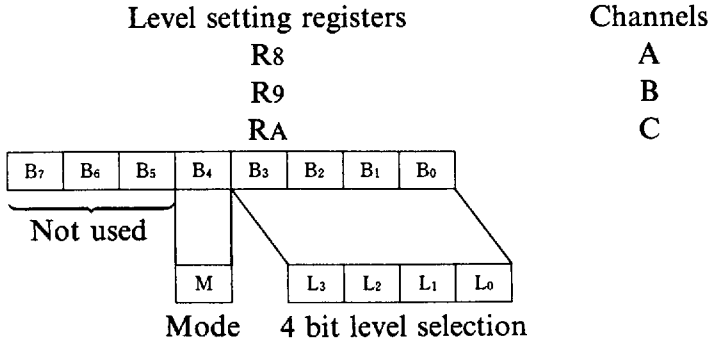
I/O port and mixer setting register R7



(Input is selected for I/O port when "0", and noise or tone can be output when "0")

(4) Level control (controlled by R8 ~ RA)

The audio level output from the D/A convertors for the three channels (A, B, and C) is adjusted by registers R8, R9, and RA).



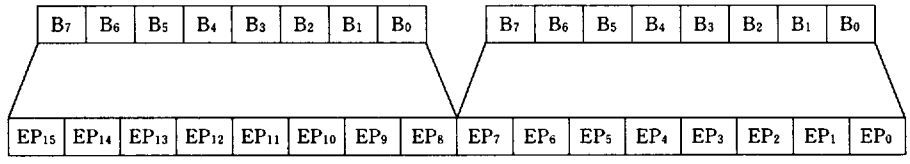
Mode M selects whether the level is fixed (when M = 0) or variable (M = 1). When M = 0, the level is determined from one of 16 by level selection signals L3, L2, L1, and L0 which compromise the lower four bits. When M = 1, the level is determined by the 5 bit output of E4, E3, E2, E1, and E0 of the envelope generator of the SSG. (This level is variable as E4 ~ E0 change over time.)

(5) Setting of envelope frequency (Controlled by RB and RC)

Thus, the envelope repetition frequency f_E is obtained as follows from the envelope setting period value EP (decimal):

$$f_E = \frac{f_{Master}}{256EP}$$ (f_{Master} is the frequency of the master clock).

Envelope rough adjustment register RC Envelope fine adjustment register RB



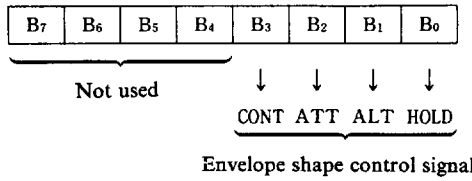
16 bit envelope period setting value (EP)

The period of the actual frequency f_{EA} used for the envelope generated is 1/32 of the envelope repetition period ($1/f_E$).

(6) Envelope shape control (controlled by RD)

The envelope generator couts the envelope clock f_{EA} 32 times for each envelope pattern cycle. The envelope level is determined by the 5 bit output (E4 ~ E0) of the counter. The shape of this envelope is created by increasing, decreasing, stopping, or repeating this counter. The shape is controlled by bits B3 ~ B0 of the register RD.

Envelope shape control register RD



The envelope can take the shapes shown in Table 4 according to combinations of the CONT, ATT, ALT, and HOLD signals.

B_3	B_2	B_1	B_0	Envelope shape
CONT	ATT	ALT	HOLD	
0	0	×	×	
0	1	×	×	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Table 4 Various envelops shapes

(7) I/O port data hold (RE and RF)

Registers RE and RF are used to store the data written from the CPU to the I/O ports, RE is used for IOA, and RF is used for IOB

2. D-A Convertor

When the maximum amplitude is normalized to 1V, the levels shown in Fig. 1 are obtained. This conversion from linear input to logarithmic output provides a wide dynamic range and a natural feeling of attenuation. (The output contains DC components of approximately 2V. Note that this discussion takes this DC level as the standard (0 level) when dealing with output voltage.)

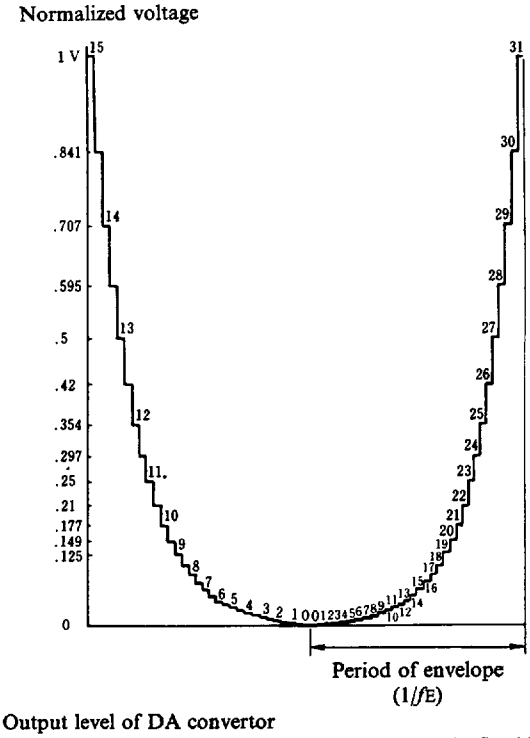


Fig. 1 Output level of DA convertor
The subscripts on the left half of the diagram are the fixed levels of the selection signals L3, L2, L1, and L0 converted into decimal values. The subscripts on the right side are decimal expressions of the envelope counter output signals E4, E3, E2, E1, and E0.

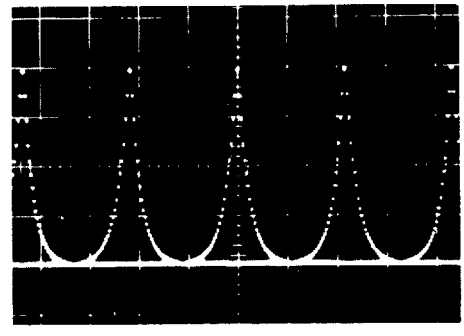


Fig. 2 Output waveform of single tone with envelope (RD = XXXX1110)

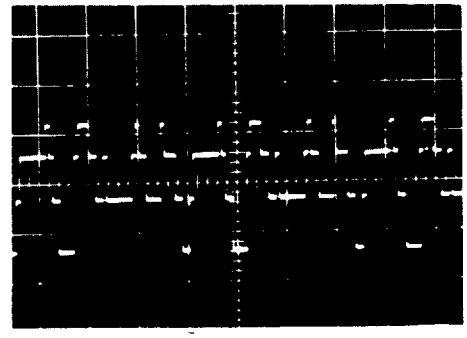


Fig. 3 Output waveform from mixing of three sounds with fixed level (R8~RA = XXX01100)

■ ELECTRICAL CHARACTERISTICS

1. Maximum allowable ratings

Item	Rating	Units
Pin voltage	−0.3 ~ +7.0	V
Operating ambient temperature	0 ~ 70	°C
Storage temperature	−50 ~ 125	°C

2. Recommended operating conditions

Item	Symbol	Minimum	Typical	Maximum	Units
Power voltage	Vcc	4.75	5.0	5.25	V
	Vss	0	0	0	V

3. DC characteristice

Item	Symbol	Conditions	Minimum	Typical	Maximum	Units
● Input pins						
Low level input voltage	V_{IL}		−0.3		0.8	V
High level input voltage	V_{IH}		2.2		Vcc	V
Input leak current	I_{LI}	V_I = 0 ~ 5V (Applicable to CLOCK, BOIR. BC1, BC2, DA0* ~ DA7)			10	μA
Pullup resistance	R_U	(Applicable to IOA0** ~ IOA7, IOB0** ~ IOB7, $\overline{RESET}$, $\overline{SEL}$, A8)	60		600	kΩ
Pulldown resistance	R_D	(Applicable to $\overline{A9}$)	60		600	kΩ
● Output pins (except analog pins)						
Low level output voltage	V_{OL}	I_{OL} = 1.6mA, C_L = 100pF	0		0.4	V
High level output voltage	V_{OH}	I_{OH} = 100μA, C_L = 100pF	2.5		Vcc	V
Output leak current	I_{LO}	V_O = 0 ~ 5V (Applicable to DA0*** ~ DA7)			10	μA
● Analog output pins						
Maximum output voltage	V_{OA}	Max. level, no mixing, R_L = 1kΩ	0.96		1.35	Vp-p
● Power supply pins						
Power supply current	I_{CC}			25	40	mA

* : DA0 ~ 7 in input mode
** : IOA and IOB in input mode
*** : DA0 ~ 7 have high impedance

4. AC characteristics

Item	Symbol	Conditions	Minimum	Typical	Maximum	Units
● Clock						
Clock frequency	fc	Max. 2MHz when $\overline{SEL}$ is high	1		4	MHz
Clock rise time	tr	Refer to Fig. 4			50	ns
Clock fall time	tf				50	ns
Duty			40	50	60	%
● Bus control						
Bus control signal switching time	tBD	Refer to Fig. 5			50	ns
● Reset						
Reset pulse width	tRW	Refer to Fig. 6	500			ns
Reset bus control delay time	tRB		100			ns
● Address mode		($\overline{A9}$, A8, DA0~7				
Address setup time	tAS	Refer to Fig. 7	300			ns
Address hold time	tAH		80			ns
● Write mode		(DA7~DA0)				
Write signal time	tDW	Refer to Fig. 8	300		10000	ns
Data setup time	tDS		0			ns
Data hold time	tDH		80			ns
● Read mode		(DA7~DA0)				
Data access time	tDA	Refer to Fig. 9			400	ns
● Inactive mode		(DA7~DA0)				
High impedance delay time	tTS	Refer to Fig. 9			100	ns

5. Capacity

Item	Symbol	Conditions	Minimum	Typical	Maximum	Units
Input capacity	CI	f = 1MHz			10	pF
Output load capacity	CL	DA0~7			100	pF

6. Timing diagrams

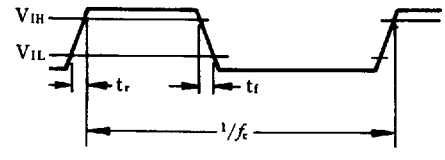


Fig. 4 Clock timing

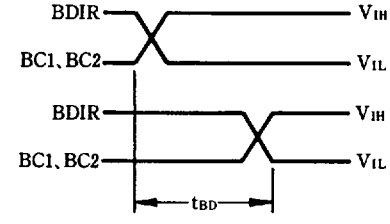


Fig. 5 Bus control timing

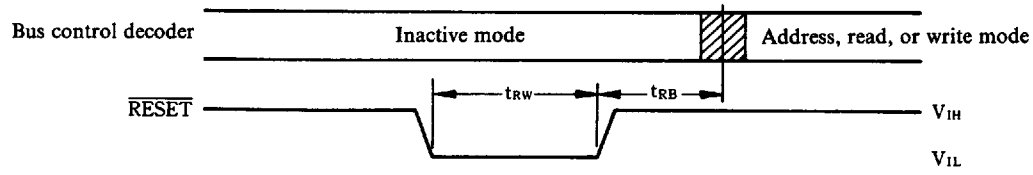


Fig. 6 Reset timing

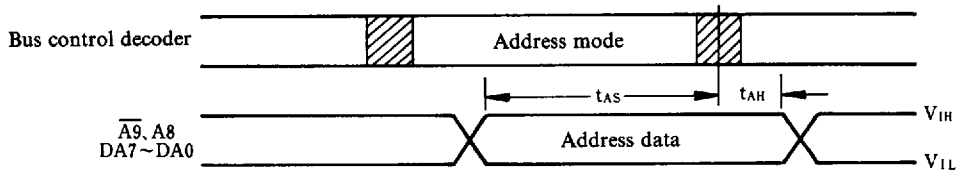


Fig. 7 Address timing

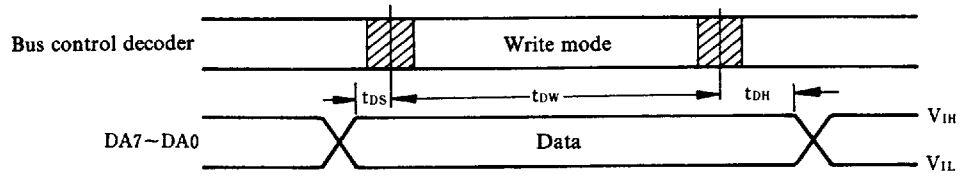


Fig. 8 Write mode

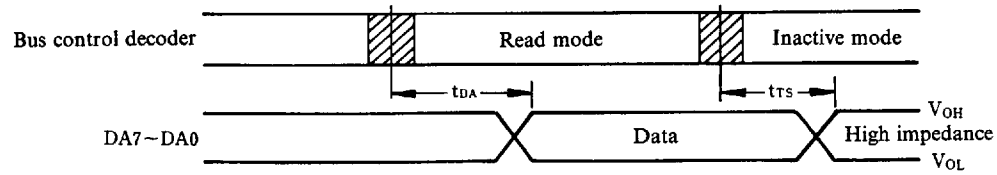
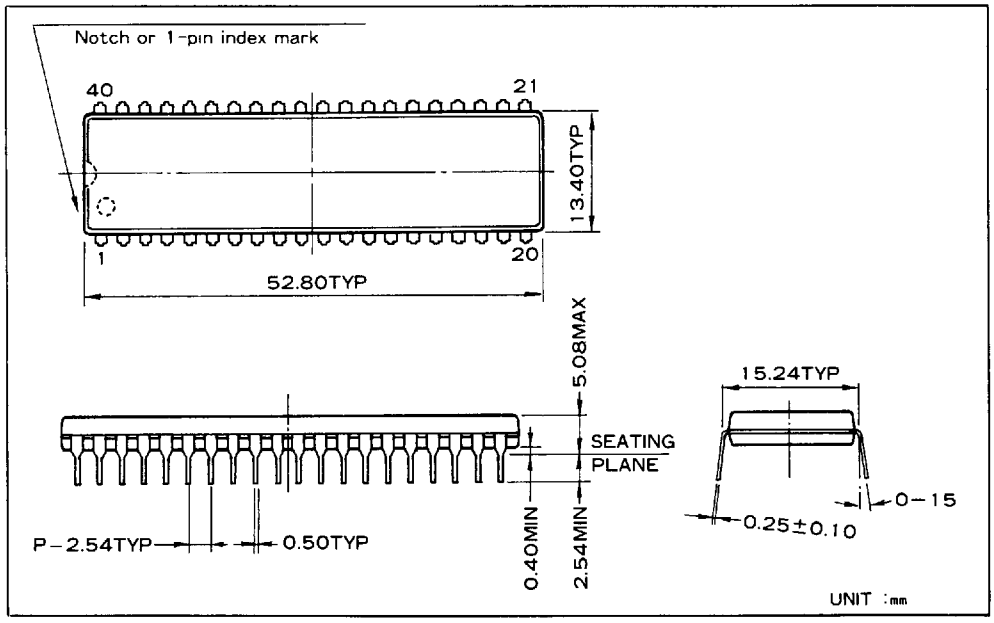


Fig. 9 Read mode

Switching time of bus control is maximum of 50ns

■ EXTERNAL DIMENSIONS



The specifications of this product are subject to improvement changes without prior notice.

AGENCY

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