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Digitizing Resistance Values

by R. Trapp

CONTENTS

1 INTRODUCTION

Resistors are used as sensing elements throughout electronics. They are cheap, available and simple to use. They bring temperature, light intensity, wiper (angular) position, force and many more parameters into the electronic world. Linearizing the characteristics is often a demanding task doing this purely in the analog domain.

Today's abilities in digital signal processing can aid in simplifying a circuit design and optimizing it in cost and PCB size requirements. Some very special sensor linearization circuitry can be replaced by software running on an off-the-shelf microcontroller doing sophisticated mathematical calculations or simply using a look up table. Even accessing measured values via the world wide web is possible. But all those need a digital representation of the resistance.

2 CONVERSION PRINCIPLE

When thinking of conversion from the analog domain into the digital domain most people instantly have the Analog to Digital Converter (ADC) of voltage type in mind. So it is required to first convert the resistance into a voltage somehow. Then this voltage is digitized as a resistance measure. Digitizing a potentiometer is easy this way but simple resistors need more circuitry. Digitizing more than one resistor needs an analog multiplexer in addition.

Several modern microcontrollers offer already the necessary circuitry on-chip, so at least these components require no extra board space. But still there is the need for circuitry to convert resistance into voltage.

2.1 RC-Time Constant Measurement

The most ancient and straight forward method uses a resistor and a capacitor to form a RC-circuit. The capacitor is charged and/or discharged via the resistor and the time needed to pass a certain threshold is measured. For example the old analog PC-joysticks (not the USB ones) worked exactly this way. The CPU triggered a 4-fold monostable and then ran a counting loop until each monostable timed out. The counts reached gave the joystick positions. A topcount ensured that the PC did not hang due to an unconnected stick. Since this is simple to implement on a microcontroller also why not doing it this way? An additional benefit might be that there is no extra circuitry to convert the resistance into voltage. And another benefit shows up: digitization of capacitances instead of resistances. The circuit remains the same and the constraints developed will apply in each case. In this document the main focus is on resistance digitization.

The experimental setup needs 4 resistors and 2 capacitors in addition to the microcontroller to digitize several potentiometers wired as variable resistors. Can you get it even simpler?

3 UNDERLYING PHYSICS

To fully understand how to optimize the circuitry for best performance the basics need to be recapitulated. Simulations were done using LTspice IV. Please check the Linear Technology website www.linear.com on how to get this software.

3.1 Charging the Capacitor

The charging circuit is presented in Fig. 1. Initially the capacitor C1 is discharged and the switch S1 is open. After 100µs S1 is closed and the voltage at node C rises exponentially due to the charge current through Pot1 into C1. At 200µs the RC-time constant is met giving ~3.16V. The resulting curve V(c) is presented in Fig. 2. V(ddr0) controls the switch state. Note that charging the capacitor to 99.966% of V_{CC} needs 8 times the RC-time constant.

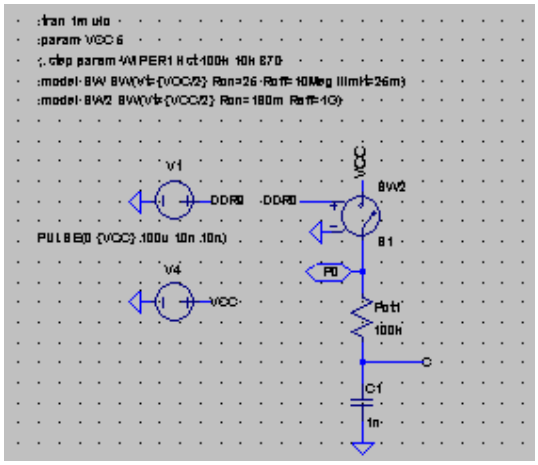

Fig. 1 – Charging Circuit

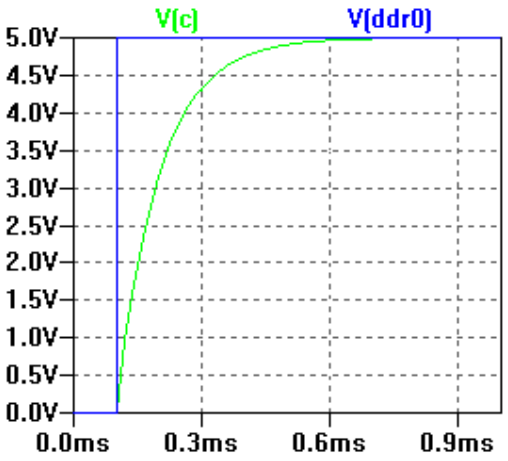

Fig. 2 – Charging Characteristic

The exponential rise of V(c) corresponds to

$$u_C(t) = U_0 \cdot \left(1 - e^{-\frac{t}{\tau}}\right) \qquad \text{Equ. 1}$$

With U_0=V_{CC} and

$$\tau = R \cdot C \qquad \text{Equ. 2}$$

Combining Equ. 1 with Equ. 2 and transforming to give t_{Thr} at the point $u_C(t_{Thr})=U_{Thr}$ reveals

$$t_{Thr} = -R \cdot C \cdot \ln\left(1 - \frac{U_{Thr}}{U_0}\right) \qquad \text{Equ. 3}$$

As is obvious the time to reach a certain threshold is linearly dependent on R, C or both. The threshold is ratiometric to the charging supply U_0.

3.2 Discharging the Capacitor

Discharging an initially charged capacitor is likewise charging. Fig. 3 presents the discharging circuit. The switch S1 only makes the simulation to initially charge the capacitor C1. At 100µs the control signal V(ddr1) closes switch S2 (switch S1 gets open) and discharging starts through R1. At 200µs the RC-time constant is met giving ~1.84V. Note that discharging C1 to 0.033% of its initial charge takes roughly 8τ.

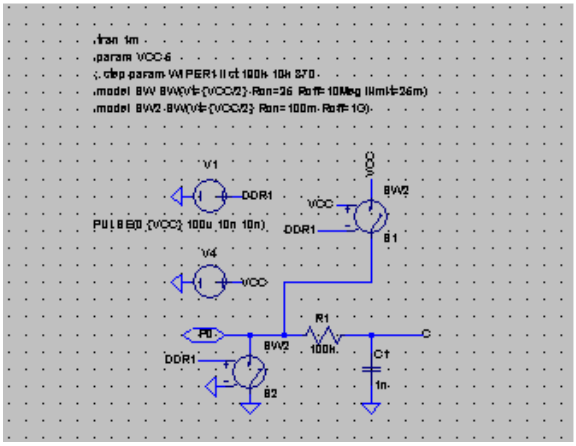

Fig. 3 – Discharging Circuit

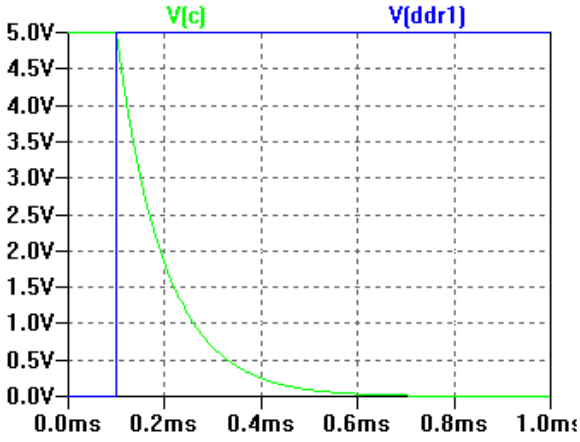

Fig. 4 – Discharging Characteristic

The exponential fall of V(c) corresponds to

$$u_C(t) = U_0 \cdot e^{-\frac{t}{\tau}} \qquad \text{Equ. 4}$$

Combining Equ. 4 with Equ. 2 and transforming to give t_{Thr} at the point $u_C(t_{Thr})=U_{Thr}$ reveals

$$t_{Thr} = -R \cdot C \cdot \ln\left(\frac{U_{Thr}}{U_0}\right) \qquad \text{Equ. 5}$$

As is obvious the time to reach a certain threshold is linearly dependent on R, C or both. The threshold is ratiometric to the charging supply U_0.

3.3 Control Sequence

The outcome of the basics on charging and discharging is not new and as expected. As is obvious there is no difference if the microcontroller measures charging time or discharging time. The thresholds used in both cases are different, of course.

Due to the close relation between charging and discharging cycle the focus is on measuring the charging cycle. Mathematics are likewise in the other case but not presented here.

The switches, controlled by a `ddr0' or `ddr1' signal, reflect the data direction setting of a microcontroller port pin. When the switch is closed the port pin drives low-impedance. When the switch is open the port is high-impedance.

So the control sequence is somewhat simple:

1. Drive logical `0' to the capacitor.
2. Wait a certain time for the capacitor to discharge completely. If not discharged completely the residual charge will falsify the next reading.
3. Drive logical `1' to the capacitor.
4. Count cycles while waiting for the capacitor voltage to cross the threshold. A comparator stage detects this.
5. The counter value is the digital representation of resistance, likewise capacitance. Loop back to step 1 for the next digitization cycle.

Counting cycles can be achieved by software and also by hardware. Depending on the microcontroller resources available the software solution might be a perfect fit.

3.4 Measuring the Charging Time

In any case a clock frequency f_{Clk} must be supplied for counting. Its inverse is the clock period T_{Clk}. So the count reached in a certain time t is determined by

$$n = \frac{t}{T_{Clk}} \qquad \text{Equ. 6}$$

Setting $t=t_{Thr}$ and applying this to Equ. 3 leads to an expression for the count n_{Thr} as a function of several parameters

$$n_{Thr} = \frac{t_{Thr}}{T_{Clk}} = -\frac{R \cdot C}{T_{Clk}} \cdot \ln\left(1 - \frac{U_{Thr}}{U_0}\right) \qquad \text{Equ. 7}$$

So at the first glance there is a wide field for adjusting T_{Clk}, U_{Thr}/U_0, R, and C to give a particular result. One aspect of interest is to determine a capacitance C to allow for a certain count n_{Thr}

$$C = -\frac{n_{Thr} \cdot T_{Clk}}{R \cdot \ln\left(1 - \frac{U_{Thr}}{U_0}\right)} \qquad \text{Equ. 8}$$

where R typically is the maximum resistance.

Limitation to the adjustments might come from errors impacting measurement precision.

3.5 Errors in Measurement

Several parasitic elements disturb the ideal measuring process. In addition noise will have an impact on the threshold detection.

3.5.1 Parasitic Capacitances

Typically a parasitic capacitance C_P is paralleling the capacitor C. It only adds and thus Equ. 7 needs an expansion.

$$n_{Thr} = -\frac{R \cdot (C + C_P)}{T_{Clk}} \cdot \ln\left(1 - \frac{U_{Thr}}{U_0}\right) \qquad \text{Equ. 9}$$

Since C_P simply adds it will affect all results the exact same way – as an offset.

3.5.2 Parasitic Resistances

Typically a parasitic resistance R_P is series-connected to resistor R. It only adds and thus Equ. 9 needs further expansion.

$$n_{Thr} = -\frac{(R + R_P) \cdot (C + C_P)}{T_{Clk}} \cdot \ln\left(1 - \frac{U_{Thr}}{U_0}\right) \qquad \text{Equ. 10}$$

Since R_P simply adds it will affect all results the exact same way – as an offset.

3.5.3 Leakage Currents

Leakage currents put a practical limit on the range of resistance R. The charging current falls exponentially. Thus too low currents will interfere with leakage currents of IO-ports or comparators. As a result there will be a time shift between the ideal trip point and the real one.

Leakage currents can be modeled by parasitic resistors paralleling the capacitor C.

It is assumed that the charging and discharging current at the threshold voltage is at least 3 to 4 magnitudes higher than any leakage current. Therefore leakage currents are neglected.

3.5.4 Noise

Due to noise at the comparator inputs the measured charging time t_{Thr} is shifted a certain value Δt. Noise influence, and thus measuring uncertainty, increases with increasing noise voltage. Also the gradient of the charging voltage comes into account since noise is less significant when this gradient is high.

Deriving Equ. 1 with respect to time calculates to be

$$u_C'(t) = U_0 \cdot \left(1 - e^{-\frac{t}{\tau}}\right) \frac{\partial u}{\partial t} = \frac{U_0}{\tau} \cdot e^{-\frac{t}{\tau}}$$ Equ. 11

Fig. 1 shows the correlation. The gradient decreases as the charging voltage rises.

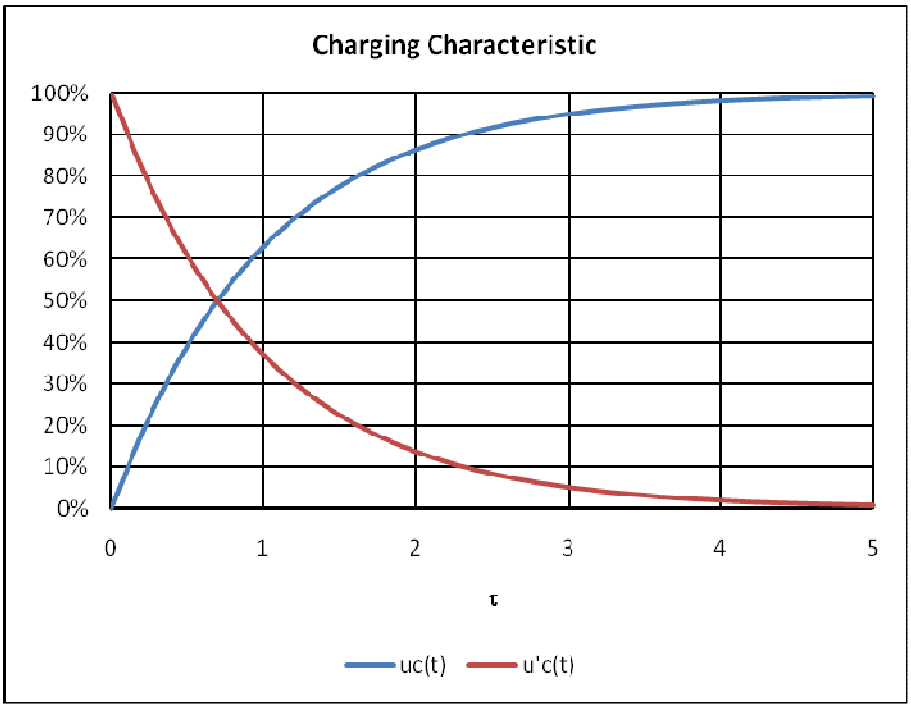

Fig. 5 – Charging Characteristic and Gradient

Replacing the charging characteristic by a linear equation in a sufficiently small period Δt, Equ. 11 gives the slope

$$\Delta u = u_C'(t) \cdot \Delta t$$ Equ. 12

Now the error in time can be expressed as a function of the superimposed noise voltage Δu at a specific point

$$\Delta t = \frac{\Delta u}{u_C'(t)} = \frac{\Delta u}{\frac{U_0}{\tau} \cdot e^{-\frac{t}{\tau}}}$$ Equ. 13

The error in time rises as the charging time rises because the gradient decreases. Thus noise of a certain amplitude will gain influence.

Scaling the absolute error in time Δt by the effective charging time t_{Thr} gives the related time error E_{tr}. This means combining Equ. 3 and Equ. 13 to give

$$E_{t_r} = \frac{\Delta t}{t_{Thr}} = -\frac{\Delta u}{U_0 \cdot e^{-\frac{t_{Thr}}{\tau}} \cdot \ln\left(1-\frac{U_{Thr}}{U_0}\right)}$$ Equ. 14

Replacing t_{Thr} by inserting Equ. 3 again the dependency on time is completely removed, leaving

$$E_{t_r} = -\frac{\Delta u}{U_0 \cdot \left(1-\frac{U_{Thr}}{U_0}\right) \cdot \ln\left(1-\frac{U_{Thr}}{U_0}\right)}$$ Equ. 15

According to this the relative error in time E_{tr} only depends on

the amplitude of the noise voltage Δu,

the available charging voltage U_0 and

the ratio of the threshold voltage and charging voltage U_{Thr}/U_0.

Neither the RC-time constant τ nor the charging time t_{Thr} will contribute to this error.

The first design considerations on least possible error contribution get obvious

The noise voltage amplitude Δu has to as low as possible.

The constant charging voltage U_0 has to be as high as possible.

The threshold voltage U_{Thr} has to be ratiometric with respect to U_0.

Looking for the optimum threshold needs to derive Equ. 15 with respect to U_{Thr}/U_0, giving

$$E'_{t_r} = -\frac{\Delta u}{U_0} \cdot \left[\frac{1}{\left(\frac{U_{Thr}}{U_0}-1\right)^2 \cdot \ln\left(1-\frac{U_{Thr}}{U_0}\right)} + \frac{1}{\left(1-\frac{U_{Thr}}{U_0}\right)^2 \cdot \left(\ln\left(1-\frac{U_{Thr}}{U_0}\right)\right)^2} \right]$$ Equ. 16

Setting Equ. 16 equal to zero and transforming it will lead – without any further proof – to a local minimum of Equ. 15 at

$$\frac{U_{Thr}}{U_0} = 1 - e^{-1} \approx 63\%$$ Equ. 17

A coefficient comparison with Equ. 1 leads to an optimum measuring time of

$$t_{Thr\_Opt} = R \cdot C = \tau$$ Equ. 18

Fig. 6 presents the result dedicated to a certain ratio of $\Delta u/U_0$. Changes to this ratio will only change the scale on the y-axis. The minimum remains constant on the x-axis.

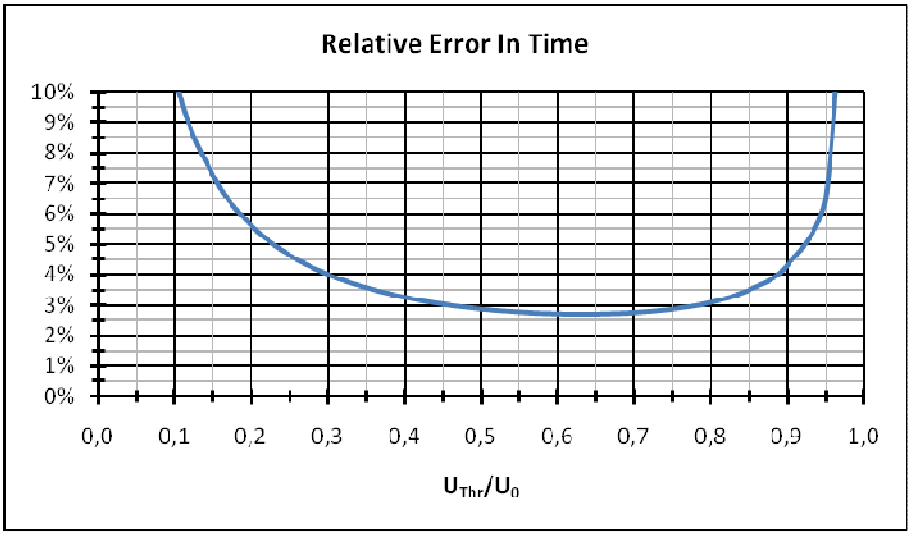

Fig. 6 – Related Error In Time $E_{tr}(U_{Thr}/U_0)$ at $\Delta u/U_0$=1%

This clearly indicates that there is an optimum ratio of U_{Thr}/U_0 at which the error related to noise gets a minimum. This minimum noise contribution always is

$$E_{t_r} = -\frac{\Delta u}{U_0 \cdot \left(e^{-1}\right) \cdot \ln\left(e^{-1}\right)} = e \cdot \frac{\Delta u}{U_0} \approx 2{,}718 \cdot \frac{\Delta u}{U_0} \qquad \text{Equ. 19}$$

Neither effective measuring time t_{Thr} nor RC-time constant τ will have an effect. Due to Equ. 15 this error only depends on U_{Thr}, U_0 and Δu.

3.5.5 Counting

A special property of the counting principle has to be considered here. Shifting the sampling point only fractions of T_{Clk} decides if the counter increments a last time or not. So this principle inherently has an uncertainty (=error) of one clock period T_{Clk}; equaling 1LSB. It is obvious that the related error E_{cr} is reciprocal to the accumulated count n

$$E_{c_r} = \frac{1}{n} \qquad \text{Equ. 20}$$

On the other hand the accumulated count n is given by the charging time t_{Thr}, reaching the threshold U_{Thr}, and the clock period T_{Clk}

$$n = \frac{t_{Thr}}{T_{Clk}} \qquad \text{Equ. 21}$$

Inserting Equ. 21 into Equ. 20 leads to the relation

$$E_{c_r} = \frac{T_{Clk}}{t_{Thr}} \qquad \text{Equ. 22}$$

As can be seen reducing E_{cr} needs the clocking period to be as short as possible and the measuring time as long as possible. Both parameters have technological constraints and thus this error cannot be made equally to zero. Refer also to Fig. 7.

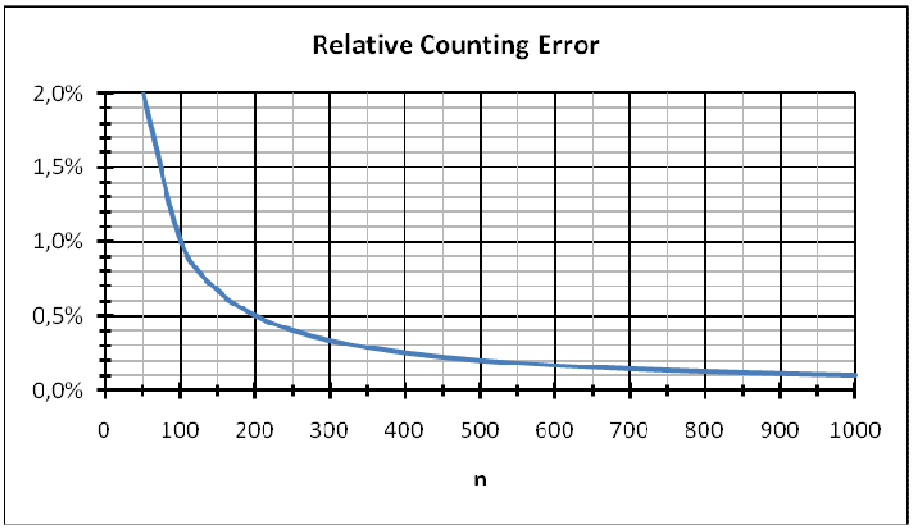

Fig. 7 – Related Counting Error $E_{cr}(n)$

A precise clock reference might be necessary but is not taken into account on the subsequent calculations.

To guarantee for a minimum precision the clock period T_{Clk} has to be adjusted to the shortest measuring time t_{min}. Equ. 22 yields a criterion on the necessary clock frequency f_{Clk}

$$f_{Clk} = \frac{1}{T_{Clk}} = \frac{1}{E_{c_r} \cdot t_{\min}} \qquad \text{Equ. 23}$$

A residual count n_0 for minimum time t_{min} follows instantaneously considering Equ. 21

$$n_0 = \frac{t_{\min}}{T_{Clk}} \qquad \text{Equ. 24}$$

On the other hand there is no counter overflow allowed when the charging time reaches its longest possible value t_{max}. The counter there reaches the value n_{max} then. Again Equ. 21 gives the count

$$n_{\max} = \frac{t_{\max}}{T_{Clk}} \qquad \text{Equ. 25}$$

So the bit depth N_{FF} (=count of flipflops) has to be selected according the common law

$$N_{FF} = lb(n_{\max}) \Leftrightarrow N_{FF} = \frac{\ln(n_{\max})}{\ln(2)}$$ Equ. 26

The resulting N_{FF} has to be rounded upwards to the next integer value.

3.5.6 Total Error

The total error here is a mixture of noise voltage and counting error. If one of those is identical to zero the result needs to be identical to the remaining error contribution; this serves as a control to the error calculation.

Parasitic R and C need not to be taken into extra account here. If they come into play, simply consider $R=(R_1+R_P)$ and $C=(C_1+C_P)$ throughout the above and below formulas.

The errors are expected not to correlate to each other and thus are said to be statistically independent of each other. In this case the total error is expressed as square mean value

$$E_{Tot} = \sqrt{\frac{E_{c_r}^2 + E_{t_r}^2}{2}}$$ Equ. 27

Controlling the expected result at $E_{cr}=0$ yields

$$E_{Tot} = \sqrt{\frac{0^2 + E_{t_r}^2}{2}} = \sqrt{\frac{E_{t_r}^2}{2}} = \frac{E_{t_r}}{\sqrt{2}}$$ Equ. 28

which does not meet the expectation. So some weighting factor has to be introduced into Equ. 27.

Checking the result at $E_{tr}=0$ is similar

$$E_{Tot} = \sqrt{\frac{E_{c_r}^2 + 0^2}{2}} = \sqrt{\frac{E_{c_r}^2}{2}} = \frac{E_{c_r}}{\sqrt{2}}$$ Equ. 29

which also does not meet the expectations. A weighting factor has to be introduced into Equ. 27 again. In both cases this weighting factor is 2 and Equ. 27 can be corrected to

$$E_{Tot} = \sqrt{\frac{2 \cdot E_{c_r}^2 + 2 \cdot E_{t_r}^2}{2}} = \sqrt{E_{c_r}^2 + E_{t_r}^2}$$ Equ. 30

Substituting for E_{cr} (Equ. 22) and E_{tr} (Equ. 15) in Equ. 30 and expressing t_{Thr} by Equ. 3 gives the total error as

$$E_{Tot} = \sqrt{\left(\frac{T_{Clk}}{-\tau \cdot \ln\left(1-\frac{U_{Thr}}{U_0}\right)}\right)^2 + \left(-\frac{\Delta u}{U_0 \cdot \left(1-\frac{U_{Thr}}{U_0}\right) \cdot \ln\left(1-\frac{U_{Thr}}{U_0}\right)}\right)^2} \quad \text{Equ. 31}$$

Transforming Equ. 31 to give T_{Clk} allows for calculating the necessary clock frequency for a maximum total error given

$$T_{Clk} = -\tau \cdot \ln\left(1-\frac{U_{Thr}}{U_0}\right) \sqrt{E_{Tot}^2 - \left(-\frac{\Delta u}{U_0} \cdot \frac{1}{\left(1-\frac{U_{Thr}}{U_0}\right) \cdot \ln\left(1-\frac{U_{Thr}}{U_0}\right)}\right)^2} \quad \text{Equ. 32}$$

Furthermore it might turn out that the criterion for minimum related time error E_{tr} from Equ. 16 does not keep valid when considering the total error E_{Tot}. So Equ. 31 has to be derived with respect to U_{Thr}/U_0

$$E_{Tot}^{'} = \frac{T_{Clk} \cdot U_0^2 \cdot \tau \cdot \left(1-\frac{U_{Thr}}{U_0}\right) + \Delta u \cdot U_0 \cdot \tau^2 \cdot \left[1+\ln\left(1-\frac{U_{Thr}}{U_0}\right)\right]}{T_{Clk}^2 \cdot U_0^2 \cdot \left(1-\frac{U_{Thr}}{U_0}\right)^2 + \Delta u^2 \cdot \tau^2} \quad \text{Equ. 33}$$

Setting the numerator of Equ. 33 equal to zero will give the extremas

$$0 = T_{Clk} \cdot U_0^2 \cdot \tau \cdot \left(1-\frac{U_{Thr}}{U_0}\right) + \Delta u \cdot U_0 \cdot \tau^2 \cdot \left[1+\ln\left(1-\frac{U_{Thr}}{U_0}\right)\right] \quad \text{Equ. 34}$$

Unfortunately it is not possible to analytically solve this expression for U_{Thr}/U_0. If the exact value is required a numerical approach has to be used, U_0, Δu, τ and T_{Clk} have to be given in this case.

In most situations the ratio U_{Thr}/U_0 is fixed for some reasons. In this case there is the possibility to optimize the ratio T_{Clk}/τ. Equ. 35 is a transformation of Equ. 34 coming handy to determine the optimum ratio

$$\frac{T_{Clk}}{\tau} = -\frac{\Delta u}{U_0 - U_{Thr}} \cdot \left[1+\ln\left(1-\frac{U_{Thr}}{U_0}\right)\right] \quad \text{Equ. 35}$$

As Equ. 34 is the criterion for the total error E_{Tot} to get minimal at a certain ratio U_{Thr}/U_0 it should be obvious that physically meaningful results needs t_{Clk}/τ to be always positive. Another limitation is that the denominator U_0-U_{Thr} must not be equal to zero and always be positive. Thus U_{Thr} is limited to the interval (0..U_0(. So the partial expression inside the square brackets has to be always negative. This leads to the condition

$$1+\ln\left(1-\frac{U_{Thr}}{U_0}\right)<0 \Leftrightarrow \frac{U_{Thr}}{U_0}>1-e^{-1} \Leftrightarrow \frac{U_{Thr}}{U_0}>\approx 63\% \qquad \text{Equ. 36}$$

Compare this to Equ. 17. Anyway the conclusion is that the optimum ratio U_{Thr}/U_0 for least possible total error E_{Tot} is above the value given by Equ. 17.

In any case it must be ensured that the denominator polynomial of Equ. 33 does not equal zero! This condition is expressed as

$$0\neq T_{Clk}^2\cdot U_0^2\cdot\left(1-\frac{U_{Thr}}{U_0}\right)^2+\Delta u^2\cdot\tau^2 \Leftrightarrow 1\neq\frac{\Delta u\cdot\tau}{U_0\cdot T_{Clk}}+\frac{U_{Thr}}{U_0} \qquad \text{Equ. 37}$$

To derive a plot of the total error some parameters need to be selected:

T_{Clk} = 500ns ⇔ f_{Clk} = 2MHz

τ = 50µs (e.g. R = 50kΩ; C=1nF)

$U_0 = V_{CC}$ = 5V

Δu = 20mV (the noise voltage)

The resulting plot is shown in Fig. 8. The minimum total error is located roughly at U_{Thr}/U_0=0.75 which is definitely in contrast with the outcome of Equ. 17! You might want to refer to Fig. 6 as a comparison.

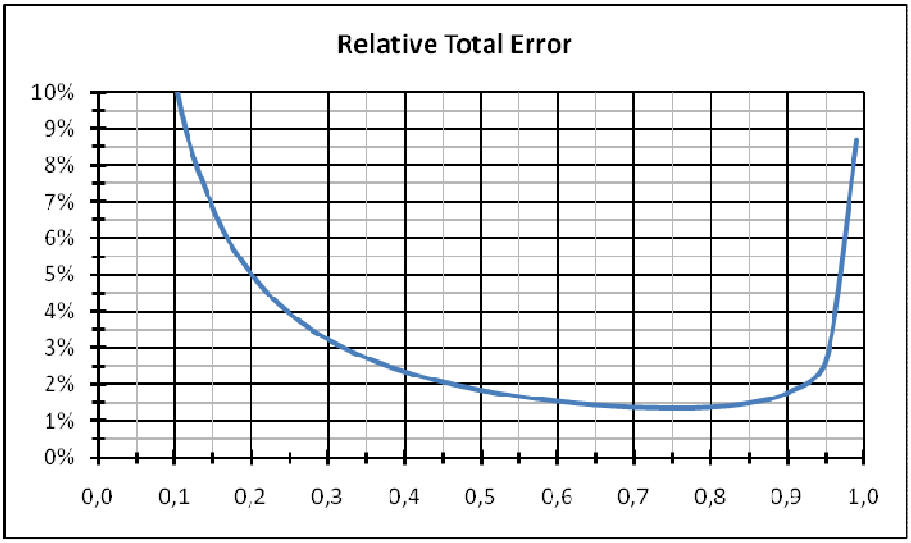

Fig. 8 – Total Error $E_{Tot}(U_{Thr}/U_0)$

According to Equ. 7 using these parameters and this U_{Thr}/U_0 setting gives a topcount of n_{max}=139.

4 A PRACTICAL CIRCUIT

What has been encountered will find its way into a reasonable setup. The constraints found so far are:

- Charge the capacitor through a variable resistor until a threshold is met. Count T_{Clk} cycles while charging. This gives the digitized value.
- Select the threshold to be at least 63% of the supply voltage. Use a resistive divider network to allow for ratio U_{Thr}/U_0. Using a R/2R setup gives a threshold of 2/3≈66.7% the supply voltage. This is a good starting point but might not be the exact optimum.
- Keep noise pickup as low as possible.
- Select $V_{CC}=U_0$ as high as possible.
- Constrain desirable total error and select f_{Clk} and N_{FF} accordingly.

From this some additional ideas arise directly:

- Discharge the capacitor through a fixed low value resistor. This allows for fast discharge times and thus virtually no residual charge falsifying the next result. A minimum resistance is required to keep the discharging current peak at low levels.
- While discharging the capacitor the variable resistor does not need to be connected. This will save energy since otherwise a current will flow through it while in the preparing condition. To further shorten the discharge cycle it is possible to connect the variable resistor to GND paralleling the fixed resistor in this case. When maximum resistance is connected this effort might be waste but in multichannel setup this aids in discharging by paralleling all resistors.
- Charge the capacitor through a fixed low value resistor series-connected to the variable resistor. This prevents large currents from flowing if the variable resistance gets too low, typically the case with a potentiometer near its start position. Maybe one common resistor is sufficient in a multichannel setup. Of course, the discharging path needs to be disconnected while charging.

4.1 Single Channel Setup

As mentioned earlier it is possible to use only some discrete resistors and capacitors in addition to the microcontroller. So the biggest point remaining is: which microcontroller to choose?

A broad range of microcontroller architectures from different suppliers is available on the market. The microcontroller finally chosen is an Atmel's ATtiny2313. It has been elected for nothing else but that it has been already in the drawer and used for some other experiments before. It features an analog comparator and a capture unit. The latter one is not necessary to get first results but the on-chip analog comparator is very welcome to obsolete extra circuitry. Communication uses I²C which gets some rudimentary support by the microcontroller's hardware (USI).

A first draft of the experimental circuit is shown in Fig. 9.

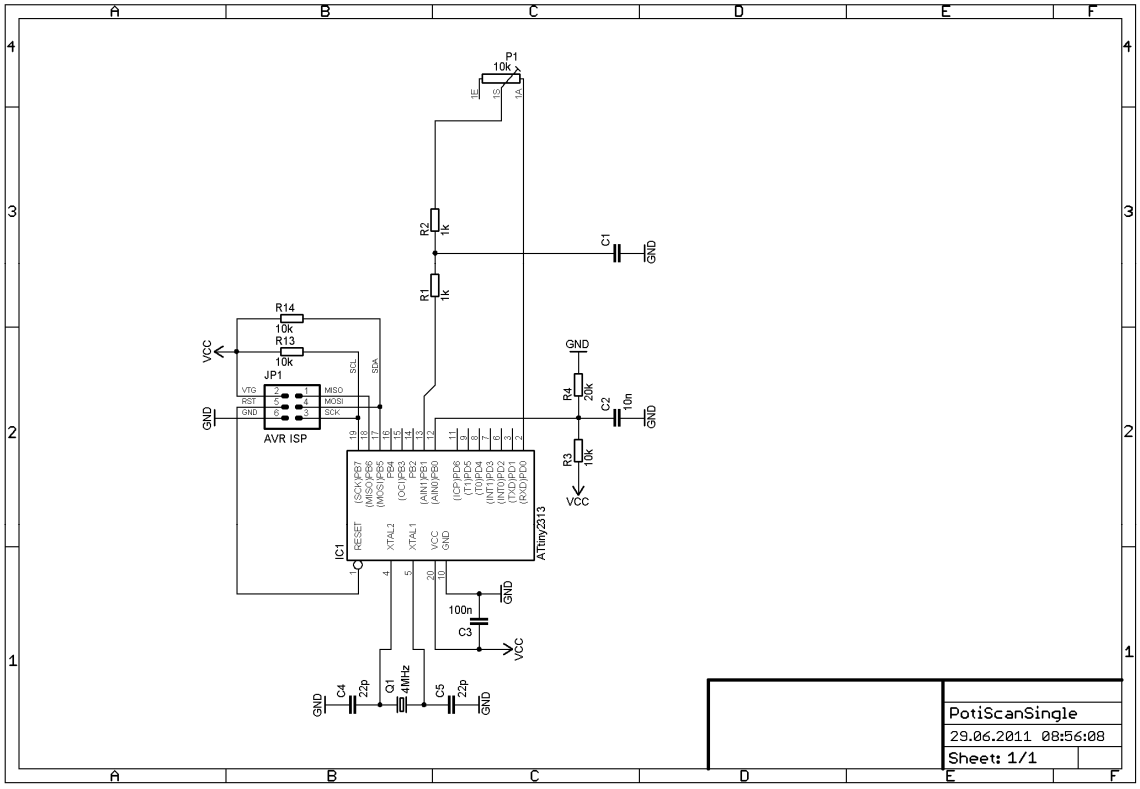

Fig. 9 – Single Channel Circuit

Voltage supply circuitry is already available on the evaluation board used (STK500). The ATtiny2313 is inserted into the appropriate socket. The necessary analog parts (fixed resistors, variable resistors and capacitors) are assembled on a project board and connected to the STK500 headers by wiring. The crystal is inserted into the evaluation board's socket and made to drive the microcontroller. When used as an I²C device all supply and communication are done using JP1.

Constraints to the circuit are:

$V_{CC} = U_0 = 5V$

$U_{Thr} = 2/3V_{CC} \approx 3.33V$ (set by R_3 and R_4)

$R_{POTI} = 0k\Omega..100k\Omega$

$R_1 = R_2 = 1k\Omega$

$E_{Tot} \leq 2.34\%$

$\Delta u \leq 10mV$ (as an expectation)

$C_1 = 10nF$ (as a starting point)

The first thing to consider is when the total error is highest, at the minimum or the maximum RC-time constant? Obviously it is at the minimum RC-time constant

$$\tau_{\min} = R_2 \cdot C_1 = 10\mu s$$

Using this RC-time constant and the remaining parameters from above with Equ. 32 will give the maximum clock period required to be

$$T_{Clk} = 250ns \Leftrightarrow 4MHz$$

The minimum charging time t_{Thr_min} can be calculated using Equ. 3 and gives

$$t_{Thr\_\min} = 10986ns$$

And together with Equ. 6 this leads to the minimum count

$$n_0^* = 43.944$$

which must be rounded downward to

$$n_0 = 43$$

Keep in mind that at this point the relative total error is 2.34% since this condition served to calculate the clock frequency. The uncertainty here is mainly due to the relative counting error giving

$$n_{0\_err} = 43 * 2.34\% = 1.0062 \approx 1$$

which meets the expectation.

At maximum resistance R the RC-time constant gets

$$\tau_{\max} = (R_{POTI} + R_2) \cdot C = 1010\mu s$$

So the maximum charging time t_{Thr_max} is

$$t_{Thr\_\max} = 1109598ns$$

This time, when calculating the maximum count n_{max}, the result has to be rounded upward

$$n_{\max} = 4439$$

The total error here reduces to

$$E_{Tot} = 0.55\%$$

According to Equ. 26

$$N_{FF} = 13$$

flipflops are necessary to store this result. This is quite a fine resolution. But due to the relative total error the precision is reduced and some LSBs get obsolete. Here the uncertainty in the result is

$$n_{\max\_err} = 4439 * 0.55\% = 24.4145 \approx 25 \Leftrightarrow 4.61bit \approx 5bit$$

So from the 13bits holding the result the 5 LSBs are prone to errors leaving 8 MSBs to rely on.

Changing the clock frequency can lower down the error but only at the lower extends of the range. As the resistance rises, noise gains more and more influence masking the effect of rising the clock frequency.

Assuming that the stability of the microcontroller's internal RC oscillator is not sufficient an external crystal (Q_1) and tank circuit (C_4, C_5) is used. C_3 is the recommended decoupling capacitor on the supply lines. The I²C-communication runs via connector JP_1, `AVR ISP', allowing also for In-System-Programming of the microcontroller. The optional resistors R_5 and R_6 perform pull-up to the I²C-bus wires.

The basic hookup is complemented by the threshold divider R_3 and R_4. C_2 decouples this node. So the comparator receives a reference ratiometric to the supply at its positive (+) input.

The negative (-) comparator input is connected via R_1, C_1 and R_2. While discharging the output PB1 drives `0'. $P_1$ is either disconnected by becoming PD0 an input or, better for several reasons, PD0 drives also `0'. Discharging current now runs through R_1 and in addition through R_2 plus P_1. The maximum discharge time constant thus is

$$\tau_{\max\_dis} = R_1 \cdot C_1 = 1k\Omega * 10nF = 10\mu s$$

Waiting for at least 8 times this value ensures that in any case the residual charge is negligible in the next cycle. After these 80µs PB1 becomes an input (= Hi-Z). The comparator output reads as `1' when the threshold is not exceeded due to the hardware setup.

The charging cycle now starts with PD0 driving `1' to $P_1$. The charging current runs through $P_1$ and $R_2$ giving the effective charging time constant. As soon as the voltage at AIN1 crosses the threshold voltage at AIN0 the comparator output reads as `0' denoting the end of the charging cycle. The count is taken as output and the discharge cycle is entered again.

4.2 Multichannel Setup

While all constraints from the single channel setup stay valid there is the need to attach and detach several variable resistors one by one to the charging and discharging process.

Extending the control sequence a little bit instantly gives way to avoiding an analog multiplexer. Simply attach one port pin to each resistor. Making the corresponding port Hi-Z will effectively prevent the resistor from charging C_1. Have the port pin to drive `0' will contribute to discharging. Driving `1' only one port at a time, while all other's are high impedance, ensures that only this circuit will charge C_1 and thus get measured.

In the single channel example there are up to 10 port pins left for extending the scan up to 11 resistors totally. *ATTENTION: P11 needs to be adjusted to maximum resistance to allow for reflashing*.

This maximum channel setup is shown in Fig. 10. Keep in mind that this multichannel setup only has one measuring range so all resistors P_1..P_{11} have the same value. Multiple ranges are addressed in the next chapter.

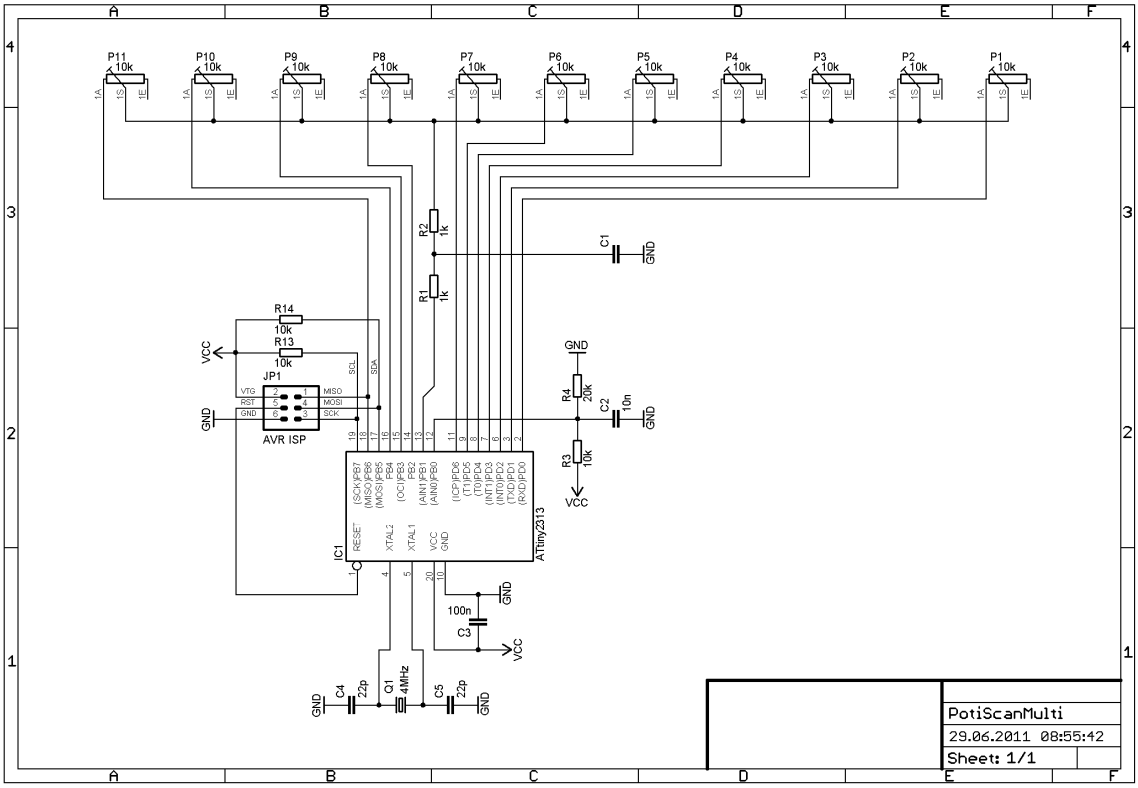

Fig. 10 – Multichannel Circuit

When comparing to the single channel setup, there are only the 10 variable resistors P_2..P_{10} added. Nothing else, especially no analog multiplexer circuitry!

But there is also a drawback to this simple setup: since all ports in Hi-Z state see the charge build up across their respective resistive connection all digital input stages have a relatively slow transition through the undefined voltage range. So on each port pin this causes increased quiescent current through the input stage transistors. This might show as a substantial current peak in the voltage supply and deny this simple setup in some cases. Discharging is not critical since the respective ports drive '0' and thus do not see the discharge voltage curve.

4.3 Adding Ranges

When considering an application where two (or more) different types of variable resistors are used, each range could get its own multichannel digitizing hardware. But typically there is no need for several dozens of

channels. The optimum way then is to modify the circuit to have multi range properties.

Since the key parameter to a dedicated count is the RC time constant it is obvious that not only changing the resistance of P_1 but also changing the capacitor C_1 will change the resulting count. A change in resistance can thus be compensated by an appropriate change in capacitance leaving the RC time constant unchanged.

Changing the capacity could be an easy job when slightly changing connections. The timing capacitor C_1 is not connected to GND with its second plate. Now it connects to a port pin. Another timing capacitor C_x also gets connected to a dedicated port pin and to the charging node.

Equ. 8 instantly gives a value for the new total capacity when simply inserting all parameters selected so far.

Setting C_x 10 times the value of C_1 adds a second range of R_{POTI} = 0kΩ..10kΩ. This takes not into account the current limiting series resistor R_2. Since it remains constant in one case it contributes 1% of the range, 10% in the other. The topcount also changes because one range is 101:1 the other is only 11:1. Interestingly enough the counting difference can be made to be equally in both cases, thus giving an equal scaling factor. So only zero resistance count (= offset) and topcount will vary.

Leaving C_1 always connected and having the range changed only by applying C_x or leaving it switched off preserves one port pin. In this case C_x is only 9 times the value of C_1. Again the difference count can be made equally in both cases. This scheme can be extended on more capacitors to have more ranges. Furthermore turning on and off combinations of capacitors can give additional ranges at no additional cost.

In either case some mathematics needs to be done to adjust the ratio C_x/C_1 in a way that range changes do not affect the scaling (= difference count). Unfortunately the offset is changed but compensating for it should be a trivial task. Especially when considering the EEPROM section of the microcontroller there are enough resources to store some adjustment settings, like offsets, for each range. Since a clever setup takes advance from scaling factors not to change the microcontroller has only to add an specific offset and apply one scaling factor in the end, if any.

Fig. 11 presents a setup having two ranges dedicated to 0Ω..10kΩ and 0Ω..100kΩ. Only 10 resistive channels are available here. The setup might suffer from problems during ISP attempts due to the series capacitance of C_x and C_1 loading the MISO line. Any other assignment of C_x and P_1..P_{10} to the port pins of the microcontroller is also possible.

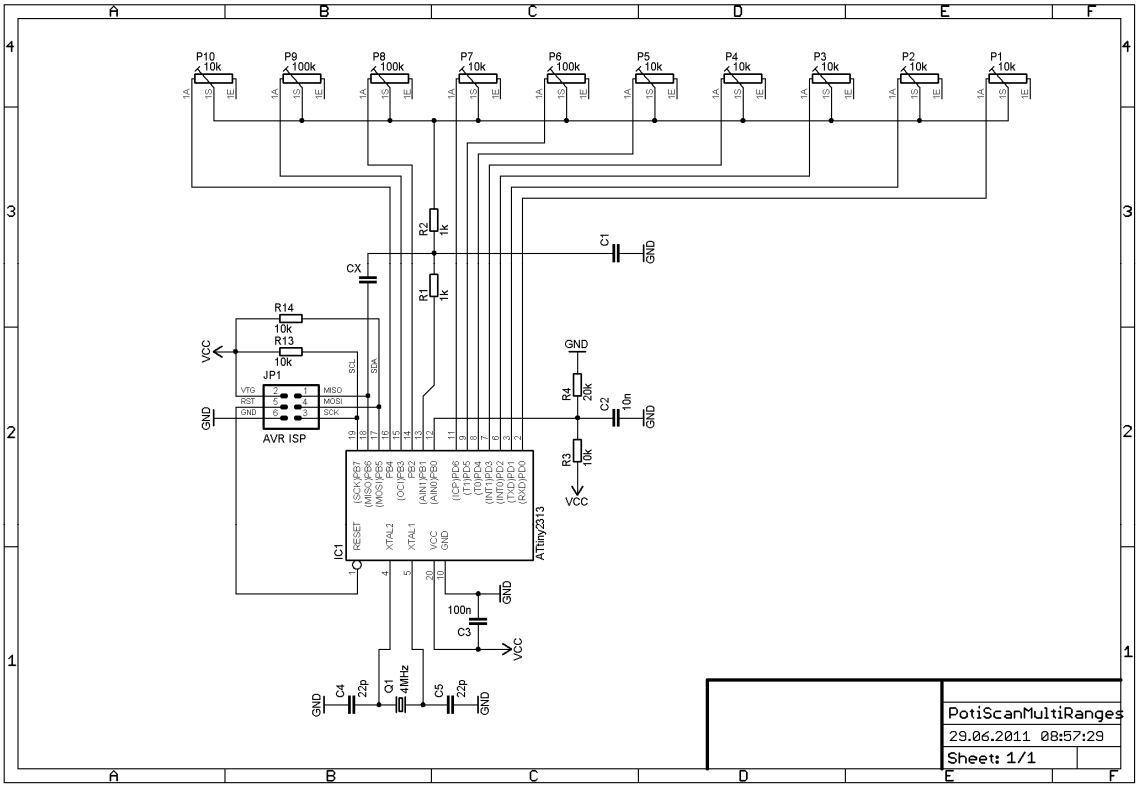

Fig. 11 – Multichannel Circuit With Multiple Ranges

5 CONCLUSIONS

Laboratory data of the experimental setups confirms the expectations are met. The key to increase precision is to reduce noise during charging time. It has to be kept as low as possible.

On the other hand there is the question about the reasonable resolution. When thinking about a potentiometer there is commonly a turning angle of 270°. In theory its resistance is absolutly proportional to the angular wiper position. But in practice this linearity is not met due to mechanical and electrical variations of the resistive layer. Another limit is the user's inability to turn the axle fractions of 1° and expecting the wiper to follow this very small movement, normally it will not. As the user slightly increases the rotational force to overcome the wiper's and axle bearings' residual momentums the wiper jumps. Experience states that digitizing a potentiometer needs no more than 7 bit of precision. The finer the granularity is the harder it gets to repeat a certain setting.

Depending on the microcontroller's features there are only some passive external components necessary to configure the digitizer. A couple of resistors can be connected with minimum additional circuitry.

The design is scalable for count of channels. Having the circuit ready to digitize more than only one resistive range makes it even more versatile. Digital adjustment of ranges allows for unified readout of values.

Also the circuit can be made to shut down minimizing its power consumption.

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7 DOCUMENT HISTORY

Revision	Date	Comment
1.0		Released to the public domain.
	26. Jul. 2011	Wording improved, typos fixed.
	14. Jul. 2011	Wording improved, typos fixed.
	29. Jun. 2011	Reworked some pictures, copyright note and disclaimer. The cross reference problem disappeared by itself.
	28. Jun. 2011	Added idea about multiple ranges. Added copyright note and disclaimer.
	27. Jun. 2011	Finalized description of single channel setup, added multichannel setup. Faced severe problems when trying to add cross references to figures or equations – currently no solution.
	21. Jun. 2011	Contents of an older german H.A.R.R.Y. report on error budget of monostable circuitry translated, adapted and inserted.
	20. Jun. 2011	Initial creation of template from rather old „Lastmessung am Schrittmotor"; reworked layout completely.

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