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14CS45

Fourth Semester B.E. Degree Examination, April/May 2016
Computer Science and Engineering
Computer Organization and Architecture (14CS45)

Time:3Hrs Max. Marks:100

Instructions:
1. Answer one full question from each unit.
2. Any missing Data can be suitably assumed.
3. Draw neat diagrams wherever necessary.

UNIT-I

				CO; BL
1.	a.	Discuss how the performance of a computer can be measured. What are the measures to improve the performance of a computer?	08 Marks	3;2
	b.	Briefly discuss Pipelining and superscalar operation	04 Marks	2;1
	c.	Discuss different interrupt priority schemes.	08 Marks	2;2
2.	a.	Showing different functional units of a computer mention function of the processor registers i) PC ii) MAR iii) IR	08 Marks	2;2
	b.	Explain exceptions with suitable examples.	06 Marks	2;1
	c.	Describe Enabling and Disabling of interrupts.	06 Marks	2;1

UNIT-II

3.	a.	Describe serial interface with neat diagram	08 Marks	2;1
	b.	Summarize multilevel memories	08 Marks	2;2
	c.	Describe hit rate and miss rate	04 Marks	2;2
4.	a.	Describe Replacement algorithm with suitable examples.	08 Marks	2;1
	b.	Classify memory hierarchy depending on speed, size and cost	08 Marks	2;2
	c.	List advantages and disadvantages of PCI bus	04 Marks	2;1

UNIT-III

5.	a.	What do you mean by virtual memory? Explain virtual address translation in virtual memory.	08 Marks	3;2
	b.	Explain a 4-bit carry look ahead adder.	07 Marks	3;2
	c.	Write a note on Guard bit and transaction	05 Marks	3;1
6.	a.	With an example, explain the Booth algorithm	10 Marks	3;2
	b.	Discuss the following: i) IEEE standard for floating point numbers ii) Binary addition-subtraction logic network.	10 Marks	3;3

UNIT-IV

7.	a.	Write the differences between hard-wired and micro-programmed control	08 Marks	2;1
	b.	Discuss the execution of a complete instruction.	07 Marks	2;3
	c.	Write a note on instruction hazards	05 Marks	2;2
8.	a.	Describe 3-bus organization with suitable diagram.	08 Marks	3;2
	b.	Write the micro routine for the "branch < 0" instruction.	06 Marks	2;3
	c.	With suitable examples illustrates the idea of instruction pipelining	06 Marks	2;2

UNIT-V

9.	a.	Describe parallel I/O ports with diagram	10 Marks	5;1
	b.	Describe Digital camera application with a block diagram.	10 Marks	5;1
10.	a.	Describe processor chips for embedded application with block diagram.	12 Marks	5;1
	b.	Describe single microcontroller with schematic diagram.	08 Marks	5;1

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Fourth Semester B.E. Degree Examination, April / May 2017
Computer Science and Engineering
Computer Organization and Architecture (14CS45)

Max. Marks:100

Instructions: 1. Answer one full question from each unit.
2. Any missing Data can be suitably assumed.

UNIT-I

				CO; BL
1.	a.	Showing different functional units of a computer, Mention function of the processor registers i) PC ii) MAR iii) IR	08 Marks	1;2
	b.	With the help of a simple circuit explain how a common interrupt request line can be implemented.	08 Marks	1;3
	c.	Discuss exception with suitable examples.	04 Marks	1;2
2.	a.	Discuss how the performance of a computer can be measured. What are the measures to improve the performance of a computer?	09 Marks	1;3
	b.	With a neat diagram explain any one method of handling multiple I/O devices.	06 Marks	1;3
	c.	How single bus structure used to interconnect functional units in computer system.	05 Marks	1;2

UNIT-II

3.	a.	Explain serial interface with a block diagram.	08 Marks	2,3;2
	b.	Discuss the advantages and disadvantages of PCI bus.	04 Marks	2,3;2
	c.	Explain the multilevel memory.	08 Marks	2,3;2
4.	a.	Paraphase on i) Hit rate ii) Miss penalty	06 Marks	2,4;2
	b.	Describe the memory hierarchy based on i) Speed ii) Size iii) Cost	09 Marks	2,3;2
	c.	Explain the significance of DMA controller. Also explain the centralised methods of bus arbitration.	05 Marks	2,3;2

UNIT-III

5.	a.	With a neat block diagram, explain organization of virtual memory.	08 Marks	3;2
	b.	Design a 16 bit carry look ahead adder from 4 bit adders.	08 Marks	3;6
	c.	Explain, IEEE standard for floating point numbers.	04 Marks	3;1,2
6.	a.	Using a neat block diagram, explain a floating point addition and subtraction unit.	08 Marks	3;3
	b.	With the help of the block diagram, explain the circuit for integer division.	08 Marks	3;2,3
	c.	Explain Guard bits and transactions.	04 Marks	3;2

UNIT-IV

7.	a.	Write the differences between hardwired and micro-programmed control.	08 Marks	4;2
	b.	Describe 3-bus organization with suitable diagram.	08 Marks	4;3
	c.	Write the micro routine for instruction branch <0.	04 Marks	4;3
8.	a.	Write the control sequence for the execution of the instruction Add (R3), R_1	08 Marks	4;3
	b.	Discuss single bus organization of data path inside a processor.	07 Marks	4;2
	c.	With suitable example explain the idea of instruction pipelining.	05 Marks	4;3

UNIT-V

9.	a.	Explain the following embedded system i) Digital camera ii) Home telemetry	10 Marks	4;2

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b. Paraphrase on
   i) Polling approach
   ii) Interrupt approach

10 Marks 4;2

10. a. Describe processor chips for embedded applications with block diagram. 12 Marks 4;2

b. Explain a simple microcontroller with neat schematic diagram. 08 Marks 4;1

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Supplementary Semester End Examination, July 2017
Fourth Semester
Computer Science and Engineering
Computer Organization and Architecture (14CS45)

Instructions: 1. Answer one full question from each unit.
2. Any missing Data can be suitably assumed.

Max. Marks:100

UNIT-I

			CO; BL
a.	Explain the history of computer developments from first generation to fourth generation.	08 Marks	1;2
b.	Summarize the accessing of Input / Output devices.	06 Marks	1;2
c.	Discuss basic input and output operations.	06 Marks	1;1,2
a.	Describe functions of the following a) PC b) MAR c) MDR d) IR e) GPR	05 Marks	1;1
b.	Using the neat block diagram, explain any two methods for handling multiple I/O devices.	10 Marks	1;3
c.	Compare the followings i) Pipelining and scalar operations ii) CISC and RISC Instruction set	05 Marks	1;4

UNIT-II

a.	Showing the possible register configurations in DMA interface explain direct memory access.	08 Marks	2;2
b.	Elaborate distributed bus arbitration scheme in detail.	08 Marks	2;3
c.	Bring out hit rate and miss penalty.	04 Marks	2;2
a.	Discuss how the impact of cache on the overall performance of a computer can be calculated.	08 Marks	2;3
b.	Give the memory hierarchy depending on speed, size and cost.	05 Marks	2;2
c.	What are functions of an I/O interface? Explain with block diagram I/O interface between a key board and a processor.	07 Marks	2;3

UNIT-III

a.	Describe virtual memory organization with suitable diagram.	08 Marks	3,;2
b.	Discuss boot algorithm with an example.	08 Marks	2,;2
c.	Paraphrase on Guard Bits and Trnasaction.	04 Marks	3,4;3
a.	Discuss 16 bit carry look ahead adder built from 4 bit address.	08 Marks	3,4;3
b.	Explain floating point addition subtraction unit with a block diagram.	08 Marks	3,3;3
c.	Paraphrase on IEEE standard for floating point numbers.	04 Marks	3;2

UNIT-IV

a.	Compare hardwired and micro programmed control.	08 Marks	4;4
b.	Write and explain the timing diagram for memory read operation.	08 Marks	4;2,3
c.	Write a note on instruction hazards.	04 Marks	4;2
a.	Discuss the organization of conditional branching control unit in the micro program.	10 Marks	4;2
b.	Describe the following with respect to data hazards i) Operand forwarding ii) Handling data hazards in software iii) Side effects	10 Marks	4;1,2

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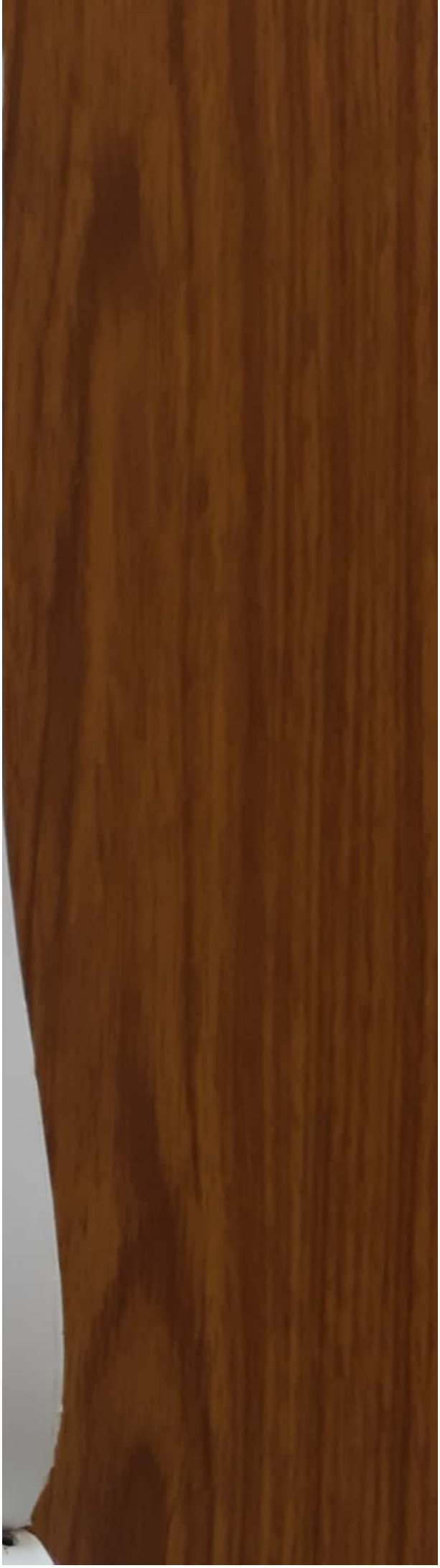

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Fourth Semester B.E Degree Examination, April/May 2018
Computer Science and Engineering
Computer Organization and Architecture (14CS45)

Max. Marks:100

Instructions: 1. Answer one full question from each unit.
2. Any missing Data can be suitably assumed.

			Marks	CO/PO; BL
		UNIT-I		
1.	a.	Explain the different functional units of a computer with a neat diagram. And also explain the function of the following processor register i) PC ii) MAR iii) IR iv) MDR	12 Marks	2/2,3;2
	b.	Describe the history of Computer developed from first generation to fourth generation computers	08 Marks	2/2,3;2
2.	a.	Briefly explain any two methods of handling Multiple I/O devices with a neat diagram	10 Marks	3/2,3;3
	b.	Explain the following with an example for each i) Pipelining and Superscalar operation. ii) SISC & RISC instruction sets. iii) Compiler	10 Marks	2/2,3;2
		UNIT-II		
3.	a.	Showing the possible register configuration in DMA interface explain Direct Memory Access.	08 Marks	2/B;2
	b.	What are the functions of an I/O interface? Explain with block diagram I/O interface between a keyboard and processor.	08 Marks	2/C;2
	c.	Bring out Hit rate and Miss penalty.	04 Marks	2/C;2
4.	a.	Explain how the impact of cache on the overall performance of a computer can be calculated.	07 Marks	2/C;3
	b.	What is the necessity of DMA Controller? Explain the centralized method of bus arbitration.	07 Marks	2/C;3
	c.	Give the memory hierarchy depending on speed, size and cost.	06 Marks	2/C;3
		UNIT-III		
5.	a.	Describe virtual memory organization with suitable diagram.	08 Marks	2/2,3;2
	b.	Discuss 16-bit carry look ahead adder built from 4-bit adders.	06 Marks	3/2,3;3
	c.	Elaborate the sequential binary multiplier with the help of a block diagram.	06 Marks	2/2,3;2
6.	a.	With the help of block diagram explain the virtual memory address translation.	08 Marks	2/2,3;2
	b.	Discuss Booth algorithm with example.	09 Marks	2/2,3;3
	c.	Write short notes on Guard bits and transaction.	03 Marks	3/2,3;2
		UNIT-IV		
7.	a.	Differentiate between hard wired and micro programmed control.	08 Marks	2/2 ,3;2
	b.	Give the control sequence for the execution of the instruction i) Add(R3),R1 ii) For unconditional branch instruction	12 Marks	3/2 ,3;3
8.	a.	Illustrate the idea of Instruction pipelining with suitable examples.	08 Marks	2/1,2;3
	b.	Explain the following with respect to data hazards. i) Operand forwarding ii) Handling data hazards in software iii) Side effects.	09 Marks	3/2,3;2
	c.	Explain Instruction Hazards.	03 Marks	2/2,3;2

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UNIT-V

9.	a.	Describe the processor chips for Embedded application with block diagram	10 Marks	4/C;2
	b.	Briefly discuss parallel I/O ports with suitable diagrams.	10 Marks	4/C;3
10.	a.	With neat schematic diagram explain microwave over Embedded application.	10 Marks	4/C;3
	b.	Elaborate simplified block diagram of a digital camera.	10 Marks	4/C;3

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Fourth Semester B.E Degree Examination, MAKEUP JUNE 2018
Computer Science and Engineering
Computer Organization and Architecture (14CS45)

Max. Marks:100

Instructions: 1. Answer one full question from each unit.
2. Any missing Data can be suitably assumed.

UNIT-I

		Marks	CO/PO; BL
a.	Showing the different functional units of a computer mention the function of the processor register i) PC ii) MAR iii) IR	08 Marks	1/C;3
b.	With the help of a simple circuit explain how a common interrupt request line can be implemented	07 Marks	1/C;2
c.	Discuss exception with suitable examples.	05 Marks	1/C;2
a.	Discuss how the performance of a computer can be measured. What are the measures to improve the performance of a computer?	08 Marks	1/C;2
b.	With a neat diagram explain any two methods of handling multiple I/O devices.	08 Marks	1/C;2
c.	Briefly explain the pipelining and superscalar operation	04 Marks	1/C;3

UNIT-II

a.	Explain input transfer on a synchronous bus with timing diagram.	07 Marks	2/2,3;2
b.	Explain a general 8-bit parallel interface with the help of a block diagram.	06 Marks	2/2,3;2
c.	What is interleaving? With the help of proper diagrams explain how addressing of multiple module memory system is done.	07 Marks	2/2,3;2
a.	Explain how the impact of cache on the overall performance of a computer can be calculated.	08 Marks	2/2,3;2
b.	Elaborate the set- associative –mapped cache.	06 Marks	1/2,3;3
c.	Bring out Hit rate and miss penalty.	06 Marks	2/2,3;2

UNIT-III

a.	Discuss the virtual memory organization with suitable diagram.	08 Marks	2/2,3;
b.	Explain the design of Fast Adders. Explain how a 4-bit carry look ahead adder designed from fast adders	12 Marks	3/2,3;
a.	Discuss the bit-pair recording method of multiplication with an example.	08 Marks	2/2,3;3
b.	Explain the following i) IEEE Standard for floating point numbers ii) Guard bits & Truncation	12 Marks	3/2,3;2

UNIT-IV

a.	Write the difference between hard-wired and micro-programmed control.	07 Marks	3/C;2
b.	Describe 3-bus organization with suitable diagram	07 Marks	3/C;2
c.	Write the control sequence for execution of the instruction Add(R3),R1	06 Marks	3/C;2
a.	With suitable example illustrate the idea of instruction pipelining.	06 Marks	3/B;2
b.	Write the micro routine for instruction branch<0.	07 Marks	3/C;2
c.	Discuss single bus organization of data path inside a processor.	07 Marks	3/C;3

UNIT-V

a.	Describe processor chips for Embedded application with block diagram	12 Marks	2/2,3;2
b.	With a neat schematic diagram explain a simple micro controller	08 Marks	2/2,3;2
a.	Describe the following i) Polling approach ii) Interrupt approach	10 Marks	2/2,3;2
b.	Briefly explain the parallel I/O ports with suitable diagrams	10 Marks	2/2,3;2

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Supplementary **Semester B.E Degree Examination,** July/August 2018

Computer Science and Engineering

Computer Organization and Architecture (14CS45)

Max. Marks:100

Instructions: 1. Answer one full question from each unit.
2. Any missing Data can be suitably assumed.

			UNIT-I	Marks	CO/PO; BL
1.	a.		How single bus structure is used to interconnect functional units in computer system.	08 Marks	1/2,3;2
	b.		With a neat diagram explain any two methods of handling multiple I/O devices.	12 Marks	2/2,3;2
2.	a.		Showing different functional units of a computer, mention the function of		
		i)	PC	08 Marks	2/2,3;2
		ii)	MAR		
		iii)	IR		
	b.		Discuss all the available exceptions with suitable examples.	07 Marks	2/2,3;2
	c.		Explain the procedure to access I/O devices.	05 Marks	2/2,3;2
			UNIT-II		
3.	a.		Explain the Direct Memory Access. With the help of a neat diagram describe the distributed bus arbitration and centralized bus arbitration methods.	12 Marks	2/1,2;2
	b.		Describe the operation of input interface circuit	08 Marks	2/2,3;2
4.	a.		Discuss the memory hierarchy depending on speed, size, and cost.	08 Marks	2/1,2;2
	b.		Explain the associative mapping technique for cache memories	06 Marks	2/1,2;2
	c.		Demonstrate with the help of proper diagram how addressing of Multiple Module memory system is done.	06 Marks	3/1,2;3
			UNIT-III		
5.	a.		Describe virtual memory organization with suitable diagram	07 Marks	3/C;2
	b.		How do you design FAST ADDERS? Explain a 4-bit Carry look ahead adder	08 Marks	3/C;3
	c.		Give the binary Addition-Subtraction logic network	05 Marks	3/B;3
6.	a.		Discuss the Bit-pair recording method of multiplication with suitable example.	08 Marks	3/C;3
	b.		With the help of block diagram explain the virtual memory address translation.	07 Marks	3/B;2
	c.		Write a short note on IEEE Standard for floating point members.	05 Marks	3/C;2
			UNIT-IV		
7.	a.		With the help of a block diagram explain the basic organization of a micro programmed control unit.	10 Marks	2/1,2;3
	b.		Explain how the control unit is organized to allow conditional branching in the micro program.	10 Marks	2/2 ,3;2
8.	a.		Describe 3-bus organization with suitable diagram.	08 Marks	3/2,3;2
	b.		Write the differences between hard wired and microprogrammed control.	08 Marks	2/2,3;2
	c.		Write a note on instruction hazards	04 Marks	2/2,3;2
			UNIT-V		
9.	a.		Demonstrate with neat block diagram the processor chips for Embedded application	12 Marks	2/2,3;1
	b.		Explain the reaction timer circuit with a neat schematic diagram	08 Marks	2/2,3;1
10.	a.		Explain the digital camera and Home telemetry Embedded System	12 Marks	3/2,3;1
	b.		Discuss the Simple Microcontroller with a neat schematic diagram.	08 Marks	2/2,3;1

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IV SEMESTER B.E DEGREE EXAMINATION. MAY - JUNE 2010

Common to Computer Science & Information Science Engineering

COMPUTER ORGANIZATION & ARCHITECTURE (08CS/IS46)

Time: 3Hrs Max. Marks:100

Instruction: ***Answer one full question from each unit.***

UNIT-I

1. a. Explain any four addressing modes with examples for each. — 10 Marks
   b. Explain how the performance of the computer can be measured. — 05 Marks
   c. Explain the following (i) Big-endian assignment (ii) Little-endian assignment. — 05 Marks
2. a. Explain the basic functional units of a computer. Mention the functions of the processor registers (i) PC (ii) MAR — 10 Marks
   b. List the steps needed to execute the machine instruction ADD LOCA, R0 in terms of transfer between the components of processor and memory. Assume that the instruction itself is stored in the memory location INSTR. — 10 Marks

UNIT-II

3. a. Considering the timing diagrams, explain the sequence of events for input transfer & output transfer on a synchronous bus. — 10 Marks
   b. Describe the use of shift and rotate operations with examples. — 05 Marks
   c. Describe how four devices can be connected in daisy chain method to process their interrupt requests. — 05 Marks
4. a. What do you understand by stack frames? Discuss their use in sub-routines. — 10 Marks
   b. Write a note on Exceptions. — 05 Marks
   c. Three devices A,B & C are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A & B is not allowed. But interrupt requests from C may be accepted while either A or B is being serviced. Suggest different ways in which this can be accomplished in the following cases: (i) The computer has one interrupt request line. (ii) Two interrupt request lines INTRI & INTR2 are available with INTRI having higher priority. Specify when & how interrupts are enabled & disabled in each case. — 05 Marks

UNIT-III

5. a. What is cache? Explain any two cache mapping functions. — 10 Marks
   b. What are the features of SCSI bus? Write a note on arbitration & selection on SCSI bus. — 06 Marks
   c. Define hit ratio & miss penalty for cache access. — 04 Marks
6. a. Which types of I/O devices are interfered through DMA? Explain the bus – arbitration process used for DMA. — 10 Marks
   b. Explain the working of a dynamic memory cell. — 05 Marks
   c. A block set–associative cache consists of a total of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks each consisting of 128 words. (i) How many bits are there in main memory address? (ii) How many bits are there in each of the TAG, SET & WORD fields? — 05 Marks

UNIT-IV

7. a. Explain how an address generated by the processor gets translated into a main memory address. — 10 Marks
   b. Compare flash drives with hard disk drives. — 05 Marks
   c. Perform 56-78 using 1's complement & 2's complement methods. — 05 Marks
8. a. Explain the working principles of magnetic disks. — 10 Marks
   b. Represent the following pair of decimal numbers in the 2's complement form of size 8 bits. Add each pair & obtain the result along with the sign, carry & overflow flags that will be generated as a result of this addition. Comment if the result (8bits) is OK in each case. (i) 35 & -120 (ii) -35 & -120 — 10 Marks

UNIT-V

9. a. Using Booth algorithm multiply (-13) & (+107) — 10 Marks
   b. List out the advantages & limitations of a hardwired control unit. Explain the organization of a micro-programmed control unit. — 10 Marks
10. a. Illustrate with an example the algorithm for non-restoring binary division. — 10 Marks
    b. Draw timing diagram for a memory read operation. — 10 Marks

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