CSE1003 Digital Logic and Design
Module 4
Combinational Circuits II
L1

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Contents

6 hrs

Binary Parallel Adder - Look ahead carry

Magnitude Comparator

Decoders

Encoders

Multiplexers

Demultiplexers

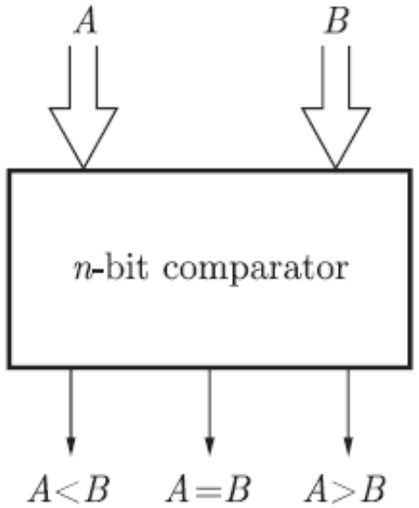
CO4: Analyze the operation of medium complexity standard combinational circuits like the encoder, decoder multiplexer, demultiplexer.

Applications – Magnitude Comparators

- Magnitude comparators are useful in control applications where a binary number representing the physical variable being controlled (e.g., position, speed, or temperature) is compared with a reference value. The comparator outputs are used to actuate circuitry to drive the physical variable toward the reference value.
- Comparators are used in central processing units (CPUs) and microcontrollers (MCUs).
- Comparators are also used as process controllers and for Servo motor control.
- Used in password verification and biometric applications.

Magnitude Comparator

- The comparator is a 2n-input, 3-output combinational logic circuit.
- It compares the magnitude of two n-bit numbers and provides the relative result as the output.



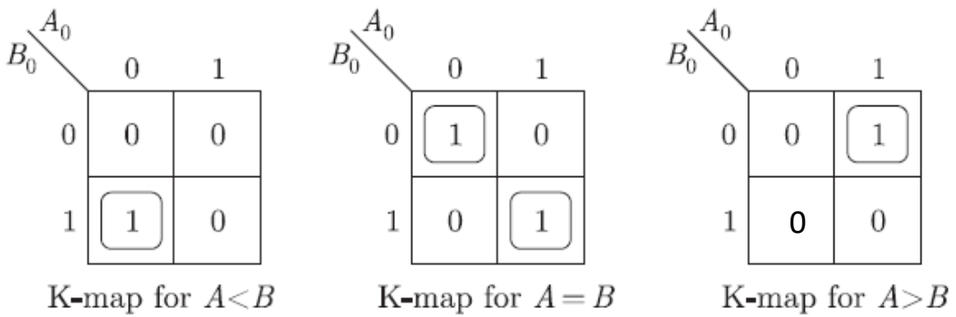
$$A = (A_{n-1}A_{n-2}\ldots A_0)_2$$
$$B = (B_{n-1}B_{n-2}\ldots B_0)_2$$

$$f_1 = 1, \quad \text{if } A < B$$
$$f_2 = 1, \quad \text{if } A = B$$
$$f_3 = 1, \quad \text{if } A > B$$

1-bit Magnitude Comparator

- The one-bit comparator is a combinational logic circuit with two inputs A and B and three outputs namely A < B, A= B and A > B.
- It compares the two single bit numbers A and B and produces an output that indicates the result of the comparison.
- Let the 1-bit numbers be A =A_0 and B =B_0.

Design of 1-bit Magnitude Comparator



Truth table of a one-bit comparator

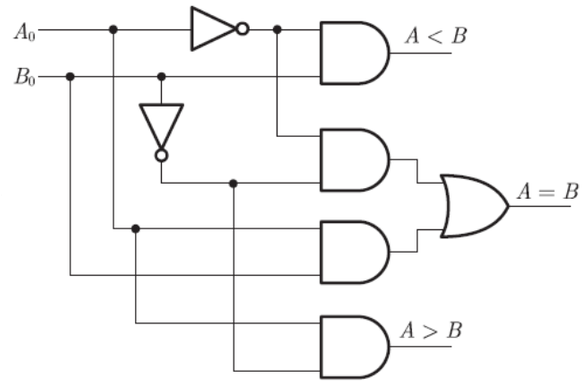
Inputs		Outputs		
A	B	$X(A<B)$	$Y(A=B)$	$Z(A>B)$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

For $(A<B)$, $X = \overline{A_0}B_0$

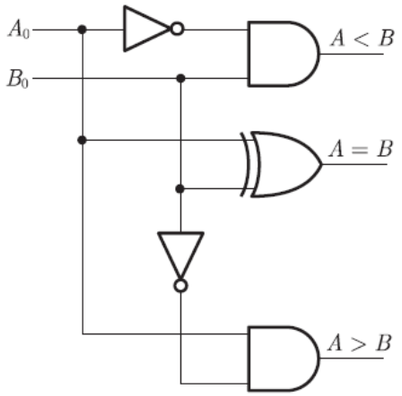
For $(A=B)$, $Y = \overline{A_0}\,\overline{B_0} + A_0B_0 = \overline{A_0 \oplus B_0}$

For $(A>B)$, $Z = A_0\overline{B_0}$

Logic diagram of 1-bit comparator



Using Basic Gates



Using AND and EX-NOR gates

Design of 2-bit Magnitude Comparator

- A comparator used to compare two binary numbers each of two bits is called a 2-bit magnitude comparator.
- It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers.
- Let the two 2-bit binary numbers be $A = A_1A_0$ and $B = B_1B_0$.
- Here each subscript represents one of the digits in the numbers.
- The binary numbers A and B will be equal if all the pairs of significant digits of both numbers are equal, i.e., $A_1 = B_1$ and $A_0 = B_0$.

Truth Table of 2-bit Magnitude Comparator

INPUT				OUTPUT		
A1	A0	B1	B0	A < B	A = B	A > B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Procedure to compare 2 2bit binary numbers:

1. First compare the two most significant bits (A_1 and B_1).

   If $A_1 > B_1$, then A >B;

   if $A_1 < B_1$, then A< B.

   If $A_1 = B_1$, then the next pair of bits (A_0 and B_0) must be compared.

2. If $A_1 = B_1$ and $A_0 > B_0$, then A> B;

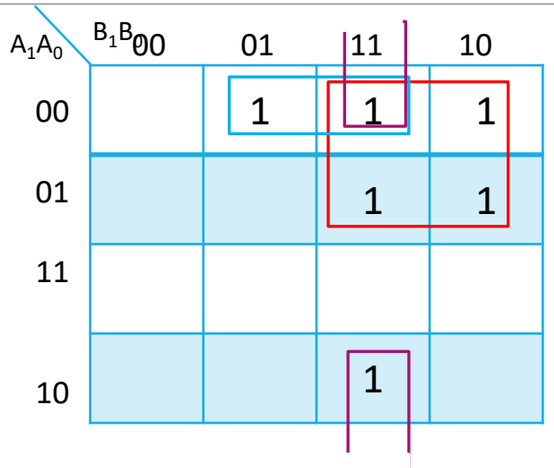
   if $A_1 = B_1$ and $A_0 < B_0$, then A< B.

   Again, if $A_1 = B_1$ and $A_0 = B_0$, then A=B.

Design of 2-bit Magnitude Comparator

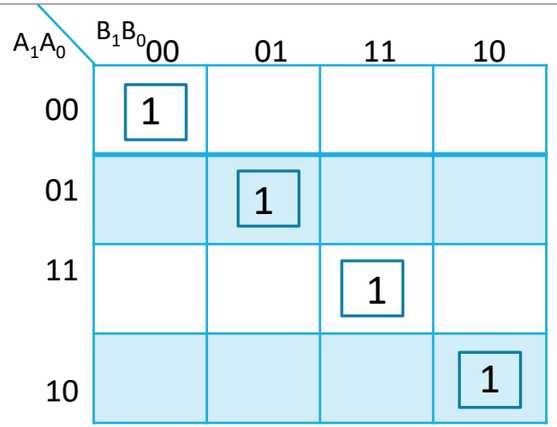
Truth Table of 2-bit Magnitude Comparator

INPUT				OUTPUT		
A1	A0	B1	B0	A < B	A = B	A > B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

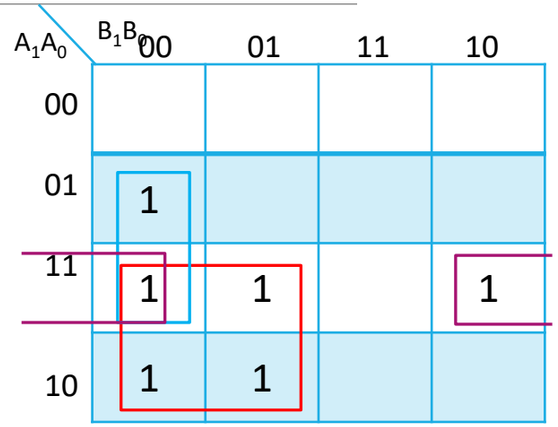


For A<B

$$X = \overline{A_1}B_1 + \overline{A_1}B_0\overline{A_0} + \overline{A_0}\,B_1B_0$$



For A=B



For A>B

$$Z = A_0\overline{B_1}\,\overline{B_0} + A_1A_0\overline{B_0} + A_1\overline{B_1}$$

$$\begin{aligned} Y &= \overline{A_1}\,\overline{B_1}\,\overline{A_0}\,\overline{B_0} + \overline{A_1}A_0\overline{B_1}B_0 + A_1A_0B_1B_0 + A_1\overline{A_0}B_1\overline{B_0} \\ &= \overline{A_1}\,\overline{B_1}(\overline{A_0}\,\overline{B_0} + A_0B_0) + A_1B_1(A_0B_0 + \overline{A_0}\,\overline{B_0}) \\ &= \overline{A_1}\,\overline{B_1}(A_0 \odot B_0) + A_1B_1(A_0 \odot B_0) \\ &= (A_0 \odot B_0)(\overline{A_1}\,\overline{B_1} + A_1B_1) \\ &= (A_0 \odot B_0)(A_1 \odot B_1) \end{aligned}$$

Design of 2-bit Magnitude Comparator

For A<B

$$X = \overline{A_1}B_1 + \overline{A_1}B_0\overline{A_0} + \overline{A_0}\,B_1B_0$$

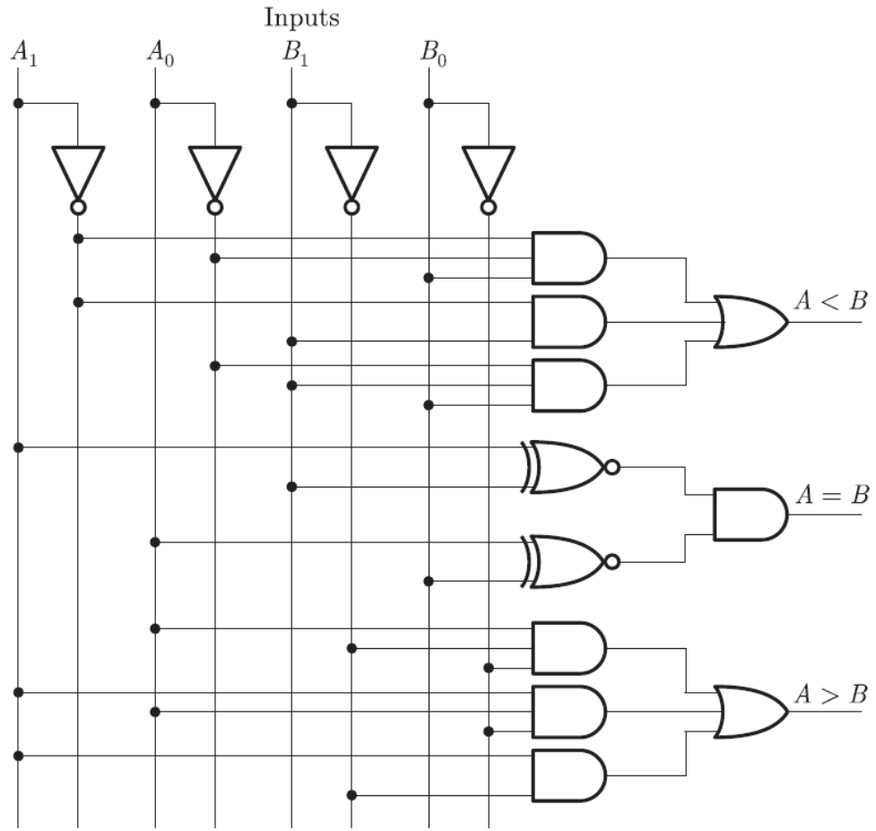
For A=B

$$\begin{aligned} Y &= \overline{A}_1\overline{B}_1\overline{A}_0\overline{B}_0 + \overline{A}_1A_0\overline{B}_1B_0 + A_1A_0B_1B_0 + A_1\overline{A}_0B_1\overline{B}_0 \\ &= \overline{A}_1\overline{B}_1(\overline{A}_0\overline{B}_0 + A_0B_0) + A_1B_1(A_0B_0 + \overline{A}_0\overline{B}_0) \\ &= \overline{A}_1\overline{B}_1(A_0 \odot B_0) + A_1B_1(A_0 \odot B_0) \\ &= (A_0 \odot B_0)(\overline{A}_1\overline{B}_1 + A_1B_1) \\ &= (A_0 \odot B_0)(A_1 \odot B_1) \end{aligned}$$

For A>B

$$Z = A_0\overline{B}_1\overline{B}_0 + A_1A_0\overline{B}_0 + A_1\overline{B}_1$$

Logic diagram of 2-bit Magnitude Comparator



Design of 4-bit Magnitude Comparator

- Let the two 4-bit numbers be $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$
- **Steps used in comparing two 4-bit numbers:**

1. First compare the two most significant bits (A_3 and B_3).

   If $A_3 > B_3$, then $A > B$; if $A_3 < B_3$, then $A < B$.

   If $A_3 = B_3$, the next pair of bits ($A2$ and $B2$) must be compared.

2. If $A_3 = B_3$ and $A_2 > B_2$, then $A > B$;

   if $A_3 = B_3$ and $A_2 < B_2$, then $A < B$

   if $A_3 = B_3$ and $A_2 = B_2$, the next pair of bits (A_1 and B_1) will be compared.

3. If $A_3 = B_3$, $A_2 = B_2$ and $A_1 > B_1$; then $A > B$;

   if $A_3 = B_3$, $A_2 = B_2$ and $A_1 < B_1$, then $A < B$.

   if $A_3 = B_3$, $A_2 = B_2$ and $A_1 = B_1$, compare the LSBs (A_0 and B_0).

4. If $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$ and $A_0 > B_0$, then $A > B$;

   if $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$ and $A_0 < B_0$, then $A < B$.

5. If $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$, $A_0 = B_0$, then $A = B$.

Design of 4-bit Magnitude Comparator

A3B3	A2B2	A1B1	A0B0	A>B	A<B	A=B
A3>B3	x	x	x	1	0	0
A3<B3	x	x	x	0	1	0
A3=B3	A2>B2	x	x	1	0	0
A3=B3	A2<B2	x	x	0	1	0
A3=B3	A2=B2	A1>B1	x	1	0	0
A3=B3	A2=B2	A1<B1	x	0	1	0
A3=B3	A2=B2	A1=B1	A0>B0	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1

The output A > B logic expression can be written as

$$G = A3\,\overline{B3} + (A3 \text{ Ex-NOR } B3)\,A2\,\overline{B2} + (A3 \text{ Ex-NOR } B3)\,(A2 \text{ Ex-NOR } B2)\,A1\,\overline{B1} + (A3 \text{ Ex-NOR } B3)\,(A2 \text{ Ex-NOR } B2)\,(A1 \text{ Ex-NOR } B1)\,A0\,\overline{B0}$$

The logical expression for A<B output can be written as

$$L = \overline{A3}\,B3 + (A3 \text{ Ex-NOR } B3)\,\overline{A2}\,B2 + (A3 \text{ Ex-NOR } B3)\,(A2 \text{ Ex-NOR } B2)\,\overline{A1}\,B1 + (A3 \text{ Ex-NOR } B3)\,(A2 \text{ Ex-NOR } B2)\,(A1 \text{ Ex-NOR } B1)\,\overline{A0}\,B0$$

The logical expression for A=B output can be written as

$$E = (A3 \text{ Ex-NOR } B3)\,(A2 \text{ Ex-NOR } B2)\,(A1 \text{ Ex-NOR } B1)\,(A0 \text{ Ex-NOR } B0)$$

Design of 4-bit Magnitude Comparator

The output A > B logic expression can be written as

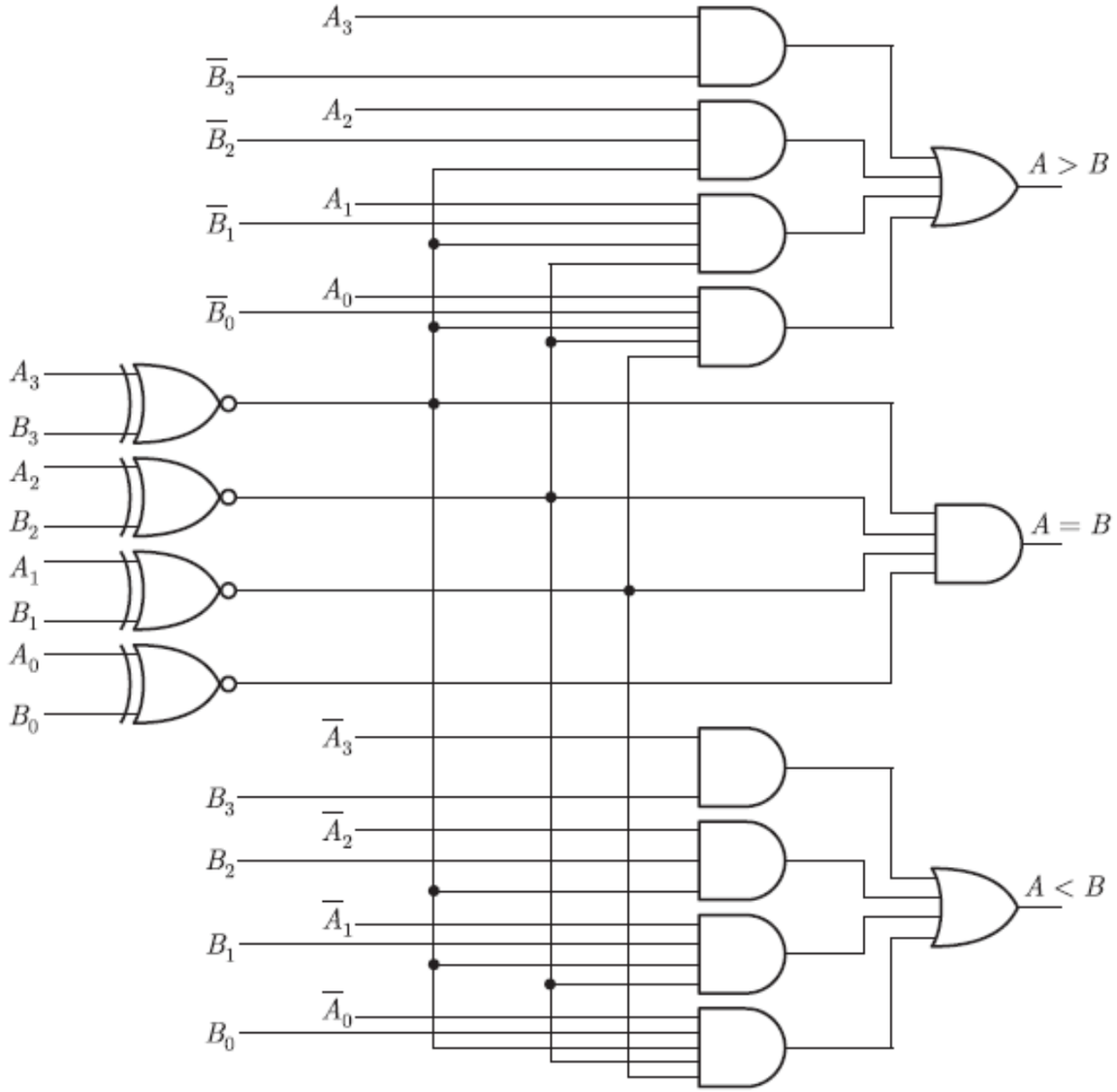
G = A3 $\overline{B3}$ + (A3 Ex-NOR B3) A2 $\overline{B2}$ + (A3 Ex-NOR B3) (A2 Ex-NOR B2) A1 $\overline{B1}$ + (A3 Ex-NOR B3) (A2 Ex-NOR B2) (A1 Ex-NOR B1) A0 $\overline{B0}$

The logical expression for A<B output can be written as

L = $\overline{A3}$ B3 + (A3 Ex-NOR B3) $\overline{A2}$ B2 + (A3 Ex-NOR B3) (A2 Ex-NOR B2) $\overline{A1}$ B1 + (A3 Ex-NOR B3) (A2 Ex-NOR B2) (A1 Ex-NOR B1) $\overline{A0}$ B0

The logical expression for A=B output can be written as

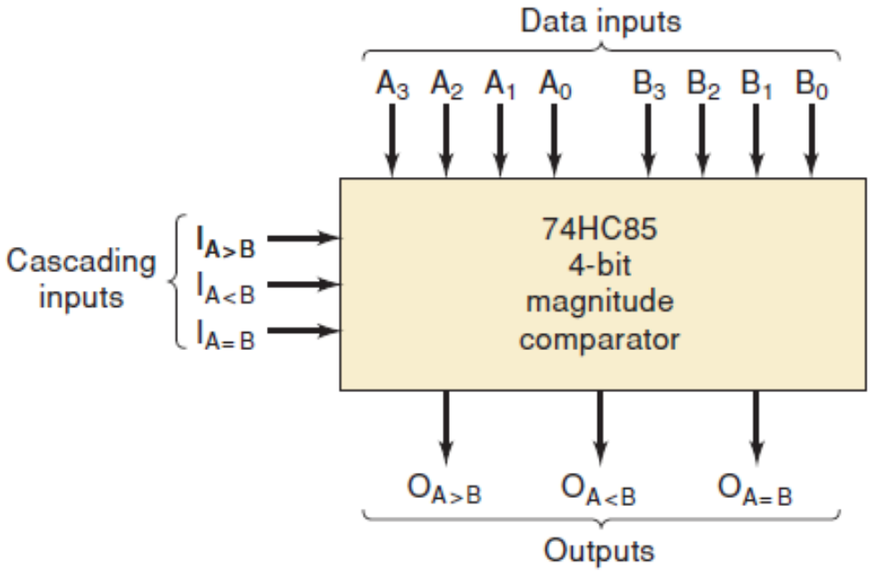
E = (A3 Ex-NOR B3) (A2 Ex-NOR B2) (A1 Ex-NOR B1) (A0 Ex-NOR B0)



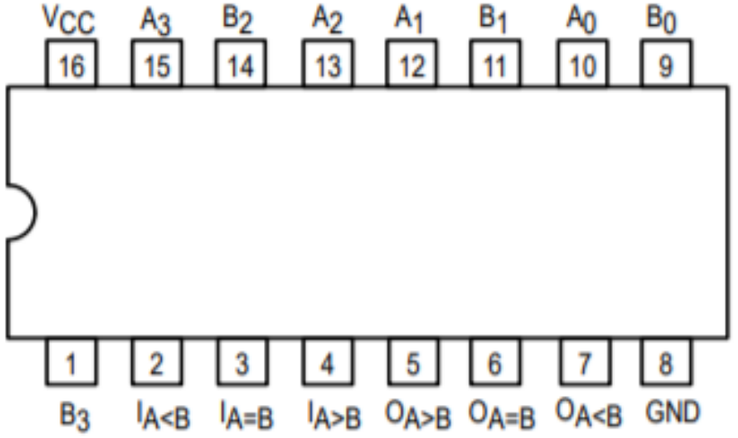
Logic diagram of 4-bit Comparator

MAGNITUDE COMPARATOR

- Magnitude Comparators are available in IC form.
- 7485 is a 4-bit magnitude comparator of the TTL logic family.



Logic Symbol



Pin Configuration

Data Inputs

$$A = (A_3, A_2, A_1, A_0)_2$$
$$B = (B_3, B_2, B_1, B_0)_2$$

Cascade Inputs

$$C1 \rightarrow A < B$$
$$C2 \rightarrow A = B$$
$$C3 \rightarrow A > B$$

Outputs

$$O_{A<B}$$
$$O_{A>B}$$
$$O_{A=B}$$

Cascading inputs provide a means for expanding the comparison operation to more than four bits by cascading two or more four-bit comparators.

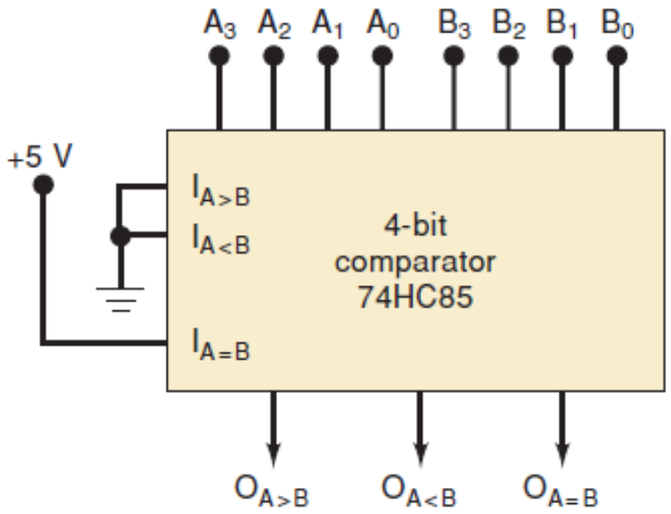
MAGNITUDE COMPARATOR

TRUTH TABLE

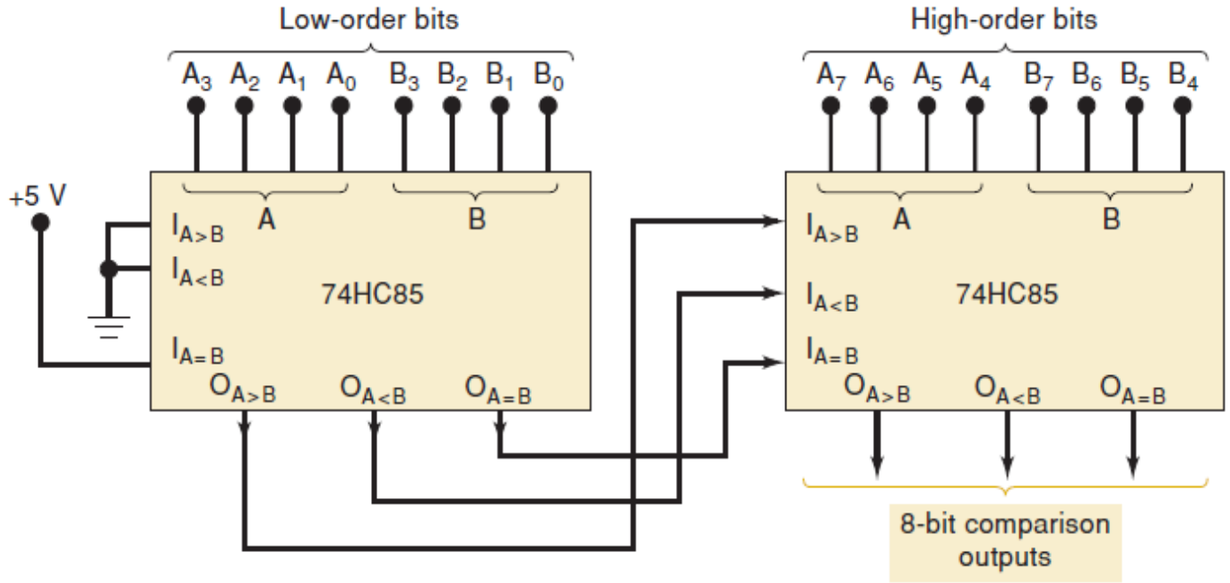
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

MAGNITUDE COMPARATOR



(a) 74HC85 wired as a four-bit comparator



(b) Two 74HC85s cascaded to perform an eight-bit comparison

MAGNITUDE COMPARATOR

Describe the operation of the eight-bit comparison arrangement in Figure for the following cases:

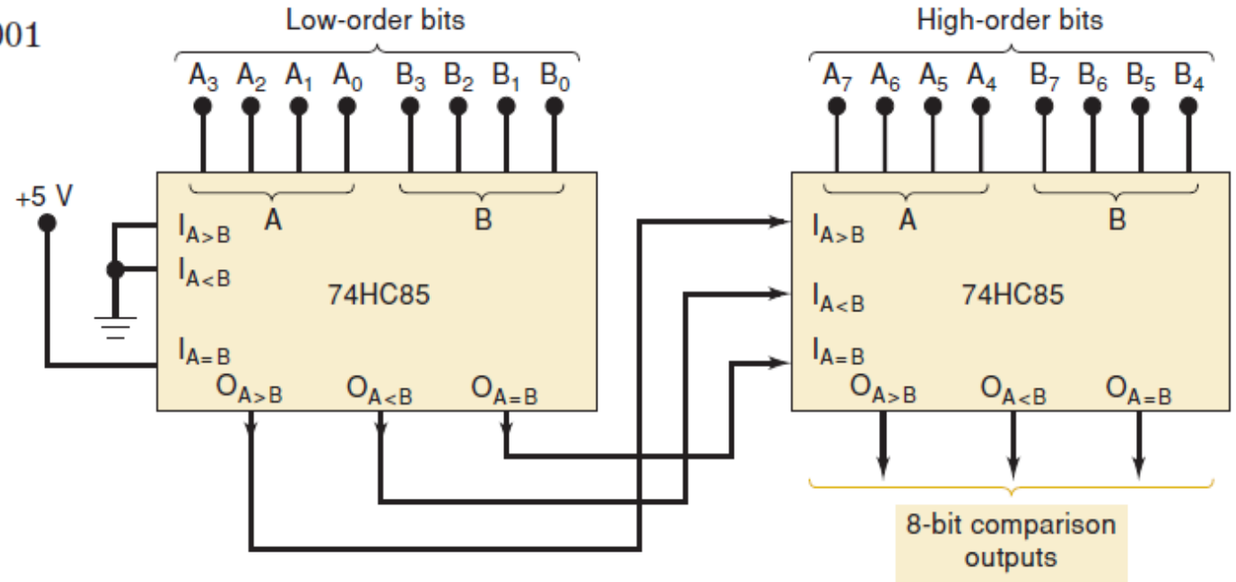
(a) $A_7A_6A_5A_4A_3A_2A_1A_0 = 10101111; B_7B_6B_5B_4B_3B_2B_1B_0 = 10110001$

(b) $A_7A_6A_5A_4A_3A_2A_1A_0 = 10101111; B_7B_6B_5B_4B_3B_2B_1B_0 = 10101001$

Solution:

$a)$ $O_{A<B}$=1

$b)$ $O_{A>B}$=1



Design a 5- bit comparator using a single 7485 and one gate.

The two 5-bit numbers to be compared are

$X_4\,X_3\,X_2\,X_1\,X_0$ and $Y_4\,Y_3\,Y_2\,Y_1\,Y_0$