VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test – I

Programme Name & Branch:B.Tech & CSE **Slot: G1+TG1**
Course Code: CSE 2001 **Exam Duration: 90 mins**
Course Title: Computer Architecture and Organization **Maximum Marks: 50**

General instruction(s): Answer All Question (5 * 10 = 50)

1. Consider two different machines, with two different instruction sets, both of which have a clock rate of 40 MHz processor.

Instruction Type	Instruction Count	Cycles per Instruction
Machine A		
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2
Machine B		
Integer arithmetic	48000	1
Data transfer	45000	2
Floating point	15000	4
Control transfer	8000	3

(a) Determine the effective CPI, MIPS rate, and execution time for this program.
(b) Comment on the results.

Solution
(a)
Machine A:
CPI_A=1.55, $MIPS_A$=25.8, Execution Time=CPU_A=3.87ms
Machine B:
CPI_B=1.91, $MIPS_B$=20.94, Execution Time=CPU_B=5.5ms
(b) Machine A has higher MIPS rate and it requires higher execution time.
Machine B has lower MIPS rate and it requires lesser execution time.

2. Illustrate expanded structure of IAS computer with neat diagram and also provide description for the following symbolic representations (i) LOAD M(X), (ii) SUB M(X), (iii) JUMP M(X,0:19), (iv) JUMP + M(X,20:39).

Expanded Structure of IAS Computer

1. Memory buffer register (MBR):-

Contains a word to be stored in memory or sent to the I/O unit, it is used to receive a word from memory or from the I/O unit.

2. Memory address Register (MAR):-

Specifies the address of memory in the word to be written from or read into the MBR.

3. Instruction register (IR):- Contains the 8bit Op-code instruction being executed.

4. Instruction buffer register (IBR):-

Employed to hold temporarily the right-hand instruction from a word in memory.

5. Program counter (PC):-

Contains the address of the next instruction-pair to be fetched from memory.

6. <u>Accumulator(AC) and multiplier quotient(MQ):-</u>

Employed to hold temporarily operands and results of ALU operations. For example, the result of multiplying two 40-bits numbers is an 80bit number, the most significant 40 bits are stored in the AC and the least significant in the MQ.

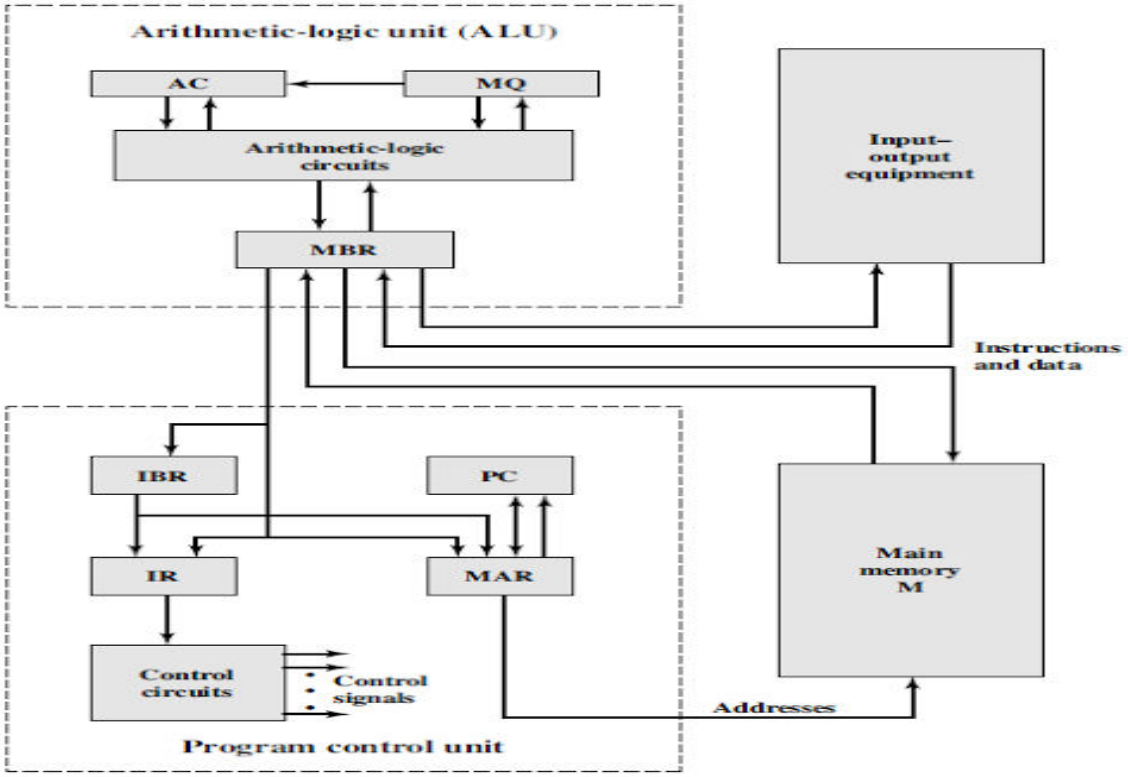


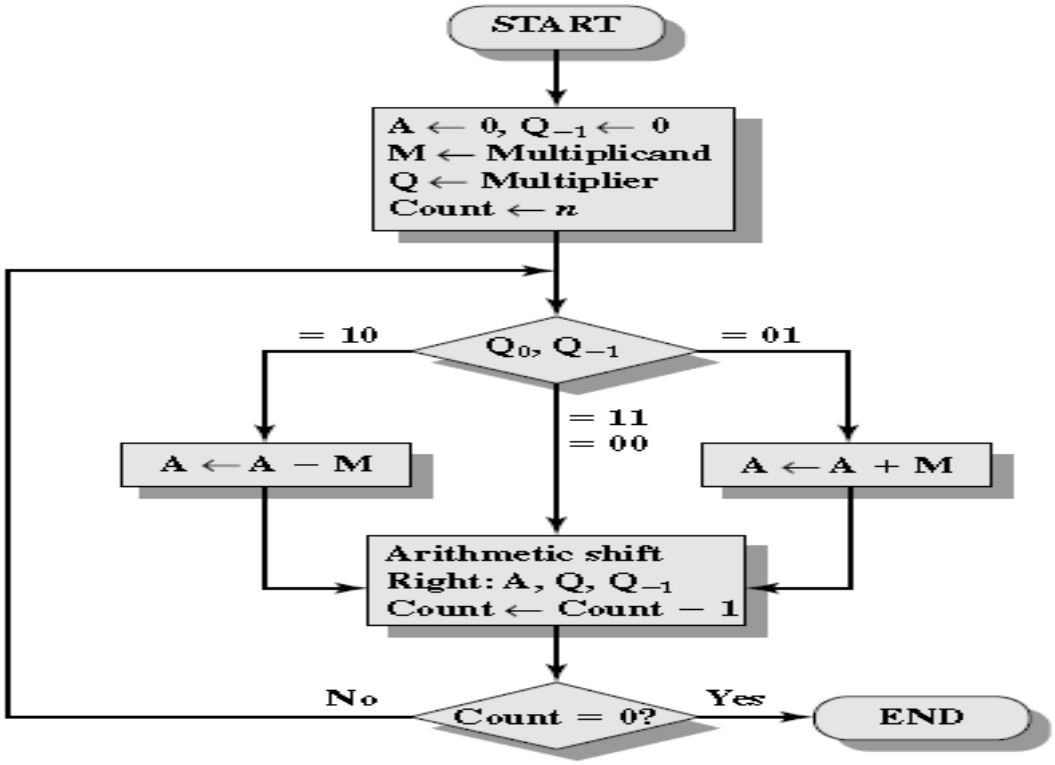
Figure : Expanded Structure of IAS Computer

(i) LOAD M(X) - Transfer M(X) to the accumulator
(ii) SUB M(X) - Subtract M(X) from AC; put the result in AC
(iii) JUMP M(X,0:19) -If number in the accumulator is nonnegative, take next instruction from left half of M(X)
(iv) JUMP + M(X,20:39)- If number in the accumulator is nonnegative, take next instruction from right half of M(X)

3. Consider the multiplier x=0111 and multiplicand y=1011 in two's complement notation, compute the product of p=x*y with Booth's algorithm and describe it with flow chart representation.

Ans:
x = 0111=7
y=1011= -5
Ans: -35
Product = 11011101

00100010 = 1s Complement
+ 1
00100011 = 35



4. Write a program to evaluate the arithmetic statement:

$$X = (A + B) * (T + Q)$$

a. Using a general register computer with three address instructions.
b. Using a general register computer with two address instructions.
c. Using an accumulator type computer with one address instructions.
d. Using a stack organized computer with Zero-address operation instructions.

a. **Three-Address Instructions**

ADD R1, A, B	R1 ← M [A] + M [B]
ADD R2, T, Q	R2 ← M [T] + M [Q]
MUL X, R1, R2	M [X] ← R1 * R2

b. **Two-Address Instructions**

MOV R1, A	R1 ← M [A]
ADD R1, B	R1 ← R1 + M [B]
MOV R2, T	R2 ← M [T]
ADD R2, Q	R2 ← R2 + M [Q]
MUL R1, R2	R1 ← R1*R2
MOV X, R1	M [X] ← R1

c. one address instructions

LOAD A	AC ← M [A]
ADD B	AC ← AC + M [B]
STORE G	M [G] ← AC
LOAD T	AC ← M [T]
ADD Q	AC ← AC + M [Q]
MUL G	AC ← AC * M [G]
STORE X	M [X] ← AC

d. Zero Address Instruction

PUSH A	TOS ← A
PUSH B	TOS ← B
ADD	TOS ← (A + B)
PUSH T	TOS ← T

PUSH	Q	TOS ← Q
ADD		TOS ← (T + Q)
MUL		TOS ← (T + Q) ∗ (A + B)
POP	X	M [X] ← TOS

5. The two-word instruction at address 300 and 301 is load to Accumulator with address field equal to 400. Program Counter has the value 300 for fetching the instruction. The content of processor register is 500 and the content of index register is 202. The memory content at each of these addresses as shown in Table.

Address	**Memory**	**Address**	**Memory**
300	Load to AC	500	700
301	400	600	250
302	Next Instruction	601	390
400	600	602	900
499	450	700	825

Compute the effective address and operand for the following addressing modes:
Direct address, Indirect address, Index address, Relative address, Autoincrement and Autodecrement.

	Effective Address	Operand
Direct address	400	600
Indirect address	600	250
Index address	602	900
Relative address	702	
Autoincrement	500	700
Autodecrement	499	450