Assignment No.-4

R (2)	C (4)	O (2)	T (2)	Dated Sign

- ***Title:*** **Realization of Boolean expression using 8:1 Multiplexer 74151**
- ***Objective:*** To learn different techniques of designing multiplexer
- ***Problem Statement:***
  1. Verification of Functional table.
  2. Verification of Sum of Product (SOP) and Product of Sum (POS) with the help of given Boolean expression.
  3. Verify the functional table using cascading of two multiplexers
  4. Realization of Boolean expression using hardware reduction method for the given equation.
- ***Hardware & software requirements:***

  Digital trainer board, IC 74151, IC 7404, IC 7432, patch cords, + 5V Power supply

Theory:

1 .What is multiplexer?

- Multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line. Basic multiplexer has several data inputs and a single output line.
- The selection of a particular input line is controlled by a set of selection line.
- There are 2^n input lines & n is the number of selection line whose bit combinations determines which input is selected .It is "Many into One".
- *Strobe*: - It is used to enable/ disable the logic circuit ***OR*** 'E' is called as enable I/P which is generally active LOW. It is used for cascading
- MUX is a *single pole* multiple way switch.

2. Necessity of multiplexer

- In most of the electronic systems, digital data is available on more than one lines. It is necessary to route this data over a single line.
- It select one of the many I/P at a time.
- Multiplexer improves the *reliability* of digital system because it reduces the number of external wire connection.

3. **Enlist significance and advantages of Multiplexer**

- It doesn't need K-map & logic simplification.
- The IC package count is minimized.
- It simplifies the logic design.
- In designing the combinational circuit
- It reduces the complexity & cost.
- To minimize number of connections in communication system were we need to handle thousands of connections. Ex. Telephone exchange.

4.Applications of MUX

- Data selector to select one out of many data I/P.
- In Data Acquisition system.
- In the D/A converter.

Multiplexer Tree

- It is nothing but construction of more number of line using less number of lines.
- It is possible to expand the range of inputs for multiplexers beyond the available Range in the integrated circuits. This can be accomplished by interconnecting several multiplexers.

8:1 MUX:

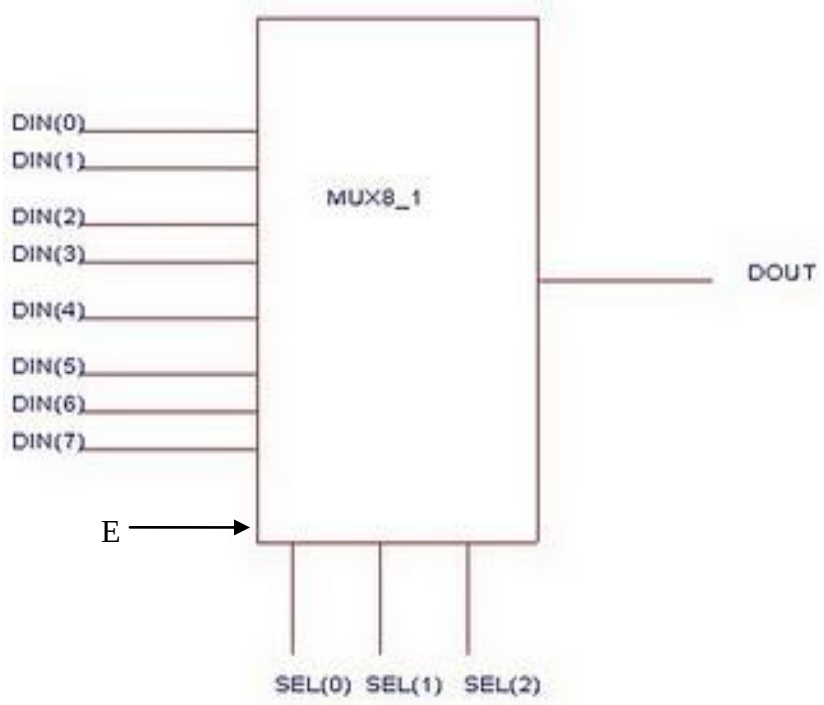
The block diagram of 8:1 MUX & its TT is shown. It has eight data

I/P & one enable input, three select lines and one O/P.

Operating principle:

When the Strobe or Enable input is active low, we can select any one of eight data I/P and connect to O/P.

Design:



Draw the connection diagram of multiplexer to verify the functional table.

SELECTION LINES			STROBE	OUTPUTS	
C	B	A	E	Y	$\overline{Y}$
X	X	X	1	0	1
0	0	0	0	D0	D0
0	0	1	0	D1	D1
0	1	0	0	D2	D2
0	1	1	0	D3	D3
1	0	0	0	D4	D4
1	0	1	0	D5	D5
1	1	0	0	D6	D6
1	1	1	0	D7	D7

X = don't care condition.

Part 1: MUX as a function generator.

Convert the given Boolean expression into standard SOP / POS format if required and complete the logic diagram design accordingly for realization of the same.

i) **As an example:**
Function = Sum of Product (SOP)
Y = ∑m (1, 2, 3, 4, 5, 6, 7)

SELECTION LINES			STROBE	OUTPUTS	
C	B	A		Y	$\overline{Y}$
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	1	0

SOP realization Diagram

SOP Y = ∑m (1, 2, 3, 4, 5, 6, 7)

Solution:-Since there are 3 variable, the multiplexer have 3 select I/P should be used.

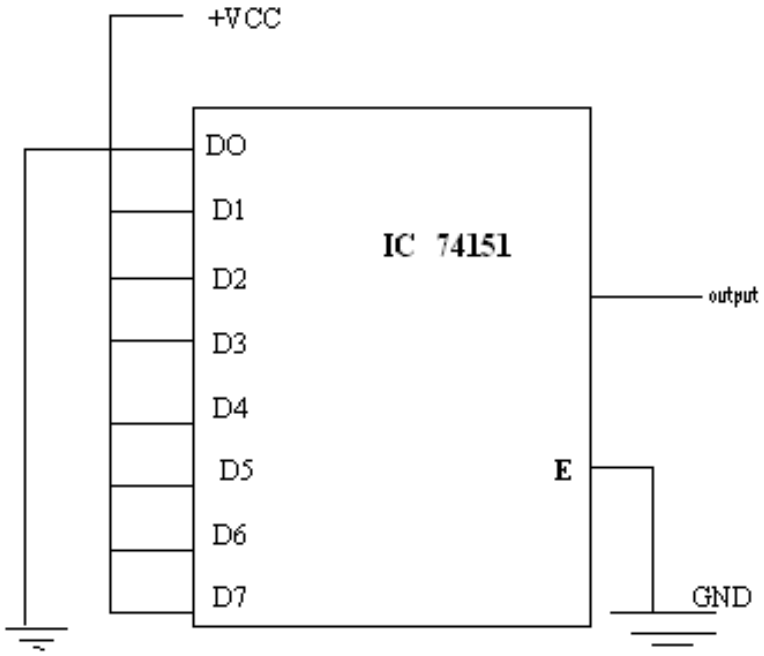
Hence one 8:1 mux should be used.

Ste p 1:-Identify the number decimal corresponding to each minterm.

Here 1,2,3,4,5,6,7

Step 2:-Connect the data input lines 1,2,3,4,5,6,7 to logic 1(+Vcc) & remaining input line 0 to logic 0(GND)

Step 3:-Connect variables A, B & C to select input.



ii) **As an example**

Function = Product of Sum (POS)

Y = ∏ M (0, 5, 6, 7)

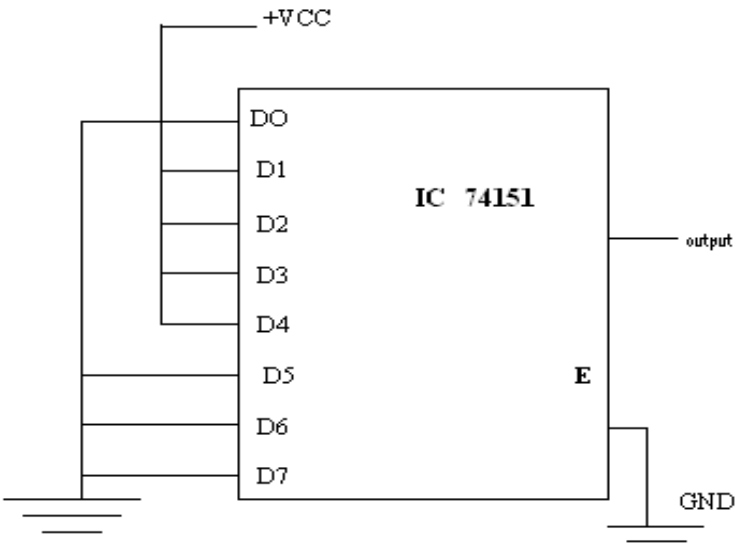
SELECTION LINES			STROBE	OUTPUTS	
C	B	A		Y	$\overline{Y}$
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	0	1

POS realization exp:

1. As there are 3 i/p so use 8:1 MUX
2. Connect the given min terms to GND and else decimal numbers to logic1(+VCC).

POS realization Diagram

POS Y = ∏ M (0, 5, 6, 7)



Part -2: Implementation of 16:1 MUX using 8:1 MUX

Use hardware reduction method and implement the given Boolean expression with the help of neat logic diagram. ***(N-circle Method)***

First Method: F(A,B,C,D) = ∑m (2, 4, 5, 7, 10, 14)

	D0	D1	D2	D3	D4	D5	D6	D7
$\overline{A}$	0	1	**2**	3	**4**	**5**	6	**7**
A	8	9	**10**	11	12	13	**14**	15
Input to Mux	0	0	1	0	$\overline{A}$	$\overline{A}$	A	$\overline{A}$

i. *Bold and red marks represent the minterms
ii. Consider B,C,D as a select line
iii. Use NOT gate to obtain A and complement of it.

Solution:-

Step 1:- Apply B, C, D to select I/P & design table(Implementation table).

Step 2: Encircle those min terms which are present in output.

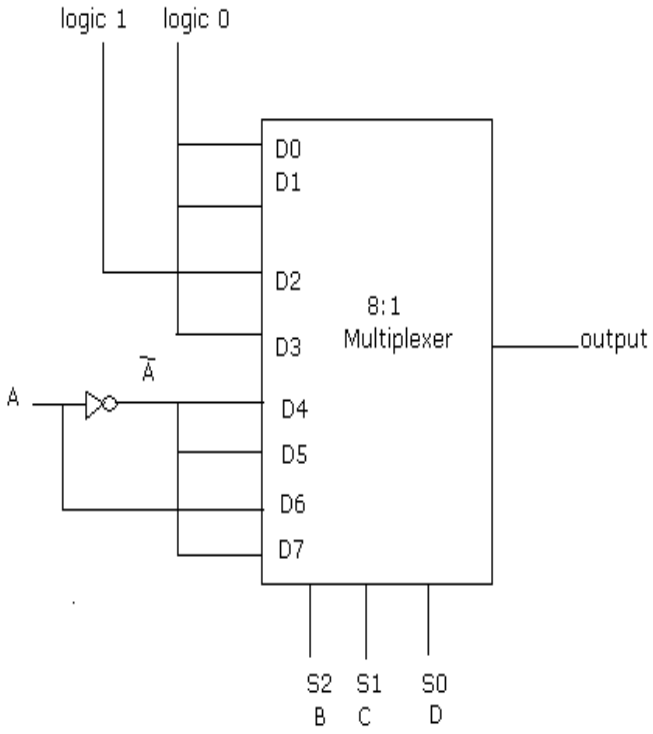
Step 3: If the min terms in a column are not circled then apply logic 0.

Step 4: If the min terms in a column are circled then apply logic 1.

Step 5: If only min term in 2nd row is encircled then 'A' should be applied to that data input. Hence apply 'A' to D6.

Step 6: If only min term in 1st row is encircled then ' $\overline{A}$ ' should be applied to that data input. Hence apply ' $\overline{A}$ ' to D4, D5, D7.

16:1 MUX using 8:1 MUX Diagram

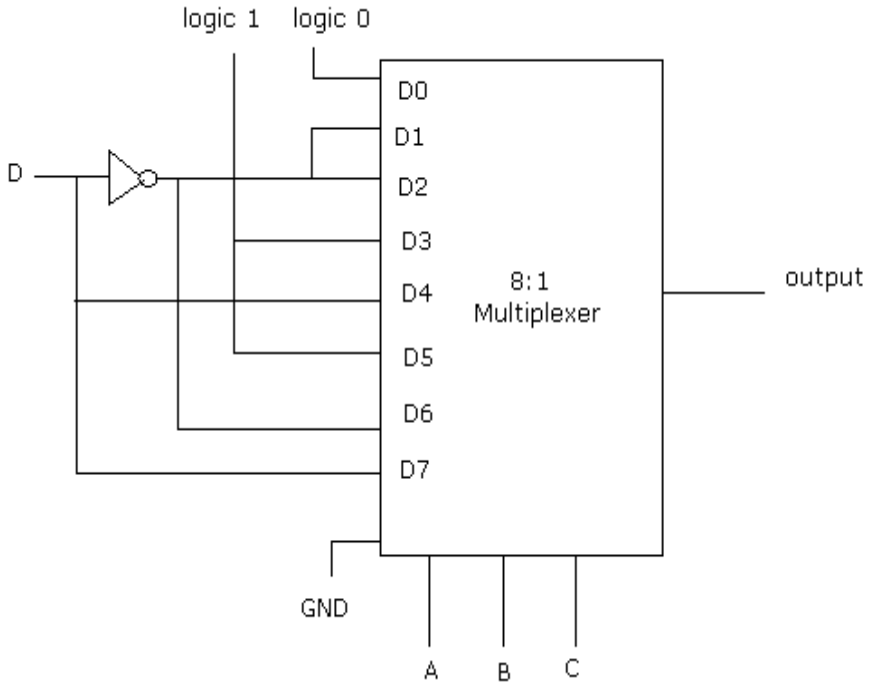


<u>Second method:</u> F (A, B, C, D) = ∑m (2, 4, 6, 7, 9, 10, 11, 12, 15)

1. Make a combination of pair according to same Values of A, B and C
2. Check the output values with respect to value of D.

A	B	C	D	output	output
0	0	0	0	0	0
0	0	0	1	0	
0	0	1	0	1	-
0	0	1	1	0	D
0	1	0	0	1	-
0	1	0	1	0	D
0	1	1	0	1	1
0	1	1	1	1	
1	0	0	0	0	D
1	0	0	1	1	
1	0	1	0	1	1
1	0	1	1	1	
1	1	0	0	1	-
1	1	0	1	0	D
1	1	1	0	0	D
1	1	1	1	1	

16:1 MUX using 8:1 MUX Diagram: Second Method



Part-3 **Implementation of 16:1 MUX using two 8:1 MUX (Cascading Method)**

F(A,B,C,D)= ∑m(2, 4, 5, 7, 10, 14)

Solution:-

Step 1: Connect S2, S1, S0 select lines of two 8:1 MUX parallel where as MSB select input is used for enabling MUX.

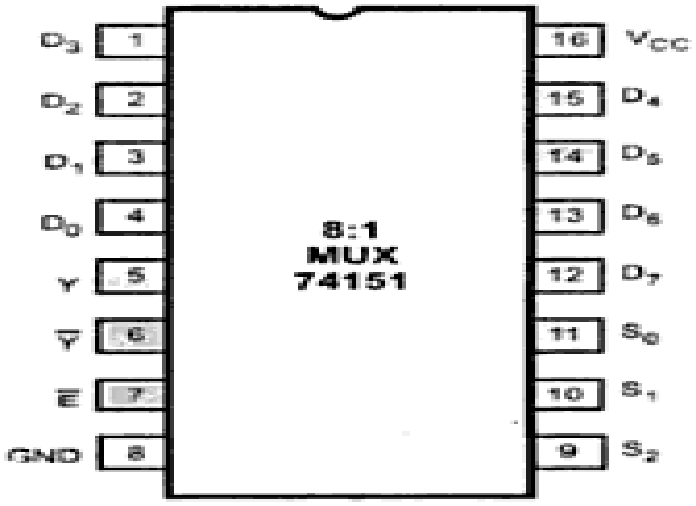
Step 2: S3 is connected directly to the enable (E) to mux-2 where as $\overline{S3}$ is connect to enable input of mux-1

Step 3: The output of two MUX are OR to get final output.

Truth table: - PART_3

Select line				Output		Final Output
S3	S2	S1	S0	Y1	Y2	Y
0	0	0	0	D0	--	D0
0	0	0	1	D1	--	D1
0	0	1	0	D2	--	D2
0	0	1	1	D3	--	D3
0	1	0	0	D4	--	D4
0	1	0	1	D5	--	D5
0	1	1	0	D6	--	D6
1	1	1	1	D7	--	D7
1	0	0	0	--	D8	D8
1	0	0	1	--	D9	D9
1	0	1	0	--	D10	D10
1	0	1	1	--	D11	D11
1	1	0	0	--	D12	D12
1	1	0	1	--	D13	D13
1	1	1	0	--	D14	D14
1	1	1	1	--	D15	D15

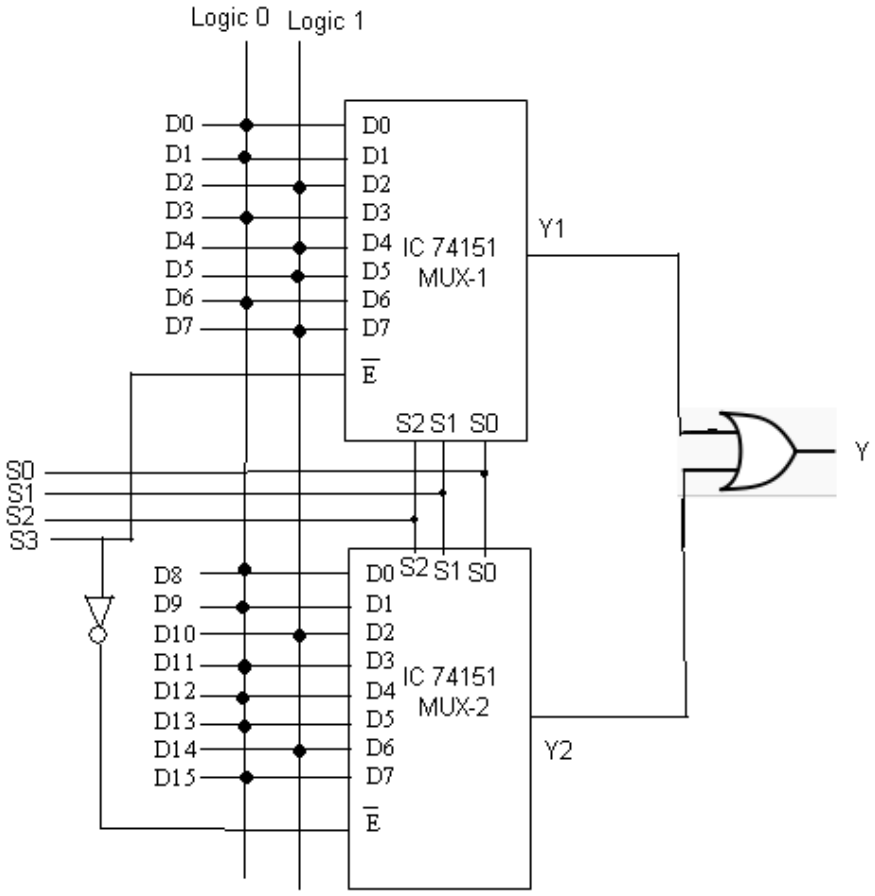
Truth Table for 16:1 MUX using two 8:1 MUX



Pin Diagram IC 74151

8:1 mux

Multiplexer Tree according to given equation:-



Outcome:

Multiplexer is used as a data selector to select one out of many data inputs.

It is used for simplification of logic design.

It is used to design combinational circuit.

Use of multiplexer minimizes no. of connections.

FAQ:

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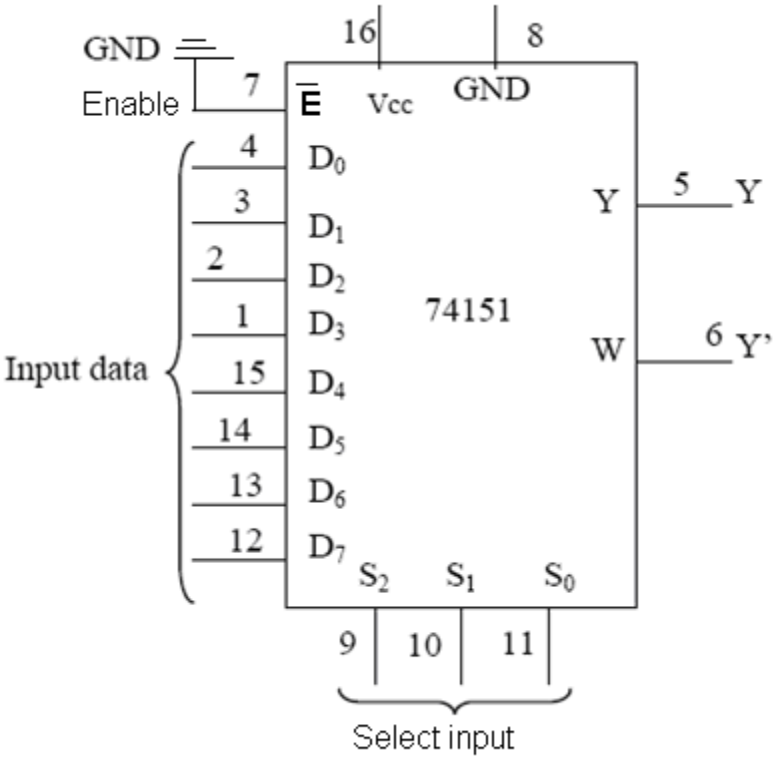
1. ***Enlist applications of MUX***

➔1. MUX is used as data selector.

2. It is used to design combinational circuit.

3. Less number of wires required which reduces complexity
4. There is no need to design k-map
5. We design equation using truth table.



2. Define the terms Encoder and Decoder

➔Encoders are used to encode given digital number into different numbering format .like decimal to BCD Encoder, Octal to Binary.

➔Decoders are used to decode a coded binary word like BCD to seven segment decoder. Thus encoder and decoder are application specific logic develop, we cannot use any type of input for any encoder and decoder.

Assignments Questions: