CSE1003	DIGITAL LOGIC AND DESIGN	L	T	P	J	C
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Pre-requisite	**NIL**	**Syllabus version**				
		v1.1				

Course Objectives:

1. Introduce the concept of digital and binary systems.
2. Analyze and Design combinational and sequential logic circuits.
3. Reinforce theory and techniques taught in the classroom through experiments in the laboratory.

Expected Course Outcome:

1. Comprehend the different types of number system.
2. Evaluate and simplify logic functions using Boolean Algebra and K-map.
3. Design minimal combinational logic circuits.
4. Analyze the operation of medium complexity standard combinational circuits like the encoder, decoder, multiplexer, demultiplexer.
5. Analyze and Design the Basic Sequential Logic Circuits
6. Outline the construction of Basic Arithmetic and Logic Circuits
7. Acquire design thinking capability, ability to design a component with realistic constraints, to solve real world engineering problems and analyze the results.

Student Learning Outcomes (SLO):	**1,2,5,14**	
Module:1	**INTRODUCTION**	**3 hours**

Number System - Base Conversion - Binary Codes - Complements(Binary and Decimal)

Module:2	**BOOLEAN ALGEBRA**	**8 hours**

Boolean algebra - Properties of Boolean algebra - Boolean functions - Canonical and Standard forms - Logic gates - Universal gates – Karnaugh map - Don't care conditions - Tabulation Method

Module:3	**COMBINATIONAL CIRCUIT - I**	**4 hours**

Adder - Subtractor - Code Converter - Analyzing a Combinational Circuit

Module:4	**COMBINATIONAL CIRCUIT –II**	**6 hours**

Binary Parallel Adder- Look ahead carry - Magnitude Comparator - Decoders – Encoders - Multiplexers –Demultiplexers.

Module:5	**SEQUENTIAL CIRCUITS – I**	**6 hours**

Flip Flops - Sequential Circuit: Design and Analysis - Finite State Machine: Moore and Mealy model - Sequence Detector.

Module:6	**SEQUENTIAL CIRCUITS – II**	**7 hours**

Registers - Shift Registers - Counters - Ripple and Synchronous Counters - Modulo counters - Ring and Johnson counters

Module:7	**ARITHMETIC LOGIC UNIT**	**9 hours**

Bus Organization - ALU - Design of ALU - Status Register - Design of Shifter - Processor Unit - Design of specific Arithmetic Circuits Accumulator - Design of Accumulator.

Module:8	**Contemporary Issues: RECENT TRENDS**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	M. Morris Mano and Michael D.Ciletti– Digital Design: With an introduction to Verilog HDL, Pearson Education – 5th Edition- 2014. ISBN:9789332535763.
Reference Books	
1.	Peterson, L.L. and Davie, B.S., 2007. Computer networks: a systems approach. Elsevier.
2.	Thomas L Floyd. 2015. Digital Fundamentals. Pearson Education. ISBN: 9780132737968
3.	Malvino, A.P. and Leach, D.P. and Goutam Saha. 2014. Digital Principles and Applications (SIE). Tata McGraw Hill. ISBN: 9789339203405.
4.	Morris Mano, M. and Michael D.Ciletti. 2014. Digital Design: With an introduction to Verilog HDL. Pearson Education. ISBN:9789332535763
Mode of Evaluation: CAT / Assignment / Quiz / FAT / Project / Seminar	

List of Challenging Experiments (Indicative)		
1.	Realization of Logic gates using discrete components, verication of truth table for logic gates, realization of basic gates using NAND and NOR gates	4.5 hours
	Implementation of Logic Circuits by verification of Boolean laws and verification of De Morgans law	3 hours
	Adder and Subtractor circuit realization by implementation of Half-Adder and Full-Adder, and by implementation of Half-Subtractor and Full-Subtractor	4.5 hours
	Combinational circuit design i. Design of Decoder and Encoder ii. Design of Multiplexer and De multiplexer iii. Design of Magnitude Comparator iv. Design of Code Converter	4.5 hours
	Sequential circuit design i. Design of Mealy and Moore circuit ii. Implementation of Shift registers iii. Design of 4-bit Counter iv. Design of Ring Counter	4.5 hours
	Implementation of different circuits to solve real world problems: A digitally controlled locker works based on a control switch and two keys which are entered by the user. Each key has a 2-bit binary representation. If the control switch is pressed, the locking system will pass the difference of two keys into the controller unit. Otherwise, the locking system will pass the sum of the two numbers to the controller unit. Design a circuit to determine the input to the controller unit.	4.5 hours
	Implementation of different circuits to solve real world problems: A bank queuing system has a capacity of 5 customers which serves on first come first served basis. A display unit is used to display the number of customers waiting in the queue. Whenever a customer leaves the queue, the count is reduced by one and the count is increased by one if a customer joins a queue. Two sensors (control signals) are used to sense customers leaving and joining the queue respectively. Design a circuit that displays the number of customers waiting in the queue in binary format using LEDs. Binary 1 is represented by LED glow and 0 otherwise.	4.5 hours
	Total Laboratory Hours	**30 hours**
Mode of assessment: Project/Activity		
Recommended by Board of Studies		

Approved by Academic Council	No. 47	Date	05.10.2017