

## Lecture 43: SECONDARY STORAGE DEVICES

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### Magnetic Disk (Hard Disk)

- Magnetic disks constitute a traditional method for non-volatile storage of information using magnetic technology.
- Broadly three types of devices appeared:
  - a) **Floppy disk** : made of bendable plastic
  - b) **Magnetic drum** : made of solid metal
  - c) **Hard disk** : made of metal or glass
- All of these rely on a rotating platter (metal or glass or plastic) coated with a thin magnetic material, and use a moveable read/write head to read and write data from / to the disk.
  - Data stored as tiny magnets.



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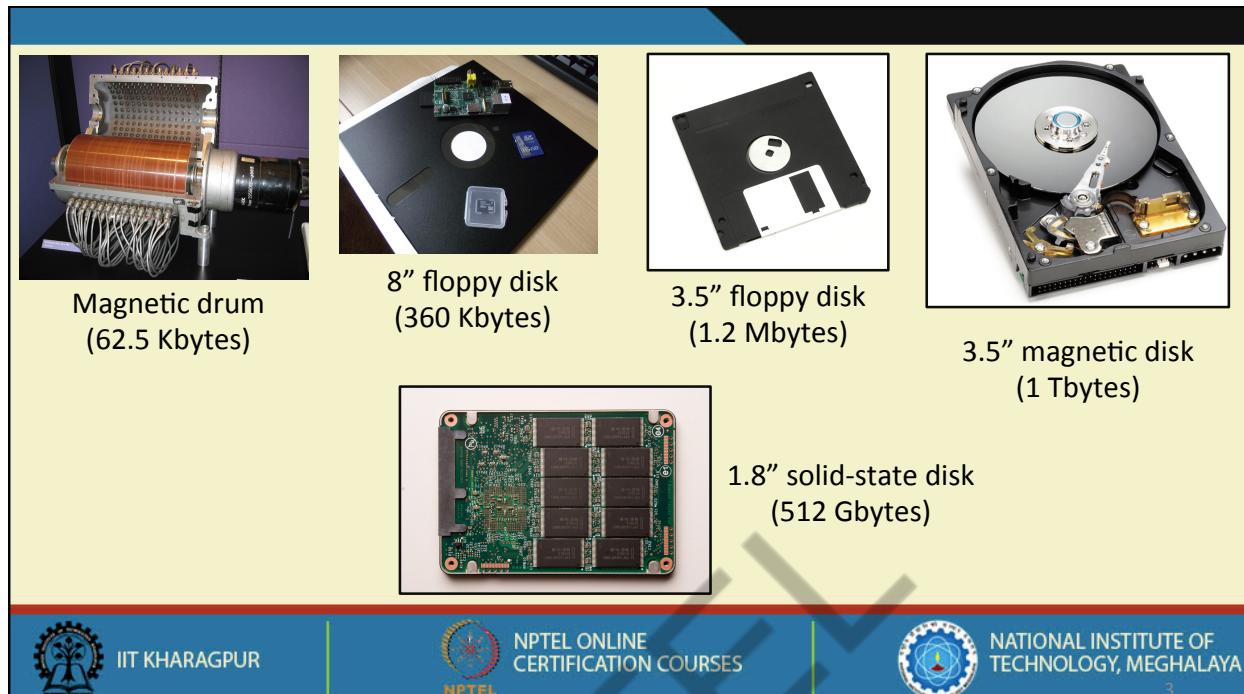


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- Since the platters in a hard disk are made of rigid metal or glass, they provide several advantages over floppy disks:
  - They can be larger.
  - Can have higher density since they can be controlled more precisely.
  - Has a higher data rate because it spins faster.
  - No physical contact with read/write head as it spins faster.
    - The read/write head floats on a cushion of air (few microns separation).
    - Requires dustless environment.
    - Results in higher reliability.
  - More than one platters can be incorporated in the same unit.



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## Organization of Data on a Hard Disk

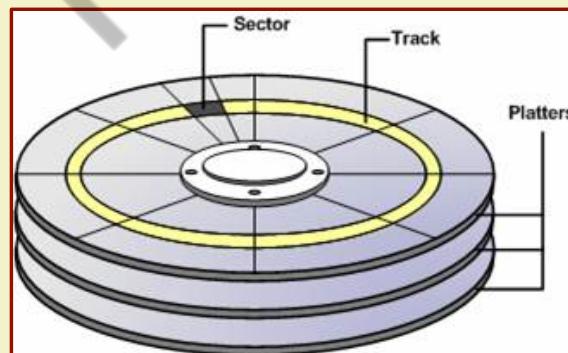
- The hard disks consists of a collection of *platters* (typically, 1 to 5), which are connected together and can spin in unison.
  - Each platter has two recording surfaces, and comes in various sizes (1 – 8 inches).
  - The stack of platter typically rotates at a speed of 5400 to 7200 rpm.
  - Each disk surface is divided into concentric circles called *tracks*.
    - The number of tracks per surface can vary from 1000 to 5000.
  - Each track is divided into a number of *sectors* (64 – 200 sectors/track).
    - Typical sector size: 512 – 2048 bytes.
    - Sector is the smallest unit that can be read or written.
  - The disk heads for all the surfaces are connected and move together.
  - All the tracks under the heads at a given time on all surfaces is called a *cylinder*.



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## Disk Access Time

- There are three components to the access time in hard disk:
  - a) Seek time:
    - The time required to move the head to the desired track.
    - Average seek times are in the range 8 – 20 msec.
    - Actual average can be 25 – 30% less than this number, since accesses to disks are often localized.



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- b) Rotational delay:

- Once the head is on the correct track, we must wait for the desired sector to rotate under the head.
- The average delay or latency is the time for half the rotation.
- Examples:
  - For 3600 rpm, average rotational delay = 0.5 rotation / 3600 rpm = 8.30 msec
  - For 5400 rpm, average rotational delay = 0.5 rotation / 5400 rpm = 5.53 msec
  - For 7200 rpm, average rotational delay = 0.5 rotation / 7200 rpm = 4.15 msec



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c) Transfer time:

- The total time to transfer a block of data (typically, a sector).
- Transfer rates are typically 15 MB/sec or more.
- Transfer time depends on:
  - Sector size
  - Rotation speed of the disk
  - Recording density on the tracks



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## Example 1

- Consider a disk with sector size 512 bytes, 2000 tracks per surface, 64 sectors per track, three double-sided platters, and average seek time of 10 msec.
  - a) What is the capacity of the disk?
  - b) If the disk platters rotate at 7200 rpm, and one track of data can be transferred per revolution, what is the transfer rate?
    - Bytes/track =  $512 \times 64 = 32K$
    - Bytes/surface =  $32K \times 2000 = 64,000K$
    - Bytes/disk =  $64,000K \times 3 \times 2 = 384,000K$
    - Transfer rate = Capacity of a track / average rotational delay  
 $= 32K / 4.15 \text{ msec} = 7,711 \text{ Kbytes/sec}$



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## Some Recent Advancements

- a) Most of the modern-day disk units include a high-speed cache directly in the disk unit.
  - Allows fast access of data that was recently read between transfers requested by the CPU.
- b) In conventional disks, each track contains the same number of bits.
  - Outer tracks record data at a lower density than inner tracks (circumference of a circle is proportional to its radius).
  - An alternate scheme uses *constant bit density*, where the outer tracks store more bits than the inner tracks.



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## Solid State Drives

- Also referred to as flash drives.
- Very popular today as removable storage devices, and also as solid-state storage devices in computer system as a replacement of hard disk.
- Some features:
  - Non-volatile
  - Low power consumption
  - Faster than hard disk
  - Random access
  - Data typically written block-wise (erase followed by write)



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## Floating-Gate MOSFET

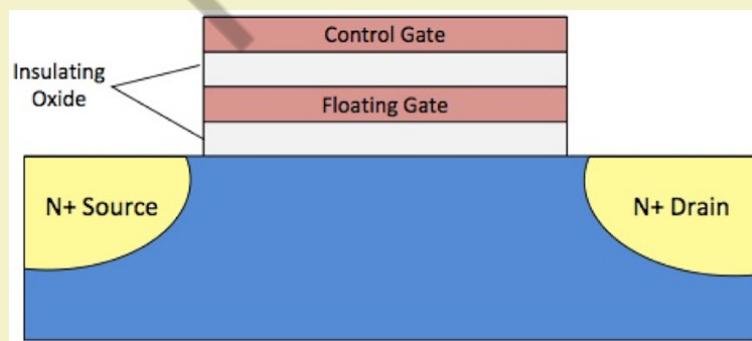
- The floating-gate MOSFET is a semiconductor device whose structure is similar to a conventional MOS transistor.
- The gate of the transistor is electrically isolated, and is referred to as floating gate (FG).
  - Since FG is surrounded by highly resistive material (insulator), the charge contained in it remains intact for long periods of time.
- By applying a suitable voltage on the control gate, the charge in FG can be controlled.
  - Presence or absence of charge can indicate binary states (0 or 1).



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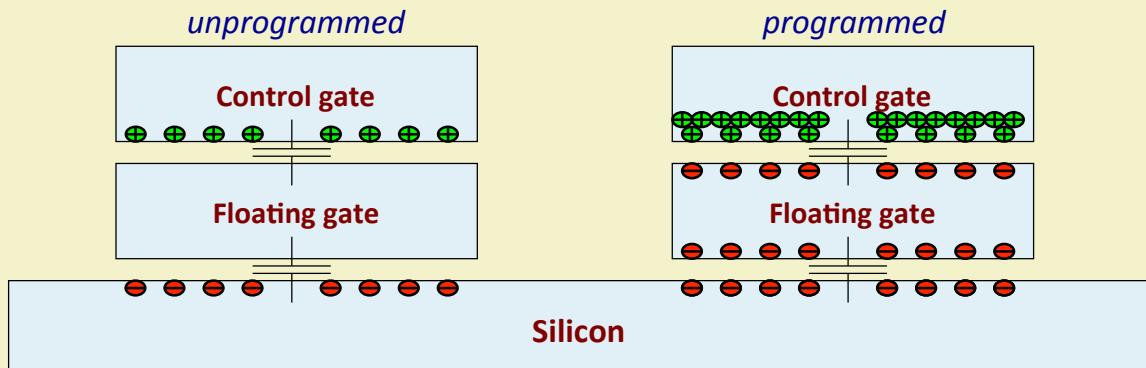
## Schematic Diagram



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## Channel charge in floating gate transistors



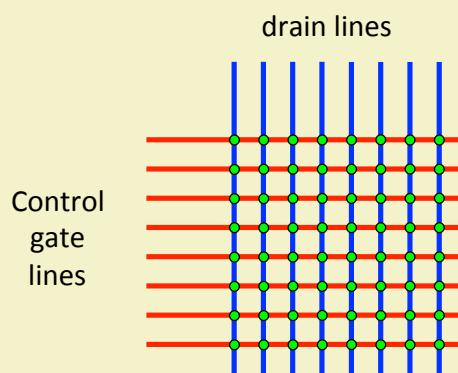
To obtain the same channel charge, the programmed gate needs a higher control-gate voltage than the unprogrammed gate



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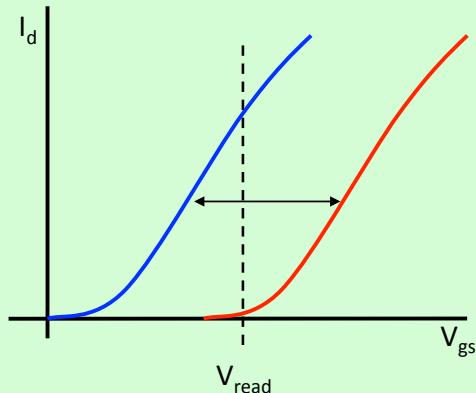
- Reading a bit means:
  - Apply a voltage  $V_{\text{read}}$  on the control gate.
  - Measure the drain current  $I_d$  of the FG transistor.
- The transistors are laid out on a 2-dimensional grid.



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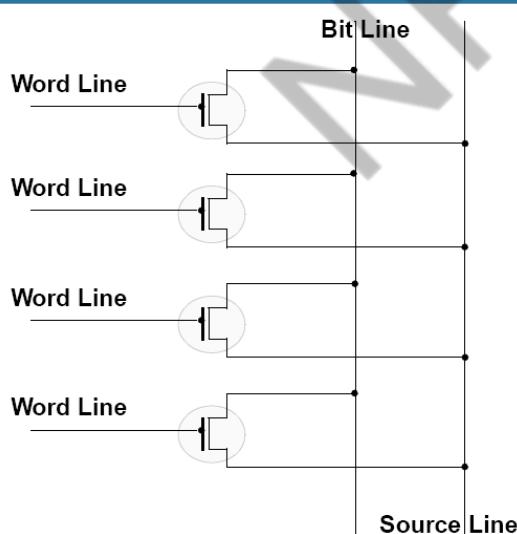
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"1"  $\rightarrow I_{read} \gg 0$   
 "0"  $\rightarrow I_{read} = 0$



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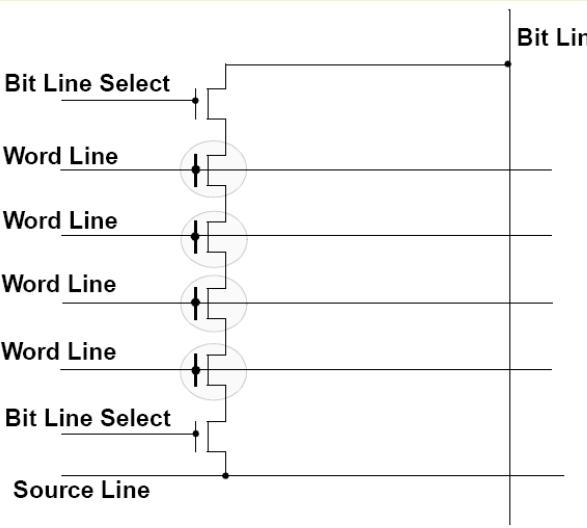
## NOR device

- Word connects to control gate; Bit connects to drain.
- Fast read ( $\sim 100$  ns)
- Slow write ( $\sim 10$   $\mu$ s)
- Used for storing code (mostly read, rarely write).
- Higher endurance.



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## NAND device

- Word connects to control gate; Bit connects to drain.
- Smaller cell size (higher density).
- Slow read ( $\sim 1 \mu\text{s}$ )
- Fast write ( $\sim 1 \mu\text{s}$ )
- Used for data storage applications.

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## Some Characteristics of NAND Flash

- Typical operations supported:
  - Read / Write a page (typical page size = 512 bytes)
  - Erase a block (set of pages)
- A block must be erased before it can be written.
- Wear leveling – an important consideration.
  - Maximum number of erases/writes per cell is typically  $\sim 1\text{M}$ .
  - Reliability of the cells decrease over time.
  - Wear leveling tries to evenly distribute cell accesses over the entire array.
    - Write page may mean copy-and-write.

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## END OF LECTURE 43



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## Lecture 44: INPUT-OUTPUT ORGANIZATION

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# Introduction

- Interfacing input/output devices is more complex as compared to interfacing memory systems.
- Why?
  - Wide variety of peripherals (keyboard, mouse, disk, camera, printer, scanner, etc.).
  - Widely varying speeds.
  - Data transfer rate can be regular or irregular.
  - Sizes of data blocks transferred at a time varies widely (few bytes to Kbytes).
- Slower than processor and memory.

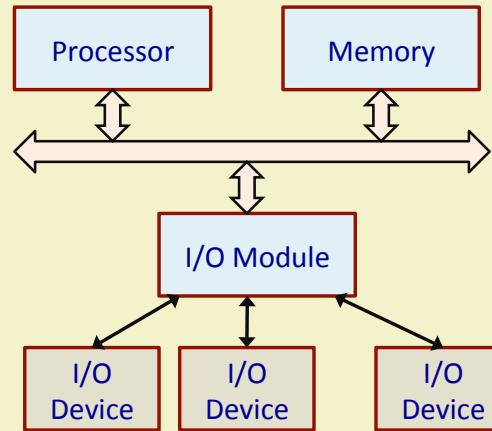


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# Input / Output Interface

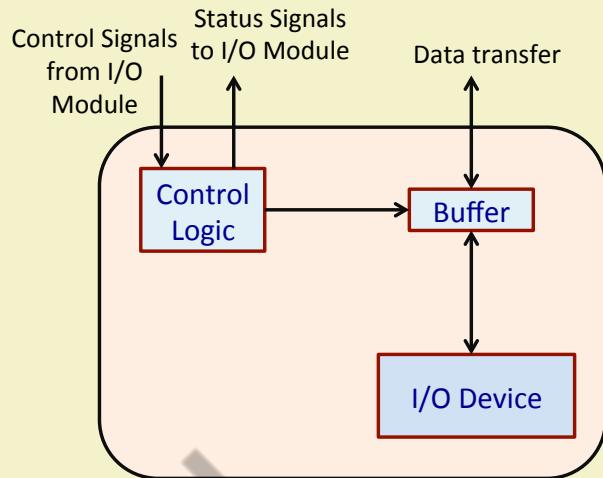
- To handle widely different types of I/O devices, we need a programmable I/O interface or *I/O module*.
  - Interfaces to processor and memory on one side.
  - Interfaces to one or more peripheral devices on the other side.



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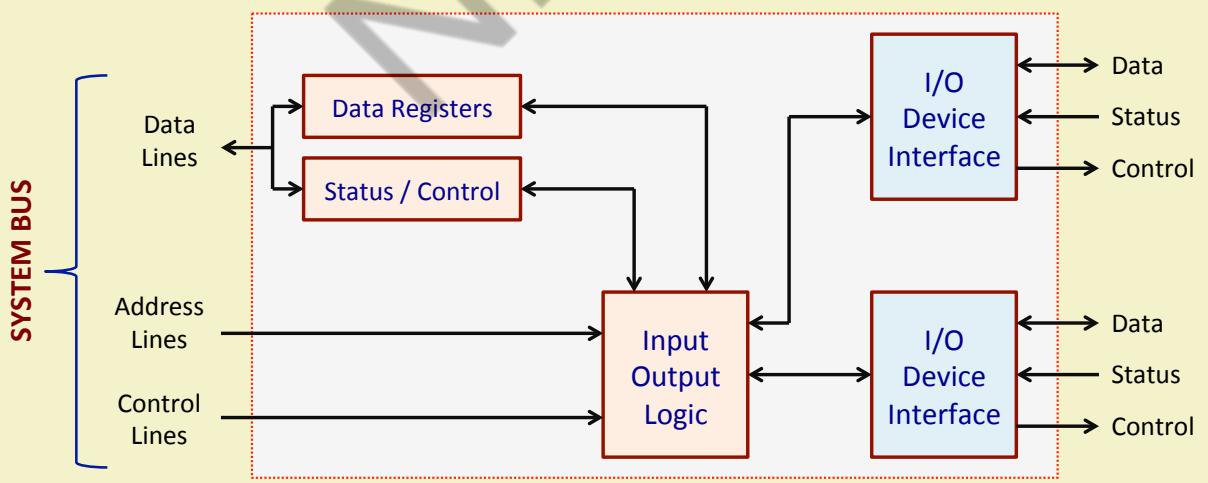
## Typical I/O Device Interface



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## I/O Module Schematic



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## Typical Steps During I/O

- a) Processor requests the I/O Module for device status.
- b) I/O Module returns the status to the processor.
- c) If the device is ready, processor requests data transfer.
- d) I/O Module gets data from device (say, input device).
- e) I/O Module transfers data to the processor.
- f) Processor stores the data in memory.



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## How are I/O devices typically interfaced?

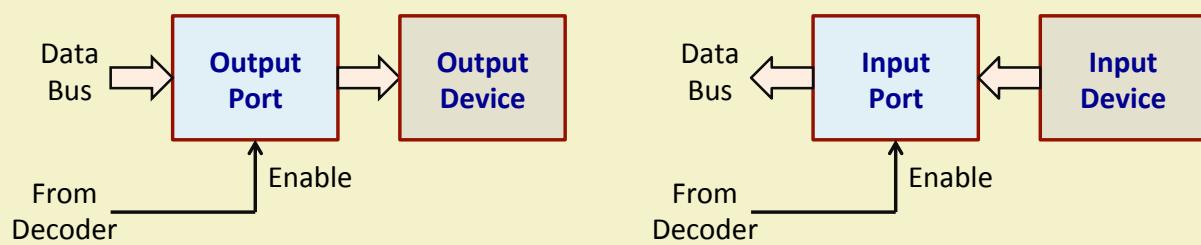
- Through input and output ports.
- Output port:
  - Basically a PIPO register that is enabled when a particular output device address is given.
  - The register inputs are connected to the data bus, and the register outputs are connected to the output device.
- Input port:
  - Basically a parallel tristate bus driver that is enabled when a particular Input device address is given.
  - The driver outputs are connected to the data bus, while the inputs are connected to the input device.



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## Example of output and input ports



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## Memory-Mapped and I/O Mapped Device Interface

- Memory-mapped device interface:
  - The same address decoder selects memory and I/O ports.
  - Some of the memory address space is occupied by I/O devices.
  - All data transfer instructions to/from memory can be used to transfer data to/from I/O devices.
  - The processor need not have separate instructions for I/O, nor it need to specify whether an address generated by the CPU is a memory address or an I/O address.



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## Example of Memory Mapped Device Interfacing



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- I/O mapped device interface:
  - Separate instructions for I/O data transfer (say, IN and OUT).
  - A processor signal identifies whether a generated address refers to a memory location or an I/O device.
  - Separate address decoders for selecting memory and I/O ports.
  - The complete memory address space can be utilized.



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## Example of I/O Mapped Device Interfacing



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**END OF LECTURE 44**



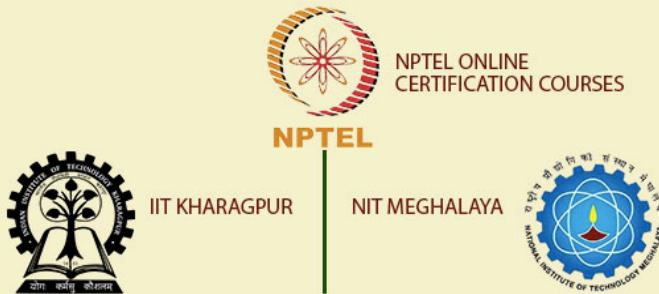
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## Lecture 45: DATA TRANSFER TECHNIQUES

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## Data Transfer Techniques

1. **Programmed**: CPU executes a program that transfers data between I/O device and memory.
  - a) Synchronous
  - b) Asynchronous
  - c) Interrupt-driven
2. **Direct Memory Access (DMA)**: An external controller directly transfers data between I/O device and memory without CPU intervention.



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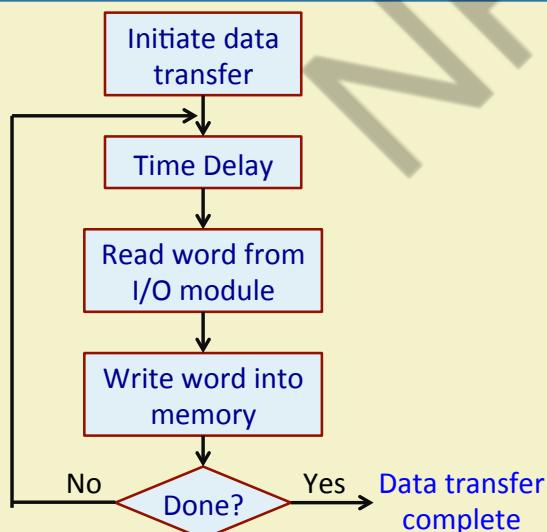
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## (a) Synchronous Data Transfer

- The I/O device transfers data at a fixed rate that is known to the CPU.
- The CPU initiates the I/O operation and transfers successive bytes/words after giving fixed time delays.
- Characteristics:
  - During the time delay, CPU lies idle.
  - Not many I/O devices have strictly synchronous data transfer characteristics.
- A flowchart for synchronous data transfer from an input device is shown on the next slide.



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- Error may occur if the input device and the processor get out of synchronization.
- Large number of words cannot be transferred in one go.
- Speed of data transfer depends not only on the speed of I/O device and memory, but also on the execution time of the code.

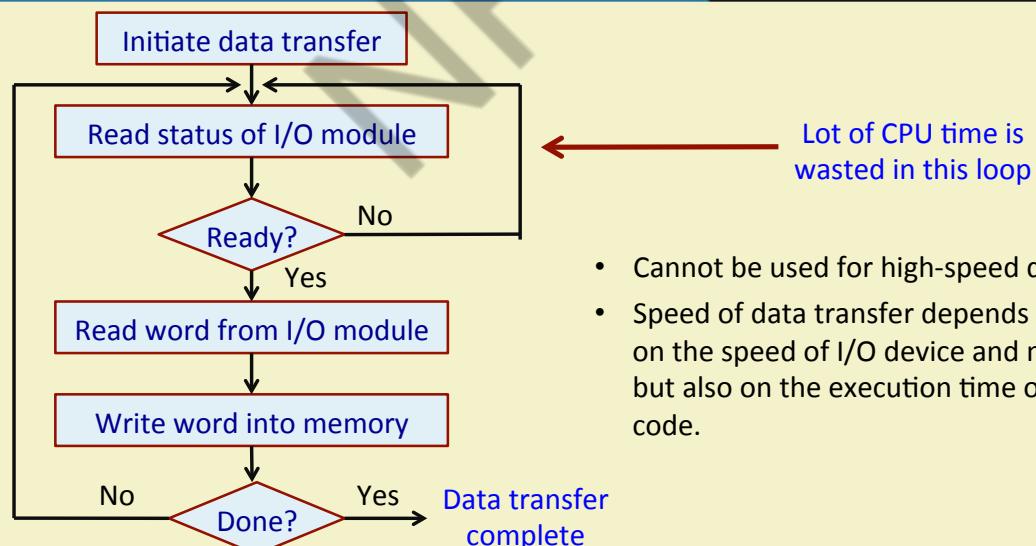


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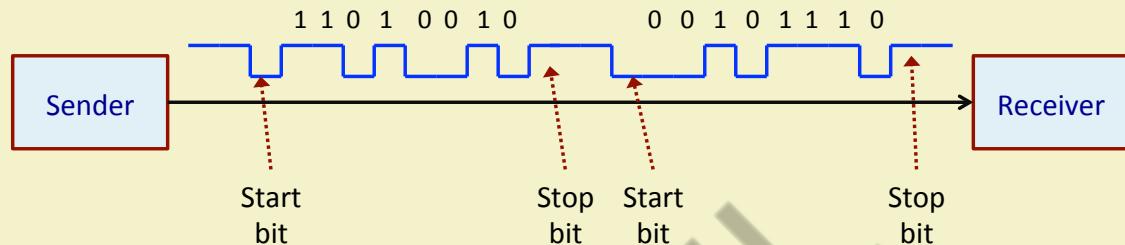
## (b) Asynchronous Data Transfer

- The CPU does not know when the I/O module will be ready to transfer the next word.
- CPU has to check the status of the I/O module to know when the device is ready to transfer the next word.
  - Called *handshaking*.
- Characteristics:
  - While the CPU is checking whether the I/O module is ready, it cannot do anything else.
  - Wasteful of CPU time for slow devices like keyboard or mouse.



- Cannot be used for high-speed devices.
- Speed of data transfer depends not only on the speed of I/O device and memory, but also on the execution time of the code.

- An example of asynchronous data transfer:
  - Serial data transfer between two devices using start and stop bits.
  - The devices are asynchronous at the level of bytes, but are synchronous at the level of bits within the bytes.



- Just like asynchronous data transfer, receiver waits for the next START bit, which indicates the beginning of a new byte transfer.
- After the START bit is received, receiver gives (known) bit delays and reads out the 8 bits of the byte.
- The STOP bits between the bytes serve to synchronize the data transmission.

## (c) Interrupt-Driven Data Transfer

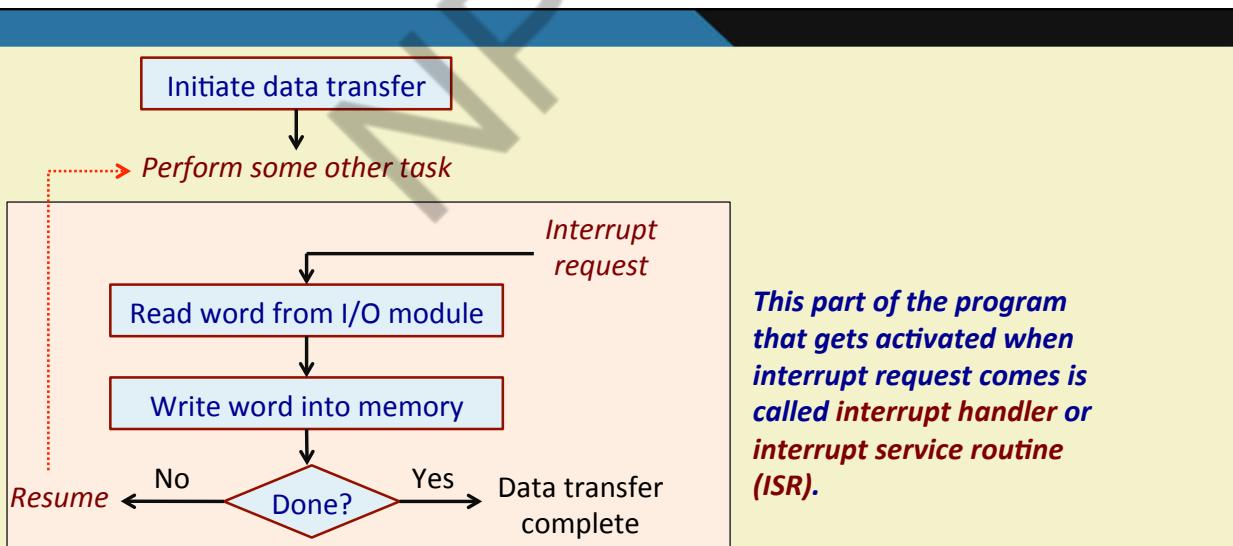
- The CPU initiates the data transfer and proceeds to perform *some other task*.
- When the I/O module is ready for data transfer, it informs the CPU by activating a signal (called *interrupt request*).
- The CPU suspends the task it was doing, services the request (that is, carries out the data transfer), and returns back to the task it was doing.
- Characteristics:
  - CPU time is not wasted while checking the status of the I/O module.
  - CPU time is required only during data transfer, plus some overheads for transferring and returning control.



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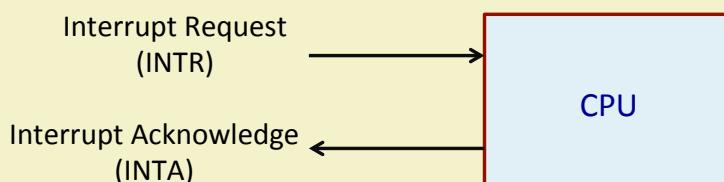
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## Some Features of Interrupt-Driven Data Transfer

- How is ISS different from a normal subroutine or function?
  - A function is called from well-defined places in the calling program.
    - Only the relevant registers need to be saved on entry to the function, and restored before return.
  - The ISS can get invoked from *anywhere* in the program that was executing.
    - Depends on when the interrupt request signal arrived.
    - So potentially all the registers that are used in the ISS needs to be saved and restored.



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- We shall learn later why the INTA signal is required.



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## Some Challenges in Interrupts

- For multiple sources of interrupts, how to know the address of the ISR?
- How to handle multiple interrupts?
  - While an interrupt request is being processed, another interrupt request might come.
  - Enabling, disabling and masking of interrupts.
- How to handle simultaneously arriving interrupts?
- Sources of interrupts other than I/O devices.
  - Exceptions, TRAP, etc.



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**END OF LECTURE 45**



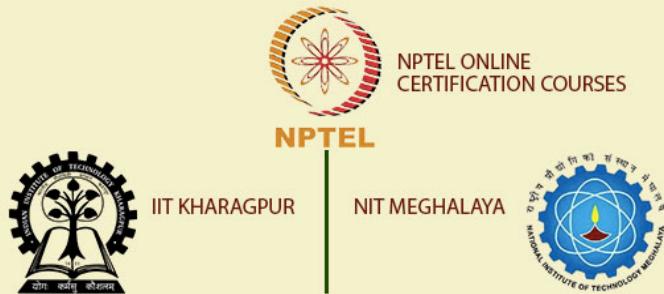
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## Lecture 46: INTERRUPT HANDLING (PART 1)

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### What happens when an interrupt request arrives?

- At the end of the current instruction execution, the PC and program status word (PSW) are saved in stack automatically.
  - PSW contains status flags and other processor status information.
- The interrupt is acknowledged, the interrupt vector obtained, based on which control transfers to the appropriate ISR.
  - Different interrupting devices may have different ISR's.
- After handling the interrupt, the ISR executes a special *Return From Interrupt (RTI)* instruction.
  - Restores the PSW and returns control to the saved PC address.
  - Unlike normal RETURN where PSW is not restored.



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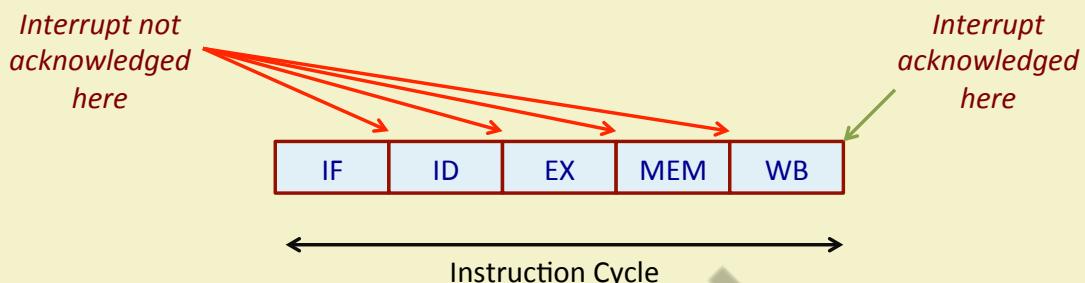
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- An instruction cycle typically consists of several machine cycles.
  - For MIPS32, there are 5 machine cycles.

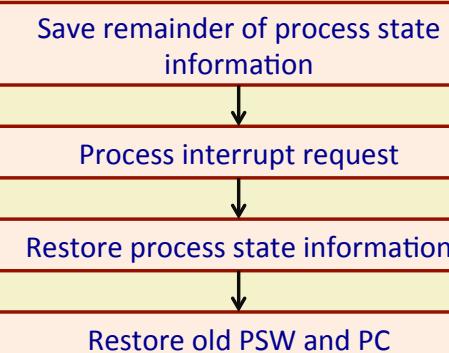
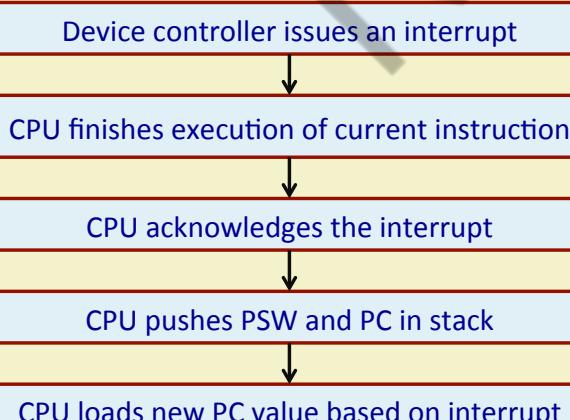


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## General Interrupt Processing

### By hardware

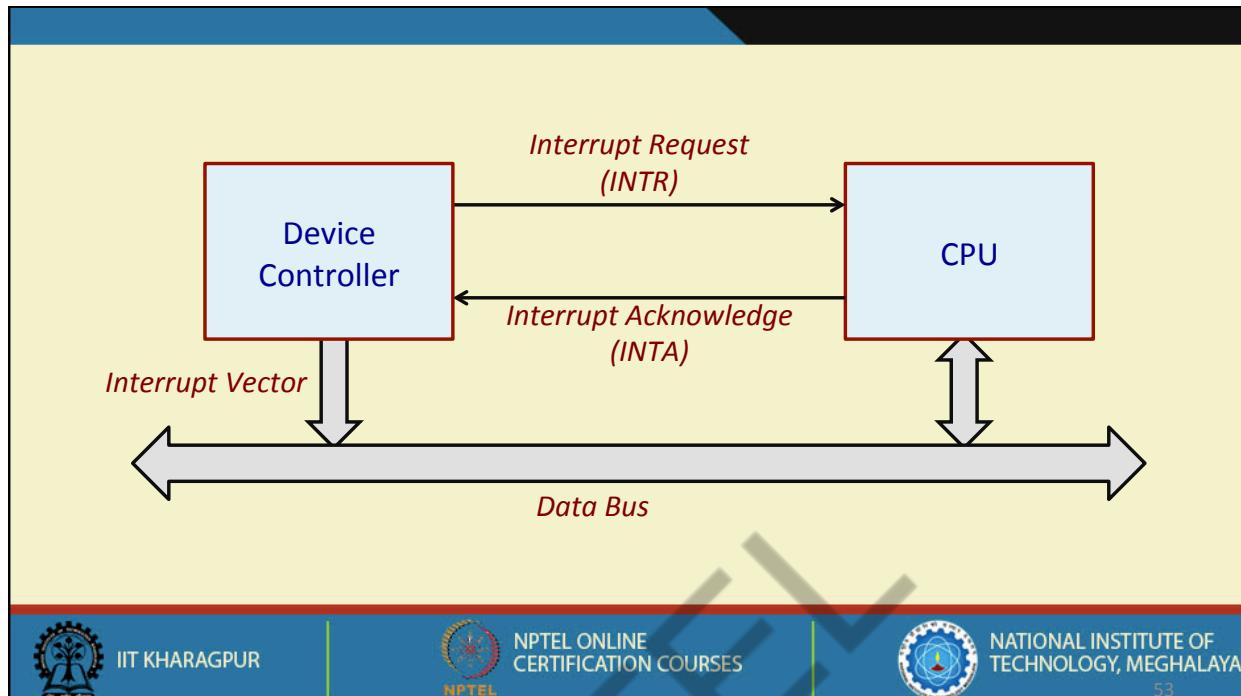


### By software



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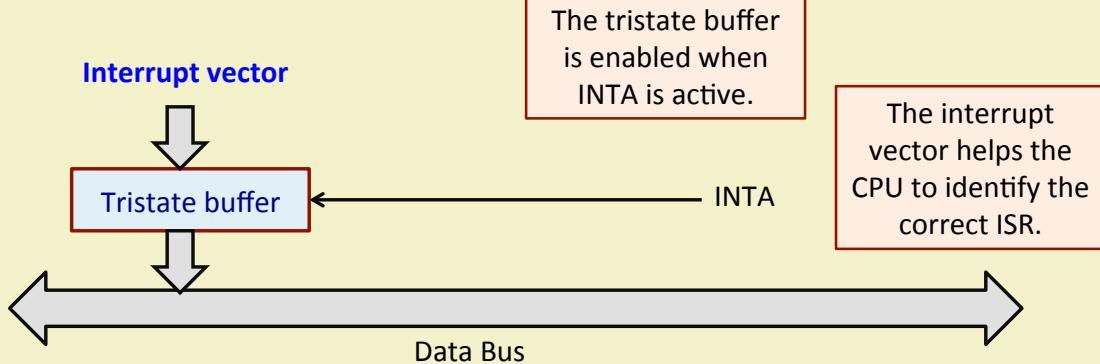
- The steps:
  - a) Device controller sends INTR to the CPU.
  - b) CPU finishes the current instruction and sends back INTA.
  - c) Device controller sends interrupt vector (or number) over data bus.
  - d) CPU reads the interrupt vector, and identifies the device.



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- How is the interrupt vector sent on the data bus in response to INTA?

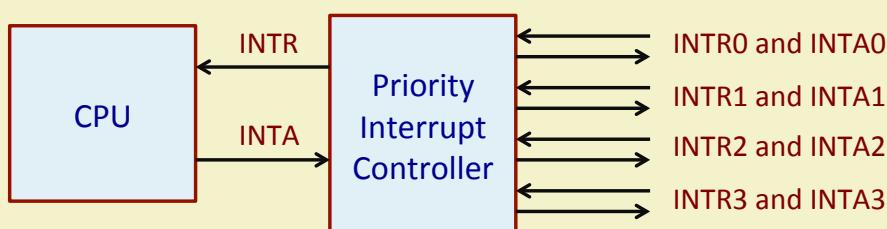


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## Multiple Devices Interrupting the CPU

- A common solution is to use a priority interrupt controller.
  - The interrupt controller interacts with CPU on one side and multiple devices on the other side.
  - For simultaneous interrupt requests, interrupt priority is defined.
  - The interrupt controller is responsible for sending the interrupt vector to CPU.



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- How it works?

- The INTR line is made active when some of the device(s) activate their interrupt request line.

$$\text{INTR} = \text{INTRO} + \text{INTR1} + \text{INTR2} + \text{INTR3}$$

- When the CPU sends back INTR, the interrupt controller sends back the corresponding acknowledge to the interrupting device, and puts the interrupt vector on the data bus.
- The interrupt controller is programmable, where the interrupt vectors for the various interrupts can be programmed (specified).
- For more than one interrupt request simultaneously active, a priority mechanism is used (e.g. INTRO is highest priority, followed by INTR1, etc.).



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## How is interrupt nesting handled?

- Consider the scenario:

- a) A device D0 has interrupted and the CPU is executing the ISR for D0.
- b) In the mean time, another device D1 has interrupted.

- Two possible scenarios here:

- D1 will interrupt the ISR for D0, get processed first, and then the ISR for D0 will be resumed. → **CREATES PROBLEM FOR MULTI NESTING**
- Disable the interrupt system automatically whenever an interrupt is acknowledged so that handling of nested interrupts is not required.



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- Typical instruction set architectures have the following instructions:
  - EI : Enable interrupt
  - DI : Disable interrupt
- For the second scenario as discussed, the ISR will give an EI instruction just before RTI.
  - Some ISA combine EI and RTI in a single instruction.
- The DI instruction is sometimes used by the operating system to execute atomic code (e.g. semaphore wait and signal operations).
  - Nobody should interrupt the code while it is being executed.



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## Cases that make interrupt handling difficult

- For some interrupts, it is not possible to finish the execution of the current instruction.
  - A special RETURN instruction is required that would return and *restart* the interrupted instructions.
- Some examples:
  - a) [Page fault interrupt](#): A memory location is being accessed that is not presently available in main memory.
  - b) [Arithmetic exception](#): Some error has occurred during some arithmetic operation (e.g. division by zero).



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## END OF LECTURE 46



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## Lecture 47: INTERRUPT HANDLING (PART 2)

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## Handling Multiple Devices

- Suppose that a number of devices capable of generating interrupts are connected to the CPU.
- The following questions need to be answered.
  - a) How can the CPU identify the interrupting device?
  - b) How can the CPU obtain the starting address of the appropriate ISR?
  - c) Should interrupt nesting be allowed?
  - d) How should two or more simultaneous interrupt requests be handled?



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### (a) Device Identification

- Suppose that an external device requests an interrupt by activating an INTR line that is common to all the devices. That is,
- $$\text{INTR} = \text{INTR}_1 + \text{INTR}_2 + \dots + \text{INTR}_n$$
- Each device can have a status bit indicating whether it has interrupted.
    - CPU can *poll* the status bits to find out who has interrupted.
  - A better alternative is to use the interrupt vector concept discussed earlier.
    - The interrupting device sends a special identifying code on the data bus upon receiving the interrupt acknowledge.



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## (b) Find Starting Address of ISR

- For a processor with multiple interrupt request inputs, the address of the ISR can be fixed for each individual input.
  - Lacks flexibility.
- If we use the interrupt vector scheme discussed earlier, the device is able to identify itself to the CPU.
  - CPU can then lookup a table where the ISR addresses for all the devices are stored.
  - The interrupt latency is somewhat increased, since we are not immediately jumping to the ISR.



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## (c) Interrupt Nesting

- A simple approach:
  - Disable all interrupts during the execution of an ISR.
  - This ensures that the interrupt request from one device will not cause more than one interruptions.
  - ISR's are typically short, and the delay they may cause in handling a second interrupt request is often acceptable.
- Interrupt priority:
  - Some interrupting devices may be assigned higher priorities than others.
  - *Example:* timer interrupt to maintain a real-time clock.
  - Higher priority interrupt may interrupt the ISR of lower priority ones.



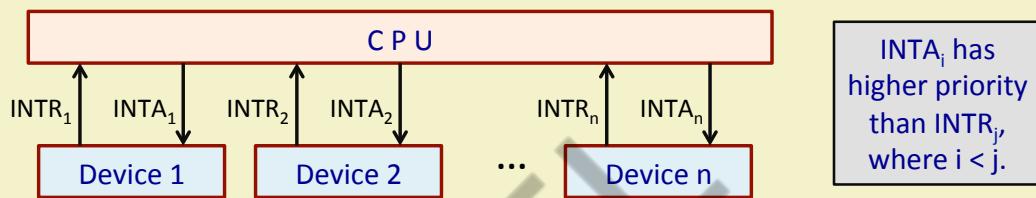
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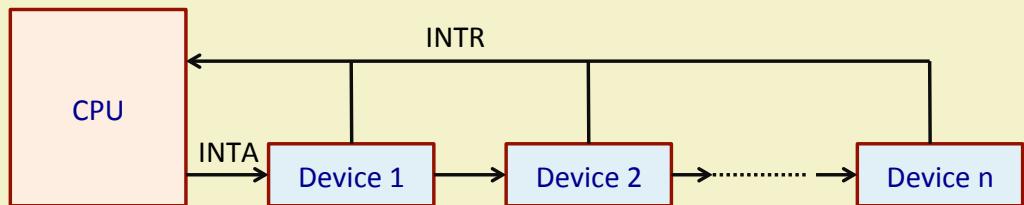
## (d) Simultaneous Requests

- Here we consider the problem of simultaneous arrivals of interrupt requests from two or more devices.
  - CPU should have some mechanism by which only one request is serviced while the others are delayed or ignored.
  - If the CPU has multiple interrupt request lines, it can have a *priority scheme* where it accepts the request with the highest priority.



- Another way to assign priority is to use polling using *daisy chaining*.
  - In polling, priority is automatically assigned based on the order in which the devices are polled.
  - In daisy chain connection, the INTR line is common to all the devices, but the INTA line is connected in a daisy chain fashion allowing it to propagate serially through the devices.
  - A device when it receives INTA, passes the signal to the next device only if it had not interrupted. Else, it stops the propagation of INTA, and puts the identifying code on the data bus.
  - Thus, the device that is electrically closest to the CPU will have the highest priority.

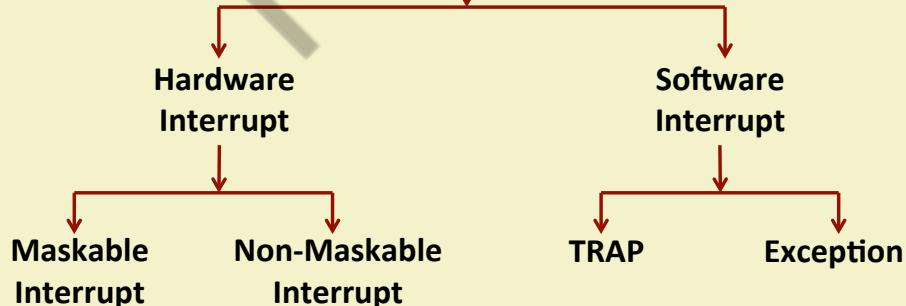
## Daisy Chain Arrangement



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## Types of Interrupts



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- **Hardware Interrupt:**
  - The interrupt signal is coming from a device external to the CPU.
  - Example: keyboard interrupt, timer interrupt, etc.
- **Maskable Interrupt:**
  - Hardware interrupts that can be masked or delayed when a higher priority interrupt request arrives.
  - There are processor instructions that can selectively mask and unmask the interrupt request lines of the CPU.



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- **Non-Maskable Interrupt:**
  - Interrupts that cannot be delayed and should be handled by the CPU immediately.
  - Examples: power fail interrupts, real-time system interrupts, etc.



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- Software Interrupt:
  - They are caused due to execution of some instructions.
  - Not caused due to external inputs.
- TRAP:
  - They are special instructions used to request services from the operating system.
  - Also called *system calls*.



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- Exception:
  - These are unplanned interrupts generated while executing a program.
  - They are generated from within the system.
  - Examples: invalid opcode, divide by zero, page fault, invalid memory access, etc.



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