VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

**CAT II-G1-AK**

## School of Computer Science and Engineering

## CSE2001-Computer Architecture and Organization

**Exam Duration: 90 minutes** **Maximum Marks: 50**

### Answer all the questions

1. A system is following Non-restoring algorithm for its division operation. Add sufficient changes to the Non-restoring algorithm to perform floating point division. Show the revised algorithm and division steps for the given data.

$(10010 * 2^{-8}) / (00011 * 2^{-3})$ 10

Ans: Include the floating point addition steps with the non-restoring division algorithm.

| | A | D | C |
|---|---|---|---|
| | 00000 | 10010 | 5 |
| SHL | 00001 | 0010- | |
| A_M | 11110 | 00100 | 4 |
| SHL | 11100 | 0100- | |
| A+M | 11111 | 01000 | 3 |
| SHL | 11110 | 1000- | |
| A+M | 00001 | 10001 | 2 |
| SHL | 00011 | 0001- | |
| A_M | 00000 | 00011 | 1 |
| SHL | 00000 | 0011- | |
| A_M | 11101 | 00110 | 0 |
| A+M | 00000 | 00110 | |

2. A) The processor needs to transfer a file of 32768 kilobytes from disk to main memory. The memory is byte addressable. The size of the data count register of a DMA controller is 16 bits. What is the minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory in the following transfer mode?

a. Cycle stealing mode : 32768*1024 times
b. Block transfer/ Burst transfer mode : $2^{15}*2^{10} / 2^{16}=512$ 5

B) Burst mode of transfer make CPU idle for a long time, Cycle stealing mode request bus for each byte transfer and transparent mode need a complex circuitry to monitor and use bus when CPU is idle. But DMA is using to save processing time. How DMA achieve it? 5
Ans: working principle of DMA

3. A) Consider a computer system with 2 level caches. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns, 10ns, and 1000ns, respectively. The hit ratio of Level 1 and Level 2 caches are 70% and 90%, respectively. What is the average access time of the system ignoring the search time within the cache? 5

Ans: (0.7*1) + (0.3(0.9*10)) + (0.3*0.1*1000) = 33.4ns

B) A computer employs RAM chips of 256 x 8 and ROM chips of 128 x 8. The computer system needs 4K bytes of RAM, 1K x 16 of ROM, and two interface units with 256 registers each. Then, calculate the following,

a. Number of RAM chips : 16 chips
b. Number of ROM chips : 16 chips
c. Value of x, y and z :

| | x | y | z |
|---|---|---|---|
| RAM | 8 | 4 | 2 |
| ROM | 7 | 3 | 2 |
| I/F | 8 | 1 | 2 |

4. A) The 12bit data stored in the memory is 101110000000 and this data met with a single data bit error. Assume that the system followed the hamming code error for error check. Identify the error bit position and correct it. 5

Ans: Check bits in the received data = 1 0 0 0 →A

Data bits are 1 0 1 1 0 0 0 0

Check bits from the data bits = 1 1 1 1 →B

A X-OR B = 0111 = 7

$7^{th}$ position / D4 is in error

B) The main memory of a system has 32bit physical address space and the page size of virtual memory is 4Kbytes. The maximum size of the page table is 12MByte and each entry of page table has 1dirty bit, 1 valid bit, 2 permission bits and frame number. Calculate the size of virtual address. 5

Page size = 4KB

Page tables size = 12MB

Single page table entry size = 1db+1vb+2pb+no. of bits for frame number

No. of bits for frame number = bits in physical Address – bits for addressing within a page

= 32 -12 = 20

Single page table entry size = 1+1+2+20 = 24

No. of page table entries = page table size / an entry size

= 12MB / 24 bits = $(12 * 2^{20}) / 3 = 2^{22}$

Virtual address space = No.of pagetable entry * page table siaze

$= 2^{22} * 2^{12}$

$=2^{34}$

Virtual address size = 34bits

5. A computer has the main memory with $2^{32}$ bytes size and has the word size $2^2$ bytes. The cache memory size is $2^{20}$ bytes and each cache line is $2^8$ words. What is the length of tag field of its physical address, for a 4-way set-associative cache memory? 10

Ans: x=32,w=2, y=20 m=8 N=4

No of bits in the address = X-W

No. of bits in the word field = M

No. of sets = $2^{Y-M-W}/N$

No. of bits in the set field = Y-M-W-logN

No. of bits in the tag field = X-W-(Y-M-W-logN+M)

= X-W-Y+M+W+logN-M

= X-Y+logN

=32-20+log 4

=14

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