Course code	Digital Logic and Design	L	T	P	J	C
CSE1003		3	0	2	0	4
Pre-requisite	-	Syllabus version				
		v. xx.xx				

Course Objectives:

1. **Introduce the concept of digital and binary systems**
2. **Design and analyze combinational logic circuits.**
3. **Design and analyze sequential logic circuits.**
4. **Design functional blocks of a digital system.**
5. **Reinforce theory and techniques taught in the classroom through experiments in the laboratory.**

Expected Course Outcome:

CO1: Comprehend the different types of number systems.
CO2: Evaluate and simplify logic functions using Boolean Algebra andK-map
CO3: Design minimal combinational logic circuits.
CO4: Analyze the operation of medium complexity standard combinational circuits like the encoder, decoder, multiplexer, demultiplexer.
CO5:Familiar with basic sequential components and analyze and design the FSM
CO6: Design different types of registers and counters using flip flops
CO7:Design Arithmetic and Logic Circuits

Student Learning Outcomes (SLO):	1,2,5,14

Module:1	INTRODUCTION	3 hours	SLO: 1

Number System - Base Conversion- Binary Codes - Complements(Binary and Decimal)

Module:2	BOOLEAN ALGEBRA	8 hours	SLO: 2

Boolean algebra - Properties of Boolean algebra - Boolean functions - Canonical and Standard forms - Logic gates - Universal gates - Karnaugh map - Don't care conditions - Tabulation Method

Module:3	COMBINATIONAL CIRCUIT – I	4 hours	SLO: 2,5

Adder -Subtractor- Code Converter -Analyzing a Combinational Circuit

Module:4	COMBINATIONAL CIRCUIT –II	6 hours	SLO: 2,5

Binary Parallel Adder- Look ahead carry - Magnitude Comparator - Decoders – Encoders - Multiplexers –Demultiplexers

Module:5	SEQUENTIAL CIRCUITS – I	6 hours	SLO: 1,2,5

Flip Flops - Sequential Circuit: Design and Analysis - Finite State Machine: Moore and Mealy model - Sequence Detector

Module:6	SEQUENTIAL CIRCUITS – II	7 hours	SLO: 2,5

Registers - Shift Registers - Counters - Ripple and Synchronous Counters - Modulo counters - Ring and Johnson counters

Module:7	**ARITHMETIC LOGIC UNIT**	**9 hours**	**SLO: 1,2,5**
Bus Organization- ALU-Design of ALU-Status Register-Design of Shifter - Processor Unit- Design of specific Arithmetic Circuits- Accumulator-Design of Accumulator			
Module:8	**Contemporary issues:**	**2 hours**	**SLO: x,x**
	Total Lecture hours:	**45 hours**	

Text Book(s)	
1.	1.M. Morris Mano – Digital Logic and Computer Design, Pearson Education India – 1st Edition-2016, ISBN: 9789332542525
Reference Books	
1.	1.A.P. Malvino, D.P. Leach and GoutamSaha – Digital Principles and Applications(SIE) – Tata McGraw Hill 8th Edition – 2014, ISBN: 9789339203405. 2.M. Morris Mano and Michael D.Ciletti– Digital Design: With an introduction to Verilog HDL - Pearson Education – 5th Edition- 2014. ISBN:9789332535763 3.Thomas Floyd – Digital Fundamentals – Pearson Education-10th Edition – 2011, ISBN: 9788131734483.
	Authors, book title, year of publication, edition number, press, place

Mode of Evaluation:

Lab (Indicative List of Experiments in the areas of)	**SLO: 1, 2, 5, 14**
Study of Logic Gates Logic gates using discreteComponents Verification of truthtable for logic gates Realization of basic gates using NAND and NOR gates Implementation of LogicCircuits Verification of Boolean laws Verification of De Morgan's law Adder and Subtractor Implementation of Half-Adder and Full-Adder Implementation of Half-Subtractor and Full-Subtractor Combinational Circuit Design Design of Decoder and Encoder	

Design of Multiplexer and De multiplexer Design of Magnitude Comparator Design of CodeConverter Sequential Circuit Design Design of Mealy and Moore circuit Implementation of Shift registers Design of 4-bit Counter Design of Ring Counter	

List of Challenging Experiments (Indicative)

1.	Consider four seats, numbered 0 to 3, arranged in a circle and described by Boolean variables I0to I3. Boolean variable I0is true if seat 0 is occupied and I0is false if the seat is not occupied, likewise for I1, I2, and I3. Write a Boolean expression that's true if at least two people are sitting next to each other and at least one seat is not occupied and design the circuit using basic gates.	X hours
2.	Controller of a car has three control switches, Accelerator (A), Brake (B) and Clutch (C). A Car runs if A is pressed and either (B and C are not pressed) or C is pressed and B is not pressed. When the switch C alone is pressed then the car will be in running state. If all the three switches are pressed together then we can't predict the result. In all other cases, car will be in off state. Design a circuit to implement this scenario using Universal gates.	X hours
3.	A digitally controlled locker works based on a control switch and two keys which are entered by the user. Each key has a 2-bit binary representation. If the control switch is pressed, the locking system will pass the difference of two keys into the controller unit. Otherwise, the locking system will pass the sum of the two numbers to the controller unit. Design a circuit to determine the input to the controller unit	X hours
4.	The controller unit in the above problem compares the input data with the predefined data to allow access to the locker. Assuming the predefined key to be (01)2, design the circuit that outputs true if the predefined key and the input to the controller unit are similar.	X hours
5.	A bank queuing system has a capacity of 5 customers which serves on first come first served basis. A display unit is used to display the number of customers waiting in the queue. Whenever a customer leaves the queue, the count is reduced by one and the count is increased by one if a customer joins a queue. Two sensors (control signals) are used to sense customers leaving and joining the queue respectively. Design a circuit that displays the number of customers waiting in the queue in binary format using LEDs. Binary '1' is represented by LED glow and '0' otherwise.	X hours
	Total Laboratory Hours	30 hours

Mode of evaluation:			
Recommended by Board of Studies	DD-MM-YYYY		
Approved by Academic Council	No. xx	Date	DD-MM-YYYY

CO-PO MAPPING:

	PO 1 SLO 1	PO 2 SLO 2	PO 3 SLO 5	PO 9 SL014	PO 10	PO 11	PO 12	PO 13	PO 15	PO 16	PO 18	PO 20
CO1	*	*										
CO2		*										
CO3		*	*									
CO4		*	*									
CO5		*	*									
CO6			*									
CO7			*	*								

2. Knowledge Areas that contain topics and learning outcomes covered in the course

Knowledge Area	Total Hours of Coverage [Theory]
CE: DIG (Digital Logic)	42
CS: AR Digital Logic and Digital Design	3
Total	45 Hours [45]

2.1 Body of Knowledge coverage

KA	Knowledge Unit	Topics Covered	Hours
CE:	History and overview	Introduction to logic circuits, switching, memory,	1

DIG 0 CS: AR	Digital Logic and Digital Systems	registers, counters and digital systems	
CE: DIG 1	Switching theory	Number System and Codes Binary Arithmetic and Complements Boolean algebra: Properties of Boolean algebra Boolean functions: Canonical and Standard forms Minimization: Karnaugh map, Don't care conditions, Tabulation Method	10
CE: DIG 2 CS:AR	Combinational Logic Circuits Digital Logic and Digital Systems	Logic gates ,Universal gates Realization of switching functions using logic gates Analyzing a Combinational Circuit	2
CE: DIG 3	Modular design of combinational circuits	Adder, Subtractor Binary Parallel Adder, Look ahead carry Magnitude Comparator, Code Converter Decoders, Encoders Multiplexers, Demultiplexers	8
CE: DIG 4 and 5	Memory Elements Sequential Logic Circuits	Flip Flops Sequential Circuit: Design and Analysis Finite State Machine: Moore and Mealy model Sequence Detector	6

CE: DIG 6	Digital systems design	Registers, Shift Registers Counters: Ripple and Synchronous Counters, Modulo counters, Ring and Johnson counter	7
CE: DIG 6	Analyze and design functional building blocks	Bus Organization -ALU –Design of ALU -Status Register –Design of Shifter -Processor Unit- Design of specific Arithmetic Circuits - Accumulator – Design of Accumulator	9
CE: DIG 6 CS:AR	Recent Trends Digital Logic and Digital Systems		2
		Total hours	45

3. Where does the course fit in the curriculum?

This course is a

- Core Course.
- Suitable from 2nd semester onwards.
- Knowledge of basic electrical and electronics is desirable.

4. What is covered in the course?

The digital logic and design covers the digital building blocks and techniques in the design of digital systems. Emphasis is on a building-block approach. This syllabus covers a variety of basic topics, including switching theory, combinational circuits such as adders, subtractors, encoder, decoder, multiplexer, demultiplexer etc. The sequential logic covers memory elements and its application includes design of counters and registers along with functional blocks of a digital computer.

4.1 Part 1: Introduction and Boolean Algebra

This section deals with introduction of number system, binary codes and its arithmetic, Boolean algebra, Boolean function and minimization techniques.

4.2 Part II: Combinational Circuits

This section covers logic gates, universal gates, adder, subtractor, encoder, decoder, multiplexer, de multiplexer and design of a minimal combinational circuit.

4.3 Part III: Sequential Circuits

This section deals with memory elements, design of sequential circuit using memory elements, analysing a sequential circuit, design of finite state machines, registers and counters.

4.4 Part IV: Functional Blocks of a Computer

This section deals with design of functional blocks of a digital computer.

5. What is the format of the course?

This Course is designed with 150 minutes of in-classroom sessions per week, additional video/reading instructional material every week and 100 minutes of lab hours per week. Generally this course has the combination of lectures, in-class discussion, assignments, mandatory off-class reading material, quizzes.

6. How are students assessed?

- Students are assessed on a combination of assignments, continuous and final assessment tests.
- Students will be provided with problem sets for every module.

7. Session wise plan

Sl. No	Topic Covered	Class Hour	Lab Hour	levels of mastery	Text/Reference Book	Remarks
1	Introduction to logic circuits, switching, memory, registers, counters and digital systems Number System and Codes	3	2	Familiarity	1,3	

	Binary Arithmetic and Complements			Usage		
2	Boolean algebra: Properties of Boolean algebra Boolean functions: Canonical and Standard forms , Simplification	3	2	Usage	1,4	
3	Minimization: Karnaugh map, Don't care conditions Tabulation Method	3		Usage	1,4	
4	Tabulation Contd., Logic gates ,Universal gates, Realization of switching functions using logic gates, Adder, Subtractor	3	2	Usage	1,4	
5	Analyzing a Combinational Circuit,Magnitude Comparator, Code Converter, Binary Parallel Adder	3	4	Assessment	1,3	
6	Look ahead carry, Decoders, Encoders Multiplexers,Demultiplexers	3	2	Usage	1,3	
7	Flip Flops Sequential Circuit: Design and Analysis	3	2	Assessment	1,3	
8	Finite State Machine: Moore and Mealy model, Sequence Detector	3	2	Usage	1,5	

10	Registers, Shift Registers , Ripple Counters	3	2	Assessment	1,5	
11	Synchronous counters, Modulo counters, Ring and Johnson counters	3	4	Usage	1	
12	BusOrganization, DesignofALU	3		Assessment	1	
13	Status Register DesignofShifter	3	2	Usage	1	
14	Processor Unit DesignofspecificArithmeticCircuits	3		Familiarity	1	
15	DesignofAccumulator Recent Trends	3		Familiarity	1	
Total hours covered		45 Hours (3 Credit hours /week 15 Weeks schedule)	30 Hours (1 Credit hours / week)			