Tutorial 2

Computer Architecture and Organization

Submission date : 31-10-2019

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1. A computer system employs a cache with the hit ratio, 80 % for write operation and 90% for read operation. Dynamic memory access time is 250ns and the cache memory access time is 28ns. Out of all memory references, 70% are read operations and 30% are write operations. Calculate the average access time for all references (both read and write), for the following two specifications of the system.
    a. Write operation is write back and read is look through.
    b. Write operation is write through and read is look aside.
2. Consider a 4-way set associative cache memory with total 8 cache lines and a main memory with 256 blocks. Find the memory blocks which will be present in the cache after the following sequence of memory block references with the following block replacement algorithms. Assuming that initially the cash is empty.

    8 2 4 7 8 4 2 3 6 2 13 2 32 7 53 7 27 53 48 18 15 7 2 82

    a. LFU policy is used for cache block replacement
    b. LRU policy is used for cache block replacement
3. A computer employs RAM chips of 128 x 8 and ROM chips of 256 x 8. The computer system needs 4K bytes of RAM, 2K x 32 of ROM, and two interface units with 256 registers each. Then, calculate the following,
    - Number of RAM chips
    - Number of ROM chips
    - Value of x, y and z
4. A computer has the main memory with 2^{32} bytes size and has the word size 2^2 bytes. The cache memory size is 2^{20} bytes and each cache line is 2^8 words. What is the length of tag field of its physical address, for a 4-way set-associative cache memory?