# CSE1003 Digital Logic and Design

#### Module 2 BOOLEAN ALGEBRA L6

Dr. S. Hemamalini
Professor
School of Electrical Engineering
VIT Chennai

# Module 2 BOOLEAN ALGEBRA 8 hrs

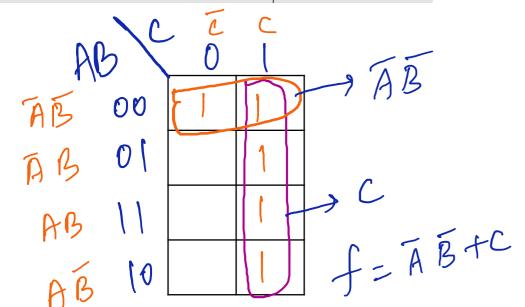
#### Boolean algebra

- Properties of Boolean algebra
- Boolean functions
- Canonical and Standard forms
- Logic gates Universal gates
- Karnaugh map Don't care conditions
- Tabulation Method

#### **Plotting a Truth Table on K-map**

A truth table and corresponding SOP K-map

	Inputs		Output
A	В	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



$$F(A,B,C,D) = ABC(D+\overline{D}) + \overline{B}CD(A+\overline{A}) + BD(A+\overline{A})(C+\overline{C})$$

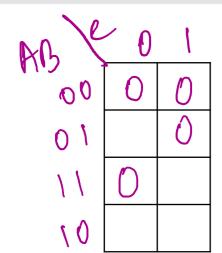
$$= ABCD + ABC\overline{D} + A\overline{B}CD + \overline{A}\overline{B}CD + ABCD$$

AB AB

#### **K-map For POS Expression**

A truth table and corresponding POS K-map

	Inputs		Output
A	В	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1



Represent the following B	Boolean e	expressio	n by K-r	nap:	1-ardan
Represent the following E $Y(A, B, C, D) = (A - C, D)$	+B+C	(A + C)	+ D) —	<i>-</i> γ(υ'`	to the
I(A, B, C, D) = (A + B + C)	+DD	A + C +	D + DD	)	
$=(A+B+\overline{C}$	+D)(A -	+B+C	$(+\overline{D})(A)$	+B+C	$(+\overline{D})$
AB C	1) CXT	0(	E+D	[0]	C+D
A+B 00			0	O	
A+B 01					
A+611		0			
A+B 10		0			
Y(A,B,C,D) = (A +	c+ 1	5) (	A+	$B+\overline{c}$	)

Wring 12-Map

Minimize the following expression in the POS form

$$F(A,B,C,D) = (\overline{A} + \overline{B} + C + D)(\overline{A} + \overline{B} + \overline{C} + D)$$

$$(\overline{A} + \overline{B} + \overline{C} + \overline{D})(\overline{A} + B + C + D)$$

$$(A + \overline{B} + \overline{C} + D)(A + \overline{B} + \overline{C} + \overline{D})$$

$$(A + B + C + D)(\overline{A} + \overline{B} + C + \overline{D})$$

$(A + B + C + D)(\overline{A} + \overline{B} + C + \overline{D})$	\C)			
	AB \ 0	100	()	10
1101	00 0			
	0 /		10	0
	11	) 0	0	0
	10 0			
F(A,B,C,D) = (B+C	+ D) (B	42)	( <del>A</del> -	+B)

#### **Don't-Care Conditions**

- Some logic circuits can be designed so that there are certain input conditions for which there are no specified output levels, usually because these input conditions will never occur.
- There will be certain combinations of input levels where we "don't care" whether the output is HIGH or LOW.

• A circuit designer is free to make the output for any don't-care condition either a 0 or a 1 to produce the simplest

output expression. В C AB  $\overline{AB}$ 0 AΒ ĀΒ Х 0 "don't AΒ AB z = Acare" AB $\overline{AB}$ 0

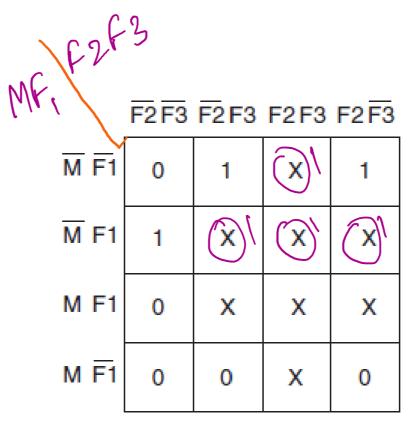
pos-Replace x'by

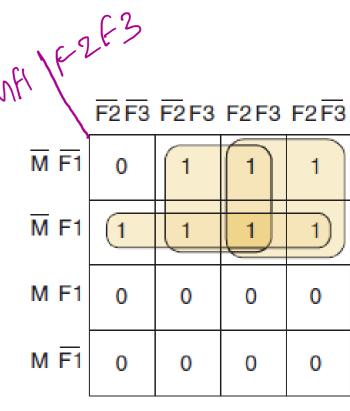
### **Example for Don't-Care Conditions**

Design a logic circuit that controls an elevator door in a three-storey building. The circuit in Figure has four inputs. M is a logic signal that indicates when the elevator is moving (M = 1) or stopped (M = 0). F1, F2, and F3 are floor indicator signals that are normally LOW, and they go HIGH only when the elevator is positioned at the level of that particular floor. For example, when the elevator is lined up level with the second floor, F2 = 1 and F1 = F3 = 0. The circuit output is the *OPEN* signal, which is normally LOW and will go HIGH when the

OPEN

<b>1</b>				
M	F1	F2	F3	OPEN
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	X
0	1	0	0	1
0	1	0	1	X
0	1	1	0	X
0	1	1	1	X
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	X
1	1	0	0	0
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X





$$OPEN = \overline{M} (F1 + F2 + F3)$$

## K-Map

#### **Advantages:**

- K mapping is a more orderly process with well-defined steps compared with the trial-and-error process sometimes
  used in algebraic simplification.
- K mapping usually requires fewer steps, especially for expressions containing many terms, and it always produces a minimum expression.

#### **Limitations:**

- K-maps are not suitable when the number of variables involved exceed four.
- It may be used with difficulty up to five and six variable systems. But, beyond 'six variables' K-maps cannot be physically visualized.
- K-map simplification is a manual technique and simplification process is heavily dependent on the abilities of the designer. It cannot be programmed.

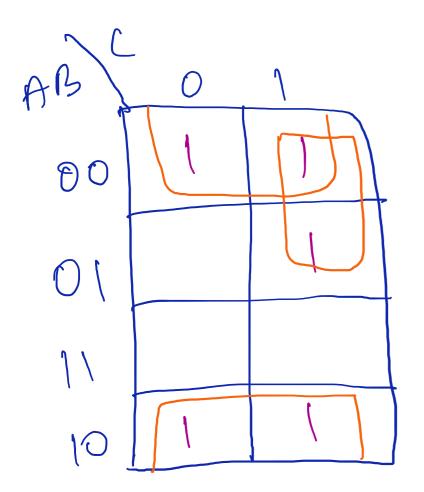
Map the following expression on a K-Map. F=A+ABZ AB They may take values

as no 01.10 11 as 00,01,10,11 tor A possible combinations tor which F can be 1 (0) / Il term AB -> C can he wither possible combinations: 100 00 101

Determine the product terms too the K-Map in fig & write the resulting minimum SOP f = ABC+BC+AB

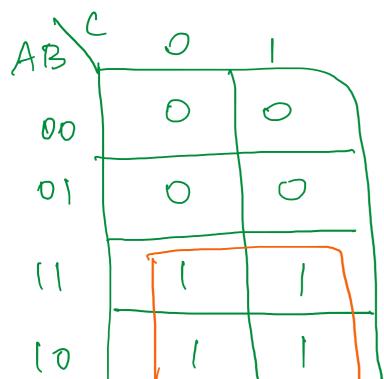
Determine the product terms for the K-Map in fig & Write the resulting minimum sop f= ABC+ABC+ABC+ABC Minimum SOP Lapression f=B+AC+AC

When a K-Map to minimize the following soperappression.  $F = ABC + \overline{ABC} + \overline{ABC$ 



f = 13 + AC

Dobtain the simplified Beapression from the truth table in the SOP form.



f = A

the standard SOP lapression (2) Ohtain and Simplified SOP expression from the K-Map-F= AB+AC+BC (a) f = Ā + BC

Simplify the logic function F in the following a)  $F(A, B, c) = \sum m(1/3, 4/7)$ 

F=ABC+BC+AC

 $f(A, B, C) = \Sigma m (0, 1, 3, 5, 7)$  minimize this by K map.

Ans 
$$f(A,B,C) = C + \overline{AB}$$