CSE1003-DIGITAL LOGIC DESIGN

Digital Assignment-1

SNo	REGISTER NO	NAME	DA1 set No
1	20BCE2762	SANGAM RAI	A
2	20BCE2765	VIBHRAT VIBHU BASNET	B
3	20BCE2767	ANJAN KUMAR SAH	C
4	20BCE2773	YASH MISHRA	D
5	20BCE2775	PRINCE PANJIYAR	E
6	20BCE2781	KARMA SANGPO GURUNG	F
7	20BCE2782	RIYESH DUWAL SHRESTHA	G
8	20BCE2881	SAURAV SAH	H
9	20BCE2882	JEEWAN GHIMIRE	I
10	20BCE2883	ELINA PARAJULI	J
11	20BCE2884	SNEHA CHAUDHARY	K
12	20BCE2885	SUMIT KUMAR MANDAL	L
13	20BCE2886	NAMAN AGRAHARI	M
14	20BCE2887	SUNIL KUSHWAHA	N
15	20BCE2888	MUDIT BHATTA	O
16	20BCE2891	ADITYA KUNWAR	P
17	20BCE2892	MD.ANWAR MANSURI	Q
18	20BCE2893	ANISH SHRESTHA	R
19	20BCE2894	ASHUTOSH BASHYAL	S
20	20BCE2895	ROHIT KUMAR GUPTA	T
21	20BCE2896	PRAMIT KARKI	A
22	20BCE2897	PRATIK LUITEL	B
23	20BCE2898	SANDESH KHATIWADA	C
24	20BCE2899	SHREYA KARKI	D
25	20BCE2900	PAWAN THAKUR	E
26	20BCE2901	PRAJWAL LAMSAL	F
27	20BCE2902	BINIT BHATTARAI	G
28	20BCE2903	AAYUSH MANDAL	H
29	20BCE2904	BIJAN SHRESTHA	I
30	20BCE2905	ABHAY RATHI	J
31	20BCE2906	ASHWIN POUDEL	K
32	20BCE2907	ANURAG KARKI	L
33	20BCE2908	MUSKAN SAH	M
34	20BCE2909	KRISHNA KUMAR RAUT	N
35	20BCE2911	PRARTHANA SHIWAKOTI	O
36	20BCE2913	SARTHAK GIRI	P
37	20BCE2914	BISHNU ROUNIYAR	Q
38	20BCE2915	GAURAB KUMAR RAUNIYAR	R
39	20BCE2916	AMAN SINGH	S
40	20BCE2917	YASHWANT BHARDWAJ	T

41	20BCE2918	AVIRAL SHARMA	A
42	20BCE2919	SUDARSHAN BHATTA	B
43	20BCE2920	DIWESH CHAURASIA	C
44	20BCE2921	PRITHAK GAJUREL	D
45	20BCE2922	SARJAK DEVKOTA	E
46	20BCE2923	BISURAJ SHARMA	F
47	20BCE2924	JAYESH PERIWAL	G
48	20BCE2925	LIJAH BABU GONGAL	H
49	20BCE2926	GAUTAM KUMAR MAHATO	I
50	20BCE2927	ADITYA KUMAR SINGH	J
51	20BCE2928	VIVAN SHRESTHA	K
52	20BCE2929	PRIYANSHU KOIRALA	L
53	20BCE2930	AANAND RIMAL	M
54	20BCE2931	PRASHAMAN POKHAREL	N
55	20BCE2932	SAKSHI AGRAWAL	O
56	20BCE2933	KARMA GURUNG	P
57	20BCE2934	ANUJ MISHRA	Q
58	20BCE2935	SHAILAJ GAUTAM	R
59	20BCE2936	SIDDHANT KARKI	S
60	20BCI0328	ANMOL GURAGAIN	T
61	20BCI0329	ABNISHA PAUDEL	A
62	20BCI0330	SHREEMA GAUTAM	B
63	20BCI0331	MD TANUWAR ANJUM	C
64	20BDS0405	BIMAL PARAJULI	D
65	20BDS0406	AADITYA BHETUWAL	E

Set - A

1. CONVERT THE FOLLOWING

i. 101010110.10011 = _____$_{9, ____16,H}$

ii. 726.5_8 = _____$_{4, 2, H}$

iii. 67AD.EF = _____$_{2,8,7}$

2. PERFORM THE FOLLOWING

i. 1001101 – 1110011 using 1's complement subtraction

ii. 1100011 – 10110011 using 2's complement subtraction

iii. 93 – 65 using both 1's and 2's complement

iv. 57 - 99 using both 1's and 2's complement

3. Simplify the following using Boolean expression

i. $(A+C)(AD+A\overline{D})+AC+C$

ii. $\overline{W}\,\overline{X}+\overline{X}\,\overline{Y}+YZ+\overline{W}\,\overline{Z}$

iii. $\bar{a}b+\bar{b}c+\bar{c}a=a\bar{b}+b\bar{c}+c\bar{a}$

4. find the SOP for the following using K –Map

i. f(a,b,c,d) = $\sum(0,2,3,4,7,8,14)$

ii. f = $\prod(0,2,4,6,8)\cdot D(1,12,9,15)$

iii $x'z+w'xy'+w(x'y+xy')$

5. A half adder is a circuit that adds two bits to give a sum and a carry. Give the truth table for a half adder, and design the circuit using only two gates. Then design a circuit which will find the 2's complement of a 4-bit binary number. Use four half adders and any additional gates.

6. Design a Code converter to convert BCD to $84\bar{2}\bar{1}$ code.

7. Draw a state diagram for a Moore type state machine specified as follows:

- Denote "a" the initial state of the machine
- set the initial output to the initial input (the input is presented to the machine bit by bit)
- The output changes value only when three successive inputs have the same value and that value is opposite to the current output. For example, if the current output is 1 and the machine detects three consecutive 0 it changes the output to 0.

design the circuit using RS – FF and write the verilog HDL.

8. Design the 4 bit 7311 code to 53-1-1 code and write the Verilog HDL using case statement.

SET – B

1. CONVERT THE FOLLOWING

i. 101011110.11101 = _____$_{9,\ ___16,H}$

ii. 467.23_8 = _____$_{4,\ 2,\ H}$

iii. C49D.B7 = _____$_{2,8,7}$

2. PERFORM THE FOLLOWING

i. 1010101 – 1010011 using 1's complement subtraction

ii. 1110001 – 10010111 using 2's complement subtraction

iii. 87 – 55 using both 1's and 2's complement

iv. 23 - 91 using both 1's and 2's complement

3. Simplify the following using Boolean expression

$i.[x(xy)'][y(xy)']$

$ii.\overline{(a\bar{b}+\bar{c}d+e\bar{f})}$

$iii.(\bar{a}+c)(\bar{a}+\bar{c})(a+b+\bar{c}d)tofourliterals$

4. find the SOP for the following using K – map

i. $A'B'C'D'+BC'D+A'C'D+A'BC+AD'$

ii. f = $\prod(1,3,5,9,11,12,14)$

iii. f = $\sum(0,1,2,5,7,8,10,15)$

5. A flow rate sensing device used on a liquid transport pipeline functions as follows. The device provides a 5-bit output where all five bits are zero if the flow rate is less than 10 gallons per minute. The first bit is 1 if the flow rate is at least 10 gallons per minute; the first and second bits are 1 if the flow rate is at least 20 gallons per minute; the first, second, and third bits are 1 if the flow rate is at least 30 gallons per minute; and so on.The five bits, represented by the logical variables *A*, *B*, *C*, *D*, and *E*, are used as inputs to a device that provides two outputs *Y* and *Z*.

(a) Write an equation for the output *Y* if we want *Y* to be 1 iff the flow rate is less than 30 gallons per minute.

(b) Write an equation for the output *Z* if we want *Z* to be 1 iff the flow rate is at least 20 gallons per minute but less than 50 gallons per minute.

6. Design a code converter to convert 84-1-2 to 5311 code.

7. Design a finite state machine (FSM) for a counter that counts through the 3-bit prime numbers downwards. Assume the counter starts with initial prime value set to 010 as its first 3 bit prime number. You need to provide the state transition table and the state transition diagram. Assume that the state is stored in three D-FFs. Write the HDL code and simulate Hint: The set of all 3-bit prime numbers includes 2, 3, 5 and7.

8. Gray codes have the useful property that consecutive numbers differ in only a single bit osition. Design a 3-bit Gray code counter FSM with no inputs and three outputs. When reset, the output should be 000. On each clock edge, the output should advance to the next Gray code. After reaching 100, it should repeat with 000. Draw a schematic for this counter using T flip-flops.

SET – C

1. Perform the following conversions

   (i) $(67.24)_8 = (\ ?\ )_2$

   (ii) $(11100.1001)_2 = (\ ?\ )_{16}$

   (iii) $(BC1.30)_{16} = (\ ?\ )_2$

   (iv) $(10111.0111)_2 = (\ ?\ )_8$

2. Perform the following

   (i) 1001100-110011 using 1's complement subtraction

   (ii) 93 – 14 using 1's complement

   (iii) 87 – 6 using 2's complement

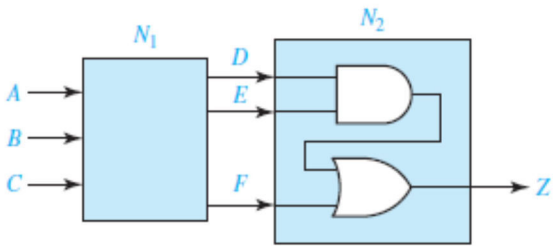
3. Simplify the following using Boolean expression

   i. $a'bcd + a'bc'd + b'ef + cde'g + a'def + a'b'ef$ (reduced to sum of 3 terms)

   ii. $(x + y)(y + z)(x + z) = (x'+y')(y'+z')(x'+z')$ (give the algebraic proof)

   iii. $F = \prod(3,5,8,11)$

4. A combinational circuit is divided into two subcircuits $N1$ and $N2$ as shown. The truth table for $N1$ is given. Assume that the input combinations $ABC = 110$ and $ABC = 010$ never occur. Change as many of the values of D, E, and F to don't-cares as you can without changing the value of the output Z.



A	B	C	D	E	F
0	0	0	1	1	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	1	0	0	0

5. Find the minimum product of sums and sum of Product for
   (a) $F(a, b, c, d, e) = \sum m(1, 2, 3, 4, 5, 6, 25, 26, 27, 28, 29, 30, 31)$

   (b) $F = M(1,4,5,8,10,13)$

6. Design a home security system as follows. There are 3 input sensors called, e (enable), w (window) and d (door). There is one output called s (alarm sound). After reset the system is disarmed. The system stays in the disarmed state until e is pressed, when it will move to the armed state. In this state, if e is pressed again the system will move back to the disarmed state. If however, w or d sensors are sensed while the system is in the armed state, the system will activate the alarm sound as follows. Signal s will be turned on for 500 clock cycles then it will shut down for 300 clock cycles. This sequence will repeat itself until e becomes 1, in which case the system returns to the disarmed state. Derive the data-path elements and the FSM in the control-path. Write/simulate the Verilog code to verify the entire design.

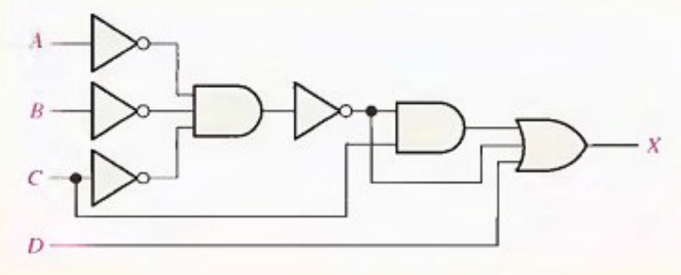
7. An up-down mod-4 binary counter has a single input x, such that the it counts up if x=0 and counts down if x=1:
   * Draw the Mealy state diagram of the circuit.
   * Draw the state Moore diagram of the circuit.
   * Implement both circuits using *negative-edge triggered* D-FFs.

SET – D

1. Convert the following
   i. $(10111.0111)_2 = (\ ?\ )_8$
   ii. $(67.67)_8 = (\ ?\ )_{10}$
   iii. $(10110.0101)_2 = (\ ?\ )_4$
   iv. $(155)_{10} = (\ ?\ )_2$
2. Perform the following
   i. 1100011 – 1011011 using 1's and 2's complement subtraction
   ii. 98 – 24 using 1's complement
   iii. 14 – 86 using 2's complement
3. Simplify the following using Boolean expression
   i. $\bar{A}B(\bar{D} + \bar{C}D) + B(A + \bar{A}CD)$ to one literal
   ii. ABCD + A'B'C'D + A'BCD + AB'CD + A'B'CD + ABCD'
   iii. F = ∏(2,4,5,7,8,10) , write the SOP
4. Simplify using K – Map
   i. f = ∑(0,6,8,13,14)+d(2,4,10)
   ii. (A'+B+D')(A'+B'+C')(A'+B'+C)(B'+C+D')
   iii. $F(v, w, x, y, z) = \sum m(4, 5, 8, 9, 12, 13, 18, 20, 21, 22, 25, 28, 30, 31)$
5. A combinational circuit has four inputs (A, B, C, D) and four outputs (W, X, Y, Z). $WXYZ$ represents an excess-3 coded number whose value equals the number of 1's at the input. For example, if $ABCD$ = 1101, $WXYZ$ = 0110.
   (a) Find the minterm expansions for X, Y, and Z.
   (b) Find the maxterm expansions for Y and Z.
6. Design a code converter to convert Excess – 1 Code to 8421 code.
7. Design a sequential circuit using RS - FFthat has 1 data input (w) and 1 data output (z). The output z will become 1 if in the last 3 clock cycles the number of 1s on the input w has been greater than 1. Draw the FSM diagram and write/simulate the Verilog code to verify it.
8. Design the 4 bit 2421 code to 53-1-1 code and write the Verilog HDL using case statement.

SET – E

1. Convert the following
   i. 111111101_2 = _____4,10, H
   ii. 8AF2.E9 = _____2, 8, 10
2. Perform the following
   i. 11110011 – 1110011 using 1's and 2's complement subtraction
   ii. 88 – 43 using 1's complement
   iii. 35 – 95 using 2's complement
3. Reduce the combinational logic circuit in Fig. to a minimum form.



4. Simplify the following using Boolean algebra
   i. f=m(1,2,4,7,10,12)
   ii. f = M(0,3,4,8,9,12)
5. Identify each of the following expression as SOP, POS and its canonical form respectively
   i. $AB + \overline{A}BD + \overline{A}C\overline{D}$
   ii. A 'B' + AB' + C' D' + CD'
6. Evaluate the following expression
   a. $\overline{(P+Q)R\overline{S}+T+\overline{U}}$
   b. Simplify using K – map and give the SOP and POS
      F = π(0,1,3,5,6,9,10,13,14)
7. Design an excess-3 code converter to drive a seven-segment indicator. The four inputs (*A*, *B*, *C*, *D*) to the converter circuit represent an excess-3 digit. Input combinations representing the numbers 0 through 9 should be displayed as decimal digits. The input combinations 0000, 0001, and 0010 should be interpreted as an error, and an "E" should be displayed. Assume that the input combinations 1101, 1110, and 1111 will never occur. Design your circuit using only two-, three-, and four input NOR gates and inverters. Any solution with 18 or fewer gates and inverters (not counting the four inverters for the inputs) is acceptable.

Use 6 (not 6) for 6. Use 9 (not 9) for 9.

8. Given the enclosed source code, draw the equivalent hardware circuit.

```
module setr(input logic clock,
output logic[7:0] f);
logic[7:0] a, b, c;
always_ff @(posedge clock)
begin
a <= b + c;
b = c + a;
```

```
c = a + b;
end
assign f = c;
endmodule
```

9. Draw the Moore state diagram and state table for a serial even parity checker. The circuit receives a word of 4-bits serially on its single input X and produces the even parity bit after the fourth bit is received. The single output Z remains 0 except when the final (fourth) bit is received and the total number of 1's in the word is odd. The machine returns to the reset initial state after the 4th input bit. Design the circuit using RS – FF and write the code using gate level and dataflow.

SET – F

1. Convert the following:
   a. 10101001.11011_2 = _____3, _____8, _____16
   b. 111011011_G = _____B
   c. A25FE.DC8 = _____10,_____7,_____2
2. Subtraction using 1's and 2's complement
   a. 673 – 76
   b. 87 – 534
3. Simplify the following using Boolean law with minimum literals and implement using Universal gates
   a. $Y = A + \overline{A}B + \overline{(A+B)}C + \overline{(A+B+C)}D$
   b. prove that $\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}\overline{C} = \overline{A} + \overline{B+C}$
4. Simplify the following Using K –map,
   a. F = ∑(0,2,3,6,7)+d(8,12,15)
   b. F = ∑(0,2, 8,10,14,16,18,19,24)+d(4,11,15,23,27,28)
5. Design a circuit which can convert BCD to 2421 code.
6. In an application 4 inputs A, B, C, D are available in true and complement Form .These are fed at a logic circuit which operates a relay. The relay is ON for ABCD = 0000, 0010, 0101, 0110, 1101 and 1110. The states 1000 and 1001 don't occur. For remaining states the relay is OFF.
   i. prepare truth table and minimize outputs F using K map
   ii. Realize F using 3 input NAND gates.
7. Show that $A \otimes B \otimes C \otimes D = \sum(0,3,5,6,9,10,12,15)$
8. Given the enclosed source code, draw the equivalent hardware circuit.

```
module setq(input logic clock,
output logic[7:0] f);
logic[7:0] a, b, c;
always_ff @(posedge clock)
begin
a = b + c;
b <= c + a;
c = a + b;
end
assign f = c;
endmodule
```

9. Draw a state diagram for a mealy type state machine specified as follows:

- Denote "a" the initial state of the machine
- set the initial output to the initial input (the input is presented to the machine bit by bit)
- The output changes value only when three successive inputs have the same value and that value is opposite to the current output. For example, if the current output is 1 and the machine detects three consecutive 0 it changes the output to 0.

design the circuit using T – FF and write the verilog HDL.

SET – G

1. Convert the following
   a. 11110010.111001_2 = _____$_{8,5,H}$
   b. 3213_4 = _____$_{2,10,8}$
   c. 34D.EFF = _____$_{4,2,O}$

2. Prove that:
   a. $A \otimes B \otimes AB = A + B$
   b. [(A+B)' + (C+D)']' = (A+B)(C+D)

3. Design a Code converter to convert 4241 to excess 2 code using only NOR gates.
4. Do the following subtractions: (a) 1100 - 1001; (b) 101101 – 11010 using 1's complement and 2's complement.
5. Simplify logic function using k – map minimization technique

   Y(A , B , C, D) = ∑ m (0, 1, 3, 7, 8, 9,11,15)

   b. Simplify the Boolean expression using four variables:

   w' z + x z + x' y + w x' z

6. Use algebraic techniques to determine whether or not the following Boolean equation is valid:

$$(abd + \bar{a}b + \bar{b}d + \bar{c})(c + ab + bd) = b(a + c)(\bar{a} + \bar{c}) + d(b + c)$$

7. I want to schedule a meeting among 6 individuals Alice, Brian, Charles, David, Elise and Frank. The meeting must be scheduled so that the following rules are satisfied: • Exactly one of Alice and Brian must be in the meeting. • Charles and David must be present in the meeting together. If Charles is not available, David and Frank must be in the meeting together. However, all three of Charles, David and Frank must not be present. • Elise is the manager of the group, so she must be present in the meeting. Each of the 6 team members indicates to me their availability for the meeting. I would like to construct a logic netlist with a single output g, such that g is equal to ′1 ′ whenever the meeting can be scheduled. (a) List the Boolean variables (b) Write down what both values of each variable indicate. (c) Draw the circuit using logic gates. (d) implement the same using only NOR gates

8. Given the enclosed source code, draw the equivalent hardware circuit.

```
module setp(input logic c1, c2, c3, a, b,
output logic f, g);
always_latch
begin
if (c1) begin
f = a;
g = b;
end else if (c2) begin
f = b;
end else if (c3) begin
g = a;
end
end
endmodule
```

9. Design a 1-bit decrementer (a circuit which subtracts 1). Give

(a) the arithmetic relationship between input and out put signals

(b) the truth table,
(c) logic diagram.
Design a logic diagram of a 1-bit increment/decrement circuit controled by an id signal (increment when id = 1, decrement otherwise). Write the HDL.
And Design a block diagram of a 4-bit increment/decrement circuit. Use the above HDL and concatenate.

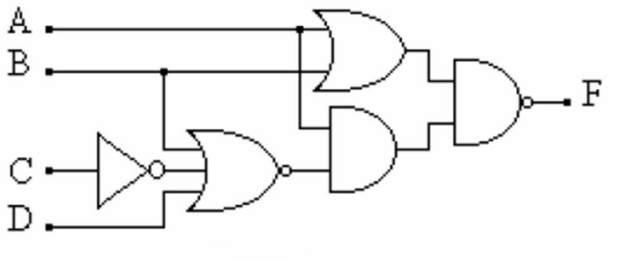
SET – H

1. Design a circuit that compares two binary numbers X and Y, each having two bits (X=x2x1; Y=y2y1). It has a single output c which is supposed to be 1 when X > Y, and 0 otherwise. Do not use adders/subtractors for this design; instead use a fundamental design process. Draw the minimum sum-of-products circuit using the correct circuit symbols for all gates. Assume complemented inputs are NOT available, but multiple input gates are. What is the delay of this circuit, assuming the delay for each gate is d?
2. Consider a function f on three variables a, b and c. Suppose f is completely specified, and written as

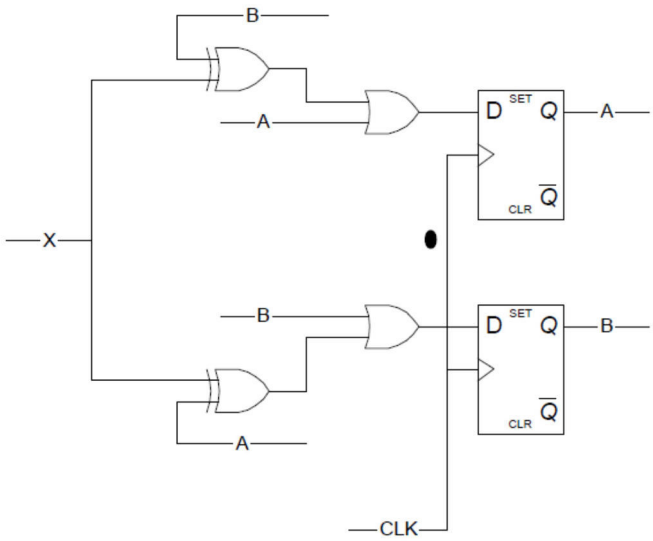
$$f = \bar{a}\bar{b}\bar{c} + \bar{a}\bar{b}c + \bar{a}b\bar{c} + a\bar{b}c + ab\bar{c} + abc$$

(a) Is the above expression a canonical SOP? If so, state why. If not, state why not.
(b) Construct a K-map for f
(c) Write down the prime implicants of f
(d) Write down a minimum SOP expression for f.
(e) If the input combination abc was a don't care, then what write down the new prime implicants of f. Also, write down a minimum SOP expression for f. What is the benefit of using this minimum SOP for f over the one from part d)?

3. Convert the following
   a. 12367.123_{10} = _____$_{2,5,16}$
   b. 11101001.101 = _____$_{o,H,9}$
   c. 654.12_8 = _____$_{2,H}$
4. Using 1's complement and 2's complement do the following i.(-12-65), ii. 97 – 143
5. Consider the following circuit:



   a. Give the algebraic expression of the function
   b. Simplify the algebraic expression
   c. Draw using only NAND gates
6. Find a minimum POS for the following
   i. F(a,b,c,d,e) = m (4,5,8,9,12,13,18,20,21,22,25,28,30,31)
   ii. F = M(9,10,4,7,2,8,13).d(0,2,15)
7. Design a code converter to convert 5311 to 24-2-1 code.
8. Design a serial subtractor with accumulator for 5-bit binary numbers. Assume that negative numbers are represented by 2's complement. Use a circuit of the form of Figure 18-1, except implement a serial subtractor using a D-CE flip-flop and any kind of gates. Give the state graph for the control circuit. Assume that *St* will remain 1 until the subtraction is complete, and the circuit will not reset until *St* returns to 0.write the HDL using behavioural level.
9. Derive the state table and state diagram of the synchronous sequential circuit shown (X is an input to the circuit). Explain the circuit function.


B
A
X
B
A
D
SET
Q
A
CLR
Q
D
SET
Q
B
CLR
Q
CLK

SET – I

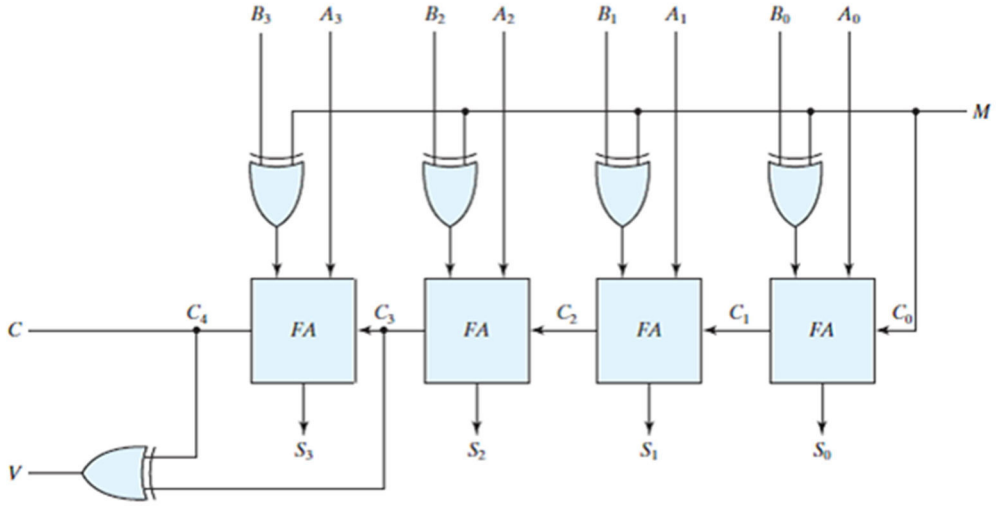
1. Find the complements for the following numbers:
   a. $(100111.1100)_2 =$ _____$_{8,9,H}$
   b. $(751.33)_8 =$ _____$_{4,9,2}$
   c. $(52,784,630)_{10} =$ _____$_{2,8,H}$
2. Simplify each of the following expressions:
   $$\overline{A}BCD + \overline{A}B\overline{C}D + \overline{B}EF + CD\overline{E}G + \overline{A}DEF + \overline{A}\overline{B}EF$$
   (reduce to a sum of three terms). Draw using only a. NAND gates, b. NOR gates
3. a. Perform the subtraction 64 – 31 and 99 – 7 in 1's and 2's complement method.
   b. Simplify the following expression to a sum of two terms and then factor the result to obtain a product of sums:
   $$ab\overline{d}\,\overline{f} + \overline{b}ceg\overline{h} + ab\overline{d}f + ac\overline{d}e + \overline{b}ce$$
4. Each of three coins has two sides, heads and tails. Represent the heads or tails status of each coin by a logical variable (*A* for the first coin, *B* for the second coin, and *C* for the third) where the logical variable is 1 for heads and 0 for tails. Write a logic function *F*(*A*, *B*, *C*) which is 1 iff exactly one of the coins is heads after a toss of the coins. Express *F*
   a. as a minterm expansion.
   b. as a maxterm expansion.

   Draw the circuit using only NOR gate.
5. Find the minimum minterms using K – map
   $F(a, b, c, d, e) = \pi M(2, 4, 5, 6, 8, 10, 12, 13, 16, 17, 18, 22, 23, 24) \bullet \pi D(0, 11, 30, 31)$
6. Design a network of NAND gates and inverters that converts from 8-4-2-1 BCD code to 6-3-1-1 code.
7. Design and write the Verilog HDL for 4 bit parallel multiplier.
8. Draw the Mealy state diagram and state table for a serial even parity checker. The circuit receives a word of 4-bits serially on its single input X and produces the even parity bit after the fourth bit is received. The single output Z remains 0 except when the final (fourth) bit is received and the total number of 1's in the word is odd. The machine returns to the reset initial state after the 4th input bit. Design the circuit using D – FF and write the code using gate level and dataflow.

SET – J

1. The adder-subtractor circuit of Fig. below has the following values for mode input M and data inputs A and B:

	M	A	B
(a)	0	0011	0101
(b)	0	1101	1101
(c)	1	0100	0011
(d)	1	0000	0001



in each case determine the values of the four SUM outputs, the carry C, and overflow V.

2. Convert the following
   a. 1110100101.11101_2 = _____$_{8,7,H}$
   b. 6531_7 = _____$_{10,2,8}$
3. Design a code converter to convert 53-1-1 to 8421
4. Perform the subtraction 52 – 73 and 111011 - 100101 using 1's and 2's complement method.
5. simplify the following using Boolean laws
   a. $AB + \overline{AC} + A\overline{B}C(AB + C)$
   b. ABCD + A'B'C'D + A'BCD + AB'CD + A'B'CD + ABCD' (Terms 4,5, and 6 are Don't Care)
6. A combinational circuit has four inputs (A, B, C, D), which represent a binary coded- decimal digit. The circuit has two groups of four outputs S, T, U, V, and W, X, Y, Z. Each group represents a BCD digit. The output digits represent a decimal number which is five times the input number. For example, if ABCD = 0111, the outputs are 0011 0101. Assume that invalid BCD digits do not occur as inputs.
   (a) Construct the truth table.
   (b) Write down the minimum expressions for the outputs by inspection of the truth table.
7. Given the enclosed source code, draw the equivalent hardware circuit. Draw also the periodic waveforms on the output signals *f* and *g*. If the reference clock is 200 MHz, then what are the frequencies of signals *f* and *g* ?

```
module setm(input logic resetn, clock,
output logic f, g);
logic[9:0] counter;
always_ff @(posedge clock or negedge resetn)
if (!resetn) begin
counter <= 10'h000;
f <= 1'b0;
g <= 1'b0;
end else begin
```

```
f <= 1'b1;
if (counter > 10'd50 && counter < 10'd250) f <= 1'b0;
g <= 1'b0;
if (counter > 10'd150 && counter < 10'd400) g <= 1'b1;
if (counter < 10'd900) counter <= counter + 10'd1;
else counter <= 10'd0;
end
endmodule
```

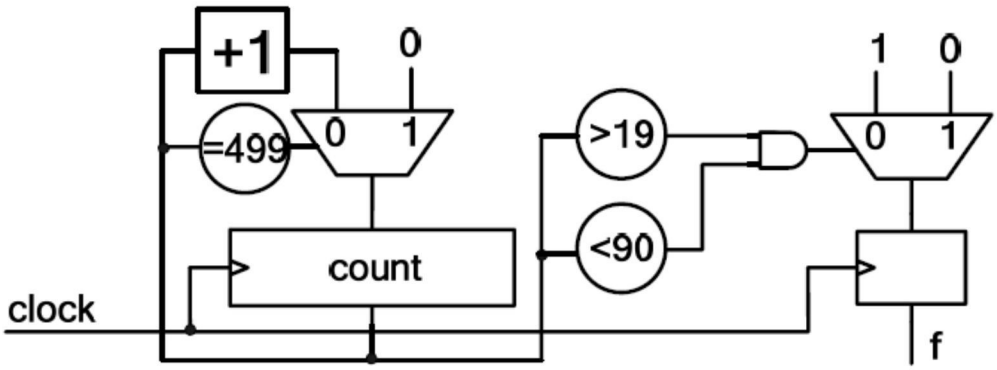
8. Design a sequential circuit using D - FF to convert excess-3 code to BCD. This circuit adds three to a binary-coded-decimal digit in the range 0 to 9.The input and output will be serial with the least significant bit first.

SET – K

1. The output of a majority circuit is 1 if a majority (more than half) of its inputs are equal to 1, and the output is 0 otherwise. Construct a truth table for a three input majority circuit and derive a simplified sum-of-products expression for its output.
2. Design a code convert to convert 8421 to 2421.
3. You are presented with a set of requirements under which an insurance policy can be issued. The applicant must be:
    a. a married female 25 years old or over , or
    b. a female under 25 , or
    c. a married male under 25 who has not been involved in a car accident , or
    d. a married male under 25 who has been involved in a car accident, or
    e. a married male 25 year or over who has not been involved in a car accident.

    Find an algebraic expression which assumes a value 1 whenever the policy is issued. Simplify the expression obtained.

4. Convert the Following
    i. 86753.12 = _____$_{2,H}$
    ii. 11110001.11 = _____$_{O,9,4}$
    iii. AED.87 = _____$_{9,2}$
5. Perform the following using 1's and 2's complement i. -21-43, ii. 76 - 111011
6. Simplify using K – map and give the SOP and POS
    F = ∏(2,30,5,4,7,19,28,21,15,0,6).d(1,11,13,18,29)
    f = (9,5,2,7,15,14,0,3)
7. Reduce the following using Boolean Algebra
    f = m(0,2,3,5,7,12,15)
    F = a'cd+ab'+ac'e+cd'+b'd'
8. Given the enclosed hardware circuit, write/simulate the equivalent Verilog code.



9. Design a sequential circuit using T - FF to convert BCD to excess-3 code. This circuit adds three to a binary-coded-decimal digit in the range 0 to 9.The input and output will be serial with the least significant bit first.

SET – L

1. Convert the following
   i. 11011010.110 = _____o,H,9
   ii. 751.33_8 = _____2,5,9
   iii. AFF.EEF = _____2,o,9
2. Perform the following using 1's and 2's complement
   i. 92 – 5
   ii. 7 – 85
3. Simplify the following using Boolean Algebra
   i. F = M(1,9,2, 5, 10,11,7,8)
   ii. $F = (A + B + \overline{C}D\overline{E}) + \overline{B}C\overline{D}$
   iii. F = (BC'+A'D)(AB'+CD')
4. Simplify using K – Map and give the SOP and POS
   i. F = m(7,13,5,30,17,5,27,8,14,19)+d(0,11,12,15,21)
   ii. Y = $\overline{C}(\overline{A}B\overline{D} + D) + A\overline{B}C + \overline{D}$
   iii. Determine the minimum expression for each K map given below

	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	1	1	1	1
$\overline{A}B$	1	1	0	0
AB	0	0	0	1
$A\overline{B}$	0	0	1	1

(a)

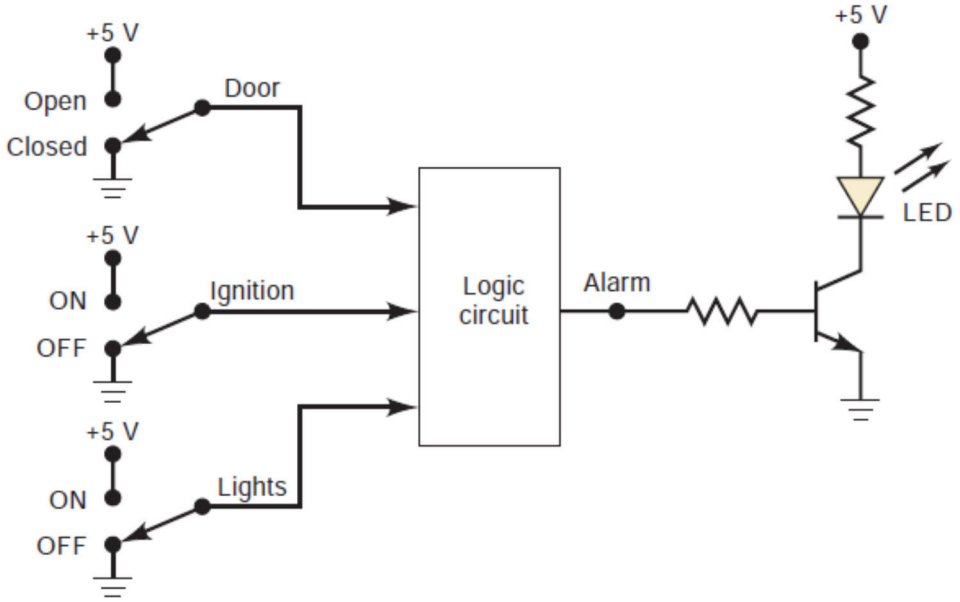
	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	1	0	1	1
$\overline{A}B$	1	0	0	1
AB	0	0	0	0
$A\overline{B}$	1	0	1	1

(b)

	$\overline{C}$	C
$\overline{A}\overline{B}$	1	1
$\overline{A}B$	0	0
AB	1	0
$A\overline{B}$	1	X

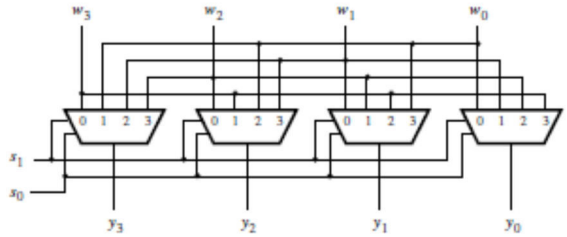
(c)

5. Fig. below shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used to indicate the status of the door by the driver's seat, the ignition, and the headlights, respectively. Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following conditions exists:

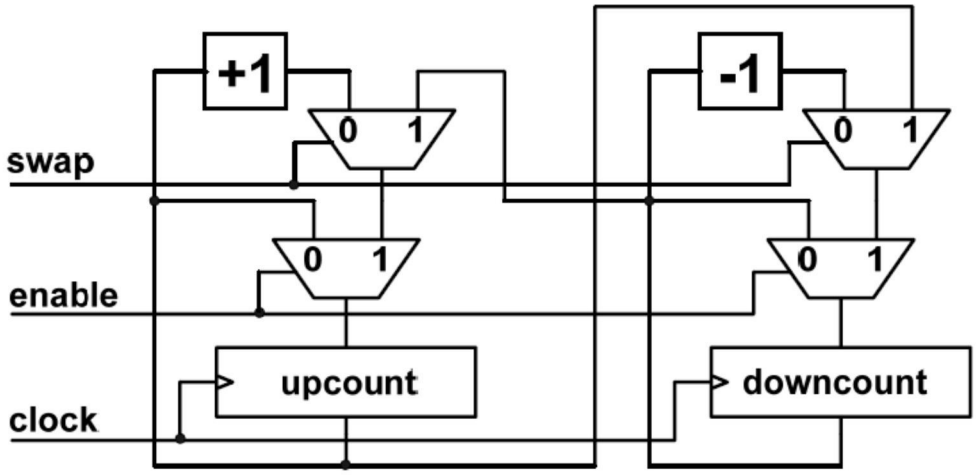


   i. The headlights are on while the ignition is off.
   ii. The door is open while the ignition is on.
6. Design a Code converter to convert 53-1-1 to excess 1 code.

7. Write the Verilog code using if else condition and truth table for the circuit given below.

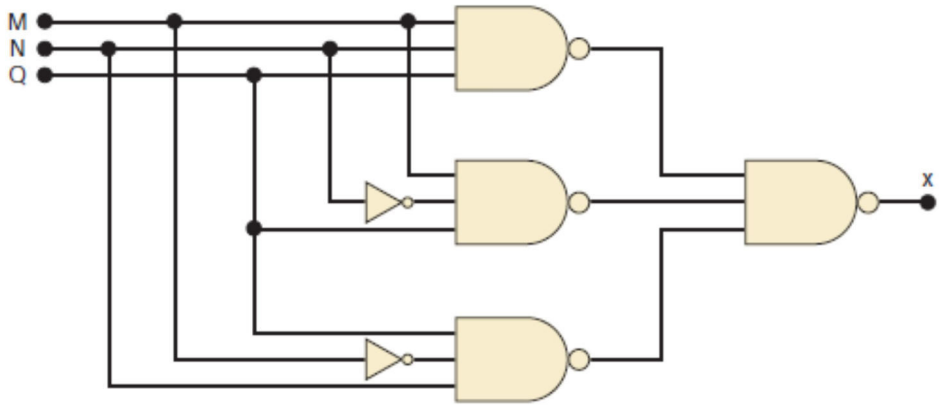


8. Given the enclosed hardware circuit, write/simulate the equivalent Verilog code.



SET - M

1. Convert the following
   i. 789.26 = _____$_{2,H,7}$
   ii. 1111111011.1101111 = _____$_{O,H}$
   iii. 8EA.59 = _____$_{O,9}$
2. Perform the following using 1's and 2's complement
   i. 11101101 – 10010
   ii. 87 – 34
3. Simplify the Following using Boolean Algebra
   i. $(w+x+\overline{y}+z)(w+x+\overline{y}+\overline{z})(w+\overline{x}+\overline{y}+z)(w+\overline{x}+\overline{y}+\overline{z})(\overline{w}+\overline{x}+\overline{y}+z)(\overline{w}+\overline{x}+\overline{y}+\overline{z})$
   ii. $Q=\overline{RST}(\overline{R+S+T})$
   iii. Change each gate into NOR gate and simplify the Boolean algebra



4. Simplify the following using K – map to SOP and POS
   i. f = M(0,3,5,6,8,10)+d(11,13,14)
   ii. $F(A,B,C,D)=A+B+\overline{D}$
   iii. F = ∑(21,7,30,2,8,15,19,3) + d(0,18,15,6)
5. Design a Code Converter to convert 2421 code to 24-2-1 code
6. A manufacturing plant needs to have a horn sound to signal quitting time. The horn should be activated when either of the following conditions is met:
   i. It's after 5 o'clock and all machines are shut down.
   ii. It's Friday, the production run for the day is complete, and all machines are shut down.

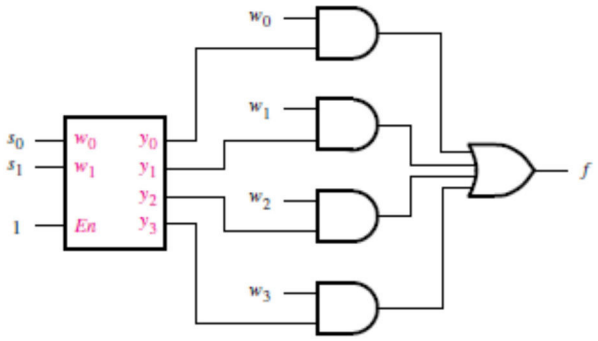
   Design a logic circuit that will control the horn. (Hint: Use four logic input variables to represent the various conditions; for example, input A will be HIGH only when the time of day is 5 o'clock or later.)

7. For the given code give the hardware equivalent circuit and convert the code using case statement.

```
module setj(input logic resetn, clock,
input logic start, stop,
input logic load, serial_in,
input logic [7:0] parallel_in,
output logic parity);
logic shift_left;
logic[7:0] shift_register;
always_ff @(posedge clock or negedge resetn)
begin
if (!resetn) begin
shift_left <= 1'b0;
shift_register <= 8'd0;
```

```
end else begin
if (start) shift_left <= 1'b1;
if (stop) shift_left <= 1'b0;
if (shift_left) shift_register <= {shift_register[6:0],serial_in};
else if (load) shift_register <= parallel_in;
end
end
always_comb begin
parity = ^shift_register;
end
endmodule
```

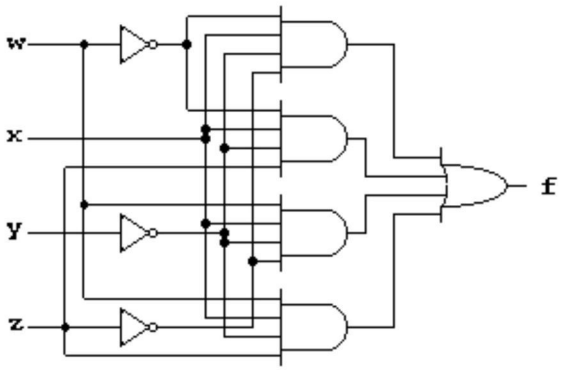
8. Write Verilog code that represents the circuit in Figure below. Use the *dec2to4* module as a subcircuit in your code using case statement.



SET – N

1. A computer interface to a line printer has seven data lines that control the movement of the paper and the print head and determine which character to print. The data lines are labeled *A*, *B*, *C*, *D*, *E*, *F*, and *G*, and each represents a binary 0 or 1. When the data lines are interpreted as a 7-bit binary number with line *A* being the most significant bit, the data lines can represent the numbers 0 to 12710. The number 1310 is the command to return the print head to the beginning of a line, the number 1010 means to advance the paper by one line, and the numbers 3210 to 12710 represent printing characters.
   (a) Write an equation for the variable *X* which is 1 iff the data lines indicate a command to return the print head to the beginning of the line.
   (b) Write an equation for the variable *Y* which is 1 iff there is an advance paper command on the data lines.
   (c) Write an equation for the variable *Z* which is 1 iff the data lines indicate a printable character. (*Hint:* Consider the binary representations of the numbers 0–31 and 32–127 and write the equation for *Z* with only two terms.)

2. Design a Code converter to convert 5311 code to gray code
3. Simplify the following using Boolean algebra
   i. $Y = \overline{(C+D)}\overline{A}C\overline{D} + A\overline{B}\overline{C} + \overline{A}\overline{B}CD + AC\overline{D}$
   ii.



   iii. F = m(3,7,8,10,12,13)
4. Simplify the following using K – Map
   i. f = m(31,0,4,6,19,25,17,7,2) + d(1,14,15,21,22)
   ii. F = $f = ab(\overline{\overline{cd}}) + \overline{a}bd + \overline{\overline{b}}\overline{\overline{c}}d$
5. Perform the Following
   i. Determine the value of the base x, $(225)_x = (341)_8$
   ii. $A9CF.B61_{16}$ = _____$_{8,9,2}$`
   iii. 1110000011.1001 = _____$_{6,9,H}$
   iv. 100100 – 1111111 and 98 – 43 using 1's and 2's complement
6. A bank vault has three locks with a different key for each lock. Each key is owned by a different person. To open the door, at least two people must insert their keys into the assigned locks. The signal lines A, B, and C are 1 if there is a key inserted into lock 1, 2, or 3, respectively. Write an equation for the variable Z which is 1 iff the door should open.
7. For the given code give the hardware equivalent circuit and convert the code using case statement

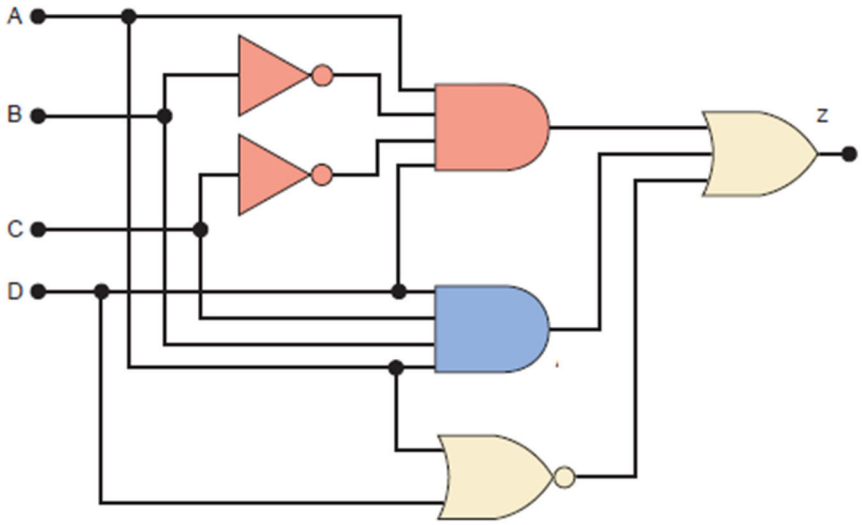
```
module problem(input logic resetn, clock,
input logic x, y, z, c1, c2,
output logic f, g);
always_ff @(posedge clock or negedge resetn)
begin
```

```
if (!resetn) begin
f <= 1'b0;
end else begin
f <= x;
if (c1) f <= y;
if (c2) f <= z;
end
end
always_comb begin
if (c2) g = z;
else if (c1) g = y;
else g = x;
end
endmodule
```

8. Design a 4 bit serial adder with accumulator and write the Verilog HDL code.

SET – O

1. Convert the following
   i. 875.18 = _____$_{8,h,2}$
   ii. 10000110.00101 = _____$_{4,9,H}$
   iii. FFEE.DDB = _____$_{10,2,O}$
2. 10011 – 1111101 and 76 – 9 using 1's and 2's complement subtraction
3. Simplify the following using Boolean law with minimum literals and implement using Universal gates
   a. $Y = A + \overline{A}B + \overline{(A+B)}C + \overline{(A+B+C)}D$
   b. prove that $\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}\overline{C} = \overline{A} + \overline{B+C}$
4. Simplify the following using K – map to SOP and POS
   i. f = M(0,3,5,6,8,10)+d(11,13,14)
   ii. $F(A,B,C,D) = A + B + \overline{D}$
   iii. F = ∑(21,7,30,2,8,15,19,3) + d(0,18,15,6)
5. Design a Code converter to convert BCD to Binary.
6. Simplify the following circuit and draw the optimized circuit using Boolean logic



7. Four large tanks at a chemical plant contain different liquids being heated. Liquid-level sensors are being used to detect whenever the level in tank *A* or tank *B* rises above a predetermined level. Temperature sensors in tanks *C* and *D* detect when the temperature in either of these tanks drops below a prescribed temperature limit. Assume that the liquid-level sensor outputs *A* and *B* are LOW when the level is satisfactory and HIGH when the level is too high. Also, the temperature-sensor outputs *C* and *D* are LOW when the temperature is satisfactory and HIGH when the temperature is too low. Design a logic circuit that will detect whenever the level in tank *A* or tank *B* is too high at the same time that the temperature in either tank *C* or tank *D* is too low.
8. Design a 1-bit decrementer (a circuit which subtracts 1). Give
   (a) the arithmetic relationship between input and out put signals
   (b) the truth table,
   (c) logic diagram.
   Design a logic diagram of a 1-bit increment/decrement circuit controled by an id signal (increment when id = 1, decrement otherwise). Write the HDL.
   And Design a block diagram of a 4-bit increment/decrement circuit. Use the above HDL and concatenate.
9. Design a sequential circuit that works as a traffic light controller. The circuit does not have any data inputs (the clock and asynchronous reset are obviously available) and it has three data outputs: *Red*, *Green* and *Yellow*. After reset the circuit will activate *Red* for 200 clock

cycles, then it will activate *Green* for 200 clock cycles and then it will activate *Yellow* for 20 clock cycles (this sequence will repeat itself). While one output signal is turned on the other two output signals are deactivated. Derive the data-path elements and the FSM in the control-path. Write/simulate the Verilog code to verify the entire design.

SET – P

1. Simplify the following using Boolean expression

i. $(A+C)(AD+A\overline{D})+AC+C$

ii. $\overline{W}\,\overline{X}+\overline{X}\,\overline{Y}+YZ+\overline{W}\,\overline{Z}$

iii. $\bar{a}b+\bar{b}c+\bar{c}a=a\bar{b}+b\bar{c}+c\bar{a}$

2. Find the SOP and POS for the following using K – map

i. $A'B'C'D'+BC'D+A'C'D+A'BC+AD'$

ii. f = ∏(1,3,5,9,11,12,14)

iii. f = ∑(0,1,2,5,7,8,10,15)

3. Design a logic circuit whose output is HIGH whenever A and B are both HIGH as long as C and D are either both LOW or both HIGH. Try to do this without using a truth table. Then check your result by constructing a truth table from your circuit to see if it agrees with the problem statement.

4. Design a code converter to convert 2421 to 5311 code.

5. Perform the following

(i) 1001100-110011 using 1's complement subtraction

(ii) 93 – 14 using 1's complement

(iii) 87 – 6 using 2's complement

6. Convert the following

i. 111111101_2 = _____$_{4,10, H}$

ii. 8AF2.E9 = _____$_{2, 8, 10}$

7. You need to design a synchronous sequential circuit in the form of a positive edge-triggered Moore machine using RS - FF. The input signal *w* is synchronized with the clock pulses *C*. The output signal *z* should become 1 each time the value of the input signal *w* had not changed for two clock pulses. This change in the output value will appear at the clock pulse following the two pulses with the identical *w* values. See the example below for clarification.

w: 00110001101110011111110000010110 ...
z: 00101010010010010101000001000001 ...

Set up the circuit's state table and draw the state diagram

8. As an example of an unstructured combinational circuit design a circuit that divides a 3-bit positive binary number a = $(a_2a_1a_0)_2$ by a 2-bit positive binary number b = $(b_1b_0)_2$ calculating a 3-bit quotient q = $(q_2q_1q_0)_2$ and a 2-bit remainder r = $(r_1r_0)2$ so that

$$\frac{a}{b}=q+\frac{r}{b}$$

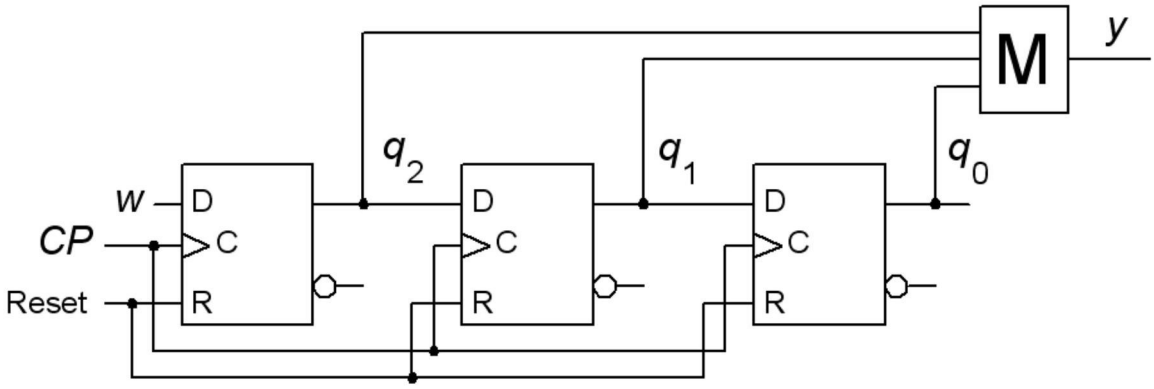
To make the task easier, take into account the following:

b	q_2	q_1	q_0	r_1	r_0
0	–	–	–	–	–
1	a_2	a_1	a_0	0	0
2	0	a_2	a_1	0	a_0

a. Complete the above table.
b. Derive logic equations for q and r. Aim at minimal implementation. Use Karnaugh maps when it makes the job easier.
c. Draw logic diagrams and write the HDL code using gate level and dataflow.

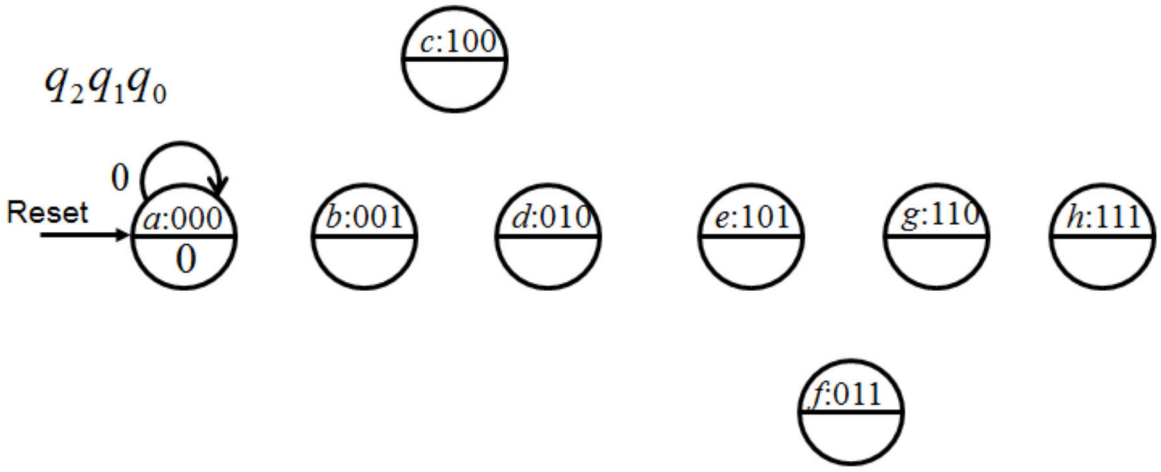
SET – Q

1. CONVERT THE FOLLOWING
   i. 101011110.11101 = _____$_{9,\ \ 16,H}$
   ii. 467.23_8 = _____$_{4,\ 2,\ H}$
   iii. C49D.B7 = _____$_{2,8,7}$
2. Find the minimum product of sums and SOP for
   (a) $F(a, b, c, d, e) = \sum m(1, 2, 3, 4, 5, 6, 25, 26, 27, 28, 29, 30, 31)$
   (b) $\pi(0,1,3,5,6,9,10,13,14)$
3. Perform the following
   i. 11110011 – 1110011 using 1's and 2's complement subtraction
   ii. 88 – 43 using 1's complement
   iii. 35 – 95 using 2's complement
4. Each of the following sentences has two possible interpretations depending on whether the AND or OR is done first. Write an equation for each interpretation. (a) The buzzer will sound if the key is in the ignition switch, and the car door is open, or the seat belts are not fastened. (b) You will gain weight if you eat too much, or you do not exercise enough, and your metabolism rate is too low. (c) The speaker will be damaged if the volume is set too high, and loud music is played, or the stereo is too powerful. (d) The roads will be very slippery if it snows, or it rains, and there is oil on the road.
5. Simplify the following using Boolean law with minimum literals and implement using Universal gates
   a. $Y = A + \overline{A}B + \overline{(A + B)}C + \overline{(A + B + C)}D$
   b. prove that $\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}\overline{C} = \overline{A} + \overline{B + C}$
6. Show that $A \otimes B \otimes C \otimes D = \sum(0,3,5,6,9,10,12,15)$
7. A synchronous sequential circuit based on a shift register is used as a "Majority voter". The value of the input signal *w* that occurred most of the times in the past three clock pulses is displayed at the output *y*. The gate denoted by the "M" is a so-called majority gate, it's output takes the same value as the majority of its inputs.



8. Analyze the shift register and draw state diagram and state table for the que 1. (Please take the

help of the initiated state diagram with eight states shown below, but draw your own figure to answer).



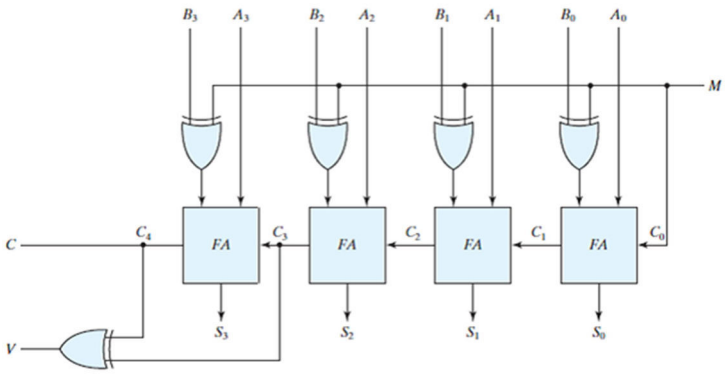
SET – R

1. Convert the following
   a. 11110010.111001_2 = _____$_{8,5,H}$
   b. 3213_4 = _____$_{2,10,8}$
   c. 34D.EFF = _____$_{4,2,O}$
2. Perform the subtraction 64 – 31 and 99 – 7 in 1's and 2's complement method.
   b. Simplify the following expression to a sum of two terms and then factor the result to obtain a product of sums:

   $$ab\bar{d}\bar{f} + \bar{b}ceg\bar{h} + ab\bar{d}f + ac\bar{d}e + \bar{b}ce$$

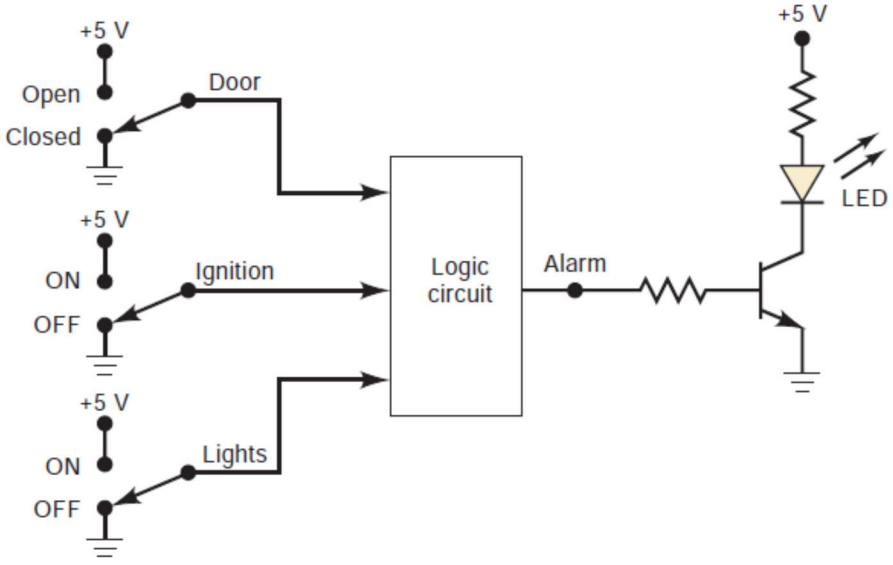
3. The adder-subtractor circuit of Fig. below has the following values for mode input M and data inputs A and B:

	M	A	B
(a)	0	0011	0101
(b)	0	1101	1101
(c)	1	0100	0011
(d)	1	0000	0001



in each case determine the values of the four SUM outputs, the carry C, and overflow V.

4. Fig. below shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used to indicate the status of the door by the driver's seat, the ignition, and the headlights, respectively. Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following conditions exists:



iii. The headlights are on while the ignition is off.
iv. The door is open while the ignition is on.

5. Design a code converter to convert gray code to 2421.

6. Draw a state diagram for a mealy type state machine specified as follows:

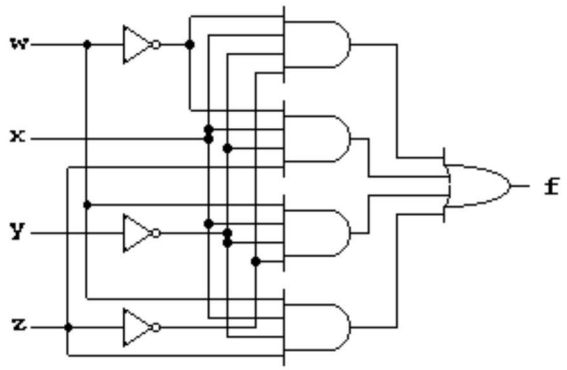
- Denote "a" the initial state of the machine
- set the initial output to the initial input (the input is presented to the machine bit by bit)
- The output changes value only when three successive inputs have the same value and that value is opposite to the current output. For example, if the current output is 1 and the machine detects three consecutive 0 it changes the output to 0.

Design the circuit using D – FF and write the Verilog HDL.

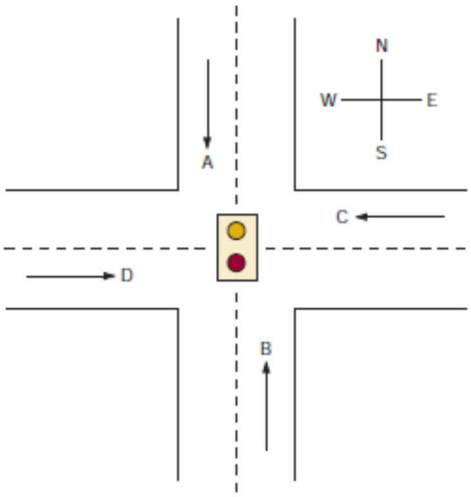
7. Design the 4 bit 7311 code to 53-1-1 code and write the Verilog HDL using if else statement.

SET – S

1. CONVERT THE FOLLOWING
   i. 101010110.10011 = _____$_{9,\ \ 16,H}$
   ii. 726.5_8 = _____$_{4,\ 2,\ H}$
   iii. 67AD.EF = _____$_{2,8,7}$
2. PERFORM THE FOLLOWING
   i. 1001101 – 1110011 using 1's complement subtraction
   ii. 1100011 – 10110011 using 2's complement subtraction
   iii. 93 – 65 using both 1's and 2's complement
   iv. 57 - 99 using both 1's and 2's complement
3. Simplify the following using Boolean algebra
   i. $Y = \overline{(C+D)}\overline{A}C\overline{D} + A\overline{B}\overline{C} + \overline{A}\overline{B}CD + AC\overline{D}$
   ii.



   iii. F = M(3,7,8,10,12,13)
4. Simplify the following using K – map to SOP and POS
   i. f = M(0,3,5,6,8,10)+d(11,13,14)
   ii. $F(A,B,C,D) = A + B + \overline{D}$
   iii. F = $\sum$(21,7,30,2,8,15,19,3) + d(0,18,15,6)
5. Design a Code Converter to convert 24-2-1 code to 2421 code
6. Figure below shows the intersection of a main highway with a secondary access road. Vehicle-detection sensors are placed along lanes *C* and *D* (main road) and lanes *A* and *B* (access road). These sensor outputs are LOW (0) when no vehicle is present and HIGH (1) when a vehicle is present. The intersection traffic light is to be controlled according to the following logic:



1. The east-west (E-W) traffic light will be green whenever *both* lanes *C* and *D* are occupied.
2. The E-W light will be green whenever *either C* or *D* is occupied but lanes *A* and *B* are not *both* occupied.
3. The north-south (N-S) light will be green whenever *both* lanes *A* and *B* are occupied but *C* and *D* are not *both* occupied.
4. The N-S light will also be green when *either A* or *B* is occupied while *C* and *D* are *both* vacant.
5. The E-W light will be green when *no* vehicles are present. Using the sensor outputs *A*, *B*, *C,* and *D* as inputs, design a logic circuit to control the traffic light.There should be two outputs, N-S and E-W, that go HIGH when the corresponding light is to be *green.* Simplify the circuit as much as possible and show *all* steps.

7. Write an HDL dataflow description of a 4-bit adder/subtractor of unsigned numbers. Use the FOR loop.
8. Design a sequential circuit using T - FF that has 1 data input (*w*) and 1 data output (*z*). The output *z* will become 1 only if the input *w* has been 1010 over the last 4 clock cycles. Draw the FSM diagram and write/simulate the Verilog code to verify it.

SET – T

1. A manufacturing plant needs to have a horn sound to signal quitting time. The horn should be activated when either of the following conditions is met:
   i. It's after 5 o'clock and all machines are shut down.
   ii. It's Friday, the production run for the day is complete, and all machines are shut down.
   iii. Design a logic circuit that will control the horn. (Hint: Use four logic input variables to represent the various conditions; for example, input A will be HIGH only when the time of day is 5 o'clock or later.)
2. Simplify using K – Map and give the SOP and POS i. F = m(7,13,5,30,17,5,27,8,14,19)+d(0,11,12,15,21) ii. Y = $\overline{C}(\overline{A}\overline{B}\overline{D}+D)+A\overline{B}C+\overline{D}$ iii. Determine the minimum expression for each K map given below

	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	1	1	1	1
$\overline{A}B$	1	1	0	0
AB	0	0	0	1
$A\overline{B}$	0	0	1	1

(a)

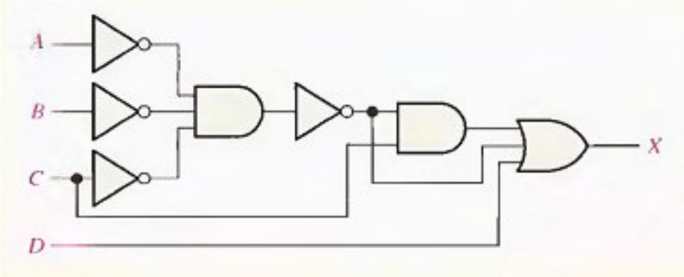
	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	1	0	1	1
$\overline{A}B$	1	0	0	1
AB	0	0	0	0
$A\overline{B}$	1	0	1	1

(b)

	$\overline{C}$	C
$\overline{A}\overline{B}$	1	1
$\overline{A}B$	0	0
AB	1	0
$A\overline{B}$	1	X

(c)

3. Convert the Following i. 86753.12 = _____$_{2,H}$ ii. 11110001.11 = _____$_{O,9,4}$ iii. AED.87 = _____$_{9,2}$
4. Design a code converter to convert 53-1-1 to 84-2-1
5. Perform the subtraction 52 – 73 and 111011 - 100101 using 1's and 2's complement method.
6. i. Reduce the combinational logic circuit in Fig. to a minimum form.



7. Simplify the following using Boolean algebra
   i. f=m(1,2,4,7,10,12)
   ii. F = M(1,2,3,8,9,10,11,14)
8. Identify each of the following expression as SOP, POS and its canonical form respectively
   a. $AB+\overline{A}BD+\overline{A}C\overline{D}$
   b. (A'+B) (A+B+D)D'
9. Write an HDL dataflow description of a 4-bit adder/subtractor of unsigned numbers. Use the conditional operator.

10. Design a sequential circuit using JK - FF that has 1 data input (w) and 1 data output (z). The output z will become 1 only if the input w has been 1 for the last 5 clock cycles. Draw the FSM diagram and write/simulate the Verilog code to verify it.