MEMORY ORGANIZATION

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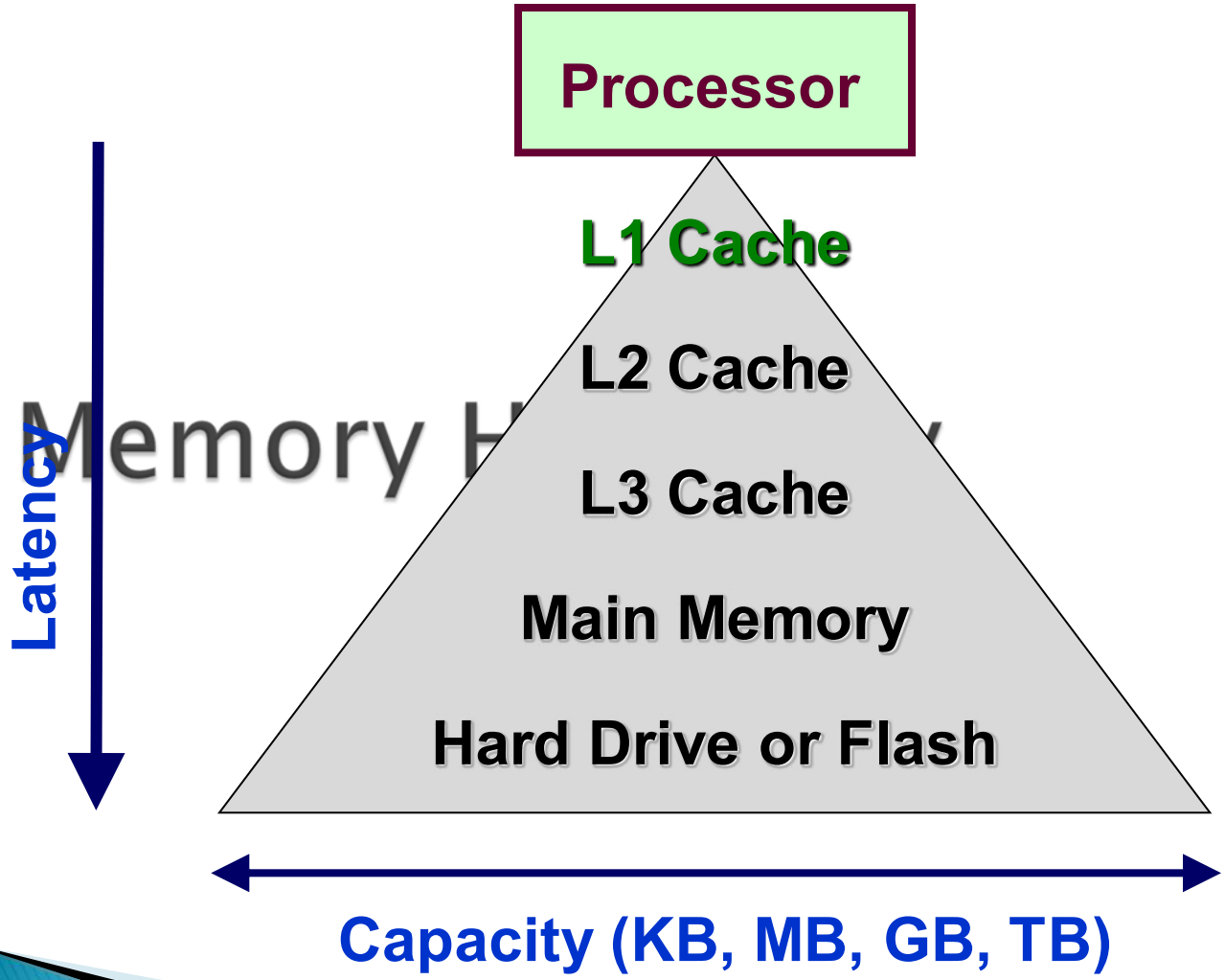
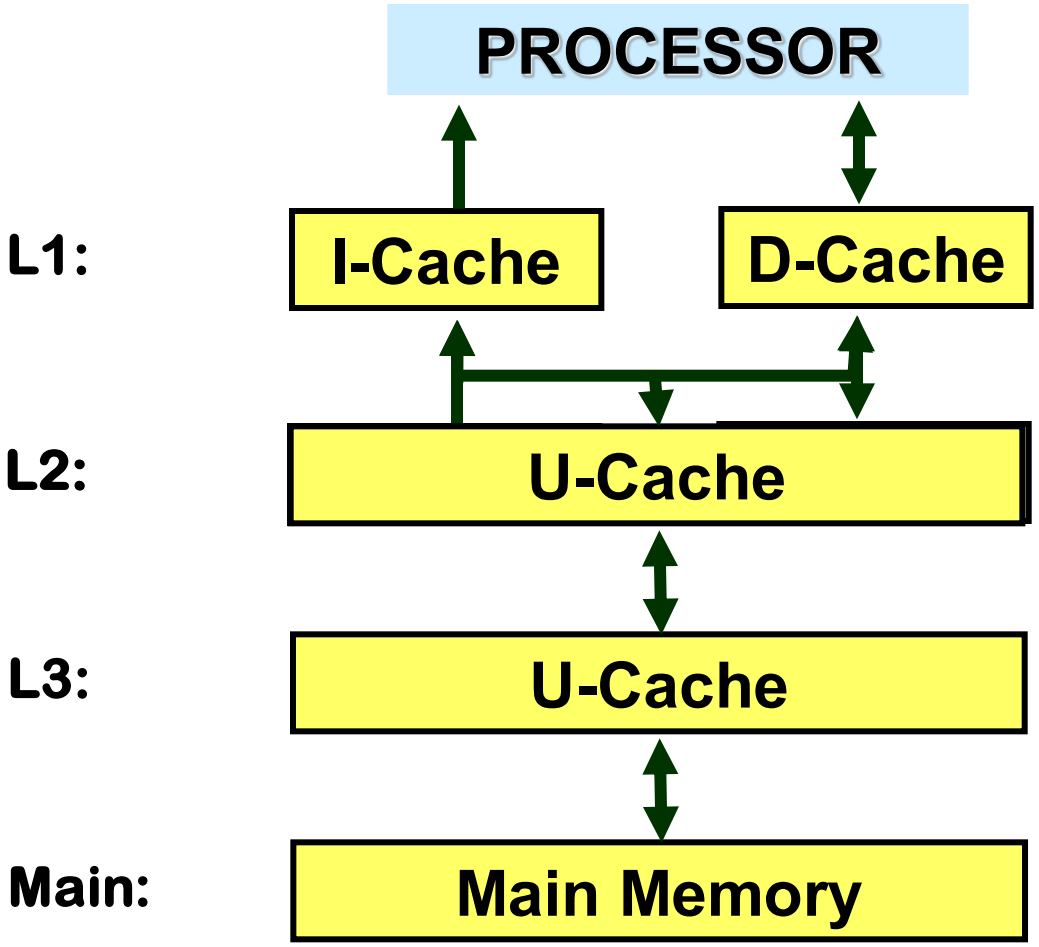
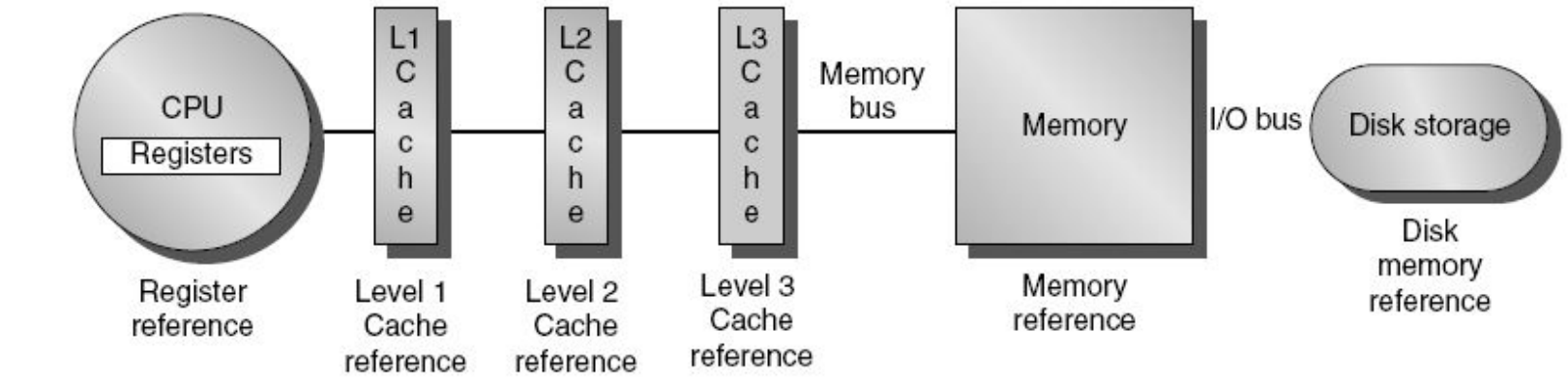
Introduction

- Programmers want very large memory with low latency
- Fast memory technology is more expensive per bit than slower memory
- Solution: organize memory system into a hierarchy
  - Entire addressable memory space available in largest, slowest memory
  - Incrementally smaller and faster memories, **each containing a subset of the memory below it**, proceed in steps up toward the processor
- Temporal and spatial locality insures that nearly all references can be found in smaller memories
  - Gives the allusion of a large, fast memory being presented to the processor

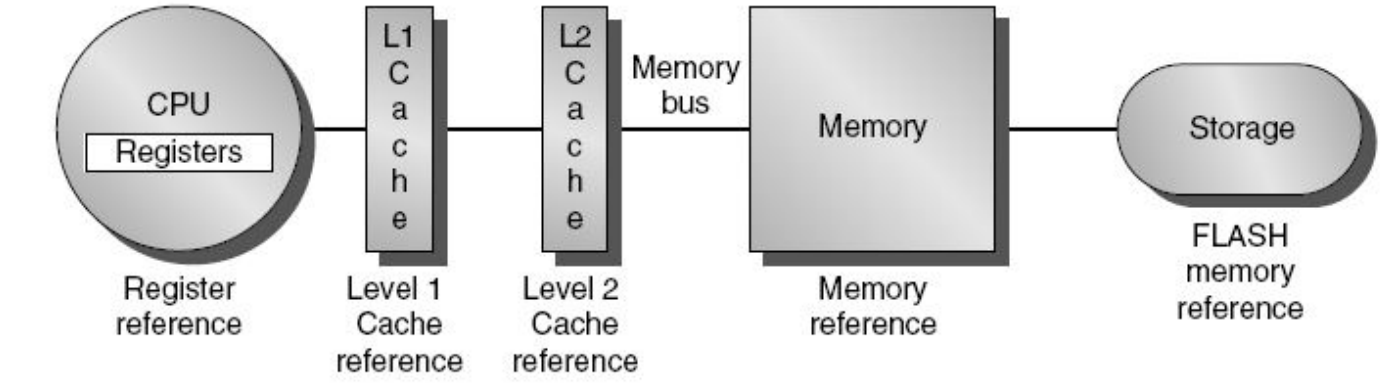
Memory Hierarchy




PROCESSOR
L1:
I-Cache
D-Cache
L2:
U-Cache
L3:
U-Cache
Main:
Main Memory

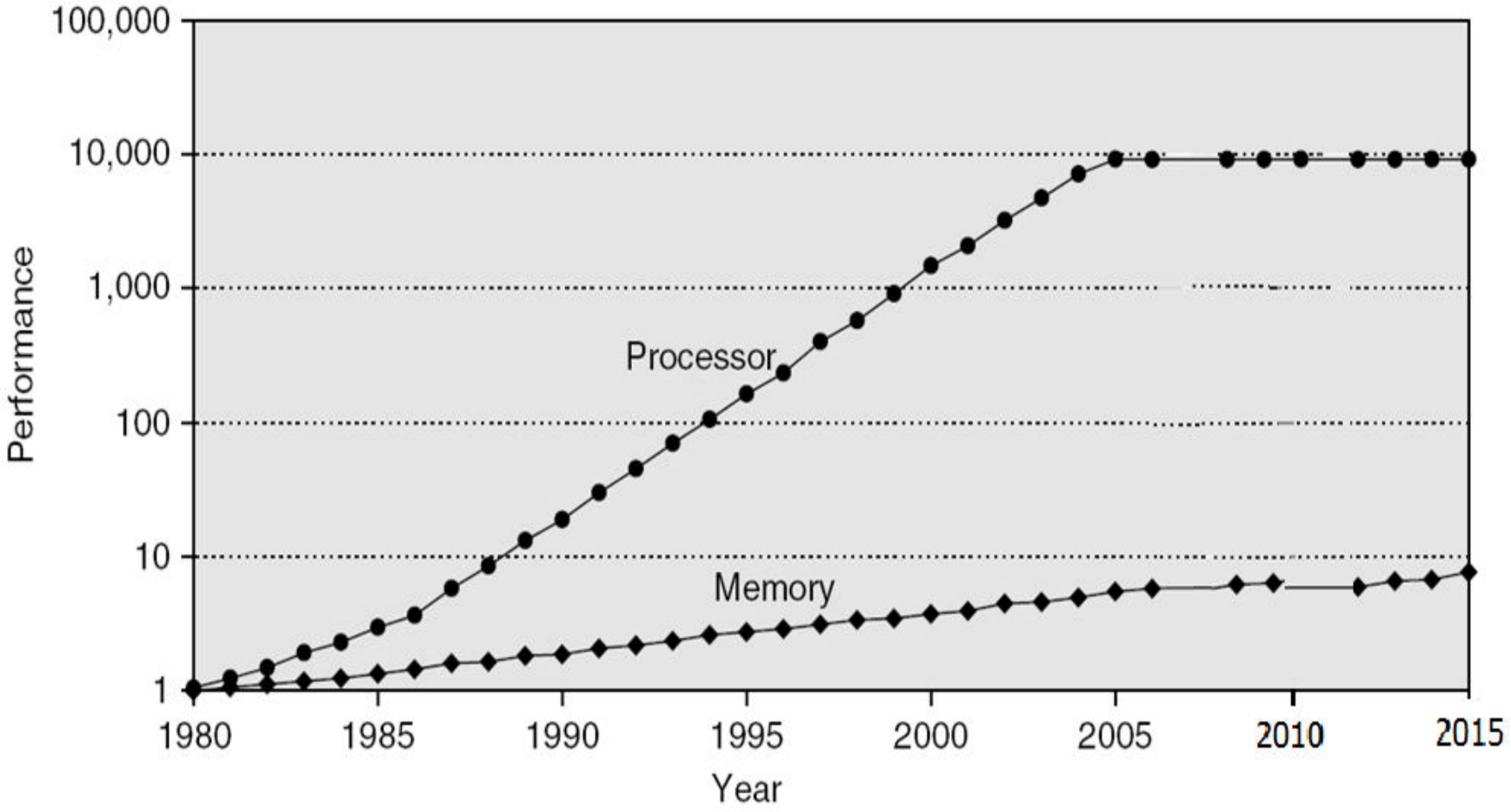


(a) Memory hierarchy for server



(b) Memory hierarchy for a personal mobile device

Memory Performance Gap



Memory organization

Byte Ordering

Ordering of bytes within a multi-byte data item

Types:

- Big-endian
- Little-endian

Byte Storage Methods (Byte Ordering)

- Big-Endian
  - Assigns MSB to least address and LSB to highest address
  - Ex: 0 × DEADBEEF

Memory Location	Value
Base Address + 0	DE
Base Address + 1	AD
Base Address + 2	BE
Base Address + 3	EF

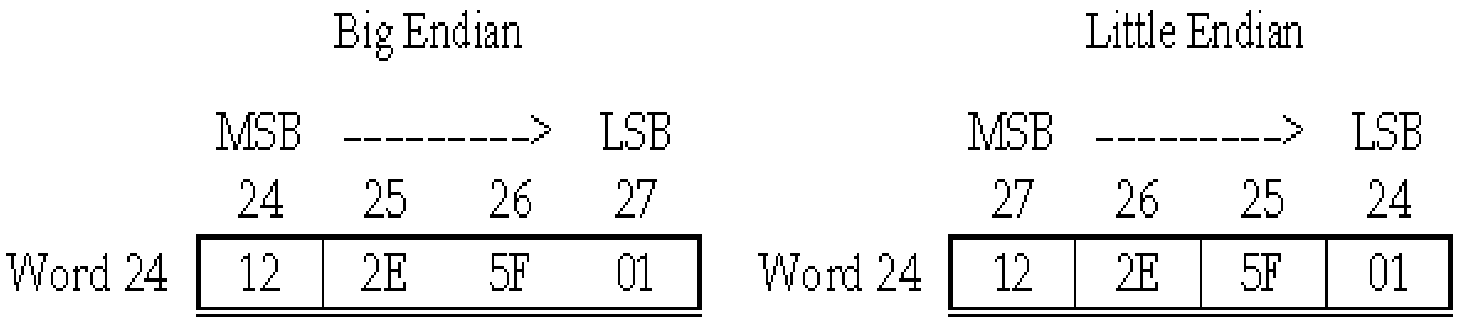
Byte Storage Methods contd.,

- Little Endian
  - Assigns MSB to highest address and LSB to least address
  - Ex: 0 × DEADBEEF

Memory Location	Value
Base Address + 0	EF
Base Address + 1	BE
Base Address + 2	AD
Base Address + 3	DE

Example

- **Example:** Show the contents of memory at word address 24 if that word holds the number given by 122E 5F01H in both the big-endian and the little-endian schemes?



Some points about endian-ness

- Computer systems, in use today are split between those that are big-endian, and those that are little-endian.
- This leads to problems when a big-endian computer wants to transfer data to a little-endian computer.
- Some architectures, for example the PowerPC and ARM, allow the endian-ness of the architecture to be changed programmatically.

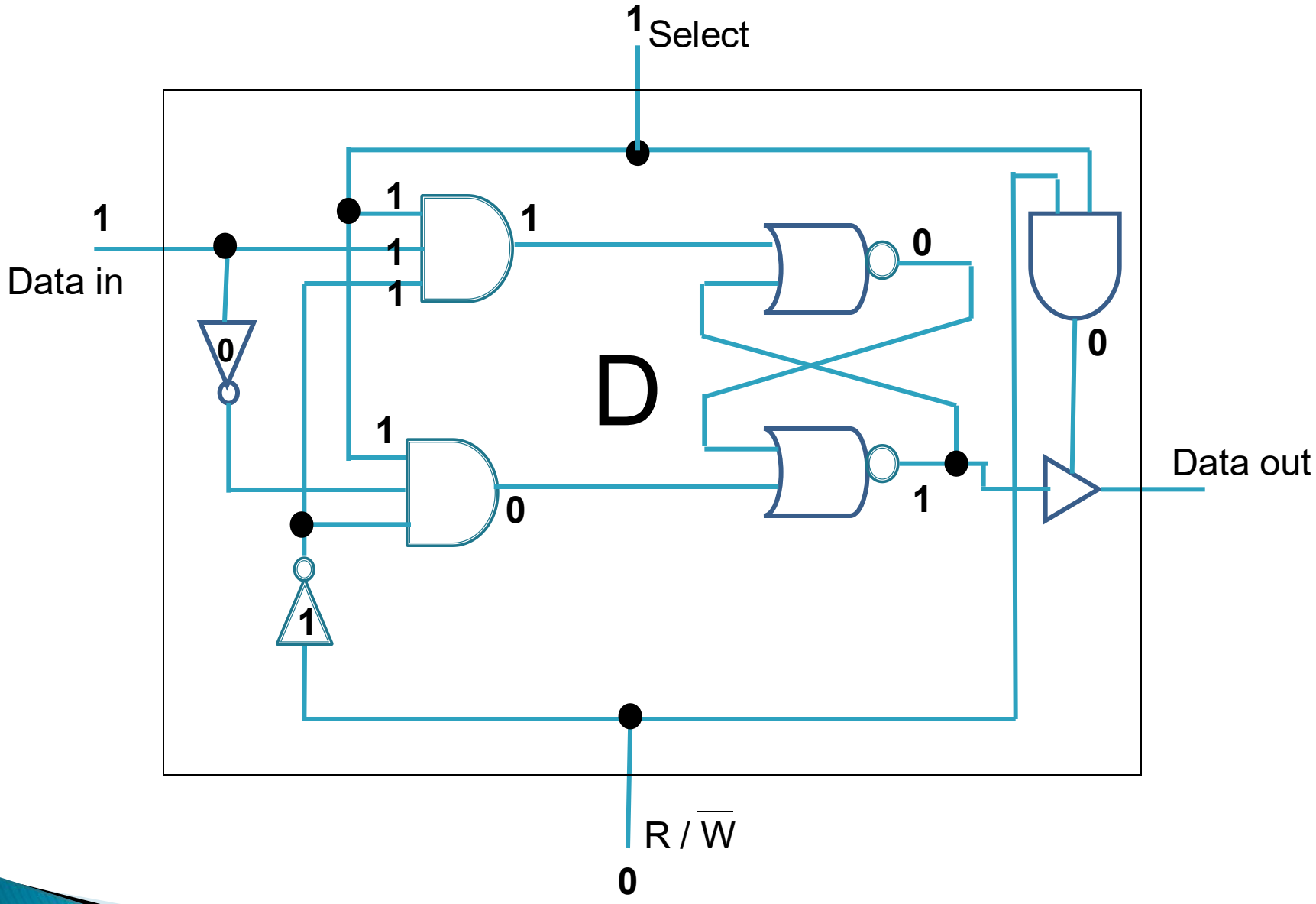
References

Text Book

- William Stallings "Computer Organization and architecture" Prentice Hall, 8th edition, 2009

Thank You

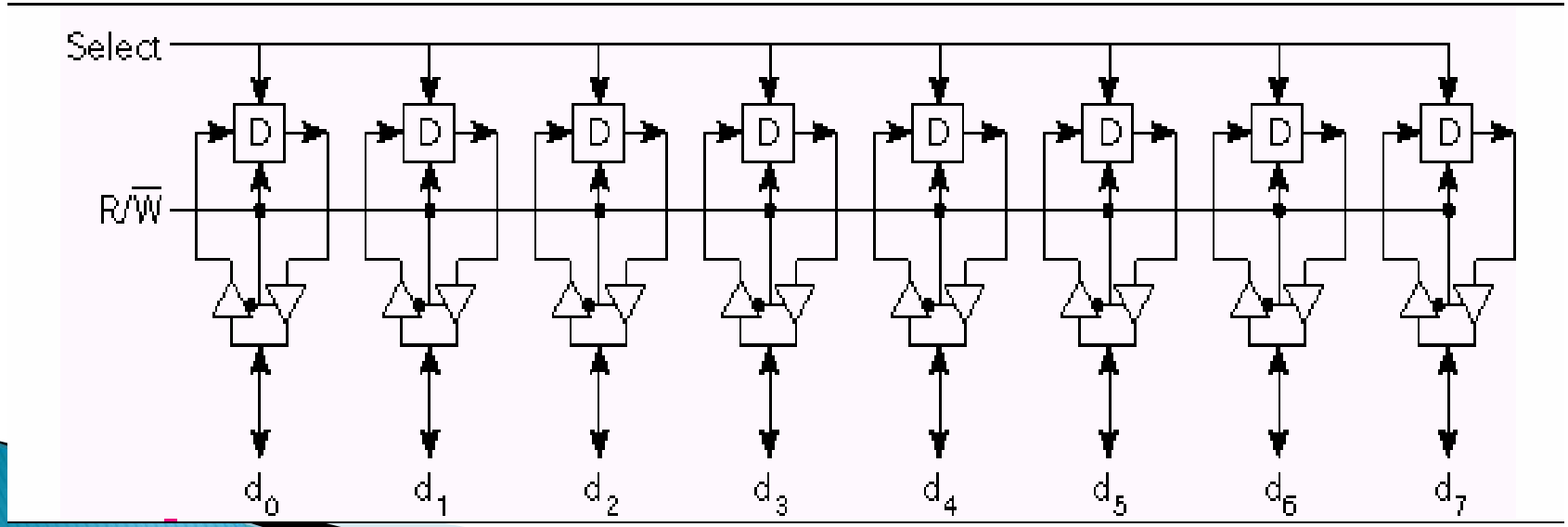
Conceptual memory cell – static RAM cell



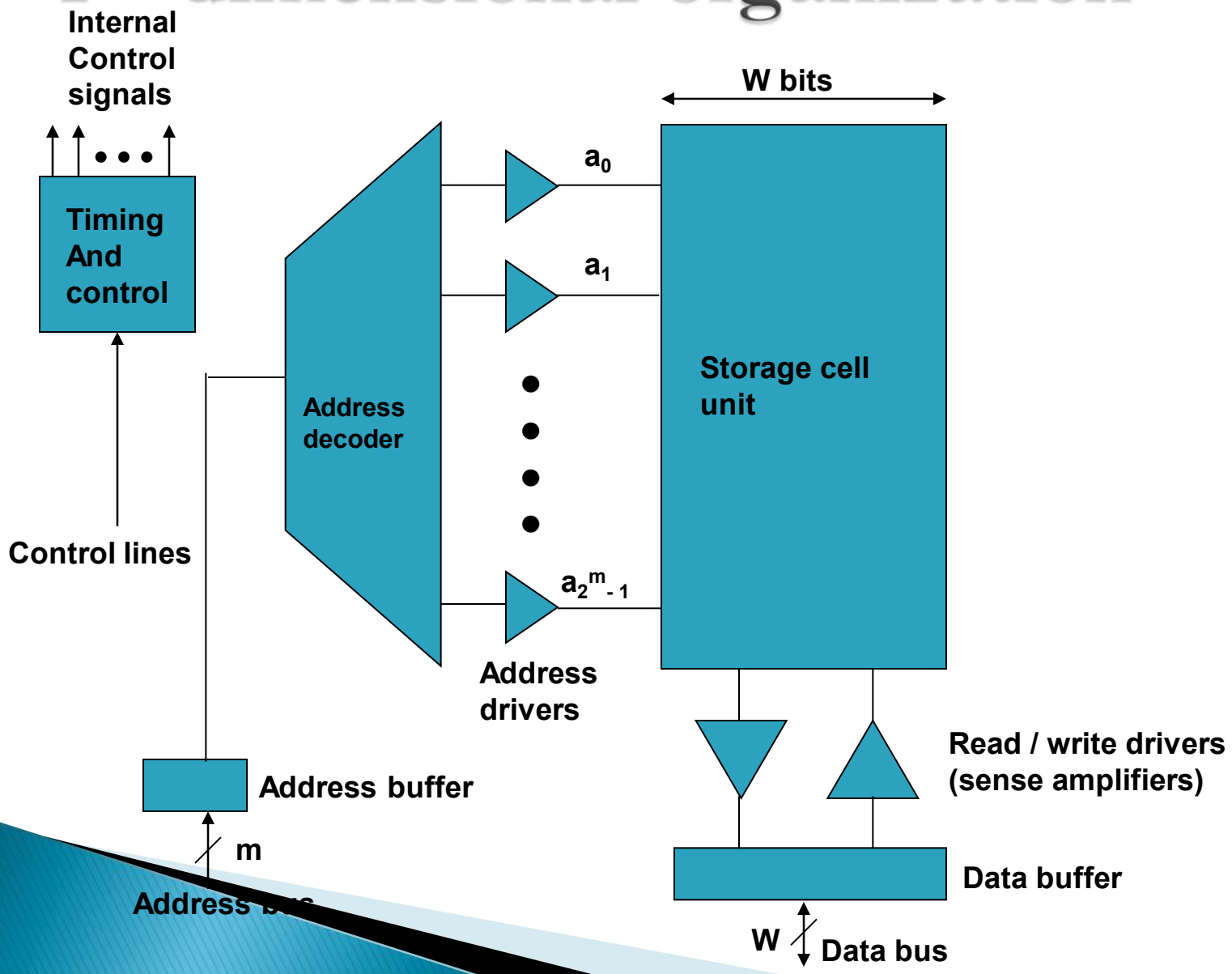
So, Tri-state buffer is in high impedance state and buffers the value

1 – dimensional organization

- Buffers would not be required, since the output of each cell is already buffered. They are shown to indicate buffering of the register from the data bus

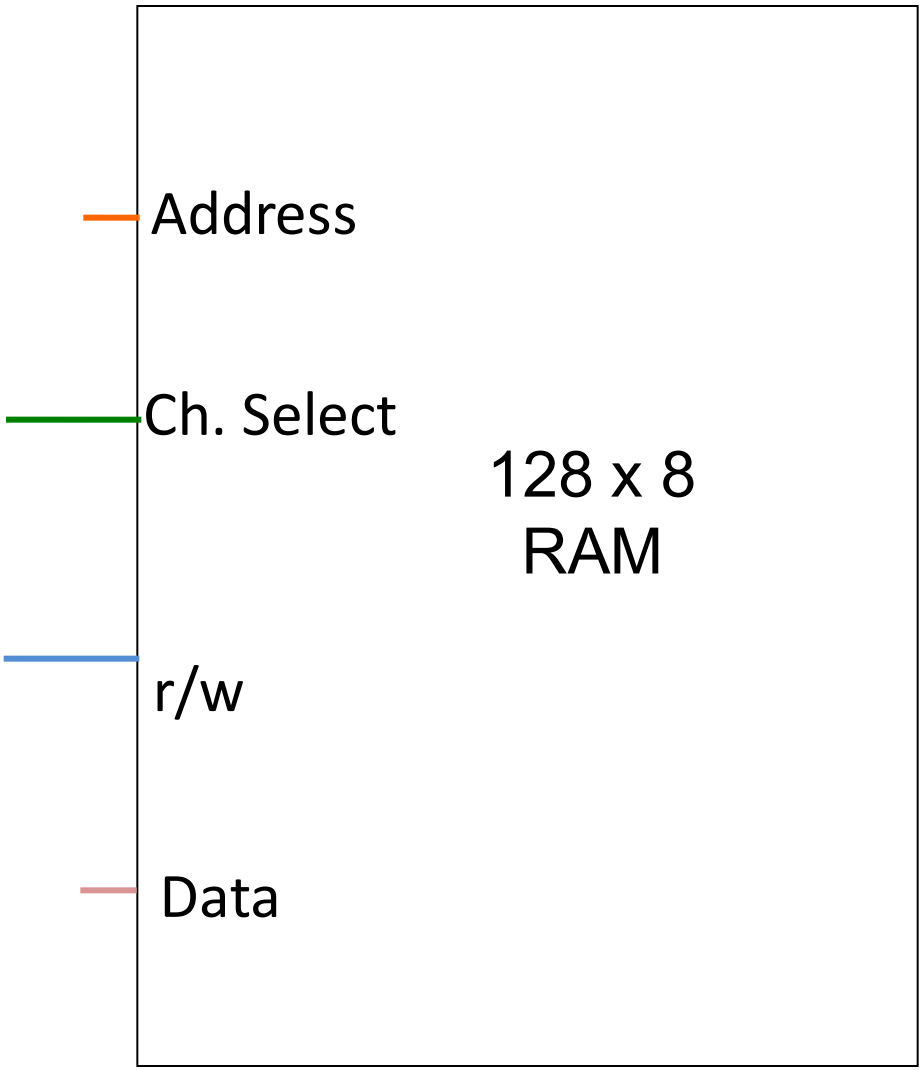


1 – dimensional organization

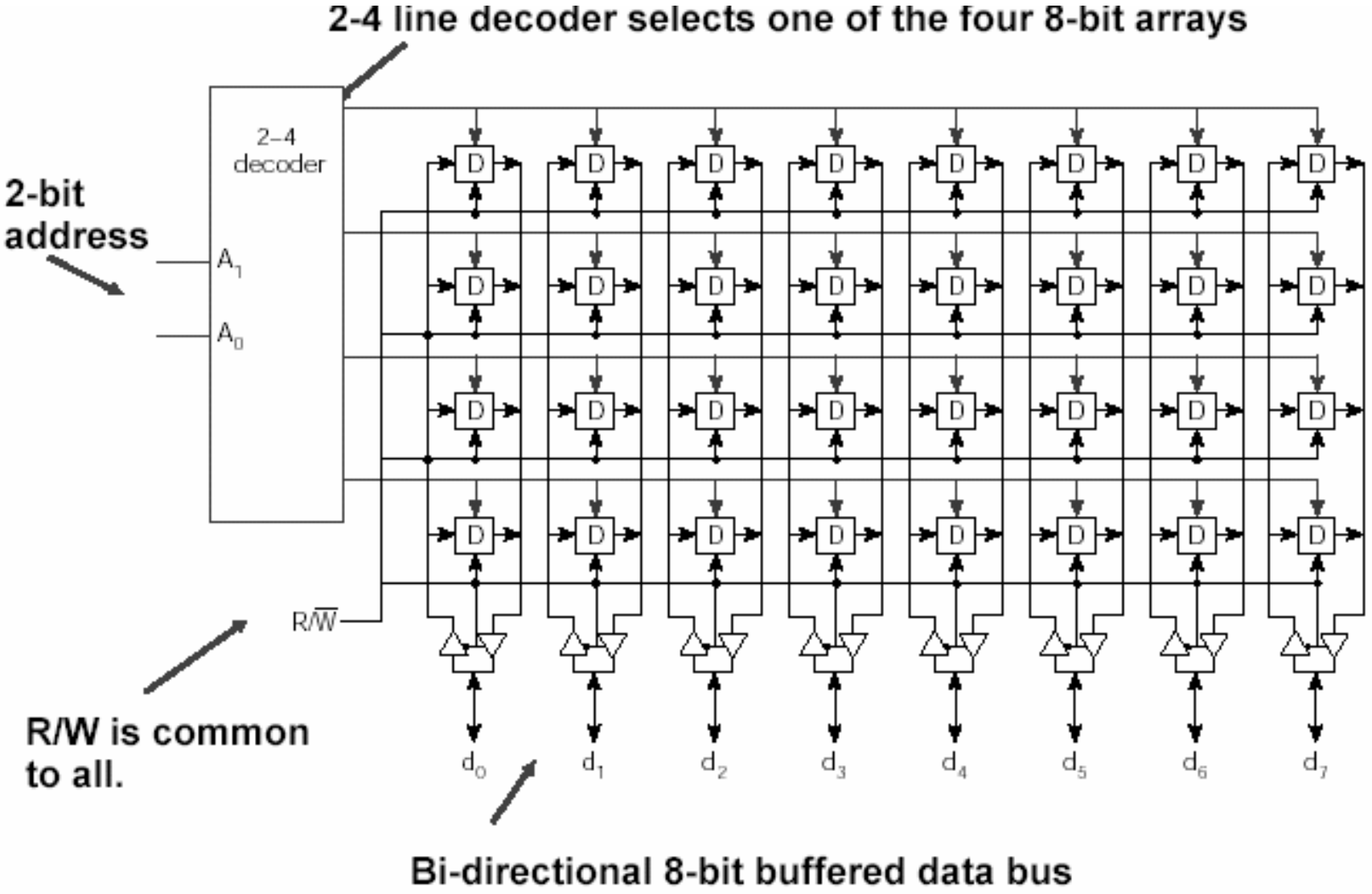



Address Lines
CHIP
R/W
Data Lines

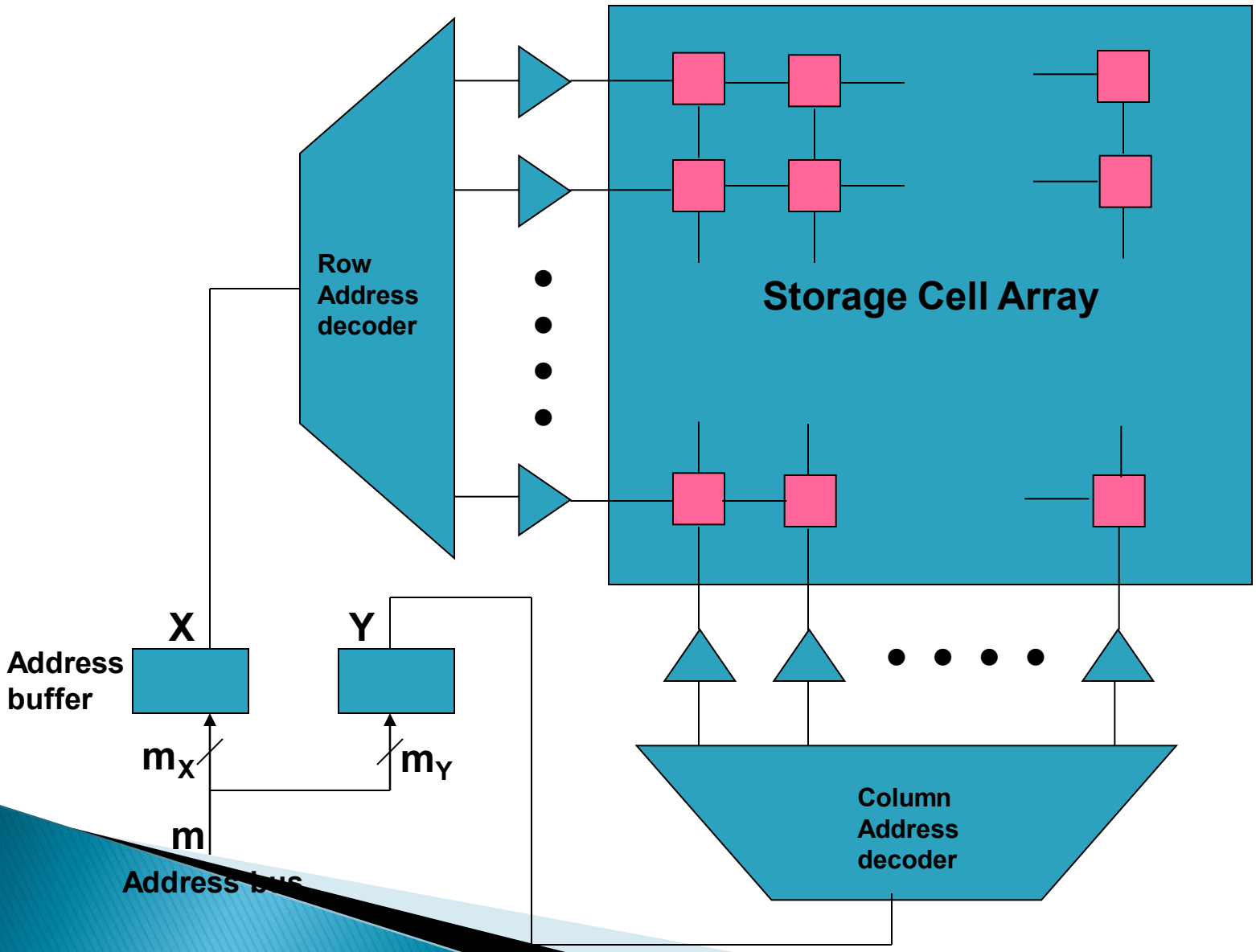
128x 8
RAM



2 – dimensional organization



2 – dimensional organization



References

Text Book

- William Stallings "Computer Organization and architecture" Prentice Hall, 7th edition, 2006
- J. P. Hayes, Computer system architecture, McGraw Hill,2000