

Lecture 48: DIRECT MEMORY ACCESS

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Introduction

- In the data transfer methods discussed under programmed I/O, it is assumed that machine instructions are used to transfer the data between I/O device and memory.
 - Not very suitable when large blocks of data are required to be transferred at high speed (e.g. transfer of a disk block).
- An alternate approach is *Direct Memory Access* (DMA).
 - Allows transfer of a block of data directly between an I/O device and memory, without continuous CPU intervention.



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- Why programmed I/O is not suitable for high-speed data transfer?
 - a) Several program instructions have to be executed for each data word transferred between the I/O device and memory.
 - Suppose 20 instructions are required for each word transfer.
 - The CPI of the machine running at 1 GHz clock is 1.
 - So, 20 nsec is required for each word transfer → maximum 50 M words/sec
 - Data transfer rates of fast disks are higher than this figure.



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- b) Many high speed peripheral devices like disk have a synchronous mode of operation, where data are transferred at a fixed rate.
 - Consider a disk rotating at 7200 rpm, with average rotational delay of 4.15 msec.
 - Suppose there are 64 Kbytes of data recorded in every track.
 - Once the disk head reaches the desired track, there will be a sustained data transfer at rate $64 \text{ Kbytes} / 4.15 \text{ msec} = 15.4 \text{ MBps}$.
 - This sustained data transfer rate is comparable to the memory bandwidth, and cannot be handled by programmed I/O.



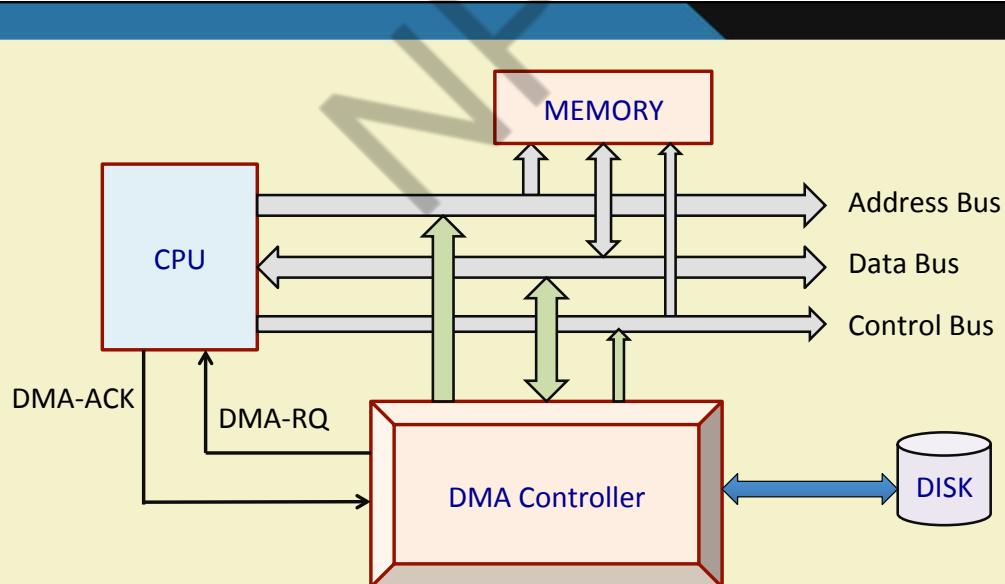
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DMA Controller

- A hardwired controller called the DMA controller can enable direct data transfer between I/O device (e.g. disk) and memory without CPU intervention.
 - No need to execute instructions to carry out data transfer.
 - Maximum data transfer speed will be determined by the rate with which memory read and write operations can be carried out.
 - Much faster than programmed I/O.



Steps Involved

- a) When the CPU wants to transfer data, it initializes the DMA controller.
 - How many bytes to transfer, address in memory for the transfer.
- b) When the I/O device is ready for the transfer, the DMA controller sends DMA-RQ signal to the CPU.
- c) CPU waits till the next DMA breakpoint, relinquishes control of the bus (i.e. puts them in high impedance state), and sends DMA-ACK to DMA controller.
- d) Now DMA controller enables its bus interface, and transfers data directly to/from memory.
- e) When done, it deactivates the DMA-RQ signal.
- f) The CPU again begins to use the bus to access memory.



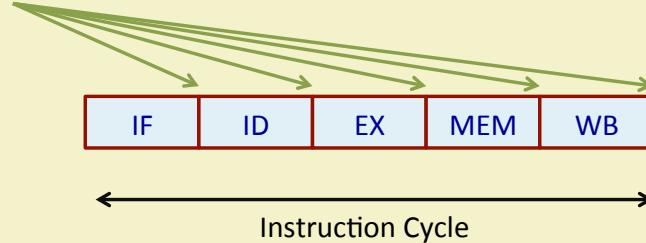
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- The DMA breakpoints:
 - DMA request can be acknowledged at the end of any machine cycle.

*DMA
breakpoints*



*Why cannot we have
interrupt breakpoints
at the end of any
machine cycle?*



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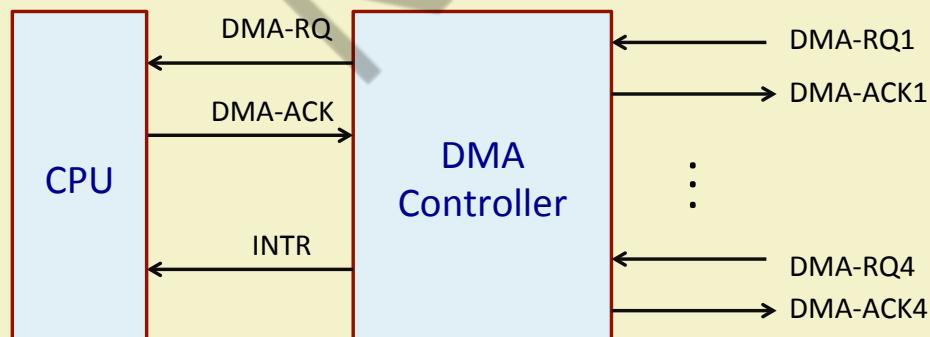
- For every DMA channel, the DMA controller will have three registers:
 - a) Memory address
 - b) Word count
 - c) Address of data on disk
- CPU initializes these registers before each DMA transfer operation.
- Before the data transfer, DMA controller requests the memory bus from the CPU.
- When the data transfer is complete, the DMA controller sends an interrupt signal to the CPU.



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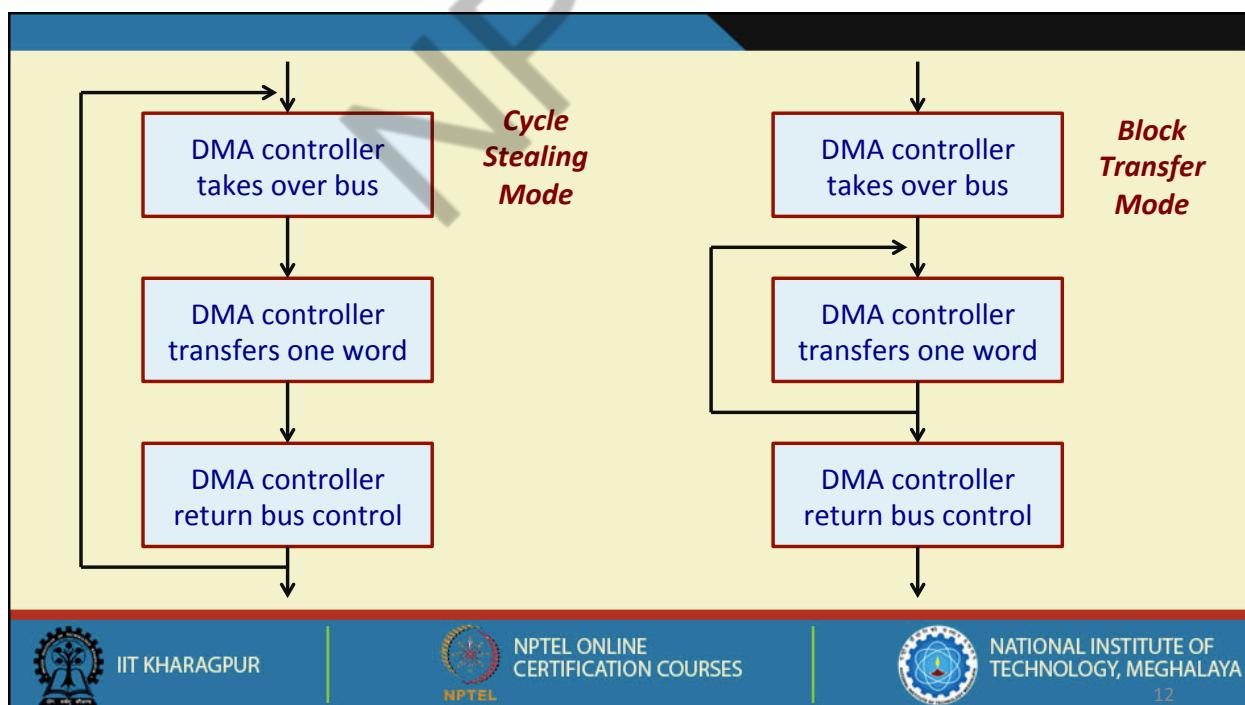
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DMA Transfer Modes

- DMA transfer can take place in two modes:
 - a) DMA cycle stealing
 - The DMA controller requests for the for a few cycles 1 or 2.
 - Preferably when the CPU is not using memory.
 - DMA controller is said to steal cycles from the CPU without the CPU knowing it.
 - b) DMA block transfer
 - The DMA controller transfers the whole block of data without interruption.
 - Results in maximum possible data transfer rate.
 - CPU will lie idle during this period as it cannot fetch any instructions from memory.



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Others Applications of DMA

- Other than data transfer to/from high-speed peripheral devices, DMA can be used in some other areas as well:
 - High-speed memory-to-memory block move.
 - Refreshing dynamic memory systems, by periodically generating dummy read requests to the columns.



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Lecture 49: SOME EXAMPLE DEVICE INTERFACING

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Introduction

- Here we consider two simple examples to illustrate the I/O device interfacing techniques discussed earlier.
 - a) Keyboard interfacing
 - b) Printer interfacing



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Keyboard Interfacing

- What is a keyboard?
 - A set of pushbutton switches (keys) interfaced to a computer.
 - Typically arranged in the form of a two-dimensional matrix.
 - A key is connected to a row line and a column line at every junction.
 - Results in minimization of the number of port lines required.



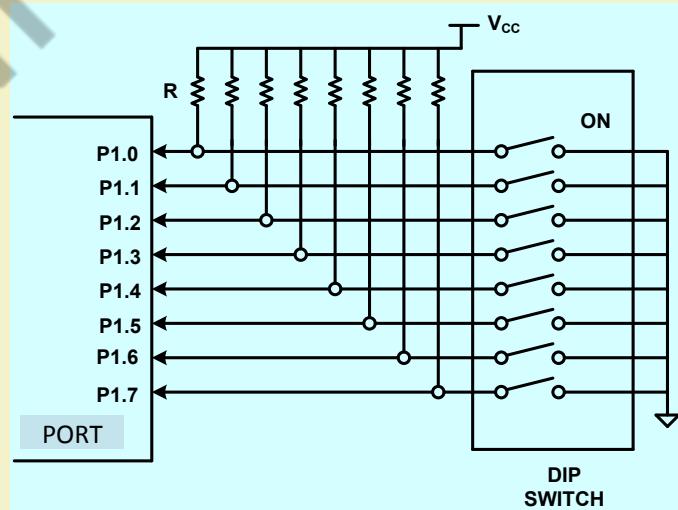
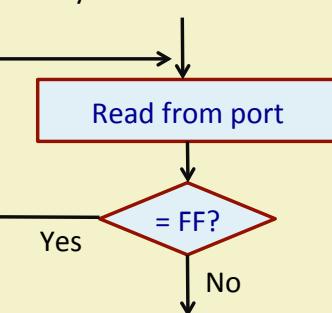
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Interfacing Switches

- How to check status for asynchronous transfer?



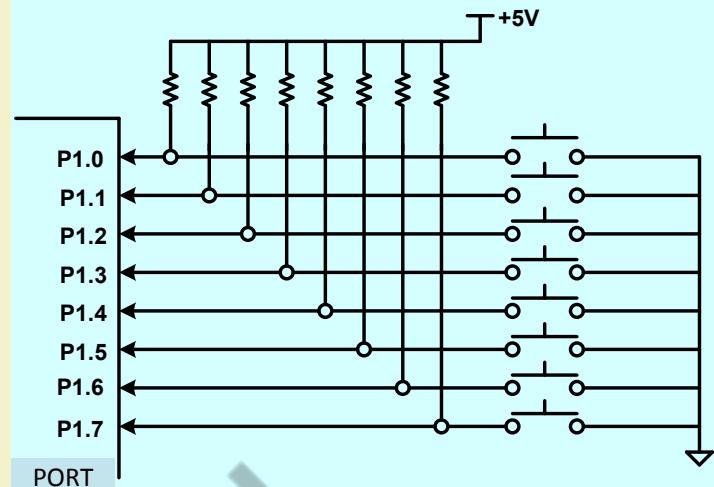
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Interfacing a Keyboard

- One key per port line.
- For N keys, number of port lines required will be N.
 - Too expensive.

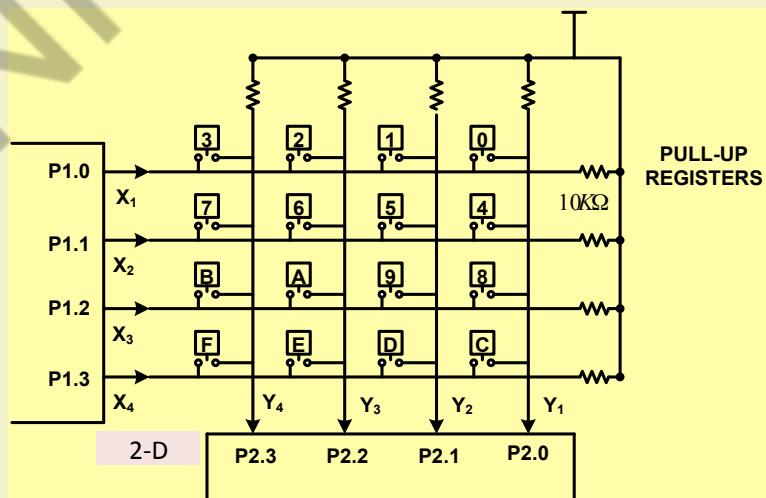


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Interfacing a Keyboard

- Keys organized in matrix form.
- For N keys, number of port lines required will be $2 \times N$.
 - Possible to interface large keyboards.



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- How to detect the status of the device (i.e. whether any key has been pressed)?
 - Output all-0's to the rows.
 - Read the column port, and check whether all the bits are 1.
 - If any of the bits is 0, it means a key has been pressed.
- Allows asynchronous mode of transfer.



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- How to detect which key has been pressed?
 - Requires a process called keyboard scanning.
 - One of the rows is made 0 at a time, and the column bits are checked.
 - We basically check whether some key in that particular row has been pressed.
- We find out both the row number and the column number of the key that has been pressed.



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- How to interface a keyboard in interrupt driven mode?
 - Normally all the rows of the keyboard are connected to ground; possibly through a set of AND gates with a control input that is made 0.
 - The column lines are connected to the inputs of a NAND gate, the output of which is connected to the INTR input.
 - The output of the NAND gate will become 1 whenever any key is pressed.
- Inside the ISR:
 - The control inputs of the AND gates are set to 1.
 - Normal keyboard scanning is carried out to identify the key pressed.



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Printer Interfacing

- Older printers has serial and parallel ports for interfacing to computer systems.
 - RS-232C serial data interface.
 - LPT parallel data interface (8 data lines).
- Modern-day printers support the much higher speed Universal Serial Bus (USB) interface.
 - Almost all devices today have USB interfaces.



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- The LPT port used a 25-pin connector:
 - 8 data lines
 - STROBE
 - BUSY
 - ACK
- After sending the data, the CPU activates the STROBE input to inform the printer that data is ready.
 - The printer will activate BUSY and start printing; once done, it will send back ACK to the CPU.
- The interface allows asynchronous data transfer using handshaking.

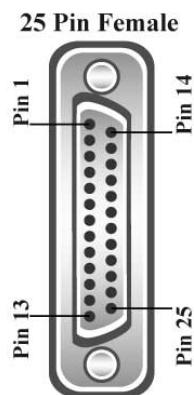


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LPT Printer Port

Pin 1	Data Strobe
Pin 2	Data 0
Pin 3	Data 1
Pin 4	Data 2
Pin 5	Data 3
Pin 6	Data 4
Pin 7	Data 5
Pin 8	Data 6
Pin 9	Data 7
Pin 10	Acknowledge
Pin 11	Busy
Pin 12	Paper Out
Pin 13	Select
Pin 14	Auto Feed
Pin 15	Error
Pin 16	Int
Pin 17	Select Input
Pin 18-25	Ground



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Lecture 50: EXERCISES ON I/O TRANSFER

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Example 1

- Suppose we want to read 2048 bytes in programmed I/O mode of transfer. The bus width is 32 bits. Each time an interrupt occurs, it takes 4 μ sec to service it (i.e. transfer 32 bits). How much CPU time is required to read 2048 bytes?



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Example 2

- A DMA module is transferring bytes to main memory from an external device at 76800 bps. The CPU can fetch instructions at a rate of 2 million instructions per second. Assume instruction size is 32 bits. How much will the processor be slowed down due to DMA activity?



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Example 3

- A DMA controller transfers 32-bit words to memory using cycle stealing. The words are assembled from a device that transmits bytes at a rate of 2400 bytes per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much time will the CPU be slowed down because of the DMA transfer?



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Example 4

- Consider a system employing interrupt-driven I/O for a device that transfers data at 8 KB/s on a continuous basis. The interrupt processing takes about $100\mu\text{sec}$ and the I/O device interrupts the CPU for every byte.

While executing the ISR, the processor takes about $8\mu\text{sec}$ for the transfer of each byte. What is the fraction of CPU time consumed by the I/O device?



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Example 5

- Consider a disk drive with 16 surfaces, 512 tracks per surface, and 512 sectors per track, 1024 bytes per sector, and a rotation speed of 3600 rpm. The disk is operated in cycle stealing mode whereby whenever one 4-byte word is ready, it is sent to memory. Similarly for writing, the disk interface reads a 4-byte word from memory in each DMA cycle. The memory cycle time is 40 nsec. Find the maximum percentage of time that the CPU gets blocked during DMA operation.



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Example 6

- A hard disk is connected to a 50 MHz processor through a DMA controller. Assume that the initial set-up time for a DMA transfer takes 2000 clock cycles for the processor, and also assume that the handling of the interrupt on DMA completion requires 1000 clock cycles for the processor. The hard disk has a transfer rate of 4000 KB/s and average block size transferred is 8 KB. What fraction of the processor time is consumed by the disk, assuming that data are transferred only during the idle cycles of the CPU?



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Example 7

- A device with transfer rate of 20 KB/s is connected to a CPU. Data is transferred byte wise. Let the interrupt overhead be 6 μ sec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt-driven mode?



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Lecture 51: BUS STANDARDS

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Introduction

- A bus is a collection of wires and connectors through which the data is transmitted.

The diagram illustrates a computer bus architecture. Three components—CPU, Memory, and Disk—are connected to a single horizontal bus line. The bus is labeled with four types of signals: Control ($C_0 - C_9$), Address ($A_0 - A_{31}$), Data ($D_0 - D_{63}$), and Power (GND, +3.3V, +/-5V, +/-12V).

- Bus = address bus + data bus
 - Data bus: transfers actual data.
 - Address bus: transfers information about data and where it should go.

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- Bus Protocol:
 - Rules determining the format and transmission of data through bus.
- Parallel Bus:
 - Data transmitted in parallel.
 - Advantage: It is fast.
 - Disadvantage: High cost for long distance communication, inter-line interference at high frequency.
- Serial Bus:
 - Data transmitted serially.
 - Advantage: low cost for long distance communication, no interference.
 - Disadvantage: Slow.



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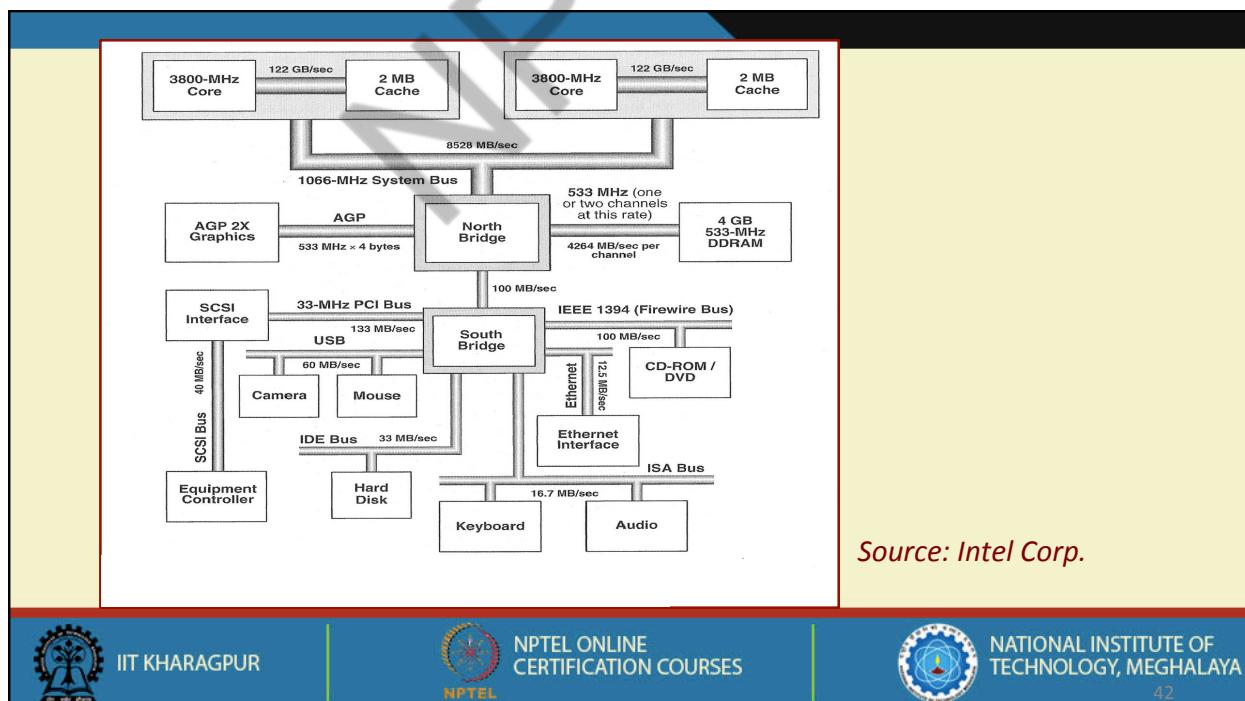
- Bus Master and Slaves:
 - The device that controls the bus is called master; others are slaves.
- Local or System Bus:
 - Bus that connects CPU and memory.
- Front-Side Bus:
 - Original concept: connects CPU to components.
 - Modern Intel architecture: connects CPU to NorthBridge chipset.
- Back-Side Bus:
 - Connects CPU to L2 cache.
- Memory Bus:
 - Connects NorthBridge chipset to memory.



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- AGP Bus:
 - Connects NorthBridge chipset to the GPU.
- ISA, PCI, Firewire, USB, PCI-Express Bus:
 - Connects motherboard to peripherals.



Some Features of a Bus

- Bus width:
 - Number of wires available in the bus for transferring data.
- Bus bandwidth:
 - Total amount of data that can be transferred over the bus per unit time.



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Bus	Width (bit)	Bandwidth (MB/s)
16-bit ISA	16	15.9
EISA	32	31.8
PCI	32	127.2
64-bit PCI 2.1 (66 MHz)	64	508.6
AGP 8x	32	2,133
USB 2	1	Slow-Speed: 1.5 Mbit/s Full-Speed: 12 Mbit/s Hi-Speed: 480 Mbit/s
Firewire 400	1	400 Mbit/s
PCI-Express 16x version 2	16	8,000



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Synchronous versus Asynchronous Bus

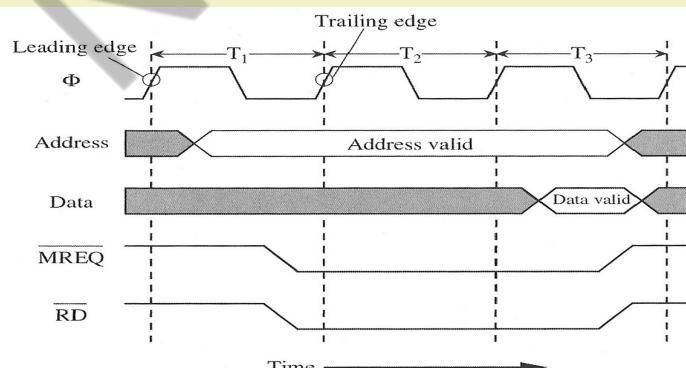
- Synchronous Bus:
 - There is a common clock between the sender and the receiver that synchronizes bus operation.
- Asynchronous Bus:
 - There is no common clock.
 - Bus master and slave have to *handshake* during the process of communication.



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Example 1: Synchronous Memory Read

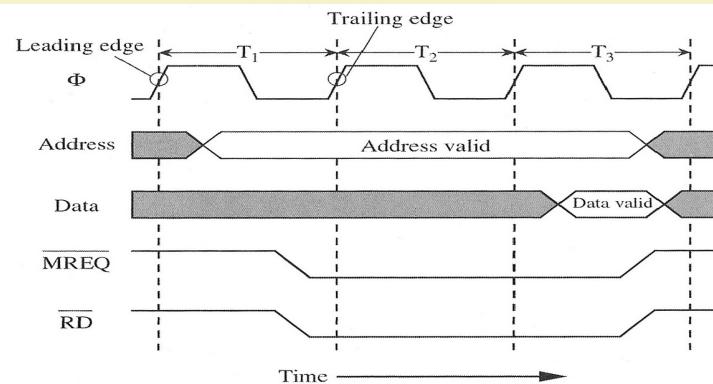


1. CPU places the address of the memory location on address lines



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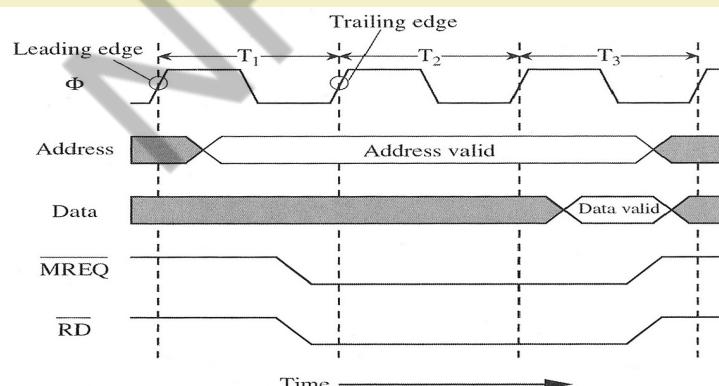
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2. After the voltages on the address line have become stable, CPU asserts MREQ and RD lines



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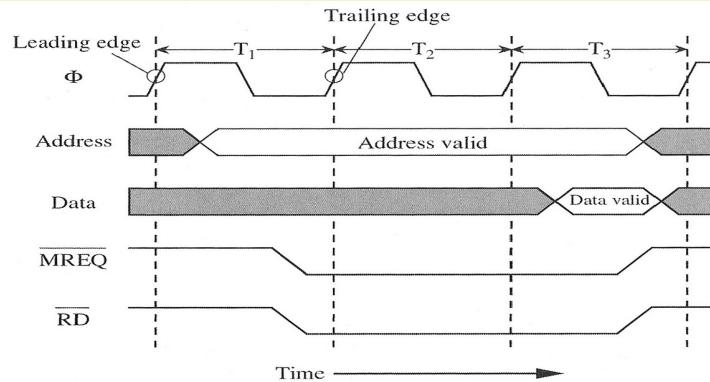
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3. Memory controller accesses memory location and loads the data on the data lines



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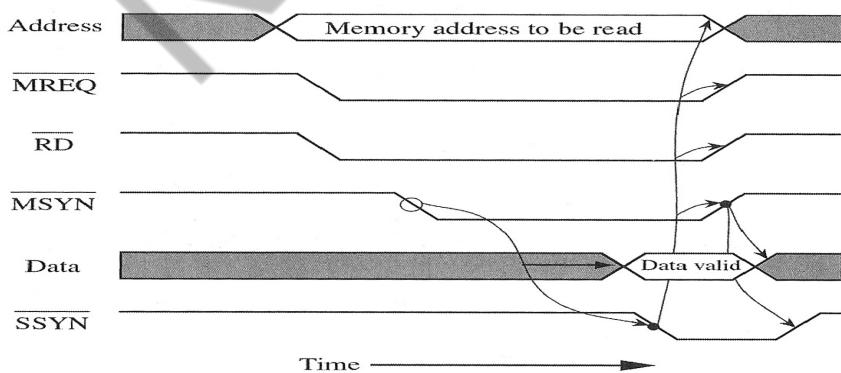
- CPU reads data from the data lines, and then de-asserts MREQ and RD to release the bus



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Example 2: Asynchronous Memory Read

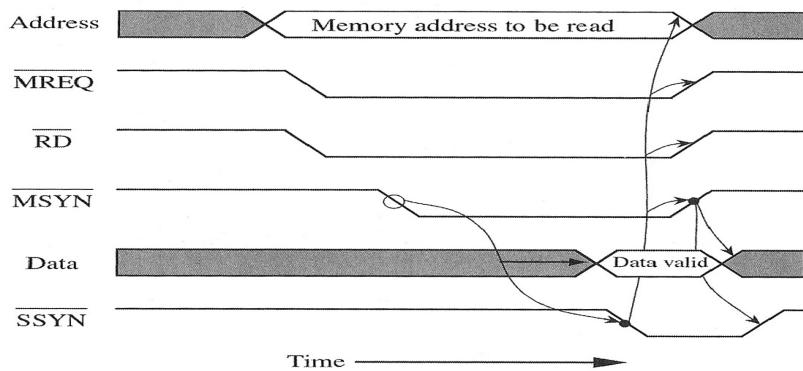


- CPU puts the address of the memory location on the address lines



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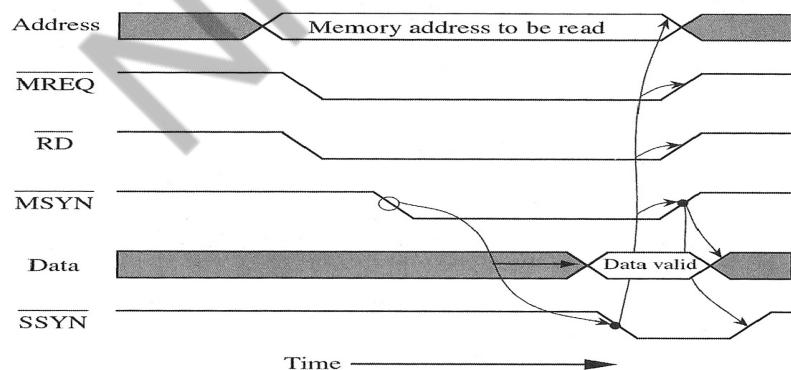
- After the voltages on the address line have become stable, CPU asserts MREQ and RD lines



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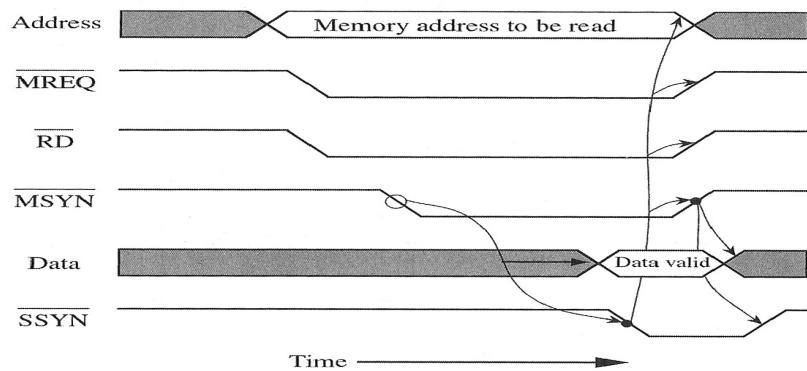
- CPU asserts the MSYN line. Memory controller accesses memory.



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4. Memory controller loads data from memory to data lines, and asserts SSYN.



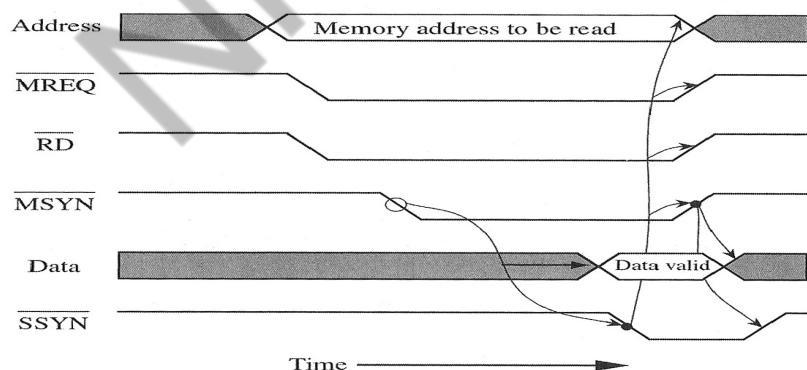
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5. CPU takes data from the data lines, and then de-asserts MREQ, RD and MSYN.



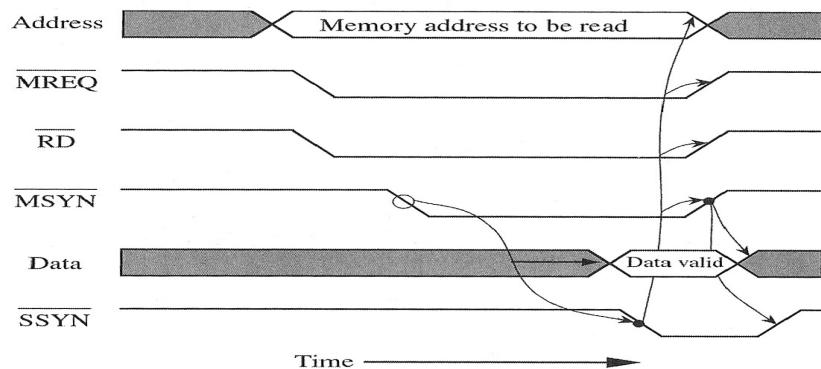
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6. Finally, memory controller de-asserts SSYN.



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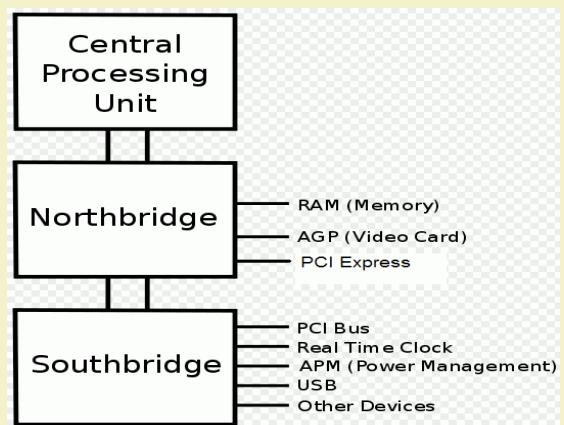
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Bridge-Based Bus Architectures

- System includes a lot of buses that are segregated by bridges.
- The advantage is that different buses can operate in parallel.
- Intel follows this kind of architecture.



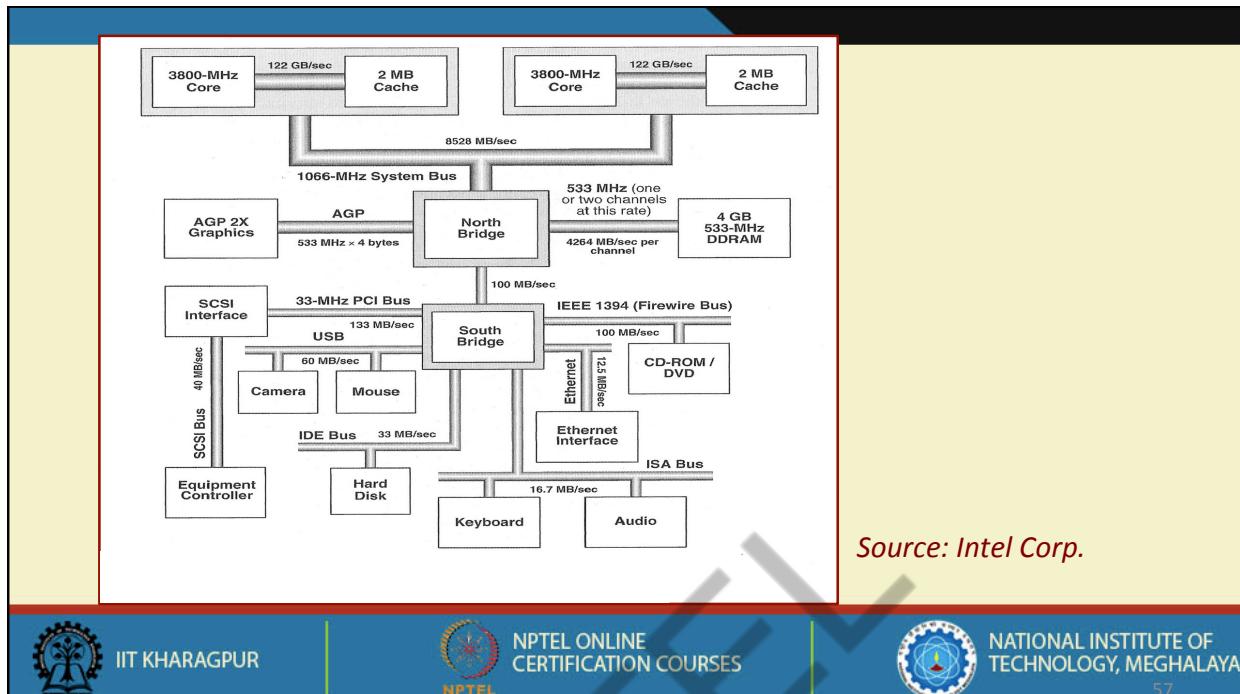
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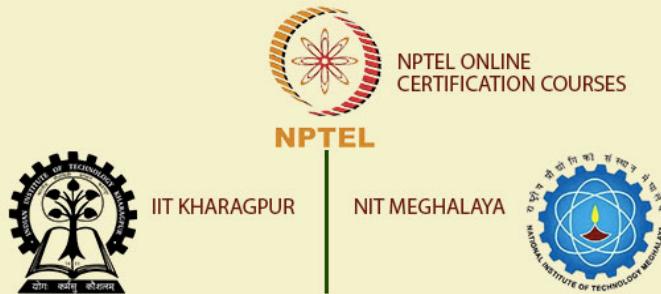
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Lecture 52: UNIVERSAL SERIAL BUS (USB)

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Universal Serial Bus (USB)

- USB is the most popular external bus standard in use today.
 - Allows connection of almost all types of peripheral devices.
 - USB interfaces exist today in keyboard, mouse, printer, scanner, mobile phones, disks, pen drives, camera, etc.
- Facilitates high-speed transfer of data.
 - USB 1.1 (1998): up to 12 Mbps
 - USB 2.0 (2000): up to 480 Mbps
 - USB 3.0 (2008): up to 5 Gbps
 - USB 3.1 (2013): up to 10 Gbps



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History of USB

- A group of 7 companies (Compaq, DEC, IBM, Intel, Microsoft, NEC, Nortel) initiated the development of the USB standard in 1994.
- Main Goal:
 - Simplify the problem of connecting external devices by replacing the variety of connectors that were available earlier.
 - Simplify software configuration of the connected devices.
- The first USB version 1.0 appeared in 1996, which was followed by many other generations, with USB 3.1 being the latest.



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- How are data transmitted?
 - Data are transmitted serially using differential NRZI encoding.

Bit to be sent	Previous line state	New line state
0	0	1
0	1	0
1	0	0
1	1	1

- Bit stuffing is used to ensure minimum bit toggle frequency during communication.
 - A 0 is inserted whenever a sequence of 6 1's is encountered.
 - 1101 1111 1101 0100 → 1101 1111 10101 0100



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USB Connectors

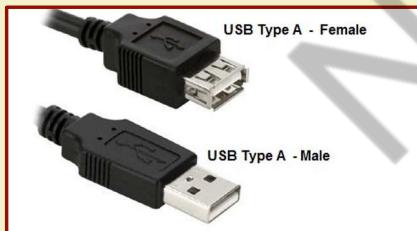
- There are two pre-defined connectors in any USB system.
 - The *Type-A plug* has an elongated cross-section, inserts into a Type-A receptacle on a downstream port on a USB host or hub, and carries both power and data.
 - The *Type-B plug* has a near square cross-section with the top exterior corners beveled. As part of a removable cable, it inserts into an upstream port on a device (e.g. printer).
- For connecting smaller devices like mobile phones and digital cameras, mini and micro USB connectors have also been developed.



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Type-A



Mini



Type-B



Micro

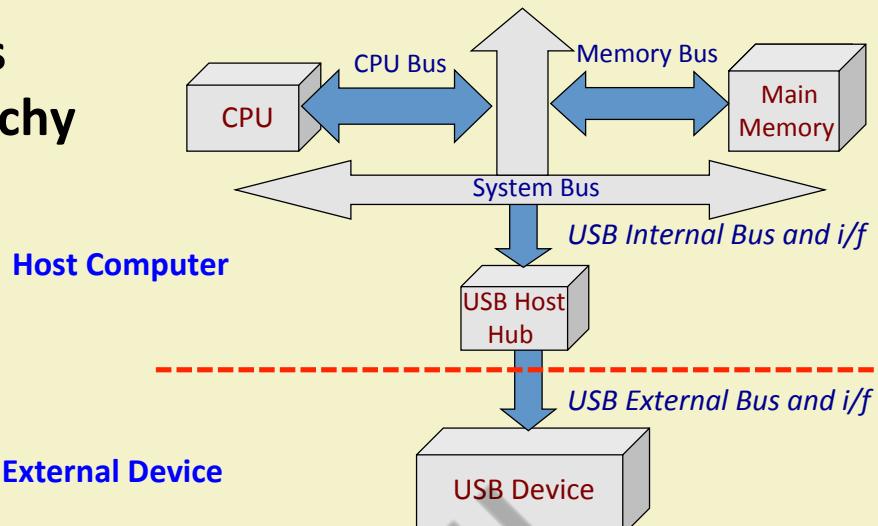


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Bus Hierarchy



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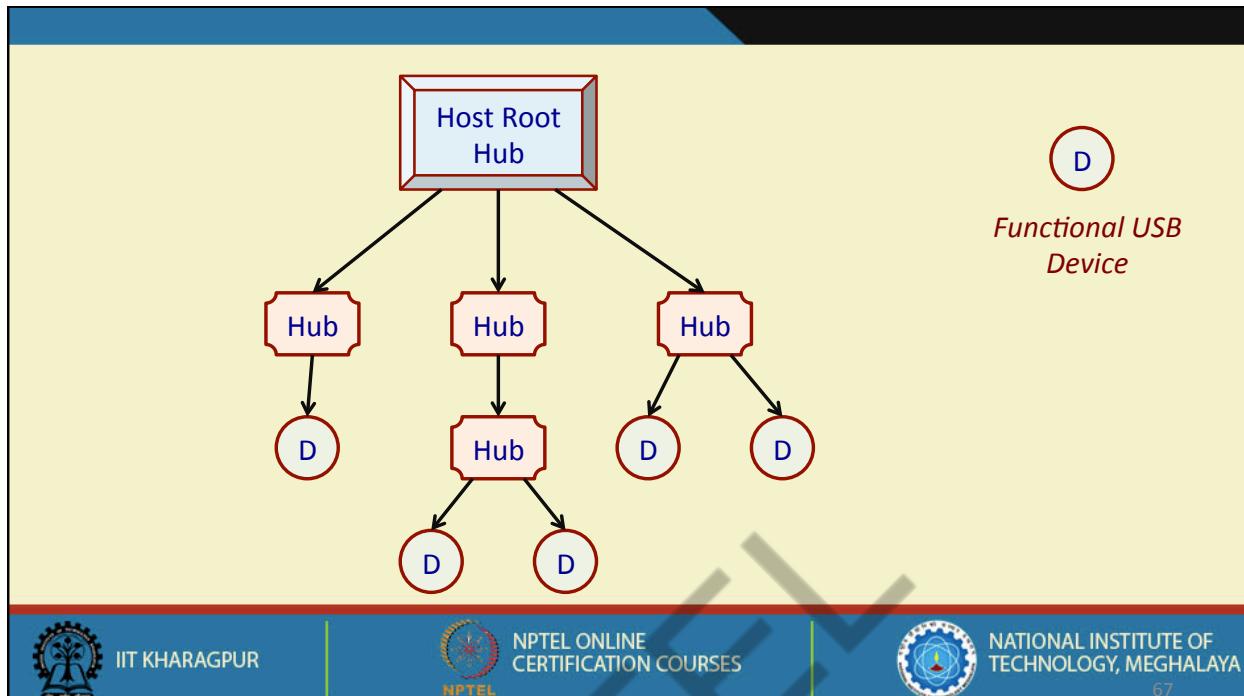
Bus Topology

- Connects computer (host) to peripheral devices.
 - Largely successful in replacing serial and parallel ports.
- Tiered Star Topology:
 - All devices are linked to a common point called the *root hub*.
 - The USB specification supports up to 127 different devices.
 - 4-wire cable is used to interconnect – power, ground, and two differential signaling lines.
 - USB is a polled bus – all transactions are initiated by the host.



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- **USB Host:**
 - It is a device that controls the entire system (usually a computer).
 - It processes data arriving to and from the USB port.
 - It contains a sophisticated set of software drivers.
 - Drivers schedule and compose USB transactions.
 - Access individual devices to obtain configuration information.
 - Software dependence of USB systems make it difficult to use on stand-alone systems (with no OS support).
 - The physical interface to ***USB Root Hub*** is called the ***USB Host Controller***.



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- USB Hub:
 - It checks for new devices and maintains status information of child devices.
 - It serves as *repeater*, boosting strength of upstream and downstream signals.
 - It *electrically isolates* devices from one another, thus allowing an expanded number of devices.
 - Allows malfunctioning devices to be removed.
 - Allows slower devices to be placed on a faster branch.
 - Can be purchased as stand-alone devices.



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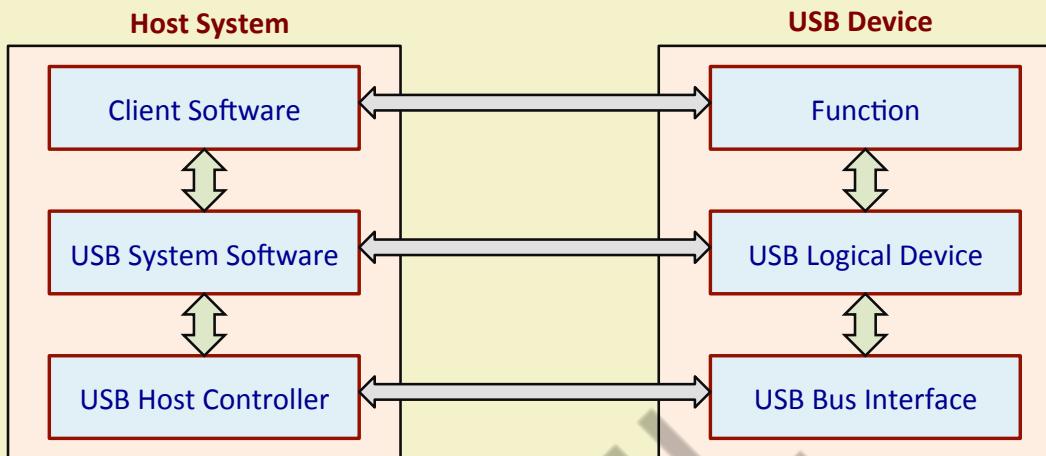
- USB Devices:
 - All functional USB devices are *slaves*; only responding to data reads or writes, never initiating any.
 - May indicate a need to transmit or receive data through polling.
 - Contain registers that identify relevant configuration information.
 - Exist in conjunction with corresponding set of software drivers inside the host system.



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USB Software Interfaces



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- The **Client Software** determines what transactions are required with a given device.
 - What data is to be transferred?
- Scheduling and configuration of data transfers are completed in **USB System Software** level.
 - When and how often data is to be transferred?
- Data transfers are composed and regulated at the **USB Host Controller** level.
 - How are data to appear to the functional device?
 - How does system keep track of data sent and received?



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Future of USB

- USB Type-C Plug:
 - They are about the same size as micro USB connectors.
 - Can deliver power output of 20 volts and 5 amps (100 watts).
 - Can be used for charging laptops and phones.
- Thunderbolt 3 port uses the same port type as USB-C.
 - Peak speed up to 40 Gbps.
 - Available on Apple machines.



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END OF LECTURE 52



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