ANSWER KEY

Name of Examination	**Final Assessment Test (FAT), Fall 2019-20 Semester, (NOV 2019)**		
Slot: G2	Course Mode: **CBL / PBL / RBL**	**Class Number (s):** 0616	

Course Code:	CSE2001	Course Title:	COMPUTER ARCHITECTURE AND ORGANIZATION	
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1. The processor A, B C and D has a 2 GHz clock frequency. Find the total execution time for the programme with instruction mix given below. If the CPI of arithmetic instruction was doubled what would be the impact on the execution time of all the processors.

Processors	Instruction mix / Processor			CPI		
	Arithmetic	Load / Store	Branch	Arithmetic	Load / Store	Branch
A	2560	1280	256	1	4	2
B	1280	640	128	1	4	2
C	640	320	64	1	4	2
D	320	160	32	1	4	2

Find the total execution time for this program on A, B, C & D processors. Assume that each processor has a 2 GHz clock frequency. If the CPI of arithmetic instructions was doubled, what would the impact be on the execution time of the program on A, B, C & D processors?

ANS: i) Total execution time:
A = 4.096 µs, B = 2.048 µs, C = 1.024 µs, D = 0.512 µs
ii) Execution time after CPI been doubled
A = 5.376 µs, B = 2.688 µs, C = 1.344 µs, D = 0.672 µs

2. Calculate M multiplied by Q using Booth's Algorithm where M = -11 and Q = 27.

ANS:

n	A	Q	Q_0	Comments
6	000000	011011	0	Initial Values
5	001011 000101	011011 101101	0 1	A<- A-M Arithmetic Shift Right

4	000010	110110	1	Arithmetic Shift Right
3	110111 111011	110110 111011	1 0	A<-A+M Arithmetic Shift Right
2	000110 000011	111011 011101	0 1	A<- A-M Arithmetic Shift Right
1	000001	101110	1	Arithmetic Shift Right
0	110110 111011	101110 010111	1 0	A<-A+M Arithmetic Shift Right

3. Write a program to evaluate the expression X= (A+B)*(C/D) with one address, two address and three address Instructions.

   ANS:

ONE ADDRESS	TWO ADDRESS	THREE ADDRESS
LOAD A	MOV T, A	ADD X, A, B
ADD B	ADD T, B	DIV T, C, D
STORE T	MOV S, C	MUL X, X, T
LOAD C	DIV S, D	
DIV D	MUL T, S	
MUL T	MOV X, T	
STORE X		

4. A. Give a block diagram for a 8M X 32 memory using 512K X 8 RAM chips.

   ANS:

   - 16 rows (of four 512×8 chips) are needed.
   - Address lines A18−0 are connected to all chips.
   - Address lines A22−19 are connected to a 4-bit decoder to select one of the 16 rows.

   B. Multiply the numbers $(0.5)_{10}$ and $(-0.4375)_{10}$ using binary floating point multiplication.

   ANS: $(1.000 \times 2^{-1}) \times (-1.110 \times 2^{-2})$
   $= -1.110 \times 2^{-3}$

5. The following is a list of 32-bit memory address references, given as word addresses of 8-bit each. 1, 134, 212, 1, 135, 213, 162, 161, 2, 44, 41, 221. For the above references, identify the binary address and the index address given a direct-mapped cache with initially 2-word blocks and a total size of blocks. Assuming the cache to be empty initially, list the hit or miss for cache references.

ANS: i) Binary Address: 00000001, 10000110, 11010100, 00000001, 10000111, 11010101, 10100010, 10100001, 00000010, 00101100, 00101001, 11011101

ii) Index: Binary address mod 16

iii) Hit/Miss: M, M, M, H, M, M, M, M, M, M, M, M.

6. Consider a two level memory hierarchy of the form (L1, L2) where L1 is connected directly to the CPU. Determine the average cost per bit and average access time for the data given below.

Level	Capacity	Cost	Access time	Hit ratio
L1	1024	0.1000	10^{-8}	0.9000
L2	2^{16}	0.0100	10^{-6}	-

ANS:

Average Cost (C) = $(C_1S_1 + C_2S_2) / (S_1 + S_2)$

$= ((0.1 \text{ X } 1024) + (0.01 \text{ X } 2^{16})) / (1024 + 2^{16})$

$= 0.011384615$

Average access time

$T_A = hT_{A1} + (1 - h) T_{A2}$

$= 0.9000 \text{ X } 10^{-8} + (1 - 0.9000) \text{ X } 10^{-6}$

$= 1.09 \text{ X } 10^{-7}$

7. It is necessary to transfer 512 words from a backup store to a memory section starting from address 1000 and the transfer is by means of DMA. i) What are the initial values that the CPU must transfer to the DMA controller. ii) Give step by step account of the actions taken during the input of the first two words.

ANS:

i) CPU initiates DMA by Transferring: 512 to the word count register. 1000 to the DMA address register. Bits to the control register to specify a write operation.

ii) 1. I/O device sends a "DMA request".
2. DMA sends BR (bus request) to CPU.
3. CPU responds with a BG (bus grant).
4. Contents of DMA address register are placed in address bus.
5. DMA sends "DMA acknowledge" to I/O device and enables the write control line to memory.
6. Data word is placed on data bus by I/O device.
7. Increment DMA address register by 1 and Decrement DMA word count register by 1.

8. Repeat steps 4-7 for each data word Transferred.

8. List and explain the levels of RAID. What is the distinction between parallel access and independent access in context of RAID?

ANS:
RAID Level 0: Non-Redundant
RAID Level 1: Mirrored
RAID Level 2: Redundancy through hamming code
RAID Level 3: Bit-interleaved parity
RAID Level 4: Block level parity
RAID Level 5: Block-level distributed parity

9. Assume a pipeline with four stages: fetch instruction (FI), decode instruction and calculate addresses (DA), fetch operand (FO), and execute (EX). Draw a diagram for a sequence of 7 instructions, in which the third instruction is a branch that is taken and in which there are no data dependencies.

ANS:

	1	2	3	4	5	6	7	8	9	10
I1	FI	DA	FO	EX						
I2		FI	DA	FO	EX					
I3			FI	DA	FO	EX				
I4				FI	DA	FO				
I5					FI	DA				
I6						FI				
I7							FI	DA	FO	EX

10. A. Discuss the difference between tightly coupled multiprocessors and loosely coupled multiprocessors from the viewpoint of hardware organization and programming techniques.

ANS:

Tightly coupled multiprocessors require that all processed in the system have access to a common global memory. In loosely coupled multiprocessors, the memory is distributed and a mechanism is required to provide message-passing between the processors. Tightly coupled systems are easier to program since no special steps are required to make shared data available to two or more processors. A loosely coupled system required that sharing of data be implemented by the messages.

B. What is the use of parity bits in an error correction code? How many check bits are needed if the Hamming error correction code is used to detect single bit errors in a 2048-bit data word?

ANS: Need K check bits such that $2048 + K \leq 2^K - 1$.

The minimum value of K that satisfies this condition is 12.