Cache Coherence Problem

The Cache Coherence Problem

- Caches in multiprocessing environment introduce the cache coherence problem.
- When multiple processors maintain locally cached copies of a unique-shared memory location, any local modification of the location can result in globally inconsistent view of memory.
- Cache coherence protocols prevent this problem by maintaining a uniform state for each cached block of data.

Causes of Cache Inconsistency

- Cache inconsistency only occurs when there are multiple caches capable of storing (potentially modified) copies of the same objects.
- There are three frequent sources of this problem:
  - Sharing of writable data
  - Process migration
  - I/O activity

Inconsistency in Data Sharing

- Suppose two processors each use (read) a data item X from a shared memory. Then each processor's cache will have a copy of X that is consistent with the shared memory copy.
- Now suppose one processor modifies X (to X'). Now that processor's cache is inconsistent with the other processor's cache and the shared memory.
- With a write-through cache, the shared memory copy will be made consistent, but the other processor still has an inconsistent value (X).
- With a write-back cache, the shared memory copy will be updated eventually, when the block containing X (actually X') is replaced or invalidated.

Inconsistency After Process Migration

- If a process accesses variable X (resulting in it being placed in the processor cache), and is then moved to a different processor and modifies X (to X’), then the caches on the two processors are inconsistent.
- This problem exists regardless of whether write-through caches or write-back caches are used

Inconsistency Caused by I/O

- Data movement from an I/O device to a shared primary memory usually does not cause cached copies of data to be updated.
- As a result, an input operation that writes X causes it to become inconsistent with a cached value of X.
- Likewise, writing data to an I/O device usually use the data in the shared primary memory, ignoring any potential cached data with different values.

Cache Coherence Protocols

- Snoopy protocols
- MSI Protocols
- MESI Protocols
- MOSI Protocols
- MOESI Protocols
- MERSI Protocol
- MESIF Protocol
- Write-once Protocol
- Firefly Protocol
- Dragon Protocol