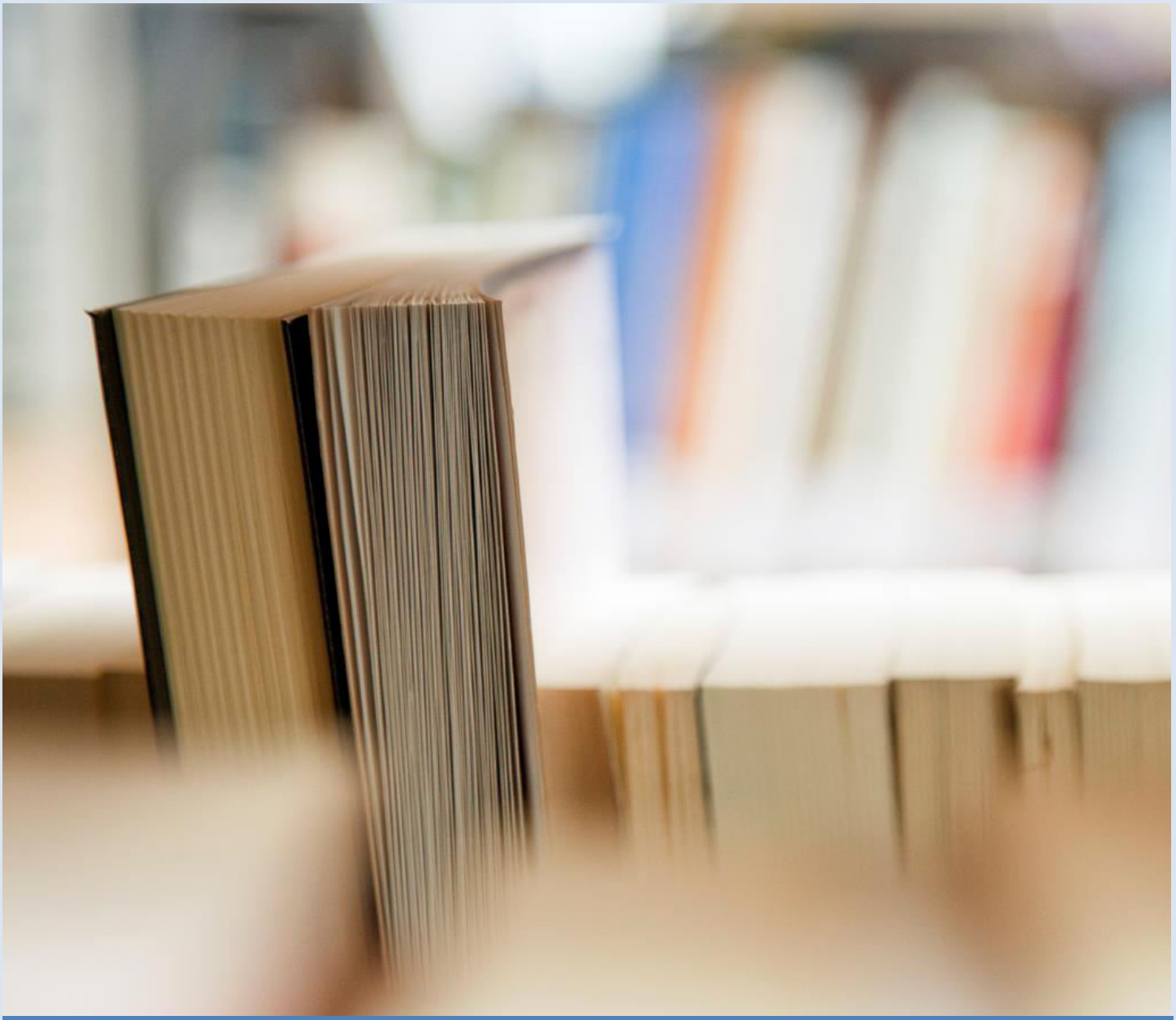


Digital Logic Gates &Boolean Algebra

Experiment – 1 & 2

Bimal Parajuli (20BDS0405)

6/12/21

CSE 1003 - LAB

DIGITAL LOGIC DESIGN

Exp # 1 - DIGITAL LOGIC GATES

OBJECTIVE:

- To study the basic logic gates: AND, OR, INVERT, NAND, and NOR.
- To study the representation of these functions by truth tables, logic diagrams and Boolean algebra.
- To observe the pulse response of logic gates.
- To measure the propagation delay of logic gates.

APPARATUS:

- IC Type 7400 Quadruple 2-input NAND gates
- IC Type 7402 Quadruple 2-input NOR gates
- IC Type 7404 Hex Inverters
- IC Type 7408 Quadruple 2-input AND gates
- IC Type 7432 Quadruple 2-input OR gates
- IC Type 7486 Quadruple 2-input XOR gate
- IC Type 7493 4-bit ripple counter
- Digi-Designer Logic Board
- Dual-trace oscilloscope

THEORY:

AND A multi-input circuit in which the output is 1 only if all inputs are 1.The symbolic representation of the AND gate is shown in Fig. 1a.

OR A multi-input circuit in which the output is 1 when any input is 1. The symbolic representation of the OR gate is shown in Fig. 1b.

INVERT The output is 0 when the input is 1, and the output is 1 when the input is 0. The symbolic representation of an inverter is shown in Fig. 1c.

NAND AND followed by INVERT. The symbolic representation of the NAND gate is shown in Fig 1d.

NOR OR followed by INVERT as shown in Fig 1e.

EX-OR The output of the Exclusive –OR gate, is 0 when it's two inputs are the same and it's output is 1 when its two inputs are different.

Truth Table Representation of the output logic levels of a logic circuit for every possible combination of levels of the inputs. This is best done by means of a systematic tabulation.

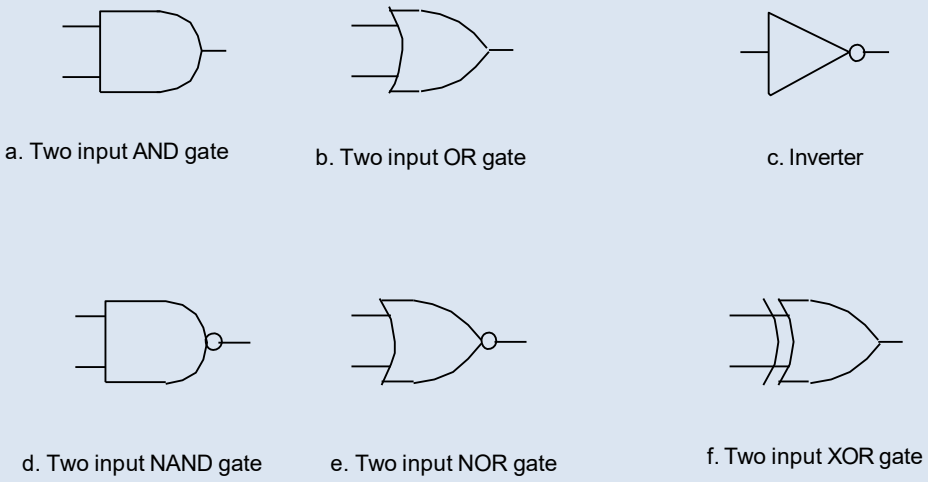
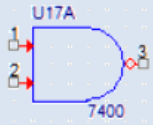


Fig.1 Symbols for digital logic gates

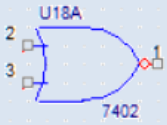
Part 1: Logic Functions

Exercises:

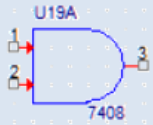
1. **Use one gate for each IC 7400 (NAND), 7402 (NOR), 7408 (AND), 7432 (OR), 7486 (XOR). Each has input pins, 1 and 2, and output pin 3.**



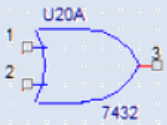
7400 (NAND gate)



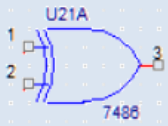
7402 (NOR gate)



7408 (AND gate)

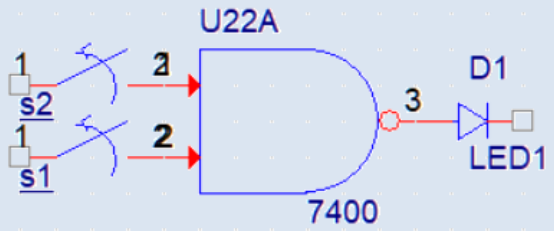


7432 (OR gate)



7486 (XOR gate)

2. **Connect pin 1 to switch S1-1, pin 2 to switch S1-2, and pin 3 to LED-1 for every gate as shown in Fig 2 as an example for the NAND gate.**



7400 (NAND gate) connected to switches and LED

3. Simulation and Truth Table of AND, OR, NAND, NOR and XOR gates:

- **AND gate**:

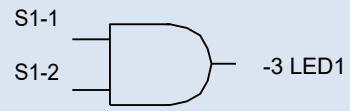
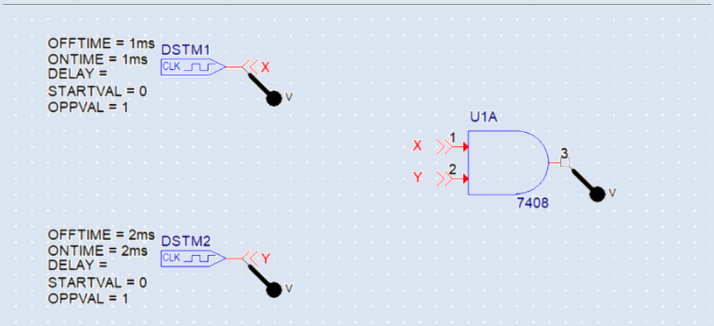
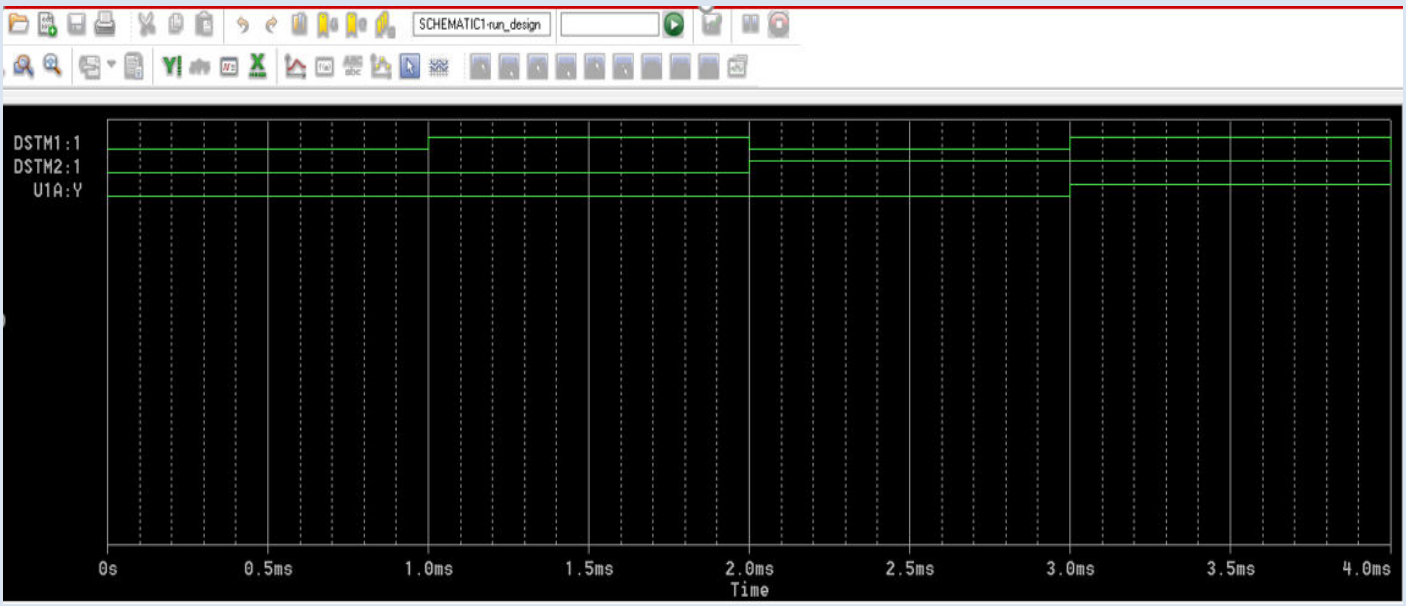


Fig.2 Two input AND gate





Observation:

Truth table of AND gate

Pin1(A)	Pin2 (B)	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

❖ **OR gate**:

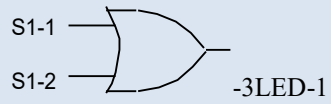
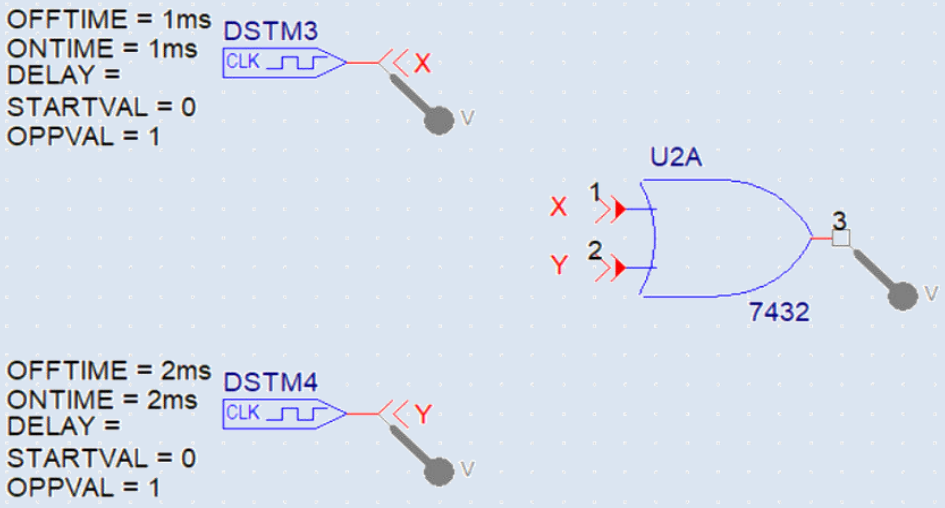
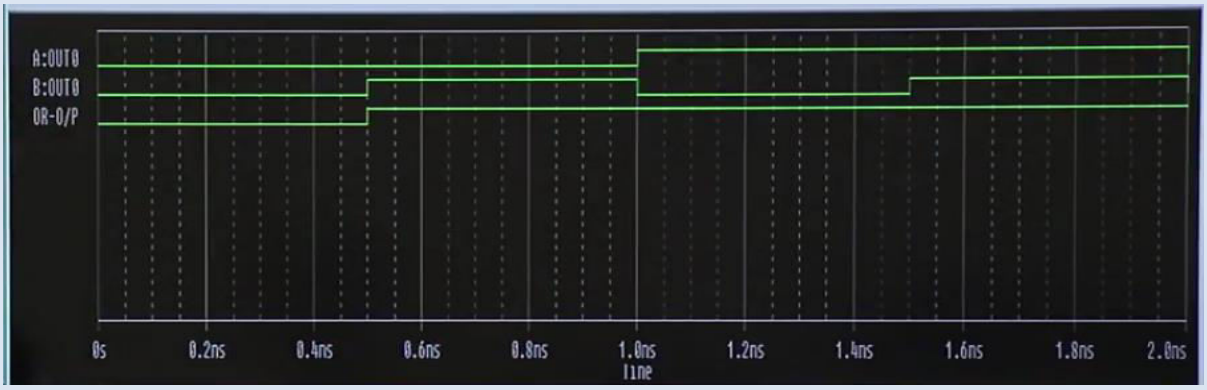


Fig.2 Two input OR gate





Observation:

Truth table of OR gate

Pin1(A)	Pin2 (B)	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

❖ **NAND gate**:

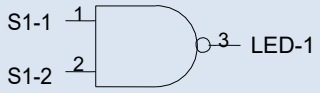
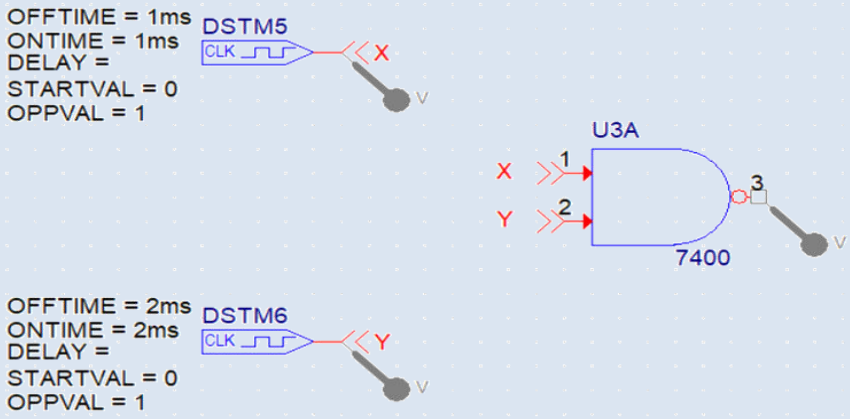
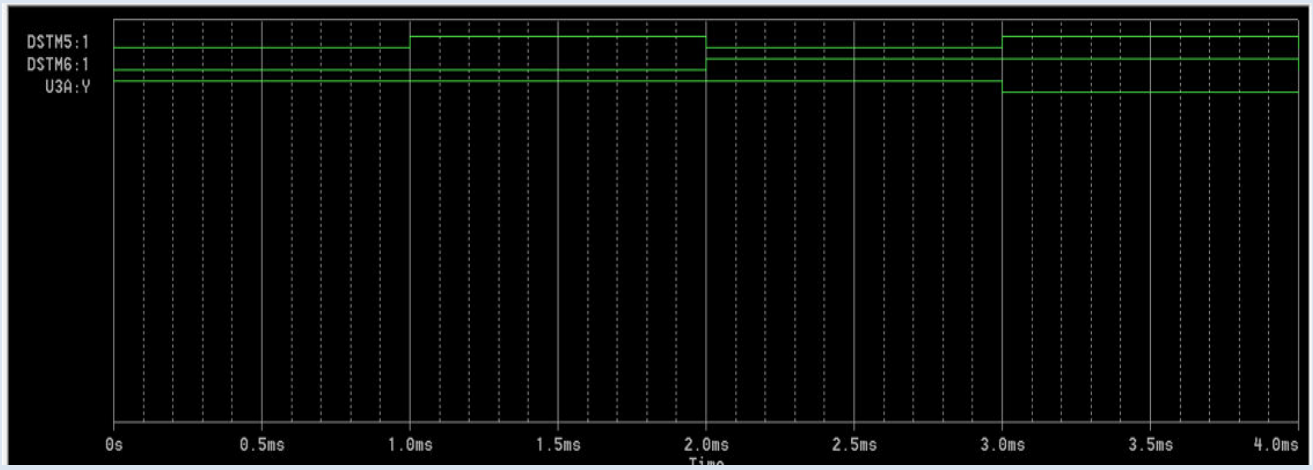


Fig.2 Two input NAND gate





Observation:

Truth table of NAND gate

Pin1(A)	Pin2 (B)	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

❖ **NOR gate:**

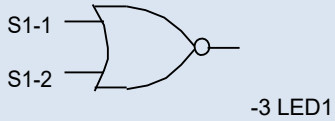
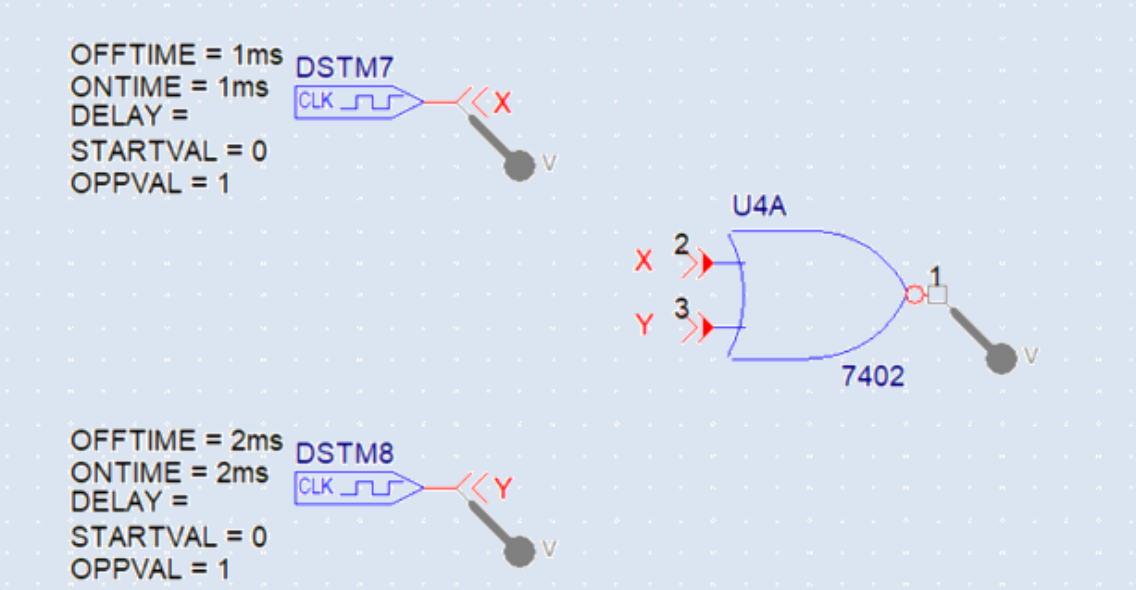


Fig.2 Two input NOR gate



Observation:

Truth table of NOR gate

Pin1(A)	Pin2 (B)	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

❖ **XOR gate:**

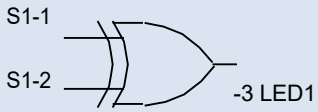
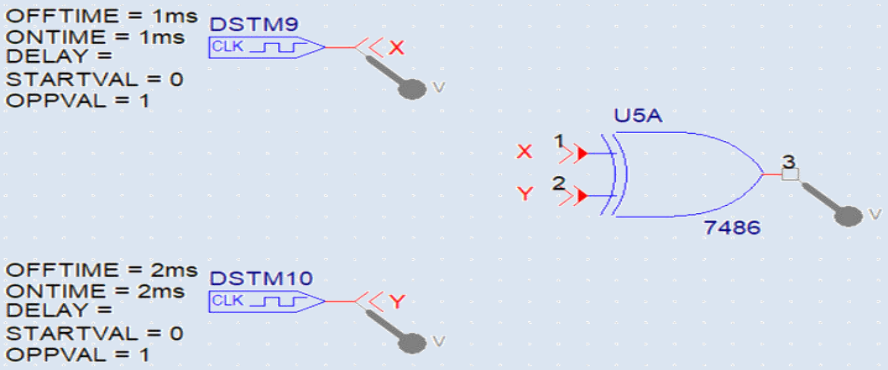
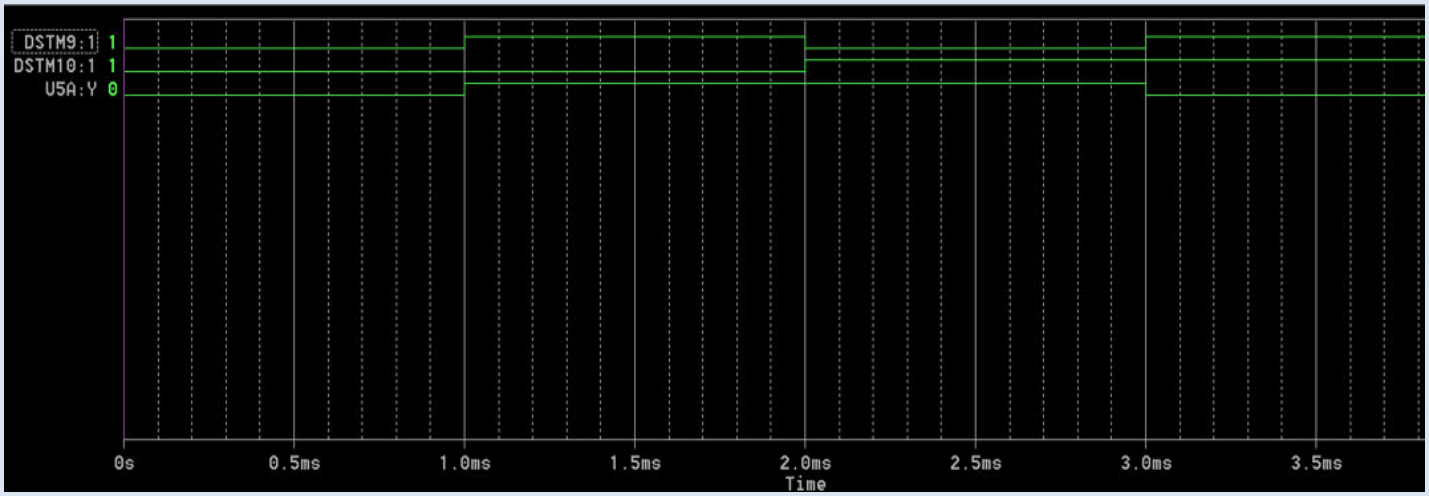


Fig.2 Two input XOR gate



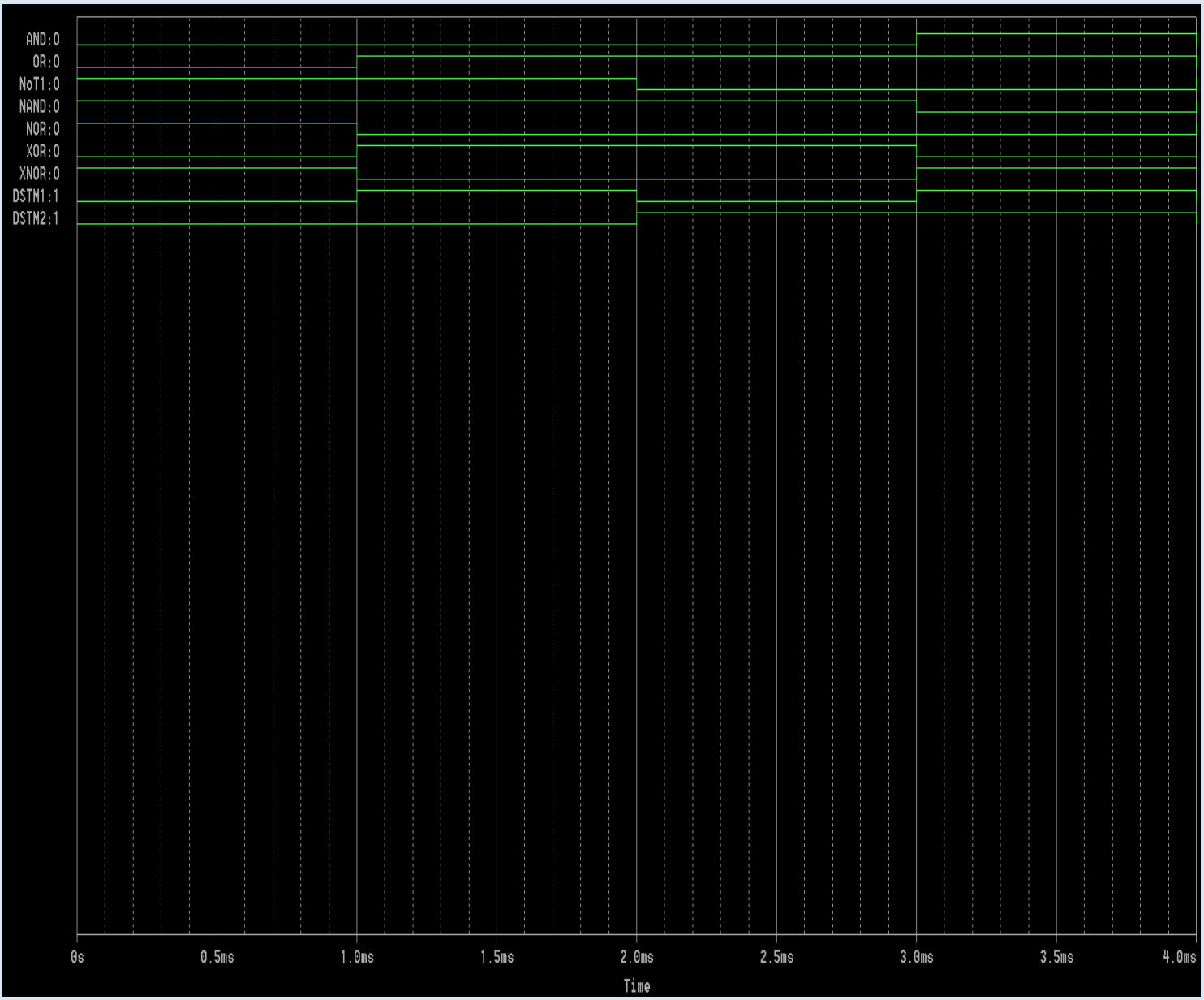


Observation:

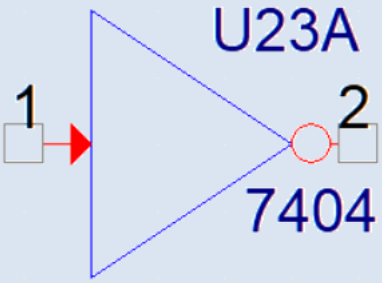
Truth table of XOR gate

Pin1(A)	Pin2 (B)	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

SIMULATION OF ALL GATES:



4. **Use an inverter gate from IC 7404 whose input pin is pin 1 and whose output pin is pin 2.**



IC7404 (NOT gate)

Observation:

Truth Table of NOT gate

Pin 1	Pin 2
0	1
1	2

Part-2: Response of Logic Gates:

Connect the circuits of figures 4 and 5 and write the corresponding truth tables 3 and 4, respectively.

A.

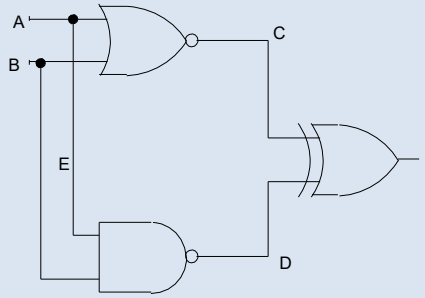
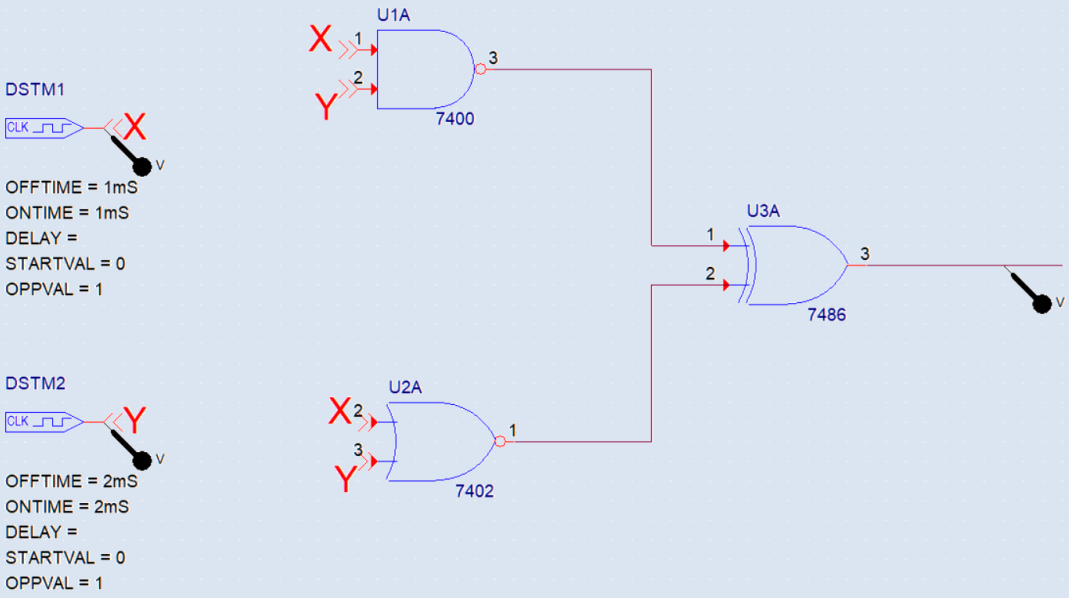
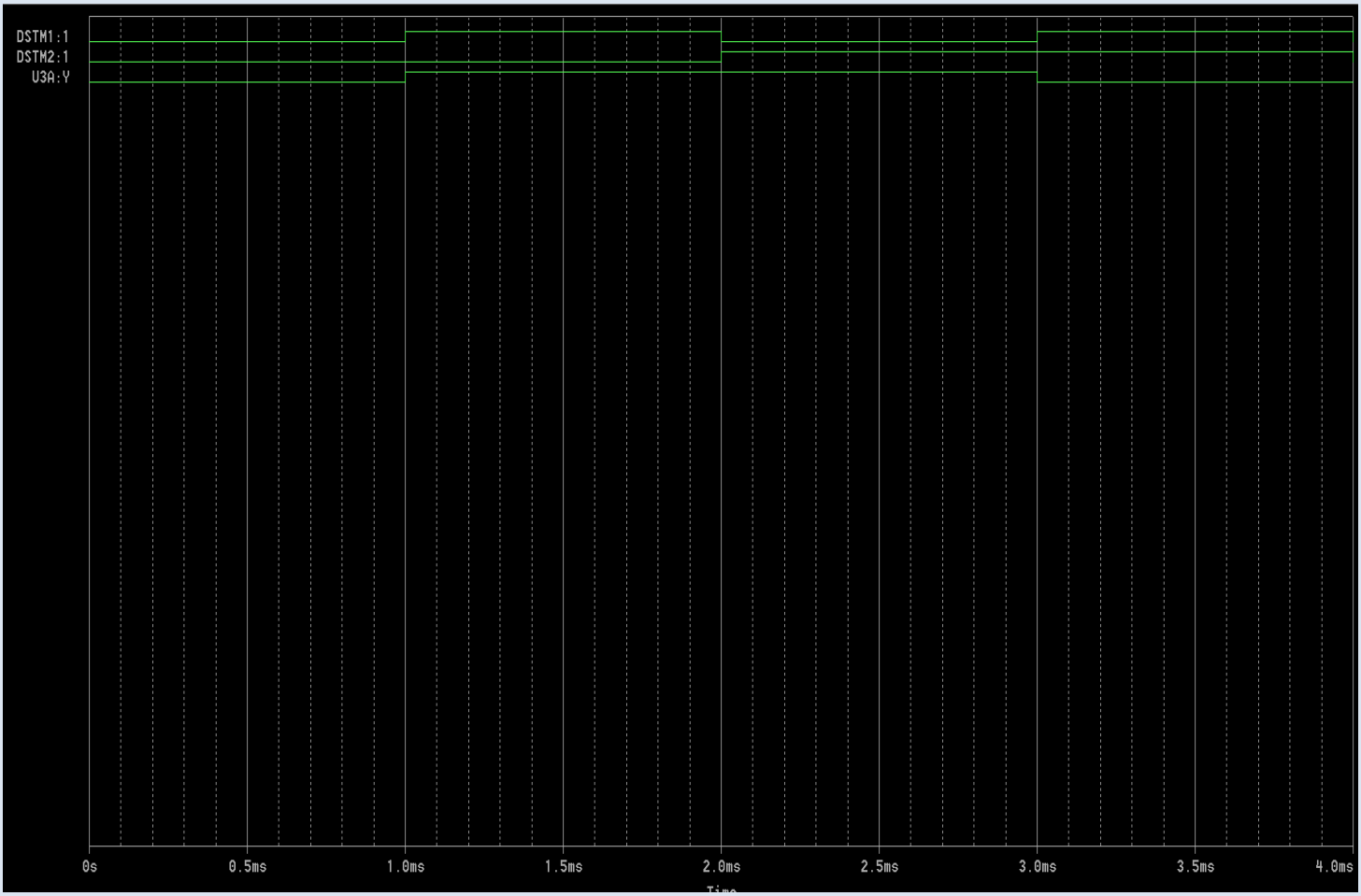


Fig. 4

Fig1:





A	B	C	D	E
0	0	1	1	0
0	1	0	1	1
1	0	0	1	1
1	1	0	0	0

B.

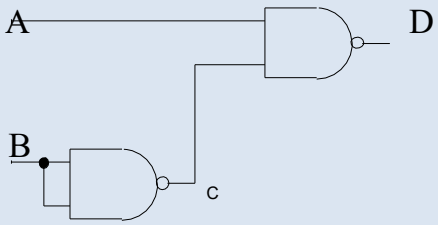
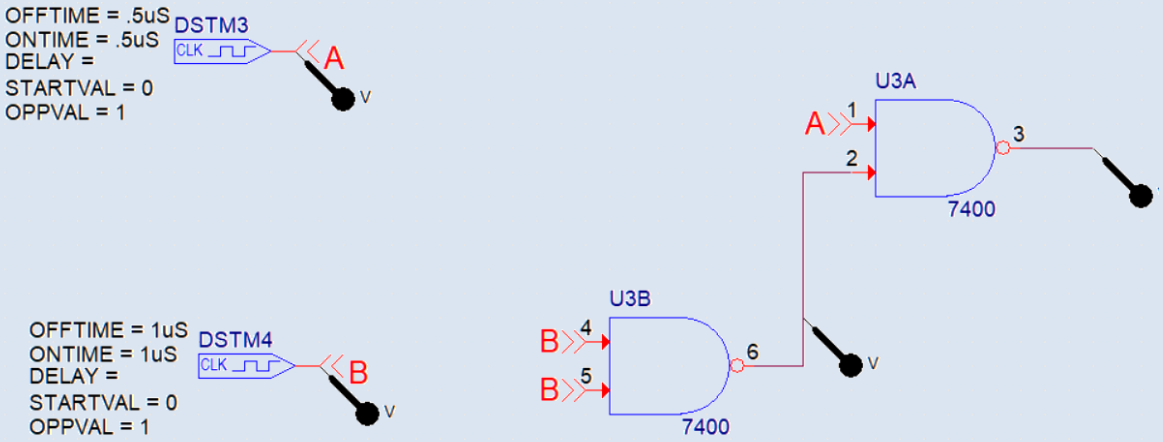
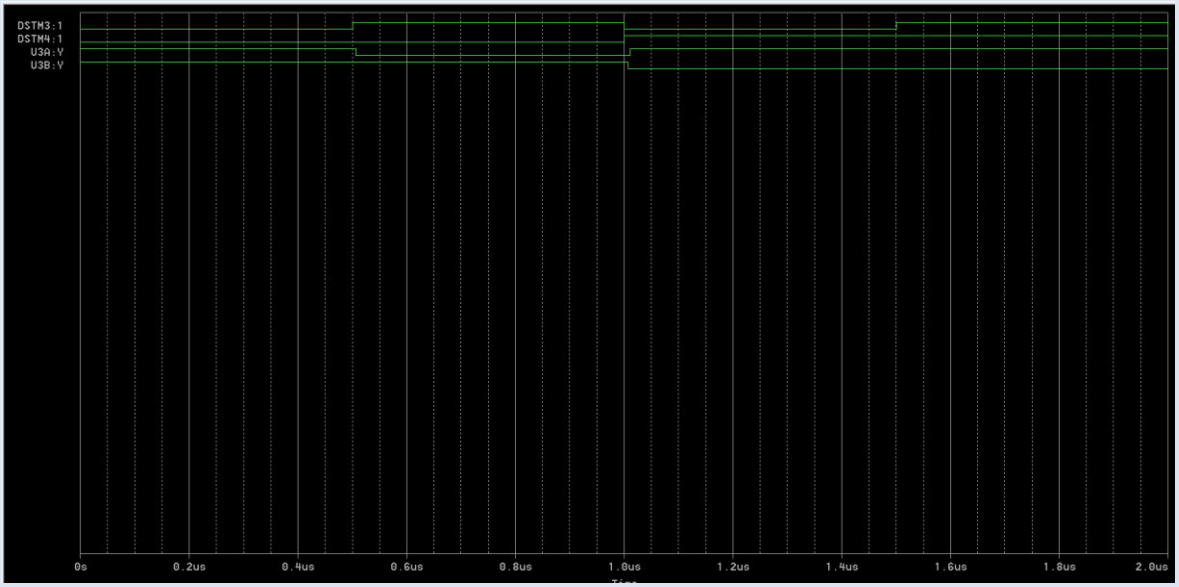


Fig: 5





Truth Table:

A	B	C	D
0	0	1	1
0	1	1	1
1	0	1	0
1	1	0	0

Part-3:

Propagation Delay in Logic Gates:

Connect all inverters inside two 7404 ICs in cascade. The output will be the same as the input except that it will be delayed by the time it takes the signal to propagate through all six inverters. Set S2 to 100 kHz and apply clock pulses to the input of the first inverter (connect pin 1 to j14) record the wave forms and determine the time delay from the input to the sixth inverter. This is done with a dual trace oscilloscope by applying the input clock pulses to one of the channels and the output of the sixth inverter to the second channel and measuring the delay between the two signals as shown in Fig 6. By using measured delay between two signals calculate the propagation delay for each inverter gate.

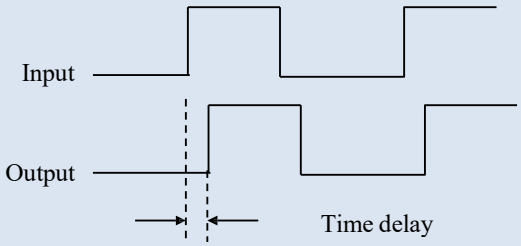
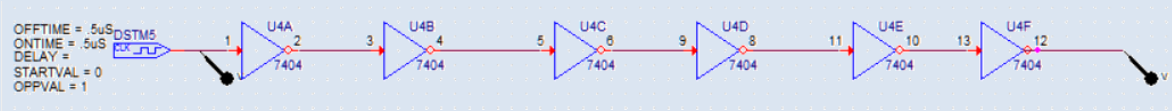
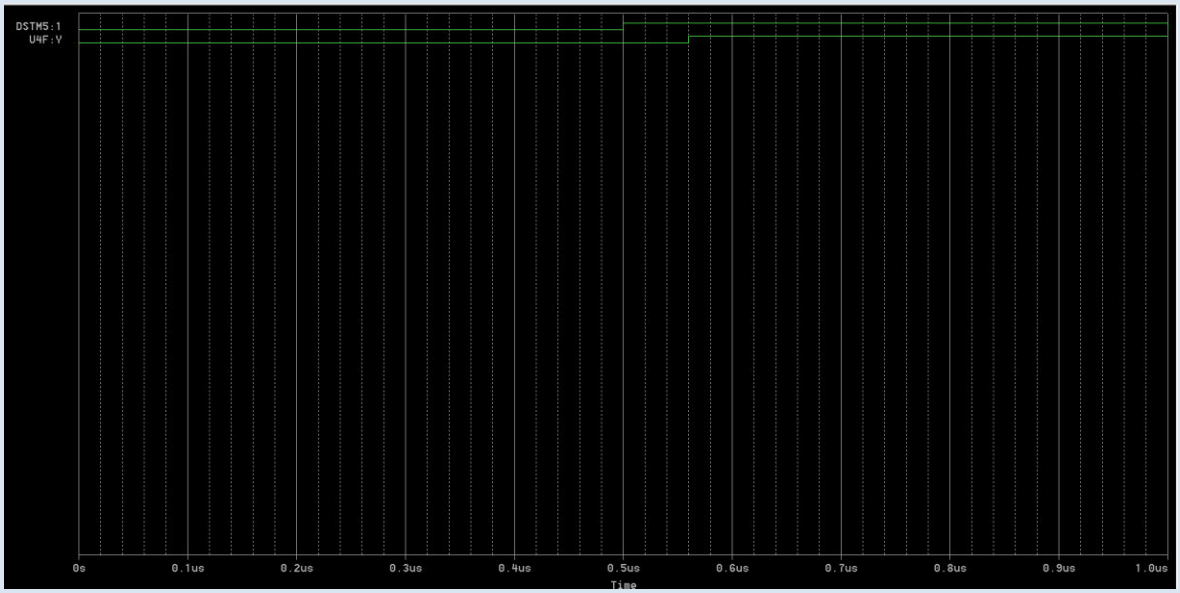


Fig. 6 Propagation delay





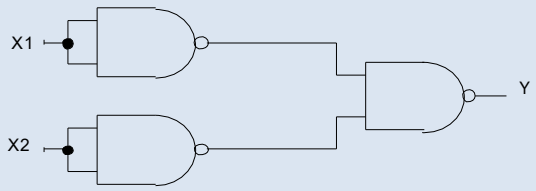
Inferences:

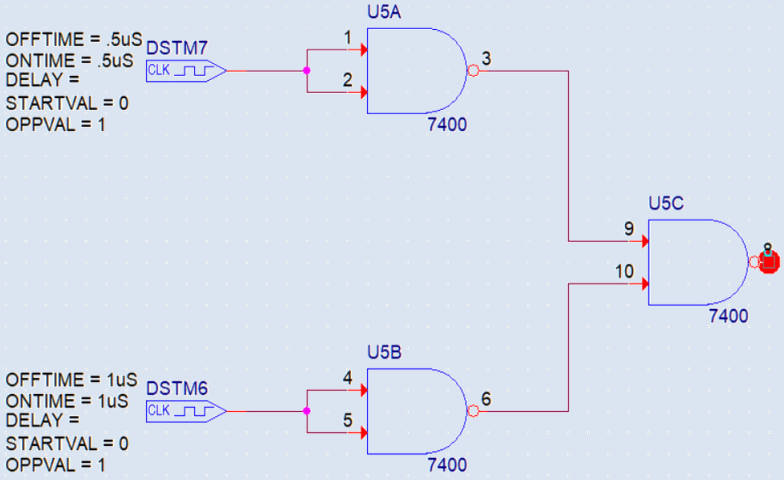
Here, we can see that the signal shifted causing a time delay of 0.06 microseconds between the input and the output signal through the series of NOT gates.

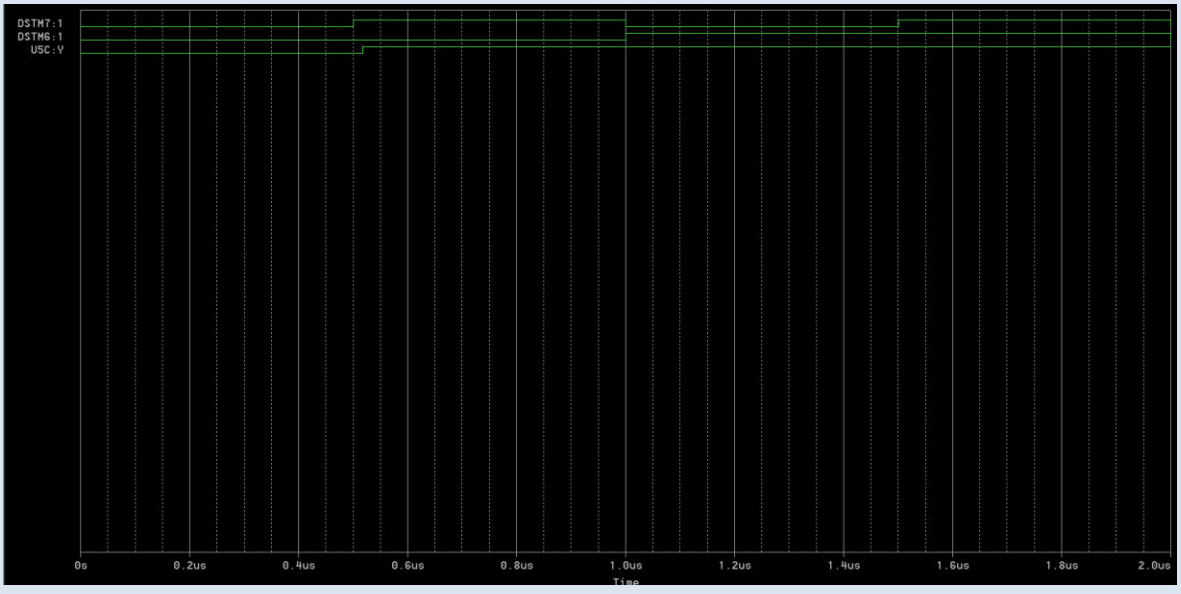
Part 4: Review Questions:

1. Write a truth table for each circuit. Derive Boolean expressions for all outputs.

A.





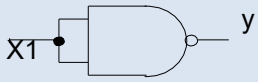


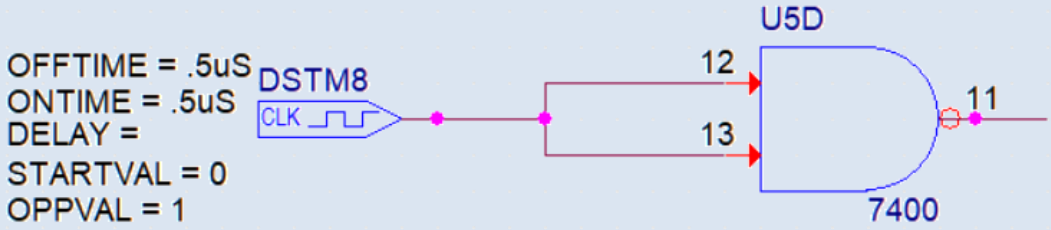
The truth table for above circuit is:

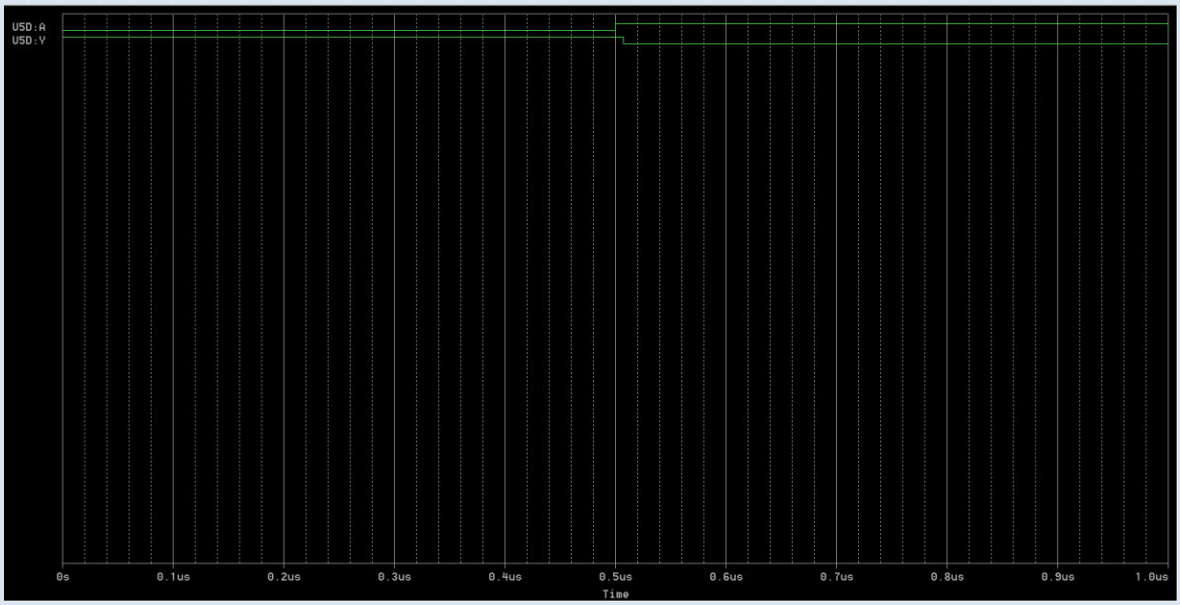
X1	X2	Y
0	0	0
0	1	1
1	0	1
1	1	1

The Boolean expression in POS (product of sums) form would be: Y = X1+ X2

B.

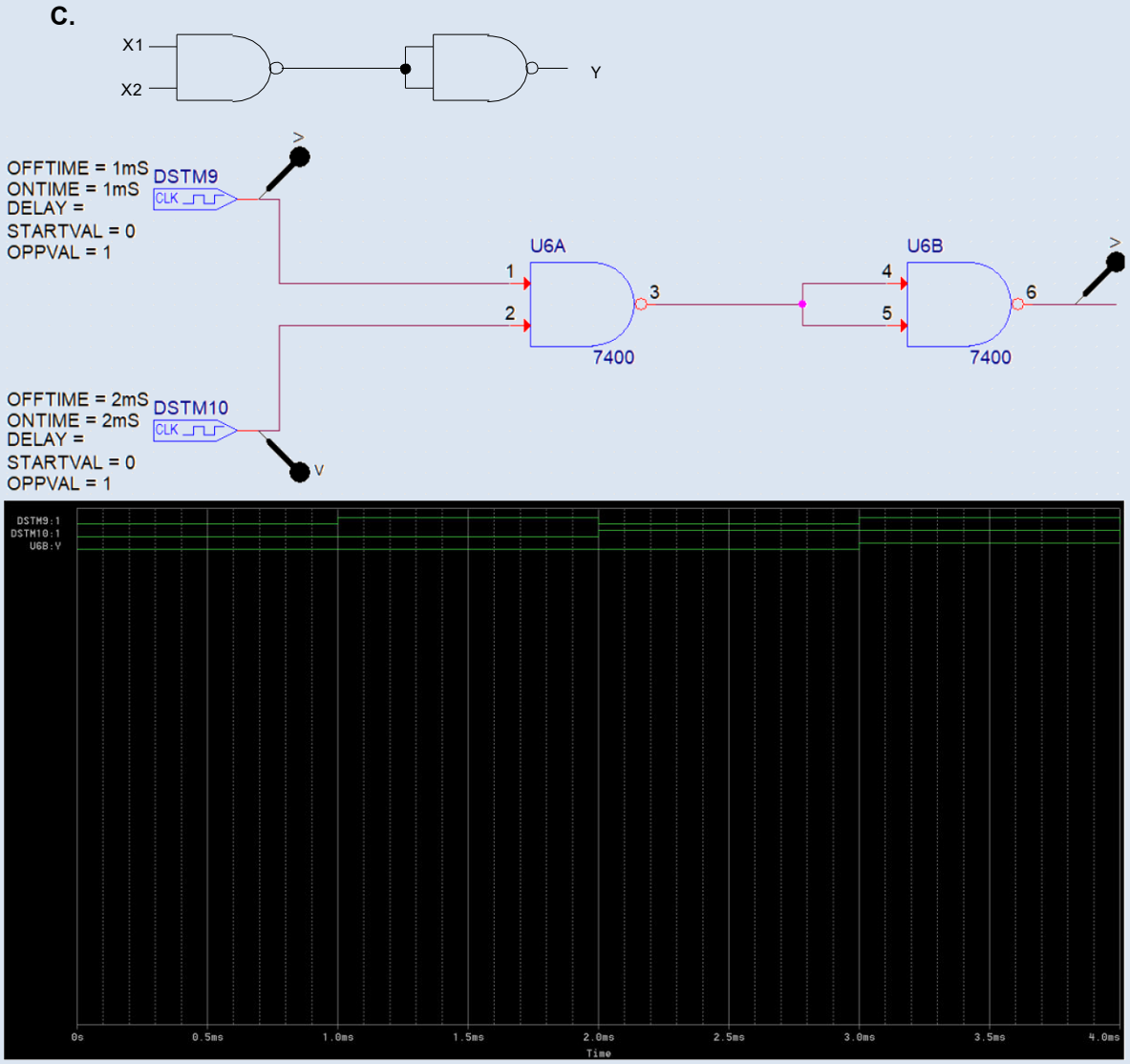






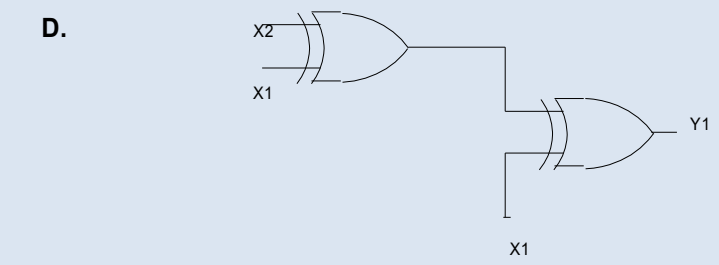
The Boolean expression for the above circuit will be:
Y = X1'

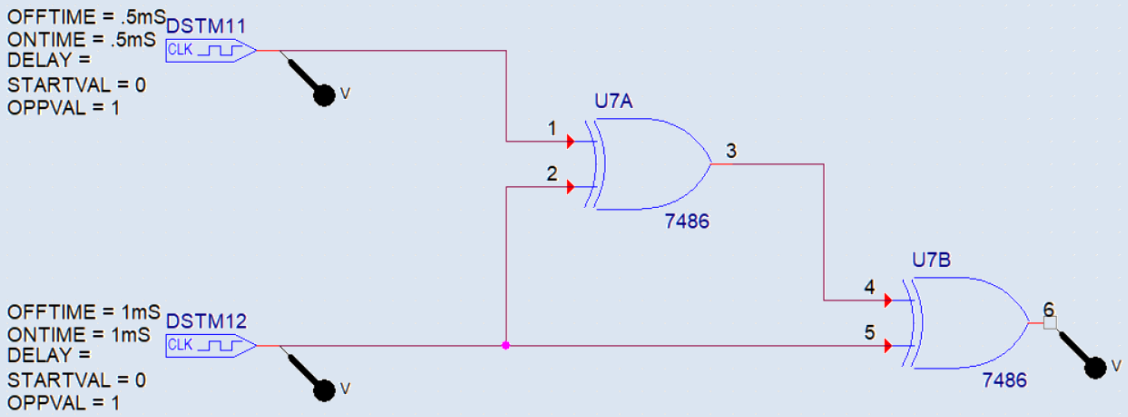
C.

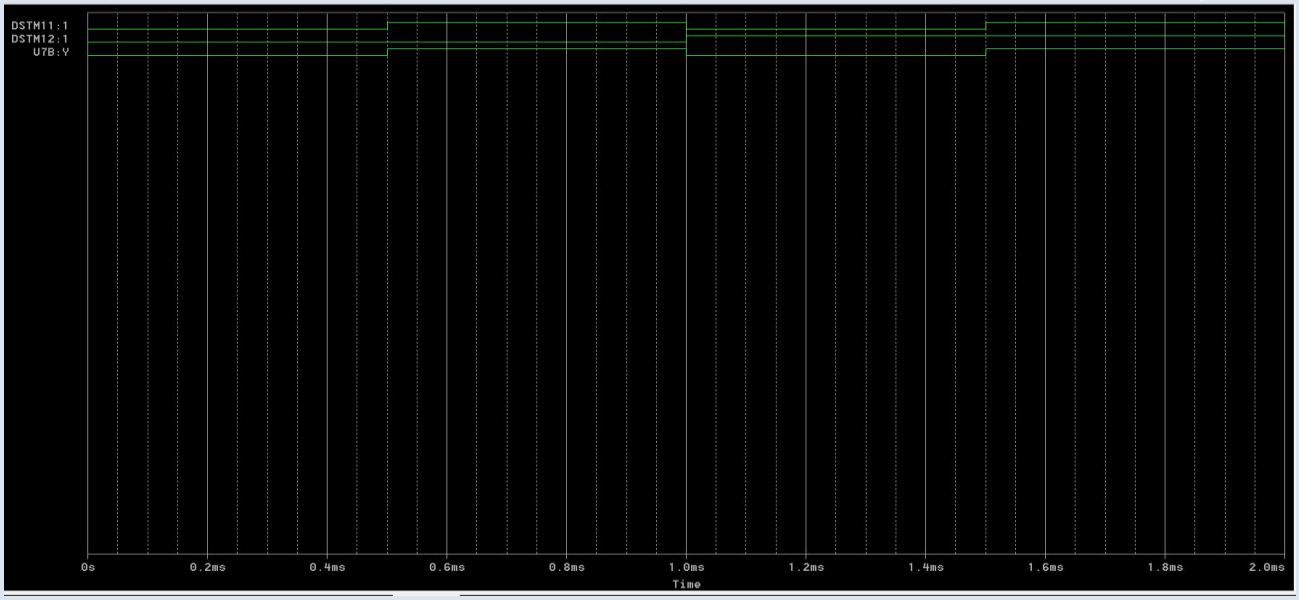


The Boolean expression of the given function is:
Y = X1 and X2

D.



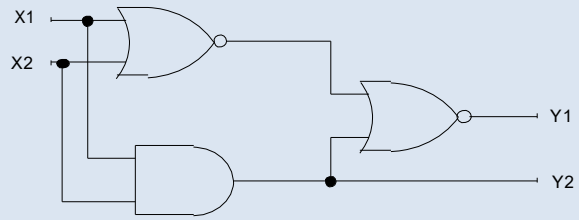


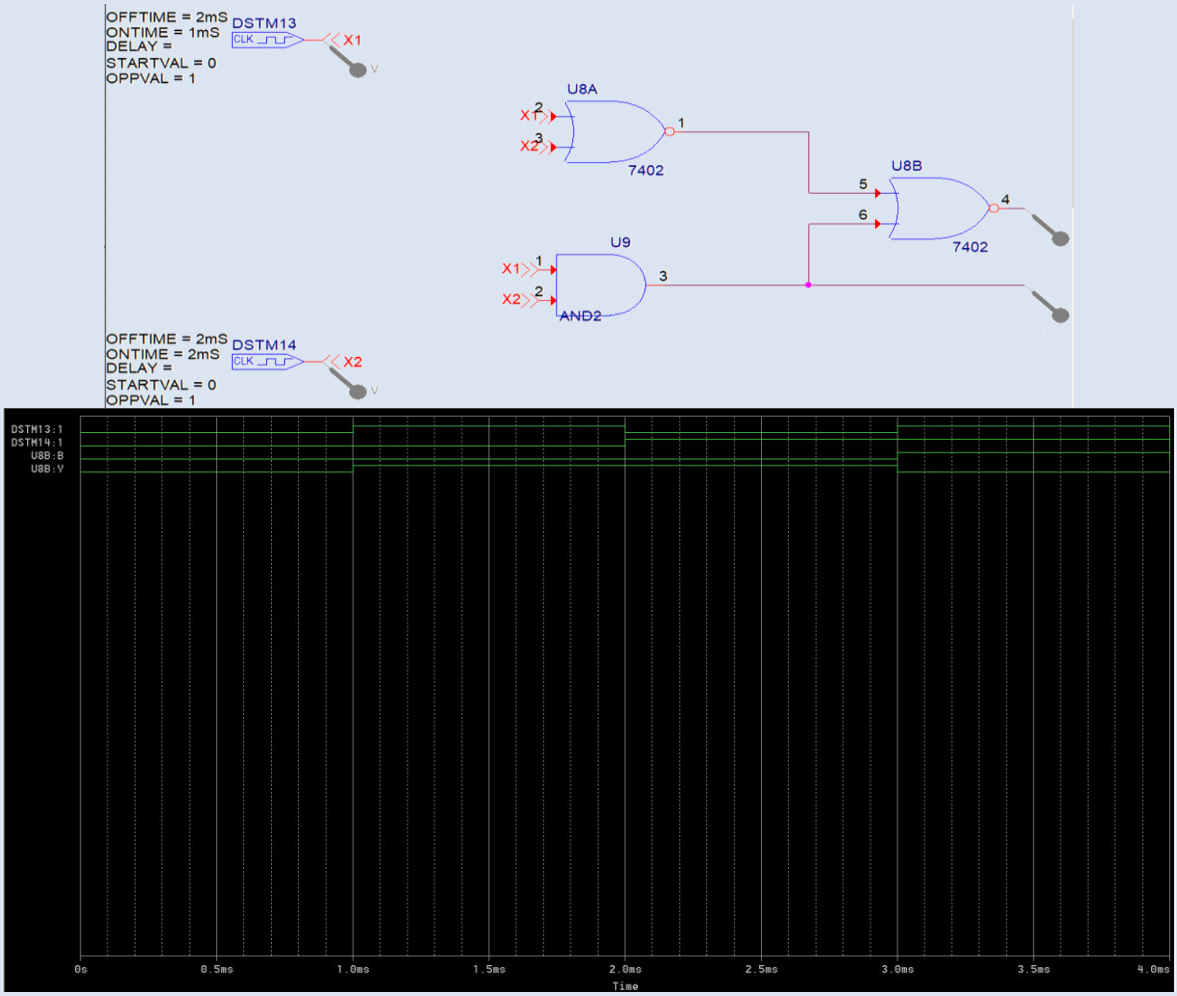


The Boolean expression is:

Y= X2

E.





The Boolean expressions of above circuit are:
Y1= X1 and X2
Y2= X1 XOR X2

2. A burglar alarm for a car has a normally low switch on each of four doors. If any door is opened the output of that switch goes HIGH. The alarm is set off with an active-LOW output signal. What type of gate will provide this logic? Support your answer with an explanation.

Answer:

For the above stated purpose of burglar's alarm, OR gate would best serve the purpose.

It is because in OR gate, the output will be high even if anyone among multiple inputs is set high. Seeing this in context of Car's Burglar alarm, the alarm should go high if at least one or many among the four doors are closed.

The truth table of OR gate for 4 inputs is:

A	B	C	D	A +B+C+D
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Clearly, it can be seen that the output is high for all cases except when all inputs are low. Thus, the alarm will stay quiet when all doors are closed. For any other condition, it will make noise.

Hence, OR gate is best fit for the alarm.

EE 200 DIGITAL LOGIC CIRCUIT DESIGN EXPERIMENT #4

BOOLEAN ALGEBRA

OBJECTIVE:

- To verify the rules and regulations of Boolean Algebra
- To simplify and modify Boolean logic functions by means of Demorgan's theorem.
- To design and implement a logic circuit.

APPARATUS:

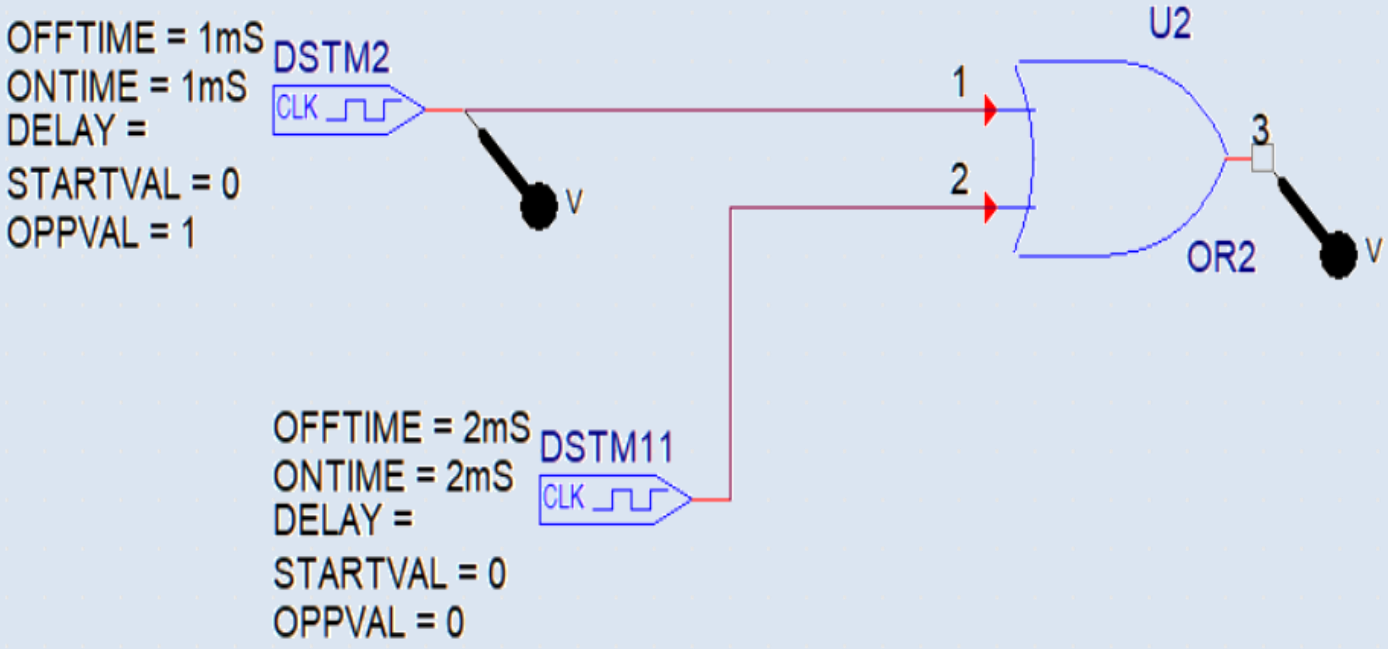
- PB-503
- 7400 Quadruple 2 input NAND gates.
- 7402 Quadruple 2 input NOR gates
- 7408 Quadruple 2 input AND gates
- 7432 Quadruple 2 input OR gates
- 7404 Hex inverters
- 7411 Triple 3-input AND gate

THEORY:

1. A+0 = A
2. A+1 = 1
3. A .0 = 0
4. A .1 = A
5. A+A = A
6. A+A' = 1
7. A.A = A
8. A.A' = 0
9. (A')' = A
10. A+AB = A
11. A+A'B = A+B
12. (A+B). (A+C) = A+BC
13. A'. B' = (A+B)'
14. A'+B' = (A.B)'

Procedure 1:

a. Prove rule 1 using OrCAD.



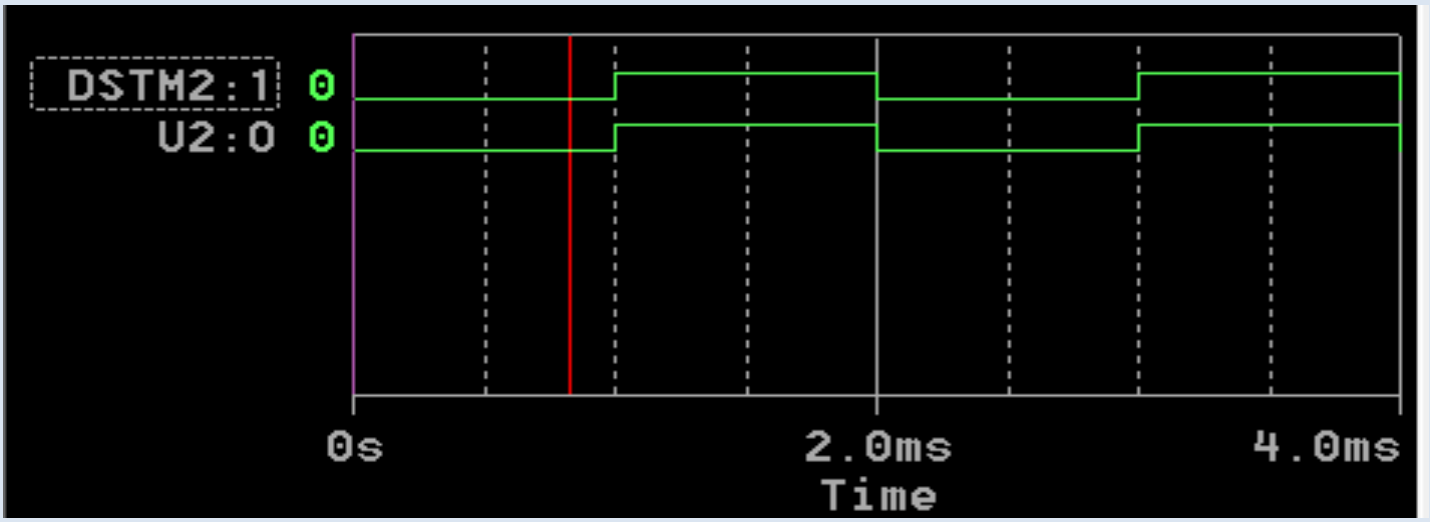


Fig.1 Verifying Rule 1

b. Connect the circuit of Fig.2 Using OrCAD. Which rule does this circuit illustrate?

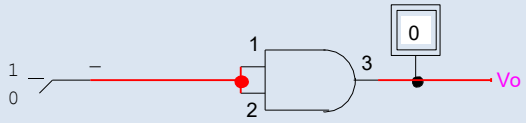
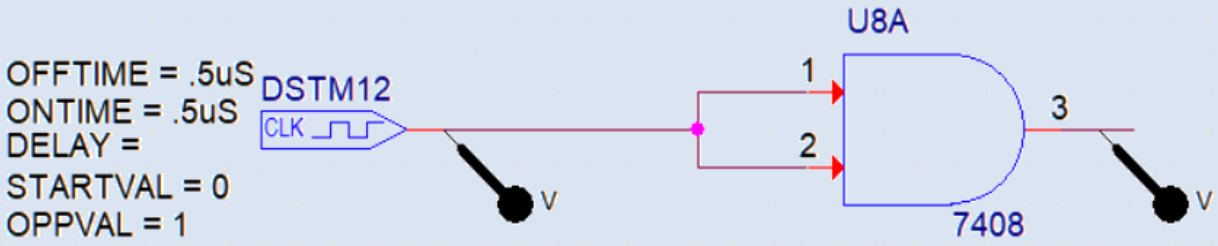
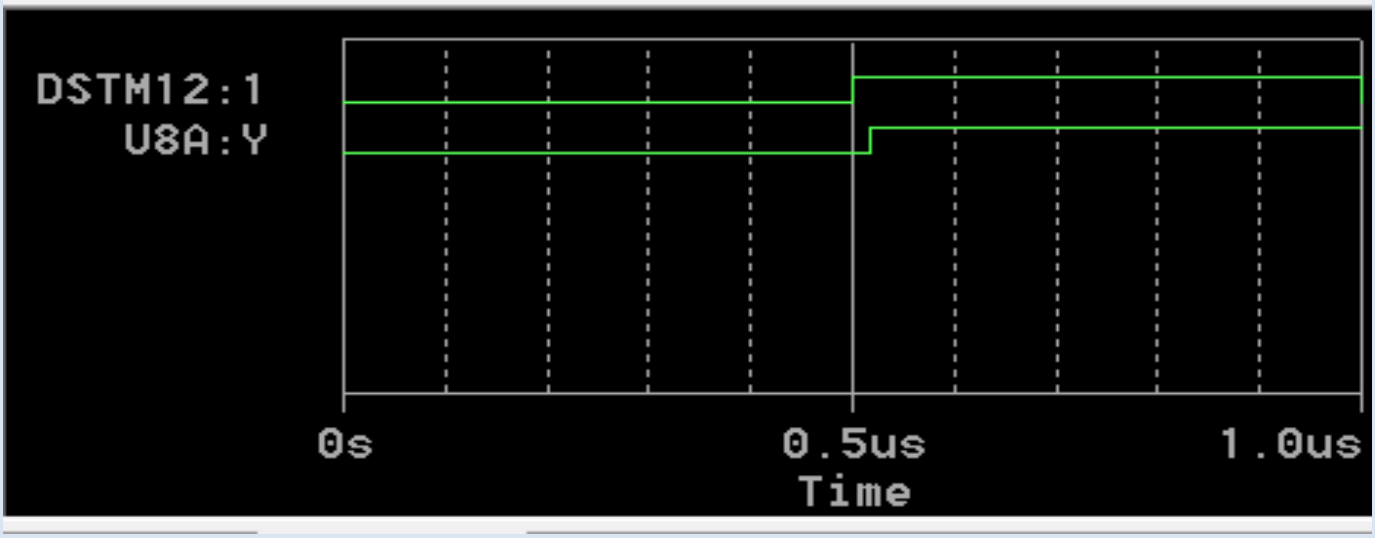


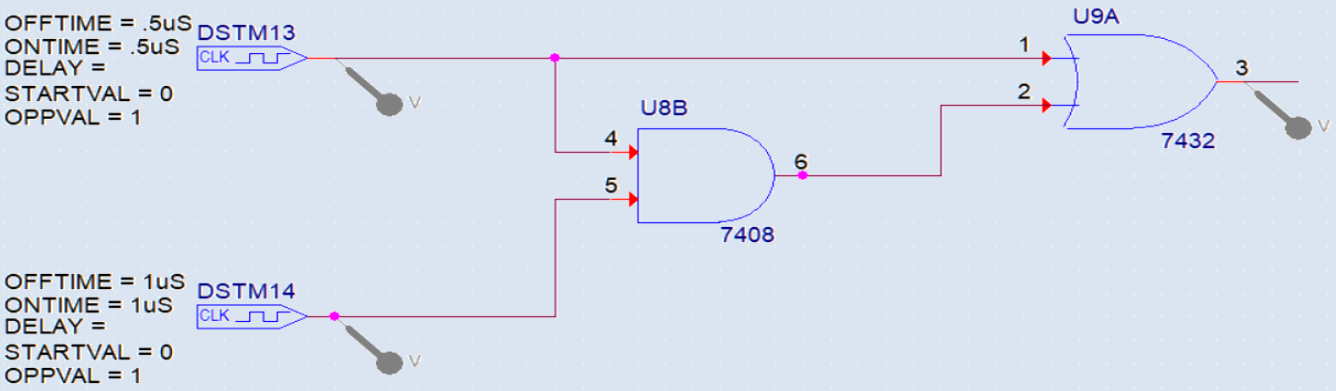
Fig.2

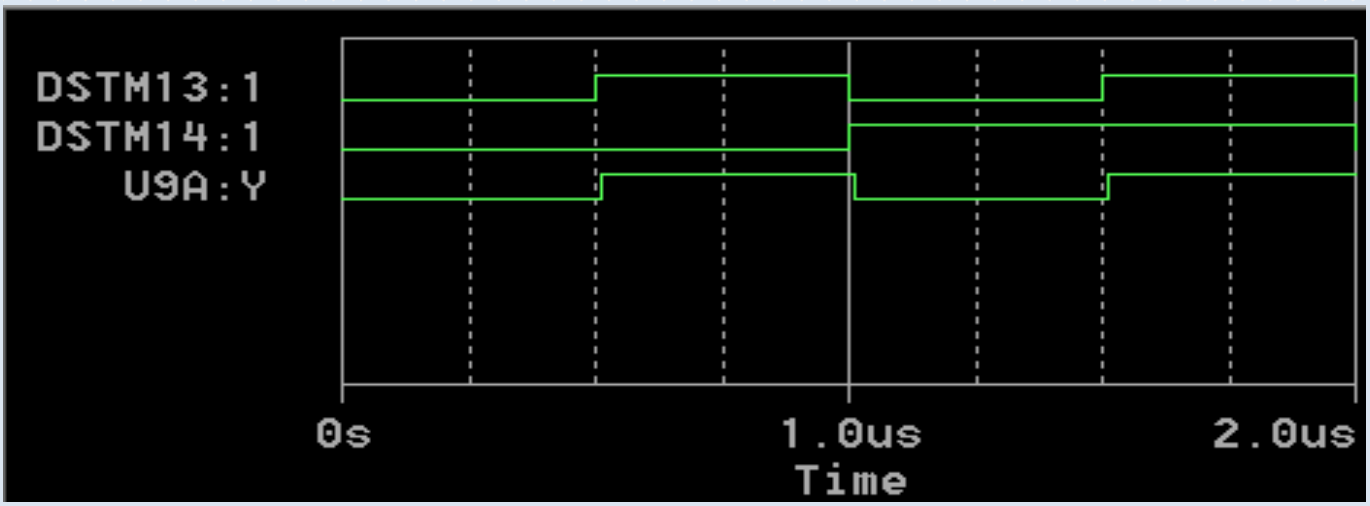




The above circuit illustrates **Idempotent Law** i.e. **A . A = A**

c. Design a circuit that illustrates rule 10. Copy the circuit from OrCAD and paste it in your lab report.





d. Rule 6 illustrates that A+A' could be replaced with a wire to Vcc. What does rule 8 illustrate?

Ans:

Rule 8 illustrates that **A.A'** can be represented with a break in the line or with a wire directly connected to the ground voltage (**GND**) because the output of **A.A'** is **Always Low.**

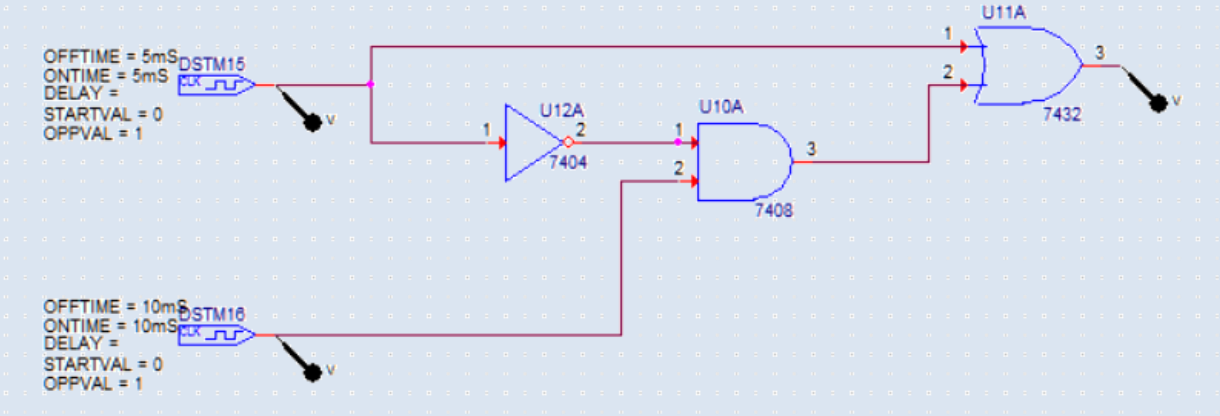
e. Rule 11 states that A+A'B = A+B. Using OrCAD design a circuit that illustrates each of these expressions.

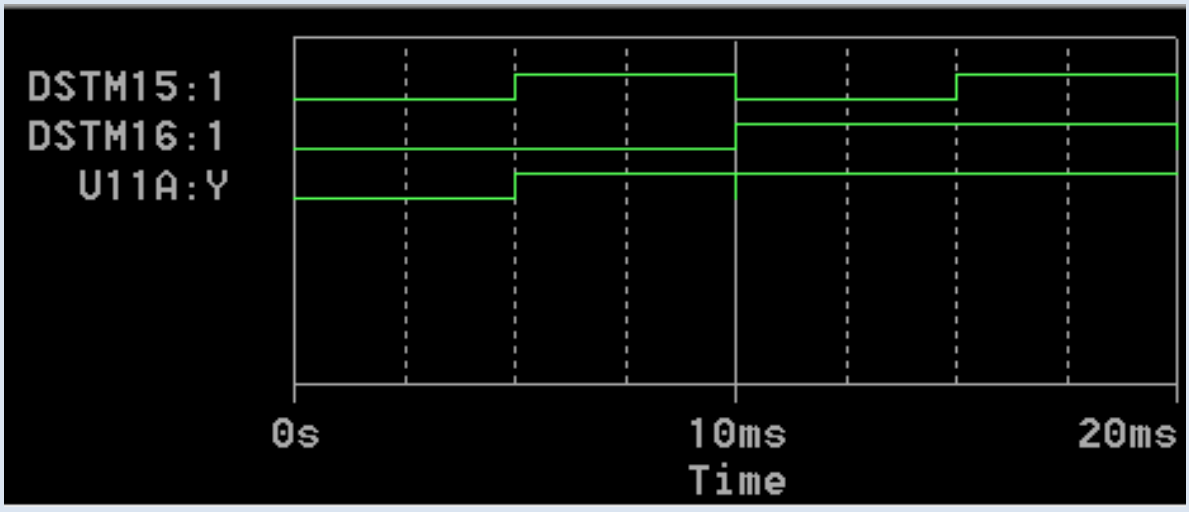
A+A'B

A+B

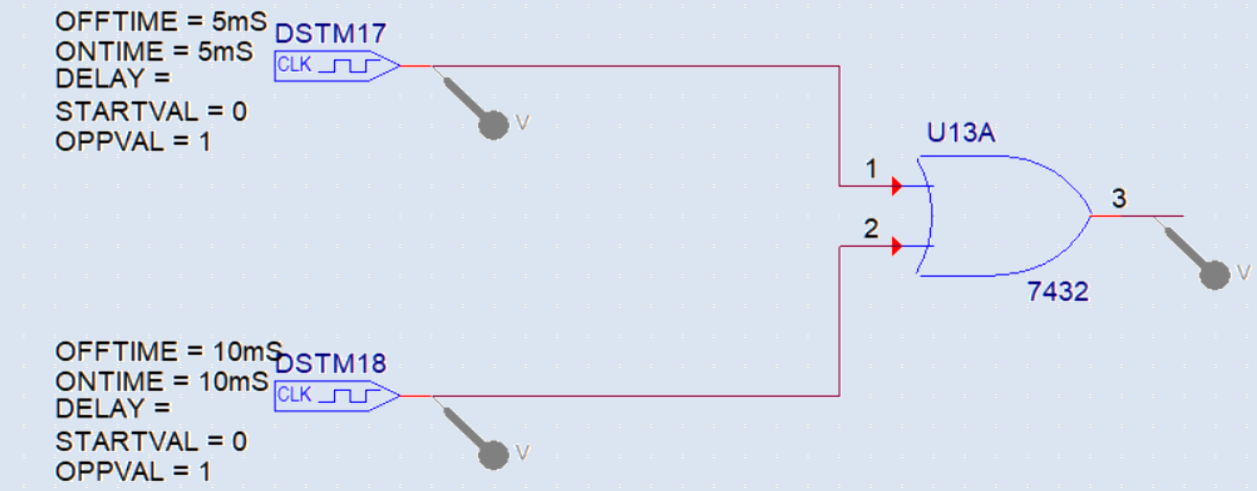
Prove that these two circuits perform equivalent logic. (Connect two circuits and show that their outputs are the same).

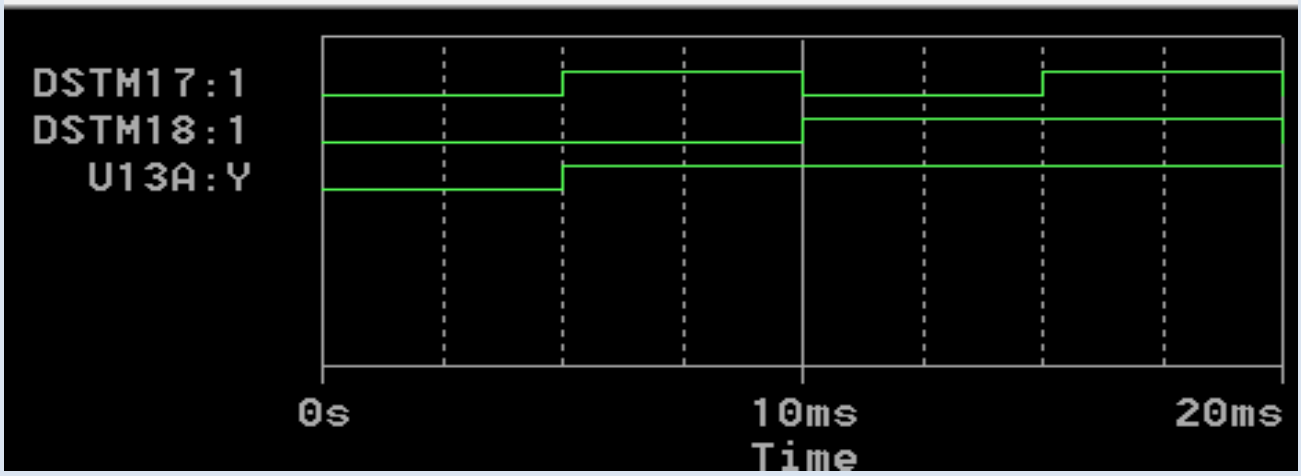
For the first circuit, **A + A'B** :





For the second circuit, **A + B**:





From the simulation, we can observe that the above circuits are logically equivalent as both of them give identical logical plots as output of simulation.

Hence, **A + A'B = A + B.**

Thus, Rule 11 is proved

Procedure 2: Demorgan's Theorem

Proof of equation (1)

Using OrCAD Cadence Capture construct the two circuits given in Figs.3 and 4 corresponding to the functions A'. B' and (A+B)' respectively.

Show that for all combinations of A and B, the two circuits give identical results.

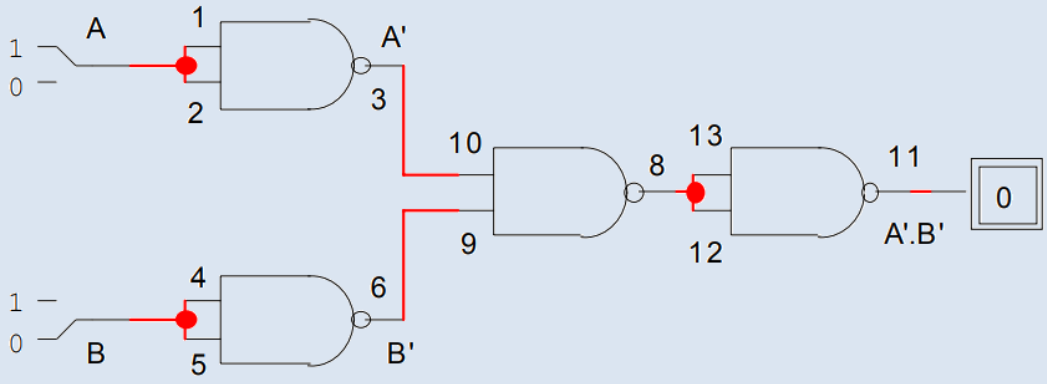


Fig.3

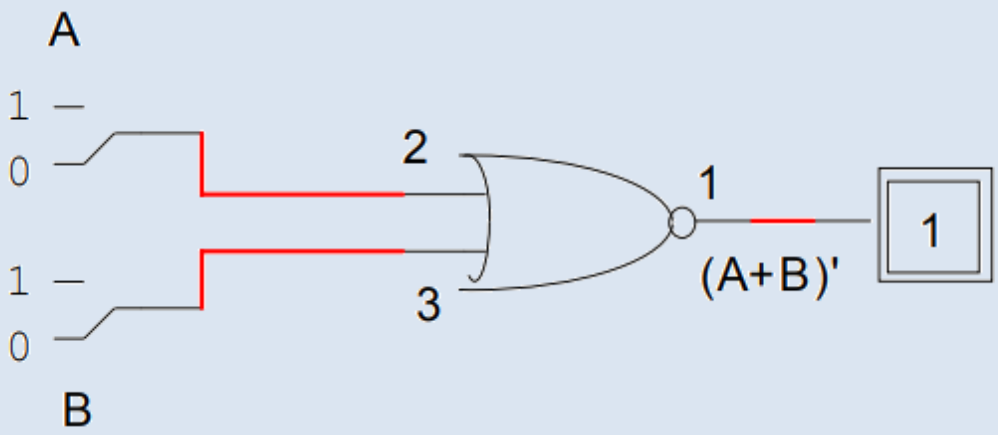
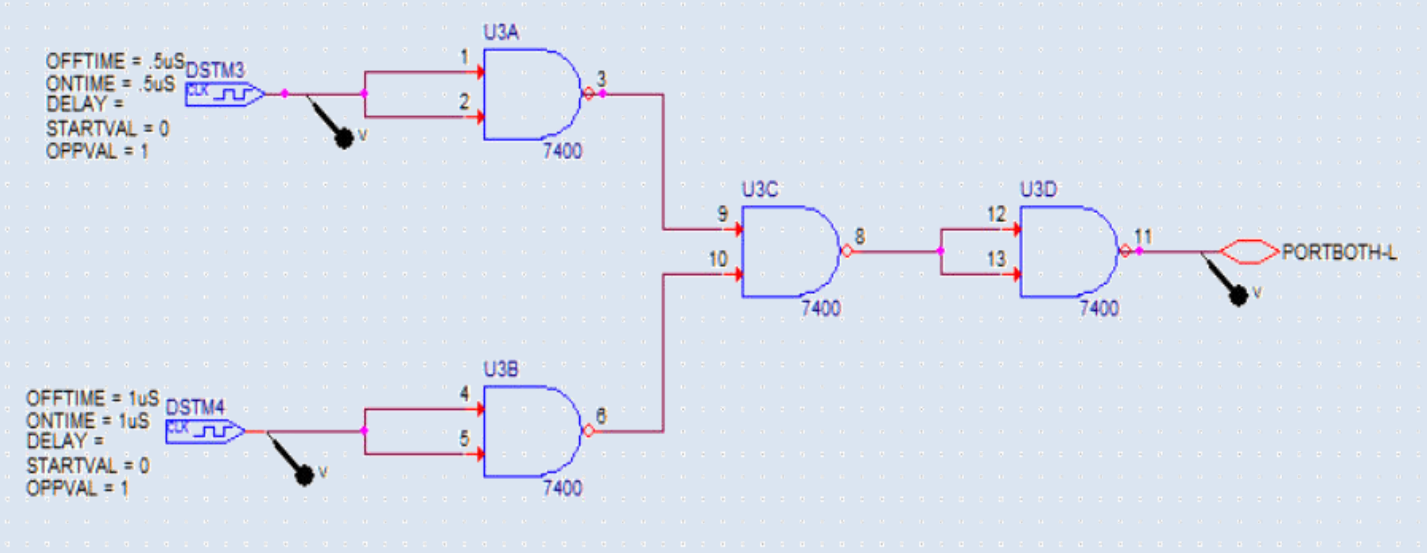
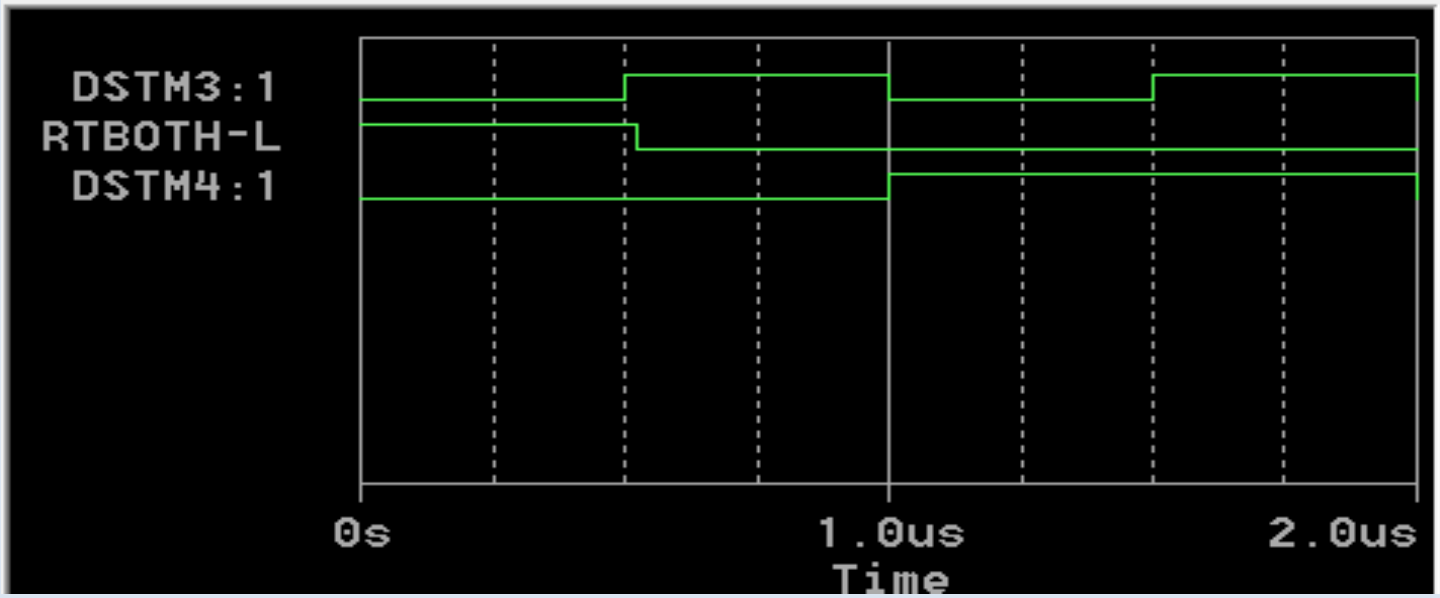


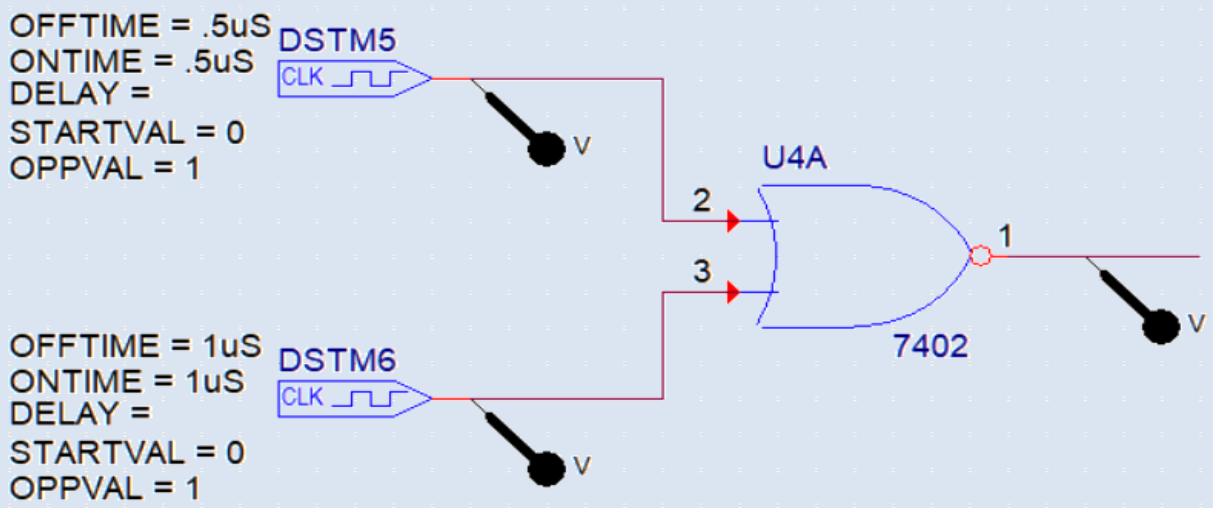
Fig.4

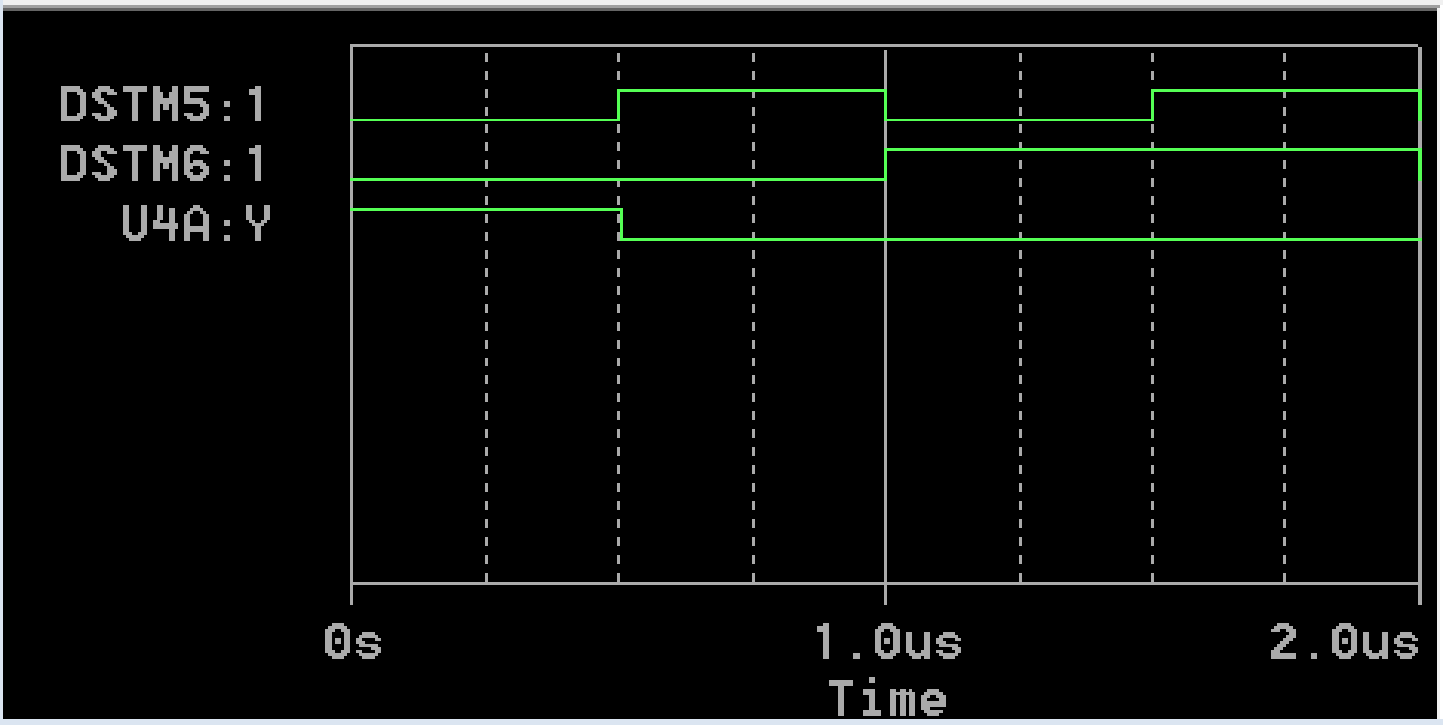
Circuit Analysis for fig 3:





Circuit Analysis for Fig 4:





Here, from the result obtained by simulation, it is clearly visible that both the gates are logically equivalent.
Thus, Demorgan's first law is verified.

Proof of equation (2)

Using OrCAD, construct two circuits given in Figs. 5 and 6, corresponding to

the functions A'+B' and (A.B)' A.B, respectively.

Show that, for all combinations of A and B, the two circuits give identical results. In the lab connect these circuits and verify their operations.

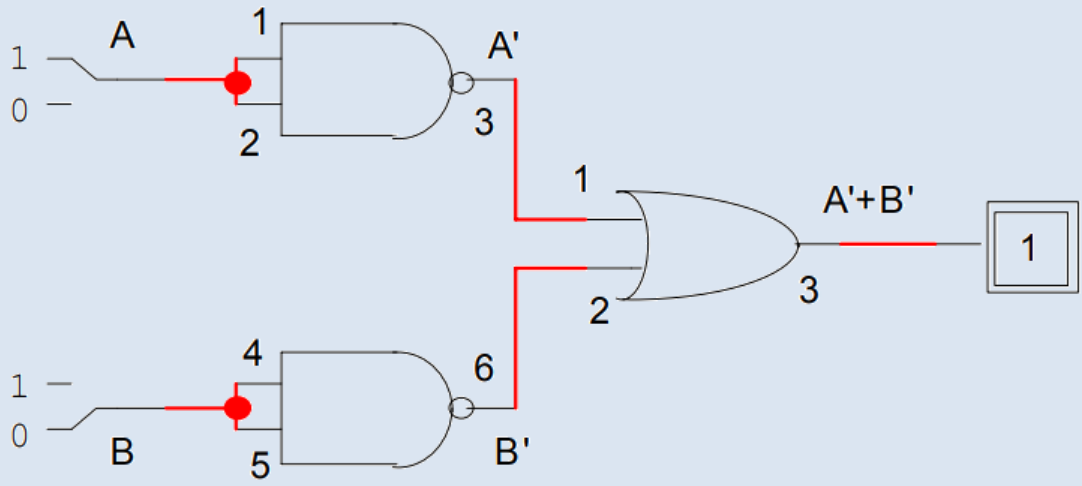


Fig. 5

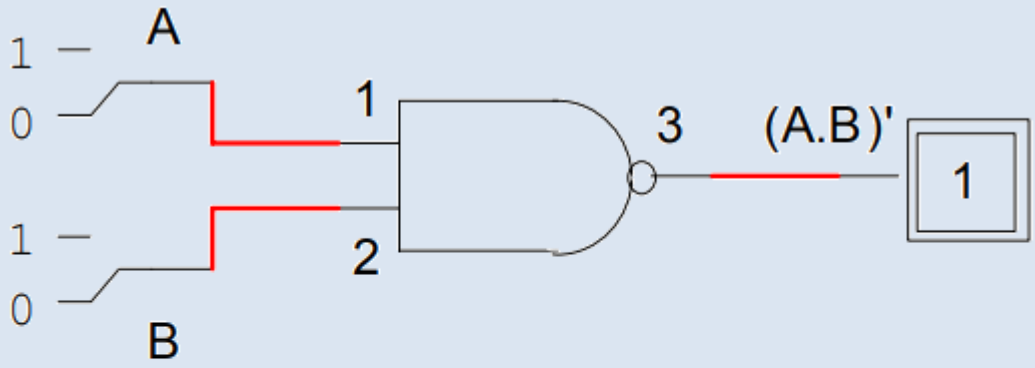
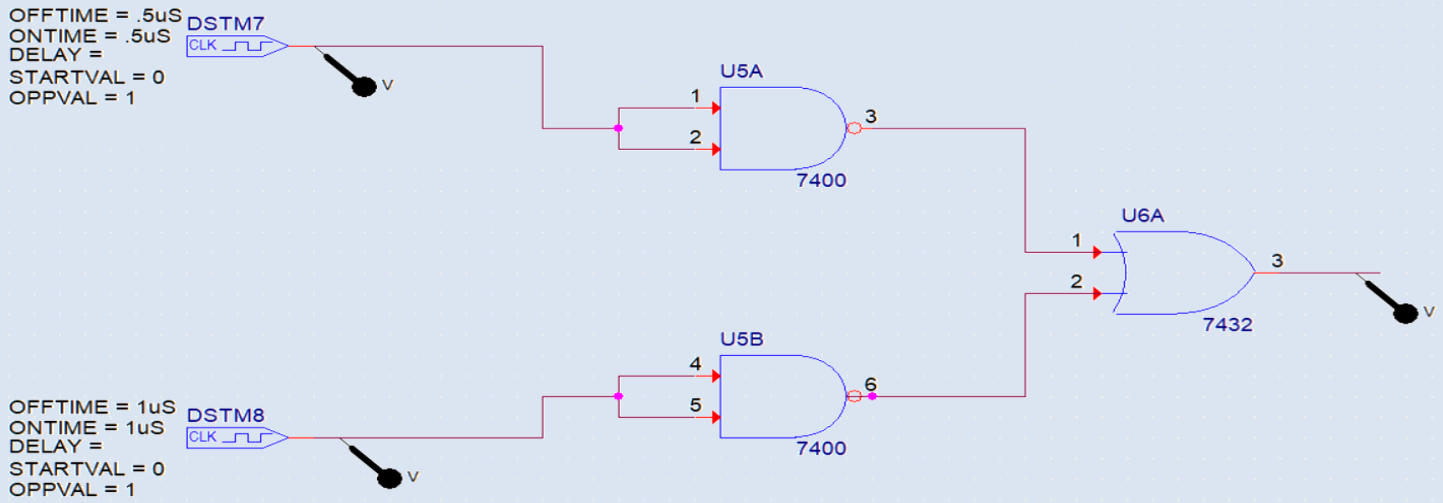
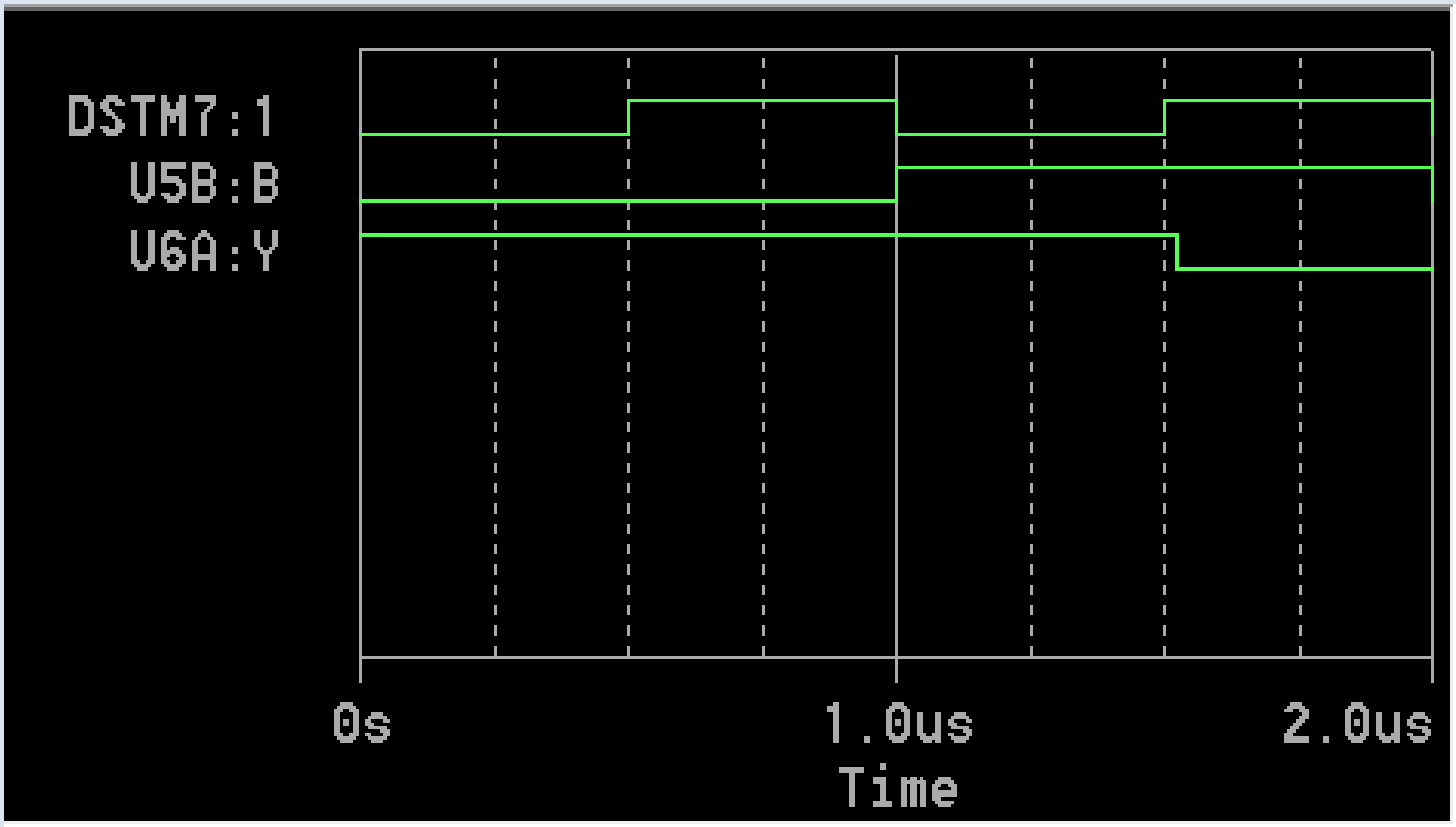


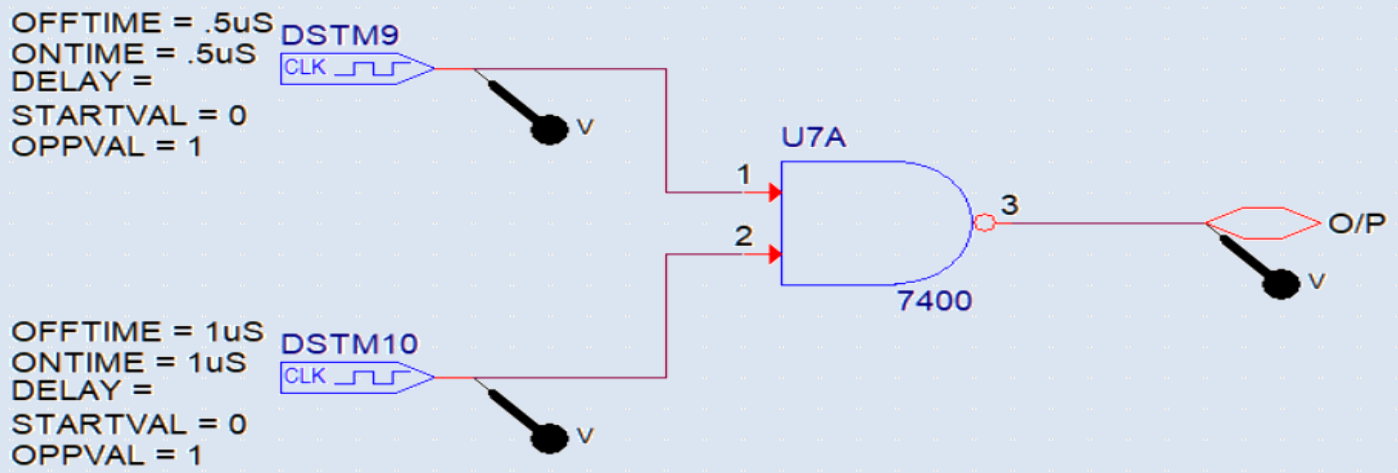
Fig. 6

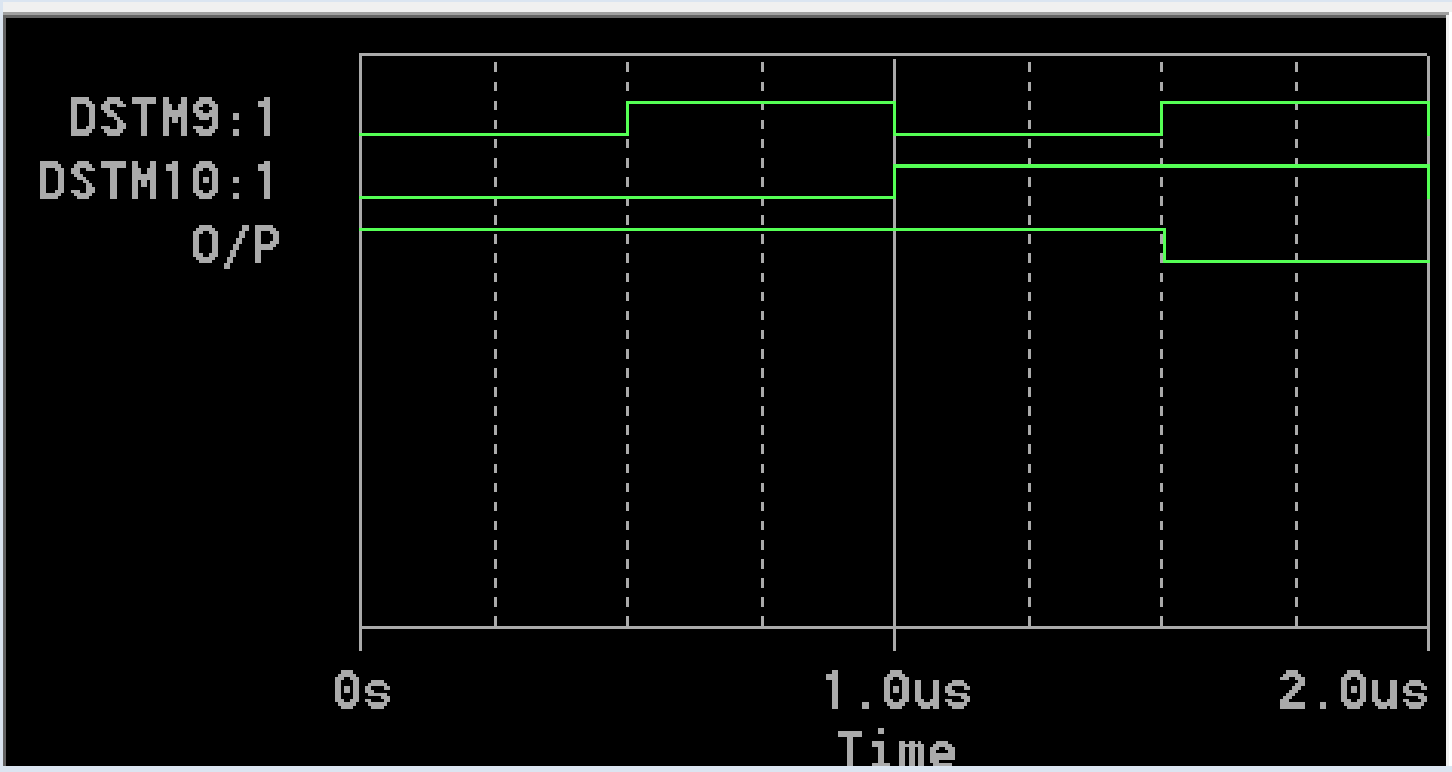
Circuit Analysis For Fig 5:





Circuit Analysis For Fig 6:





Here, from the result obtained by simulation, it is clearly visible that both the gates are logically equivalent.

Thus, Demorgan's second law is verified.

II. Design of a Digital Circuit

Consider the following problem:

Four chairs A, B, C, and D are placed in a row. Each chair may be

occupied ("l") or empty ("0"). A Boolean function F is "l" if and only if there are two or more adjacent chairs that are empty.

1. Give the truth table defining the Boolean function F

Ans:

The required truth table for this problem is:

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

`

2. Express F as a minterm expansion (standard sum of product)

Ans:

The minterm expansion of above Boolean function is:

$$\mathbf{F} = A'.B'.C'.D' + A'.B'.C'.D + A'.B'.C.D' + A'.B'C.D + A'.B.C'.D' + A'.B.C'.D + A'.B.C.D' + A.B'.C'.D' + A.B'.C'.D + A.B'.C.D' + A.B.C'.D'$$

3. Express F as a maxterm expansion (standard product of sum).

Ans:

The maxterm expansion of above Boolean function is:

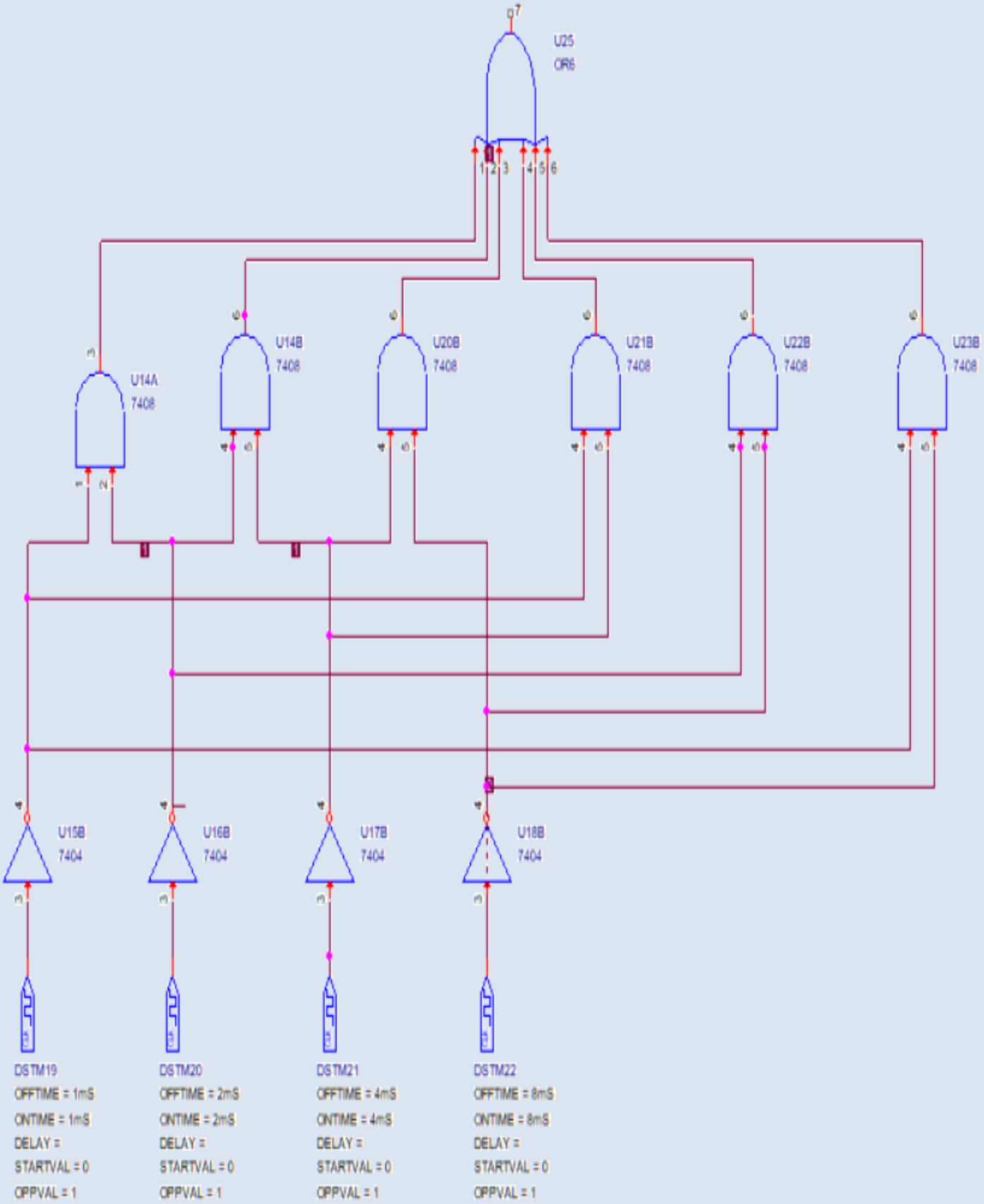
$$F = (A+B'+C'+D') \cdot (A'+B+C'+D') \cdot (A'+B'+C+D') \cdot (A'+B'+C'+D) \cdot (A'+B'+C'+D')$$

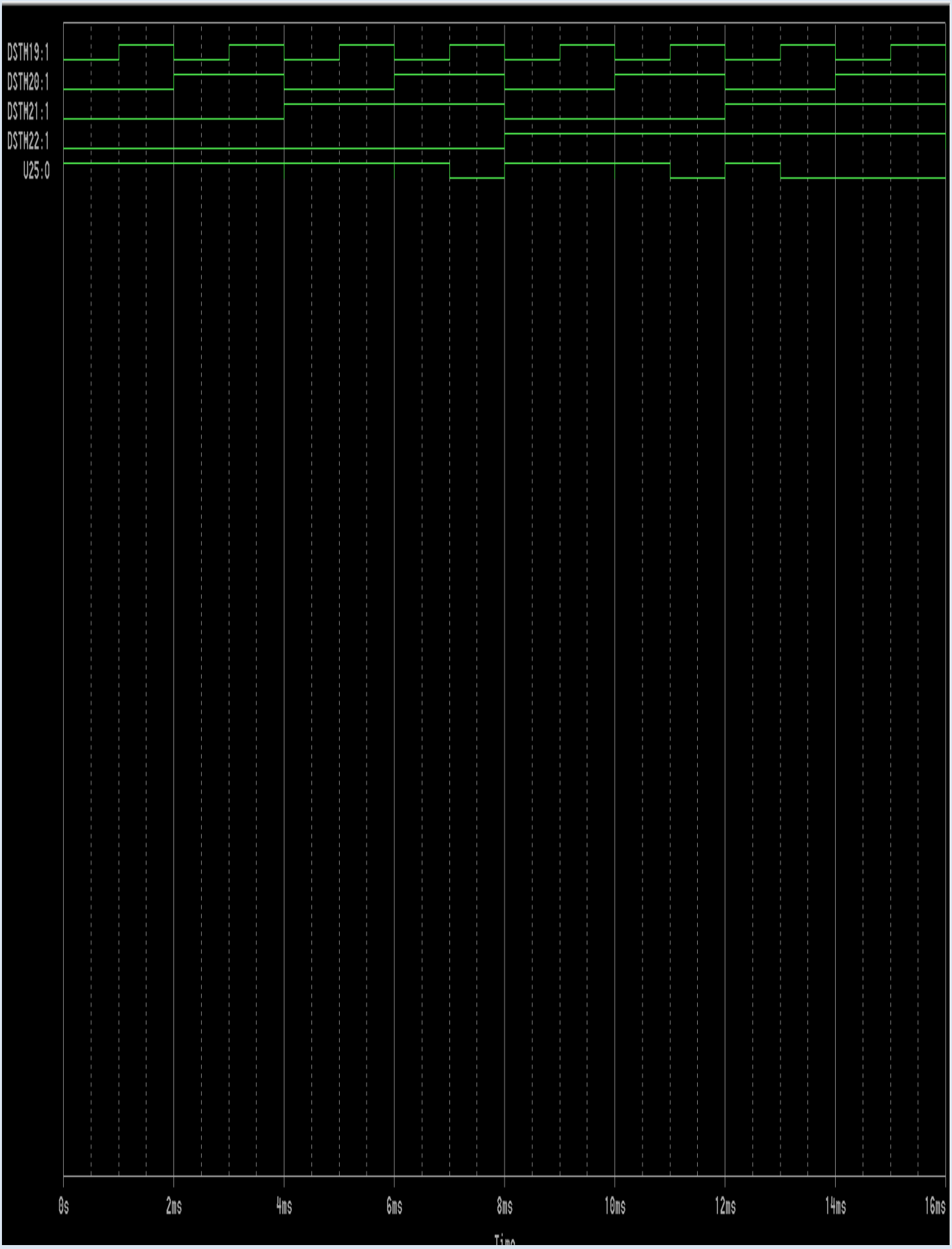
4. Using postulates and theorems Of Boolean algebra, simplify the minterm expansion of F to a form with as few occurrences of each as possible.

The above Boolean function can be reduced to the following form using the **Laws of Boolean Algebra:**

$$F = A'.B' + B'.C' + C'.D' + A'.C' + B'.D' + A'.D'$$

5. Implement on LogicWorks for the pre-lab and then on PB-503, the simplified Boolean function with logic gates and check the operation of the circuit.


U25
OR6
U14A
7408
U14B
7408
U20B
7408
U21B
7408
U22B
7408
U23B
7408
U15B
7404
U16B
7404
U17B
7404
U18B
7404
DSTM19
OFFTIME = 1mS
ONTIME = 1mS
DELAY =
STARTVAL = 0
OPPVAL = 1
DSTM20
OFFTIME = 2mS
ONTIME = 2mS
DELAY =
STARTVAL = 0
OPPVAL = 1
DSTM21
OFFTIME = 4mS
ONTIME = 4mS
DELAY =
STARTVAL = 0
OPPVAL = 1
DSTM22
OFFTIME = 8mS
ONTIME = 8mS
DELAY =
STARTVAL = 0
OPPVAL = 1


DSTM19:1
DSTM20:1
DSTM21:1
DSTM22:1
U25:0
0s
2ms
4ms
6ms
8ms
10ms
12ms
14ms
16ms
Time

Result:

All truth tables, circuits (using Or CAD), etc. used in completing this experiment has been shown above.

In this way, the laws of Boolean algebra can be observed, verified and studied practically using circuits and simulations