CSE1003 Digital Logic and Design
Module 4
Combinational Circuits II
L2

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Contents

6 hrs

- Binary Parallel Adder - Look ahead carry
- Magnitude Comparator
- Decoders
- Encoders
- Multiplexers
- Demultiplexers

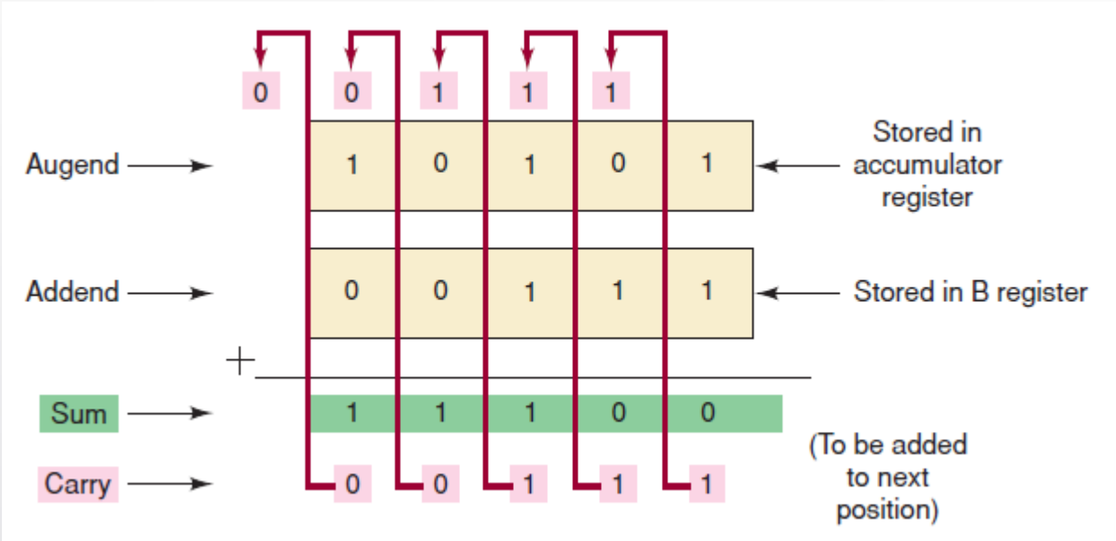
- CO4: Analyze the operation of medium complexity standard combinational circuits like the encoder, decoder, multiplexer, demultiplexer.

Binary Parallel Adder

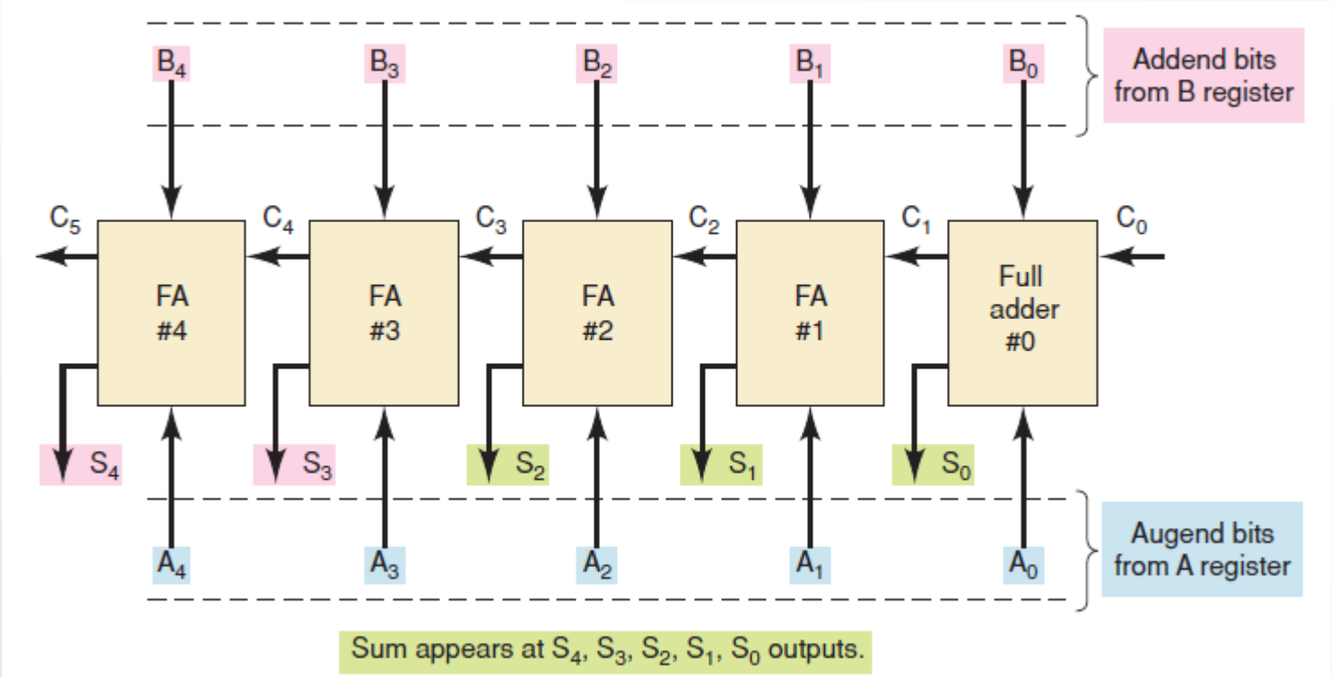
- **A binary parallel adder is a digital circuit that adds two binary numbers in parallel form and produces the arithmetic sum of those numbers in parallel form.**
- **It consists of full adders connected in a chain, with the output carry from each full-adder connected to the input carry of the next full-adder in the chain.**
- **An n-bit parallel adder requires n-Full adders.**
- **<u>Practical Applications:</u>**

1. It is used in Digital Processors
2. ALU in computers and in calculators
3. Different IC and microprocessor chips in PCs and laptops
4. In Ripple counters
5. Important tool in DSP (Digital Signal Processing)

Binary Parallel Adder

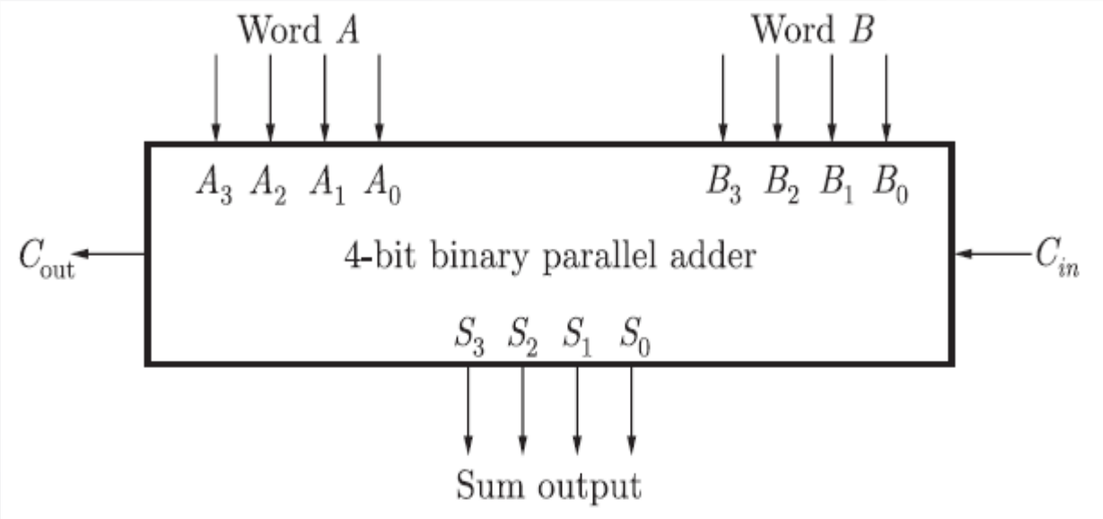


Typical binary addition process

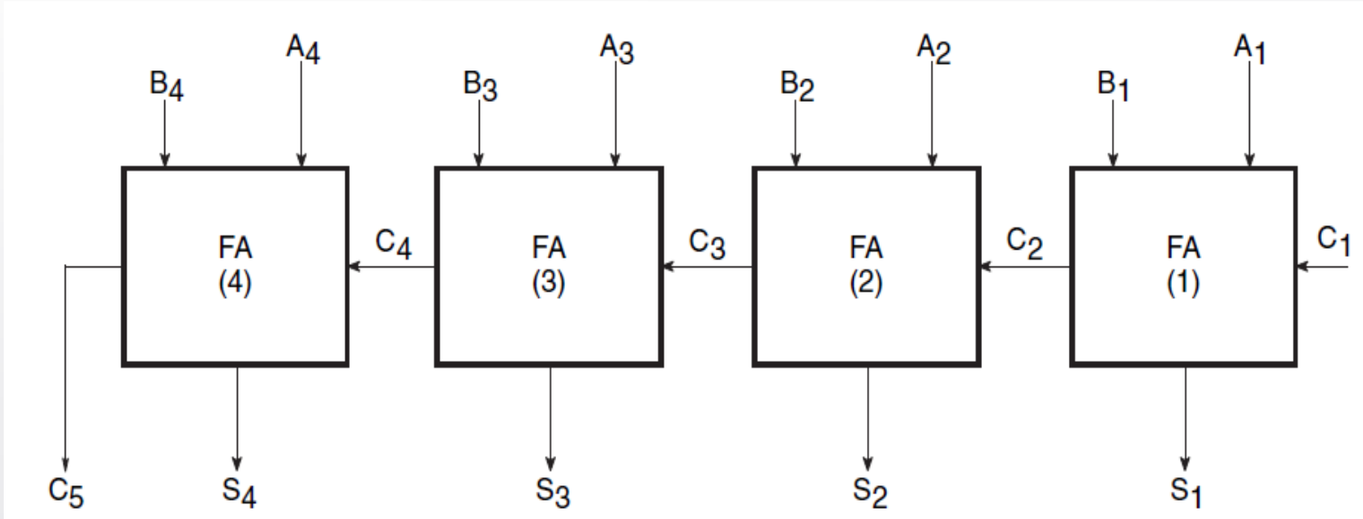


Block diagram of a five-bit parallel adder circuit using full adders.

Binary Parallel Adder

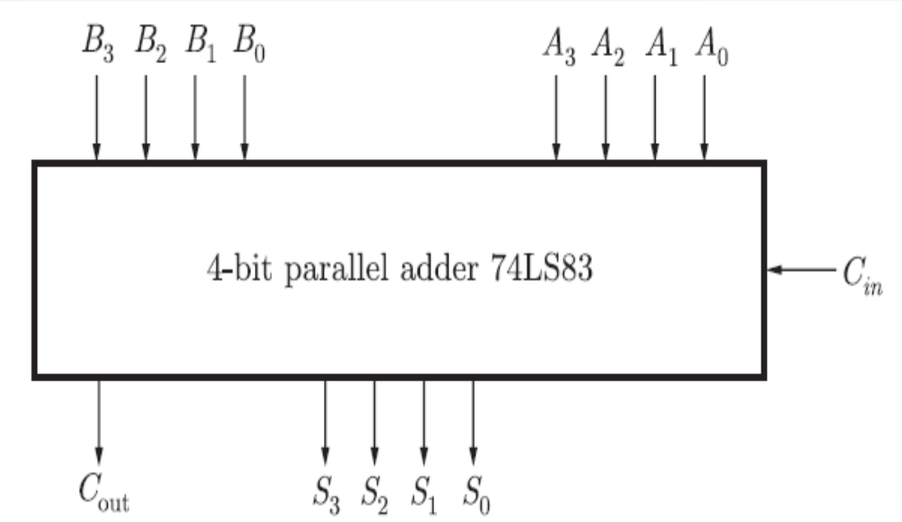


Block diagram of 4-bit binary adder

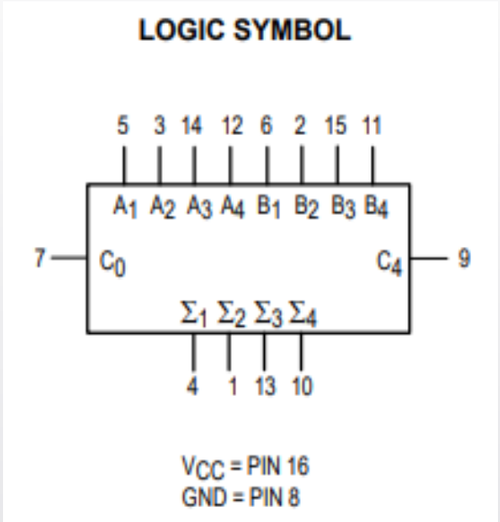


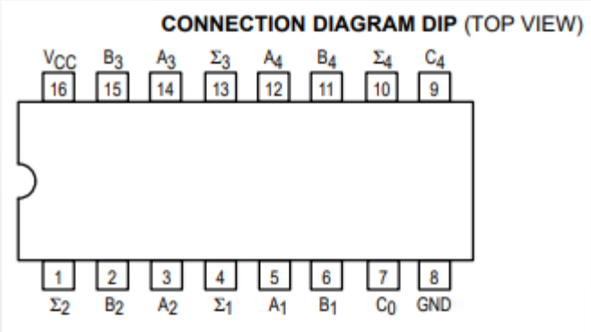
Logic diagram of a 4-bit binary parallel adder

Binary Parallel Adder



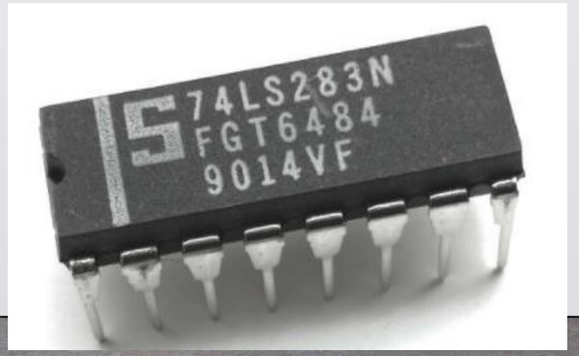
Logic symbol of 74LS283



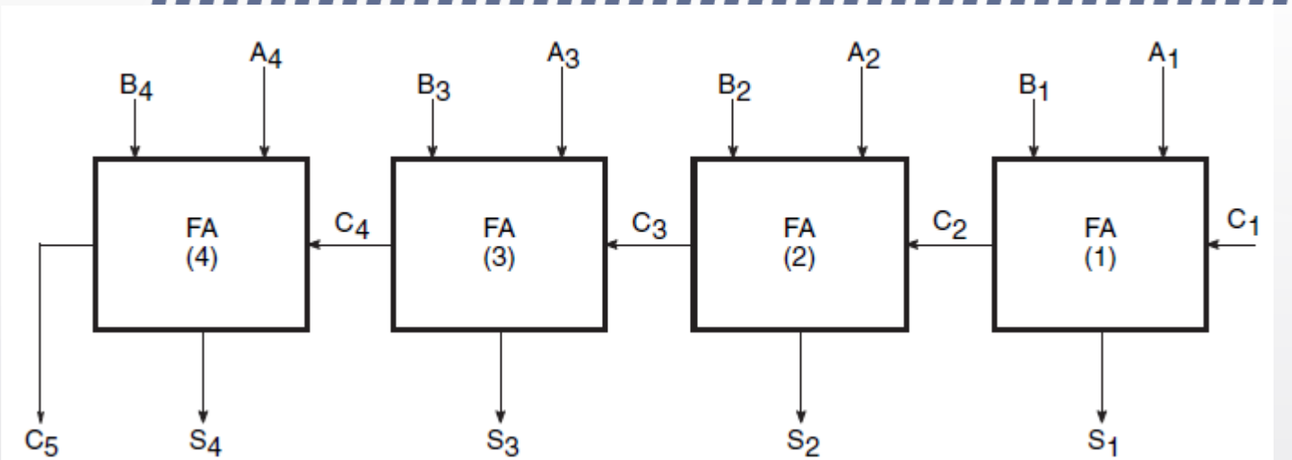


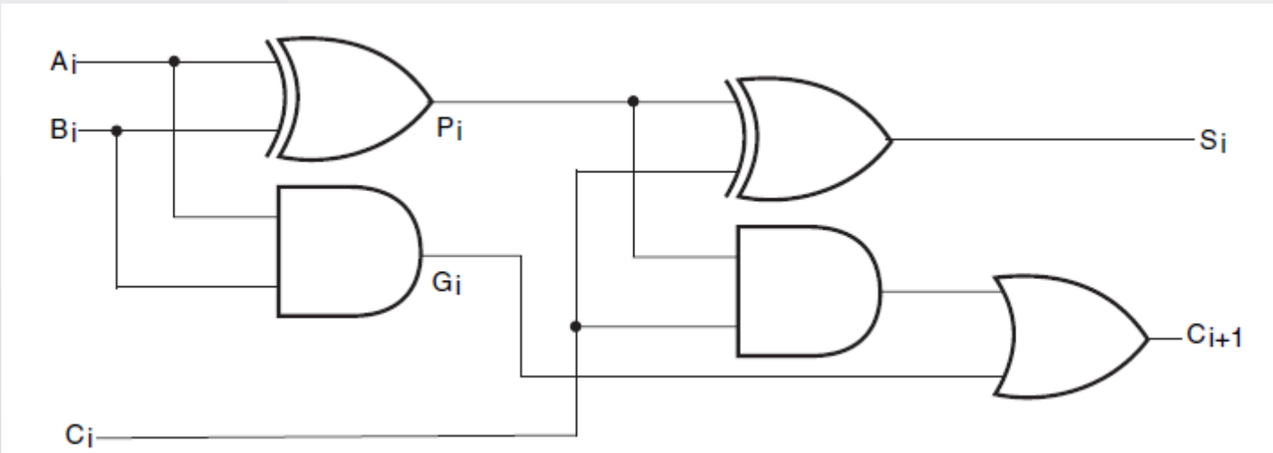
PIN NAMES

A_1–A_4	Operand A Inputs
B_1–B_4	Operand B Inputs
C_0	Carry Input
Σ_1–Σ_4	Sum Outputs
C_4	Carry Output



Binary Parallel Adder



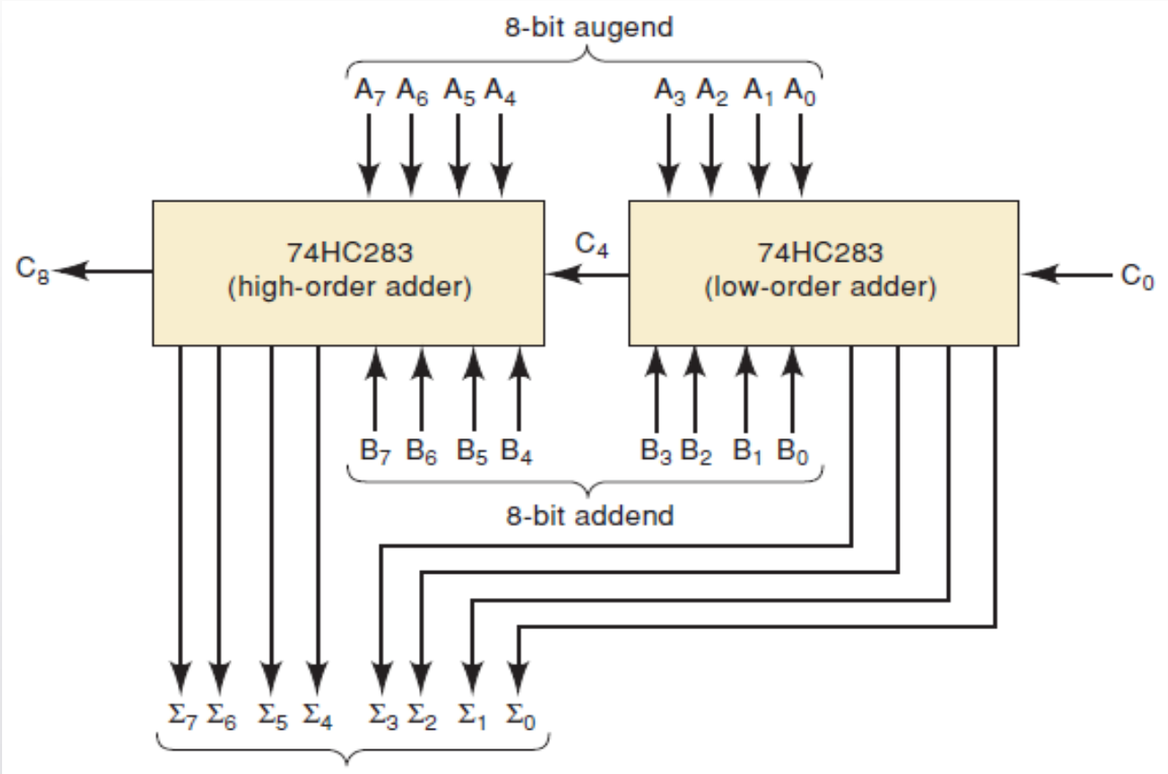


Logic diagram of a full adder

- Parallel adders suffer from propagation delay problem because higher bit additions depend on the carry generated from lower bit addition.
- The **carry propagation delay** for each full adder is the time between the application of the carry-in and the occurrence of the carry out.
- For an *n*-bit parallel adder, the total delay time is equal to nt_p , *where* t_p is the propagation delay of full-adder.
- The parallel adder in which the carry-out of each full adder is the carry-in to the next most significant adder is called a **ripple carry adder**.

The speed of parallel adder depends on the time required for the carries to propagate or ripple through all of the stages of the adder.

Binary Parallel Adder



Block symbol for cascading two 74HC283s

Binary Parallel Adder

- How many inputs does a full adder have? How many outputs?

Ans: 3,2

- Assume the following input levels in Figure.

$A_4A_3A_2A_1A_0 = 01001$; $B_4B_3B_2B_1B_0 = 00111$; $C_0 = 0$

(a) What are the logic levels at the outputs of FA #2?

Ans: $S_2=0$, $C_3=1$

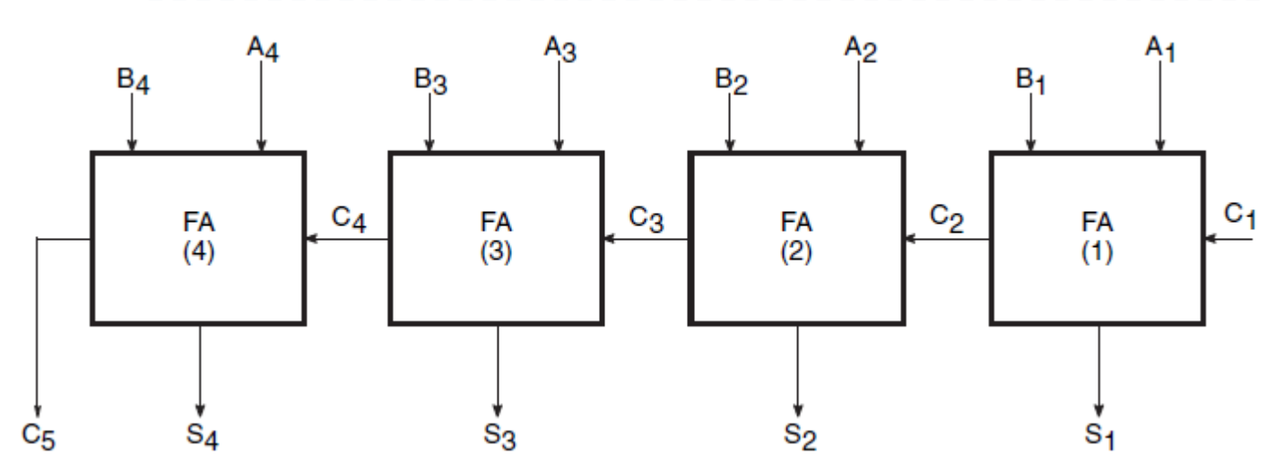
(b) What is the logic level at the C_5 output?

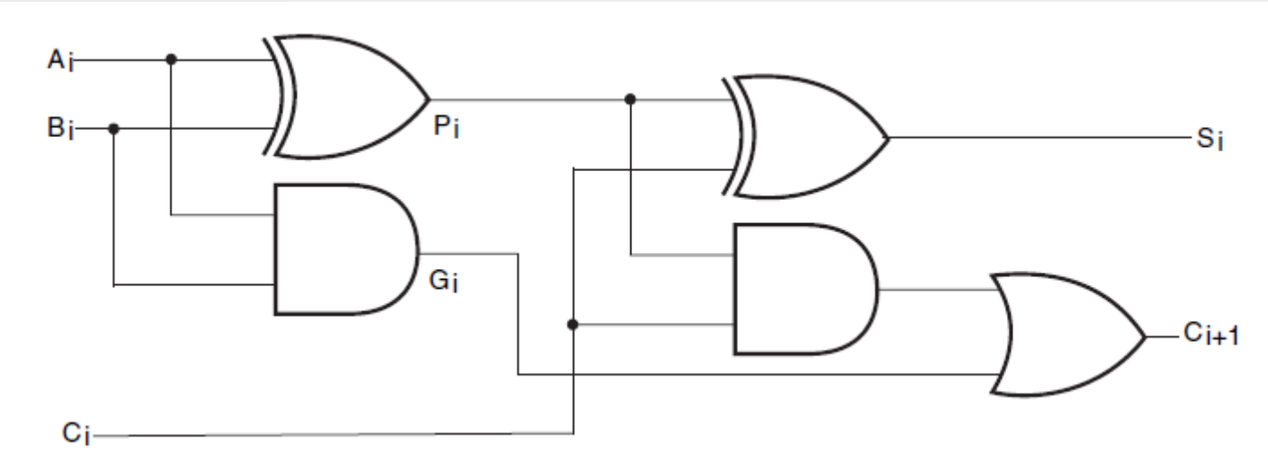
Ans: $C_5=0$

Look ahead carry Adder

- The look-ahead-carry adder speeds up the operation by eliminating the ripple carry delay.
- It examines all the input bits simultaneously and also generates the carry-in bits for all the stages simultaneously.
- It looks ahead and generate the carry for a certain given addition operation.
- The method of speeding up the addition process is based on the two additional functions of the full-adder, called the carry generate and carry propagate functions.

Look ahead carry Adder





Logic diagram of a full adder

$$P_i = A_i \oplus B_i$$

$$G_i = A_i.B_i$$

$$S_i = P_i \oplus C_i$$

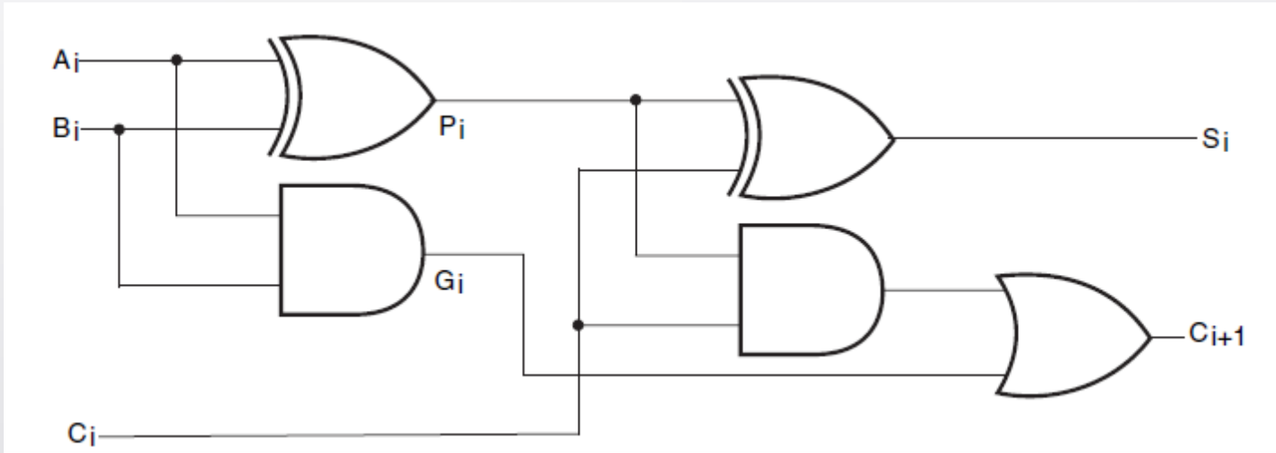
$$C_{i+1} = P_i.C_i + G_i$$

Look ahead carry Adder

Carry Generation

- Carry is generated only if both the input bits are 1, that is, if both the bits *A* and *B* are 1's, a carry has to be generated in this stage regardless of whether the input carry C_{in} is a 0 or a 1. Otherwise carry will not be generated.

Carry-generation function, $G_i = A_i B_i$



Look ahead carry Adder

Carry Propagation

- A carry is propagated if any one of the two input bits *A* or *B* is 1.
- If both *A* and *B* are 0, a carry will never be propagated.
- On the other hand, if both *A* and *B* are 1, then it will not propagate the carry but will generate the carry.
- Carry-propagation function

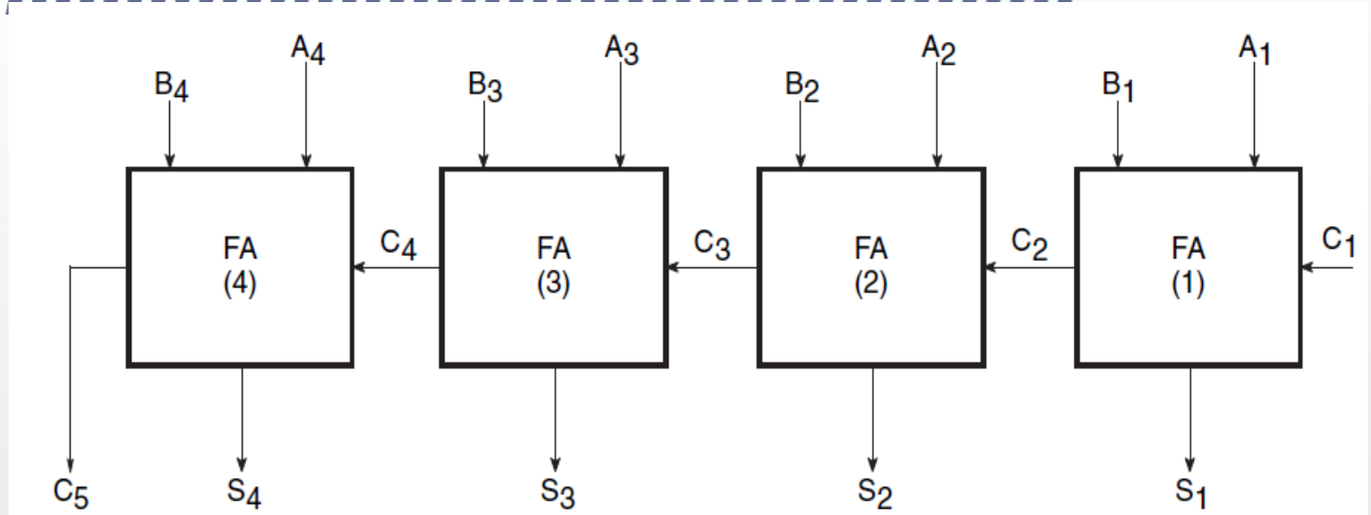
$$P_i = A_i \oplus B_i$$

Carry-generation and carry-propagation

Inputs			Outputs	
A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1 □
1	0	0	1	0
1	0	1	0	1 □
1	1	0	0	1 ○
1	1	1	1	1 ○

□ : Indicates carry propagated
○ : Indicates carry generated

Look ahead carry Adder



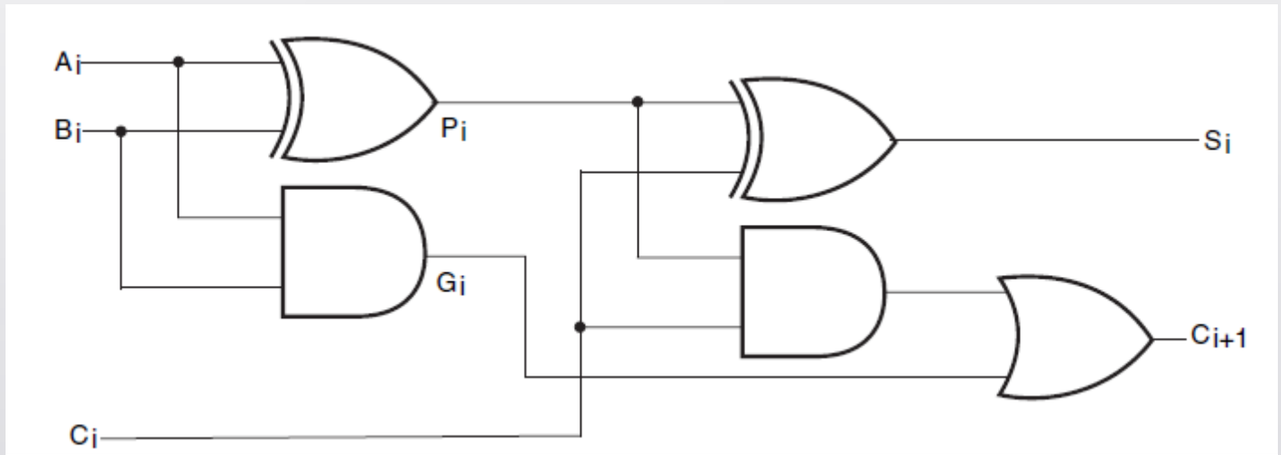
CARRY output of each full adder stage in the four-bit binary adder

$$C_2 = G_1 + P_1.C_1$$

$$C_3 = G_2 + P_2.C_2 = G_2 + P_2.(G_1 + P_1.C_1) = G_2 + P_2.G_1 + P_1.P_2.C_1$$

$$C_4 = G_3 + P_3.C_3 = G_3 + P_3.(G_2 + P_2.G_1 + P_1.P_2.C_1)$$

$$C_4 = G_3 + P_3.G_2 + P_3.P_2.G_1 + P_1.P_2.P_3.C_1$$



Look ahead carry Adder

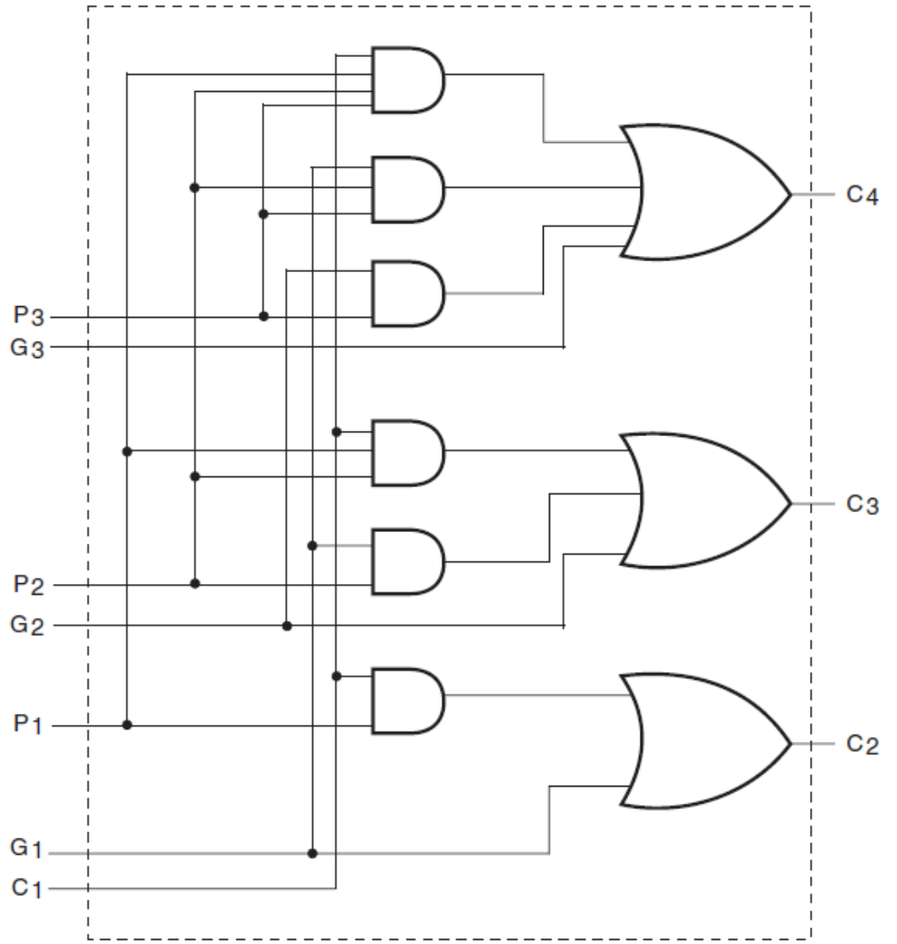
Four-bit full-adder with a look-ahead carry generator

$$C_2 = G_1 + P_1.C_1$$

$$C_3 = G_2 + P_2.C_2 = G_2 + P_2.(G_1 + P_1.C_1) = G_2 + P_2.G_1 + P_1.P_2.C_1$$

$$C_4 = G_3 + P_3.C_3 = G_3 + P_3.(G_2 + P_2.G_1 + P_1.P_2.C_1)$$

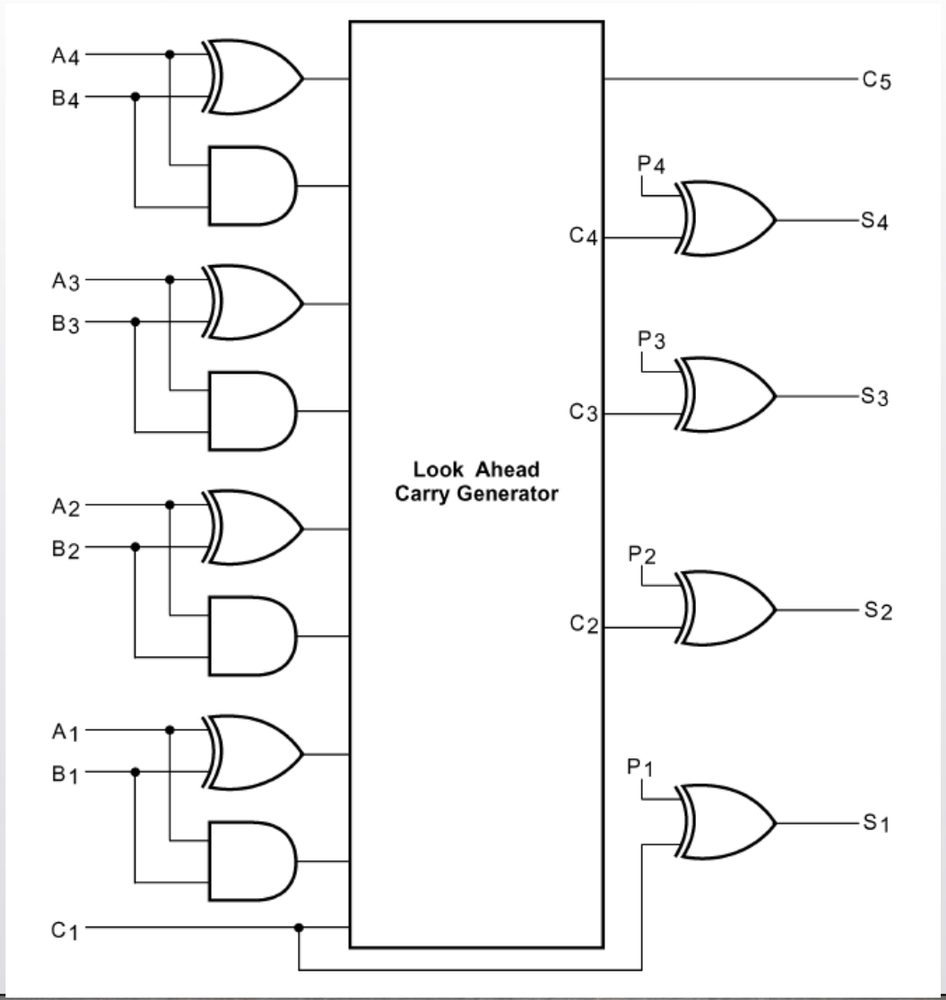
$$C_4 = G_3 + P_3.G_2 + P_3.P_2.G_1 + P_1.P_2.P_3.C_1$$



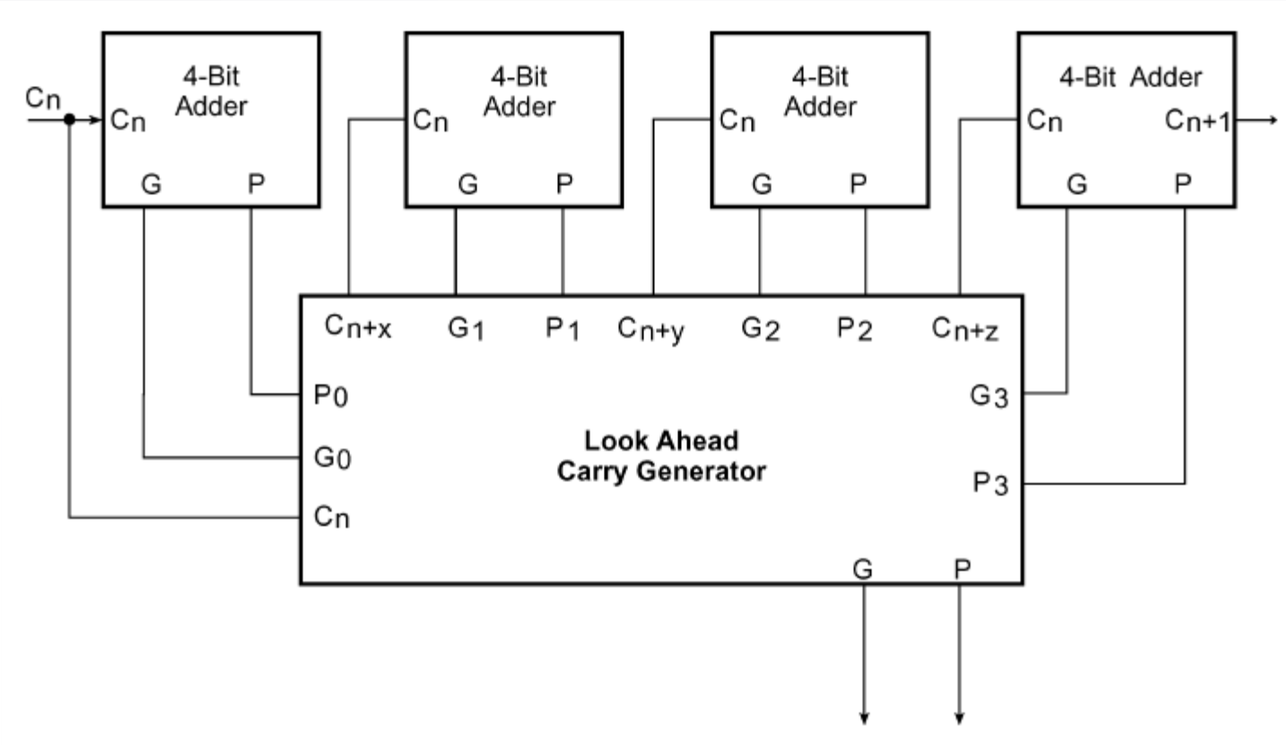
The circuit for look-ahead-carry introduces a delay corresponding to two gate levels.

Look ahead carry Adder

Four-bit full adder with a look-ahead carry generator

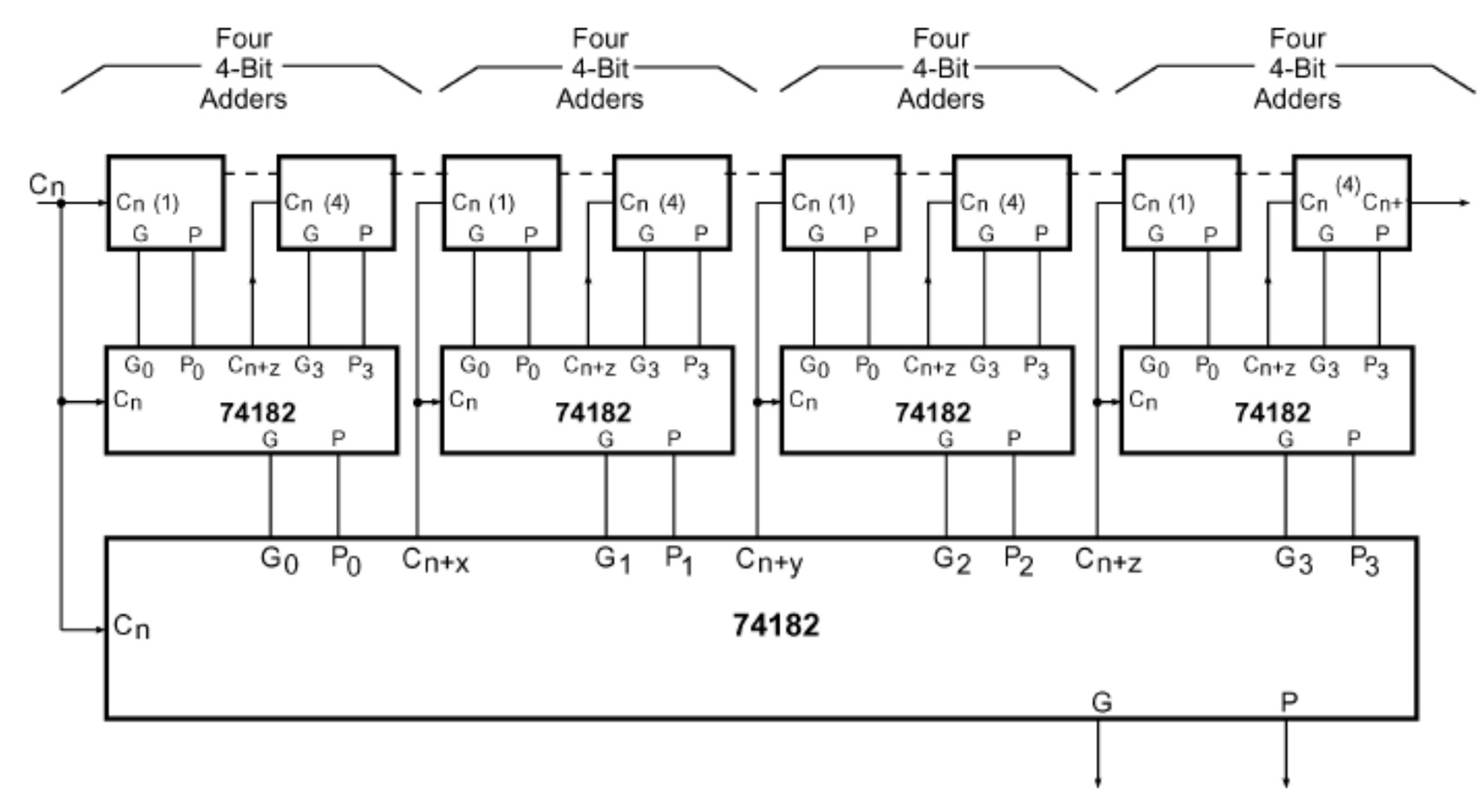


Look ahead carry Adder



IC 74182 interfaced with four four-bit adders

Look ahead carry Adder



Look-ahead carry generation for adding 64-bit numbers