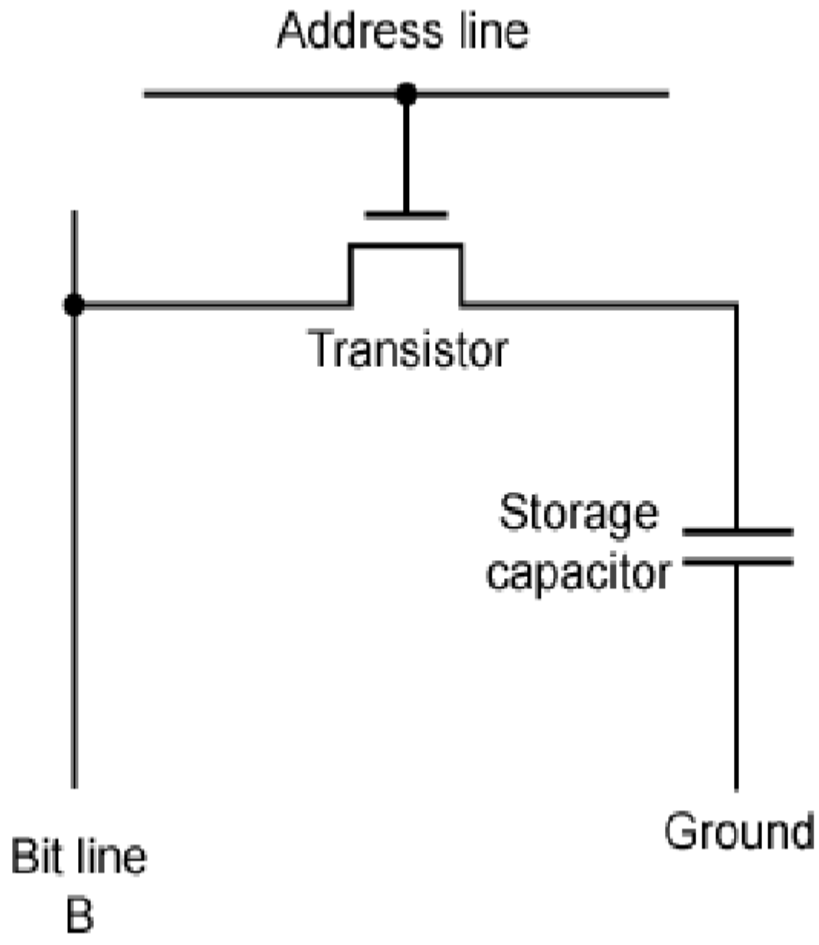
D- RAM

- Stores data as charge on capacitors
- If capacitor is charged
  - Data is 1
- Else
  - Data is 0.
- Needs refreshing cycle as capacitors have a tendency of discharging.
- The term *dynamic* refers to this tendency of the stored charge to leak away, even with power continuously applied.
- Volatile
- When read, data is lost. So, restoring need to be done.

D- RAM

- DRAM cell
  - Consists of a transistor and a capacitor.
  - Transistor acts a switch
    - If transistor is closed
      - Allows current to flow
    - Else
      - No current flows



D- RAM

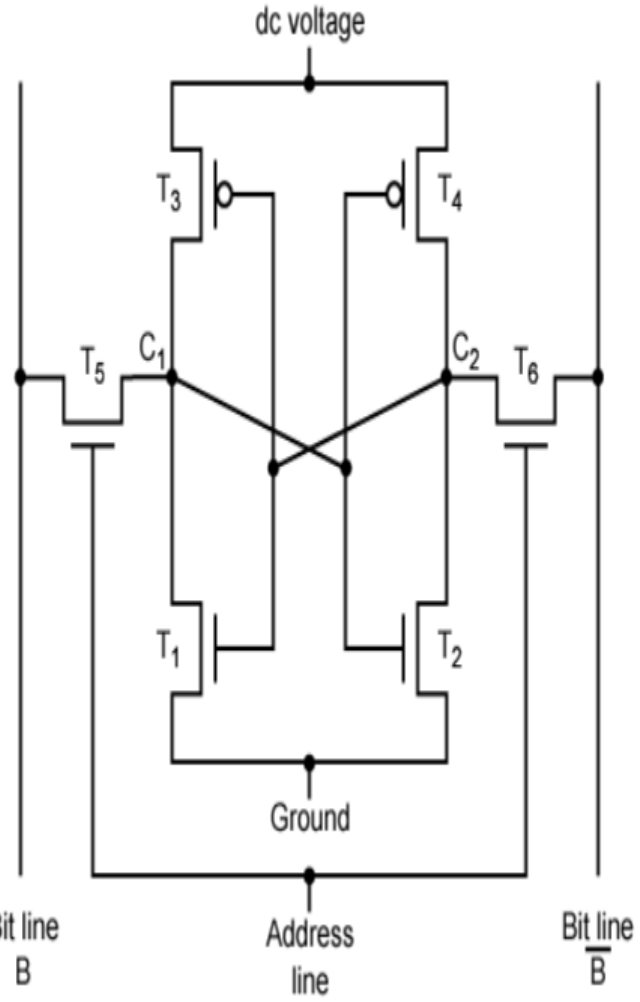
- Write
  - Voltage signal is applied to the bit line.
    - High voltage – 1
    - Low voltage – 0
  - Address line is activated allowing the charge to be transferred to the capacitor
- Read
  - Address line is activated
  - Charge on capacitor is fed out onto a bit line and to a sense amplifier.
  - Sense amplifier compares with reference value and determines if the cell contains 0 or 1.
  - The value is restored
- Used for large memory requirements

S-RAM

- Holds the data as long as the power is supplied
- Read operation don’t destroy the original data.
- Expensive than DRAM but shorter cycle times.
- Used for faster small memories like cache memory.
- Uses 4 – 6 transistors to store a single bit of data
- Less power consumption than DRAM
- Complex construction

S-RAM

- Transistor arrangement gives stable logic state
- Logic State 1
  - C_1 high, C_2 low
  - T_1 T_4 off, T_2 T_3 on
- Logic State 0
  - C_2 high, C_1 low
  - T_2 T_3 off, T_1 T_4 on
- Address line controls two transistors T_5 T_6.
- When signal is applied to address line, T_5 and T_6 are on.
- Write – apply value to B & complement to B
- Read – bit value is read from line B



D-RAM Vs S-RAM

SRAM	DRAM
- Volatile	- Volatile
- Faster	- Slower
- Smaller memory units	- Larger memory units
- Complex construction	- Simpler to build
- Don’t require refreshing circuit	- Require refresh
- Cache memory	- Main memory
- Digital	- Analog
- Expensive	- Less expensive