MEMORY DESIGN

Memory Design

- Available Memory chip Size $M_{N, W}$: $N \times W$
- Required memory size: $N^1 \times W^1$, Where $N^1 \geq N$ and $W^1 \geq W$
- Required number of $M_{N, W}$ chips: $p \times q$, Where $p = \lceil N^1 / N \rceil$ and $q = \lceil W^1 / W \rceil$

Memory design

There are 3 types of organizations of $N^1 \times W^1$ that can be formed using $N \times W$

- $N^1 = N$ and $W^1 > W$ => increasing the word size of the chip
- $N^1 > N$ and $W^1 = W$ => increasing the number of words in the memory
- $N^1 > N$ and $W^1 > W$ => increasing both the number of words and number of bits in each word.

There are different types of organization of $N^1 \times W^1$ –memory using N x W –bit chips

How many 1024x 8 RAM chips are needed to provide a memory capacity of 2048 x 8?

Case 1: If $N' > N$ & $W' = W$

Increase number of words by the factor of $p = \left\lceil \frac{N'}{N} \right\rceil$

How many 1024x 4 RAM chips are needed to provide a memory capacity of 1024 x 8?

Case 2:

If $N' = N$ & $W' > W$

Increase the word size of a Memory by a factor of $q = \left\lceil \frac{W'}{W} \right\rceil$

How many 1024x 4 RAM chips are needed to provide a memory capacity of 2048 x 8?

Case 3: If $N' > N$ & $W' > W$

Increase number of words by the factor of p &
Increase the word size of a Memory by a factor of q

Memory design – Increasing the word size

- Problem - 1
- Design 128 × 16 - bit RAM using 128 × 4 - bit RAM
- Solution: p = 128 / 128 = 1; q = 16 / 4 = 4
- Therefore, p × q = 1 × 4 = 4 memory chips of size 128 × 4 are required to construct 128 × 16 bit RAM

S.No	Memory Type	N × W	$N^1 \times W^1$	p	q	p * q	x	y	z	Total
1	RAM	128 × 4	128 × 16	1	4	4	7	0	0	7

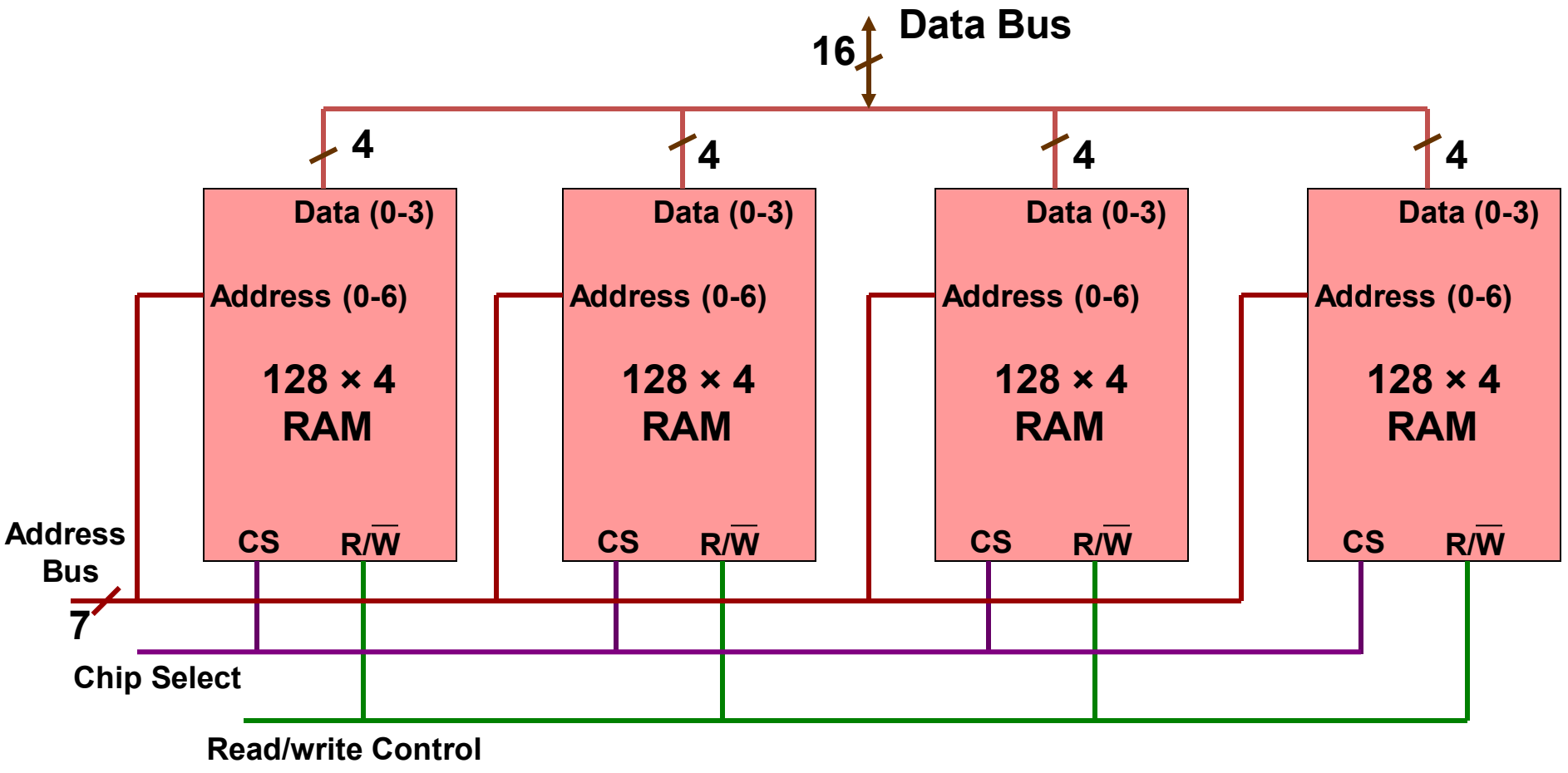
x – number of address lines
y ($p = 2^y$) – to select one among the same type of memory
z – to select the type of memory

Memory Address Map

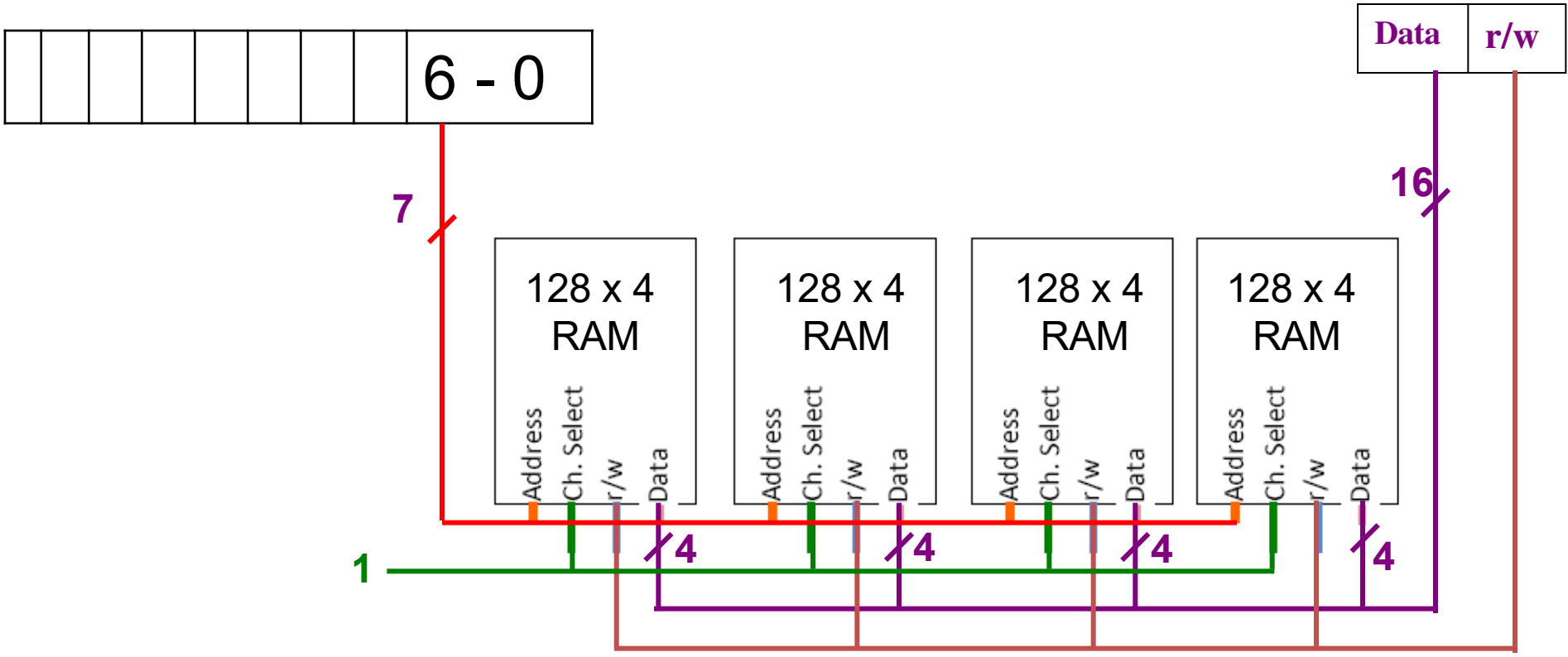
Component	Hexadecimal address		Address Bus														
	From	To	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM 1.1	0000	007F																
RAM 1.2	0000	007F										x	x	x	x	x	x	x
RAM 1.3	0000	007F										x	x	x	x	x	x	x
RAM 1.4	0000	007F										x	x	x	x	x	x	x

Substitute 0 in place of x to get 'From' address and 1 to get 'To' address

Memory design – Increasing the word size



Memory Design



Memory Design – Increasing the number of words

- Problem - 2
- Design 1024 × 8 - bit RAM using 256 × 8 - bit RAM
- Solution: p = 1024 / 256 = 4; q = 8 / 8 = 1
- Therefore, p × q = 4 × 1 = 4 memory chips of size 256 × 8 are required to construct 1024 × 8 bit RAM

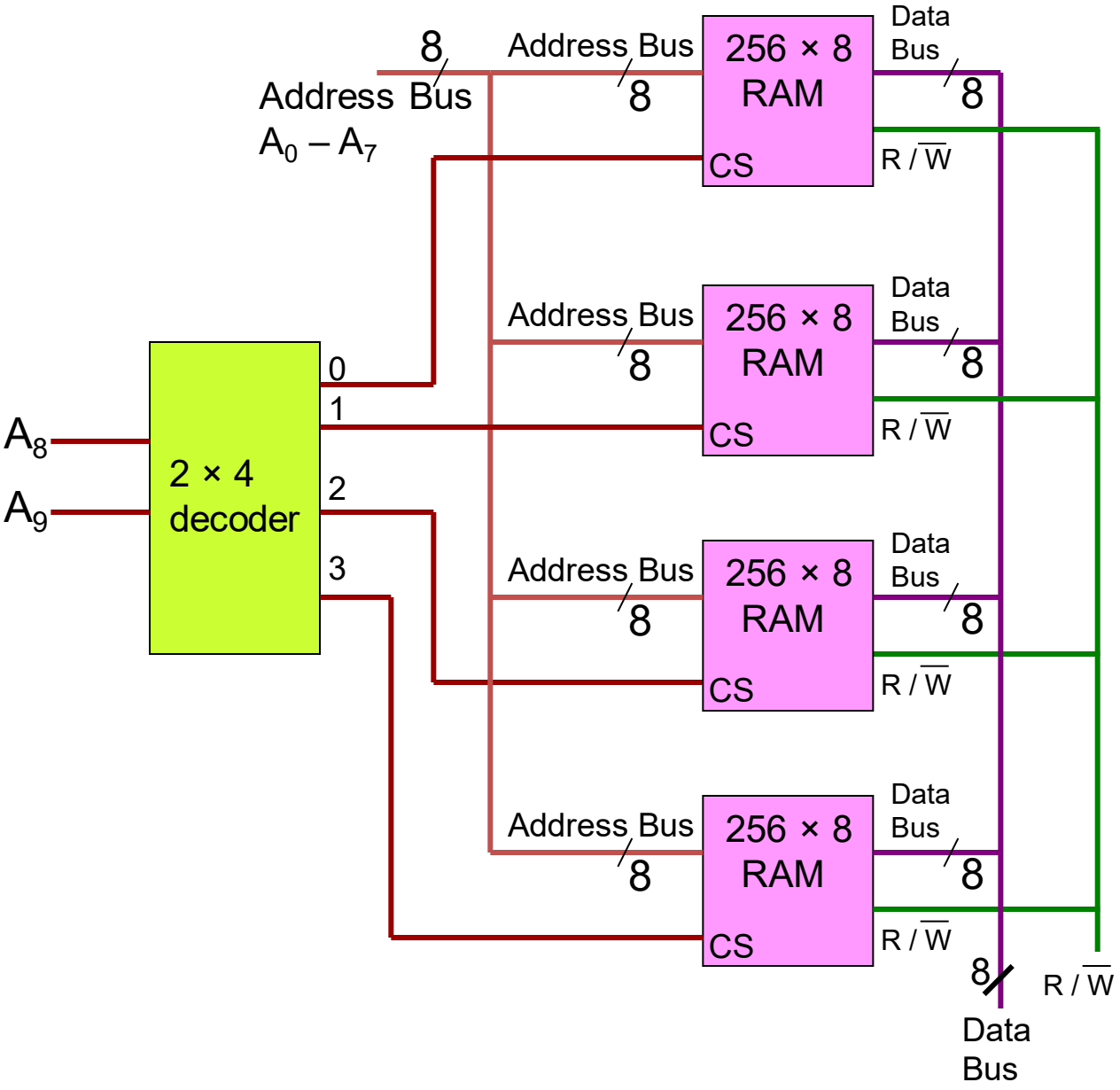
S.NO	Memory	N x W	N^1 x W^1	P	q	p * q	x	y	z	Total
1	RAM	256 × 8	1024 × 8	4	1	4	8	2	0	10
2										
3										
4										

Memory Address Map

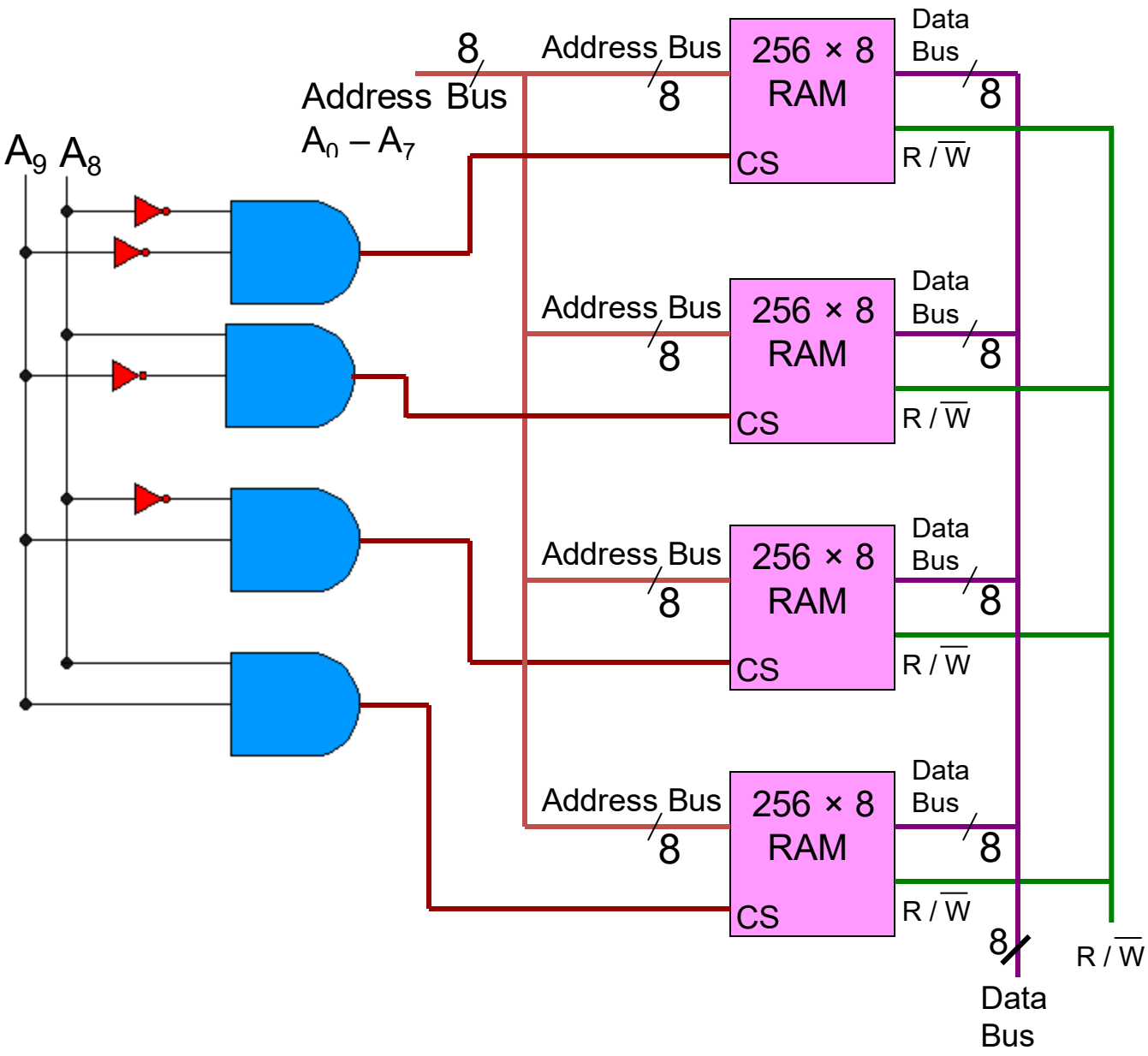
Component	Hexadecimal address		Address Bus															
	From	To	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM 1	0000	00FF							0	0	x	x	x	x	x	x	x	x
RAM 2	0100	01FF							0	1	x	x	x	x	x	x	x	x
RAM 3	0200	02FF							1	0	x	x	x	x	x	x	x	x
RAM 4	0300	03FF							1	1	x	x	x	x	x	x	x	x

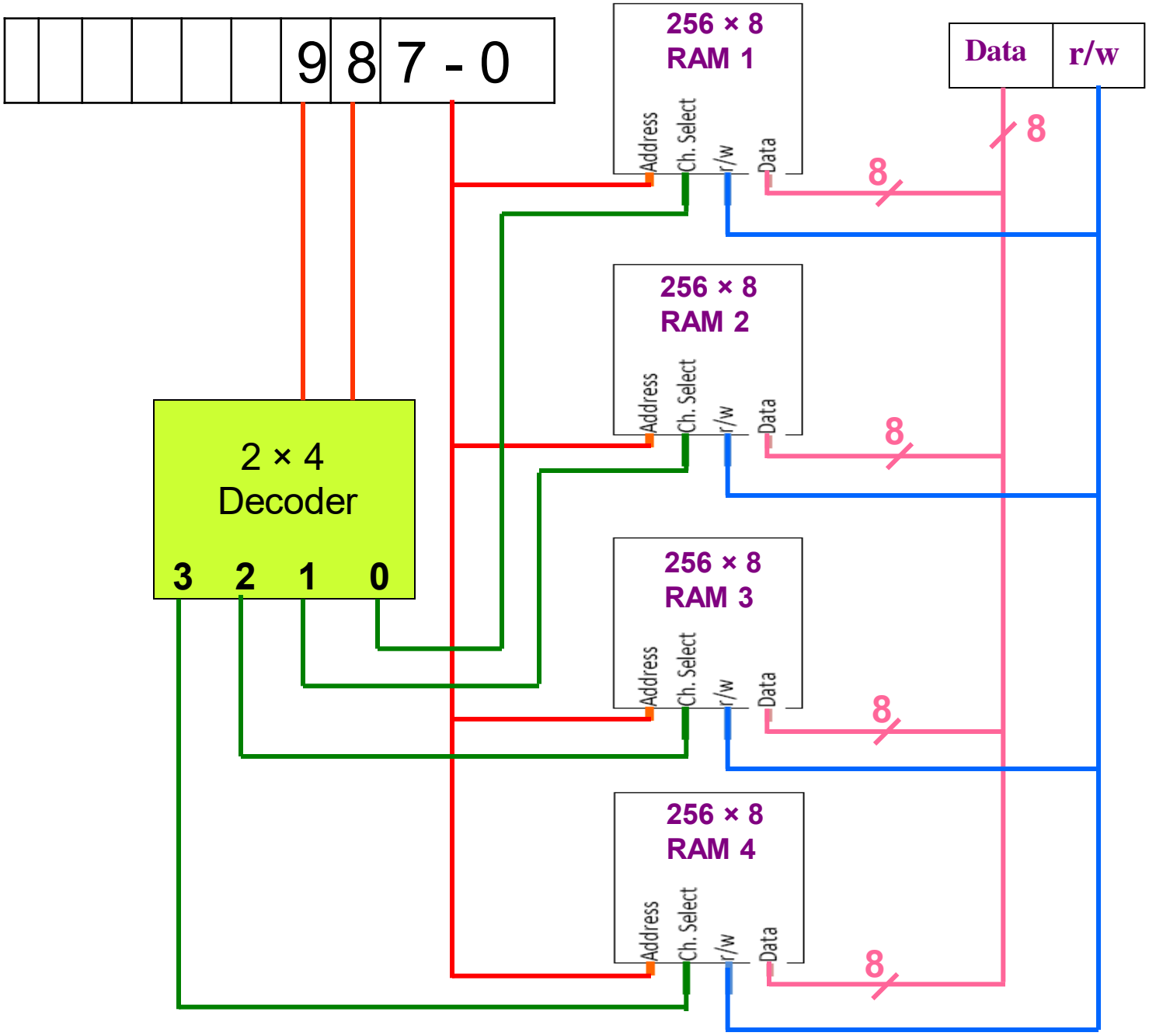
Substitute 0 in place of x to get 'From' address and 1 to get 'To' address

Memory Design – Increasing the number of words



Design with gates




9 8 7 - 0
256 × 8
RAM 1
256 × 8
RAM 2
256 × 8
RAM 3
256 × 8
RAM 4
Address
Ch. Select
r/w
Data
Data
r/w
8
2 × 4
Decoder
3 2 1 0

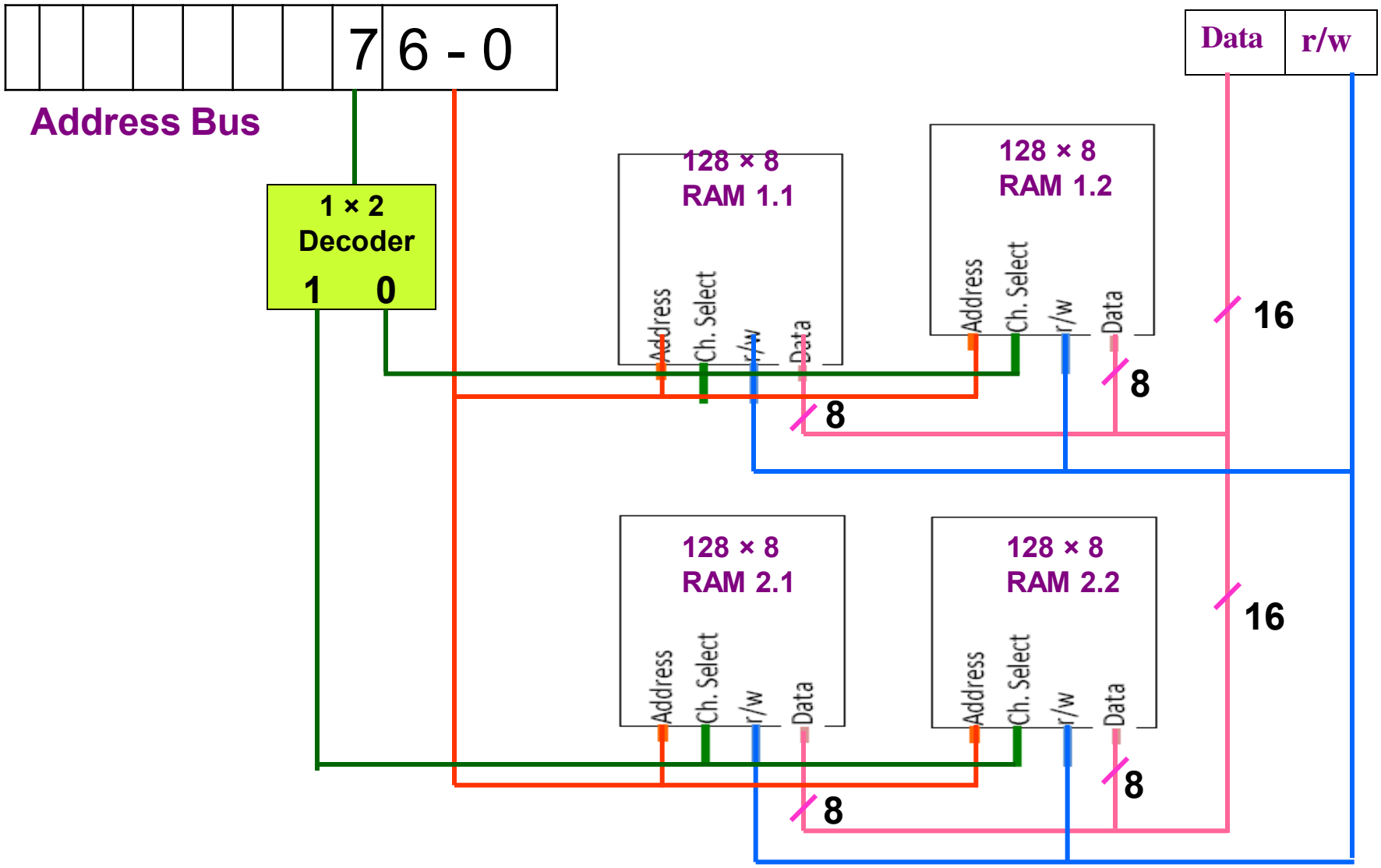
Memory Design

- Problem - 3
- Design 256 × 16 – bit RAM using 128 × 8 – bit RAM chips

S.NO	Memory	N x W	N^1 x W^1	P	q	p * q	x	y	z	Total
1	RAM	128 × 8	256 × 16	2	2	4	7	1	0	8
2										
3										
4										

Memory Address Map

Component	Hexadecimal address		Address Bus															
	From	To	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM 1.1	0000	007F									0	x	x	x	x	x	x	x
RAM 1.2	0000	007F									0	x	x	x	x	x	x	x
RAM 2.1	0080	00FF									1	x	x	x	x	x	x	x
RAM 2.2	0080	00FF									1	x	x	x	x	x	x	x


7 6 - 0
Address Bus
Data
r/w
1 × 2
Decoder
1 0
128 × 8
RAM 1.1
128 × 8
RAM 1.2
128 × 8
RAM 2.1
128 × 8
RAM 2.2
Address
Ch. Select
r/w
Data
16
8
8
16
8
8

Memory Design

- Problem - 4
- Design 256 × 16 – bit RAM using 256 × 8 – bit RAM chips and 256 × 8 – bit ROM using 128 × 8 – bit ROM chips.

Memory Design

- Problem - 4
- Design 256 × 16 – bit RAM using 256 × 8 – bit RAM chips and 256 × 8 – bit ROM using 128 × 8 – bit ROM chips.

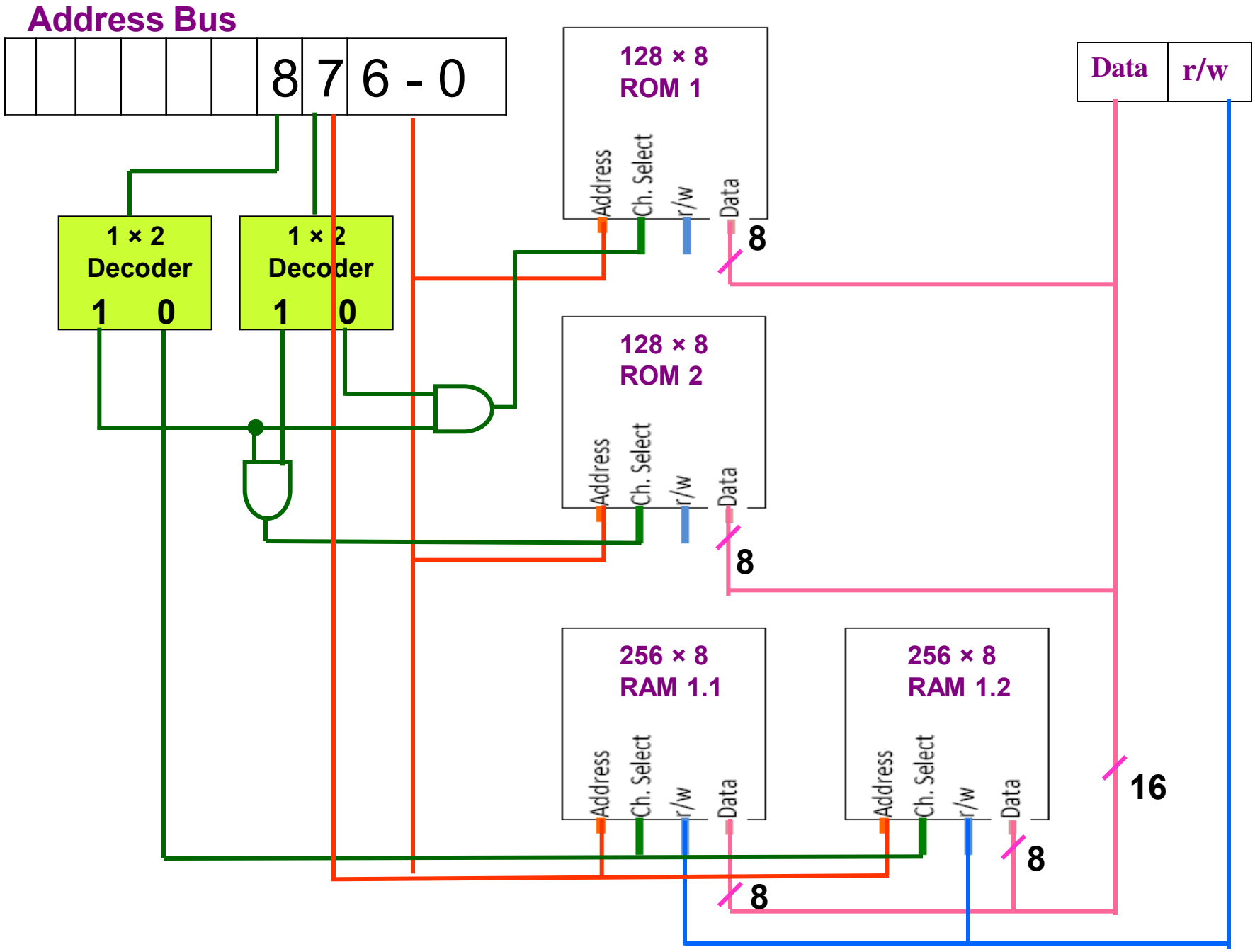
Memory Design

- Problem - 4
- Design 256 × 16 – bit RAM using 256 × 8 – bit RAM chips and 256 × 8 – bit ROM using 128 × 8 – bit ROM chips.

S.NO	Memory	N x W	N^1 x W^1	P	q	p * q	x	y	z	Total
1	RAM	256 × 8	256 × 16	1	2	2	8	0	1	9
2	Rom	128 × 8	256 × 8	2	1	2	7	1	1	9
3										
4										

Memory Address Map

Component	Hexadecimal address		Address Bus															
	From	To	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM 1.1	0000	00FF								0	x	x	x	x	x	x	x	x
RAM 1.2	0000	00FF								0	x	x	x	x	x	x	x	x
ROM 1	0100	017F								1	0	x	x	x	x	x	x	x
ROM 2	0180	01FF								1	1	x	x	x	x	x	x	x


Address Bus
8 7 6 - 0
1 × 2 Decoder
1 0
1 × 2 Decoder
1 0
128 × 8 ROM 1
Address
Ch. Select
r/w
Data
8
128 × 8 ROM 2
Address
Ch. Select
r/w
Data
8
256 × 8 RAM 1.1
Address
Ch. Select
r/w
Data
8
256 × 8 RAM 1.2
Address
Ch. Select
r/w
Data
8
Data
r/w
16

Memory design

- Problem – 5
- A computer employs RAM chips of 128 x 8 and ROM chips of 512 x 8. The computer system needs 256 bytes of RAM, 1024 x 16 of ROM, and two interface units with 256 registers each. A memory mapped I/O configuration is used. The two higher - order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.
- a. Compute total number of decoders are needed for the above system?
- b. Design a memory-address map for the above system
- c. Show the chip layout for the above design

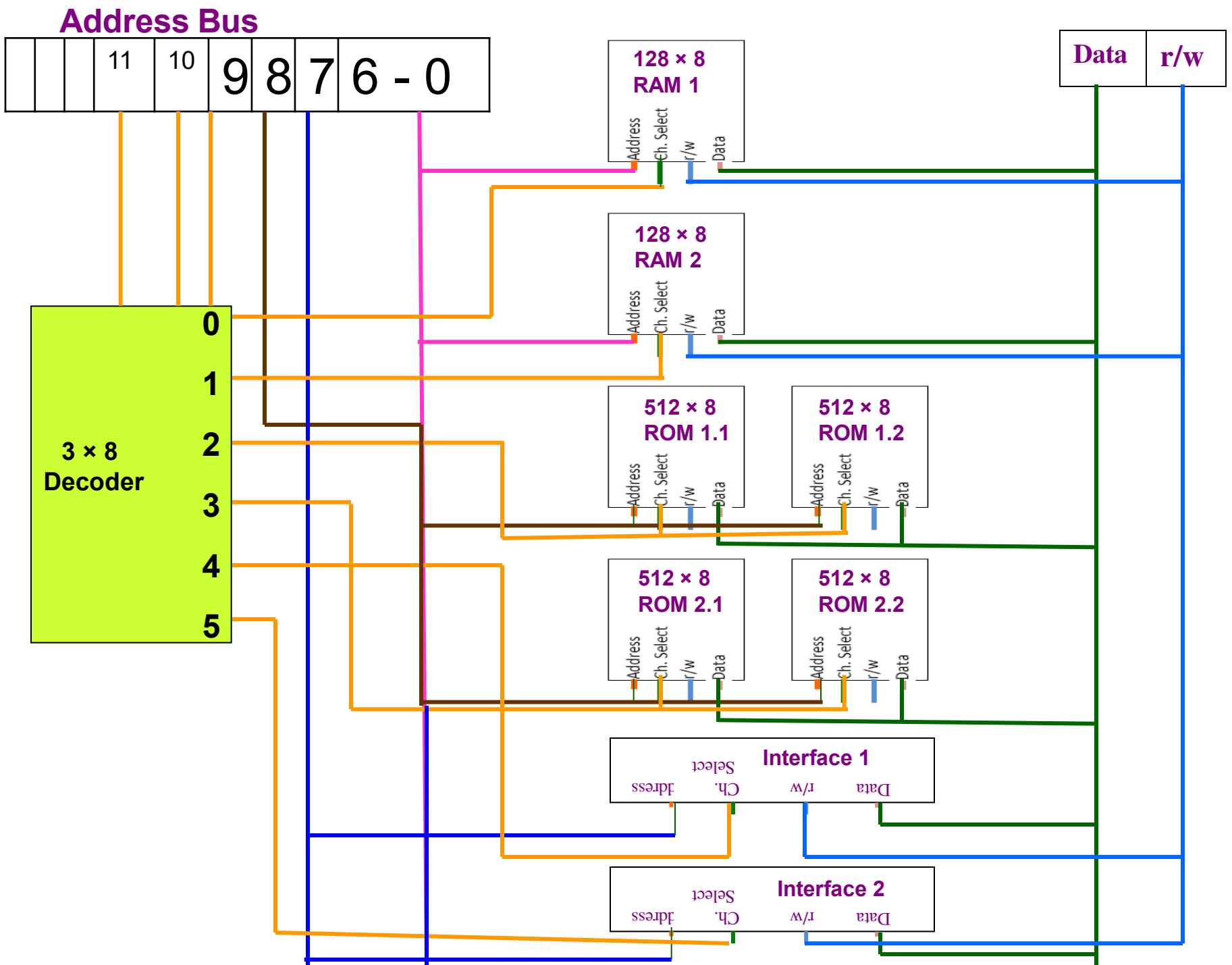
Requirements

S.NO	Memory	N x W	N^1 x W^1	P	q	p * q	x	y	z	Total
1	RAM	128 × 8	256 × 8	2	1	2	7	1	2	10
2	ROM	512 × 8	1024 × 16	2	2	4	9	1	2	12
3	Interface	256		2	1	2	8	1	2	11
4										

q is 1 always for interfaces.
Number of registers = 2^x
P = number of interfaces
Number of data lines = size of registers

Memory Address Map

Component	Hexadecimal Address		Address Bus												
	From	To	15 - 12	11	10	9	8	7	6	5	4	3	2	1	0
RAM1	0000	007F		0	0	0	0	0	x	x	x	x	x	x	x
RAM2	0200	027F		0	0	1	0	0	x	x	x	x	x	x	x
ROM1.1	0400	05FF		0	1	0	x	x	x	x	x	x	x	x	x
ROM1.2	0400	05FF		0	1	0	x	x	x	x	x	x	x	x	x
ROM2.1	0600	07FF		0	1	1	x	x	x	x	x	x	x	x	x
ROM2.2	0600	07FF		0	1	1	x	x	x	x	x	x	x	x	x
Interface1	0800	08FF		1	0	0	0	x	x	x	x	x	x	x	x
Interface2	0A00	0AFF		1	0	1	0	x	x	x	x	x	x	x	x


Address Bus
11
10
9
8
7
6 - 0
Data
r/w
128 × 8
RAM 1
128 × 8
RAM 2
512 × 8
ROM 1.1
512 × 8
ROM 1.2
512 × 8
ROM 2.1
512 × 8
ROM 2.2
Address
Ch. Select
r/w
Data
3 × 8
Decoder
0
1
2
3
4
5
Interface 1
Interface 2
Data
r/w
Ch. Select
Address

Example

A computer employs RAM chips of 1024 x 8 and ROM chips of 2048 x 4. The computer system needs 2K bytes of RAM, and 2K bytes of ROM and an interface unit with 256 registers each. A memory-mapped I/O configuration is used. The two higher -order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface.

a). How many RAM and ROM chips are needed?

b). How many lines of the address bus must be used to access Computer system memory? How many of these lines will be common to all chips?

c). How many lines must be decoded for chip select? Specify the size of the decoder

d). Draw a memory-address map for the system and Give the address range in hexadecimal for RAM, ROM

e). Develop a chip layout for the above said specifications

Example 2

A computer employs RAM chips of 1024 x 8 and ROM chips of 2048 x 4. The computer system needs 2K x 16 of RAM, and 2K x 16 ROM and an interface unit with 256 registers each. A memory-mapped I/O configuration is used. The two higher -order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface..

a). How many RAM and ROM chips are needed?

b). How many lines of the address bus must be used to access total memory? How many of these lines will be common to all chips?

c). How many lines must be decoded for chip select? Specify the size of the decoder

d). Draw a memory-address map for the system.

e). Draw a memory-address map for the system and Give the address range in hexadecimal for RAM, ROM

f). Develop a chip layout for the above said specifications

References

Text Book(s)

- M. M. Mano, Computer System Architecture, Prentice-Hall,2004
- J. P. Hayes, Computer system architecture, McGraw Hill,2000