Assignment-2	EE204 - Analog Circuits	4th Feb 2019
Submission Deadline-17.00 11th Feb, 2019	Submission Protocol: Notebook submission	Comment: Partial

1.A	Consider the differential amplifier we have discussed in the class with the following parameters: $g_{m1} = g_{m2} = 2$ mS, $R_{D1} = R_{D2} = 20$ kΩ, $R_{SS} = 200$ kΩ, $r_{01} = r_{02} = \infty$. I. Find out the differential gain (A_{DM}) of the amplifier. II. Find out the common mode to differential model conversion (A_{CM-DM}) when: (a) $g_{m1} = g_{m0}+\Delta g_m/2$ and $g_{m2} = g_{m0}+\Delta g_m/2$ where $g_{m0} = 2$ mS and $\Delta g_m = 0.2$ mS and all other parameters remain same. Find out CMRR. (b) $R_{d1} = R_{D0}+\Delta R_D/2$ and $R_{D2} = R_{D0}+\Delta R_D/2$ where $R_{D0} = 20$ kΩ and $\Delta R_D = 2$ kΩ and all other parameters remain same. Find out CMRR. (c) Both g_m and R_d are varying as in (a) and (b). (d) Repeat (a), (b) and (c) when $r_{01} = r_{02} = 50$ kΩ. Also find out A_{DM} and CMRR for this case. Comment on the effect of the finite output resistance of the transistors. (e) Find out the sensitivity of the A_{CM-DM} for a mismatch of R_D and r_0. Also qualitatively explain your observations obtained from the calculations.
1.B	Consider nMOS with the following characteristics: k' = 1 mA/V^2, $V_T = 1$ V, $R_D = 10$ kΩ, λ = 0. I. Design a perfectly matched differential amplifier with multiple instances of the above nMOS for a bias current of $I_{SS} = 8$ mA and $R_{SS} = \infty$. II. Plot V_{O1}-V_{O2} versus V_{IN1}-V_{IN2}. Plot in any software and attach the plot. III. Plot I_{DS1}-I_{DS2} versus V_{IN1}-V_{IN2}. Plot in any software and attach the plot. IV. Find out A_{DM} for the first and second harmonic differential output as a function of the small signal differential input amplitude.