Experiment 3: VHDL Experiment

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1 Overview of the experiment

- The aim of this experiment is to get implement the four bit added we designed in experiment 2 on a krypton board.
- This experiment also serves to familiarize students with the interface between quartus and krypton to allow us to upload much more compicated designs onto the krypton board.
- The next section (Procedure) describes the procedure we use to perform the experiment, the
- We provide screen shots of gate level simulations proving that our four bit adder design works perfectly when actually implemented using gates. We also provide screenshots of our pin planner and the actual imlementation so that the reader can check the overlap of the encoded layout and the actual output.

2 Procedure

UrJTAG was used to connect PC to Krypton circuit board. To familiarize with the process of loading svf file we used the jtag interface to load the CPLD with a svf code for 4-bit-counter whose svf file was given to us well in

advance. The svf file was generated using Quartus Prime. In the process we also changed the settle time in the testbench file to 20ns to ensure expected response from the code. The implementation of the code was checked using netlist simulation. After ascertaining the correctness of our design, we generated the svf file which was parsed to the CPLD. In the Observations section, we upload the screenshots of transcripts, results and snapshot of CPLD when loaded with Full adder and 4-bit-adder.

3 Output

3.1 Transcript Output

Here is a screen shot of the transcript output showing that our design works on a gate level implementation.

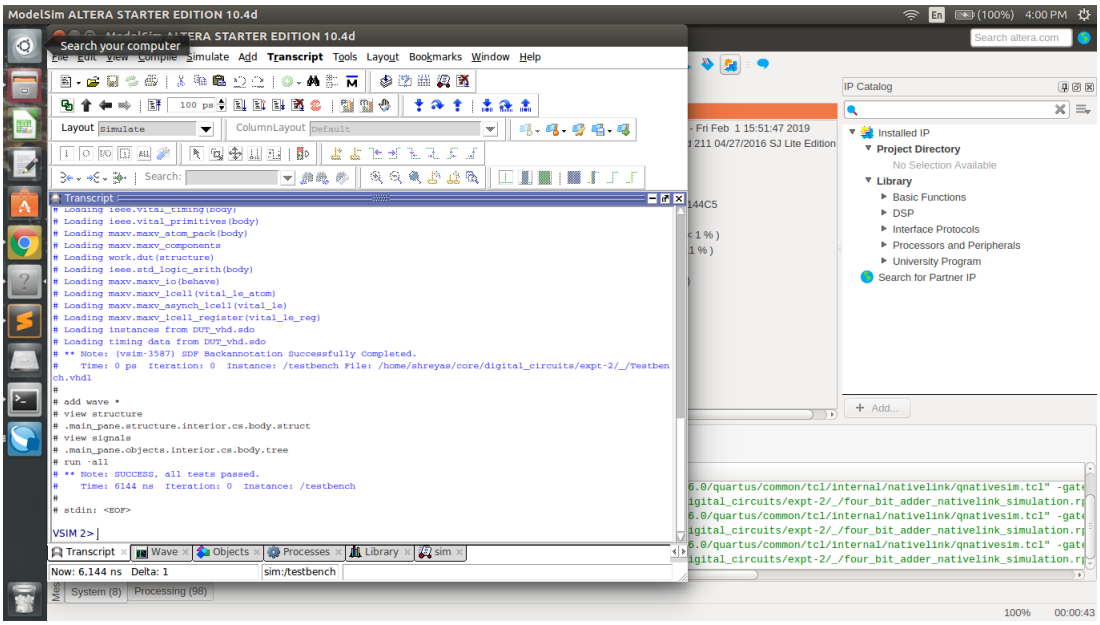

Figure 1: Gate Level Simulation Transcript Result

3.2 Pin Planned Diagram

This shows the bijection between the design implemented in VHDL and the pin numbers of the CPLD krpyton board.

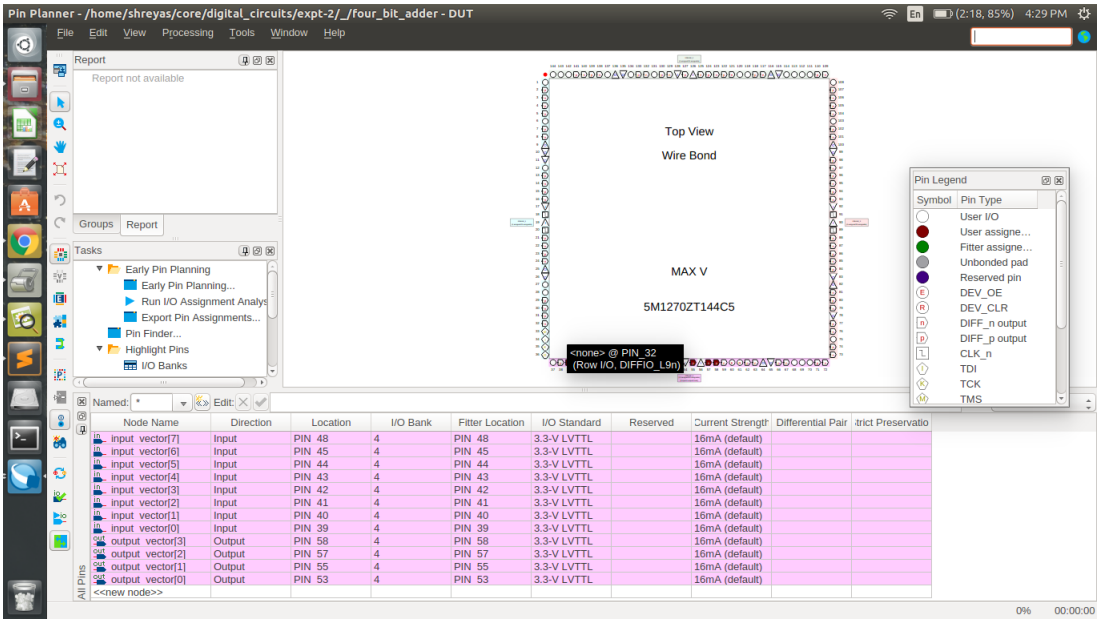

Figure 2: PIN planner diagram of the implemetation

3.3 Krypton Board

Here is a diagram of the krypton board with input to adder 0001 (S1 S2 S3 S4) and 0010 (S5 S6 S7 S8) giving an output of 0011 (LED1 LED2 LED3 LED4).
Reader can use this image with our earlier pin planner diagram to verify that the adder is working correctly.

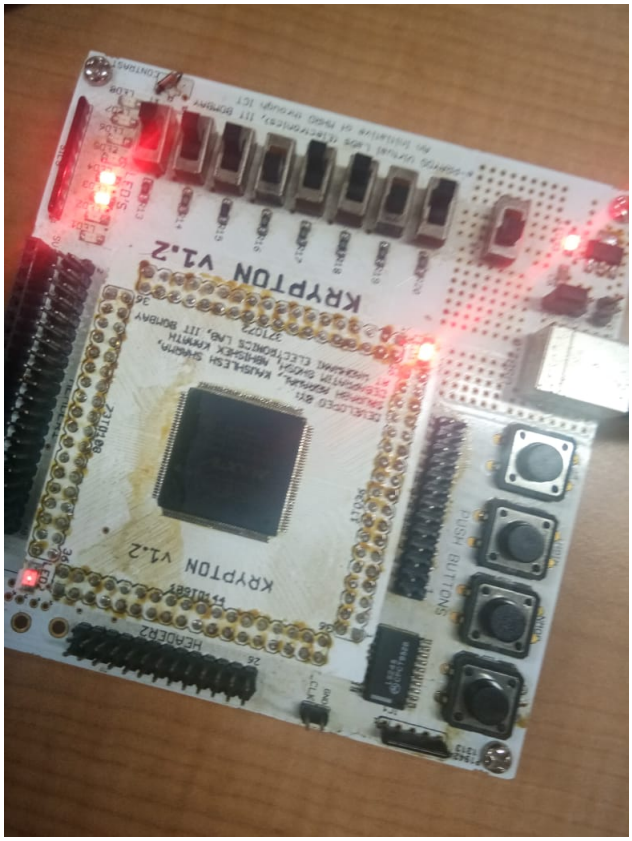

Figure 3: Krypton board adding 0001 and 0010