## Phase Sensitive Detection( Lock-in-amplifier) Applications

#### Wadhwani Electronics Lab

Department of Electrical Engineering Indian Institute of Technology Bombay Mar 2016 Updated: Jan 2019

## Phase sensitive detection (Session 2)

We have studied the principle of phase detection in the last week. In this session, we will study two applications of phase sensitive detection:

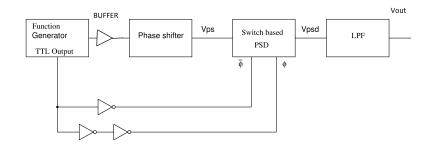
- To extract capacitance and resistance using a single PSD system.
- To measure the signal buried in noise.

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## Phase sensitive detection (Session 2)

You will use the preassembled circuit from the last week with following blocks:

- 1 Buffer: 741 based voltage follower
- 2 Phase shifter
- 3 Switch driving circuit: generating complementary clock signals using 74C04
- 4 Switch based phase sensitive detector
- 5 Low pass filter



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## Testing the last week's PSD circuit

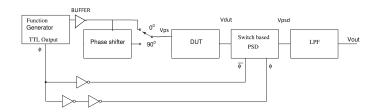
Before the actual measurements, we shall quickly test the last week's circuit on your breadboard.

- Apply  $1V_{p-p}$ , 1kHz sinusoidal signal from CH1 of AFG.
- Connect the TTL output of AFG to TTL input to the switch driving circuit.
- Using oscilloscope, make sure that you get appropriate signals at the output of each block.

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# Phase sensitive detection: Extracting capacitance and resistance using a single PSD system

The simplified block diagram for this experiment is shown below.

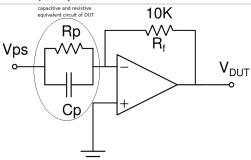


- The main blocks of the PSD system are the same as we did in the last week.
- For this application, we need either  $0^0$  shifted signal (the input signal from AFG) or  $90^0$  phase shifted signal (from the phase shifter) with respect to reference signal. Hence the phase shifter can be adjusted for  $90^0$  and a wire can be used to switch to between  $0^0$  or  $90^0$  phase shift.
- The DUT block consists of the actual "Device Under Test" (the parallel combination of  $R_p$  and Cp) with an inverting opamp.

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## Testing DUT block

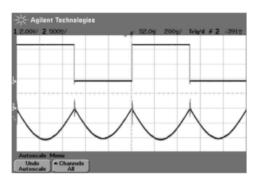
- Connect the DUT circuit is as shown below. Use  $R_p=10$ K and  $C_p=10$  nF. We shall test this block for  $0^0$  phase shift for the sake of simplicity.
- Derive the expression for  $V_{DUT}$  in terms of  $R_p$ ,  $C_p$ ,  $R_f$ , and  $V_{ps}$ .
  - Connect only  $R_p$  first by leaving the terminals for capacitor open and observe  $V_{DUT}$ . The circuit acts as an inverting amplifier with gain -1.
  - Now connect only the capacitor. What do you expect at the output? Observe  $V_{DUT}$  with respect to  $V_{ps}$ .
  - Now connect both  $R_p$  and  $C_p$  and observe  $V_{DUT}$  with respect to  $V_{ps}$ . What should you get at the output of DUT block? Verify with your estimated values(amplitude and phase).



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## Testing the Switch Based PSD

- Connect only  $R_p$  (10K) in the DUT circuit.
- Connect the output of DUT to the input of PSD.
- ullet Check the two reference signals  $\phi$  and  $\overline{\phi}$  .
- Observe  $V_{psd}$  with respect to  $\phi$ .
- You should get negative rectified waveform as shown below (this is due to an additional inverting amplifier with gain -1 in DUT block).



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## Testing the Low pass filter

- Connect the output of the phase sensitive detector as input to LPF.
- Measure the output of LPF  $(V_{out})$ . What is the expected output? Its value should be around  $\frac{2V_m}{\pi}$ , where  $V_m$  is the amplitude of the input signal. This is the maximum output voltage of the lock-in-amplifier for the current values of  $R_p$  and  $C_p$ . Observe the waveform  $V_{psd}$  on DSO with maximum sensitivity.
- If you get any abrupt transition in the  $V_{\it psd}$  waveform, it is because of some inherent phase difference between CH1 and TTL output of the AFG. In such a case, adjust the phase of the CH1 output (CH1 menu) such that you get the complete full wave rectified output.
- Now put the switch in 90<sup>0</sup> position and observe the output of PSD on DSO and that of LPF on DMM. You should measure the output voltage closed to zero. (Why?) If it is not so, fine tune the potentiometer of the phase shifter to read minimum voltage at the output of LPF.
- Show the readings and waveforms for both the phase angles to your TA.

#### This completes the testing of the PSD CIRCUIT!

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## Extracting the values of $R_p$ and $C_p$

- We shall now evaluate the performance of our lock-in-amplifier by extracting capacitance  $C_p$  and loss-conductance (in terms of  $R_p$ ) of a medium or a sensor. We shall use a parallel combination of known  $R_p$  and  $C_p$  for measurement and will verify the measurement.
- $\bullet$  Put the switch in  $0^{\circ}$  position to measure resistance and in  $90^{\circ}$  position to measure capacitance. (Why?)
- Connect  $R_p$  (10K) only. Measure the output of LPF on DMM. Use this value of  $V_{out}$  as  $V_{in}$  for the calculations as dc equivalent of the input signal.

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## Extracting the values of $R_p$ and $C_p$ continued...

- Now connect  $C_p$  (10nF) also and observe  $V_{psd}$  with respect to  $\phi$  and measure the output voltage of LPF using DMM.
- Repeat the measurements for all combinations of  $R_p$  and  $C_p$  of values 4.7K,10K, 10nF, and 22nF.
- Tabulate the observations and calculate the values of  $R_p$  and  $C_p$  in each case and complete the table. Compare the calculated values with actual values of  $R_p$  and  $C_p$  measured using DMM/ LCR meter.

$$R_p = R_f \frac{V_{in}}{V_{out}}$$

where,  $V_{out}$  is measured at  $0^0$  phase shift

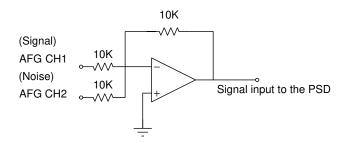
$$C_p = \frac{V_{out}}{\omega R_f V_{in}}$$

where,  $V_{out}$  is measured at  $90^{\circ}$  phase shift

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## Measurement of signal buried in noise

- In this part of the experiment, we shall see how the output of lock-in-amplifier is insensitive to noise signal.
- Connect a simple opamp adder (that adds signal and noise) on your breadboard.
- Apply  $1V_{p-p}$ , 1kHz signal and  $1V_{p-p}$ , 500 Hz as noise input.
- Observe the output waveform of this adder circuit on DSO. Can you distinguish between signal and noise?



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## Measurement of the signal buried in noise continued..

- Now connect the output of this adder circuit as signal input to the buffer.
- Bypass the DUT block and connect  $V_{ps}$  directly as input to switch based PSD block.
- Observe the output of PSD on DSO and that of LPF on DMM for all the readings.
- Vary the noise voltage from  $1V_{p-p}$  to  $4V_{p-p}$  in steps of  $1V_{p-p}$  keeping frequency constant at 500Hz. Note the output of the LPF in each case.
- Now keep the noise amplitude constant at  $1V_{p-p}$  and vary the frequency of noise signal from 500Hz to 1.5 kHz in the steps of 100 Hz. Note the output of the LPF in each case.
- Tabulate your observations.
- What is the effect of changing the noise frequency and amplitude? What do you observe at the noise frequencies close to the signal frequency?

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## What should you report

#### Part 1:Extracting the values of $R_p$ and $C_p$

- Take the pictures of the following waveforms and include them in the report:
  - $V_{ps}$  and  $\phi$  at  $90^{\circ}$  phase shift
  - $\bullet$  The two reference signals  $\phi$  and  $\overline{\phi}$
  - $V_{psd}$  with respect to  $\phi$  with only  $R_p$  connected
    - at phase shift 0<sup>0</sup>.
    - at phase shift 90<sup>0</sup>.
- Your observations for the measurement of  $R_p$  and  $C_p$  in tabular form.

#### Part 2: Measurement of signal buried in noise

Your observations in tabular form.

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### circuit layout on breadboard

