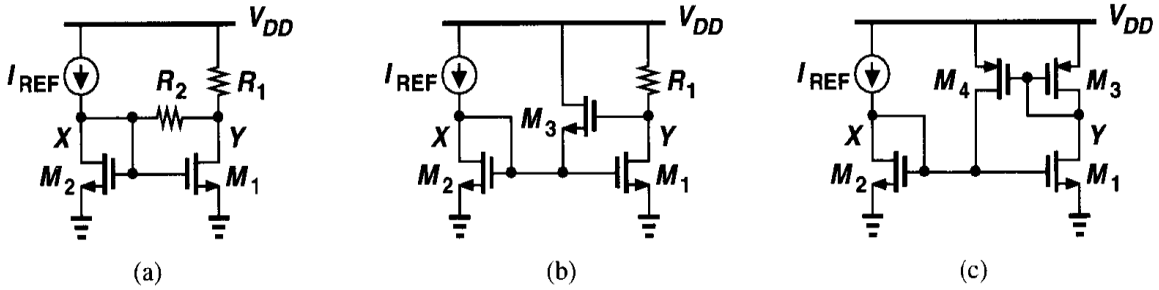
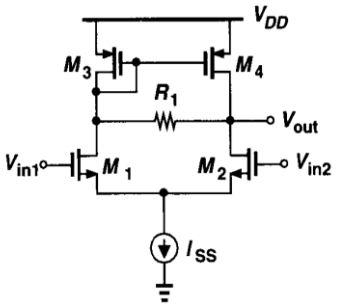
Assigment-3	EE204 Analog Circuits	14th Feb 2019
Submission Deadline-17.00 22nd Feb, 2019	Submission Protocol: Notebook submission. Plots through Moodle	Comment: None

1. For each circuit shown below, sketch V_x and V_y as a function of I_{REF}.



2. Due to a manufacturing defect, a large parasitic resistance, R_1, has appeared in the circuit as shown below. Calculate the gain of the circuit.



3. Assuming all of the circuits shown in figure below are symmetric, sketch V_{out} as (a) V_{in1} and V_{in2} vary differentially from zero to VDD, and (b) Vin1 and Vin2 are equal and they vary from zero to $_{VDD}$.