EE214 (24,25 January, 2019)
Design and simulate a four bit adder

January 23, 2019

You are asked to design a four bit adder. The inputs to this adder are two 4-bit numbers, and the output of the adder is a 4-bit sum.

You may use the gates that have already been described in VHDL in order to construct your adder.

1. Work out the design of your adder (in the form of equations, structure or a combination of the two, as you wish). Hint: ripple-carry adder.
2. Describe the entity/architecture for your design (in VHDL).
3. Customize the generic test bench in order to simulate your VHDL description. You will need to generate a trace file for this test bench.
4. Simulate your design description using the generic test bench to confirm that it is working as expected.
5. Along with the report, submit your code (upload only) and the simulation log.
6. This laboratory experiment needs to be finished in one session.