2.4 DIFFERENCE AMPLIFIERS

Having studied the two basic configurations of op-amp circuits together with some of their direct applications, we are now ready to consider a somewhat more involved but very important application. Specifically, we shall study the use of op amps to design difference or differential amplifiers.[2] A difference amplifier is one that responds to the difference between the two signals applied at its input and ideally rejects signals that are common to the two inputs. The representation of signals in terms of their differential and common-mode components was given in Fig. 2.4. It is repeated here in Fig. 2.15 with slightly different symbols to serve as the input signals for the difference amplifiers we are about to design. Although ideally the difference amplifier will amplify only the differential input signal v_{Id} and reject completely the common-mode input signal v_{Icm}, practical circuits will have an output voltage v_O given by

$$v_O = A_d v_{Id} + A_{cm} v_{Icm} \tag{2.13}$$

where A_d denotes the amplifier differential gain and A_{cm} denotes its common-mode gain (ideally zero). The efficacy of a differential amplifier is measured by the degree of its rejection of common-mode signals in preference to differential signals. This is usually quantified by a measure known as the **common-mode rejection ratio (CMRR),** defined as

$$\text{CMRR} = 20 \log \frac{|A_d|}{|A_{cm}|} \tag{2.14}$$

The need for difference amplifiers arises frequently in the design of electronic systems, especially those employed in instrumentation. As a common example, consider a transducer providing a small (e.g., 1 mV) signal between its two output terminals while each of the two wires leading from the transducer terminals to the measuring instrument may have a large interference signal (e.g., 1 V) relative to the circuit ground. The instrument front end obviously needs a difference amplifier.

Before we proceed any further we should address a question that the reader might have: The op amp is itself a difference amplifier; why not just use an op amp? The answer is that the very high (ideally infinite) gain of the op amp makes it impossible to use by itself.

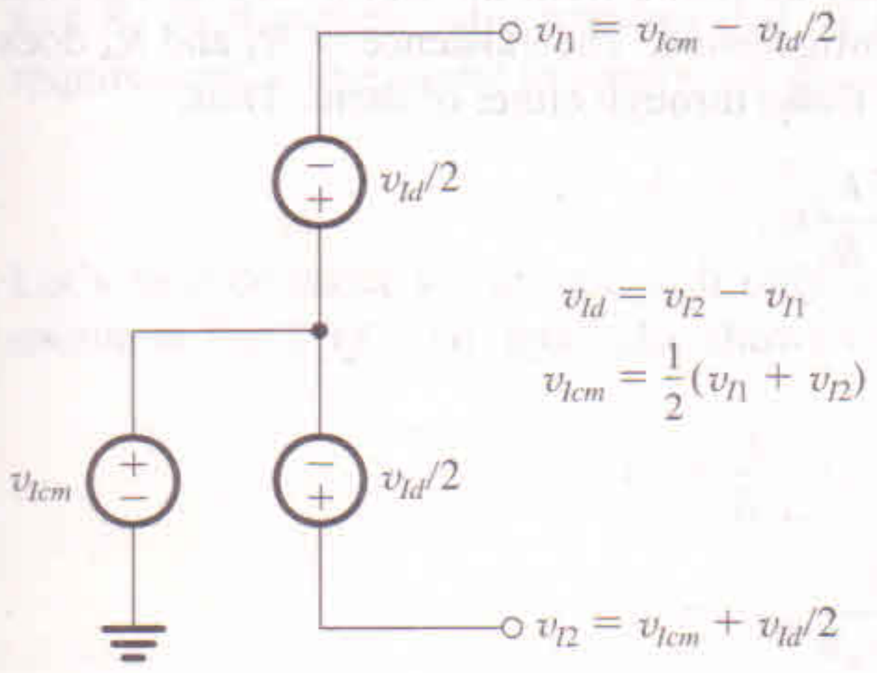

FIGURE 2.15 Representing the input signals to a differential amplifier in terms of their differential and common-mode components.

[2] The terms *difference* and *differential* are usually used to describe somewhat different amplifier types. For our purposes at this point the distinction is not sufficiently significant. We will be more precise near the end of this section.

Rather, as we did before, we have to devise an appropriate feedback network to connect to the op amp to create a circuit whose closed-loop gain is finite, predictable, and stable.

2.4.1 A Single Op-Amp Difference Amplifier

Our first attempt at designing a difference amplifier is motivated by the observation that the gain of the noninverting amplifier configuration is positive, $(1 + R_2/R_1)$, while that of the inverting configuration is negative, $(-R_2/R_1)$. Combining the two configurations together is then a step in the right direction—namely, getting the difference between two input signals. Of course, we have to make the two gain magnitudes equal in order to reject common-mode signals. This, however, can be easily achieved by attenuating the positive input signal to reduce the gain of the positive path from $(1 + R_2/R_1)$ to (R_2/R_1). The resulting circuit would then look like that shown in Fig. 2.16, where the attenuation in the positive input path is achieved by the voltage divider (R_3, R_4). The proper ratio of this voltage divider can be determined from

$$\frac{R_4}{R_4 + R_3}\left(1 + \frac{R_2}{R_1}\right) = \frac{R_2}{R_1}$$

which can be put in the form

$$\frac{R_4}{R_4 + R_3} = \frac{R_2}{R_2 + R_1}$$

This condition is satisfied by selecting

$$\frac{R_4}{R_3} = \frac{R_2}{R_1} \tag{2.15}$$

This completes our work. However, we have perhaps proceeded a little too fast! Let's step back and verify that the circuit in Fig. 2.16 with R_3 and R_4 selected according to Eq. (2.15) does in fact function as a difference amplifier. Specifically, we wish to determine the output voltage v_O in terms of v_{I1} and a v_{I2}. Toward that end, we observe that the circuit is linear, and thus we can use superposition.

To apply superposition, we first reduce v_{I2} to zero—that is, ground the terminal to which v_{I2} is applied—and then find the corresponding output voltage, which will be due entirely to v_{I1}. We denote this output voltage v_{O1}. Its value may be found from the circuit in Fig. 2.17(a), which we recognize as that of the inverting configuration. The existence of R_3 and R_4 does not affect the gain expression, since no current flows through either of them. Thus,

$$v_{O1} = -\frac{R_2}{R_1} v_{I1}$$

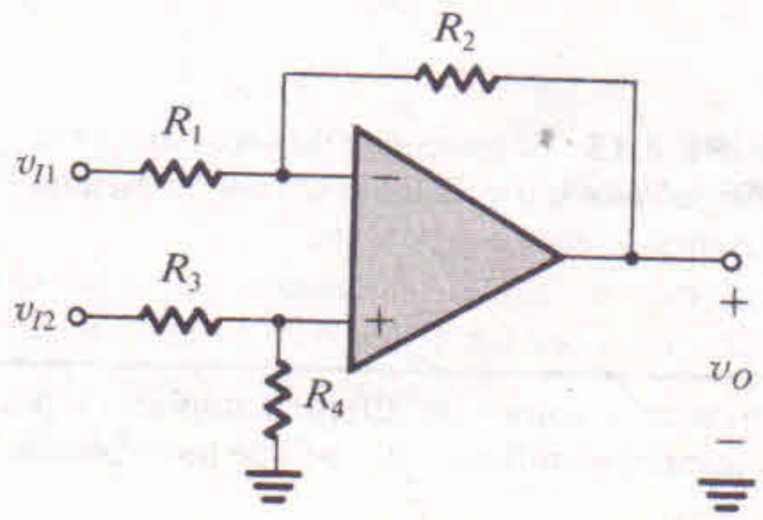

FIGURE 2.16 A difference amplifier.

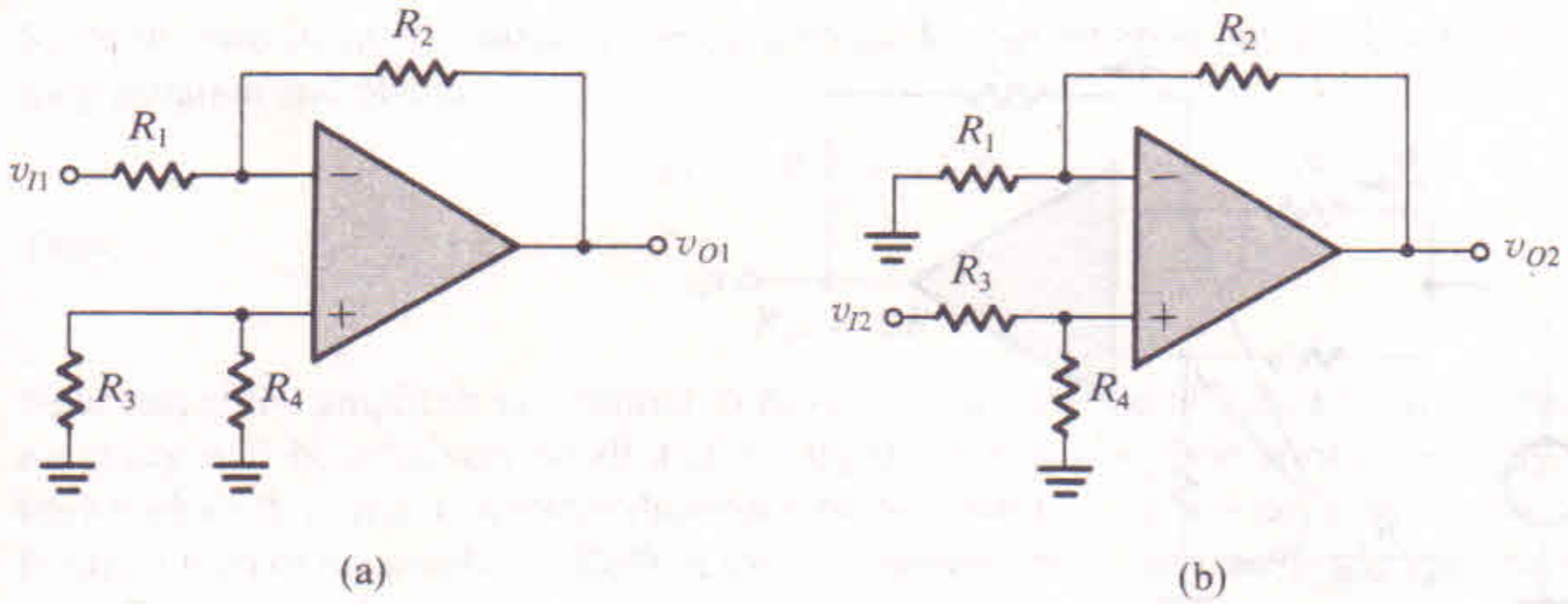

FIGURE 2.17 Application of superposition to the analysis of the circuit of Fig. 2.16.

Next, we reduce v_{I1} to zero and evaluate the corresponding output voltage v_{O2}. The circuit will now take the form shown in Fig. 2.17(b), which we recognize as the noninverting configuration with an additional voltage divider, made up of R_3 and R_4, connected to the input v_{I2}. The output voltage v_{O2} is therefore given by

$$v_{O2} = v_{I2}\frac{R_4}{R_3 + R_4}\left(1 + \frac{R_2}{R_1}\right) = \frac{R_2}{R_1}v_{I2}$$

where we have utilized Eq. (2.15).

The superposition principle tells us that the output voltage v_O is equal to the sum of v_{O1} and v_{O2}. Thus we have

$$v_O = \frac{R_2}{R_1}(v_{I2} - v_{I1}) = \frac{R_2}{R_1}v_{Id} \tag{2.16}$$

Thus, as expected, the circuit acts as a difference amplifier with a differential gain A_d of

$$A_d = \frac{R_2}{R_1} \tag{2.17}$$

Of course this is predicated on the op amp being ideal and furthermore on the selection of R_3 and R_4 so that their ratio matches that of R_1 and R_2 (Eq. 2.15). To make this matching requirement a little easier to satisfy, we usually select

$$R_3 = R_1 \quad \text{and} \quad R_4 = R_2$$

Let's next consider the circuit with only a common-mode signal applied at the input, as shown in Fig. 2.18. The figure also shows some of the analysis steps. Thus,

$$\begin{aligned} i_1 &= \frac{1}{R_1}\left[v_{Icm} - \frac{R_4}{R_4 + R_3}v_{Icm}\right] \\ &= v_{Icm}\frac{R_3}{R_4 + R_3}\frac{1}{R_1} \end{aligned} \tag{2.18}$$

The output voltage can now be found from

$$v_O = \frac{R_4}{R_4 + R_3}v_{Icm} - i_2R_2$$

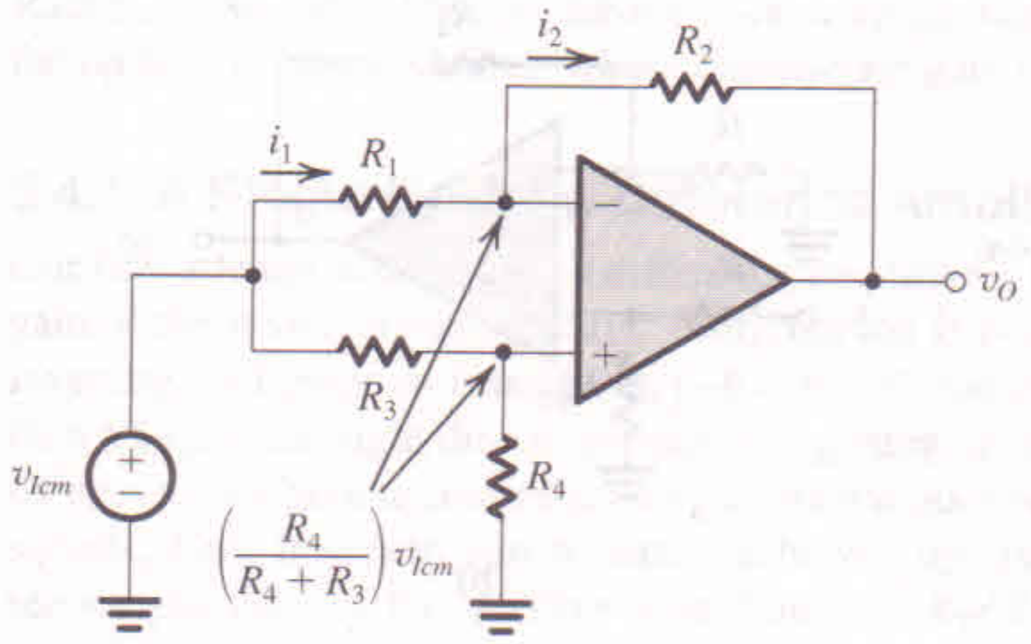

FIGURE 2.18 Analysis of the difference amplifier to determine its common-mode gain $A_{cm} \equiv v_O / v_{Icm}$.

Substituting $i_2 = i_1$ and for i_1 from Eq. (2.18),

$$v_O = \frac{R_4}{R_4 + R_3} v_{Icm} - \frac{R_2}{R_1}\frac{R_3}{R_4 + R_3} v_{Icm}$$

$$= \frac{R_4}{R_4 + R_3}\left(1 - \frac{R_2}{R_1}\frac{R_3}{R_4}\right) v_{Icm}$$

Thus,

$$A_{cm} \equiv \frac{v_O}{v_{Icm}} = \left(\frac{R_4}{R_4 + R_3}\right)\left(1 - \frac{R_2}{R_1}\frac{R_3}{R_4}\right) \tag{2.19}$$

For the design with the resistor ratios selected according to Eq. (2.15), we obtain

$$A_{cm} = 0$$

as expected. Note, however, that any mismatch in the resistance ratios can make A_{cm} nonzero, and hence CMRR finite.

In addition to rejecting common-mode signals, a difference amplifier is usually required to have a high input resistance. To find the input resistance between the two input terminals (i.e., the resistance seen by v_{Id}), called the **differential input resistance** R_{id}, consider Fig. 2.19. Here we have assumed that the resistors are selected so that

$$R_3 = R_1 \quad \text{and} \quad R_4 = R_2$$

Now

$$R_{id} \equiv \frac{v_{Id}}{i_I}$$

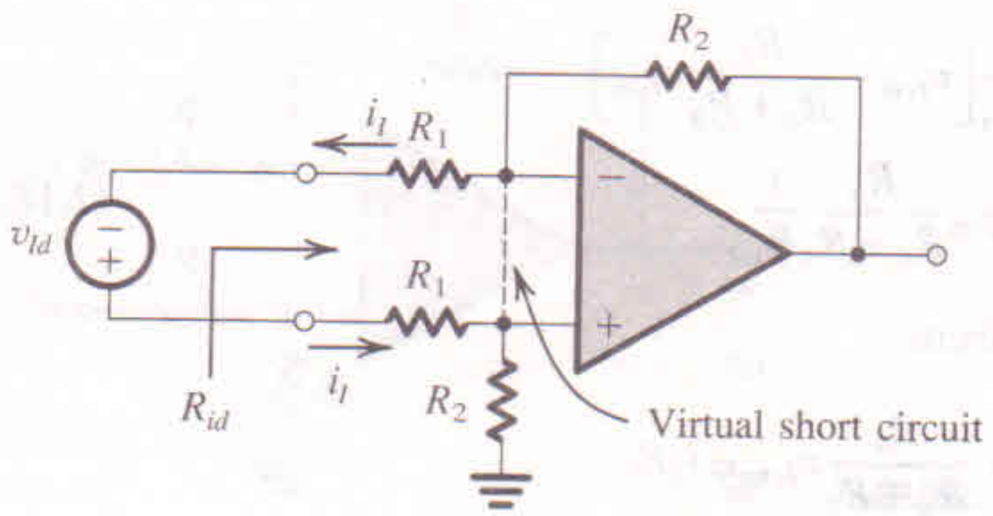

FIGURE 2.19 Finding the input resistance of the difference amplifier for the case $R_3 = R_1$ and $R_4 = R_2$.

Since the two input terminals of the op amp track each other in potential, we may write a loop equation and obtain

$$v_{Id} = R_1 i_1 + 0 + R_1 i_1$$

Thus,

$$R_{id} = 2R_1 \tag{2.20}$$

Note that if the amplifier is required to have a large differential gain (R_2/R_1), then R_1 of necessity will be relatively small and the input resistance will be correspondingly low, a drawback of this circuit. Another drawback of the circuit is that it is not easy to vary the differential gain of the amplifier. Both of these drawbacks are overcome in the instrumentation amplifier discussed next.

EXERCISES

2.15 Consider the difference-amplifier circuit of Fig. 2.16 for the case $R_1 = R_3 = 2\ \text{k}\Omega$ and $R_2 = R_4 = 200\ \text{k}\Omega$. (a) Find the value of the differential gain A_d. (b) Find the value of the differential input resistance R_{id} and the output resistance R_o. (c) If the resistors have 1% tolerance (i.e., each can be within ±1% of its nominal value), find the worst-case common-mode gain A_{cm} and the corresponding value of CMRR.

Ans. (a) 100 V/V (40 dB); (b) 4 kΩ, 0 Ω; (c) 0.04 V/V, 68 dB

D2.16 Find values for the resistances in the circuit of Fig. 2.16 so that the circuit behaves as a difference amplifier with an input resistance of 20 kΩ and a gain of 10.

Ans. $R_1 = R_3 = 10\ \text{k}\Omega$; $R_2 = R_4 = 100\ \text{k}\Omega$

2.4.2 A Superior Circuit—The Instrumentation Amplifier

The low-input-resistance problem of the difference amplifier of Fig. 2.16 can be solved by buffering the two input terminals using voltage followers; that is, a voltage follower of the type in Fig. 2.14 is connected between each input terminal and the corresponding input terminal of the difference amplifier. However, if we are going to use two additional op amps, we should ask the question: Can we get more from them than just impedance buffering? An obvious answer would be that we should try to get some voltage gain. It is especially interesting that we can achieve this without compromising the high input resistance simply by using followers-with-gain rather than unity-gain followers. Achieving some or indeed the bulk of the required gain in this new first stage of the differential amplifier eases the burden on the difference amplifier in the second stage, leaving it to its main task of implementing the differencing function and thus rejecting common-mode signals.

The resulting circuit is shown in Fig. 2.20(a). It consists of two stages. The first stage is formed by op amps A_1 and A_2 and their associated resistors, and the second stage is the by-now-familiar difference amplifier formed by op amp A_3 and its four associated resistors. Observe that as we set out to do, each of A_1 and A_2 is connected in the noninverting configuration and thus realizes a gain of $(1 + R_2/R_1)$. It follows that each of v_{I1} and v_{I2} is amplified by this factor, and the resulting amplified signals appear at the outputs of A_1 and A_2, respectively.

The difference amplifier in the second stage operates on the difference signal $(1 + R_2/R_1)(v_{I2} - v_{I1}) = (1 + R_2/R_1)v_{Id}$ and provides at its output

$$v_O = \frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right)v_{Id}$$

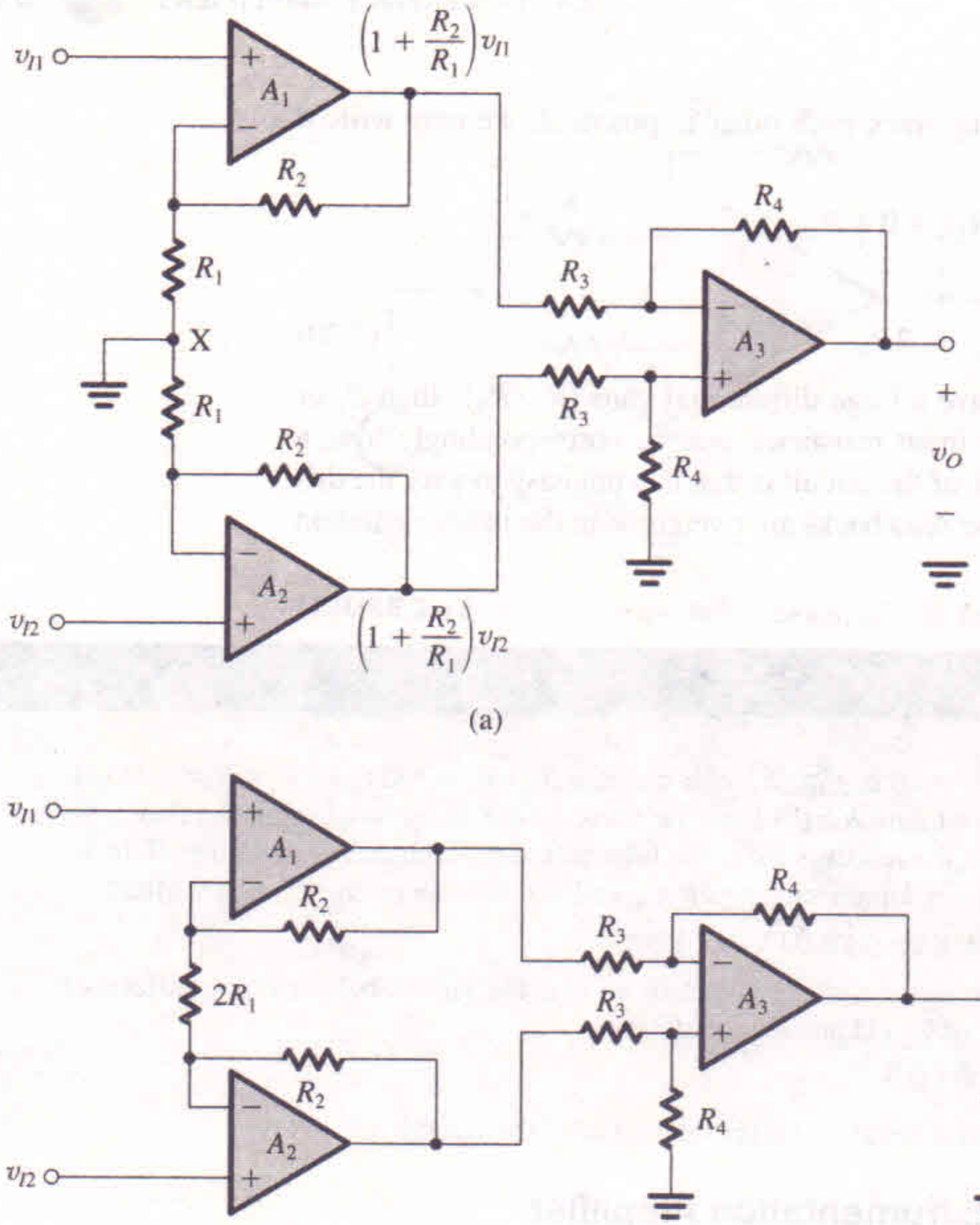

FIGURE 2.20 A popular circuit for an instrumentation amplifier: **(a)** Initial approach to the circuit; **(b)** The circuit in **(a)** with the connection between node X and ground removed and the two resistors R_1 and R_1 lumped together. This simple wiring change dramatically improves performance; **(c)** Analysis of the circuit in' **(b)** assuming ideal op amps.

Thus the differential gain realized is

$$A_d = \left(\frac{R_4}{R_3}\right)\left(1 + \frac{R_2}{R_1}\right) \tag{2.21}$$

The common-mode gain will be zero because of the differencing action of the second-stage amplifier.

The circuit in Fig. 2.20(a) has the advantage of very high (ideally infinite) input resistance and high differential gain. Also, provided that A_1 and A_2 and their corresponding resistors are matched, the two signal paths are symmetric—a definite advantage in the design of a differential amplifier. The circuit, however, has three major disadvantages:

1. The input common-mode signal v_{Icm} is amplified in the first stage by a gain equal to that experienced by the differential signal v_{Id}. This is a very serious issue, for it could result in the signals at the outputs of A_1 and A_3 being of such large magnitudes that the op amps saturate (more on op-amp saturation in Section 2.6). But even if the op amps do not saturate, the difference amplifier of the second stage will now have to deal with much larger common-mode signals, with the result that the CMRR of the overall amplifier will inevitably be reduced.
2. The two amplifier channels in the first stage have to be perfectly matched, otherwise a spurious signal may appear between their two outputs. Such a signal would get amplified by the difference amplifier in the second stage.
3. To vary the differential gain A_d, two resistors have to be varied simultaneously, say the two resistors labeled R_1. At each gain setting the two resistors have to be perfectly matched, a difficult task.

All three problems can be solved with a very simple wiring change: Simply disconnect the node between the two resistors labeled R_1, node X, from ground. The circuit with this small but functionally profound change is redrawn in Fig. 2.20(b), where we have lumped the two resistors (R_1 and R_1) together into a single resistor ($2R_1$).

Analysis of the circuit in Fig. 2.20(b), assuming ideal op amps, is straightforward, as is illustrated in Fig. 2.20(c). The key point is that the virtual short circuits at the inputs of op amps A_1 and A_2 cause the input voltages v_{I1} and v_{I2} to appear at the two terminals of resistor ($2R_1$). Thus the differential input voltage $v_{I2} - v_{I1} \equiv v_{Id}$ appears across $2R_1$ and causes a current $i = v_{Id}/2R_1$ to flow through $2R_1$ and the two resistors labeled R_2. This current in turn produces a voltage difference between the output terminals of A_1 and A_2 given by

$$v_{O2} - v_{O1} = \left(1 + \frac{2R_2}{2R_1}\right)v_{Id}$$

The difference amplifier formed by op amp A_3 and its associated resistors senses the voltage difference ($v_{O2} - v_{O1}$) and provides a proportional output voltage v_O:

$$\begin{aligned} v_O &= \frac{R_4}{R_3}(v_{O2} - v_{O1}) \\ &= \frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right)v_{Id} \end{aligned}$$

Thus the overall differential voltage gain is given by

$$A_d \equiv \frac{v_O}{v_{Id}} = \frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right) \tag{2.22}$$

Observe that proper differential operation does *not* depend on the matching of the two resistors labeled R_2. Indeed, if one of the two is of different value, say R_2', the expression for A_d becomes

$$A_d = \frac{R_4}{R_3}\left(1 + \frac{R_2 + R_2'}{2R_1}\right) \tag{2.23}$$

Consider next what happens when the two input terminals are connected together to a common-mode input voltage v_{icm}. It is easy to see that an equal voltage appears at the negative input terminals of A_1 and A_2, causing the current through $2R_1$ to be zero. Thus there will be no current flowing in the R_2 resistors, and the voltages at the output terminals of A_1 and A_2 will be equal to the input (i.e., v_{icm}). Thus the first stage no longer amplifies v_{icm}; it simply propagates v_{icm} to its two output terminals, where they are subtracted to produce a zero common-mode output by A_3. The difference amplifier in the second stage, however, now has a much improved situation at its input: The difference signal has been amplified by $(1 + R_2/R_1)$ while the common-mode voltage remained unchanged.

Finally, we observe from the expression in Eq. (2.22) that the gain can be varied by changing only one resistor, $2R_1$. We conclude that this is an excellent differential amplifier circuit and is widely employed as an instrumentation amplifier; that is, as the input amplifier used in a variety of electronic instruments.

EXAMPLE 2.3

Design the instrumentation amplifier circuit in Fig. 2.20(b) to provide a gain that can be varied over the range of 2 to 1000 utilizing a 100-kΩ variable resistance (a potentiometer, or "pot" for short).

Solution

It is usually preferable to obtain all the required gain in the first stage, leaving the second stage to perform the task of taking the difference between the outputs of the first stage and thereby rejecting the common-mode signal. In other words, the second stage is usually designed for a gain of 1. Adopting this approach, we select all the second-stage resistors to be equal to a practically convenient value, say 10 kΩ. The problem then reduces to designing the first stage to realize a gain adjustable over the range of 2 to 1000. Implementing $2R_1$ as the series combination of a fixed resistor R_{1f} and the variable resistor R_{1v} obtained using the 100-kΩ pot (Fig. 2.21), we can write

$$1 + \frac{2R_2}{R_{1f} + R_{1v}} = 2 \text{ to } 1000$$

Thus,

$$1 + \frac{2R_2}{R_{1f}} = 1000$$

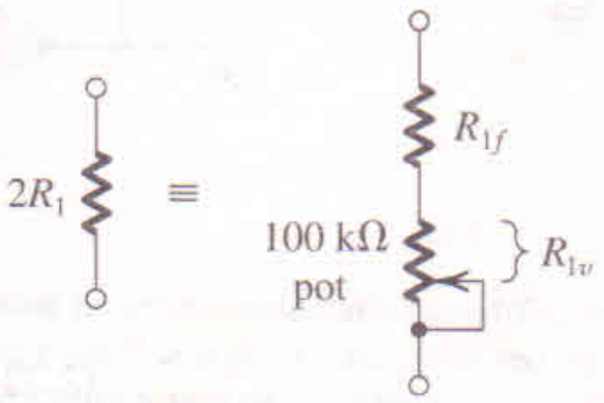

FIGURE 2.21 To make the gain of the circuit in Fig. 2.20(b) variable, $2R_1$ is implemented as the series combination of a fixed resistor R_{1f} and a variable resistor R_{1v}. Resistor R_{1f} ensures that the maximum available gain is limited.

and

$$1 + \frac{2R_2}{R_{1f} + 100\ \text{k}\Omega} = 2$$

These two equations yield $R_{1f} = 100.2\ \Omega$ and $R_2 = 50.050\ \text{k}\Omega$. Other practical values may be selected; for instance, $R_{1f} = 100\ \Omega$ and $R_2 = 49.9\ \text{k}\Omega$ (both values are available as standard 1%-tolerance metal-film resistors; see Appendix G) results in a gain covering approximately the required range.

EXERCISE

2.17 Consider the instrumentation amplifier of Fig. 2.20(b) with a common-mode input voltage of +5 V (dc) and a differential input signal of 10-mV-peak sine wave. Let $(2R_1) = 1\ \text{k}\Omega$, $R_2 = 0.5\ \text{M}\Omega$, and $R_3 = R_4 = 10\ \text{k}\Omega$. Find the voltage at every node in the circuit.

Ans. $v_{I1} = 5 - 0.005 \sin \omega t$; $v_{I2} = 5 + 0.005 \sin \omega t$; v_- (op amp A_1) $= 5 - 0.005 \sin \omega t$; v_- (op amp A_2) $= 5 + 0.005 \sin \omega t$; $v_{O1} = 5 - 5.005 \sin \omega t$; $v_{O2} = 5 + 5.005 \sin \omega t$; $v_-(A_3) = v_+(A_3) = 2.5 + 2.0025 \sin \omega t$; $v_O = 10.01 \sin \omega t$ (all in volts)

2.5 EFFECT OF FINITE OPEN-LOOP GAIN AND BANDWIDTH ON CIRCUIT PERFORMANCE

Above we defined the ideal op amp, and we presented a number of circuit applications of op amps. The analysis of these circuits assumed the op amps to be ideal. Although in many applications such an assumption is not a bad one, a circuit designer has to be thoroughly familiar with the characteristics of practical op amps and the effects of such characteristics on the performance of op-amp circuits. Only then will the designer be able to use the op amp intelligently, especially if the application at hand is not a straightforward one. The nonideal properties of op amps will, of course, limit the range of operation of the circuits analyzed in the previous examples.

In this and the two sections that follow, we consider some of the important nonideal properties of the op amp.[3] We do this by treating one parameter at a time, beginning in this section with the most serious op-amp nonidealities, its finite gain and limited bandwidth.

2.5.1 Frequency Dependence of the Open-Loop Gain

The differential open-loop gain of an op amp is not infinite; rather, it is finite and decreases with frequency. Figure 2.22 shows a plot for $|A|$, with the numbers typical of most commercially available general-purpose op amps (such as the 741-type op amp, which is available from many semiconductor manufacturers and whose internal circuit is studied in Chapter 9).

[3] We should note that real op amps have nonideal effects additional to those discussed in this chapter. These include finite (nonzero) common-mode gain or, equivalently, noninfinite CMRR, noninfinite input resistance, and nonzero output resistance. The effect of these, however, on the performance of most of the closed-loop circuits studied here is not very significant, and their study will be postponed to later chapters (in particular Chapters 8 and 9). Nevertheless, some of these nonideal characteristics will be modeled in Section 2.9 in the context of circuit simulation using SPICE.