EE224: Mid-semester Test

22 February 2014, 1100-1300 hrs

1. (2 marks) Using NMOS and PMOS transistors, construct a three-input gate which implements the function $\overline{(A+B).C}$.

   - The pull-down network implements $(A+B).C$. Thus, it consists of a series combination of: a parallel pair of NMOS transistors (controlled by A and B), and a single NMOS transistor controlled by C. The pull-up network implements $(\overline{A}.\overline{B}) + \overline{C}$. Thus, it consists of a parallel combination of: a series chain of PMOS transistors controlled by A, B, and a single PMOS transistor controlled by C.

2. (2 marks) You are given a two-input logic gate with inputs x_1, x_2 and output y whose behaviour is described as follows: the input values x_1, x_2 are treated as integers in $\{0, 1\}$, and the output y is 1 if and only if the following inequalities are satisfied.

$$\begin{aligned} x_1 + x_2 &> 1/2 \\ x_1 + x_2 &< 3/2 \end{aligned}$$

   What Boolean function does the gate implement?

   - The function evaluates to 1 for the input combinations $0, 1$ and $1, 0$. Thus, it is a two variable XOR.

3. (5 marks) Using only two-input NAND gates and inverters, construct a circuit which compares two 8-bit numbers $X = x_7x_6 \ldots x_0$ and $Y = y_7y_6 \ldots y_0$ and produces an output of 1 if and only if $X < Y$. Assuming that each gate has a unit delay, what is the maximum delay through your circuit?

- Several solutions are possible: A recursive divide/conquer circuit can be constructed using the decomposition:

$$x_7 \ldots x_0 = y_7 \ldots y_0$$

if and only if

$$\begin{aligned} x_7 \ldots x_4 &= y_7 \ldots y_4 \\ x_3 \ldots x_0 &= y_3 \ldots y_0 \end{aligned}$$

are both true. Further

$$x_7 \ldots x_0 > y_7 \ldots y_0$$

if and only if

$$x_7 \ldots x_4 > y_7 \ldots y_4$$

OR

$$(x_7 \ldots x_4 = y_7 \ldots y_4)\ AND\ (x_3 \ldots x_0 > y_3 \ldots y_0)$$

Repeat this decomposition and you get a 3-deep tree of single-bit comparators, each of which has inputs x, y and outputs $e = x \oplus y$, $g = x.\overline{y}$. The maximum delay from input to output of this single-bit comparator is 3 units (implement the XOR using five NAND2 gates as in the homework). The maximum input-output delay of the circuit is then 9 units.

4. (2 marks) Given two functions f, g, under what conditions can we write $f = g.h$ for some Boolean function h? Show that $x_1 \oplus x_2 \oplus x_3$ is divisible by $x_1 + x_2 + x_3$.

   - It must be the case that $g = 1$ whenever $f = 1$. It is easy to check that this is true in this particular example).

5. (5 marks) Let $f = x_1 \oplus x_2 \oplus x_3$, and

$$g = (x_1 + x_2 + x_3)$$

   Find the simplest possible function of x_1, x_2, x_3 (smallest sum-of-products formula) h such that $f = g.h$.

   - We wish to write f as a function of x_1, x_2, x_3, g. If we use a Karnaugh map of four variables

x3,g \ x1,x2	00	01	11	10
00		d	d	d
01	d	1		1
11	1		1	
10	d	d	d	d

where the dont-cares are due to the fact that some of the combinations are not possible (e.g. $x_1 = x_2 = x_3 = 0$, $g = 1$). The best h is then

$$x_1.x_2.x_3 + \overline{x_1}.\overline{x_2} + \overline{x_1}.\overline{x_3} + \overline{x_2}.\overline{x_3}$$

6. (4 marks) For a CMOS inverter with $\beta_P = 2 \times \beta_N$, find the switching point, and the left unity gain point (Assume that $V_{DD} = 1V$ and $V_T = 0.3V$).

   - Solve as in the assignment. The switching point and the left unity gain point should move to the right (when compared with that obtained in the balanced case).