Homework Lecture 2

1. Exercise A.28

Design a circuit that produces a 1 at the output Z when the input X changes from 0 to 1 or from 1 to 0 and produces a zero at all other times. For the initial state, assume a 0 was last seen at the input. Show the state diagram, state table and the SOP form solution and realization.

=====notes:

"**changes from 0 to 1**" should be interpreted as the "in previous clock cycle the input was 0 (at active edge of clock) and the current input value is 1". (Mealy FSM)

In the assignment in the book the last sentence it is mentioned to use MUXes. That is not required, a SOP solution and realization is expected.

2. Exercise A.29

Design an FSM that has as output the value 1 when:

a) In the previous 2 clock cycles the value 0 followed the value 1 is read (at active edges of the clock) and the current input value is 1
   or
b) In the previous 2 clock cycles the value 1 followed the value 1 is read (at active edges of the clock) and the current input value is 0

else the output is 0.

You do not have to design the logic.

3. Exercise A.36

Given the following functions, construct the Karnaugh map and find the simplified SOP form for f and g.

$f(A,B,C,D) = 1$ when two or more inputs are 1, otherwise $f(A,B,C,D) = 0$

$g(A,B,C,D) = 1$ when the number of inputs that are 1 is even (including all inputs 0),
otherwise $g(A,B,C,D) = \overline{f(A,B,C,D)}$

4. Exercise A37

Simplify using Karnaugh map

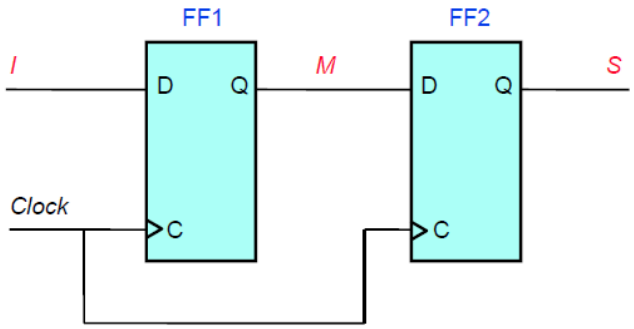
$$f(A,B,C,D) = \sum m(2,8,10,11) + \sum_{d} m(0,9)$$

(only SOP-form)

5. Exercise A.38

Given a logic circuit. Is it possible to generate a truth table that contains don't cares for that circuit? Explain your answer.

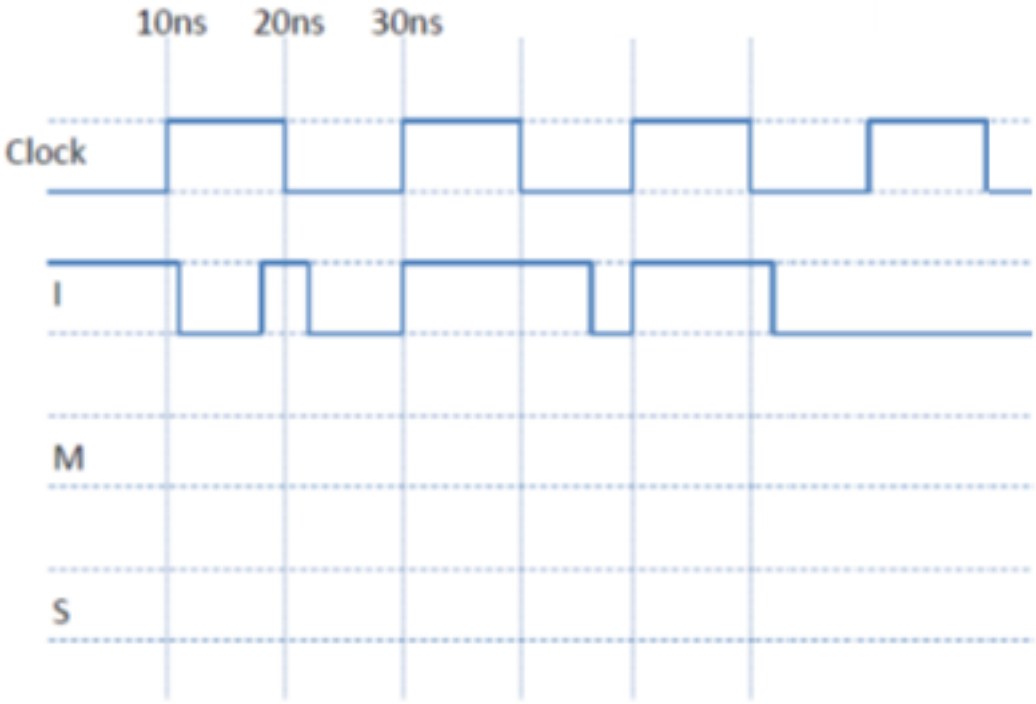
6. Exercise: 2 Flip-Flops in series



In this exercise 2 flip-flops (FFs) are placed in series; they have the following timing properties:

- Setup time T_{su} = 6 ns,
- Hold time T_h = -2 ns,
- Clock-to-output delay T_{co} = 3 ns.

It can be assumed the wires have no delay and that the initial values of both FFs are 0. We also assume ideal edges; transitions are instantaneous from 0→1 and 1→0. Below, a diagram is given with a clock signal with a period of 20ns and input signal I, these corresponds to the labels in the circuit above.



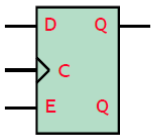
a) Describe what the setup time, hold time and clock-to-output delay of a flip flop is.
b) Show with vertical lines the setup, hold and clock-to-output delay for the first clock period in the diagram.
c) Given the clock and input signal, draw the waveform for M and S. At 0ns M and S are both 0.

7. Exercise: realize a DE flipflop

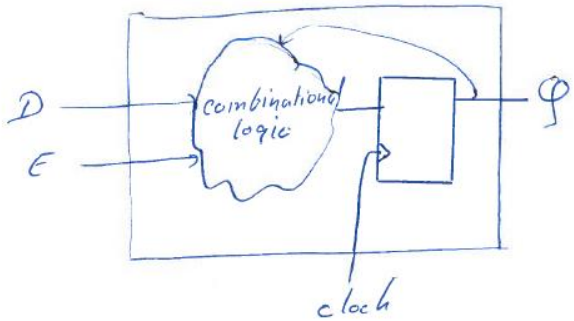
DE flip-flop

° DE flip-flop is D flip-flop with enable **E**; when **E=0** flip-flop output is unchanged. When **E=1** flip-flop behaves as D flip-flop

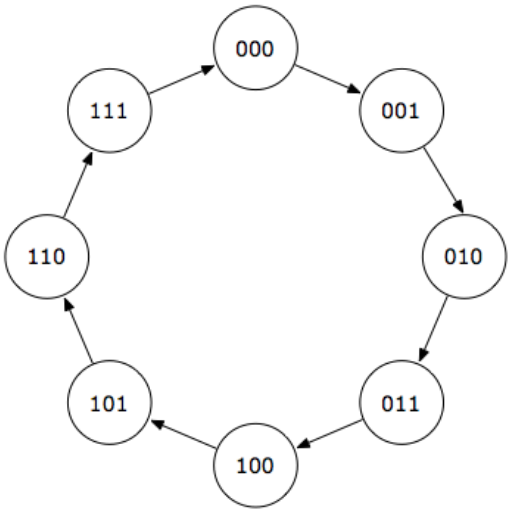
E	D	Q+	
0	0	Q	Unchanged
0	1	Q	Unchanged
1	0	0	Reset
1	1	1	Set



Realize the DE flip-flop with a D flip-flop and combinational logic.



Exercise 8



Given is an FSM with 8 states. This is a synchronous counter. The system has no inputs (except the clock input). At each active edge it goes to the next state. The system is realized with 3 D flip-flops, Q_2, Q_1 and Q_0. (The flip-flop outputs are also the outputs of the system).

Give simplified Boolean equations for the combinational logic for the data inputs of these flip-flops in SOP form.

Exercise 9

Design a synchronous MOORE system with 1-bit input *I* and 1-bit output *Y*. The system also has a clock (*CLK*) and asynchronous low active reset input (*RST_N*).

The output *Y* is for the duration of one clock period 1when the input *I* is 1 at the rising edge of the *CLK* and at the previous rising edge of the *CLK* the input was 0.

Note: it is assumed that a change of the input does not violate the setup and hold conditions of the flip-flops.

a) Draw an FSM for this system (using meaningful names for the states!).
b) D flip-flops and binary encoding for the states are used. Determine the Boolean equations (SOP-form) for the combinational logic (input of D flip-flops and output). (You must derive this from the FSM.)
c) Draw the schematic