Aashutosh Taikar

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Education

OREGON STATE UNIVERSITY
MEng in Electrical and Computer Engineering
Dec 2018 | Corvallis, OR
GPA: 3.25/4.0
Mixed Signal Validation Application Development | Embedded Software Development

MUMBAI UNIVERSITY
BE in Electronics and Telecom
May 2015 | Mumbai, India

Links

Github:// **aashutoshtaikar**
LinkedIn:// **aashutoshtaikar**

Coursework

Analog CMOS Integrated Circuits
CMOS Integrated Circuits-1
Contemporary Energy Applications
Intro to Parallel Programming
High Performance Computer Architecture
Computer Architecture
Advanced Computer Networking
Interconnection Networks
Distributed Systems
Human Computer Interaction

Skills

Programming languages
•C/C++(STL,Qt) • C#/VB.Net •Bash
•Python

CAD Tools:
•Cadence Virtuoso •Allegro OrCad
•Diptrace • Proteus •LTspice

Protocols:
GPIB, I2C, SPI, UART, CAN, PCIe

Research(survey)

•Overview of SSDs and parallelism in SSD controller

Experience

On Semiconductor | Technology Reliability Applications Intern
Jun 2018 – Sep 2018 | Pocatello, Idaho
Project: In-Situ Parametric Test System for process Reliability
• Designed schematic for the Control board containing extensive relays, shift registers to test DUTs(Device Under Test) controlled via DAQ
• Developed an application in VB.Net and National Instruments GPIB/VISA,DAQ libraries which controls 12 Power Supplies(Keithley 2400 Source Meter Unit) and an oven for stress test via GPIB interface, control board and functions as per the user input and selected DUTs
• Performed Wafer / Device level testing using Keithley Parametric Test System, Oscilloscope and DMM.

Oregon State University | Graduate Teaching Assistant
Mar 2018 – June 2018 | Corvallis, Oregon | C++, OpenMP, OpenCL, SIMD
CS-475/575 Intro to Parallel Programming - Code debugging and Solved doubts during office hours

Continuum Managed Solutions | Network Support Engineer
Oct 2015 – June 2016 | Mumbai, India
Maintaining windows server network, checking server event logs, Created bat scripts for troubleshooting server windows network services

Projects

OpAmp Design
Spring 18 | Analog CMOS Integrated Circuits | Cadence Virtuoso
Designed 2 stage telescopic cascode OpAmp: Closed Loop gain = 5; CL=2pf; Settling Time = 30nS for 0.01% settling; VDD = 1.8V
Fall 17 | CMOS/Mixed Signal Integrated Circuits | Cadence Virtuoso
Designed a miller compensated 2 stage differential Amplifier for the following specs: CL=5pf; VDD = 0.9V, VSS = -0.9V; Open Loop gain>=65dB; Phase Margin >=60

Autocorrelation using OpenMP, SIMD and OpenCL | C++
Spring17 | Parallel Programming
Reads a random signal file, runs the Autocorrelation function on multiple threads using OpenMP. The same is implemented using the SIMD and OpenCL.

Link Management Protocol - Control Channel - Finite State Machine | C
Winter17 | Advanced Computer Networking
Implemented a part of the LMP protocol, which is the Control Channel Finite State Machine(FSM) described in RFC4204 using socket programming by studying 5 states and 17 events of the FSM.

Cache Simulation | Booksim(Cycle Accurate Simulator)
| Spring17 | Computer Architecture
•least-recently-used (LRU) replacement policy,32 to 512 sets, 1-way to 8-way associativity, 16-byte cache lines. • least-recently-used (LRU) replacement policy, 16-byte cache lines (block size), Sets/associativity combinations: 128/1, 128/2, 128/4, 2048/1, 2048/2, 2048/4, (Only L1 caches assumed present).

FARMBOT-Agricultural Automation robot | Diptrace | Proteus | C
| March15 | Undergrad Final Project
Created Schematics and Code for 8-bit micro-controller for actuation of a prototype bot which can perform basic farming functions for acquiring data from IR sensor using ADC and controlling motor driver ICs by PWM.